P/O/E/T/S

CENTER FOR POWER OPTIMIZATION OF ELECTRO-THERMAL SYSTEMS

Materials Enabling Higher Heat Fluxes for Components with the Goal of Improved Thermal Management

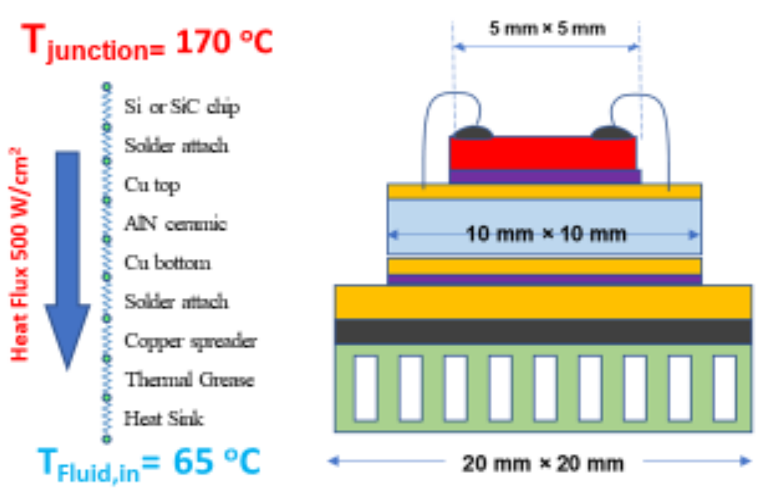
Hansen Qiao and Katherine Jiang (Stanford University), Bakhtiyar Mohammad Nafis (University of Arkansas)
Advisor: Prof. Kenneth E. Goodson (Stanford University)
Faculty Collaborators: Adjunct Prof. M. Asheghi, Prof. E. Pop (Stanford University); Prof. D. Huitink (University of Arkansas)

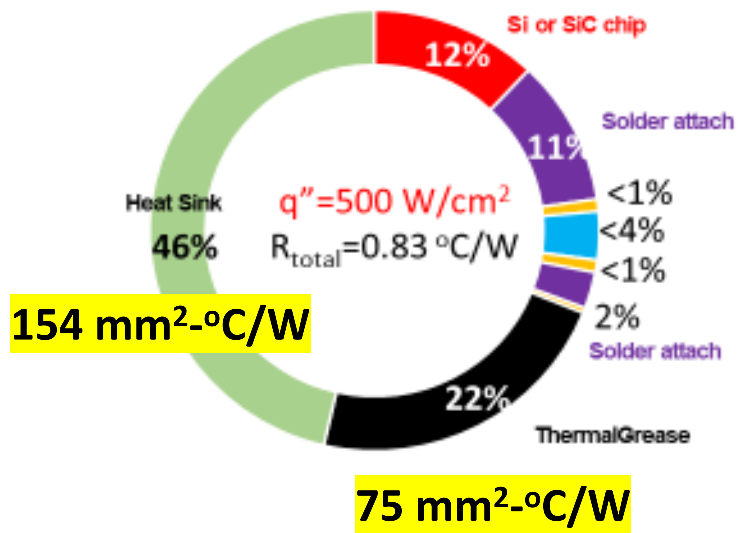
2022 Annual Meeting

October 18 – Noon to 2:00pm PDT

Thermal Resistance Contributions of Power Electronics Packaging Components

Center Goal: Compared with current state-of-the-art, the POETS center will create integrated electrothermal systems with a >10X improvement in 3 dimensional power density. We will develop new materials & fabrication techniques, system architectures, design methodologies, and operational strategies.

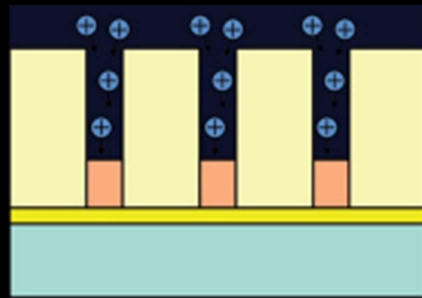




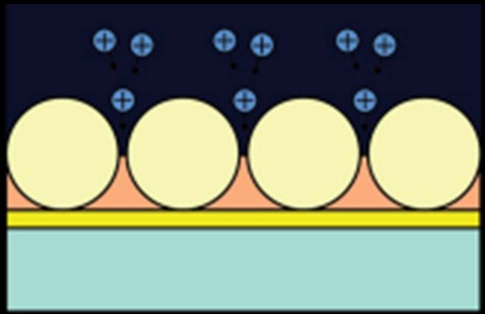
Material/Layer	Area (mm²)	Thickness (mm)	Thermal Conductivity (W/mK)	Thermal Resistance R" (cm²-°C/W)	Thermal Resistance R (°C/W)
Si or SiC chip	5×5	0.30	120	0.025	0.100
Sn4Ag Solder attach	5×5	0.10	45	0.022	0.089
DBC Top Copper	10×10	0.30	398	0.008	0.008
DBC AlN Substrate	10×10	0.50	170	0.029	0.029
DBC Bottom Copper	10×10	0.3	400	0.008	0.008
Sn4Ag Solder attach	10×10	0.1	50	0.022	0.022
Copper heat spreader	20×20	0.5	400	0.013	0.003
Thermal Grease	20×20	0.3	4	0.750	0.188
Heat Sink, R" (cm²-°C/W)=1.543	20×20	20		1.543	0.386
					0.832 (total)

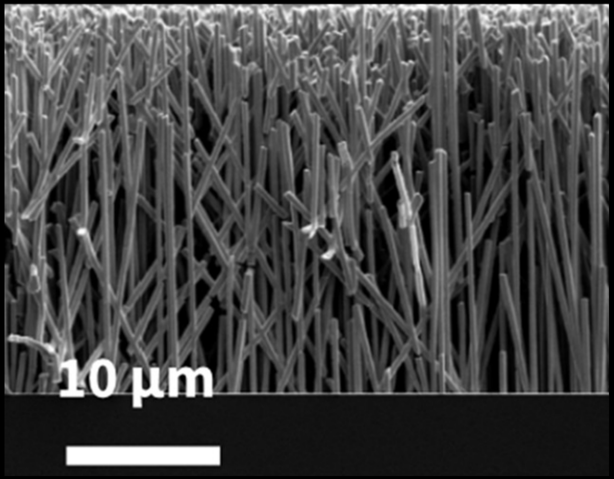
Materials Enabling Higher Heat Fluxes

Metal Nanowires

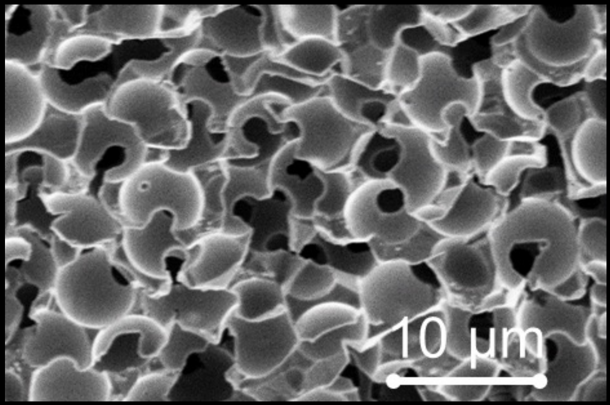


Metal Inverse Opals





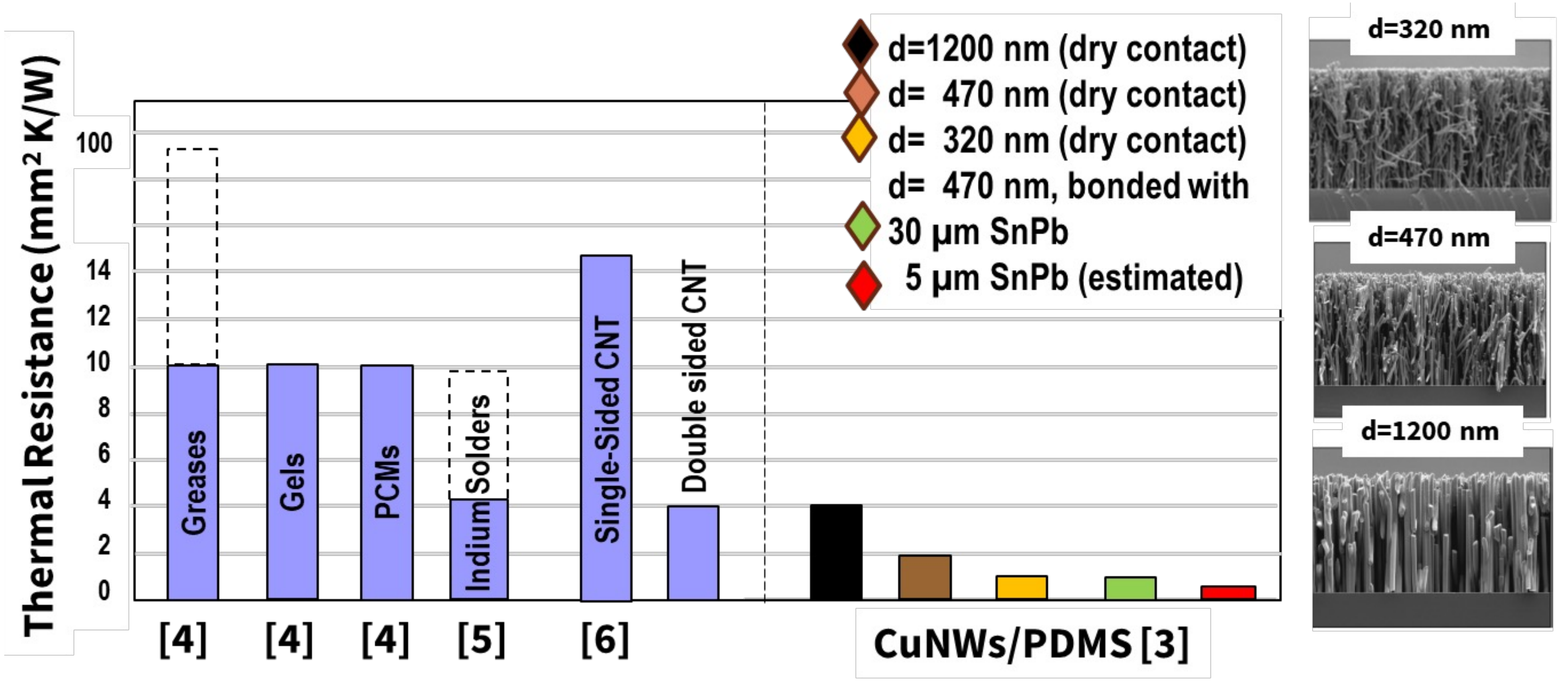
Barako, Goodson et al. Nanoletetrs (2015)



Application: Thermal interface materials and composites
Template: Porous dielectric membranes
Polycarbonate track-etched (PCTE) membranes
Anodic aluminum oxide (AAO) membrane
Characteristic Geometry: $D_{nanowire}$ 100 nm to 10 µm, L=1-60 µm , V_{metal}=1% to 50%

Application: high Thermal conductivity and permeability porous structure
Template: Closed-packed nano/micro-spheres (an "opal"), Polystyrene, Paraffin etc. Assembled by vertical deposition
Characteristic Geometry: $D_{nanowire}$ 100 nm to 10 µm, L=1-60 µm , V_{metal}=26% to 45%

Comparison of thermal resistance of State-of-the-Art commercial and laboratory demo thermal interface materials

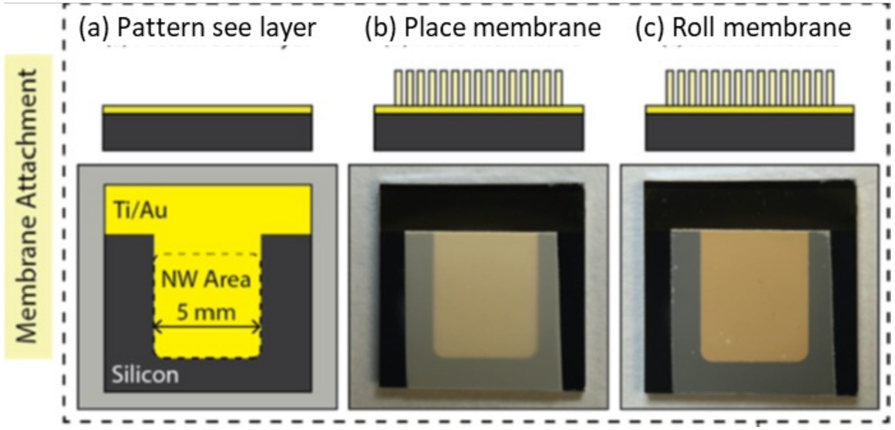


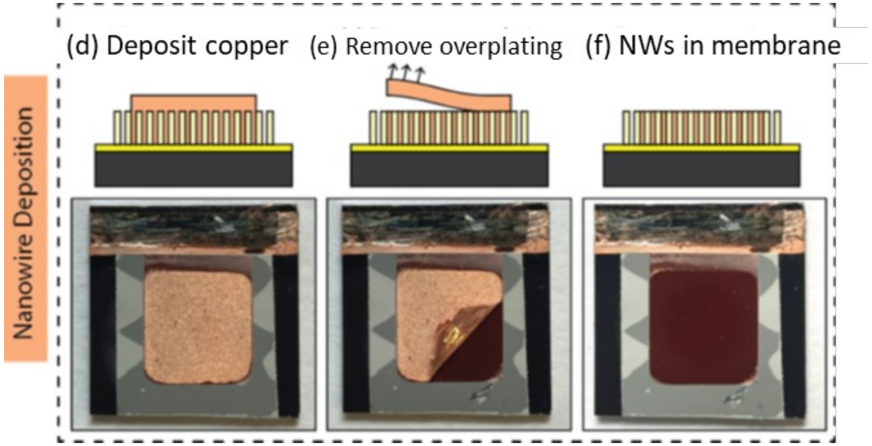
Comparison of thermal resistance of State-of-the-Art commercial and laboratory demo [4] thermal interface materials (CNT: carbon nanotubes, PCM: phase-change material; greases, gels, PCMs: [4]; Indium solders [5], CNTs: [6], with that of the proposed CuNWs/PDMS TIMs tape (1 cm^2). The thermal resistance of the CuNWs/PDMS composite of various nanowire volume fractions and diameters (dry contact: 320 ♦, 470 ♦, 1190 ♦, and 470 nm ♦ bonded with 30 μm thick SnPb). The SnPb bonded CuNWs/PDMS composite performs better although the thermal resistances are nearly a factor 2-4 smaller than the stand-alone (without filler) CuNWs [1]. The CuNWs/PDMS TIMs tape performs a factor of 4 better than CNTs [6], with a potential to achieve thermal resistances as low as 0.5 mm^2-K/W ♦.

Fabrication steps for CuNW/PDMS Composite on Silicon Substrate

Sacrificial membrane attachment (a~c)

- Patterned Au seed layer deposited on silicon substrate;
- Sacrificial porous polycarbonate track-etched (PCTE) film electrostatically adhered to surface and rolled flat
- 200~1000nm pores in PCTE film



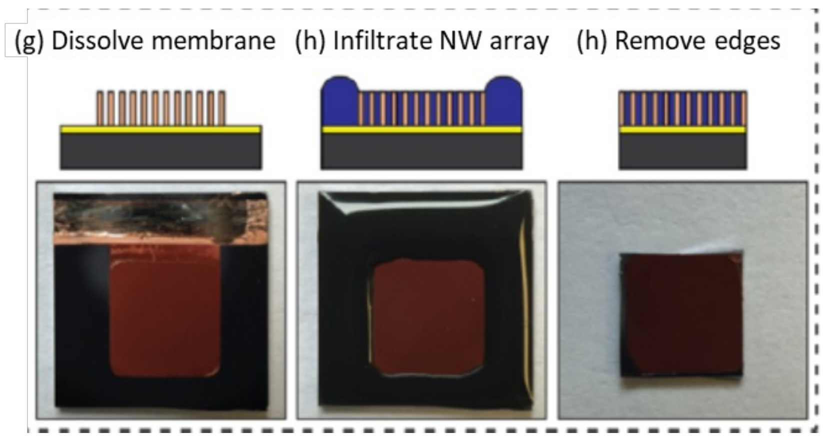


Copper nanowire growth (d~f)

- Electrodeposition of copper through pores & overplating on top of PCTE membrane
- Extra copper layer peeled off after deposition

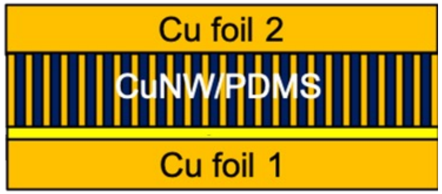
PDMS infiltration (g~i)

- PCTE template dissolved for freestanding CuNW
- PDMS infiltration from edge to center through capillary force

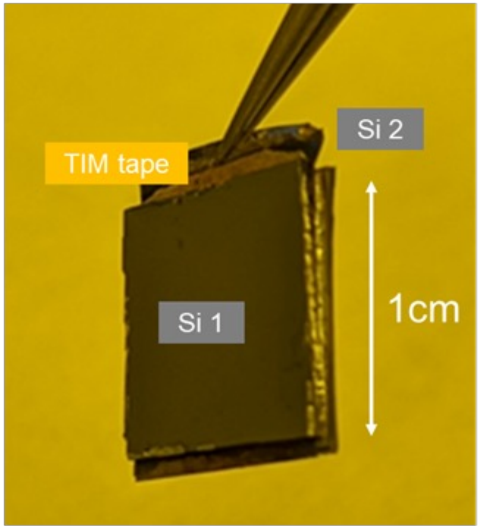


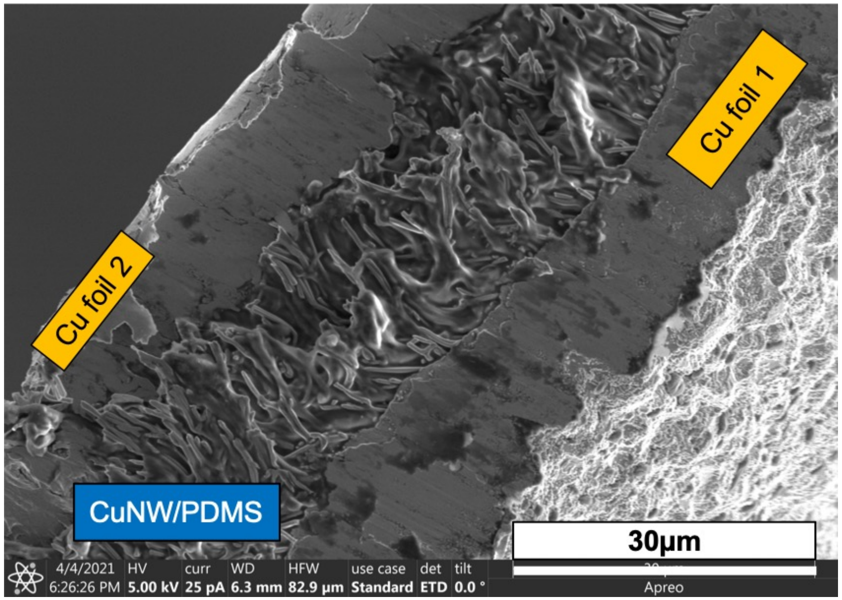
Barako, M. T., Isaacson, S. G., Lian, F., Pop, E., Dauskardt, R. H., Goodson, K. E., & Tice, J. (2017). Dense vertically aligned copper nanowire composites as high performance thermal interface materials. *ACS applied materials & interfaces*, *9*(48), 42067-42074. https://nanoheat.stanford.edu/sites/default/files/publications/2017-Barako.pdf

R3.032.20: Development of Copper Nanowires (CuNWs) Thermal Interface Materials (TIMs) with (Cu,Ni) – Sn Transient Liquid Phase (TLP) Bonding for High-Temperature Power Electronics Applications



TIM "tape" with ~24μm for CuNW/PDMS layer and 2x 15μm Cu foil

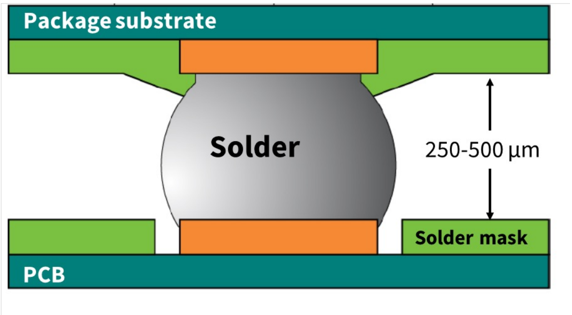




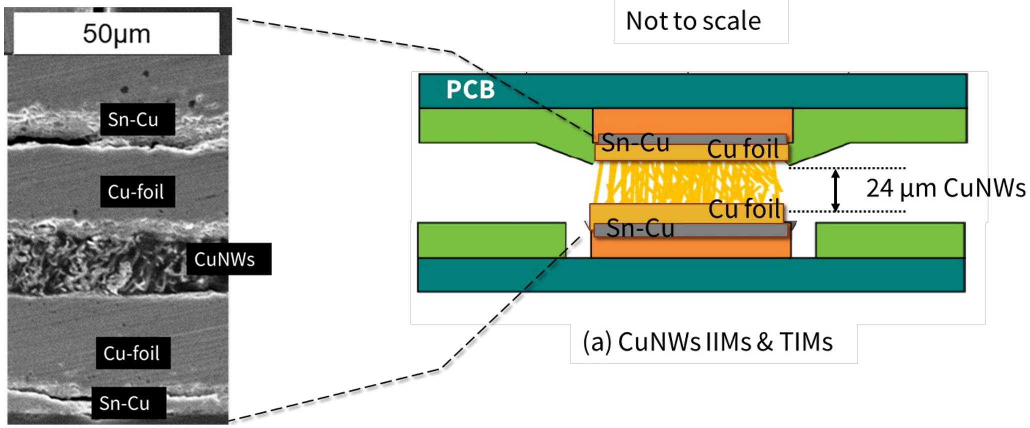
Graduate Students: Hansen Qiao (Stanford University); Advisor: Prof. Kenneth E. Goodson (Stanford University), Faculty Collaborators: Adjunct Prof. M. Asheghi, Prof. E. Pop (Stanford University); Prof. D. Huitink (University of Arkansas)

R3.038.22 Replacing the Solder Ball Technology: Development of a Compliant Electrical (EIMs) and Thermal Interface Materials (TIMs) Interconnects using Copper Nano-wire (CuNWs) (New Project)

Graduate Students: Hansen Qiao (Stanford), Katherine Jiang (Stanford), Bakhtiyar Mohammad Nafis (UArk)
Advisor: Prof. Kenneth E. Goodson (Stanford), Adjunct Prof. M. Asheghi (Stanford), Prof. D. Huitink (UArk), Prof. E. Pop (Stanford)

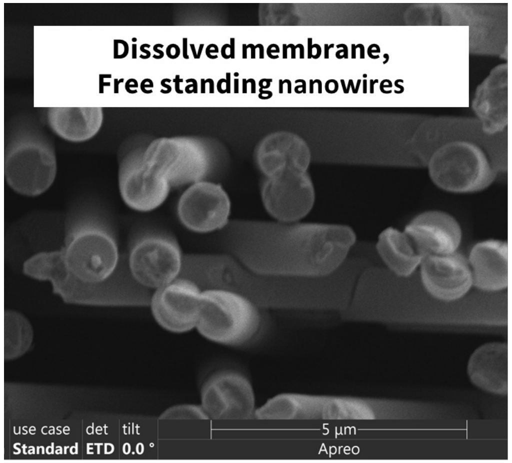


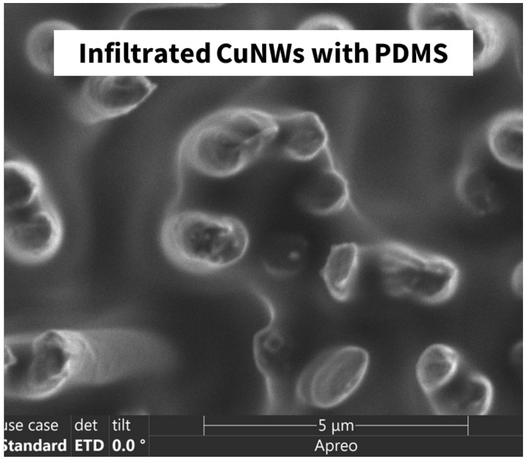
(b) CuNWs IIMs & TIMs



(a) CuNWs IIMs & TIMs

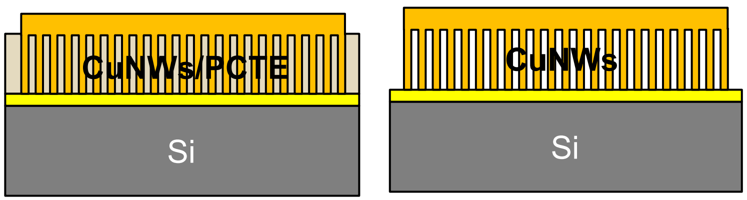
- In the previous Approach, some of the nanowire tips were covered by PDMS after infiltration
- Imperfect or poor electrical, thermal and mechanical contact connection between CuNWs and the 2nd Cu foil.

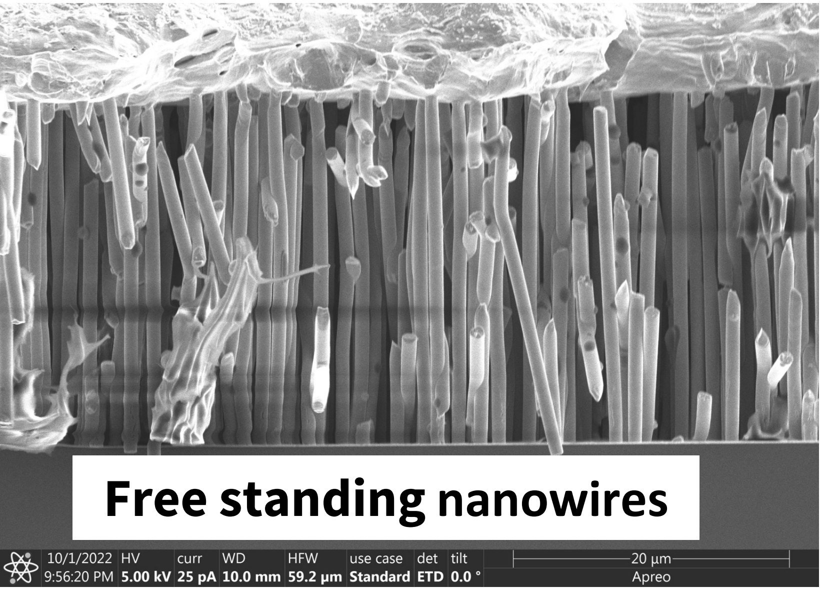




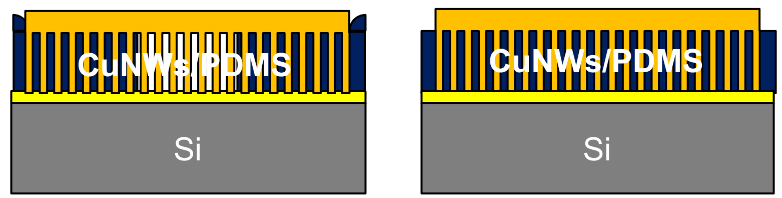
Development of the Gen#2 Flexible CuNWs Interconnects

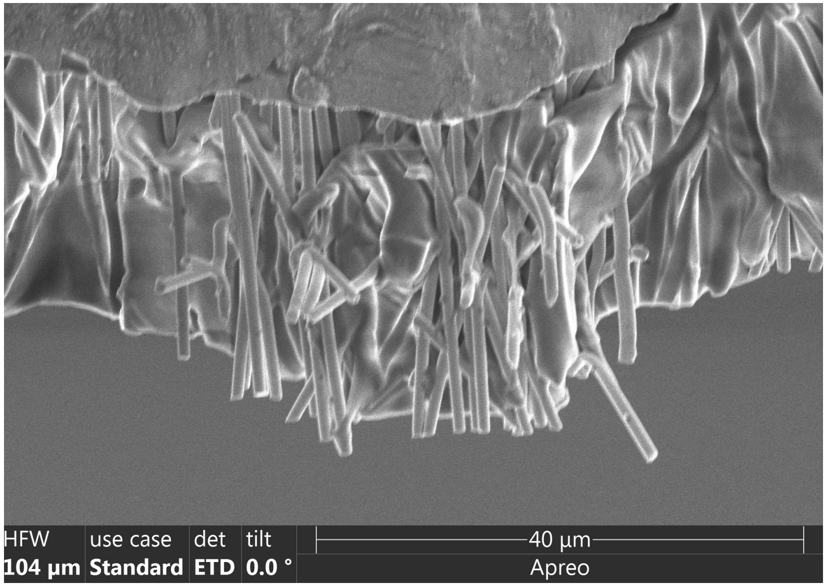
Dissolved PCTE without removing the overpalted Cu foil





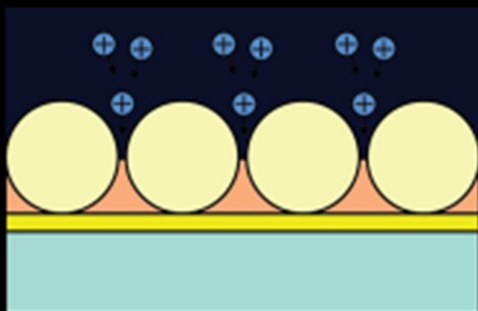
PDMS infiltrated in the CuNWs without removing the overpalted Cu foil

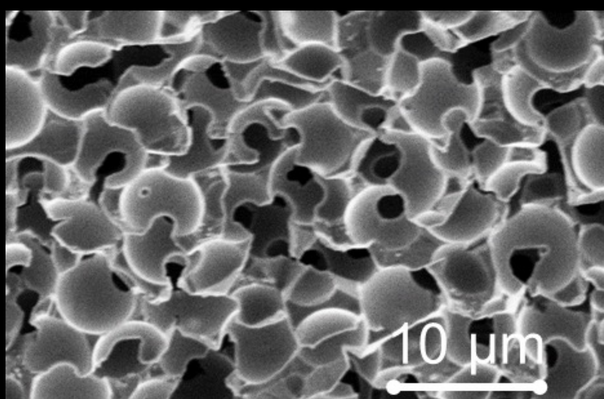


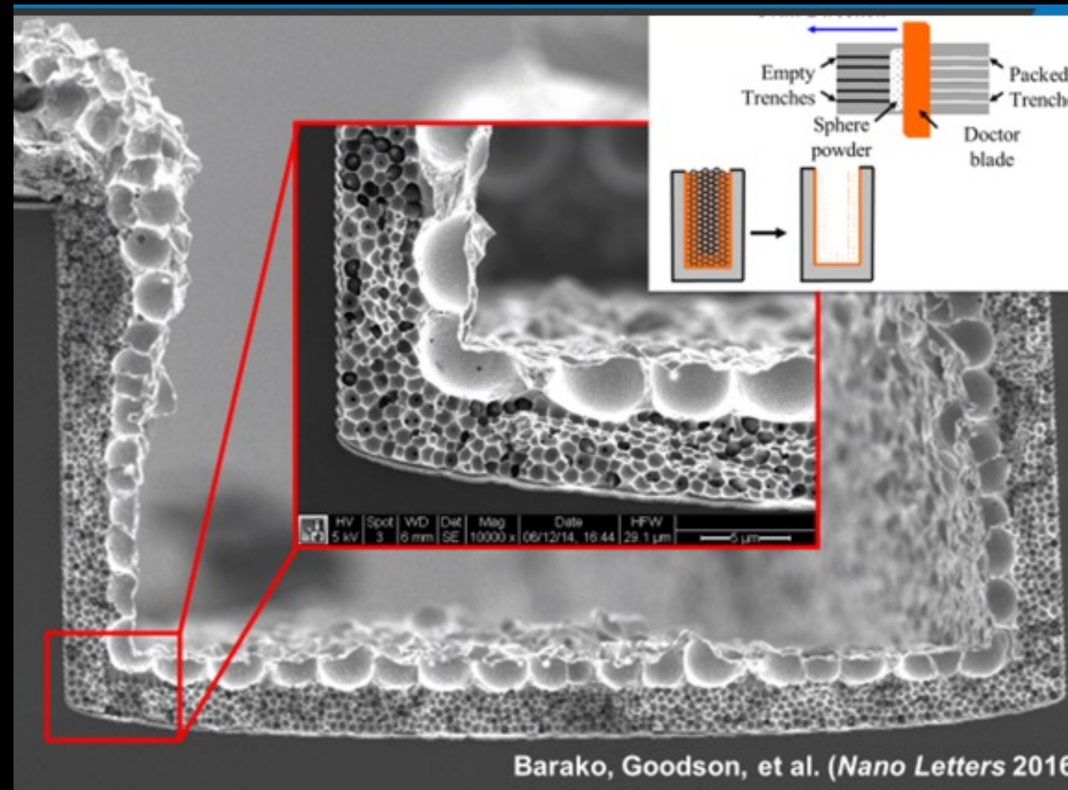


Materials Enabling Higher Heat Fluxes

Metal Inverse Opals







Barako, Goodson, et al. (*Nano Letters* 2016)

<u>Application: </u>high Thermal conductivity and permeability porous structure
<u>Template: </u>Closed-packed nano/micro-spheres (an “opal”), Polystyrene, Paraffin etc.
Assembled by vertical deposition

R3.023.18: Development of a High Performance μ-cooler (0.01 cm^2-^{o}C/W at <1 kW/cm^2) …

Dr. Heungdong Kwon, Qianying Wu, Sougata Hazra, Dr. Chi Zhang , Katherine Jiang, Adjunct Prof. Mehdi Asheghi,Prof. Ken Goodson

“Convective-based” vs. “Capillary-based cooling”

Micro-coolers: Combinations of different Wicks and 3D-Manifolds

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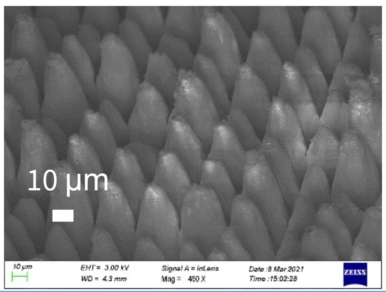
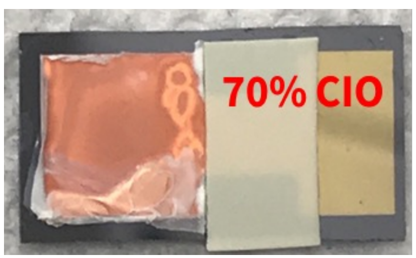
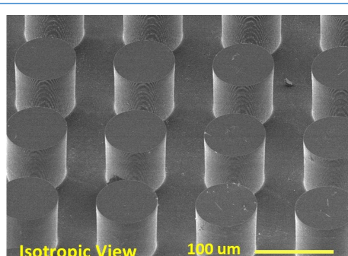


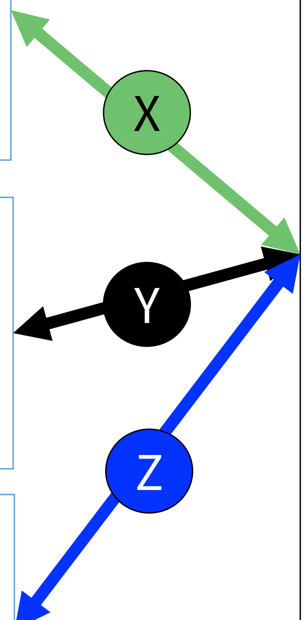
AlN pyramid Fins



Copper Inverse Opals (CIOs)



Silicon Pin Fins



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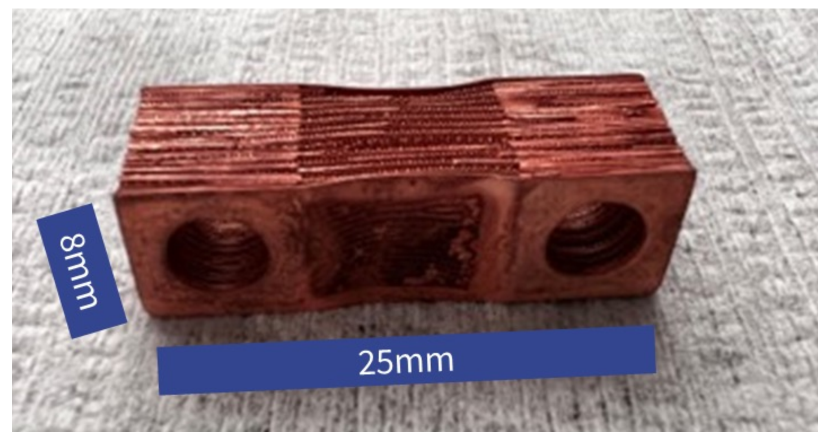
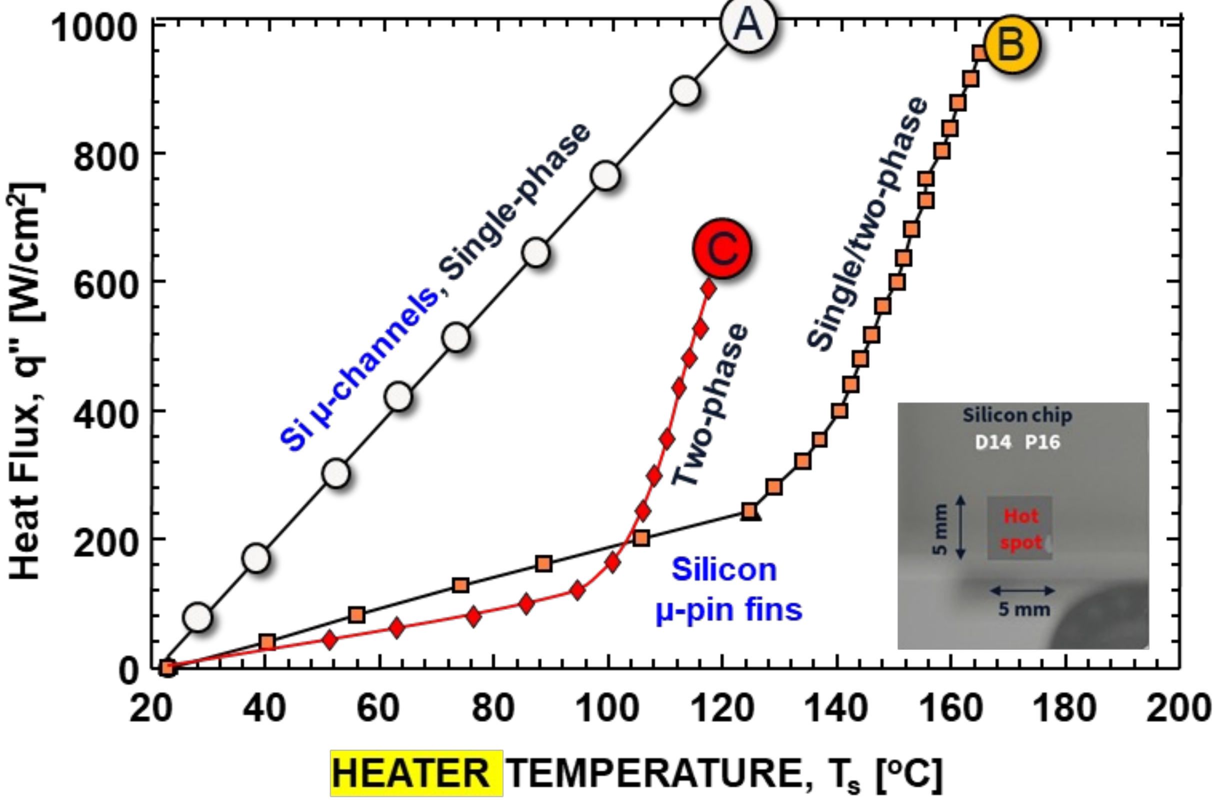
Additive manufacturing of Wiremesh 3D-Manifold



Prof. James Palko, Neda Tehrani (Ph.D. Student), Souvik Roy (Ph.D. Student), Muhammad Shattique (Ph.D. Student), Roman Giglio (Ph.D. Student)

R3.023.18: Development of a High Performance μ-cooler (0.01 cm^2-oC/W at <1 kW/cm^2) …

"Convective-based" vs. "Capillary-based cooling"



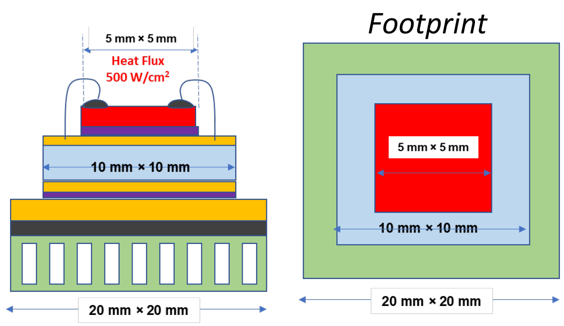
We achieved thermal resistance of ~0.05 cm^2-$^oC/W$ at maximum critical heat flux (CHF) of 600 W/cm^2 and superheat of 18 ^oC using **capillary-based boiling,** consuming ~3 grams/min (vapor quality: χ~0.9) of water without a pump.

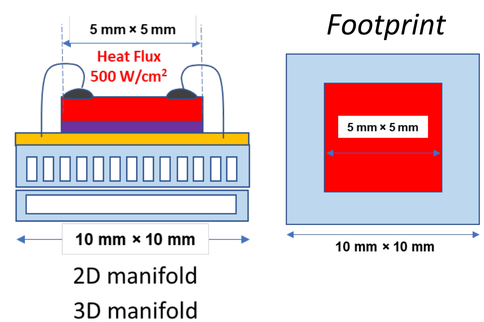
Thermal resistance of the silicon pin fins ~0.02 cm^2-$^oC/W$ at the superheat of 8^oC.

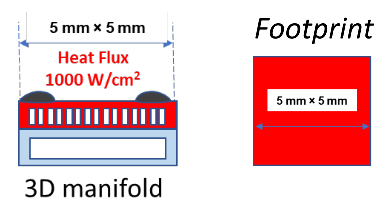
	Critical Heat flux q" [W/cm²]	Superheat ΔT [°C]	Thermal Resistance R" [cm²-°C/W]	Flow rate (grams/min)	ΔP [Pa]
A	1,000	NA	0.08	400	30
B	956	> 40 °C	> 0.06 (2-phase)	78	1
C	600	25 °C	0.05 (2-phase)	~3	NA

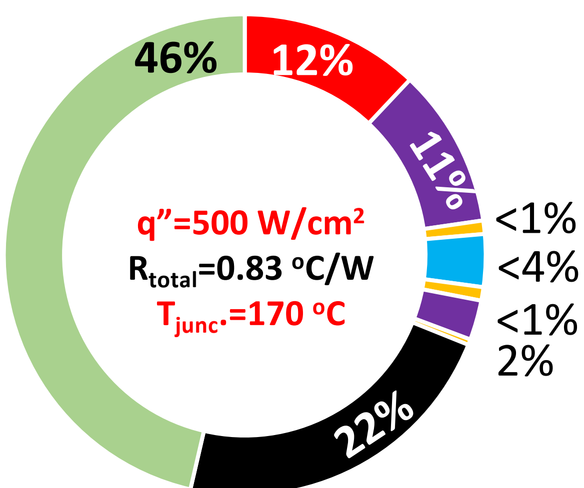
Fluidic Cooling in Coldplate, DBC Substrate and Chip

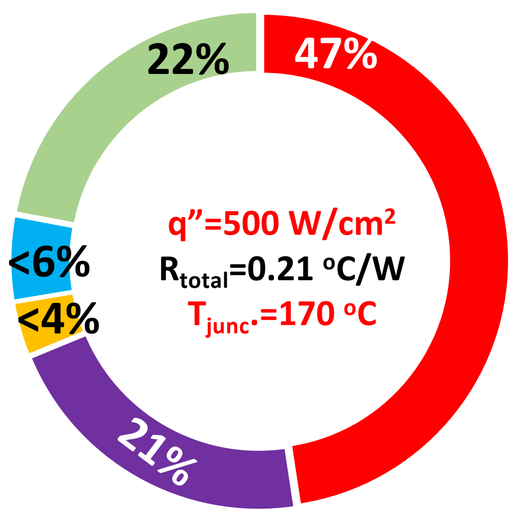
Fluidic Cooling In the …….	Cold-plate	Ceramic substrate	Chip
	Packaging layers in a standard power module with heat sink where heat is removed through the substrate. Each layer is a thermal impediment to heat flow	Modified packaging stack where a number of layers and interfaces have been eliminated from the thermal path by moving the fluidic cooling into the ceramic substrate.	Modified packaging where μ-channels are etched into the chip

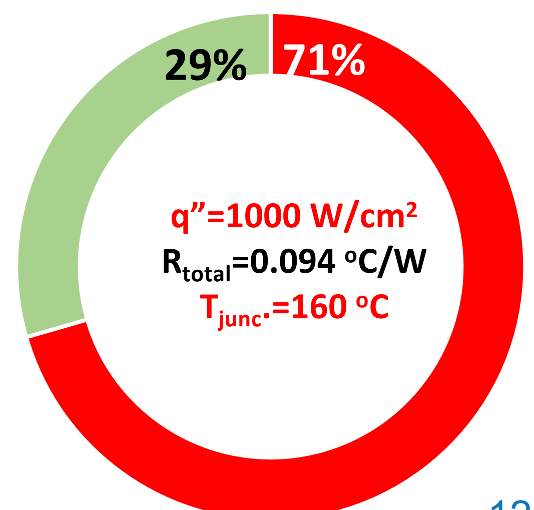










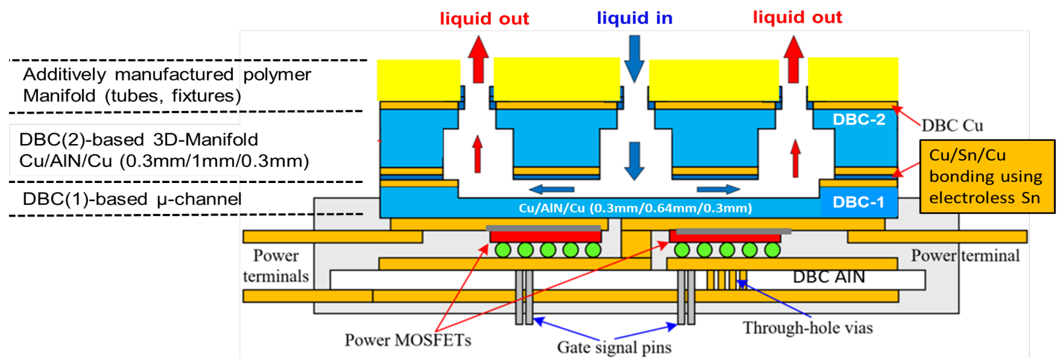


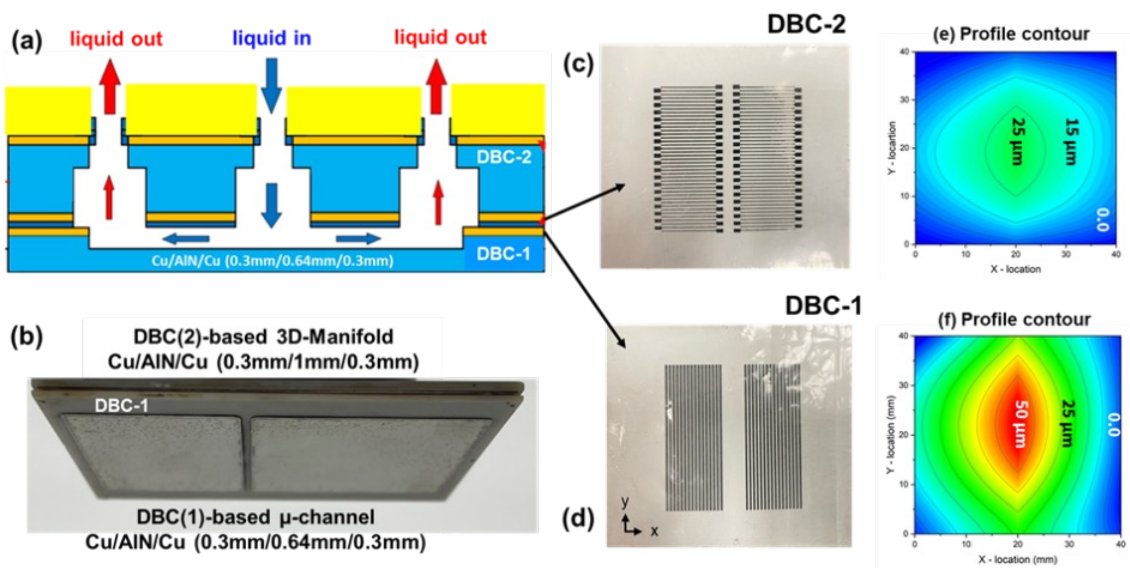
Integrated 3D Manifold Microchannel Cooling within Direct Bonded Copper (DBC) Platform

Hao Chen, Yujui Lin, Tiwei Wei, Wyatt Jason Moy, and Profs. Alan Mantooth, Kenneth Goodson, Nenad Miljkovic, Mehdi Asheghi, David Huitink

R2.036.22 Addressing DBC Warpage and Long-term Reliability of Microchannels in Heterogeneous SiC Power Modules

Cross-section view of micro-cooler integrated power module. Instead of bonding through interface material, the micro-channels of micro-cooler are directly etched in the ceramic layer of top DBC.



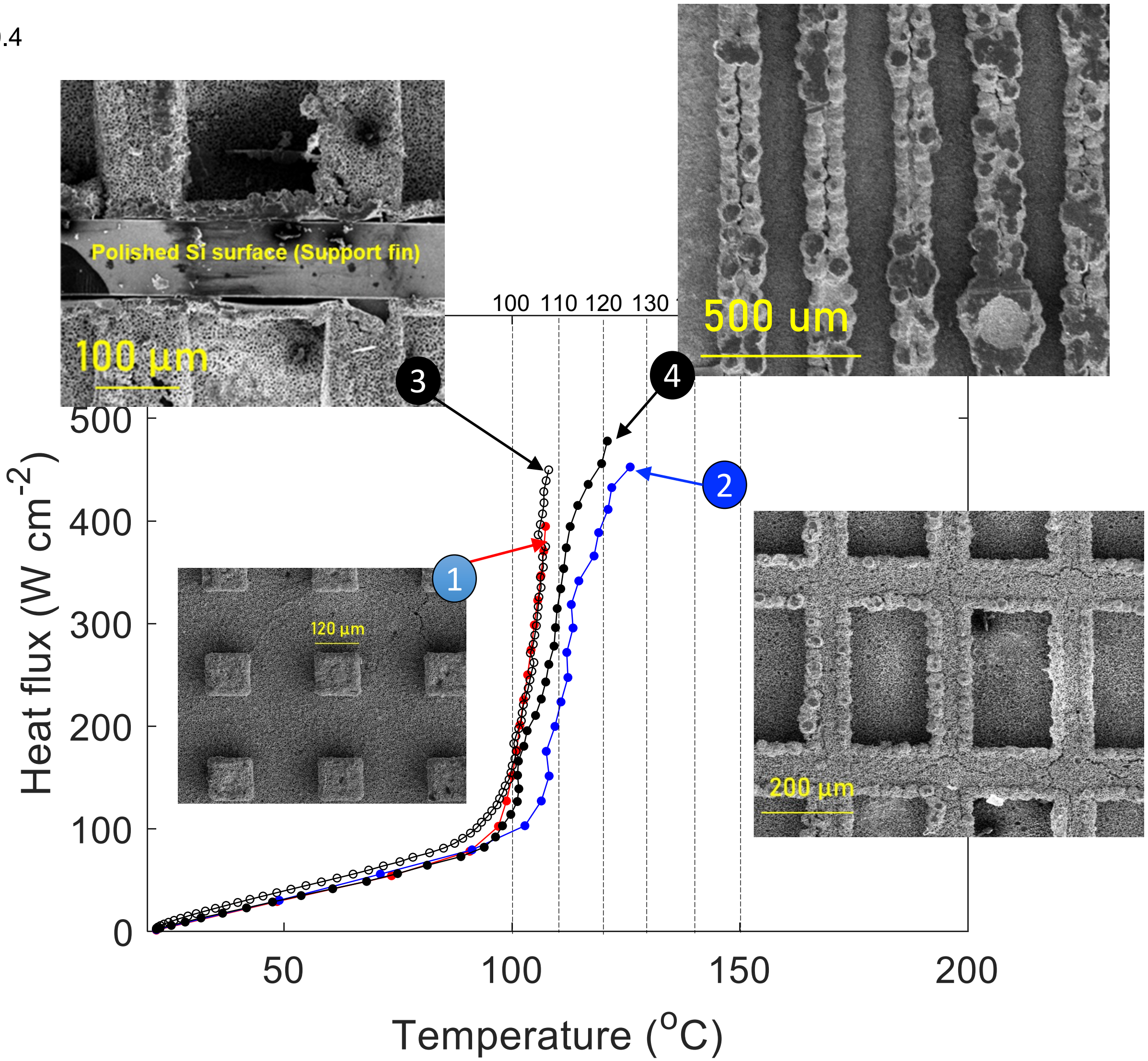


(a) A schematics of the DBC-based µ-cooler (b) bonded DBC-based u-cooler (c) DBC-2: laser cut slots that forms 3D manifold (d) DBC-1: laser cut micro-channels (e,f) Profile contours of the warpage in the 5 cm x 5 cm DBCs.

“Capillary-based cooling”

Copper Inverse Opals (CIOs): d_{CIO}~30 µm, d_n/d_p ~ 0.4

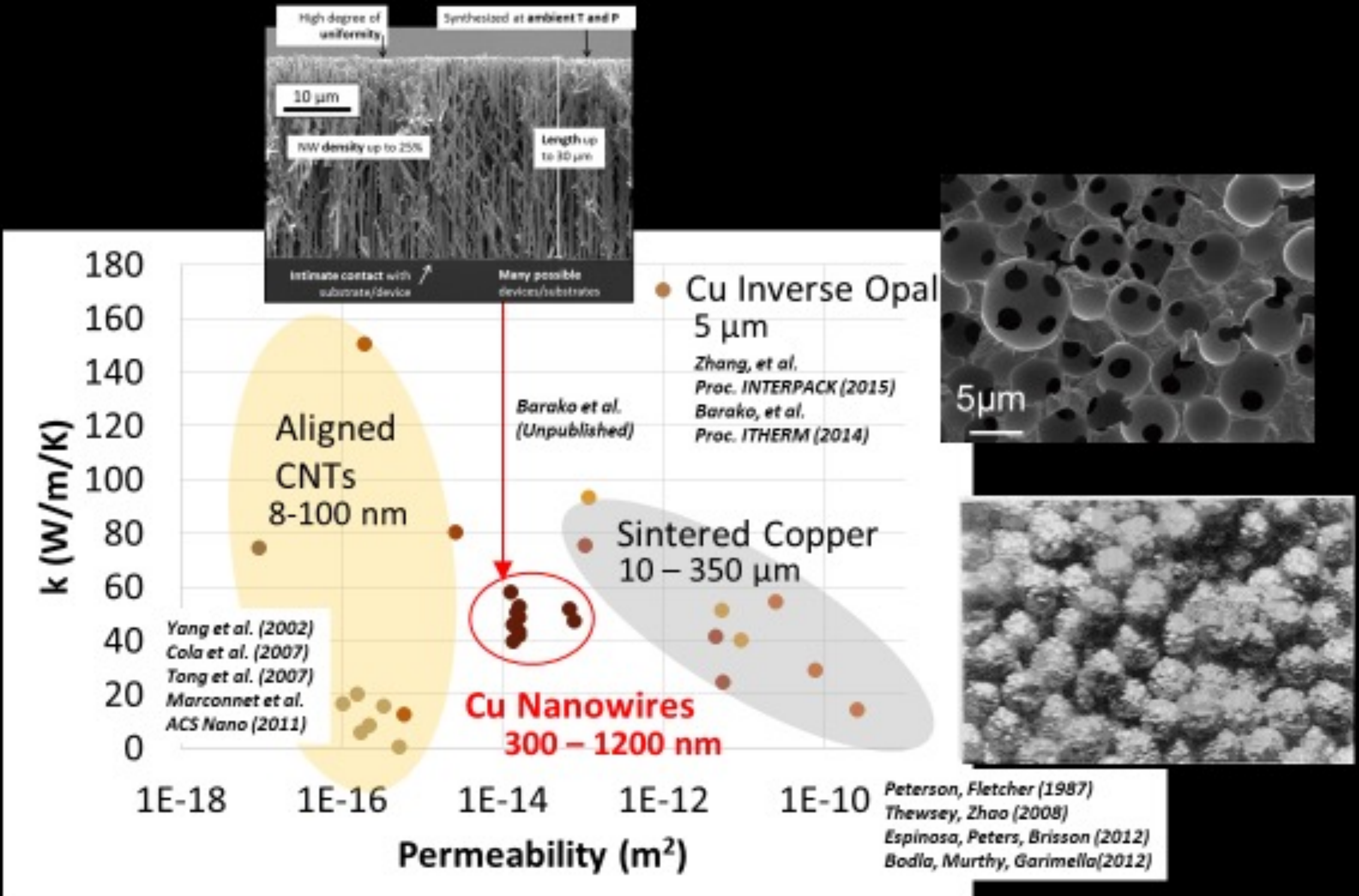
For the CIOs wick, a high CHF_{ave}~ 400 W/cm^2 is achieved with superheat (T_{wick}-T_{sat})= 6 °C that translates to a 2-phase thermal resistance R”$_{CIOs}$~ 6^{o}C/300 Wcm^{-2}=0.02 to 0.025 cm^2 -°C/W (water vapor quality: χ~0.9).



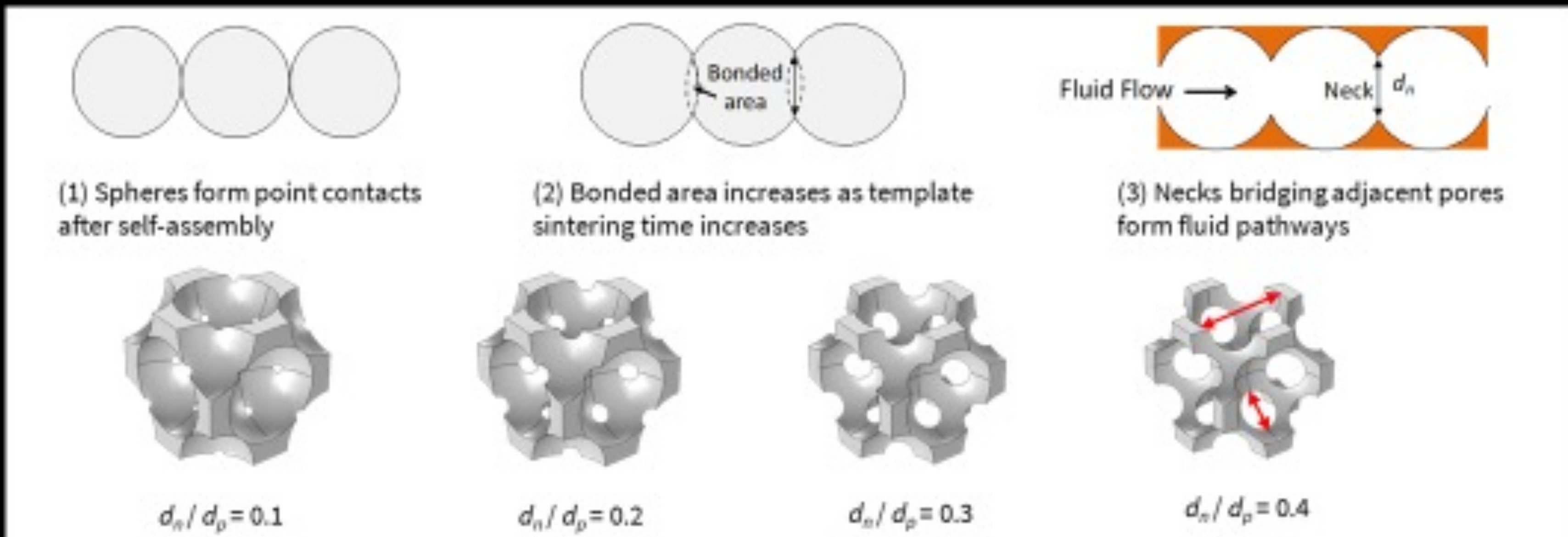
Wicking Metamaterials

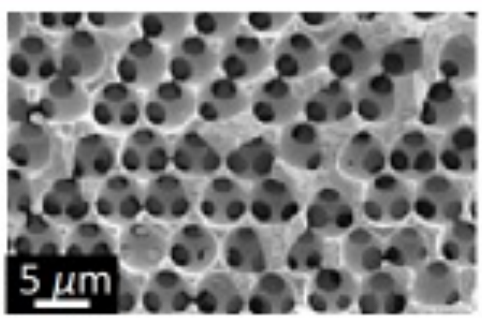
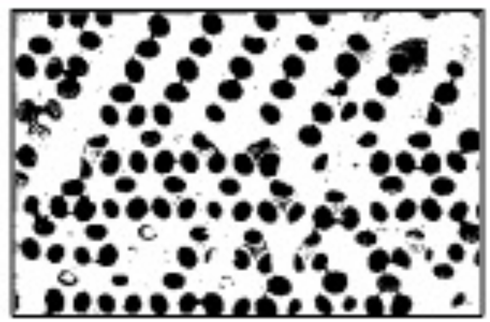
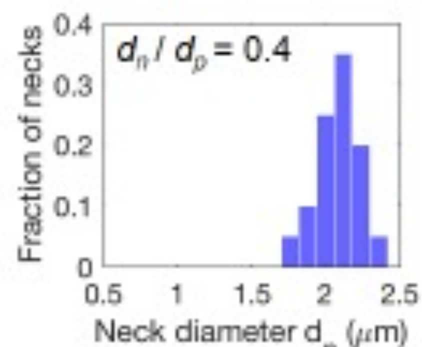
Barako, Goodson, et al. *NanoLetters* (2015)

NANO LETTERS



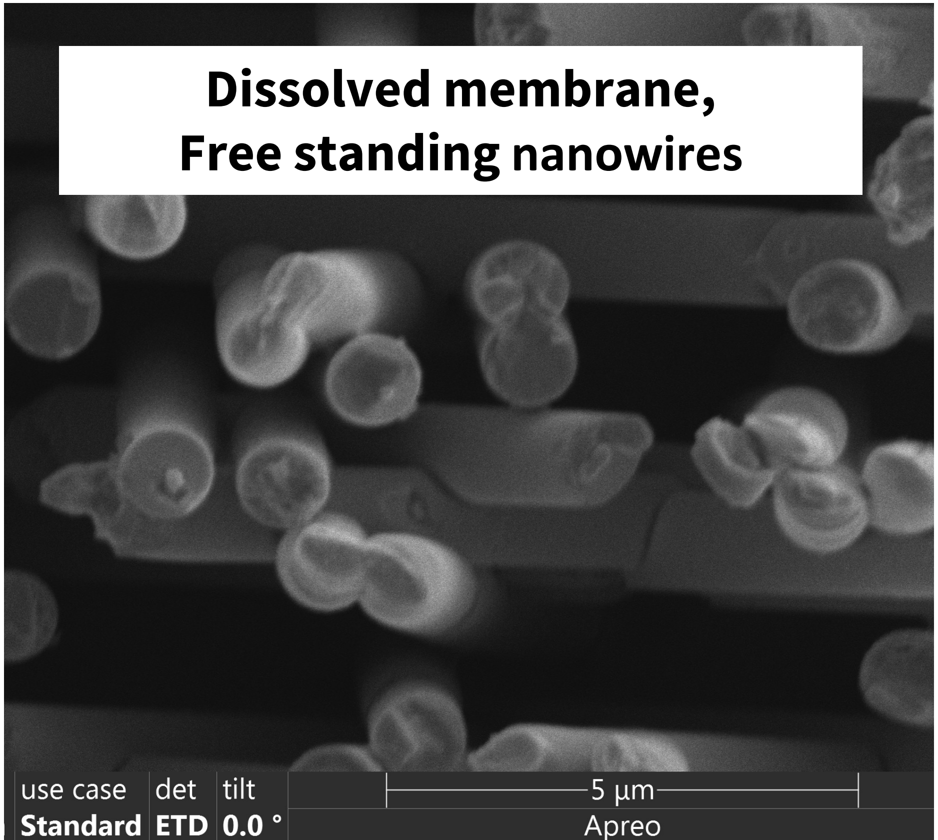
Tailoring the hydraulic permeability of inverse opal wicks via template sintering

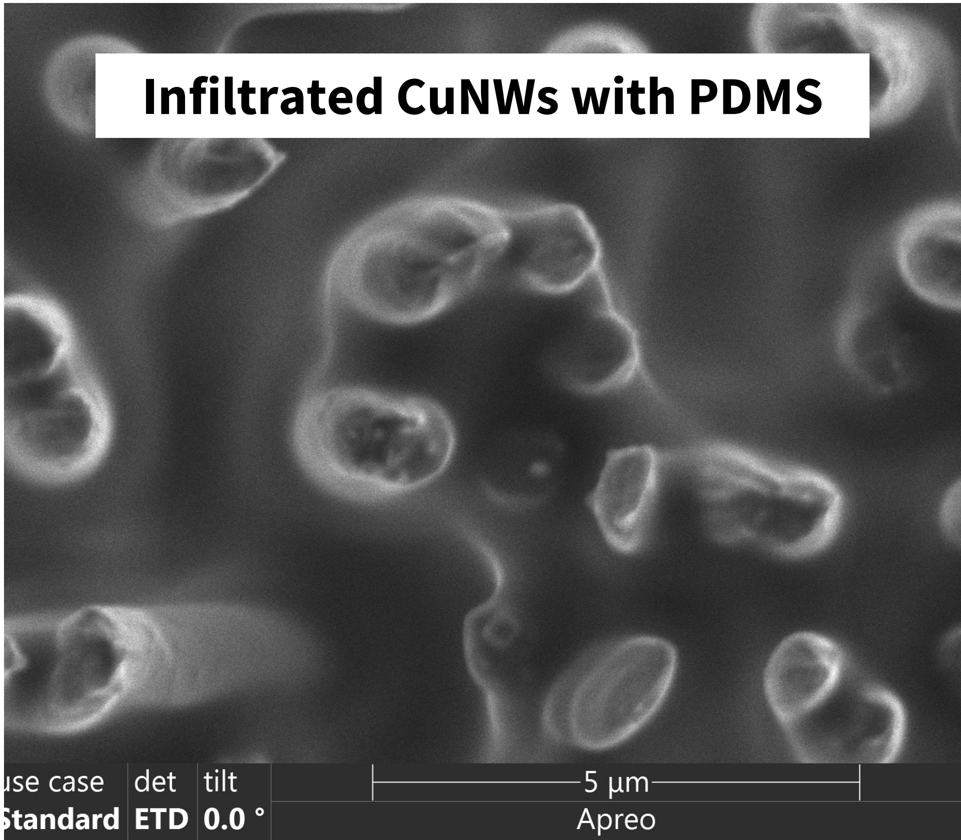


Template sintering time	SEM images	Analyzing necks	Neck diameter distribution
120 min			

Problem with the Gen#1 Flexible CuNWs Interconnects

- In the previous Approach, some of the nanowire tips were covered by PDMS after infiltration
- Imperfect or poor electrical, thermal and mechanical contact connection between CuNWs and the 2nd Cu foil.

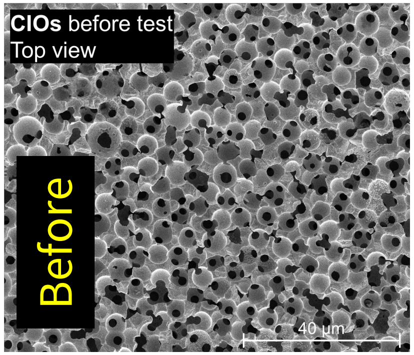




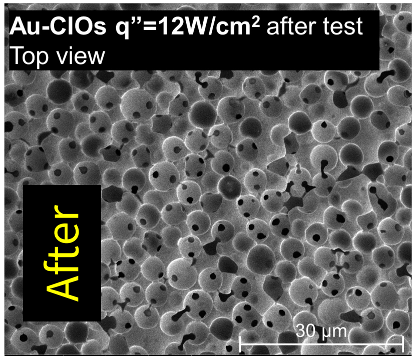
Conducted CHF and Reliability Pool Boiling Tests on CIOs using HFE 7100 and R-1233zd Refrigerant

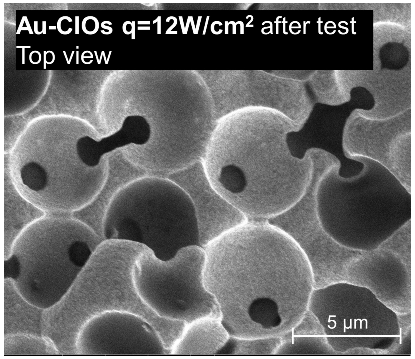
• Kiwan Kim, Katherine Jiang, Daeyoung

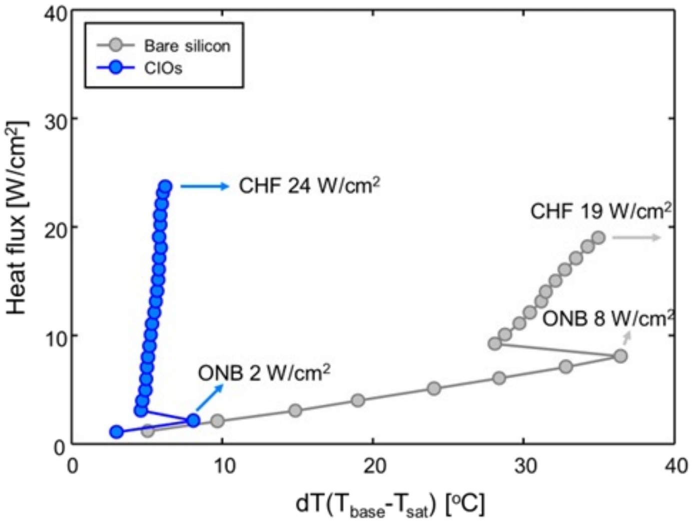
We observed no degradation of CIOs over 6- and 11-days tests at 50-67% CHF levels

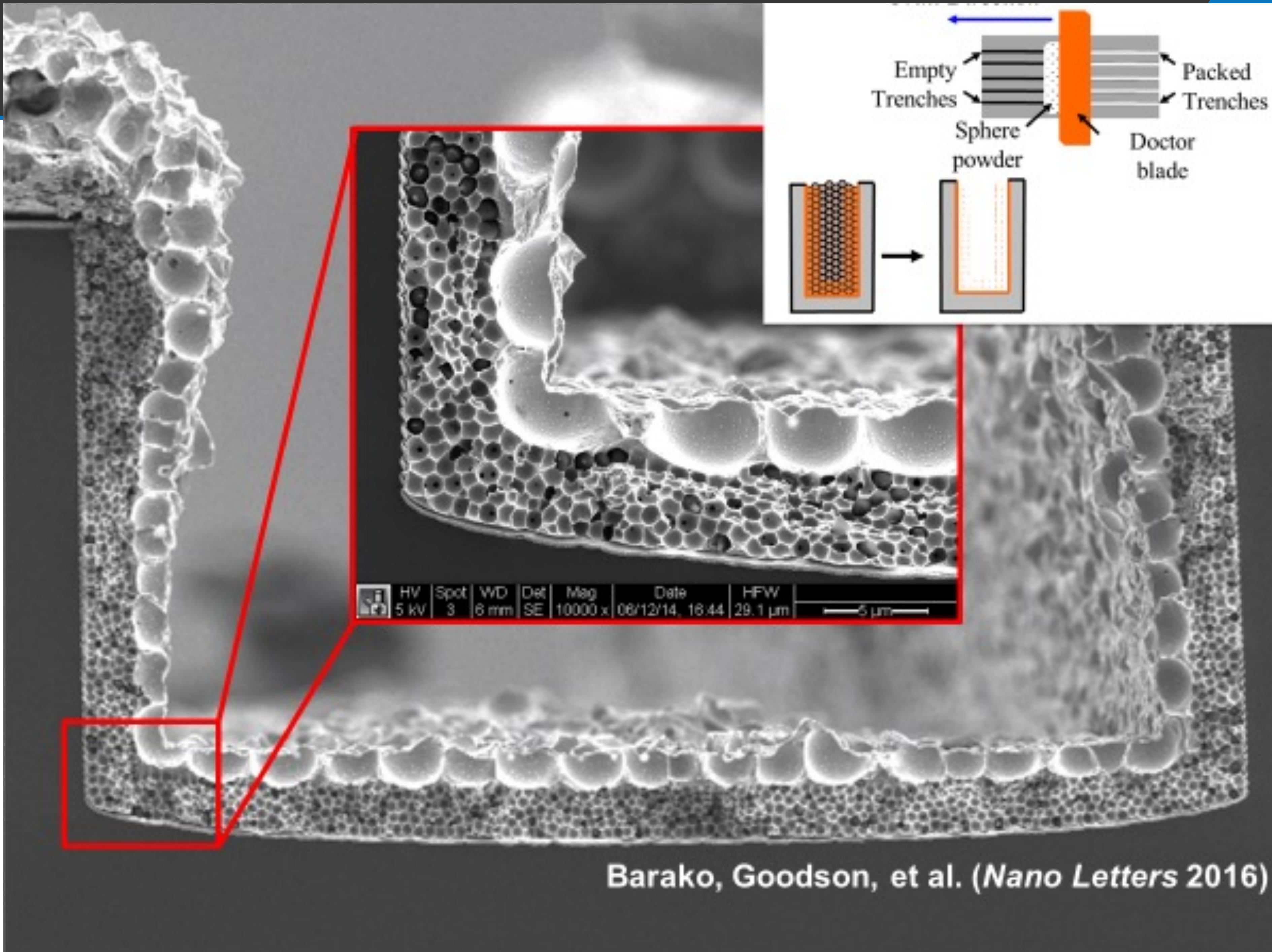


Significant improvement in the CHF and thermal resistance were observed compared to bare silicon.









Barako, Goodson, et al. (*Nano Letters* 2016)

Goals of Session

Materials selection and development has been at the heart of POETS efforts since the start of the center; however, they take a significant amount of time to assess, develop and mature. This session will explore the development and integration of new materials and materials systems for electro-thermal power density improvements.

Outcomes:

- Review POETS active research in the area of materials over the last several years.
- Address some of the challenges and industry needs surrounding materials research.
- Identify focus areas of **fundamental research** and **enabling technologies** where POETS can contribute as we move forward

Session Agenda

Session Facilitated by Dr. Sonya Smith

- **20 Min – Industry Presentation**
  - TBD - Working with NASA Ames
- **60 Min – Technology Presentations**
  - **15 Min** - Materials enabling higher heat fluxes for components with the goal of improved thermal management. (**Dr. Ashegi**)
  - **15 Min** - Novel materials and approaches for high power and energy density thermal energy storage (**Dr. Miljkovic/Dr. Braun/Dr. Lyding**)
  - **15 Min** - Nitride materials in power electronics (**Dr. Stillwell)**
  - **15 Min** - Cryogenics for conventional systems and for superconductivity - (**Dr. Haran, Dr. Mantooth**)
- **40 Min - Guided discussion**
  - Challenges and needs regarding materials and how POETS can contribute. Group encouraged to rank and stack ideas to ensure POETS is focusing on highest need objectives.

Faculty – Please insert your slides here and return to Owen by **Monday, October 17** for placement into the overall slide deck.

For Information Only

Tasks for Technical Presentation

- Provide high-level introduction of topic area
- Highlight current state of POETS research; including challenges
- Showcase specific projects that demonstrate POETS competency

Audience

- POETS’ Industry Reps – multi-disciplines
- POETS’ Faculty
- POETS’ Students

Support

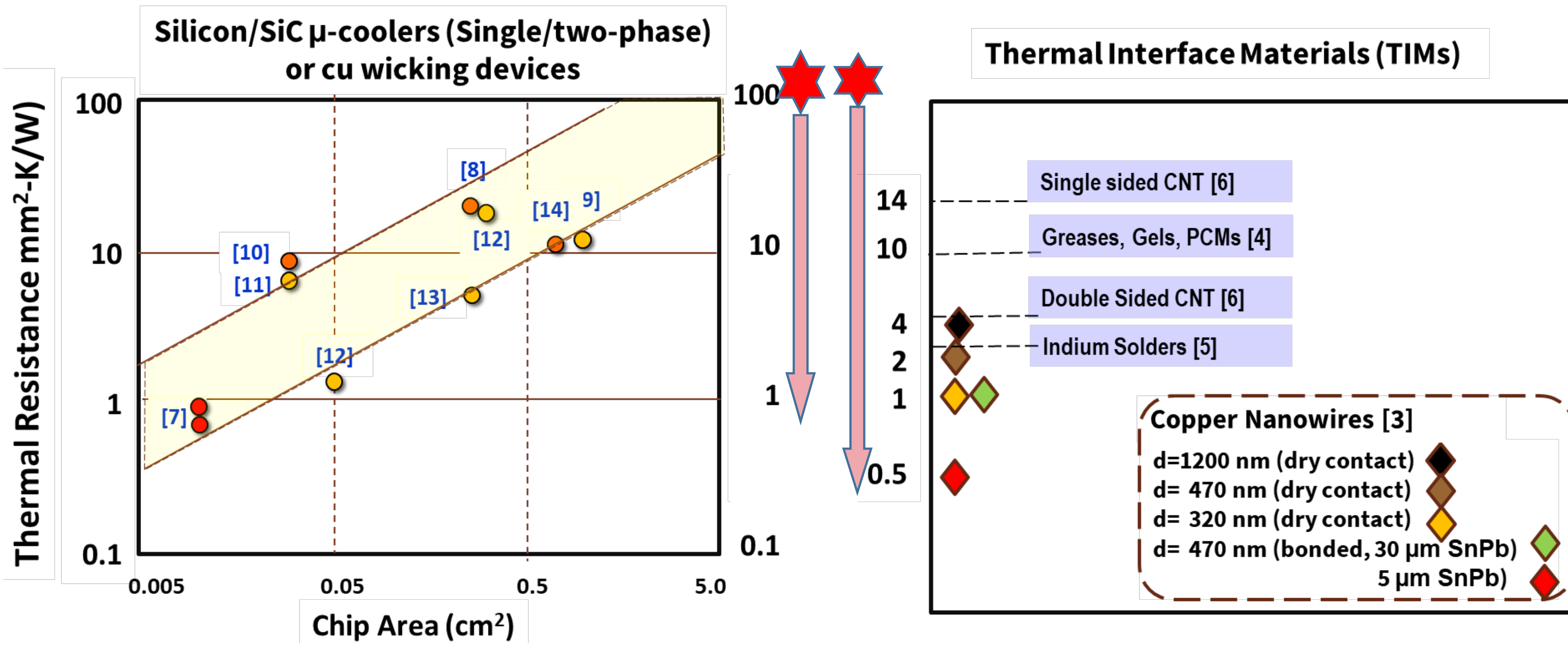
- If you want to include graphics or information on a POETS project in your topic area that is not your project, let Owen know and he can pull that information.
- If you have some papers or documents you would like to provide the IAB/Students to help with technical backgrounds, please provide them to Owen and he will disseminate prior to event.

Tasks for Technical Presentation

- Provide high-level introduction of topic area
- Highlight current state of POETS research; including challenges
- Showcase specific projects that demonstrate POETS competency

Thermal Interface Materials

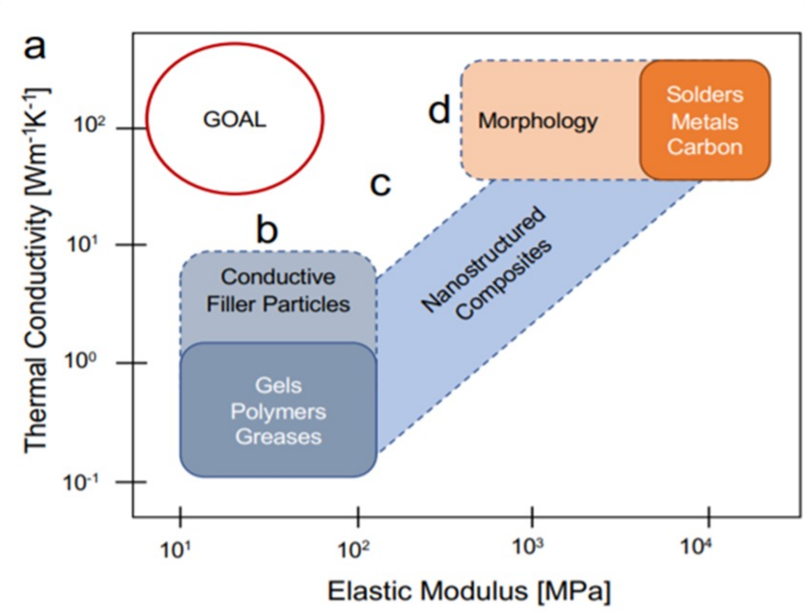
Comparison of thermal resistance of the State-of-the-Art lab demo for silicon or silicon-based single/two-phase micro coolers with thermal interface materials

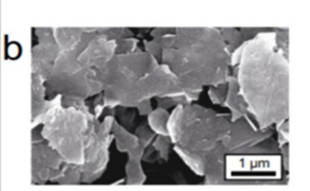


Comparison of thermal resistance of the State-of-the-Art laboratory demonstration for silicon or silicon-carbide-based single/two-phase micro coolers with thermal interface materials (CNT: carbon nanotubes, PCM: phase-change material; greases, gels, PCMs : [5]; CNTs: [6], with that of the proposed CuNWs/PDMS TIMs tape (1 cm x 1 cm). Application of the high-performance micro-coolers with thermal resistance smaller than 5 mm^2-K/W requires development of commercial TIMs with thermal resistance comparable or lower than the u-coolers. The proposed CuNWs/PDMS TIMs tape performs a factor of 4 better than CNTs [6], with a potential to achieve thermal resistances as low as 0.5 mm^2-K/W.

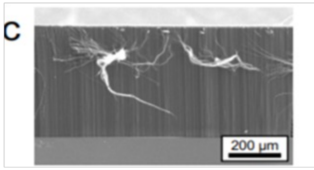
Thermal Interface Materials

Two common strategies can be employed to create high-performance TIM composites

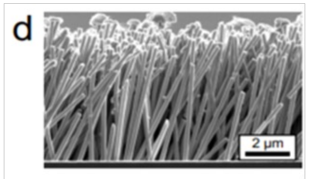




intrinsically soft material and add fillers to increase the thermal conductivity, such as (e.g., metal nanoparticles, carbon nanoparticles, and graphene nanomaterials).



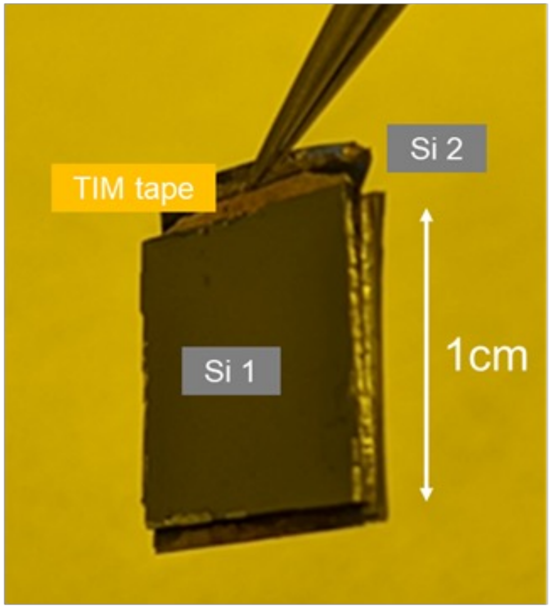
The second strategy is to form a nano-structure from an intrinsically conductive material into a mechanically compliant morphology,

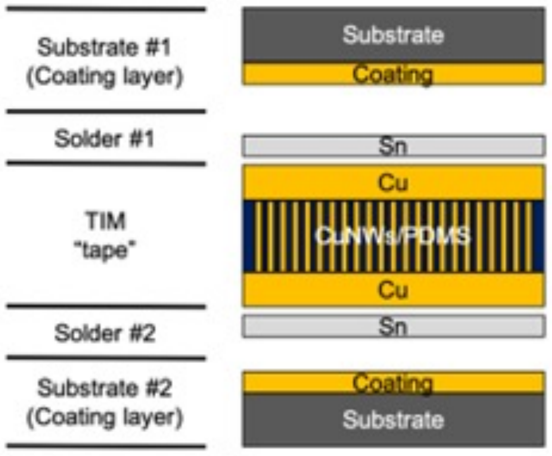


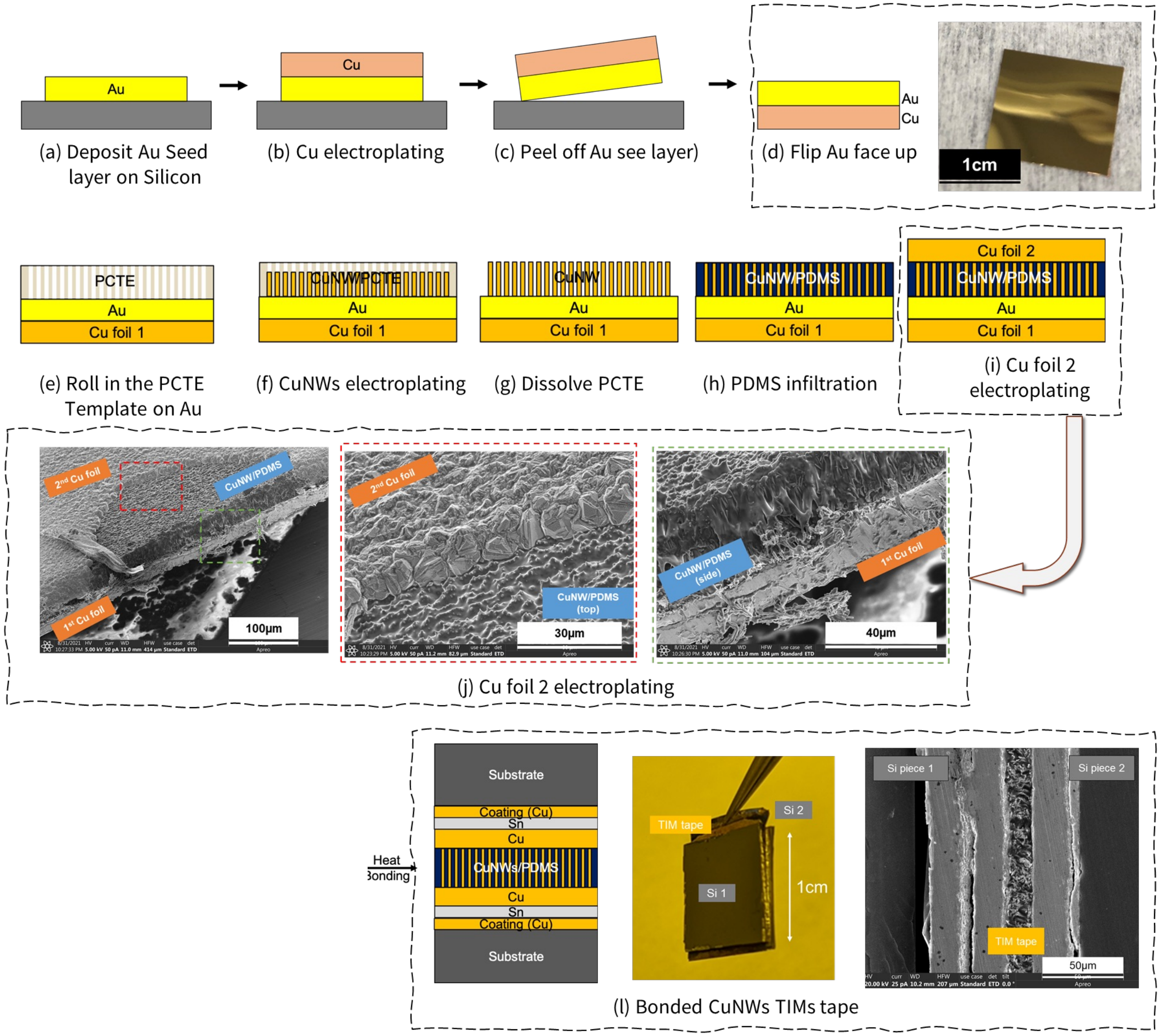
(c) vertically grown nanotubes [16-17], and

(d) vertically electro-deposited nanowires (< 0.5 mm^2 K/W with < 50 μm thickness) [18].

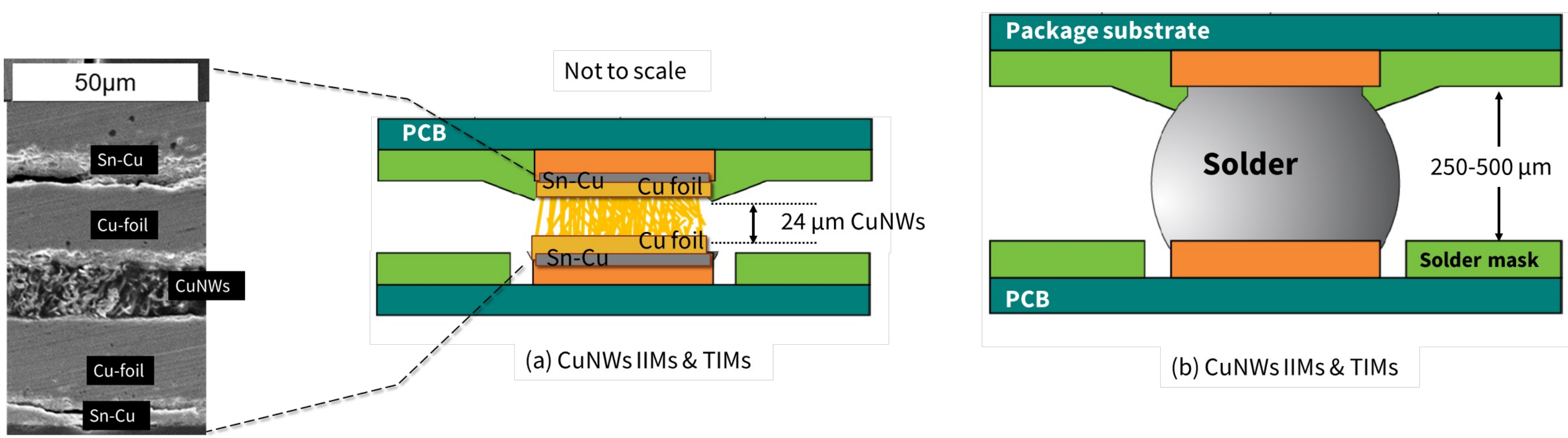
"CuNWs TIMs Tape" with Sn Solder Bonding Films







R3.038.22 Replacing the Solder Ball Technology: Development of a Compliant Electrical (EIMs) and Thermal Interface Materials (TIMs) Interconnects using Copper Nano-wire (CuNWs) (New Project)



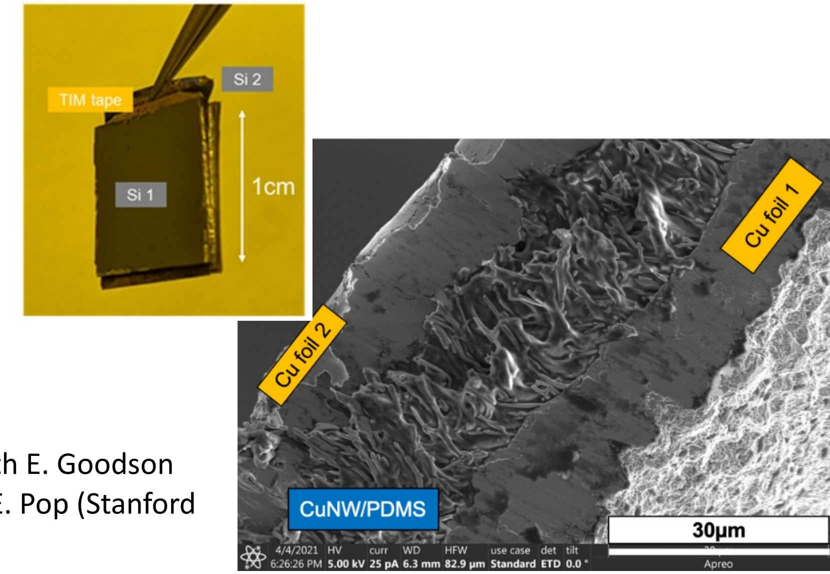
(a) CuNWs IIMs & TIMs

(b) CuNWs IIMs & TIMs

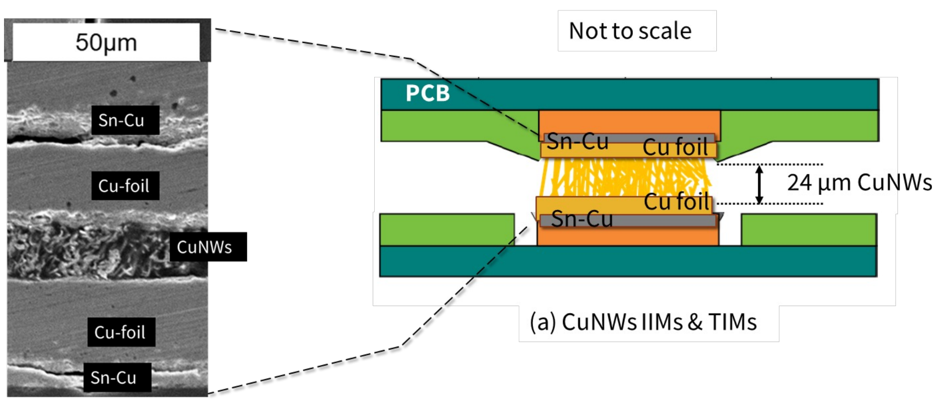
Graduate Students: Hansen Qiao (Stanford), Katherine Jiang (Stanford), Bakhtiyar Mohammad Nafis (UArk)

Advisor: Prof. Kenneth E. Goodson (Stanford), Adjunct Prof. M. Asheghi (Stanford), Prof. D. Huitink (UArk), Prof. E. Pop (Stanford)

R3.032.20: Development of Copper Nanowires (CuNWs) Thermal Interface Materials (TIMs) with (Cu,Ni) – Sn Transient Liquid Phase (TLP) Bonding for High-Temperature Power Electronics Applications



Graduate Students: Hansen Qiao (Stanford University); Advisor: Prof. Kenneth E. Goodson (Stanford University), Faculty Collaborators: Adjunct Prof. M. Asheghi, Prof. E. Pop (Stanford University); Prof. D. Huitink (University of Arkansas)



(a) CuNWs IIMs & TIMs

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