SYNTHESIS AND CHARACTERIZATION OF TWO-DIMENSIONAL MATERIALS FOR ELECTRONIC AND THERMOELECTRIC APPLICATIONS

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Abstract

Exponential increases in transistor density since the 1960s, made possible through continued transistor scaling, have allowed for incredible technological advancements up until the present day. However, fundamental physical limitations of Silicon-based transistors have made it necessary to explore novel avenues to address growing technology needs. To this end, the family of two-dimensional (2D) materials has been demonstrated to possess unique characteristics that make them appealing for scaled electronic applications. However, this versatile class of materials comes with its own unique challenges for fabrication and integration into widespread adoption. Therefore, in this work, we investigate the synthesis and properties of selected 2D materials, working to understand how their unique characteristics may impact their utility.

First, we develop and refine processes for large-area chemical vapor deposition (CVD) of hexagonal boron nitride (h-BN) onto carbon nanotube (CNT) and metal substrates. We report one of the first demonstrations of direct deposition of multilayer h-BN on CNTs, resulting in a thin capping layer on the CNTs without the use of a transfer process. Additionally, we elucidate some effects of substrate crystallinity on the resultant h-BN film by characterizing films deposited on both polycrystalline and single crystal Pt substrates. Finally, we demonstrate the use of monolayer h-BN as an ultra-thin protective barrier layer, protecting monolayer MoS_2 from degradation at elevated temperatures, and we discuss additional applications for this material.

In addition, we investigate fundamental thermoelectric properties of thin WSe_2, fabricating on-chip heater and thermometer structures and quantifiably demonstrating the benefits of using a low-thermal conductivity substrate to maintain a larger temperature gradient along the channel. Using our measurement platform, we measure the highest Seebeck coefficients for thin WSe_2 reported in literature to date, demonstrating its promise for temperature sensing and energy harvesting applications. We conduct measurements on multiple WSe_2 samples, studying the effect of film thickness on the thermoelectric properties, and electrostatically gate the channels using an ion gel, which enables us to sweep over a wide range of electron and hole carrier densities.

Finally, we explore the effects of edge contributions to narrow MoS_2 and WSe_2 channels, fabricating back-gated devices on exfoliated nanoribbons. The exfoliation process to deposit these nanoribbons is promising for maintaining "pristine" edges, which are ideally in the armchair or zigzag configuration. This can allow for the impact of these edges on the electronic transport properties to be studied, and we measure numerous transistors with parallel nanoribbon channels to consider these effects. We observe some trends with the maximum and minimum currents vs. the average ribbon width of these channels, and outline the next steps for this project to further understand the edge contributions.

This work explores the deposition as well as fundamental electronic and thermoelectric properties of 2D materials, aiming to incrementally advance this family of materials towards viability in larger-scale applications.

Acknowledgements

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Chapter 1

Introduction

1.1 Two-Dimensional (2D) Materials Overview

1.1.1 Challenges with Further Transistor Scaling

Continued transistor scaling and density increases following Moore's law have allowed for incredible technological advancements over the last century [1]. Despite challenges that arose from the end of Dennard scaling in the early 21st century [2], innovations in materials, transistor architectures, and semiconductor fabrication processes have allowed for scaling to continue, enabling transistor density increases at an exponential rate [3]. This trend is illustrated in the plot in Figure 1.1 [4].

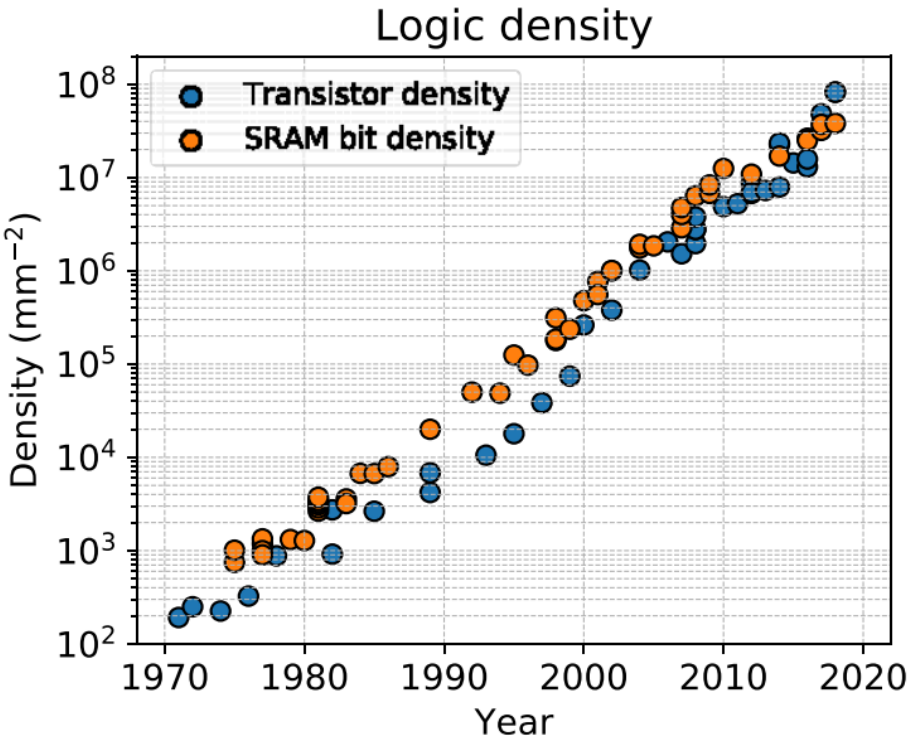

Figure 1.1: A plot displaying the consistent exponential increases in transistor density over time [4].

Although not all the advancements in transistor scaling have come directly from only device dimensions shrinking, with each subsequent node, the physical dimensions of transistors generally will reduce. Currently, the semiconductor industry has reached the 5 nm node, and although this label is somewhat arbitrary as it no longer refers to the physical gate length of the transistor, the device dimensions are still on the order of only a few dozen atoms. At this rate, continued scaling will eventually lead to fundamental physical limitations, and these may be surmounted in part through the use of alternate material systems.

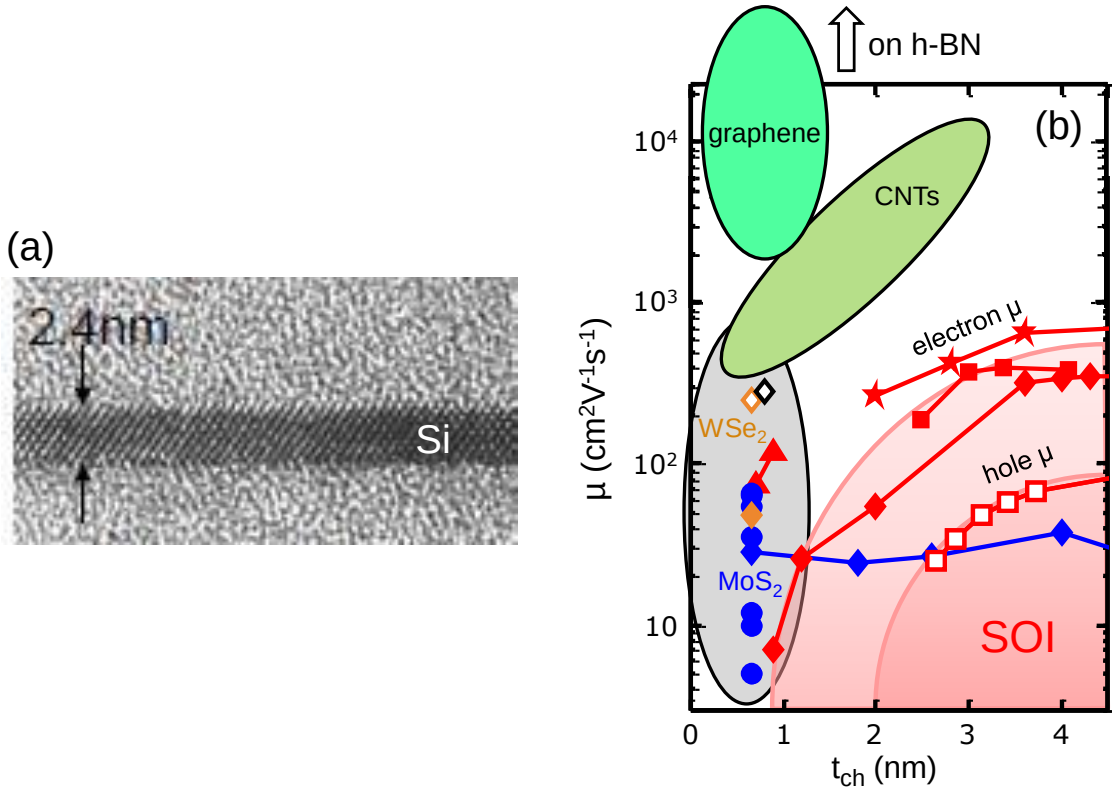

Figure 1.2: (a) A transmission electron microscopy (TEM) image illustrating thickness fluctuations and rough interfaces for an ultra-thin Si channel [5] and (b) a plot of mobility (μ) vs. channel thickness for various materials at room temperature, highlighting the degradation in μ for Si at very scaled dimensions [6].

To describe this phenomenon in more detail, at extremely small device dimensions, the electronic properties of Si begin to degrade. This is due to short channel effects such

as threshold voltage roll off and drain induced barrier lowering, and the charge carrier mobility can degrade due to thickness fluctuations over the Si channel and interface roughness, as illustrated in Figure 1.2(a) [3, 5, 7]. Therefore, it may be necessary to explore alternate material systems that can maintain good electronic performance at those dimensions. Two-dimensional (2D) materials are a family of materials with unique properties that may help to address these scaling challenges [6]. The plot in Figure 1.2(b) highlights some 2D materials with preserved mobility at sub-1 nm channel thickness [6].

1.1.2 Selected Properties of 2D Materials

It has been shown that 2D materials may be promising for use in electronic applications [8]. These materials are characterized by their strong in-plane bonds, but weak, out-of-plane Van der Waals bonds to adjacent layers. Because they do not have out of plane dangling bonds, they can be considered atomically thin by nature when isolated from the bulk crystal, and this makes them especially attractive for nanometer-scaled applications. The family of 2D materials is expansive, with electrical band gaps ranging from 0 eV in semi-metallic materials such as graphene, through semiconducting materials such as the transition metal dichalcogenides (TMDs), up to electrically insulating materials such as hexagonal boron nitride (h-BN). These are illustrated in Figure 1.3.

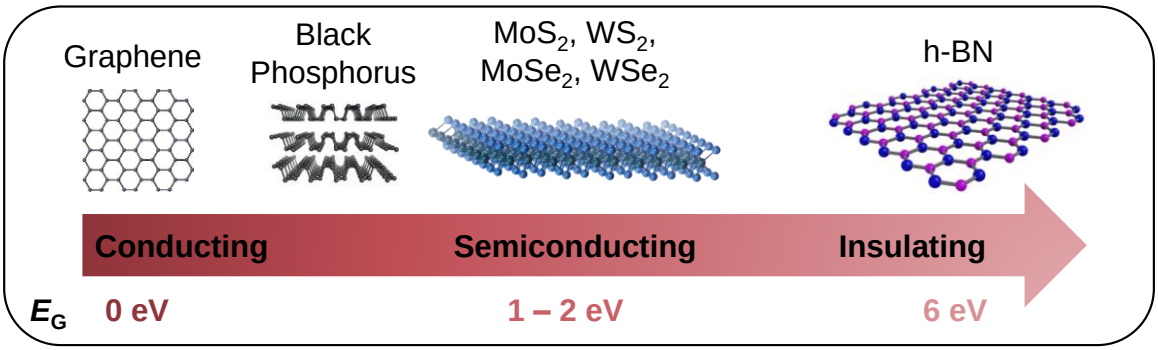

Figure 1.3: Illustrated list of selected 2D materials spanning a wide range of band gaps.

In addition to these electrical properties, the family of 2D materials also spans a wide range of thermal properties. There are 2D materials with highly anisotropic thermal conductivities, such as h-BN with high in-plane thermal conductivity [9], as well as ones

with more isotropic and low thermal conductivities, such as SnSe [10]. These thermal properties are also tunable through stacking, and so can be engineered to have the desired qualities [11, 12]. Therefore, 2D materials can be utilized for heat spreading, heat blocking, and even thermoelectric purposes (which require a low thermal conductivity and are described subsequently).

In this work, we focus primarily on transition metal dichalcogenides (TMDs) as well as hexagonal boron nitride (h-BN). TMDs are a subset of 2D materials which consist of the form MX_2, where M represents a transition metal atom, and X is a chalcogen atom. These materials have band gaps that typically fall between 1 – 2 eV, depending on thickness and dielectric environment, and therefore are useful as semiconductor materials [13].

1.2 Thermoelectrics: Background and Motivation

1.2.1 Thermoelectric Principles

As briefly mentioned previously, 2D materials may exhibit novel thermoelectric properties, which should be studied in more depth to determine potential applications in this space. The thermoelectric effect is partially comprised of the Seebeck effect, in which charge carriers will diffuse in the presence of a temperature gradient. This diffusion leads to a buildup of charge on one side of the thermoelectric material, which then results in a built-in potential difference. This effect is quantified through the Seebeck coefficient, $S = -\frac{\Delta V}{\Delta T}$ [14].

Connecting multiple thermoelectric legs electrically in series and thermally in parallel in the presence of a temperature gradient can then lead to a larger summed voltage, which is useful for energy harvesting or temperature sensing. This is schematically illustrated in Figure 1.4. On the other hand, the reverse is called the Peltier effect, in which pushing current through a thermoelectric material can heat one side and cool the other, which is useful as a solid-state cooling technique. As this effect is reversible, it fundamentally differs from Joule heating, which involves the moving charge carriers colliding with and transferring energy to the lattice.

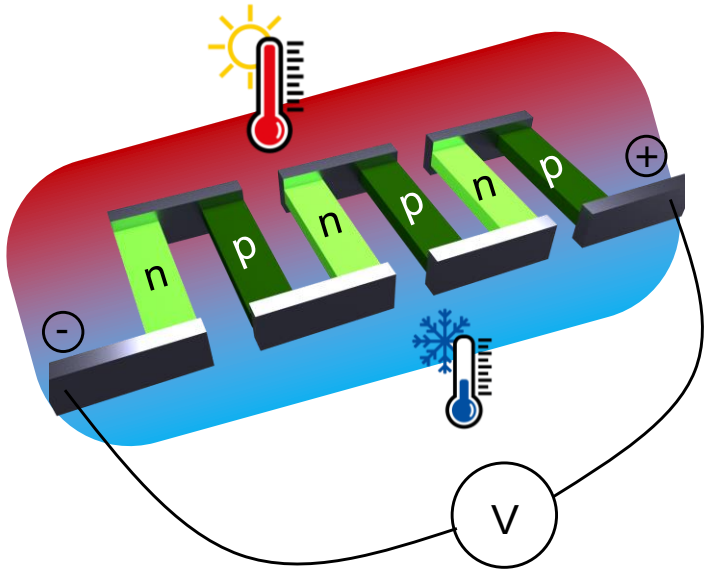

Figure 1.4: A schematic illustration of multiple n- and p-type thermoelectric legs connected electrically in series and thermally in parallel. The buildup of electrons and holes on one end of the thermoelectric legs due to the temperature gradient results in a voltage summed over the legs.

Understanding thermoelectric properties of 2D materials is crucial if they are to be widely adapted for electronic applications, as thermoelectric effects can lead to uneven heating or cooling of the channel material, depending on current flow direction. Because the electronic properties of 2D materials are sensitive to temperature, it can be important to ensure that any localized heating or cooling effects are understood. An example of asymmetric heating across a 2D device under operation is shown in Figure 1.5. In this work, scanning Joule expansion microscopy (SJEM) was used to probe the local temperature rise of the device surface during operation, where the temperature rise is primarily dominated by Joule heating, but the direction of current flow plays a role in the precise temperature profile [15].

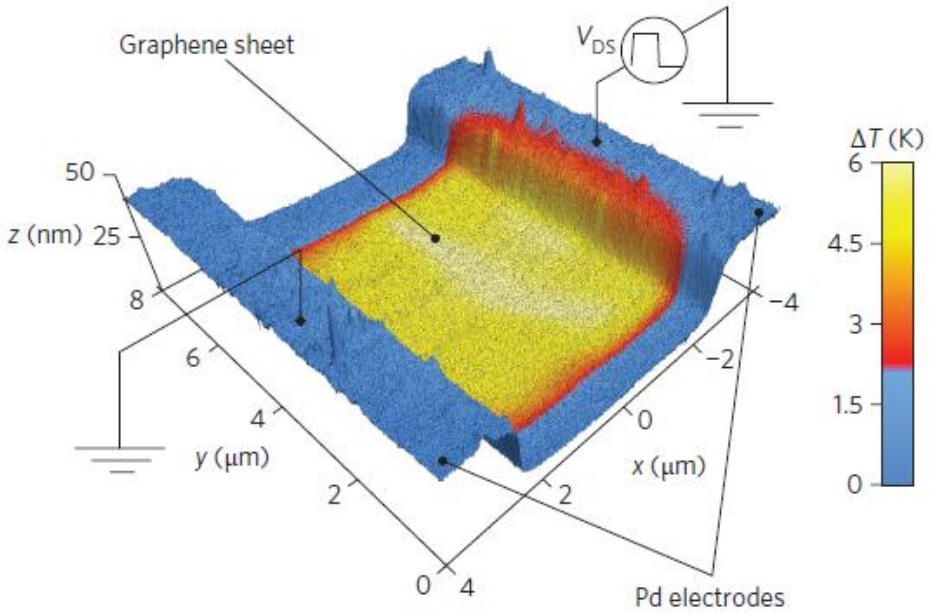

Figure 1.5: A temperature map of a graphene device during operation, overlaid on its topography, showing asymmetric heating at the source vs. drain, in part due to the thermoelectric effect at the graphene/metal contact interface [15].

1.2.2 Efficiency of Thermoelectric Materials

Additionally, thermoelectric materials can be useful for small-scale power generation and energy harvesting of waste heat. For these applications, the efficiency of a thermoelectric energy harvester is defined as $zT = \frac{S^2\sigma}{\kappa}T$, where S is the Seebeck coefficient, σ is the electrical conductivity, κ is the thermal conductivity, and T is the absolute temperature. While it is desirable to maximize efficiency, since the constitution parameters that comprise zT are interrelated, it requires careful material tuning. Figure 1.6 plots these variables against a semiconductor's carrier density, highlighting the complex relationship between them.

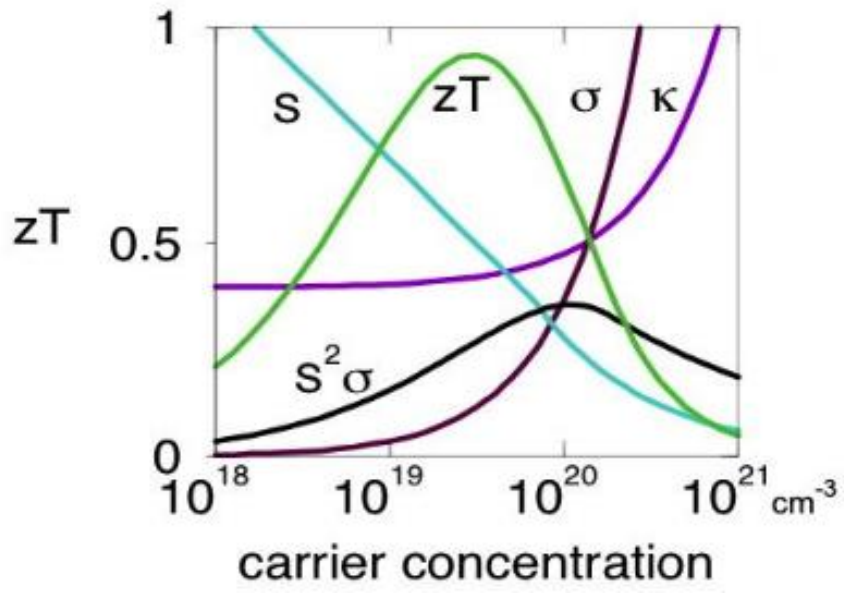

Figure 1.6: Plot of zT and its components (S, σ, and κ) vs. carrier concentration for a typical semiconductor material. Because these parameters are interrelated and do not trend in the same direction with increasing carrier density, the zT requires careful tuning in order to maximize thermoelectric efficiency [14].

Traditional, bulk materials that are used for thermoelectric energy harvesting, such as Bi_2Te_3, are relatively inefficient, and therefore primarily only used in niche applications [16]. However, 2D materials have shown promise for obtaining higher *zT* values, in part due to quantum confinement effects that occur in these ultra-thin layers [17]. These steep features in their density of states can result in an enhanced *S*. To highlight how this can be the case, an example with 3D materials is shown in Figure 1.7.

An illustration of density of states (DOS) and differential conductivity [σ(E)] vs. energy (*E*) for a metal and semiconductor is shown in Figure 1.7 [18]. In Figure 1.7(a), the DOS is shown for a typical bulk metal. The electrical conductivity (σ) is large, but the S is low because the Fermi Energy (E_F) is further from the band edge, and therefore there is a similar number of states available for transport above and below E_F. However, for a semiconductor, as shown in Figure 1.7(b), with E_F positioned close to the band edge, the DOS is more asymmetric with respect to E_F. In this case, there are more available states above E_F than below, and *S* will be higher.

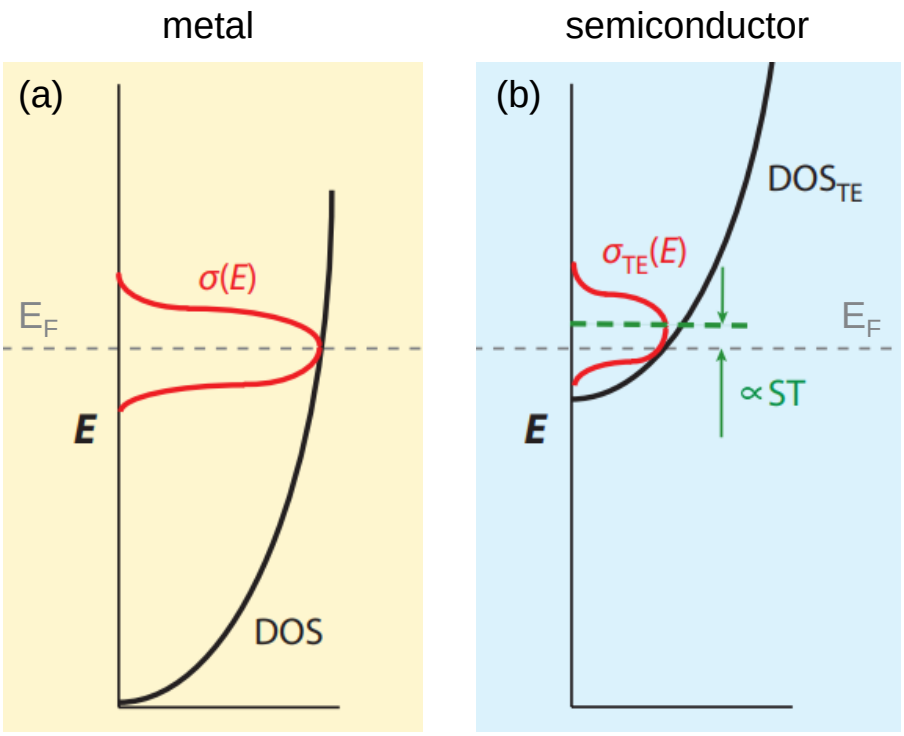

Figure 1.7: Representative density of states (DOS) and differential conductivity [σ(E)] vs. energy (*E*) for a typical (a) metal and (b) semiconductor [18]. The Fermi Energy (E_F) is designated with the gray dashed line.

Additionally, the charge carrier concentrations of 2D materials can be modulated through gating or doping, and so the σ is tunable. And finally, the interfaces of 2D materials in some cases can help to lower the κ. Therefore, additional experimental investigation into the thermoelectric properties of these materials would help to assess their viability for small-scale energy harvesting or self-powered sensors. In practice, to harvest large enough amounts of energy for most useful applications, some kind of composites with 2D materials would likely be necessary.

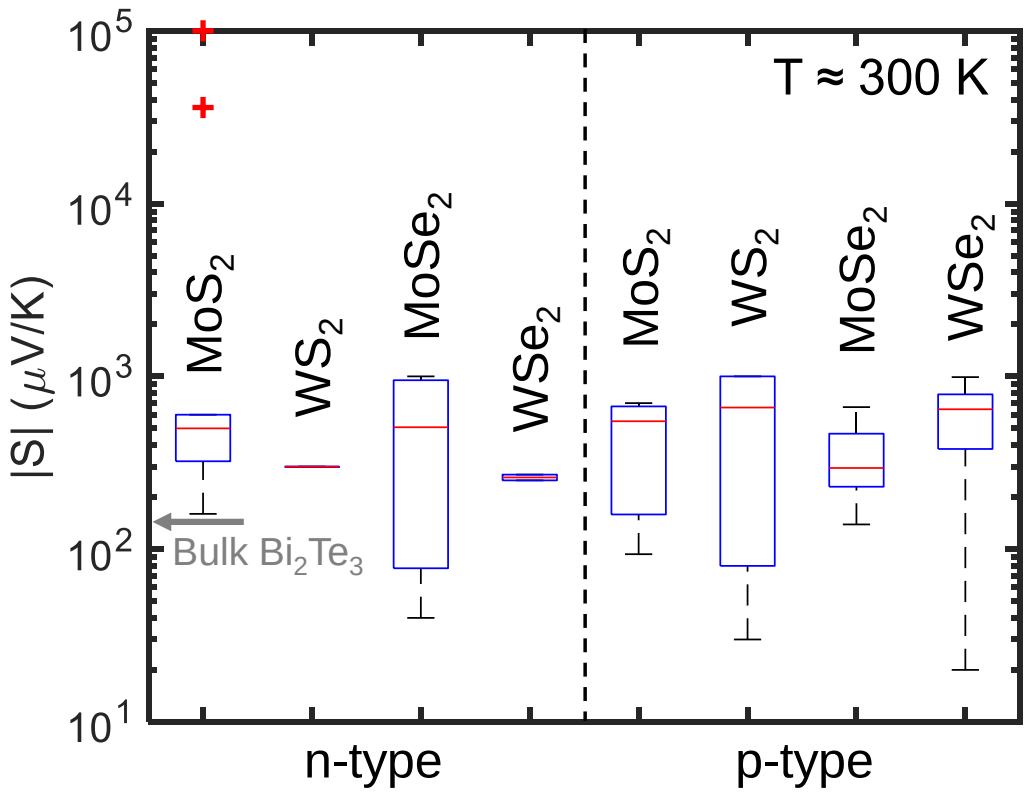

Figure 1.8: A plot of experimentally measured Seebeck coefficients for four common TMD materials – MoS_2 [19-31], WS_2 [32-37], $MoSe_2$ [34, 38-45], and WSe_2 [25, 32-34, 38-41, 46, 47]. N-type data is plotted on the left, and p-type on the right, using the absolute value of the Seebeck coefficient in order to include the negative n-type Seebeck values on the same axis as the positive p-type. The red "+" symbols represent outlier points. These measurements are at ~300 K, and a value for bulk Bi_2Te_3 is indicated with a gray arrow [48].

Prior experimental work has been done on measuring the thermoelectric properties of TMD materials, and some of these are plotted in Figure 1.7 for four commonly studied TMDs – MoS_2, WS_2, $MoSe_2$, and WSe_2. These compiled measurements at room temperature span from monolayer to bulk, and include in-plane, cross-plane, as well as intermixed samples (typically resulting from spark plasma sintering). A value for bulk Bi_2Te_3 is indicated with a gray arrow, and it is evident that many measured TMD Seebeck coefficients fall above that of the commonly used commercial thermoelectric

material. The majority of Seebeck measurements for these TMDs fall around the order of ~10^2 μV/K; however, we note that there are a couple points above this range (the outliers that are indicated with red "+" symbols) [23, 49]. These values are at extremely low carrier densities, and therefore represent samples with a low electrical conductivity.

1.3 Edge Effects in 2D Materials

1.3.1 Fundamental Properties of the Edges

As devices fabricated with 2D material channels scale to narrower channel widths, the contribution from the edges becomes increasingly significant. If the edges are either pristine armchair or zigzag configurations, they can have unique electrical, optical, and magnetic properties. These edge configurations are schematically illustrated in Figure 1.8.

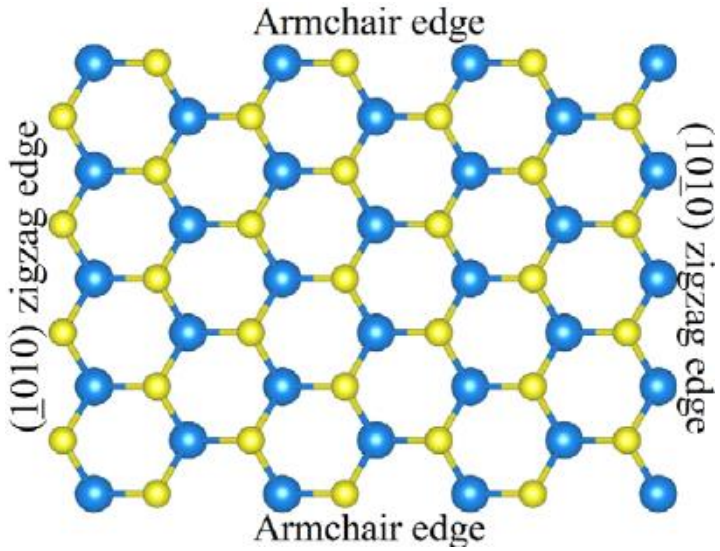

Figure 1.9: A schematic illustration of different zigzag and armchair edges for a top-down view of a monolayer of MoS_2 [50].

Depending on the orientation of the edges, they may contribute states in the band gap of the MoS_2 channel, and this can lead to shifts in the band structure and even metallic behavior [51]. One example of this is shown in Figure 1.9, where the evolution in band structure for increasingly narrow MoS_2 channels has been computationally evaluated. Through this figure, it is evident that narrowing the MoS_2 material leads to a more

dramatic change in the band structure, deviating from that of the center material. These calculations are for an armchair edge configuration.

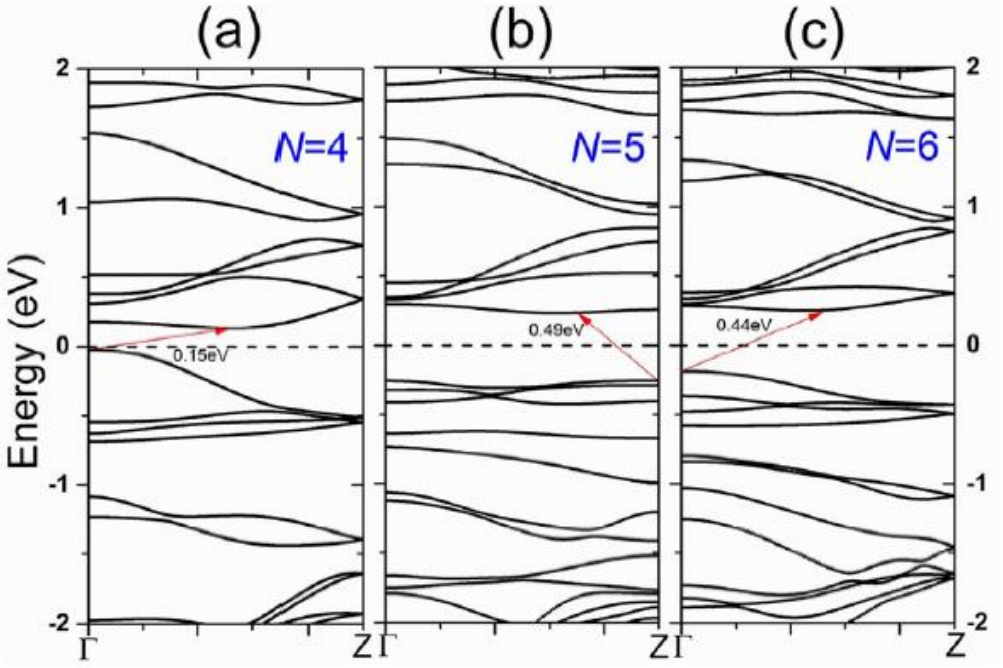

Figure 1.10: Calculated energy band structures for armchair MoS_2 nanoribbons with varying widths, where N represents the number of dimer lines in the structure [51]. Narrower MoS_2 ribbons display a shrinking band gap compared to the wide material due to the increasing contribution from these edges.

Practically, this contribution from edge states would lead to increased electronic conduction below the threshold voltage when the center of the MoS_2 channel should be in the off state. This has been experimentally demonstrated through the use of microwave impedance microscopy (MIM) on MoS_2 transistors, pictured in Figure 1.10 [52]. Figure 1.10(a) displays the MIM-Im (the imaginary component of the small changes of tip-sample admittance) images from the edge of an exfoliated MoS_2 sample. As the back-gate voltage (V_{BG}) increases, the edges appear to turn on before the center of the channel. This is confirmed in Figure 1.10(b), which shows averaged line profiles of these data. Finally, in Figure 1.10(c), the calculated sheet conductance for the edge and bulk are plotted against V_{BG}, and displays conductance from the edges below the threshold voltage for this device. This experimental demonstration of edge conduction furthers the assertion

that the edges will have an impact on the electronic performance of a scaled, narrow 2D channel.

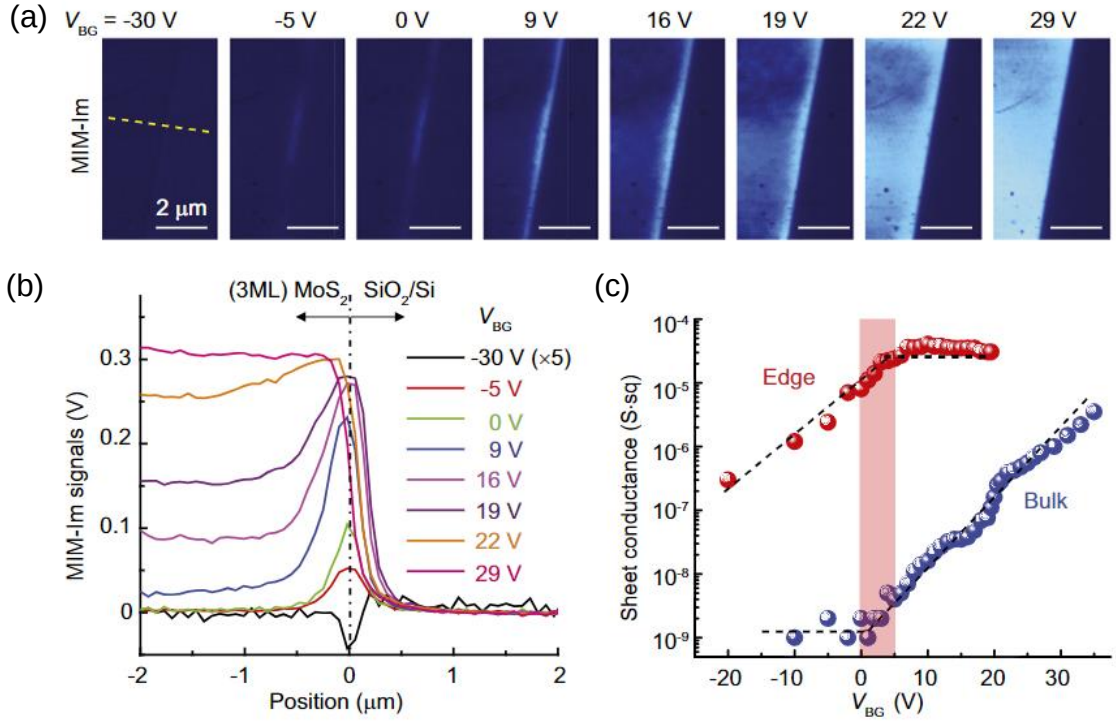

Figure 1.11: (a) MIM images from the edge of an exfoliated MoS_2 sample with varied applied back-gate voltage, V_{BG}. (b) Line profiles of the MIM-Im signals as a function of position and V_{BG}. (c) The edge and bulk conductance plotted vs. V_{BG}, showing the presence of conductive edge states before the bulk of the sample is turned on [52].

1.3.2 Nanoribbon Devices from Prior Literature

Experimentally, nanoribbon devices have been studied through various methods of fabrication. Some of these works (on MoS_2 specifically) are compiled in Table 1.1, along with pertinent measured electrical properties. The works in this table were able to obtain their narrow, sub-100 nm wide MoS_2 channels through combinations of exfoliation or chemical vapor deposition (CVD) and etching – utilizing BCl_3, SF_6, XeF_2, or UV/ozone. Back-gated devices were then fabricated with evaporated top-contacts, and the transistor characteristics were measured. Device details, peak mobilities, and I_{on}/I_{off} ratios are listed in Table 1.1. These prior works also note electronic phenomena such as positive

threshold voltage shifts for narrower MoS_2 channels [53, 54] and Coulomb diamonds at low temperatures, where the device is small enough such that electrons in the channel create a Coulomb repulsion, preventing others from flowing and resulting in oscillations in the current-voltage curve [55, 56].

However, as mentioned previously, many unique properties arise from pristine edges, either in the armchair or zigzag structure. The works that are compiled in Table 1.1 study MoS_2 nanoribbons that were ultimately formed through some etch step, and therefore it is likely that there is some disorder or roughness at the edges. Ideally, we would like to measure the electrical transport properties of TMD nanoribbons with narrow channels that do not undergo any etching, and this is explored later in the thesis.

Finally, in back-gated device structures where the oxide thickness is greater than the width of the TMD nanoribbon, it is important to consider the effects of the fringing capacitance, especially when calculating the mobility of the devices [56, 57]. If the contribution from the fringing capacitance is neglected, then this can lead to an overestimation of the mobility. Figure 1.11 plots the relative contribution from the fringing capacitance (C_{fringe}) to the total capacitance for a 285 nm SiO_2/Si back-gated device, where the C_{fringe} becomes considerable for channel widths < 100 nm [56].

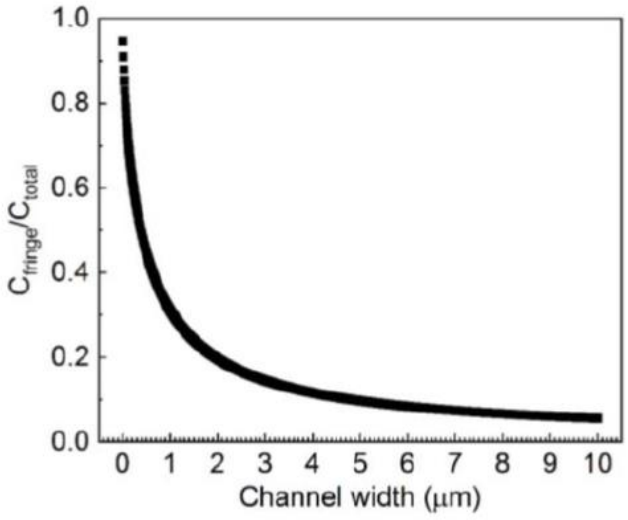

Figure 1.12: The relative contribution of the fringing capacitance (C_{fringe}) to the total capacitance ($C_{total} = C_{parallel} + C_{fringe}$) vs. the MoS_2 ribbon width for a 285 nm SiO_2/Si back-gated device [56, 57].

Table 1.1: Selected works on MoS_2 Nanoribbon Devices

Ref.	W_{ch} (nm)	Fabrication Method	MoS_2 Thickness	Gating	Mobility ($cm^2V^{-1}s^{-1}$)	I_{on}/I_{off}
H. Liu et al. [53]	60	Exfoliated, ebeam to define channel with PMMA, plasma dry etch (BCl_3)	6 nm	300 nm SiO_2/Si back gate	Not reported for 60 nm channel	10^5
D. Kotekar-Patil et al. [55]	50	Exfoliated, ebeam to define channel with PMMA, plasma dry etch (SF_6)	Monolayer	300 nm SiO_2/Si back gate	22	10^4
D. Kotekar-Patil et al. [58]	50	Exfoliated, ebeam to define channel with PMMA, plasma dry etch (SF_6)	Monolayer	300 nm SiO_2/Si back gate	50	10^5
S. Chen et al. [54]	30	CVD, scanning probe lithography to deposit polymer structures, XeF_2 etch, Al_2O_3 capped	Monolayer	285 nm SiO_2/Si back gate	8.5	2×10^5
X. Li et al. [56]	8	CVD bilayer, etch bottom layer with UV/ozone	Bilayer	285 nm SiO_2/ Si back gate	4	10^4

1.4 Thesis Organization

The objective of this work is to investigate unique properties of 2D materials in order to further understand their potential as candidates for scaled electronic applications. Towards this end, we examine the synthesis of one electrically insulating 2D material, hexagonal boron nitride, as well as study fundamental properties of TMDs that could affect their integration into larger-scale applications. We report thermoelectric measurements of WSe_2, and additionally study edge effects through electrical measurements of MoS_2 and WSe_2 nanoribbons.

Chapter 1 provides an introduction to 2D materials, highlighting some challenges with current Silicon device scaling and providing an overview of a few unique properties of the 2D material family. This chapter additionally briefly describes the thermoelectric effect as well as edge effects in 2D materials.

Chapter 2 is an overview of work towards large-area chemical vapor deposition (CVD) of hexagonal boron nitride (h-BN) on a variety of substrates, with tailored film properties depending on the target applications. This section additionally discusses applications for thin h-BN films.

Chapter 3 covers ambipolar, layer-dependent thermoelectric characterization of thin WSe_2, highlighting the design of the thermoelectric test structure and reporting measurements for multiple WSe_2 samples.

Chapter 4 describes our investigation of exfoliated TMD nanoribbons, with scanning electron microscopy (SEM) imaging and device fabrication. Through electrical characterization of numerous MoS_2 and WSe_2 nanoribbon devices, our initial results show some preliminary evidence of edge contribution towards narrow TMD devices.

Finally, Chapter 5 summarizes conclusions and provides some thoughts on future work to build upon the projects described in this thesis.

Chapter 2

Synthesis of Hexagonal Boron Nitride

In this chapter, we investigate the material properties of h-BN deposited using chemical vapor deposition (CVD) on metal and carbon nanotube (CNT) substrates. We make the first direct comparison of h-BN monolayer films deposited on polycrystalline Pt and on single crystal Pt, demonstrating reduced surface roughness and greater film uniformity for h-BN from the single crystal substrate. In addition, we discuss numerous potential applications and demonstrate the use of an h-BN monolayer as an ultrathin 3.33 Å barrier for protecting MoS_2 from damage in an anneal above its oxidation temperature. Our results will also help guide substrate choices for future h-BN work, depending on the application. This chapter is adapted from our published work, V. Chen, et al., "Application-driven synthesis and characterization of hexagonal boron nitride deposited on metals and carbon nanotubes," 2D Materials, vol. 8, p. 045024, 2021 [59].

2.1 Introduction and Methods

2.1.1 Introduction to Hexagonal Boron Nitride

The family of two-dimensional (2D), layered materials are characterized by relatively strong in-plane bonds and weaker out-of-plane van der Waals coupling between layers. While there has been significant interest in the electrically conductive graphene and semiconducting transition metal dichalcogenides (TMDs), there are also numerous applications for an electrically insulating 2D material. Hexagonal boron nitride (h-BN) in its monolayer form has a “thickness” of 3.33 Å, taken as the interlayer spacing of the bulk material [60]. With an electrical band gap of 6 eV, h-BN is an electrical insulator structurally similar to graphene, but composed of ionically bonded boron and nitrogen atoms [61, 62]. This structure, which contains no out-of-plane dangling bonds, results in the h-BN film’s high mechanical strength, chemical inertness, and extremely high in-

plane thermal conductivity – even greater than the thermal conductivity of bulk copper near room temperature [9, 63-68]. An illustration of the atomic structure of multilayer h-BN is depicted in Figure 2.1.

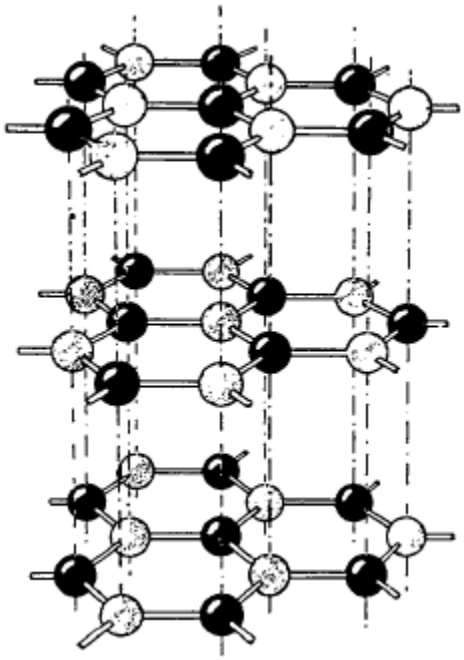

Figure 2.1: One possible stacking arrangement of multilayer h-BN, illustrating the one-atom-thick hexagonal structure of each layer [60].

The unique characteristics of h-BN have made it demonstratively useful as the gate dielectric in a 2D field effect transistor (FET) [69], substrate and encapsulant for record high velocity saturation in graphene [70], passivation layer to protect air-sensitive materials as well as prevent electromigration [71, 72], and substrate for heat spreading [73]. While mechanical exfoliation from a bulk crystal can yield micron-sized h-BN flakes for proof-of-concept experiments, large area, continuous h-BN films are necessary for practical applications. A promising method to achieve this goal is through low-pressure chemical vapor deposition (LPCVD) at temperatures >900°C [63, 74-76]. Monolayer and multilayer h-BN films have been grown on a variety of substrates, including metals such as copper, platinum, and nickel, and work is also being done in order to improve the scalability of these processes [76-80]. In addition, h-BN can be

deposited on silicon-based substrates (SiO_2 and Si_3N_4) although the resultant film grain size is limited to ~10-20 μm [81, 82], and by low-temperature electron-enhanced atomic layer deposition (ALD) in nanocrystalline form [83]. These studies have demonstrated that substrate material and crystallinity influence h-BN growth rates, spatial uniformity, and film quality. Researchers have also reported differences in h-BN film properties among different grains of the same growth substrate, another important factor to consider when targeting a uniform, high-quality film for several applications [74, 84].

However, despite growing interest in this material, a direct comparison of monolayer h-BN grown by CVD from an air-stable, solid-source precursor on polycrystalline Pt and single crystal Pt using the same deposition conditions has not been previously reported. Because Pt is a frequently used growth substrate, it is vital to understand the differences in film properties from different Pt crystallinities. Additionally, the characterization of h-BN deposited directly onto both single crystal Pt as well as other unconventional substrates (e.g. carbon nanotubes, CNTs) is relatively limited, even though direct deposition onto CNTs could enable improved device performance as gate dielectrics and CNT protection without requiring the transfer of h-BN. An in-depth study of CVD h-BN on a number of substrates can open doors to a variety of potential applications with unique requirements for the film properties.

Here we report the LPCVD of monolayer h-BN films on single crystal and polycrystalline Pt substrates, as well as multilayer h-BN films on both polycrystalline Cu foil and aligned, single-walled CNTs. From the metal growth substrates, the h-BN films are transferred off and characterized using atomic force microscopy (AFM) and Raman spectroscopy, yielding new data that illustrate h-BN film characteristic variations between h-BN from polycrystalline Pt vs. single crystal Pt. We additionally show cross-sectional transmission electron microscopy (TEM) images of the crystalline multilayer h-BN films from the Cu substrate and CNTs. Only one previous study [85] has experimentally shown CNTs wrapped with few-layer h-BN; going beyond this, here we provide the first demonstration of CNTs capped with as-grown h-BN, and their electrical characterization. We also demonstrate, for the first time, the use of monolayer h-BN as an ultrathin capping layer that protects monolayer MoS_2 from degradation in high temperature conditions.

2.1.2 Deposition Substrates and Growth Parameters

Large-area (on the order of cm^2) h-BN films were prepared by LPCVD in a 2" diameter furnace that is schematically represented in figure 1(a). The Pt growth substrates (polycrystalline and single crystal) are placed on a quartz boat inside the furnace chamber and heated to 1100°C, the Cu substrate to 1050°C, and the CNTs on quartz substrate to 1100°C. In each case, the air-stable, solid source precursor, ammonia borane (H_3NBH_3), is placed in an ampoule that is heated independently from the main furnace chamber. The ammonia borane is heated to 100°C, at which point it decomposes into borazine [$(HBNH)_3$], polyiminoborane (BHNH), and hydrogen [86]. H_2 is used as the carrier gas for the borazine to diffuse through the furnace which is at ~900 mTorr and onto the growth substrates. The metal substrates were annealed at their respective growth temperatures for 40 minutes prior to the h-BN growth, which serves to remove impurities and, in the case of Cu, smooth the substrate surface. The substrates and relative thicknesses of h-BN deposited are schematically summarized in Figures 2.2(b)-(e).

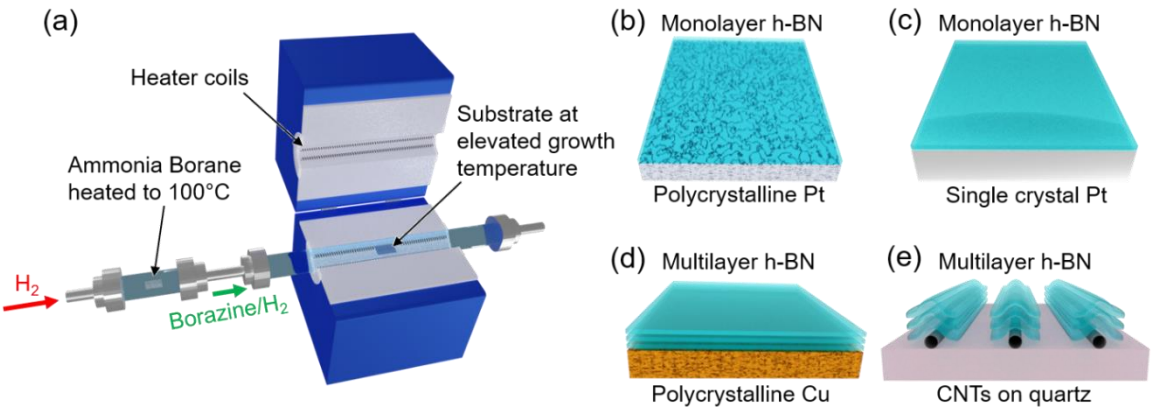

Figure 2.2: Schematics of the CVD furnace and growth substrates. (a) The CVD system used for h-BN growth, (b) monolayer h-BN on a polycrystalline Pt substrate, (c) monolayer h-BN on a single crystal Pt(111) substrate, (d) multilayer h-BN on a Cu substrate, and (e) multilayer h-BN on carbon nano-tubes (CNTs) on a quartz substrate.

The monolayer h-BN growth on Pt substrates is hypothesized to occur by physisorption after the thermal decomposition of the borazine [87]. After the initial monolayer is formed on these surfaces, the surface reactivity decreases and therefore the formation of additional h-BN layers slows, so that the CVD process on Pt is effectively limited to one monolayer at the growth pressure of ~900 mTorr, without the presence of bilayer regions [88]. On the other hand, it should be noted that other works report few-layer regions of h-BN deposited on polycrystalline Pt with different CVD conditions [84, 89]. Therefore, it is evident that the growth mechanisms are highly dependent on variables such as the precursor temperature and pressure of the furnace chamber.

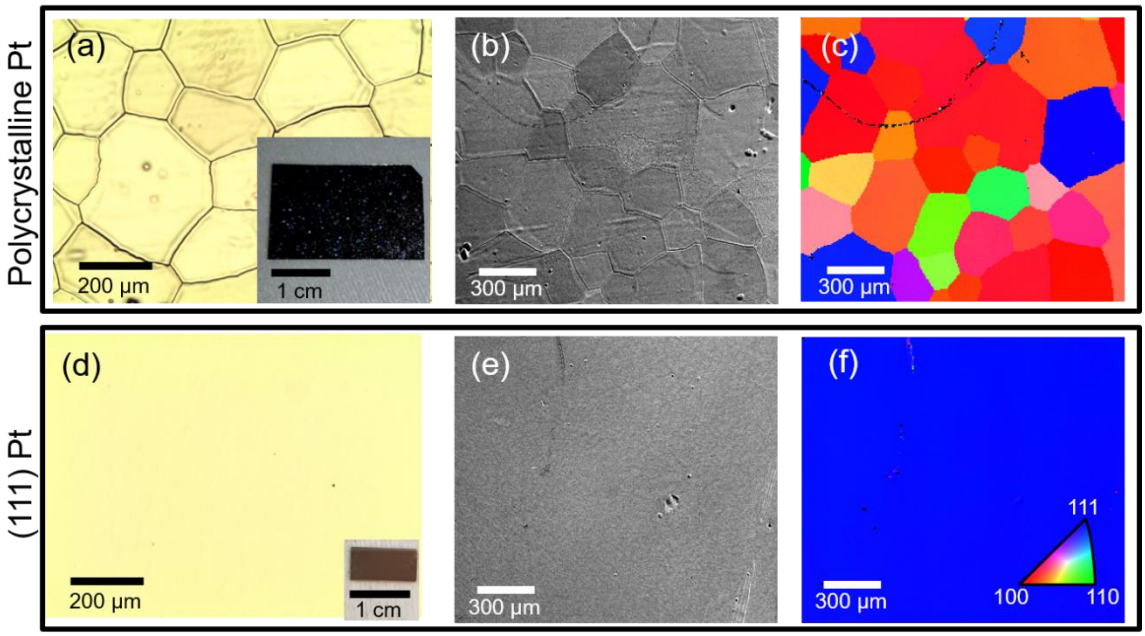

Figure 2.3: Imaging and characterization of Pt growth substrates for h-BN. (a) Zoomed-in optical image of polycrystalline Pt (inset zoomed-out, showing entire foil), (b) scanning electron microscope (SEM) image and (c) EBSD of the same polycrystalline Pt, showing the individual grains and grain boundaries. (d) Zoomed-in optical image of single crystal Pt(111) growth substrate (inset zoomed-out, showing entire sample), (e) SEM image and (f) EBSD of the same single-crystal Pt substrate.

Figure 2.3 compares the polycrystalline Pt with the single crystal Pt(111) substrate. Figure 2.3(a) shows a magnified optical image of the polycrystalline Pt foil, with an inset of a photograph of the substrate. Grains on the order of a few hundred μm appear as "sparkles" to the naked eye due to different crystal orientations of the grains reflecting light differently. These grains are also shown by SEM in Figure 2.3(b) and EBSD in Figure 2.3(c). The boundaries between different Pt crystal orientations are very clear in the SEM and EBSD images, and these relatively sharp boundaries indicate that the grain size of the Pt substrate may be a limiting factor in the grain size of the h-BN that is grown. This hypothesis is further explored through TEM imaging, where we map the spatial orientation of a monolayer h-BN film that was grown on polycrystalline Pt and reveal clusters of points with the same h-BN orientation in regions of comparable areas to the polycrystalline Pt grain size. Figure 2.3(d) shows an optical image of the single crystal Pt(111) substrate, with no grain boundaries visible optically or by the SEM image in Figure 2.3(e). EBSD in Figure 2.3(f) confirms the crystallinity. The surface of the Pt(111) substrate is smoother than the polycrystalline substrate and may demonstrate higher catalytic activity because of its relatively higher surface density of atoms (as compared to other crystal orientations). After characterizing the two Pt substrates, the same conditions (temperature, gas flow, and pressure) are used for CVD of h-BN growth on each. These h-BN films are then transferred with the same method onto 300 nm SiO_2 on Si substrates for further characterization.

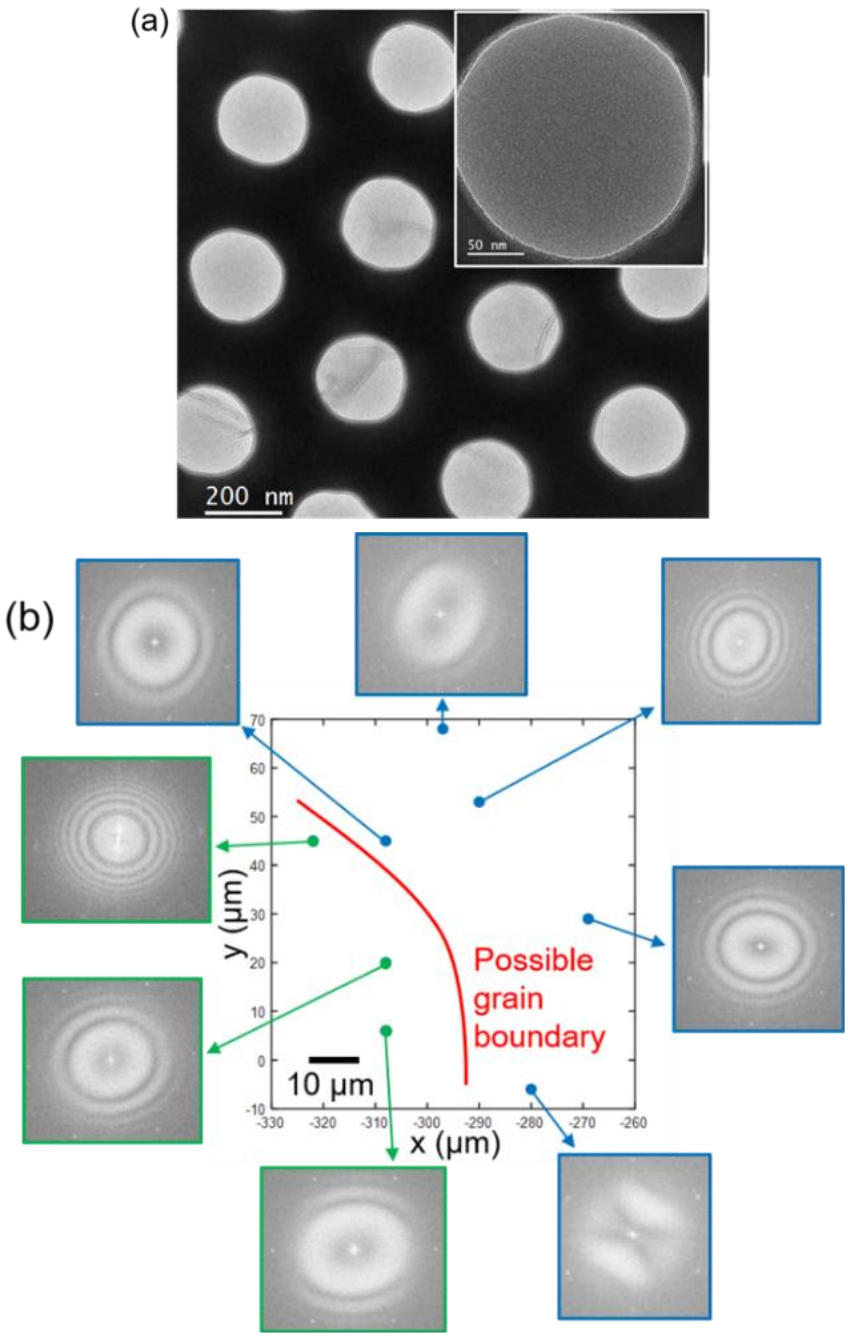

Figure 2.4: TEM images showing diffraction patterns of monolayer h-BN transferred from polycrystalline Pt to a SiN grid. (a) SiN grid with partial coverage of monolayer h-BN (inset showing zoomed-in image of one SiN hole) and (b) spatially mapped diffraction patterns showing similar h-BN orientations in regions of comparable size to the polycrystalline Pt substrate grain sizes.

For TEM imaging, we transfer monolayer h-BN grown on the polycrystalline Pt foil onto a SiN grid, and this grid is pictured in Figure 2.4(a). Then, by examining the diffraction patterns of the h-BN at different points spaced apart from each other in Figure 2.4(b), we observe two distinct clusters of points with two different orientations – one group of points is marked in blue and consistently shows the same orientation in spots up to ~80 μm apart, while the green points mark an adjacent region with a different orientation. A possible grain boundary between the two distinct orientations is sketched with a red line in Figure 2.4(b), and the size of the regions is comparable to the grain size of the polycrystalline Pt growth substrate. Although the number of points imaged was limited due to imperfect h-BN film transfer to these delicate SiN grids, the measured clusters of similar orientations supports the hypothesis that the polycrystalline Pt grain size is a limiting factor in the h-BN domain size.

The singular sets of diffraction spots in Figure 2.4(b) also serve as evidence that there cannot be multiple h-BN layers stacked in an AB orientation. While this does not definitively prove the presence of monolayer h-BN on its own (as there could be more than one layer still if they follow an AA' stacking order), it is further indication that the film is most likely a monolayer, an assertion also supported through other characterization techniques.

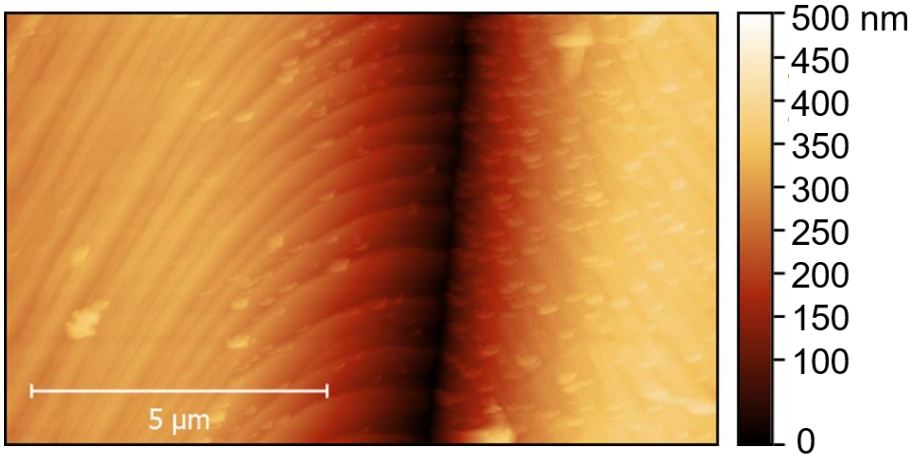

Figure 2.5: AFM topography scan over a grain boundary in the polycrystalline Pt substrate, illustrating the thermal grooving (~250 nm deep) occurring in the Pt.

Additionally, in Figure 2.5, we show an AFM topography scan over a grain boundary in the polycrystalline Pt. The AFM topography image in figure S3 maps the surface of the polycrystalline Pt at a grain boundary and shows evidence of thermal grooving. This occurs due to Pt atom migration at the high temperature and low pressure growth conditions, and is typically unavoidable for polycrystalline metals [90]. These relatively deep grooves contribute to the spatial non-homogeneity of h-BN deposited on the polycrystalline Pt and may be avoided through the use of single crystal metal growth substrates.

2.2 Results and Discussion

2.2.1 Transfer and Characterization of h-BN

After completing the h-BN growths, we used an electrochemical bubbling method at room temperature to delaminate the h-BN films from the Pt substrates [76], and a wet etching method to transfer them from the Cu substrate to SiO_2. This process allows the expensive Pt substrates to be reused for hundreds of growths with no measurable degradation in the substrates or in the grown h-BN quality. Simultaneously, by utilizing this low-temperature transfer process, the h-BN film can ultimately be deposited onto another substrate that is never exposed to the high-temperature growth conditions. Therefore, this process is compatible with applications which contain temperature-sensitive substrates. The majority of samples in this work were transferred onto a 300 nm SiO_2 on Si substrate for characterization purposes. Transferring the h-BN films onto the same kind of substrates using the same transfer procedure ensures a fair comparison between films that were originally grown on different substrates.

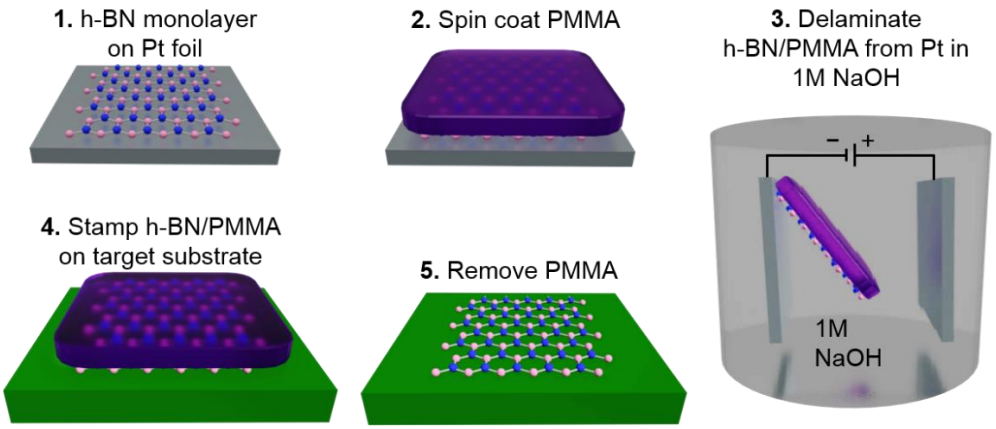

Figure 2.6: Schematic of transfer process illustrating the delamination of monolayer h-BN deposited onto Pt foil and transferred to the target substrate.

In order to transfer the h-BN monolayer films from the Pt growth substrates for characterization and comparison, we utilize an electrochemical bubbling-based transfer method that has been previously demonstrated [76, 91], as shown in Figure 2.6. After the h-BN is grown on the Pt foil, a 200 nm layer of PMMA is spun onto it and baked at 80°C on a hotplate for 30 min. Then, this stack is subsequently placed in a 1M solution of NaOH and attached to the negative terminal of a power supply, with another Pt foil as the positive electrode. Applying a voltage will generate bubbling at the interface of the h-BN and Pt, allowing the monolayer h-BN capped with the PMMA scaffold to peel off the Pt surface. Once the h-BN/PMMA stack is removed, it is subsequently rinsed in deionized (DI) water and then placed onto the target substrate. Immediately after, a nitrogen spray gun is aimed perpendicular to the sample surface, and the gentle gas flow is used to flatten the film and remove trapped air bubbles. The PMMA is then removed by soaking the sample in acetone for 30 minutes. This relatively clean transfer process allows for the continued reuse of expensive Pt foil substrates, as it does not require any etching and so can preserve the substrate and h-BN films.

While the large band gap of h-BN renders it somewhat optically transparent, especially for such thin films, we are able to see some optical contrast on the 300 nm SiO_2/Si substrates. The presence of h-BN is additionally verified using Raman spectroscopy, with a 532 nm laser and 100x objective. Bulk h-BN has a Raman peak

centered at approximately 1366 cm^{-1}. However, thinner h-BN films exhibit blue shifts up to ~4 cm^{-1} with monolayer samples having a peak centered at approximately 1370 cm^{-1} [92]. While this is commonly referred to as the E_{2g} peak, monolayer h-BN belongs to the D_{3h} point group, which differs from the bulk point group (D_{6h}). Therefore, we refer to this peak at ~1370 cm^{-1} as the E' peak. In monolayers, the E' peak can shift because of the slightly shorter B-N bonds resulting from the missing interlayer forces that would lengthen B-N bonds in multilayer h-BN [93]. To characterize film thicknesses and compare surface roughness, we use AFM in non-contact mode with a scan rate of 0.5 Hz. We use scanning electron microscopy (SEM) as well as electron backscatter diffraction (EBSD) with an accelerating voltage of 20 kV to examine and analyze the crystallinity of the metal growth substrates. Finally, the samples for cross-sectional TEM imaging were capped with a protective carbon layer and cut with a focused ion beam (FIB).

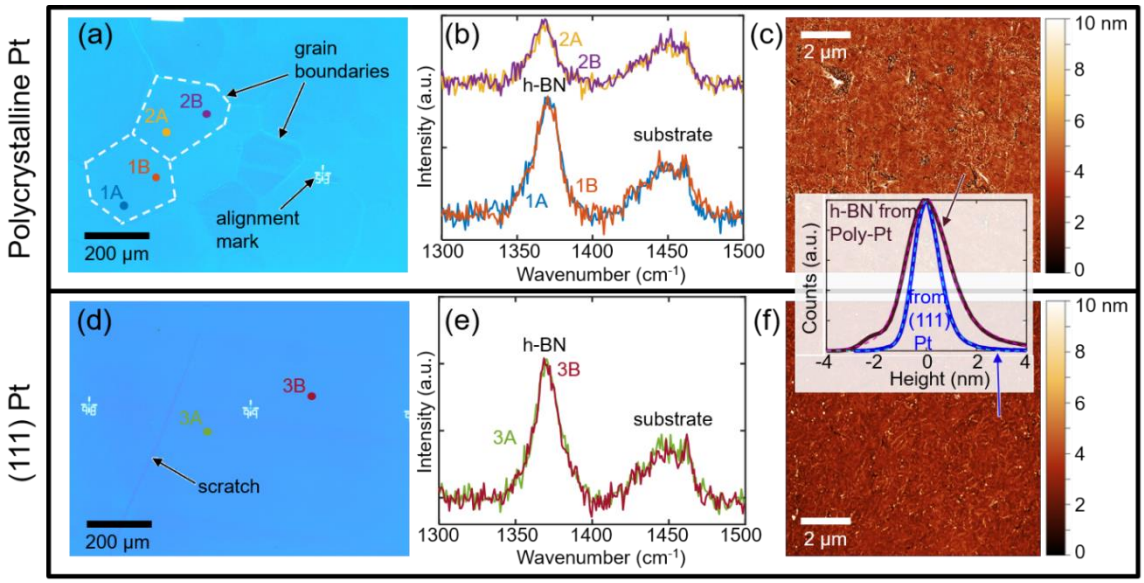

Figure 2.7: Characterization of grown h-BN transferred to SiO_2, from growth on (a-c) polycrystalline Pt foil and (d-f) on single-crystal Pt. (a) Optical image, (b) Raman spectra, and (c) AFM topography of h-BN from within a grain marked in (a). Raman signatures are the same within the same grain, but differ between grains. (Spectra offset for clarity.) (d) Optical image, (e) Raman spectra, and (f) AFM topography of h-BN grown on single crystal Pt(111) and transferred to a 300 nm SiO_2 substrate on Si. Raman signatures are the same across the uniform h-BN.

In Figure 2.7, we compare monolayer h-BN after transfer from the polycrystalline and Pt(111) substrates to the SiO_2/Si substrate. The bubbling-based transfer method has been demonstrated previously in the literature and is summarized previously in Figure 2.6 [76, 91]. Figures 2.7(a-c) show optical, Raman, and AFM images of the h-BN film transferred from the polycrystalline Pt substrate. Grain boundaries are visible optically in Figure 2.7(a), corresponding to the size and shape of grains from the original metal growth substrate.

Points on different regions of the h-BN film transferred from polycrystalline Pt have different Raman signal intensities as well, which may indicate differences in film quality, coverage, and strain. This is illustrated in Figure 2.7(b), with points 1A and 1B from the same domain showing very similar signals that both differ from points 2A and 2B in an adjacent domain. The characteristic E' Raman peak of h-BN monolayer can be observed around 1370 cm^{-1}, and although there are small variations in its location, the peak still falls within the reported range for a monolayer [92]. The additional peak at ~1460 cm^{-1} is due to the Si substrate [82, 94]. By extracting the full width at half maximum (FWHM) values from Lorentzian fits of the Raman data, we also see that the average FWHM from grain 1 is approximately 18.6 cm^{-1}, whereas it is 16.9 cm^{-1} in grain 2. These FWHM values have been correlated with the in-plane grain size of the h-BN film, and therefore are evidence of spatial differences in film properties that may arise from different growth substrate grains [95].

The h-BN Raman peaks from different grains in Figure 2.7(b) are also slightly shifted in wavenumber with respect to each other. This variation is common for h-BN monolayers and may be indicative of differing amounts of strain in the different grains of the film. Strain levels < 1% can shift the peak by 1 to 2 cm^{-1}, which explains the observed variations in the monolayer measurements [92]. Small tears in the film can be seen in the AFM image in Figure 2.7(c) with the underlying SiO_2 exposed beneath, and the measured rms surface roughness on the surface of the h-BN film is 1.70 nm.

Figures 2.7(d-f) show optical, Raman, and AFM images of the h-BN transferred from the single crystal Pt(111) substrate; no grains boundaries are optically visible, but a

scratch made in the film provides contrast against the underlying SiO_2 substrate. The AFM image in Figure 2.7(e) has a rms surface roughness of 0.80 nm, which is lower than the film from the polycrystalline Pt even though identical transfer methods were used for each film. While surface roughness is an extrinsic measurement that is dependent on AFM scan size, resolution, scan speed, tip sharpness, and other factors, by using the same conditions for each scan we are able to compare the h-BN films from different growth substrates and conclude that the film from the Pt(111) substrate is smoother.

In the inset shared between Figures 2.7(c) and 2.7(f), we plot the height distributions of the AFM data for the h-BN films. The h-BN film deposited on the Pt(111) substrate shows a narrower distribution than the one from the polycrystalline Pt substrate, which supports the assertion that the h-BN film is smoother when grown on a single crystal substrate. Raman spectra plotted in Figure 2.7(e) are taken at two different points and have very similar intensities and FWHM values, indicating that the film quality and coverage are much more spatially consistent across the film. While these qualities are desirable for certain applications, a scalable process may be limited by the high cost of the single crystal Pt substrate. However, recent work has shown that large area (111) Pt can be synthesized in a cost effective method, therefore demonstrating a potential pathway forward [96]. We are also able to reuse the Pt(111) for numerous growths that do not measurably consume the substrate material.

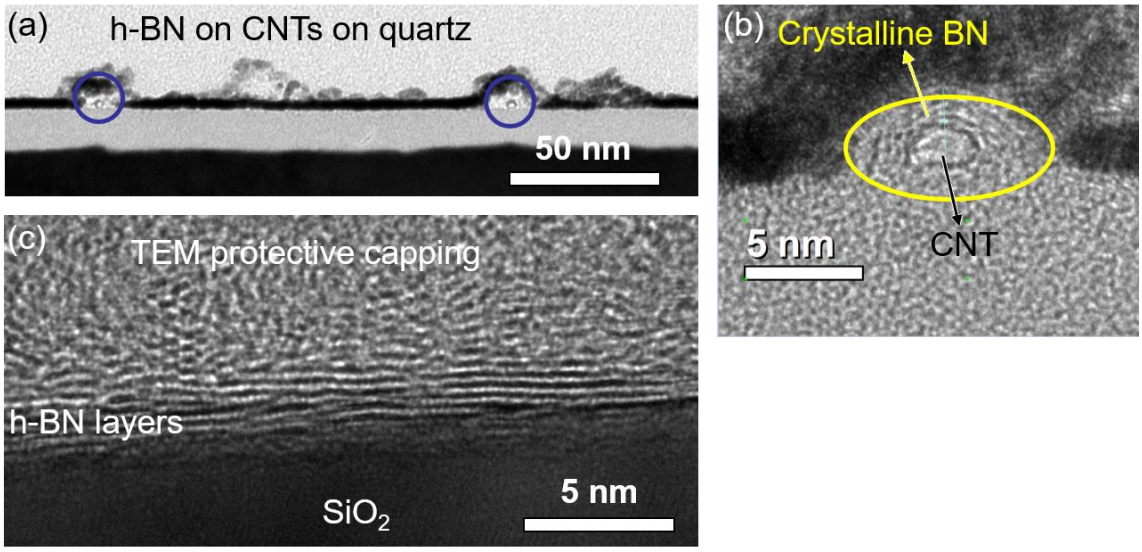

Figure 2.8: Cross sectional TEM images of crystalline, continuous multilayer h-BN grown by CVD on (a) single walled carbon nanotubes, with an image zoomed-in on one h-BN wrapped CNT in (b), and h-BN grown on (c) copper foil (but transferred to SiO_2 for imaging).

Next, we turn to multilayer h-BN films grown on CNTs/quartz and Cu foil. In Figure 2.8(a), the aligned, single-walled CNTs were grown on a quartz substrate and subsequently placed into the h-BN furnace without transfer [97]. From the TEM cross-section in Figure 2.8(a), it is evident that h-BN selectively deposits onto each individual CNT, but not on the quartz substrate between them. This is also clear in Figure 2.8(b), which shows a cross-sectional TEM of just one CNT that is conformally blanketed with few-layer h-BN. We can refer back to Figure 2.2(e) for a schematic illustration of this geometry. Capping CNTs with h-BN is appealing for improving the electrical performance of CNT transistors; the lack of dangling bonds and surface charge traps make h-BN a promising candidate for higher performance devices (e.g. as gate dielectric), as has been shown with graphene in the past [70, 98]. However, if the h-BN is grown on a different substrate and then transferred to the CNTs, residue left from the transfer process may degrade the transistor performance. Direct growth of h-BN on CNTs is a scalable method of deposition that avoids issues caused by the transfer process.

Finally, in Figure 2.8(c), we show the cross-sectional TEM image of multilayer h-BN that has been transferred to SiO_2 from Cu for characterization purposes. These ordered layers in Figure 2.8(c) are uniform across the image, demonstrating the spatial conformity of the deposited h-BN layers. In addition to depositing multilayers as opposed to monolayers with Pt, the h-BN on Cu may be used without transfer in specific applications, as the Cu substrate has a lower cost than Pt and therefore does not need to be reused for growths.

To further characterize the deposition of h-BN on carbon nanotubes (CNTs), we fabricate two-terminal CNT devices directly on their quartz growth substrates, with evaporated Ti/Pt contacts [97]. Each device has between 5 and 10 aligned CNTs between their electrical contacts, which are 1 μm apart. These CNTs were kept on their original growth substrate (quartz) to ensure that they would be pristine for the electrical tests, and not influenced by any transfer process or residue. We made two types of devices, 7 devices with h-BN deposited on top and 10 control devices without, as shown in Figure 2.9(a).

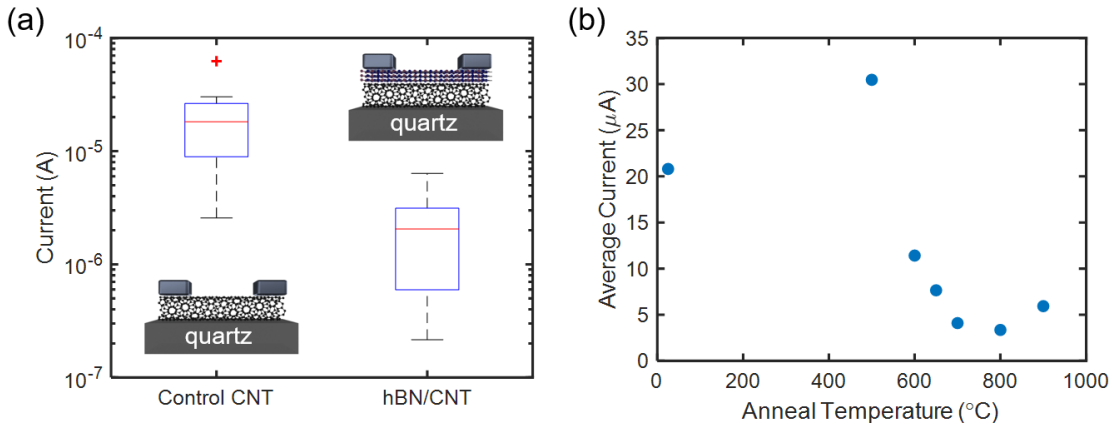

Figure 2.9: Electrical data showing (a) current degradation from 10 control CNT devices to 7 CNT devices after h-BN deposition (insets schematically illustrating the device structures) and (b) average current across CNTs after annealing at high temperatures without any precursor material, ensuring the lack of h-BN chemistry. This control experiment reveals that CNT current degradation occurs due to (unwanted) oxygen leakage into our furnace, not due to the h-BN growth chemistry.

The plot in Figure 2.9(a) shows that the CNT devices suffer some (partial) current degradation after the h-BN deposition, and the inset schematics illustrate the device structures. However, we find this current decrease is due to two main factors: the added contact resistance from the h-BN layers under the contacts and CNT oxidation from O_2 leakage into our furnace at high temperatures. The former issue is difficult to avoid here, as it would require etching the h-BN (under the contacts) without damaging the CNTs. The second issue, however, is more specific to our particular furnace setup and could be avoided with better, industrial furnaces.

To confirm the suspected O_2 leakage issue, we also performed several control measurements on similar CNT devices annealed at high temperatures *without* the use of the ammonia borane precursor. In other words, this replicated the temperatures and H_2/Ar gases the CNTs are exposed to during our h-BN growth process, except without the h-BN growth. The results in Figure 2.9(b) show that current degradation in these CNT devices occurs after they were exposed to furnace temperatures above 600°C, without the presence of any BN chemistry, which is due to oxygen and moisture entering the furnace chamber when it is pumped down to typical growth pressure (~900 mTorr) [99]. Although this effect is unavoidable in our specific academic CVD tool, the furnace chambers typically used for industrial applications have a much lower leak rate (~1 mTorr/min. or lower) [100]. Therefore, our demonstration of direct h-BN deposition onto CNTs could remain a viable technique for capping CNTs without the need for a transfer process, as long as the furnace leak rate can be mitigated.

2.2.2 Applications Discussion

Using the films discussed previously, we demonstrate the use of monolayer h-BN from the polycrystalline Pt as an encapsulation to protect monolayer MoS_2 from anneals at atmospheric pressure under 200 sccm H_2 and 200 sccm Ar flow up to 500°C.

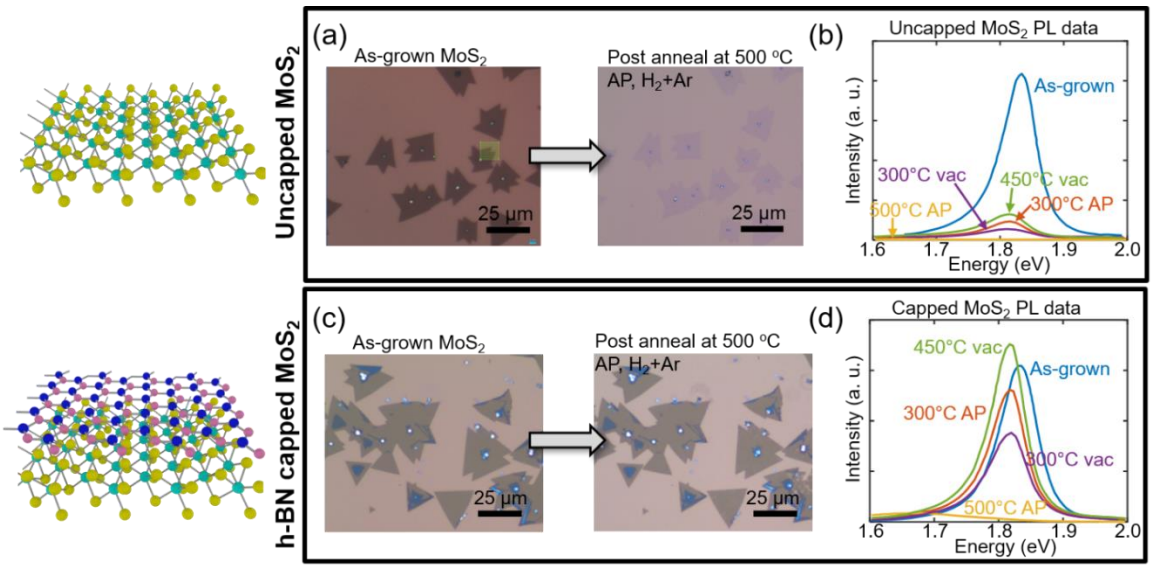

Figure 2.10: Optical and photoluminescence (PL) data on bare vs. h-BN capped MoS_2 exposed to elevated temperature conditions. (a) Optical images showing uncapped MoS_2 on SiO_2 before and after a 500°C anneal at atmospheric pressure (AP) with H_2 and Ar, (b) photoluminescence data for as-grown, uncapped MoS_2 and MoS_2 films after anneals under vacuum (vac) and atmospheric pressure conditions (c) Optical images of h-BN capped MoS_2 before and after anneal, and (d) photoluminescence data of the h-BN capped MoS_2 after the same anneals.

Figure 2.10 shows optical images and photoluminescence (PL) spectra for MoS_2, as grown and after annealing. The MoS_2 is grown on SiO_2 on Si using CVD [101], and in Figure 2.10(a) immediately undergoes an anneal at atmospheric pressure in a H_2/Ar environment at 500°C; the optical images showing the film before and after clearly illustrate film degradation from the high-temperature environment. Degradation of MoS_2 films exposed to elevated temperatures in a hydrogen atmosphere has been previously shown [102, 103] and our PL results confirm this phenomenon. Figure 2.10(b) shows PL spectra from MoS_2 films that are annealed under different conditions, and there is significant quenching of the PL peak even down to anneals at 300°C, indicating damage to the film. On the other hand, by transferring a monolayer of h-BN to blanket the MoS_2 prior to the anneal, the MoS_2 film is protected from degradation, as shown optically in

Figure 2.10(c). In Figure 2.10(d), the PL spectra are retained for anneals up to 450°C, as further evidence that the MoS_2 is protected.

In comparison, similar results have been previously achieved with encapsulation by depositing ~15 nm Al_2O_3 onto the MoS_2 [104]. In other words, the results shown in Figure 2.10 of this work demonstrate an h-BN capping monolayer with similar film protection performance that is only one atomic layer thick – nearly 50 times thinner than the Al_2O_3 capping layer previously used. Oxidation prevention methods are a widely researched area, and h-BN is emerging as an extremely thin candidate that can sustain high temperatures while contributing minimal weight to components [105].

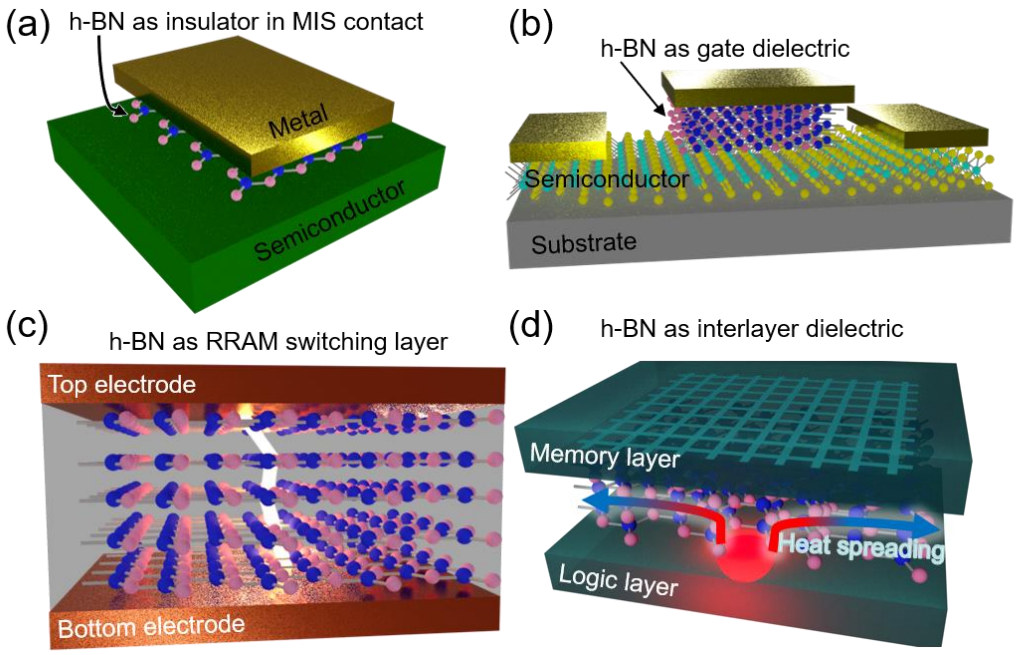

Figure 2.11: Examples of h-BN applications: (a) insulating layer in metal-insulator-semiconductor (MIS) contacts, (b) gate dielectric material, (c) switching layer in RRAM devices, and (d) interlayer dielectric material in a 3D IC to dissipate heat from a hot spot in the logic layer.

To further explore applications of h-BN, we summarize other potential uses in Figure 2.11. As schematically represented in Figure 2.11(a), h-BN may serve as the insulating layer in a metal-insulator-semiconductor (MIS) contact, depinning the Fermi level while acting as a solid-state barrier that prevents metal contacts from reacting with the semiconductor material. This concept has been experimentally demonstrated with both MoS_2 and $MoTe_2$ as the 2D semiconductor material [106, 107]. Along these lines, the h-BN lattice structure is highly impermeable to many small chemical species, and therefore is a useful solid-state barrier to prevent undesirable chemical reactions and preserve materials of interest [108]. With excellent measured dielectric properties, it has also been demonstrated as an ultra-thin gate dielectric material for transistors, opening a new potential avenue to explore in the field of transistor scaling [69, 70, 109-111]. This is schematically represented in Figure 2.11(b).

With Figure 2.11(c), we illustrate how multilayer h-BN grown on Cu foil can be used as the switching layer of a resistive random-access memory (RRAM) device, with defects utilized to form the conductive filament [112, 113]. Finally, the high in-plane thermal conductivity of h-BN makes it a promising candidate for heat spreading applications where an electrical insulator is required [73]. Because electrical and thermal conductivity are often positively correlated (e.g. for metals), materials with a high thermal conductivity that are electrical insulators are relatively rare (e.g. just diamond, BN, and AlN) [114]. In addition to this unique property, h-BN also has an anisotropic thermal conductivity between the in-plane vs. cross-plane directions, with a much lower cross-plane thermal conductivity [115]. This would make it valuable in applications where directional heat spreading is important. For example, Figure 2.11(d) shows h-BN as the interlayer dielectric material for a 3D integrated circuit, stacking a memory layer on top of a logic layer. The h-BN can spread heat laterally, and reduce peak hot spot temperatures from logic devices, while blocking the heat from affecting the memory layer above.

2.3 Summary

We have demonstrated a scalable method for depositing large-area h-BN films on various substrates (including crystalline Pt, polycrystalline Pt and Cu, and single-wall CNTs) and characterized the resulting films. The crystallinity of the substrates affects the properties of the h-BN as well as the resulting thickness of the film, and this knowledge can be used to selectively tailor the resulting h-BN film properties. In addition, direct growth on CNT and Cu substrates can enable use of the h-BN without a transfer being necessary. We also discuss applications for h-BN grown by CVD and use this material as an ultra-thin barrier layer to effectively protect a monolayer of MoS_2, allowing it to reach temperatures above the threshold at which it would typically degrade without sustaining measurable damage. This illustrates promising applications for h-BN as a protective coating against oxidation, which would be of use in numerous industries. While future work remains needed to reduce the growth temperature of h-BN and improve the transfer process when required, this study explores h-BN synthesis and specifies potential target applications that would utilize the carefully tuned properties of the films.

Chapter 3

Ambipolar Layer-Dependent Thermoelectric Measurements of Tungsten Diselenide (WSe_2)

Thermoelectric materials can harvest electrical energy from temperature gradients, and could play a role as power supplies for sensors and other small devices. Here, we characterize fundamental in-plane electrical and thermoelectric properties of layered WSe_2 over a range of thicknesses, from 10 nm to 96 nm, between 300 K and 400 K. The devices are electrostatically gated with an ion gel, enabling us to probe both electron and hole regimes over a large range of carrier densities. We measure the highest *n*- and *p*-type Seebeck coefficients for thin-film WSe_2, -400 and 740 μV/K respectively, reported to date at room temperature. We also emphasize the importance of the substrate thermal conductivity on thermoelectric measurements, providing a platform for future studies on other two-dimensional materials.

3.1 Thermoelectric Introduction

Over half of the energy generated by humanity is ultimately dissipated without being utilized, and the majority of that rejected energy is lost in the form of waste heat [116]. In this context, thermoelectric energy harvesting could play an important role, by converting spatial temperature gradients into an electrical voltage [14]. Most existing commercial thermoelectric devices are primarily based on Bi_2Te_3 and its related compounds; however, many of these materials are relatively inefficient and expensive [16, 117].

The efficiency of a thermoelectric material is quantified by its figure of merit, zT, which is defined as $zT = S^2\sigma T/\kappa$, where S is the Seebeck coefficient, σ is the electrical conductivity, T is the absolute temperature, and κ is the thermal conductivity. High zT can be achieved by maximizing the power factor $S^2\sigma$ and minimizing κ. This can be accomplished by tuning the material's (electron or hole) carrier concentration, but

because the constituent parameters of zT are interconnected, this can be a difficult process [14]. For example, S is inversely proportional to the material's carrier density while σ is directly proportional. Therefore, increasing the carrier density can cause varying effects on zT, depending on the regime.

Another method to achieve more efficient thermoelectrics is to consider novel material systems. For example, low-dimensional materials with quantum confinement effects are uniquely suited to have efficient thermoelectric properties. Due to sharp features in their density of states, certain semiconducting two-dimensional (2D) materials could achieve large Seebeck coefficients [17], boosting their power factor. Furthermore, the dominant presence of interfaces and mass differences between constituent atoms in some 2D materials can lead to relatively low thermal conductivity [118, 119]. Although some theory and experiments have been done on 2D material thermoelectric properties, additional in-depth studies are required before these can be considered a viable commercial technology [25-27, 46, 120-122].

In this work, we measure in-plane, thickness-dependent thermoelectric properties of WSe_2, probing both *n*- and *p*-type regimes. Among 2D materials, WSe_2 is relatively unique, as it is one of the few options that is readily ambipolar, either through gating or doping, which has also made it promising for nanoscale electronic applications [123-125]. Using ion gel gating, we can tune the Fermi level, evaluating S and σ over a range of carrier densities, mapping the power factor through its peak value, which is difficult to accomplish with traditional back-gating through a thick oxide [26, 126]. We measure peak room-temperature $S_p \approx 740$ μV/K for *p*-type and $S_n \approx -400$ μV/K for *n*-type, some of the highest reported values for WSe_2 to date. This establishes WSe_2 as a promising candidate for applications such as temperature sensing, which benefit from higher induced voltages in a given temperature gradient [127]. Such large thermopower may also play a role in WSe_2 devices such as transistors or diodes, contributing to significant heating or cooling depending on current flow direction [15, 128, 129].

3.2 Methods and Device Structure

In order to accurately measure the Seebeck coefficient of our WSe_2 films, it is important to sustain a constant, known temperature gradient across the material. To accomplish this, we use a measurement structure whereby the WSe_2 samples are placed on a glass substrate, which has a lower thermal conductivity than the commonly used SiO_2/Si substrates [130]. The lower thermal conductivity substrate also limits vertical heat spreading, resulting in a longer and more gradual lateral temperature gradient, which enables a greater temperature difference to be sustained across the WSe_2 sample. This effect is quantified in using finite-element method simulations showing a ~10× greater temperature difference (ΔT) across the sample when using a glass substrate. The larger ΔT, in turn, leads to a larger measurable Seebeck voltage, increasing the signal-to-noise ratio and reducing measurement error.

To highlight the importance of the choice of substrate in the thermal design of the test structure, we have performed thermal finite-element method simulations for a cross-section of the test structure (Figure 3.1). For the same heater temperature, we compare the temperature differences, ΔT, between the two thermometer lines for the glass substrate used in this work [Figure 3.1(a)] and a substrate with 300 nm-thick SiO_2 on Si [Figure 3.1(b)] similar to those used in other studies [26, 27]. The high thermal conductivity silicon substrate ($\kappa_{Si} \approx 140$ W/m/K for undoped Si near room temperature) acts like a thermal ground, causing the temperature at the top of the sample to drop close to ambient temperature (T_0) within a short distance (comparable to the SiO_2 thickness) from the heater line. This causes the temperatures on both thermometer lines, as well as their difference, to be much less than the heater temperature. This problem can be largely avoided by using a uniform substrate with low thermal conductivity, such as glass, for which ΔT between the thermometer lines is close to 10× that of the SiO_2/Si substrate.

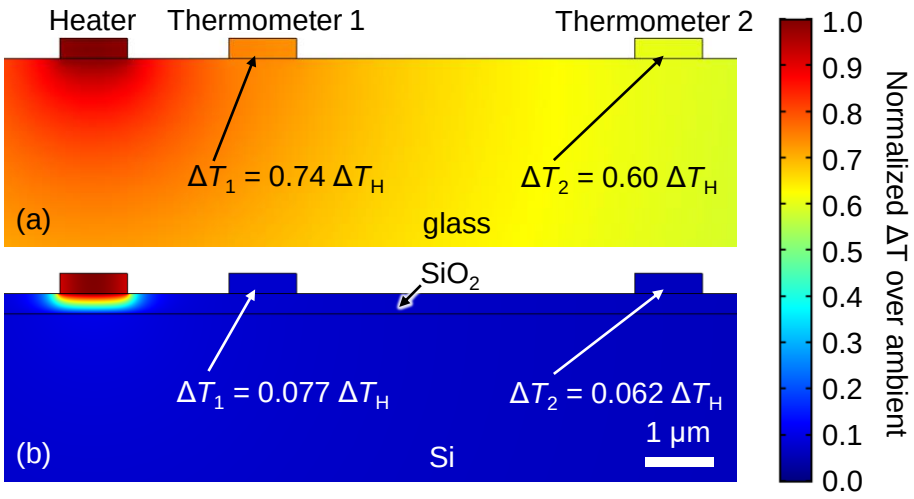

Figure 3.1: Normalized temperature rise ($\Delta T/\Delta T_H$) in the vicinity of the heater and thermometer lines for typical heater-thermometer line spacings, with (a) the glass substrate used in this work, and (b) a typical substrate with 300 nm-thick SiO_2 (κ_{SiO2} = 1.4 W/m/K) on Si. The temperature rise is normalized to the peak temperature rise in the heater line. The bottom of the substrate is assumed to be at ambient temperature, T_0. The thermometer temperature differences ($\Delta T_1 - \Delta T_2$) in (a) and (b) are 14% and 1.5% of the peak heater temperature rise (ΔT_H), respectively. The thicknesses of the metal lines have been exaggerated for this visualization (300 nm instead of the 40 nm thickness used in the experiments and simulation).

The WSe_2 samples are exfoliated from a bulk crystal using the "tape method" directly onto the glass substrates, and subsequently contacted with 40 nm of Pd deposited by electron-beam evaporation. An additional Pd line running parallel to WSe_2 contacts serves as the heater, as shown in Figure 1. While not in direct contact with the WSe_2 channel, this heater line is closely positioned and Joule-heated to create the lateral temperature gradient. All metal lines are ~400 μm long, significantly longer than the width of the WSe_2 sample, to ensure a one-dimensional temperature gradient along its length rather than any temperature gradients along the width, which would confound the measurement [131]. The Pd lines in contact with the WSe_2 serve as the source and drain for electrical transport measurements, as well as the resistive thermometers. These metal lines (except for the channel area) are then capped with 100 nm evaporated SiO_2 for

electrical insulation from the ion gel. Finally, a large Pd gate pad (with area on the order of ~mm^2) is deposited on the same platform, such that the ion gel can simultaneously bridge the gate pad and the WSe_2 sample. A schematic of this device is pictured in Figure 3.2(a), with a zoomed-in optical image in Figure 3.2(b). The WSe_2 sample thicknesses are determined by atomic force microscopy (AFM) measurements.

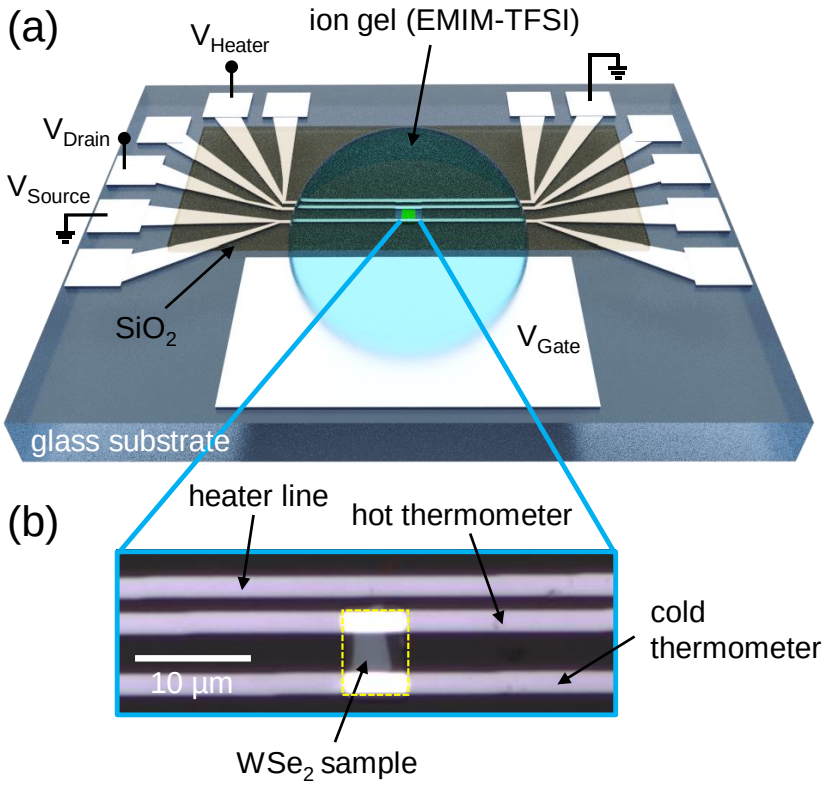

Figure 3.2: (a) Schematic of the electro-thermal measurement platform, on a glass substrate (not to scale). (b) Zoomed-in optical image of a WSe_2 sample with Pd contacts and heater line capped with 100 nm SiO_2 for electrical isolation. The dashed yellow line marks the window opened into the SiO_2, exposing the WSe_2 sample to the ion gel for electrostatic gating. The two thermometer lines in contact with the WSe_2 sample also serve as the source and drain for further electrical characterization.

To quantify the temperature gradient induced by the metal heater line along the sample, we calibrate our Pd lines by measuring their temperature coefficient of resistance (TCR). This is done by measuring the four-point resistance of each Pd thermometer line

at elevated temperatures, uniformly heating the substrate on a heated stage. Pd is chosen due to its chemical stability, linear TCR in the working temperature range, and good contact to WSe_2 [132-134].

The TCR is calculated as:

$$\alpha = \frac{R - R_0}{R_0(T - T_0)}$$

where α is the TCR, R is the measured resistance, R_0 is the resistance of the line at ambient temperature, T is the temperature, and T_0 is the ambient temperature.

Figure 3.3 shows plots of R/R_0 vs. $\Delta T = T - T_0$ for the two metal thermometer lines on each device, with dashed lines representing the linear fit from which the TCR is extracted. Although the TCR for thin Pd is well characterized in the literature, small nonidealities in the deposition and fabrication processes may cause the value to deviate slightly, and so it is still important to calibrate each line individually. The values are compiled in Table 3.1, and all fall within the expected range [132].

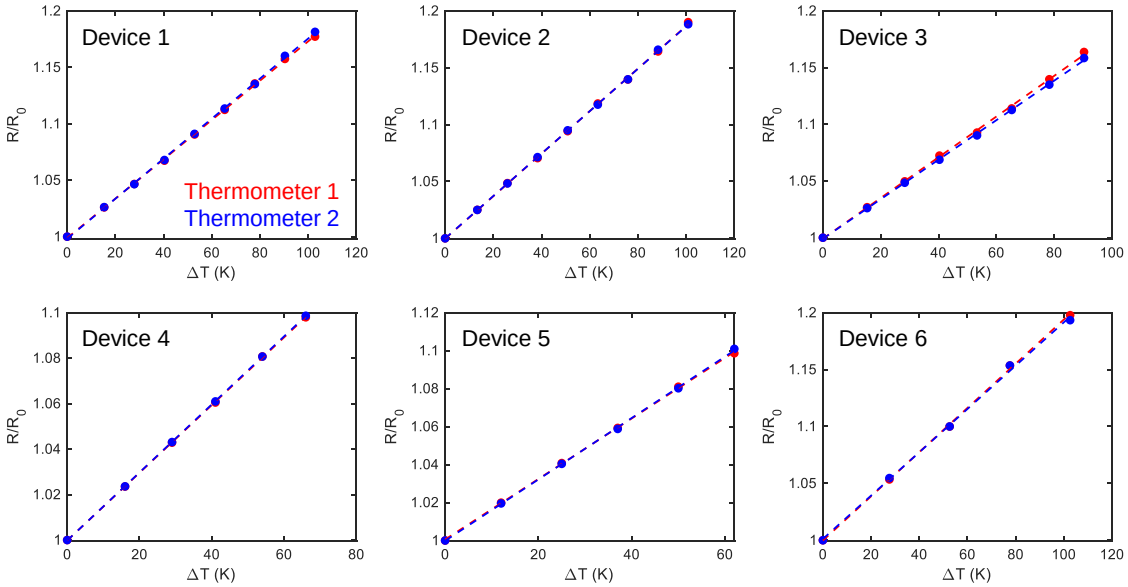

Figure 3.3: TCR calibrations for each of the two Pd thermometer lines on six devices. The four-point resistance is measured for each line at room temperature and elevated temperatures, and the ratio of the measured resistance (R) to the room temperature resistance (R_0) is plotted against the temperature increase. The dashed lines represent

linear fits of the data, and the slopes of these lines are the TCRs. The TCRs are listed in Table 3.1.

Table 3.1: Compiled Device Information

WSe_2 Device Parameters				**Pd Line Parameters**			
Device	**Thickness (nm)**	**Width (μm)**	**Length (μm)**	**TCR_{line1} (K^{-1})**	**TCR_{line2} (K^{-1})**	**R_{line1} (Ohms)**	**R_{line2} (Ohms)**
1	10	3.7	5.9	1.74×10^{-3}	1.77×10^{-3}	1104	1157
2	12	5.6	4.2	1.87×10^{-3}	1.86×10^{-3}	961	997
3	18	3.8	2.5	1.80×10^{-3}	1.74×10^{-3}	1202	1389
4	23	5.6	5.4	1.49×10^{-3}	1.50×10^{-3}	1440	1622
5	30	3.9	3.5	1.59×10^{-3}	1.62×10^{-3}	1420	1593
6	96	13.6	5	1.94×10^{-3}	1.90×10^{-3}	938	1030

Here, we tabulate the physical dimensions of each exfoliated WSe_2 sample, measured using atomic force microscopy (AFM). Although all Pd lines are nominally the same thickness of evaporated material, small differences in the processing conditions or imperfections in patterning may lead to differences in their TCR values and resistances. Therefore, we individually calibrate TCR values for each line separately and compile them in Table 3.1. There is some variation; however the measured TCR values are within a reasonable range for thin, evaporated Pd [132].

To modulate the carrier density and Fermi level, we use ion gel gating. This enables us to reach higher electron and hole densities on a glass substrate which is a better thermal insulator than the commonly used SiO_2/Si substrates, preserving a larger lateral temperature gradient. The ionic liquid EMIM-TFSI (1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide), is mixed with PS-PEO-PS triblock copolymer and dissolved in acetonitrile before being deposited on the WSe_2 channel to form an ion gel for more structural stability. The sample is then cured in air at 80 °C for 10 minutes. The ion gel contacts the WSe_2 channel as well as the gate pad, such that an applied voltage on the gate pad leads to an electric field over the channel.

3.3 Results and Discussion

3.3.1 Initial Electrical Characterization

We first characterize the electrical properties of the WSe_2 devices. Representative transfer (I_D vs. V_{GS}) and output (I_D vs. V_{DS}) characteristics are shown for a 96 nm thick sample in Figure 3.4(a) and 3.4(b), respectively. By utilizing an ion gel for gating, we are able to sweep over a large range of carrier densities with a relatively small gate voltage range. This device shows nearly "perfect" ambipolar behavior, i.e. it conducts both with electrons (for positive V_{GS}) and holes (for negative V_{GS}), and does so with nearly the same maximum current for both electron and hole branches in Figure 3.4(a). The maximum-to-minimum current ratio is $I_{max}/I_{min} \sim 10^8$, where I_{min} is limited by gate leakage and I_{max} reaches ~3 µA/µm at a low V_{DS} = 100 mV.

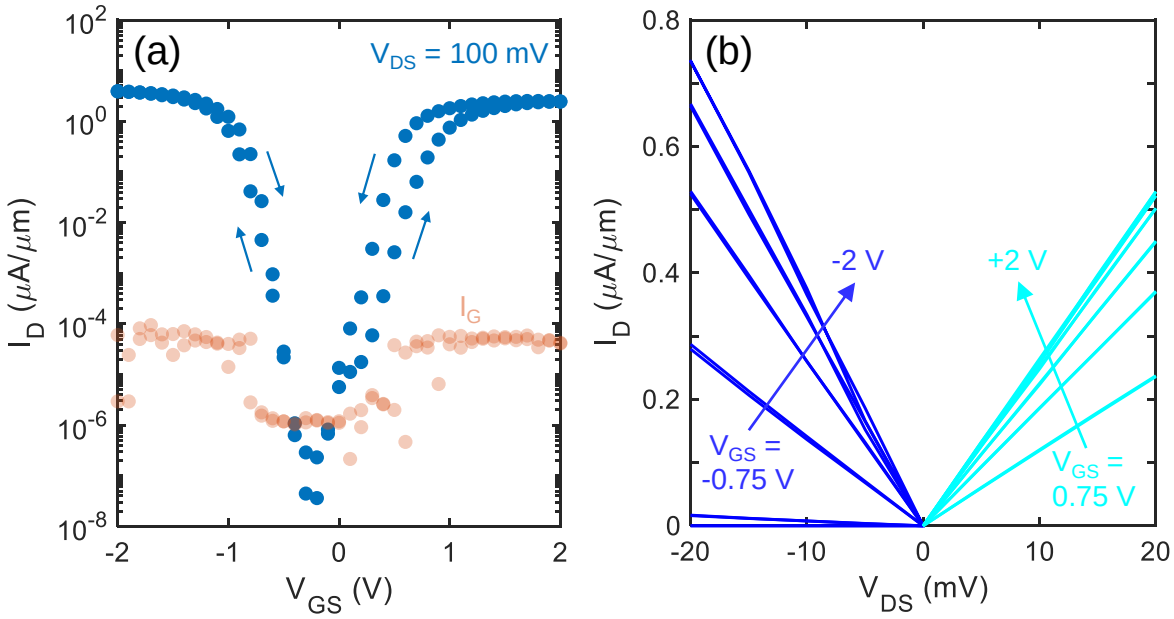

Figure 3.4: (a) Measured transfer (I_D vs. V_{GS}) characteristics of a WSe_2 sample that is 96 nm thick and 5 µm long, at room temperature. The gate leakage (light orange points) is minimized due to the SiO_2 layer insulating the metal lines from the ion gel. Small arrows mark voltage sweep directions. Hysteresis caused by the ion gel is minimized with a slow voltage sweep, 10 seconds at each data point. (b) Measured output characteristics (I_D vs. V_{DS}) of the same sample, taken in V_{GS} increments of 0.25 V. Negative and positive V_{GS} voltages are for hole and electron conduction, respectively.

Using these test structures and measurements, we investigate six different WSe_2 sample thicknesses, between 10 nm and 96 nm. Figure 3.7(a) displays the sheet conductance at each gate bias, $G_{sh} = (I_D/V_{DS}')(W/L)$, for the range of WSe_2 sample thicknesses investigated. The intrinsic voltage $V_{DS}' = V_{DS} - I_D R_{ser}$ subtracts out the series resistance R_{ser} caused by the long and thin Pd lines, which becomes a significant component when the channel is in the low-resistance on-state. These line resistances are measured in a 4-point configuration, their values are included in Table 3.1, and discussed further below. As shown in Figure 3.7(a), G_{sh} sharply drops for all devices in the off-state, at small $|V_{GS}|$ when the Fermi level is in the band gap. The WSe_2 channels are ambipolar and all show *p*- and *n*-type conduction, although any trend with thickness is not immediately apparent from these data.

Due to the relatively long and thin Pd lines used as the source and drain contacts to the WSe_2 samples, there is a series resistance added to the WSe_2 channel resistance that becomes especially significant when the channel is in the on-state. Therefore, to more accurately estimate the sheet conductance (G_{sh}) of the samples, we subtract the Pd line resistances as shown in the circuit diagram in Figure 3.5. We apply a drain-to-source voltage (V_{DS}), calculate the actual voltage drop across the WSe_2 (V_{DS}'), then use this V_{DS}' value to calculate G_{sh}. Here,

$$V_{DS}' = V_{DS} - I_D \frac{R_{line\,1} + R_{line\,2}}{2}, \text{ and therefore } G_{sh} = \frac{I_D}{V_{DS}'} \frac{L}{W}.$$

The four-point resistance values for each Pd line at room temperature are included in Table 3.1.

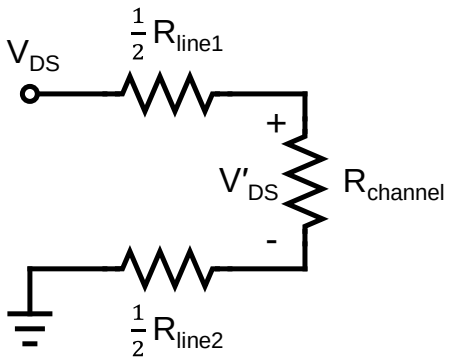

Figure 3.5: A simplified circuit diagram showing the current path through half of one Pd line, through the WSe_2 channel, and out through the other half Pd line.

3.3.2 Thermoelectric Characterization

During the Seebeck measurements, we apply a voltage bias across the heater line using a Keithley 2612 source-meter to Joule-heat it and create a lateral temperature gradient along the channel. We then measure the resulting open circuit voltage induced across the WSe_2 sample using a Keithley 4200 while simultaneously varying the applied gate voltage. The measured Seebeck voltage is then normalized over the temperature gradient (calculated using the calibrated TCR values mentioned previously) to calculate the Seebeck coefficients. All reported Seebeck values are relative to the contact metal, Pd. To verify that the measured Seebeck voltage is not due to inadvertent electrical coupling effects, we confirm that it varies quadratically with the applied heater current, as expected for a temperature gradient induced by Joule heating [26]. Additionally, reversing the polarity of the applied heater current does not affect the measured Seebeck voltage.

When measuring low voltage values, we validate that these are from the thermovoltage, and not from spurious signals. In Figure 3.6, we plot the measured voltage between the source and drain contacts (i.e. the two parallel thermometer lines) against the heater current. Because Joule heating is directly proportional to I^2R and the Seebeck voltage is directly proportional to the temperature gradient, the measured voltage should be approximately quadratic with respect to the heater current. This relationship is confirmed in Figure 3.6.

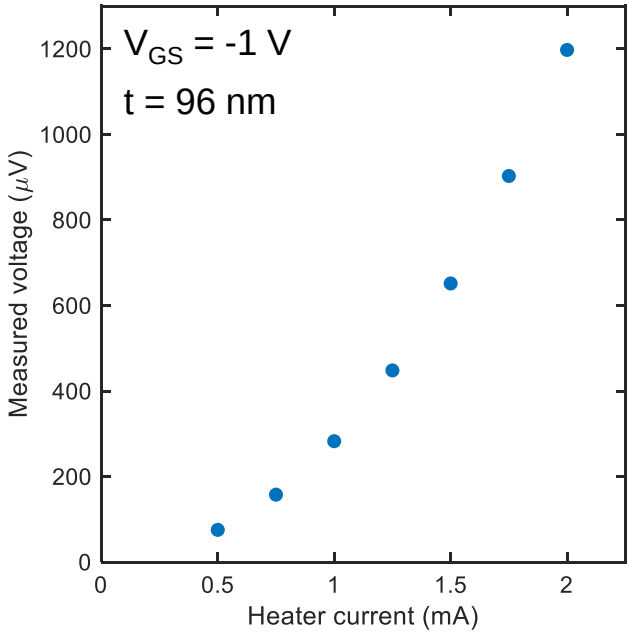

Figure 3.6: The voltage measured between the source and drain contacts of a 96 nm thick WSe_2 sample biased at a gate-source voltage $V_{GS} = -1$ V, plotted as a function of the applied heater current.

In Figure 3.7(b), we plot the measured Seebeck coefficients for both electrons ($S_n < 0$) and holes ($S_p > 0$) over the range of our gate bias voltages. As expected for a semiconductor, the absolute value of the Seebeck coefficient increases with decreasing carrier density, reaching peak values of 740 µV/K for *p*-type (in the 96 nm thick sample) and -400 µV/K for *n*-type (in the 12 nm thick sample), at room temperature. These are the highest experimentally-reported Seebeck coefficient values for thin-film WSe_2, exceeding those of bulk Bi_2Te_3, a commonly-used commercial thermoelectric material [16, 135]. Care must be taken in the Seebeck voltage measurement, as the input impedance of the measurement tool must be greater than the channel resistance for an accurate reading [26]. Therefore, no points are measured for the Seebeck coefficient when the devices are in their off-states, as indicated on Figure 3.7(b).

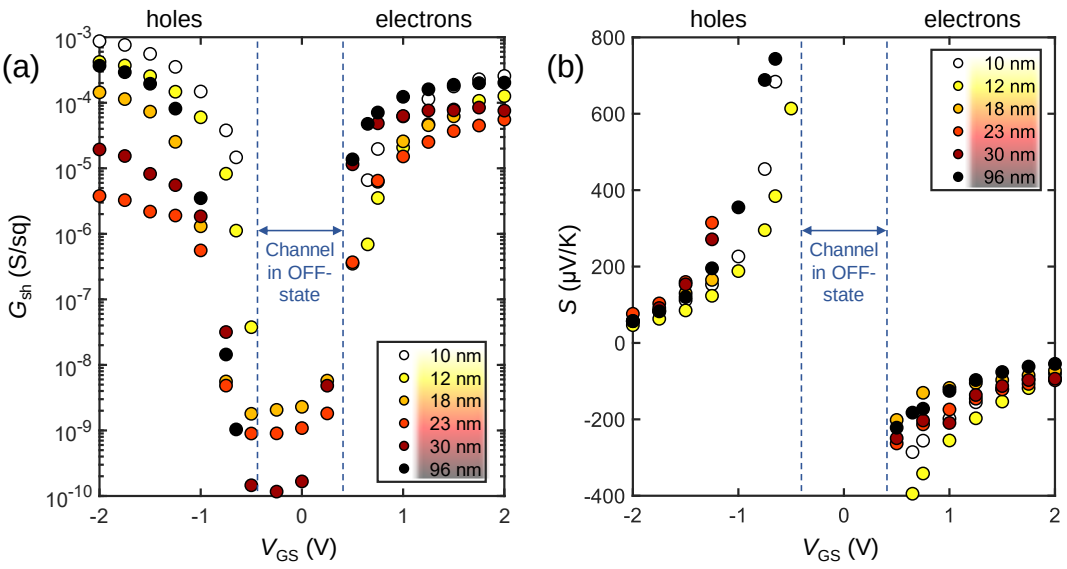

Figure 3.7: (a) Sheet conductance (G_{sh}) and (b) Seebeck coefficient (S) measured as a function of applied gate voltage (V_{GS}) for our WSe_2 samples of varying thicknesses, at room temperature. Negative and positive V_{GS} voltage ranges are for hole and electron conduction, respectively. For low $|V_{GS}|$, when the Fermi level is in the band gap, the devices are in the off-state and no values for S are measured as the channel resistance begins to exceed the input impedance of the measurement tool.

While the electrical conductivity of the WSe_2 channel increases with increasing carrier density, the magnitude of the Seebeck coefficient follows the opposite trend. Thus, in order to gain a deeper understanding of the material's overall thermoelectric performance, we consider the power factor (PF), defined as $S^2\sigma$. As the electrical conductivity increases and there are additional charge carriers in the channel (either *n*- or *p*-type), the PF will first increase to a maximum point, and then subsequently decrease as the Seebeck coefficient drops when the Fermi level is pushed deeper into the conduction or valence band.

The PF is plotted vs. electrical conductivity in Figure 4 for each sample thickness. We find a maximum PF of 830 μW m^{-1} K^{-2} for p-type conduction and 280 μW m^{-1} K^{-2} for n-type, both in the 10 nm thick WSe_2 sample. These PF estimates use the entire WSe_2 sample thickness (t_s) to calculate the electrical conductivity, $\sigma = G_{sh}/t_s$; however, the

entirety of the sample is not conducting charge equally—rather, current flow is confined to a channel within the top few layers gated under the ion gel [136, 137]. Therefore, if we considered only the thickness of the conducting channel in these calculations, the PF values would be higher, and this is also further discussed as follows.

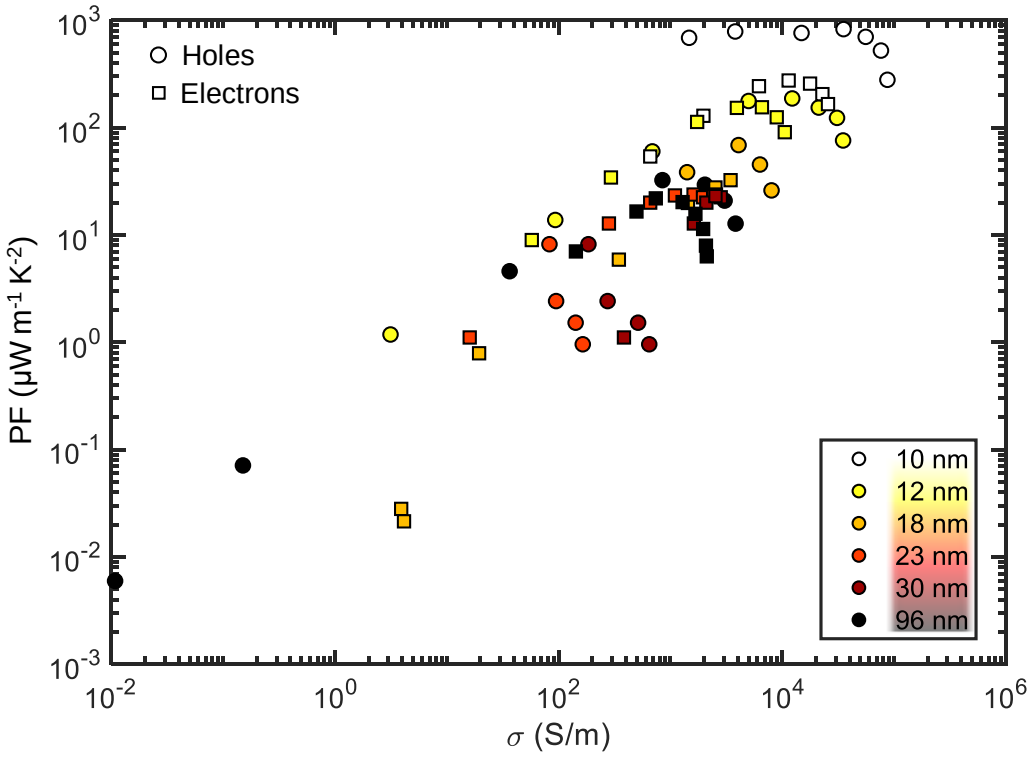

Figure 3.8: Plot of our measured power factor (PF) vs. electrical conductivity (σ) for WSe_2 samples of varying thicknesses. σ is normalized over each sample thickness. Circles represent holes and squares are for electrons. The PF ($= S^2\sigma$) for most data sets displays a clear maximum, which occurs because σ increases while S decreases at higher gate voltages and carrier densities. The high capacitance of our ion gel gating enables the sample conductivity and carrier density to be swept through this maximum point.

In a 2D, multilayered transistor, the layers contributing to conduction are a subset of the total number of layers, and the specifics depend on the channel thickness as well as the applied gate-source voltage [137]. In this analysis, we make a rough estimate that the majority of the current flows through the top two layers of the samples, and thus, we recalculate the PFs using this "effective" channel thickness (t_{eff}), where t_{eff} = 1.3 nm [46,

136]. As shown in Figure 3.9, the adjusted PF values for each device follow the same trend, increasing with electrical conductivity to a maximum and turning over as the Seebeck coefficient decreases. However, the PFs are higher when only t_{eff} is considered, peaking at ~6400 μW/m/K^2 for holes in the 10 nm sample and ~2400 μW/m/K^2 for electrons in the 96 nm sample. Comparing to the values in Table 3.2, this represents one of the highest PF values for a p-type 2D material.

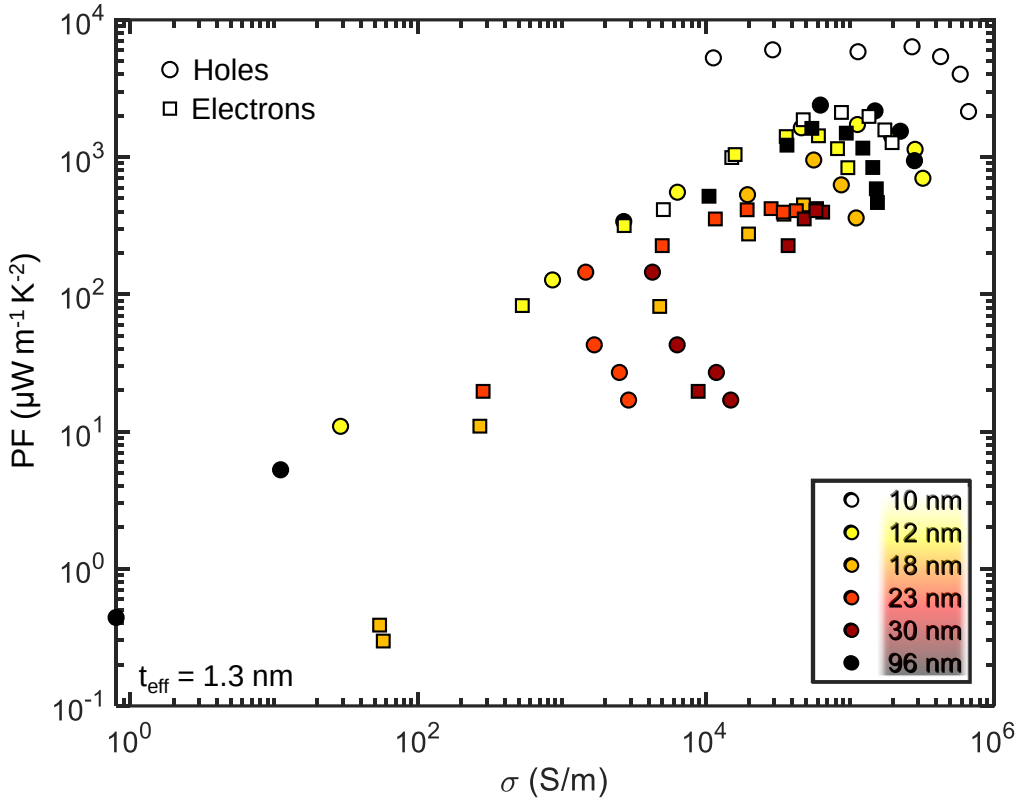

Figure 3.9: Power factor (PF) plotted against electrical conductivity (σ), where σ is calculated using an "effective" channel thickness, t_{eff} = 1.3 nm.

Additionally, we consider the effect of the WSe_2 sample thickness on the measured electrical and Seebeck data. While the variation in G_{sh} may be in part due to device-to-device variation, there is a general trend of decreasing PF with increasing thickness for a given gate voltage. The maximum PF values we measure are for the 10 nm sample, and these roughly decrease for the thicker samples. Figures 3.10(a) and (b) plot G_{sh} vs. sample thickness (t_s) for holes and electrons, respectively. As expected, higher $|V_{GS}|$ leads

to higher carrier densities and higher G_{sh}. Figures 3.10(c) and (d) display the PF vs. sample thickness for electrons and holes, respectively, where we can see that the PF roughly decreases with increasing thickness. This can be partially explained by the electrical conductivity component of the PF—since σ is normalized by thickness, the thicker samples have lower average σ if the thickness of the conducting channel is limited to the surface layers of the sample.

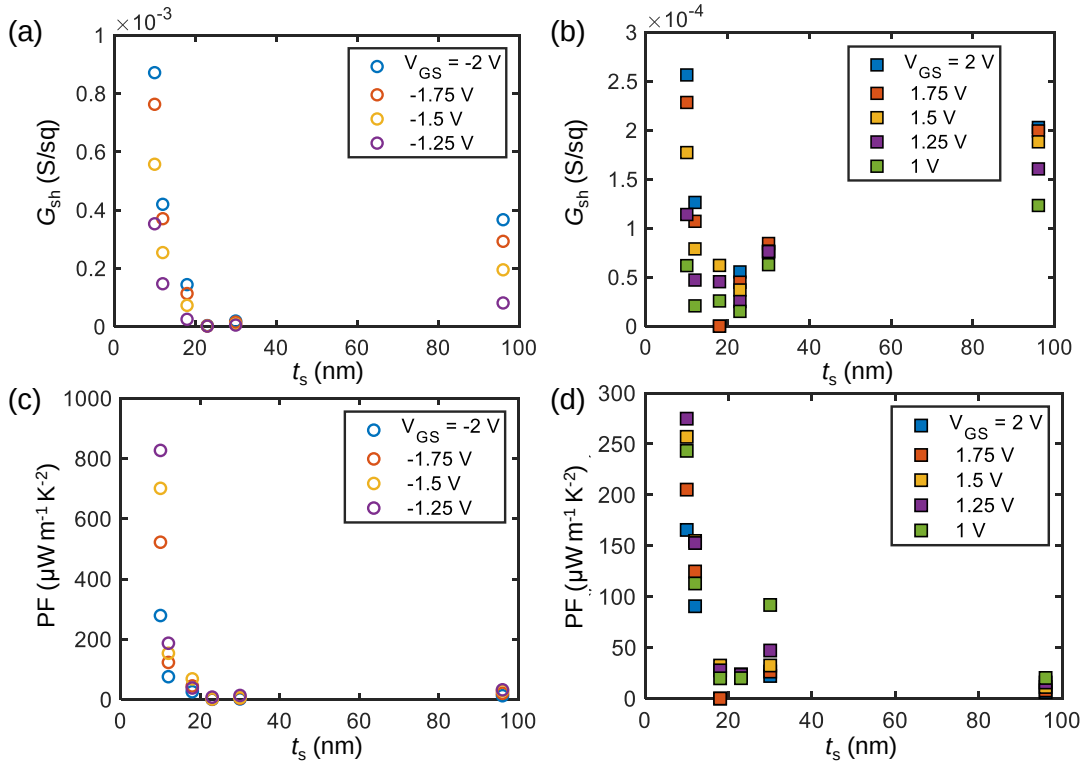

Figure 3.10: Sheet conductance (G_{sh}) vs. sample thickness (t_s) for (a) holes and (b) electrons at several V_{GS} values. Power factor (PF) vs. t_s for (c) holes and (d) electrons at several V_{GS} values, showing a general decrease of PF for increasing sample thicknesses.

While quantum confinement in low-dimensional materials has long been recognized to boost the Seebeck coefficient and power factor by introducing sharp features in the electronic density of states [17, 138, 139], the WSe_2 samples used in this work ($\geq$ 10 nm thickness) are not thin enough to benefit from confinement along the cross-plane direction. However, we note that in the on-state, at the high electric fields enabled by the

high-gate capacitance ion gel, the carriers that are responsible for conduction are in fact confined in a near-triangular field-induced potential well at the surface of WSe_2. The width of this potential well, and the thickness of the 2D electron gas formed therein, are on the order of nanometers [46, 137]. It has been experimentally shown in other materials that this field effect-induced quantum confinement can lead to an enhancement in Seebeck coefficient [140-142].

Therefore, thicker WSe_2 samples do not have inherently lower Seebeck coefficients than thinner samples in the thickness regime probed here, if they are electrostatically surface-gated to tune the carrier density. We expect that this, coupled with good material quality, is the reason that values of S we measure here are higher than those reported for monolayer or few-layer WSe_2, and that the PFs we measure are likewise competitive.

3.3.3 Temperature-Dependent Electrical and Seebeck Measurements

For the thinnest two WSe_2 samples in this work, we carry out temperature-dependent electrical and Seebeck coefficient measurements, which are summarized in Figure 3.11 below. Transfer characteristics as well as Seebeck coefficients are plotted for 296 K (both in the beginning and again after cooling back down), 350 K, and 400 K. The temperature range we measure over is restricted due to limitations of the ion gel used. At higher temperatures, the ion gel becomes more conductive and leakage currents increase [143]; in turn, any current through the ion gel causes measurements to become unreliable. These measurements confirm that the WSe_2 sample characteristics are consistent and stable between room temperature and 400 K.

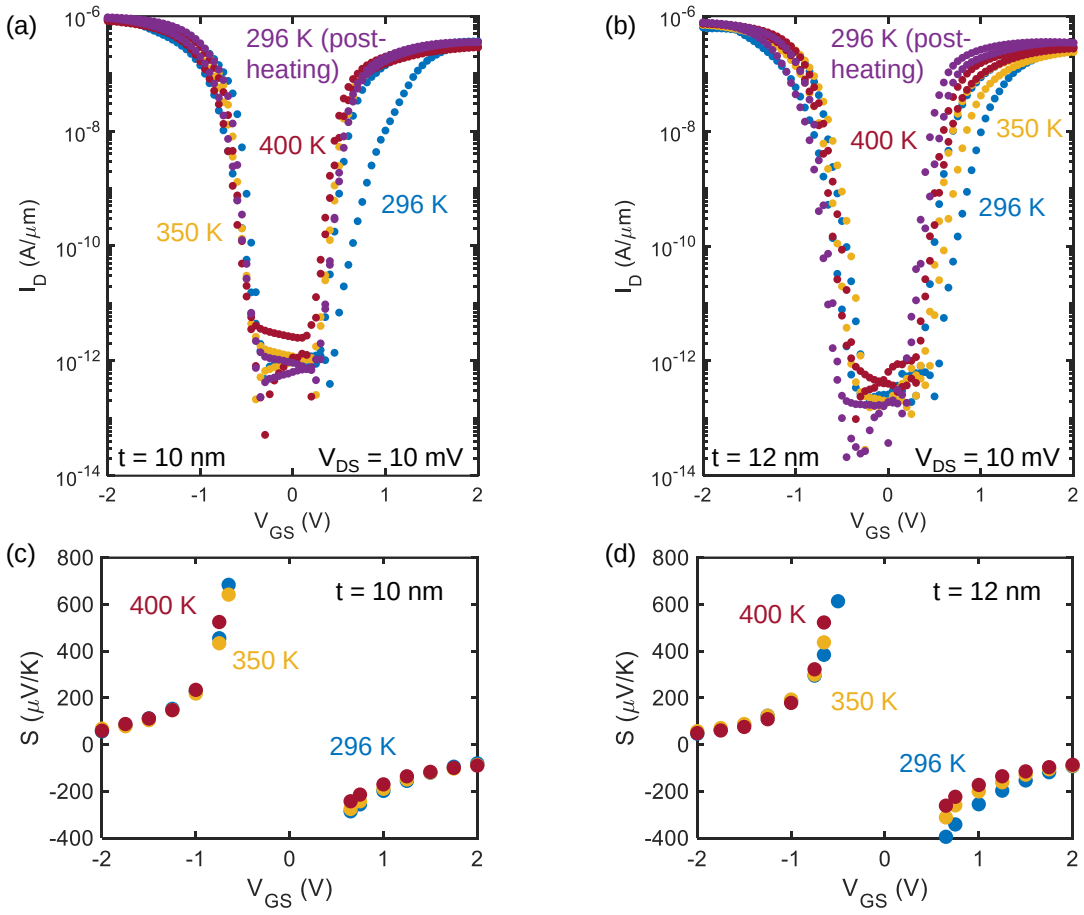

Figure 3.11: Temperature-dependent transfer characteristics for (a) 10 nm and (b) 12 nm thick WSe_2 samples, and Seebeck coefficients for the same (c) 10 nm and (d) 12 nm thick samples. The use of the ionic liquid limits our temperature range between approximately room temperature and 400 K to ensure stable measurements.

3.3.4 Comparison of Our Results with Existing Literature

The second row of Table 3.2 below contains values from our work, and subsequent rows contain a compilation of other thermoelectric studies of semiconducting 2D materials at room temperature. The maximum Seebeck coefficient and power factor (PF) values reported in these works are listed, along with the material type, thicknesses measured, and further pertinent details. In the last column, we list the method used to gate the material and modulate its carrier density.

From this table, we note that Seebeck coefficients that are orders of magnitude higher than the median reported value are at very low carrier densities, such that the power factor would likely be too low for use in efficient thermoelectric energy harvesting. Additionally, for 2D materials specifically, it is important to distinguish between the total material thickness vs. the thickness that is conducting charge—these values will differ for multilayer systems and affect the estimation of electrical conductivity. Our reported Seebeck coefficient is one of the highest obtained for a p-type 2D material, and our PF values are competitive with other works when only the thickness of the conducting channel (t_{eff}) is considered.

Table 3.2: Comparing These Results to Literature Values

Ref.	**Material**	**Thicknesses Studied**	**|S| (μV/K)**	**PF ($\mu W/m/K^2$)**	**Gating**
This work	WSe_2	10-96 nm	740 (p-type, 96 nm) 400 (n-type, 12 nm)	827 (p-type, 10 nm) 275 (n-type, 10 nm)	EMIM-TFSI
M. Kayyalha et al.[26]	MoS_2	1-23 layers	500 (n-type, 4 layers)	5000 (n-type, 2 layers)	300 nm SiO_2/Si
M. Yoshida et al.[46]	WSe_2	3 layers*	~300 (p-type, 3 layers) ~280 (n-type, 3 layers)	3200 (n-type) 3700 (p-type)	DEME-TFSI
Hippalgaonkar et al.[27]	MoS_2	1, 2, 3 layers	~520 (n-type, 2 layers)	8500 (n-type, 2 layers)	275 nm SiO_2/Si
S. Timpa et al.[122]	WSe_2	~3-4 nm (4-6 layers)	180 (n-type, 6 layers) 160 (p-type, 4 layers)	2400 (p-type, 4 layers)	40-60 nm hBN/Au/280 nm SiO_2/Si

J. Pu et al.[25]	MoS_2, WSe_2	monolayer	380 (p-WSe_2) 250 (n-WSe_2) 160 (n-MoS_2)	300 (p-WSe_2) 100 (n-WSe_2) 200 (n-MoS_2)	EMIM-TFSI
M. Buscema et al.[49]	MoS_2	monolayer	1×10^5 (n-type**)	Not reported	285 nm SiO_2/Si, laser heating
J. Wu et al.[144]	MoS_2	monolayer	3×10^4 (n-type***)	Not reported	285 nm SiO_2/Si
Y. Saito et al.[121]	BP	40 nm	510 (p-type****)	460 (p-type)	DEME-TFSI
S. Choi et al.[120]	BP	10 and 30 nm	400 (p-type)	Report "sheet" PF	300 nm SiO_2/Si
J. Fleurial et al.[135]	Bi_2Te_3	Bulk (3 mm)	250 (n-type) 230 (p-type)	Not reported	Annealed to vary carrier concentration
M. Saleemi et al.[48]	Bi_2Te_3	Bulk, nanostructured	120 (n-type)	2800 (n-type)	None

*to calculate σ, only the thickness of the conducting channel, 1.3 nm, is considered

**Seebeck value is measured for a very low carrier density

***at 280 K and at very low carrier density

****at 210 K

3.4 Summary

In conclusion, we investigated fundamental thermoelectric properties for layered WSe_2, sweeping through a range of carrier densities for both electrons and holes and measuring the highest reported Seebeck coefficients for this material. Our on-chip measurement platform demonstrates the advantages of utilizing a low thermal conductivity substrate to preserve a greater temperature difference across the WSe_2 channel, and the use of an ion gel for electrostatic gating allowed for a high degree of

control over Fermi level tuning. These initial results as well as the ability of WSe_2 to support both n- and p-type conduction make it a promising candidate for thermoelectric applications; however, future studies are still necessary to improve the scalability of the material synthesis and processing for viability in commercial applications.

Chapter 4

Electrical Transport Measurements of Transition Metal Dichalcogenide Nanoribbons

As semiconductor scaling continues, contribution from the edges of a semiconducting transition metal dichalcogenide (TMD) becomes more significant in narrower channels. Clean edges, with armchair or zigzag configurations, have been shown to have unique electronic, optical, and magnetic properties, and as the edges play a larger proportional role in narrower channels, these effects need to be considered. Prior experimental works have been done to investigate the electronic properties of narrow-channel MoS_2 devices (also referred to as "nanoribbons"). However, the majority of these works rely on some form of etching in order to fabricate the nanoribbons, and these etch processes can lead to damaged edges, with edge roughness that could negatively impact device performance. Therefore, in this work, we study nanoribbons that have been deposited through an exfoliation process, resulting in "clean" edges. By fabricating back-gated MoS_2 and WSe_2 nanoribbon devices, we investigate the contribution of edges to the electrical performance of the transistors.

4.1 Fabrication of Transition Metal Dichalcogenide Nanoribbons

The nanoribbons are deposited on an SiO_2/Si substrate through a Au-assisted exfoliation process from the surface of the bulk crystal. Because this material is exfoliated from the surface of the crystal, rather than the interior as is done with the traditional tape-exfoliation method, there is often contamination on the surface of the nanoribbon material. This surface carbide-contamination is subsequently physically removed through contact-mode atomic force microscopy (AFM) to scrape the surface of the ribbons. This technique has been demonstrated previously in the literature [145].

After depositing the nanoribbons onto 90 nm SiO_2/p++ Si substrates, we fabricate back-gated field-effect transistors (FETs) for electrical characterization. An optical image of a representative device is pictured in Figure 4.1(a), and a cross sectional schematic in Figure 4.1(b). As the exfoliated nanoribbons are often adjacent to larger areas of exfoliated material, we remove the adjacent material using a XeF_2 vapor phase etch. We use 950K A4 PMMA as an etch mask and pattern the areas to be etched using electron beam (ebeam) lithography with a JEOL JBX-6300FS system. Once the channels are defined, we use ebeam lithography again to pattern the large contact pads and leads, depositing 25 nm SiO_2/3 nm Ti/30 nm Au through ebeam evaporation and lifting off in acetone. Finally, the fine contacts are patterned and 60 nm Au is evaporated.

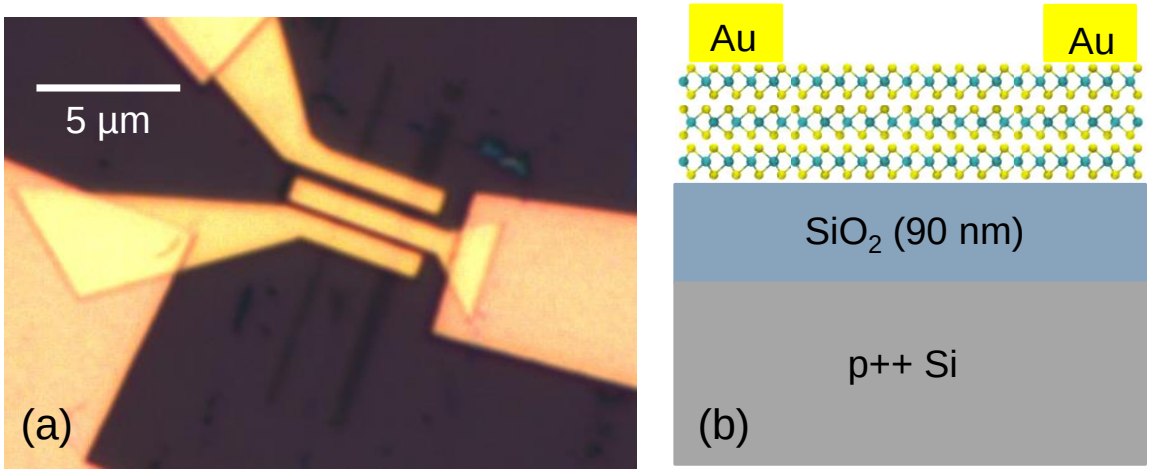

Figure 4.1: A representative MoS_2 nanoribbon back-gated FET shown in (a) an optical image and (b) a cross-sectional schematic.

Finally, because the channels of these FETs consist of multiple ribbons of material in parallel, we consider the total width ($W_{tot} = W_1 + W_2 + \cdots + W_n$) for current normalization, and the average width ($W_{avg} = W_{tot}/n$) for further analysis, where n is the number of conducting ribbons comprising the channel. These variables are also illustrated in Figure 4.2.

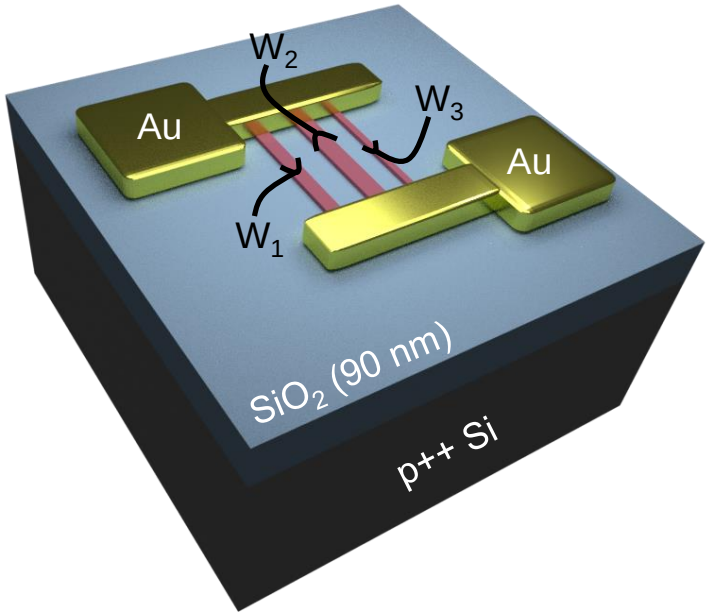

Figure 4.2: A schematic illustrating the nanoribbon device structure with parallel conducting channels between the Au source and drain contacts. The structure is back-gated through the 90 nm SiO_2/p++ Si substrate.

4.1.1 Scanning Electron Microscopy (SEM) Imaging of Devices

Scanning Electron Microscopy (SEM) images of our MoS_2 nanoribbon devices are taken after the electrical characterization is complete. These images are shown in Figure 4.3, and were acquired in an FEI Magellan 400 XHR Scanning Electron Microscope with an accelerating voltage of 1 kV. From the SEMs, we note that the edges of the MoS_2 nanoribbons appear to glow brighter than the center of the channel, which may indicate sharper features and is supportive of the hypothesis that these edges are pristine. Additionally, we note from the SEMs that there are breaks in some of the nanoribbons, and so it is important to determine the widths of the conducting channels by measuring each individually, as it cannot be assumed that each ribbon spans the full length of the device structure. The differences in widths and spacings of these nanoribbons are partially determined by the geometry of the original bulk crystal surface.

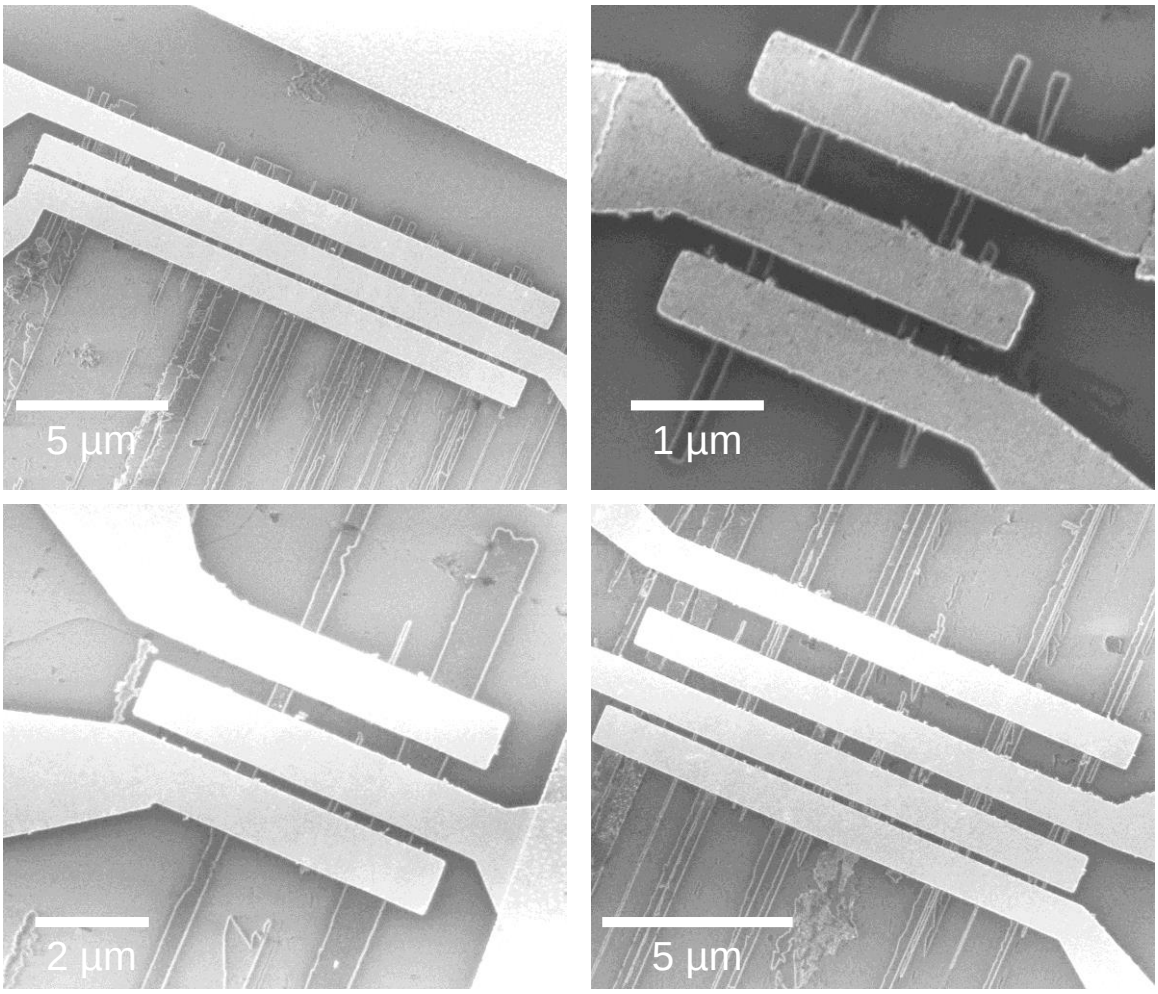

Figure 4.3: SEM images of selected MoS_2 nanoribbon FETs, picturing Au contacts on top of MoS_2 channels on a SiO_2/Si substrate. These channels vary in the number, spacing, and widths of their constituent nanoribbons.

4.2 Initial Electrical Characterization of MoS_2 Nanoribbons

These FETs are measured under vacuum (~10^{-4} Torr) in a Janis probe station with a Keithley 4200 Semiconductor Parameter Analyzer. Transfer characteristics for a number of MoS_2 FETs are plotted in Figure 4.4. These currents are normalized to the total width of the devices, and the number of nanoribbons comprising the conducting channels are also noted. Through these initial dual-sweep transfer characteristics, we observe very low hysteresis, which is a positive indication of good quality material and oxide.

Additionally, there is variable I_{max}/I_{min} behavior, and on currents reaching ~30 µA/µm for the shorter channel devices.

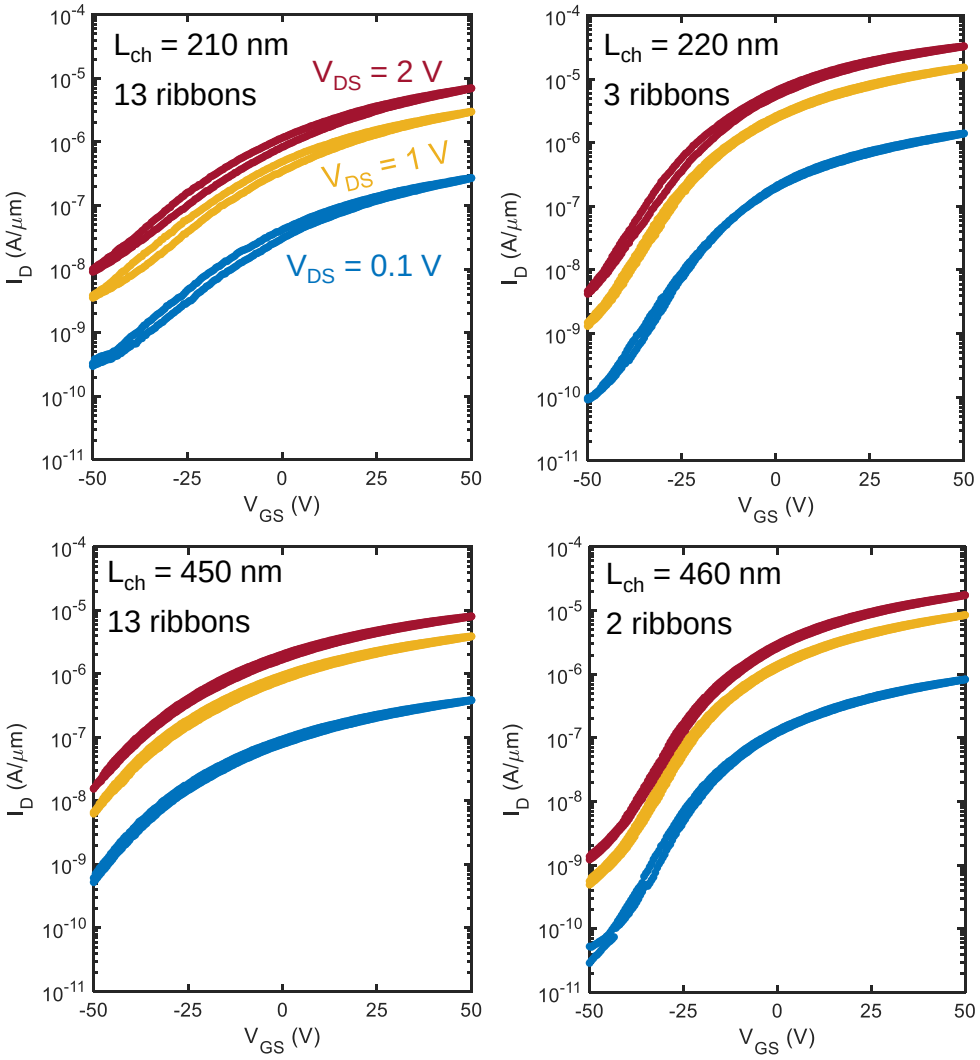

Figure 4.4: Forward and backward swept transfer characteristics for selected MoS_2 nanoribbon FETs, with channels comprised of multiple nanoribbons in parallel.

To further explore trends in the initial electrical characterization of the MoS_2 nanoribbon devices, we plot the transfer characteristics for multiple channels on the same axes, all with a drain-to-source bias (V_{DS}) of 1 V, and separated by nominal channel length. These plots are shown in Figure 4.5. From these plots, we note that the I_{min} values very roughly seem to increase for channels with narrower average ribbon widths.

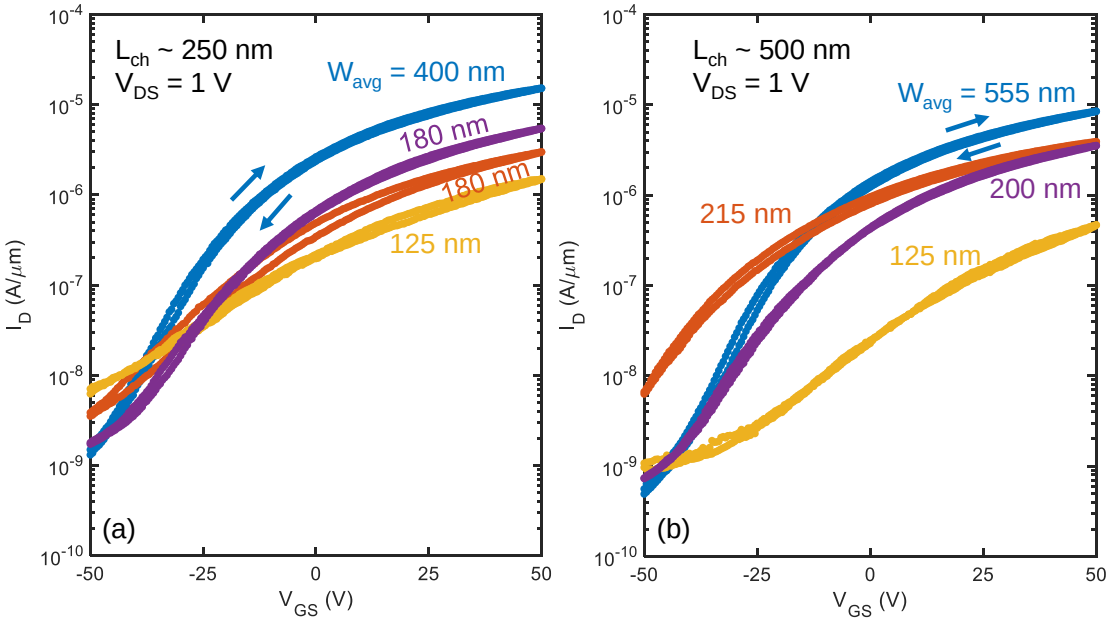

Figure 4.5: Transfer characteristics for MoS_2 nanoribbon channels with V_{DS} = 1 V for normal channel lengths of (a) 250 nm and (b) 500 nm. The average width of the ribbons comprising the conducting channels is also noted, and all curves include data from the forward and backward V_{GS} sweep directions.

To quantify the trends that may indicate increasing contribution from edges, we plot the I_{max}/I_{min} ratio vs. the average ribbon width in Figure 4.6. This plot highlights a trend of decreasing I_{max}/I_{min} ratios for MoS_2 channels with narrower average ribbon widths. While not definitively conclusive yet, this trend may be indicative of the edge contribution, if there are metallic edges from the clean exfoliation process. These edges would then not turn off in the same manner as the center of the semiconducting MoS_2 channels, which would then lead to a decrease in the I_{max}/I_{min} ratio as the ribbons become narrower. Finally, we measure a peak field effect mobility (μ_{FE}) of around 2 $cm^2V^{-1}s^{-1}$ for the channel with 400 nm average ribbon width.

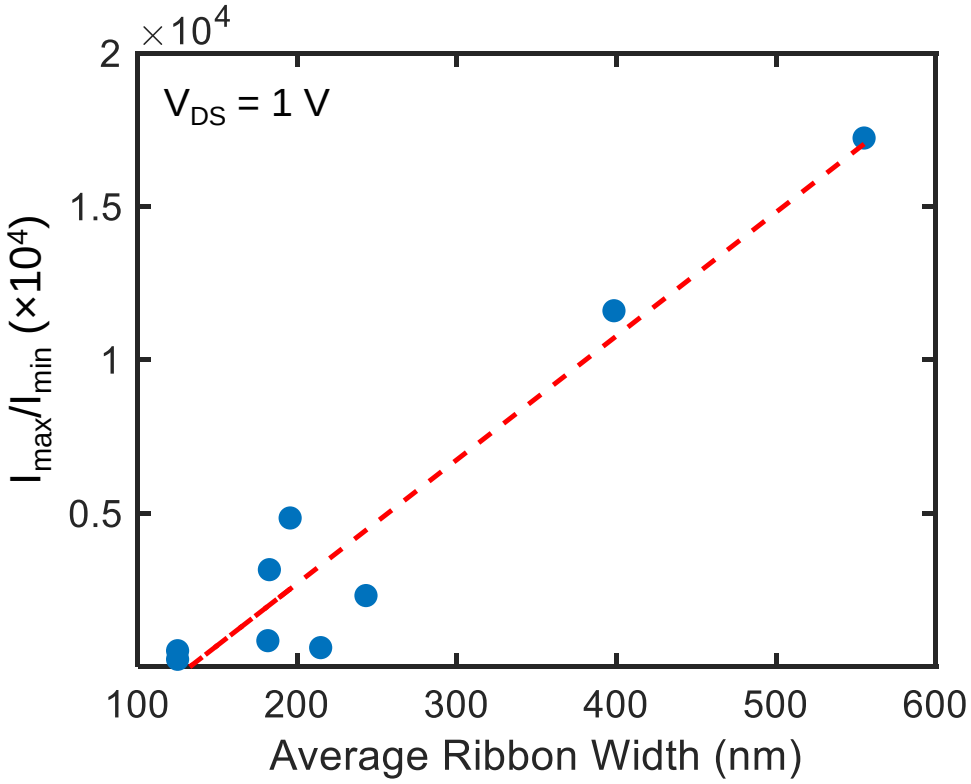

Figure 4.6: Plot of I_{max}/I_{min} ratio vs. the average ribbon width, with data points in blue and a red dashed guideline to highlight the trend. All points are for V_{DS} = 1 V for a more fair comparison.

4.3 Initial Electrical Characterization of WSe_2 Nanoribbons

In addition to the MoS_2 nanoribbons, we also fabricate and electrically characterize WSe_2 devices that were exfoliated in a similar manner from the bulk crystals. The fabrication process is similar to the previous description; however, for the WSe_2 devices, we use Pd contacts instead of Au, as Pd has been demonstrated to make good contact to WSe_2 [133]. Representative transfer characteristics for two WSe_2 channels are plotted in Figure 4.6. While these devices have a larger hysteresis than what was observed for the MoS_2 devices, they also display greater I_{max}/I_{min} ratios, and are both fairly n-type, dominated by electron conduction.

We also anneal these devices in Figure 4.7 at 523 K for 1 hour under vacuum (~10^{-4} Torr), and plot the resulting transfer characteristics in orange points. This vacuum anneal

serves to drive off surface adsorbents from the WSe_2 channels, which can then lead to improved electron currents. After the anneal, the n-type on-currents for these WSe_2 channels increase by nearly an order of magnitude, while the off-currents remain largely the same.

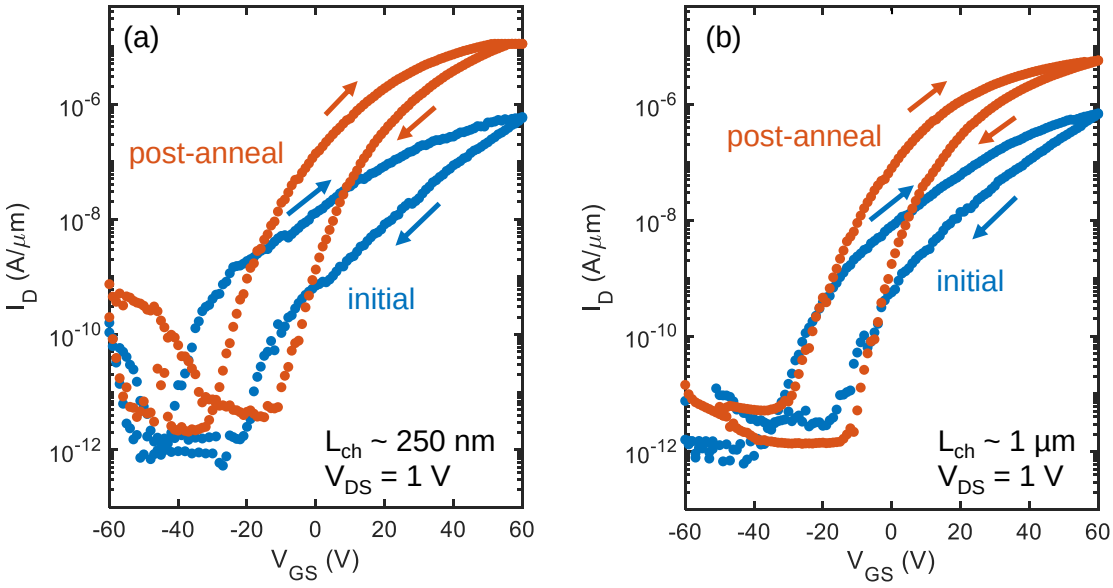

Figure 4.7: Transfer characteristics for channels comprised of multiple WSe_2 ribbons in parallel for with channel lengths of (a) 250 nm and (b) 1 μm. The devices were annealed for 1 hour at 523 K under vacuum (~10^{-4} Torr), and the annealed data is shown in orange, alongside the initial data in blue. V_{GS} sweep directions are indicated with arrows.

4.4 Next Steps

The next steps for this project involve fabricating nanoribbon FETs on individual MoS_2 and WSe_2 nanoribbons, rather than many in parallel, in order to more clearly elucidate the contribution from the edges. In the analysis of these individual nanoribbon channels, we should consider how the effect of the edges impacts the I_{max}/I_{min} ratios, as well as threshold voltages and charge carrier mobilities. Additionally, these devices should ideally consist of narrower ribbons (< 100 nm), again to exemplify the effect of the edges on the electrical performance. To explore these effects further, temperature dependent electrical measurements would also be useful in investigating the fundamental

behavior. Finally, a longer-term goal for this project is to fabricate ultra-short devices, with thinner effective oxide thicknesses and short, narrow channels. If this exfoliation process is able to preserve the edges without inducing the same type of damage and disorder than can result from etched edges, then ultra-scaled devices from the exfoliated material may be able to attain higher performances.

4.5 Summary

In summary, we have fabricated and electrically characterized exfoliated MoS_2 and WSe_2 nanoribbons. This is the first demonstration of electrical measurements of exfoliated nanoribbons, and we have reported low levels of hysteresis for parallel MoS_2 channels, and reasonable on-current levels for both MoS_2 and WSe_2 channels. These device structures and measurements provide a baseline for future additional work that will further elucidate the effects of the edges on electronic behavior.

Chapter 5

Conclusions and Future Work

This thesis has worked towards investigating various aspects of 2D materials that may impact their usage in electronic applications. By investigating CVD processes for h-BN, demonstrating direct deposition of h-BN on CNTs, and examining potential applications for thin h-BN films, we have contributed to a foundation that may be relevant for furthering the use of h-BN in electronics.

Future work along these lines may involve the development and refinement of large-area deposition of h-BN at lower temperatures, as the depositions in this work had a substrate held at > 1000°C. While this is generally acceptable when the resultant film will be transferred to the desired substrate, it would be beneficial to lower the deposition temperature and increase flexibility of deposition substrates. The high temperature is required to dehydrogenate the BN rings, and so if this energy can be provided by another source, the required thermal energy could be decreased. Additionally, another longer-term goal is to accomplish wafer-scale deposition of h-BN.

We also fabricate and measure the thermoelectric properties of a number of WSe_2 samples with varying thicknesses. The Seebeck coefficients we report for thin WSe_2 are some of the highest in literature to date, and help to illustrate the viability of WSe_2 for energy harvesting or sensing applications. Additional temperature-dependent measurements of this material over a larger temperature range would be enlightening for determining more specific applications for where the WSe_2 would operate most efficiently. Furthermore, modulating the carrier density of the channel through doping, rather than ionic liquid gating, would make the devices more robust for future applications. And finally, one ultimate goal would be to integrate WSe_2 into small scale energy harvesters, with both n- and p-type legs.

After fabricating and measuring a number of MoS_2 and WSe_2 parallel nanoribbon devices, we show preliminary evidence of edge contributions to relatively narrow back-gated device channels. While this may be indicative of edge conduction below the threshold voltage of the channel, additional measurements are still necessary to draw definitive conclusions. The next steps for this work are to fabricate devices on individual nanoribbons, ideally even narrower ones. It would also be helpful to fabricate a device exfoliated from the same bulk crystal as the nanoribbons, but with an etched channel, to have a fair comparison on how the exfoliated edges would differ from etched ones.

In conclusion, this thesis has worked to advance fundamental understanding of 2D materials synthesis and electronic as well as thermoelectric properties. Through process development, fabrication, and measurements, we have characterized various aspects of h-BN, MoS_2, and WSe_2, demonstrating their promise for future large-scale electronic applications.

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