CONTROLLING HEAT TRANSFER IN ELECTRONIC PACKAGING USING THERMAL SWITCHES AND HIGH POWER THERMAL BUFFERS

BY

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DISSERTATION

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ABSTRACT

Advances in electronic devices and vehicle electrification have resulted in increased power density (power-to-volume ratio) and specific power (power-to-mass ratio). The temporally and spatially irregular heat generation from high-power devices causes temperature spikes and gradients, leading to reduced device reliability and bulky thermal management systems. Controlling heat transfer is a key challenge of electronic packaging. Thermal devices able to actively control heat transfer in space and time are desired for advanced thermal management.

We focus on two thermal devices – a thermal switch and a thermal buffer – that can provide spatial and temporal control of heat transfer. In an analogy with electrical circuits, a thermal switch is a device to bridge or break a heat transfer pathway between a heat source and heat rejection system. A thermal buffer with a large thermal capacitance can absorb large amounts of heat and suppress temperature swings of electronics in transient operation.

This dissertation reports the development of a high contrast thermal switch and a high cooling capacity thermal buffer designed to control heat transfer in electronic packaging. The main contributions of this work are: (i) Design of a millimeter-scale liquid metal droplet thermal switch with high ON/OFF switching ratios > 70; (ii) Control of heat transfer from one or two gallium nitride (GaN) devices using the thermal switch; (iii) Integration of a solid copper (Cu) thermal switch with a 3 kW DC/AC power converter to isothermalize silicon carbide (SiC) modules; (iv) Development of a composite phase change material (PCM) thermal buffer with high cooling capacity and large energy density; and (v) Stabilization of GaN device temperatures under transient heat loads using the PCM thermal buffer heat sink.

This work investigates the fundamentals of steady and transient heat transfer in electronic packaging controlled by the thermal switch and thermal buffer, and demonstrates opportunities for applications and further research into thermal management systems of power electronics.

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CHAPTER 1: INTRODUCTION

1.1 Background on thermal management of power electronics

Thermal management techniques for electronics have been investigated for decades and are continuously evolving with increased cooling efficiency [1]–[3]. Prior publications have focused on enhancing thermal conductivity of packaging materials [4]–[6] or convective heat transfer coefficients by using one or two phase flows in jet impingement, spray cooling and mini or micro channels [7]–[11]. With recent advances in power electronics, traditional thermal management schemes are stymied by highly spatial and temporal heat dissipation of high-power semiconductors [12]–[14]. Solid-state electronics for electric power conversion enable technologies for electrification and green energy [15]–[22]. To reduce cost and achieve high performance, light and compact power electronics with wide band gap semiconductors are developed for power conversion at high power density and specific power [23]–[27]. The high power results in elevated heat generation of power electronics with device-level heat dissipation up to 500 W/cm^2 [28]. Thermomechanical stresses induced by large temperature gradients and swings reduce reliability which is one of the most important factors in power electronics packaging [29]. Advanced thermal management is required to remove high heat fluxes and reduce device temperatures and temperature swings for improved power density as well as reliability.

1.2 Motivation for spatial control of heat transfer

Thermal management of electronic devices is a challenge due to high heat fluxes but also due to generation of non-uniform heat losses. Power electronics generate different heat losses due to different work loads and operation conditions, which results in spatially distributed hotspots [30]. Figure 1.1 shows a conventional power electronics package with two power devices

generating different heat losses [31]. The non-uniform heat loads lead to formation of hot spots which require a large and bulky heat sink to reduce the local maximum temperature [32]. The temperature gradient in the packaging is elevated by the spatially distributed hotspots, which deteriorates safety risks from thermomechanical stresses [33]. To mitigate hotspots and achieve uniform temperature distributions, thermal management techniques for spatial control of heat transfer are desired in electronic packaging.

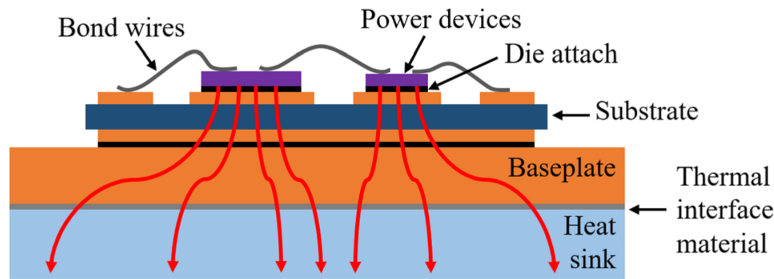

Figure 1.1 Typical scheme of power electronics packaging showing heat transfer from two power devices which dissipate different heat losses [31].

1.3 Background on spatial control of heat transfer

The non-uniform heat generation of power electronics has appealed to thermal management community for spatial control of heat transfer. Previous research demonstrated that jumping-droplet based electric-filed-enhanced condensation can be a potential method for active hot spot cooling [30]. A few publications have studied microchannel heat sinks to mitigate non-uniform heat generation in multicore processors. For example, microchannel heat sinks with different geometry of channels and headers were performed to investigate the effect on temperature distribution under non-uniform heat flux conditions [34]. A diverging channel with a trapezoidal header was helpful to enhance uniformity of temperature distribution. Nevertheless, the temperature gradient in the processor was high and changing distribution during real-time

operation of multiple cores. Although utilizing flow distribution and nanofluids in microchannel was helpful to moderate spatial temperature distribution [35], [36], active control of heat transfer was not achieved for adaptive thermal management.

A thermal switch provides spatial control of heat transfer and can mitigate hot spots of power electronics. A thermal switch controls heat transfer from the heat source to the heat sink by breaking or bridging thermal pathways in OFF or ON state. The switching ratio as the major figure of merit (FOM) is the ratio of thermal resistances in OFF and ON state (R_{OFF} / R_{ON}). The switching ratio depends on material properties, thermal switch design and geometry [37]. Figure 1.2(a) shows the concept of a MEMS thermal switch that moves a water droplet in the gap between a heat source and a heat sink via electrowetting actuation [38]. A high voltage around 100 V was applied to electrodes for droplet actuation. A switching time in tens of seconds was demonstrated. Figure 1.2 (b) shows the switching ratio as a function of the gap width at different pressures. The thermal switch had a maximum switching ratio of 14 when the pressure was reduced to 0.6 Torr. However, the switching ratio at ambient pressure was low and the micro-scale size was not suitable for power electronics with large amounts of heat generation. Challenges remain to develop and integrate a thermal switch with power electronics for spatial control of heat transfer with high switching ratio, large heat flux, quick response, and low power consumption.

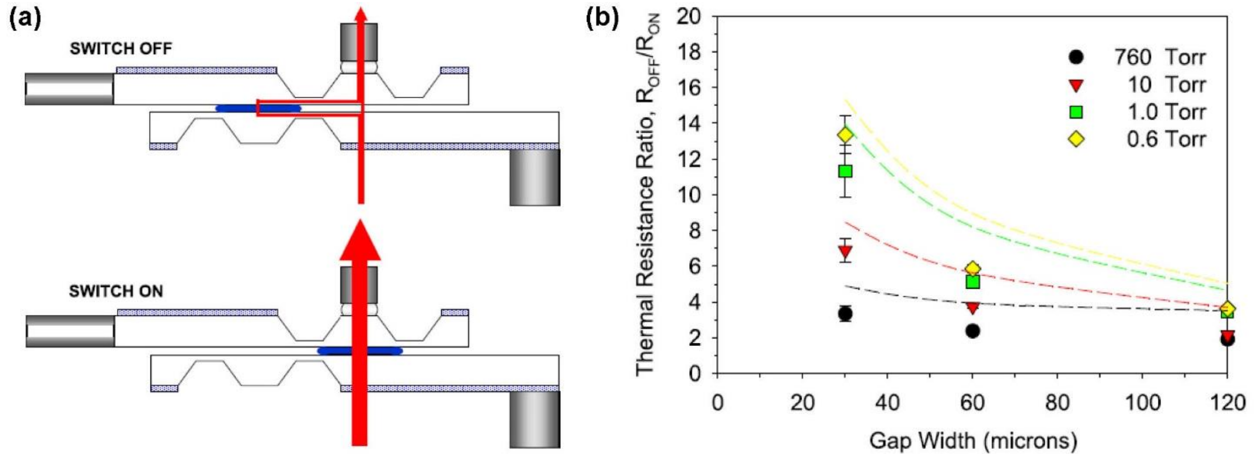

Figure 1.2 (a) Concept of a MEMS thermal switch based on electrowetting actuation of a dielectric liquid contact. (b) Thermal resistance ratio of the thermal switch as a function of gap width for gas pressures of 760, 10, 1.0 and 0.6 Torr. Measurements are indicated with symbols. Model predictions are indicated with dashed lines [38].

1.4 Motivation for temporal control of heat transfer

Thermally accelerated failures due to cyclic temperature swings account for a majority of failures of power semiconductors [39], [40]. Figure 1.3 (a) shows a power semiconductor with multilayered structures consisting of bond wire, chip, direct Cu-bonded (DCB) ceramic substrate and baseplate having different materials with different coefficients of thermal expansion (CTE) [20]. The pulsed heat losses generated from the chips propagate through these structures and cause temperature swings. The materials with different CTEs expand and compress until failure mechanisms are triggered. Three dominant failure mechanisms for semiconductor modules are bond wire liftoff, solder joints cracking under the chip and the DCB ceramics. Several models were developed to predict cycles of failure of power semiconductors as a function of junction temperature swings [41]. The simplest of the prediction models is a Coffin-Manson model $N_f = \alpha\cdot(\Delta T_j)^{-n}$, where α and n are positive constants acquired experimentally. This model indicates that a large temperature swing reduces cycles of failure and device lifetime. To enhance reliability, both temperature swing amplitude and frequency should be reduced.

Pulsed heat losses inducing cyclic temperature swings are common during operation of power electronics. Figure 1.3 (b) shows heat losses generated by Si and SiC MOSFET semiconductors of a hybrid electrical vehicle converter as a function of time during driving [42]. Although using the wide bandgap SiC semiconductor reduces the heat losses and spikes, the pulsed heat losses in a miniature device lead to severe temperature swings. In addition, thermal transients occur in power electronics from the large current inrush while starting the vehicle. The suppression of temperature overshoots is an important challenge to design electronic packaging, since most electronics have maximum operation temperatures below 150 °C. Conventional thermal management based on peak heat loads leads to overdesign of heat rejection systems. To enhance reliability as well as power density, temporal control of heat transfer to mitigate transient heat loss is desired for thermal management of high power electronics.

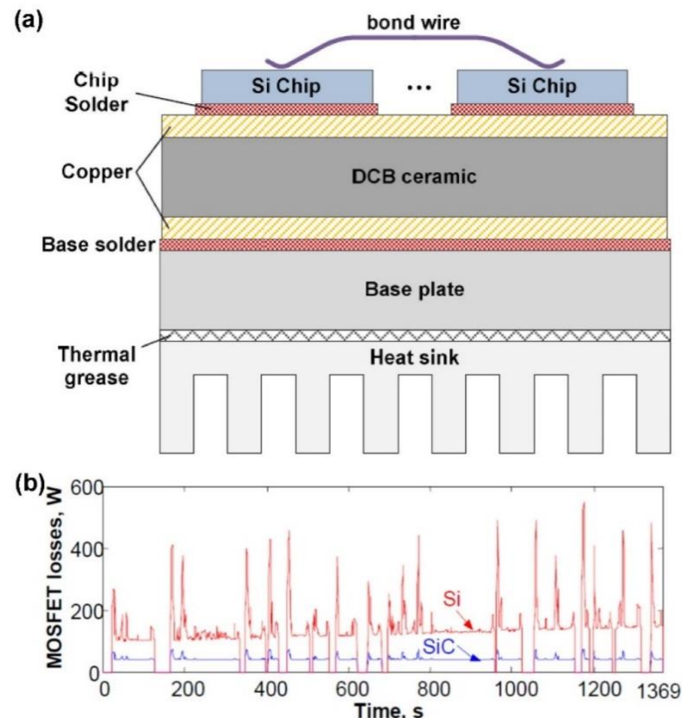

Figure 1.3 (a) Different layers of materials in a Si semiconductor module mounted on a heat sink [20]. (b) Transient heat losses of silicon (Si) and silicon carbide (SiC) MOSFET devices of a hybrid electrical vehicle converter simulated over the federal urban driving schedule (FUDS) using the department of energy's advanced vehicle simulator (ADVISOR) models [42].

1.5 Background on temporal control of heat transfer

A thermal buffer controls heat transfer by quickly absorbing a large quantity of heat. Traditionally, transient heat loads are managed by large metal heat sinks [43]. Although a metal heat sink has good thermal conductance, the relatively low thermal capacitance stymies heat absorption compared with phase change materials (PCM). Solid-liquid phase change thermal energy storage has attracted much attention for thermal buffering of transient heat loads [44], [45]. PCMs can store large amounts of heat during phase change without significant volume or temperature changes, which provides a way to suppress temperature swings and allow cooling system to be designed for the average rather than peak thermal loads [46].

A key challenge in designing a phase change material (PCM) thermal buffer is to achieve both high power density and high energy density. Cooling capacity as an important figure of merit for PCMs is calculated as $\eta = (k \cdot E)^{1/2}$ analogous to the thermal effusivity [47], [48], where k is the thermal conductivity representing the power density and E is the energy density mainly from the latent heat. By solving the Stefan problem of phase change in a semi-infinite solid, the cooling capacity determines the absorbed heat flux as a function of time shown in Fig. 1.4. Metallic PCMs have higher cooling capacities than salts and organic PCMs due to higher thermal conductivities and volumetric latent heats [49]. However, organic PCMs like paraffin waxes have advantages of light weight and tunable melting points, which promotes their commercial applications [45]. To enhance thermal conductivities, thermal conductors such as metal foams, graphene and carbon nanotubes are added to fabricate composite PCMs [50]–[52]. In addition, hybrid PCM heat sinks utilizing Cu heat sinks and organic PCMs are designed to enhance both heat absorption and conduction from transient heat sources [53]–[55].

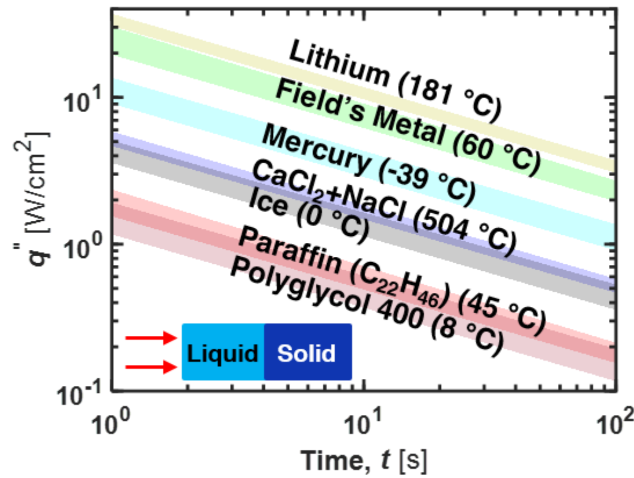

Figure 1.4 Heat flux absorbed by different phase change materials (PCM) upon melting as a function of time with the boundary superheat below 10 °C. Semi-infinite PCMs are initially solid at melting temperature given in parentheses, and an abrupt temperature increase or heat flux input is applied at the left boundary to initiate melting.

1.6 Overview of dissertation

This dissertation reports the fundamental study of a high contrast thermal switch and a high power thermal buffer and their applications to control heat transfer in electronic packaging of power devices. Following this introductory chapter, Chapter 2 describes a millimeter-scale liquid metal droplet thermal switch. The thermal switch is demonstrated to have a high switching ratio > 70. Chapter 3 investigates the active thermal management of one or two GaN power devices mounted on a circuit board using the liquid metal droplet thermal switch. Chapter 4 develops a solid copper (Cu) thermal switch to isothermalize a 3 kW DC/AC SiC power converter. Active switch motion is required for isothermalization when the converter operates at different power levels based on experiments and simulations. Chapter 5 reports a composite phase change material thermal buffer based on porous Cu metal foam and low melting-temperature Field's metal. The composite thermal buffer is demonstrated to have an enhanced cooling capacity. Chapter 6 describes the design and integration of a PCM heat sink for transient cooling of high-power GaN

devices. Finally, Chapter 7 summarizes the main results and discusses possible future researches based on this dissertation.

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CHAPTER 2: MILLIMETER-SCALE LIQUID METAL DROPLET THERMAL SWITCH

2.1 Introduction

Recent advances in electronic devices have resulted in increased power density (power-to-volume ratio) and specific power (power-to-weight ratio) of both stationary and mobile systems [1]. The trend of replacing traditionally mechanical systems with smaller electrical systems has created a demand for lighter and more compact electronic devices [1], [2]. Yet, the ability to control the flow of heat from hot spots is a key constraint for the design and operation of electrical systems, particularly at the millimeter scale [2]. For power electronics, heat generation can be temporally and spatially irregular, leading to temperature spikes and gradients that can negatively affect system performance and reliability. While passive systems that use thermal buffers based on phase change materials can partially mitigate these issues [3], technologies that enable active thermal switching would enable additional freedom in the design and operation of electro-thermal systems [4]–[6]. A thermal switch can be defined using electronic analogs [7], [8], as a thermal circuit element which controls the effective thermal conductivity between hot and cold reservoirs, and is hence capable of turning heat transfer 'ON' or 'OFF.' A thermal switch can realize active thermal management of high power electronics for temperature equalization, a key design challenge for power sharing among parallel-connected devices. Thermal switches can also enable the temperature reduction of temperature sensitive devices located in close proximity to heat sources [9]. Furthermore, a versatile and robust thermal switch would enable additional thermal circuit elements such as thermal diodes and thermal rectifiers [5]. A key measure of the thermal

switch performance is the switching ratio, defined as the ratio of effective thermal resistance of the ON to the OFF state. In previous work [10], a hydrogen gas gap-based thermal switch operating at low temperature (<170 K) achieved a thermal resistance ratio of >700. More recently, mercury and carbon nanotube (CNT) based thermal switches have been reported with thermal resistance ratios of 224 and 27.8, respectively at room temperature [11].

This paper describes a novel millimeter-scale thermal switch based on Galinstan liquid metal. Galinstan, due to its low melting temperature (-19 °C), relatively high thermal conductivity, and low toxicity, is a promising microchannel coolant [12]. In contrast to previous research focusing on actuating the thermal reservoirs [13], the present approach actuates the liquid metal droplet to connect or disconnect the reservoirs. The low friction coefficient allows the droplet to be easily actuated [14], [15], and we demonstrate hydraulic pressure, electrostatic fields, or gravitational potential as potential actuation mechanisms. Detailed modeling and experimental measurements show the thermal switching ratios of > 15 for "wet" liquid-filled channels and > 70 for "dry" vapor-filled channels.

2.2 Design and experiments

Figure 2.1 shows the liquid metal thermal switch concept. When the metal droplet bridges the two thermal conductors (Fig. 2.1a), the switch is in the ON state, resulting in heat flow from the heat source (red block) to the heat sink (blue block). When the metal droplet moves away from the bridge location (Fig. 2.1b), heat transfer is reduced due to the filling of the bridge by a liquid or vapor fluid ($k_{\text{electrolyte}}$ = 0.03 - 0.6 W/m·K), resulting in the OFF state. Galinstan liquid metal and liquid/vapor electrolyte were chosen due to the large difference between their thermal conductivities [16]. A scaling analysis of the thermal resistances reveals $R_{\text{ON}} \sim d/(k_{\text{Galinstan}} \cdot A)$ and $R_{\text{OFF}} \sim d/(k_{\text{electrolyte}} \cdot A)$, resulting in a theoretical switching ratio of $R_{\text{OFF}}/R_{\text{ON}} \approx 27$ for liquid and

≈550 for vapor. Figure 1c shows the device designed to measure this switching ratio. The device incorporates a silicone (poly dimethyl siloxane) insulator material ($k_{silicone}$ ≈ 0.15 W/m-K) and two Aluminum Nitride (Shapal Hi-M) solid block conductors (k_{shapal} = 92 W/m·K). The conductor material (Shapal) was chosen mainly due to electrochemical compatibility between the electrolyte, liquid metal, and conductor block material (see Supplementary Information, section I). Because the thermal conductivity of Shapal is much larger than that of the silicone insulator, heat flow can be modeled using a 1-D approximation (Fig. 1d) with input heat flow rate, Q_{IN}, and output heat flow rate, Q_{OUT}. The heat flows through the hot side block conductor, through the channel gap occupied with the metal droplet or the electrolyte, through the cold side block conductor, and finally out to the heat sink. The 1D model is particularly helpful for analyzing the interfacial thermal resistance (R_{INT}) and effects of natural convection on the thermal resistance of the metal droplet ($R_{DROPLET}$) and the electrolyte ($R_{ELECTROLYTE}$), in order to determine the total ON state ($R_{ON} = 2R_{INT} + R_{DROPLET}$) and OFF state thermal resistances ($R_{OFF} = 2R_{INT} + R_{ELECTROLYTE}$), and switching ratio.

Fabrication of the thermal switch device (Fig. 2.1c) began with a 10:1 mixture of Sylgard 184 silicone elastomer base and Sylgard 184 silicone elastomer curing agent that was poured into molds for the conductors and the channel. After 6 hours of curing at 100°C in air, the cured silicone pieces were bonded together with a silicone gel. After a period of 24 hours for gel solidification, the electrolyte and Galinstan were injected into the channel sequentially. To create dry channels, the electrolyte was extracted after injection, leaving vapor residue in the channel. The NaOH solution was selected in order to reduce the Galinstan oxide layer and thus reduce the droplet friction due to its high surface energy and large contact angle (see Supplementary Information, section II for additional fabrication details) [16], [17].

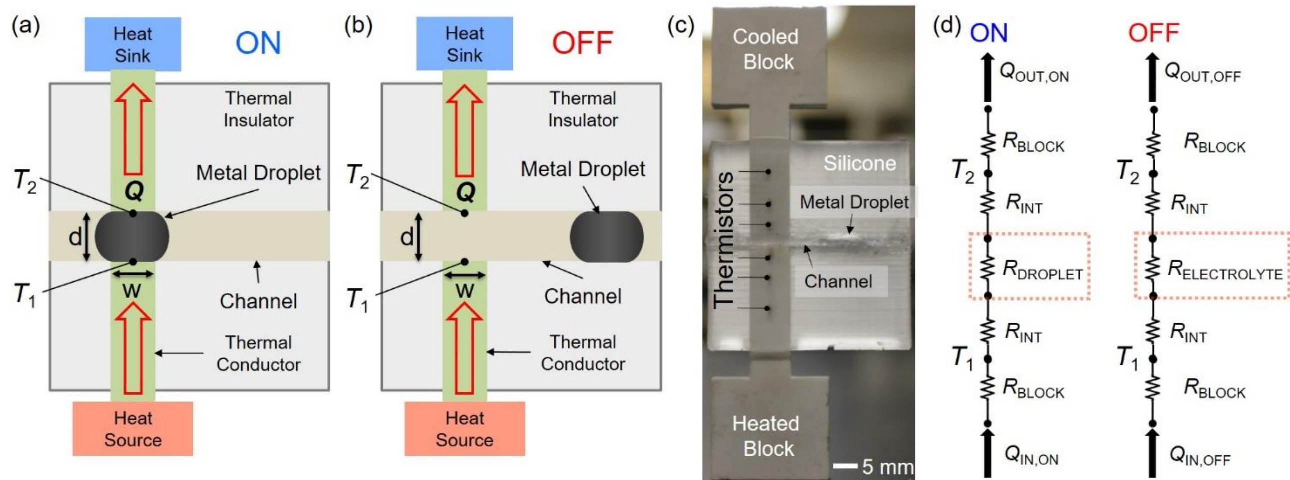

Figure 2.1 Schematic of the thermal switch showing the (a) ON-state with liquid metal droplet bridging the heat source and sink and (b) OFF-state with liquid metal removed from the channel. (c) Side view image of the fabricated thermal switch device. (d) The ON and OFF thermal resistance circuits based on a 1-D heat transfer model.

To evaluate the thermal performance of the thermal switch, three thermistors (LSMC700A010KD002, Selco Products) with an accuracy of ± 0.1°C were inserted into 600 ± 100 μm diameter micro-machined holes on each block conductor together with a thermal compound (silver paste, Arctic Silver 5) reducing contact resistances. These thermistors were connected in series to a current source meter and a DAQ (USB-1608G) acquiring voltage signals across each thermistor, which were converted to resistances and temperatures according to the Steinhart-Hart equation [18]. The heated block was attached by a thermally conductive tape and rubber bands to a copper reservoir electrically heated via two embedded cartridge heaters. The cooled block was attached similarly to a liquid cooled aluminum reservoir using a 1:1 mixture of Ethylene Glycol and DI water as the cooling fluid. The entire thermal switch device was thermally insulated by a thick layer (≈ 5 cm) of fiberglass material ($k_{\text{fiberglass}}$ = 0.04 W/m·K). Around three hours after the power supply and the chiller were turned on, the system reached dynamic

equilibrium, and the thermistor voltage signals were recorded and converted to temperatures automatically via LabVIEW.

2.3 Experimental results

Figure 2.2 shows the measured temperatures from one device using the temperature distribution assumed from the 1-D model. The device in Fig. 2.2 had a 1.96 mm thick channel, filled with 1 M/L NaOH solution. The temperature data points for each block in the ON/OFF states were Pearson correlated with coefficients of -1.000, -0.919, -0.994, and -0.995, respectively, verifying the 1D assumption. In the ON state, the average heat flow rate ($Q = (Q_{IN} + Q_{OUT})/2$) is ≈ 1.83 ± 0.04 W, with a temperature difference ($\Delta T = T_1 - T_2$) across the channel as identified by the dash lines corresponding to 6.01 ± 0.1192°C. In the OFF state, the average heat flow rate Q is ≈ 1.45 ± 0.04 W, with a larger temperature difference ΔT of 42.09 ± 0.1133 °C. Figure 2.2(b) shows the data presented in Fig. 2.2(a) with higher resolution for the temperature profile across the droplet or electrolyte solution in the channel, according to the thermal resistance model (inset). The slopes of the ON and OFF state temperature profiles indicate different effective thermal resistances. The experiment was repeatable for relatively long time scales (~1 week) for different heat flow rates and different temperature differences (see Supplementary Information, section III for a detailed summary of all measured temperatures and heat transfer rates). To investigate the effects of channel geometries and fluid medium inside the channel on the performance of thermal switches, six experiments were conducted on devices having 0.90 mm, 1.96 mm, and 2.80 mm thick channels filled with either an aqueous solution of NaOH (wet), or NaOH vapor (dry). A summary of the experimental results is shown in Table 2.1.

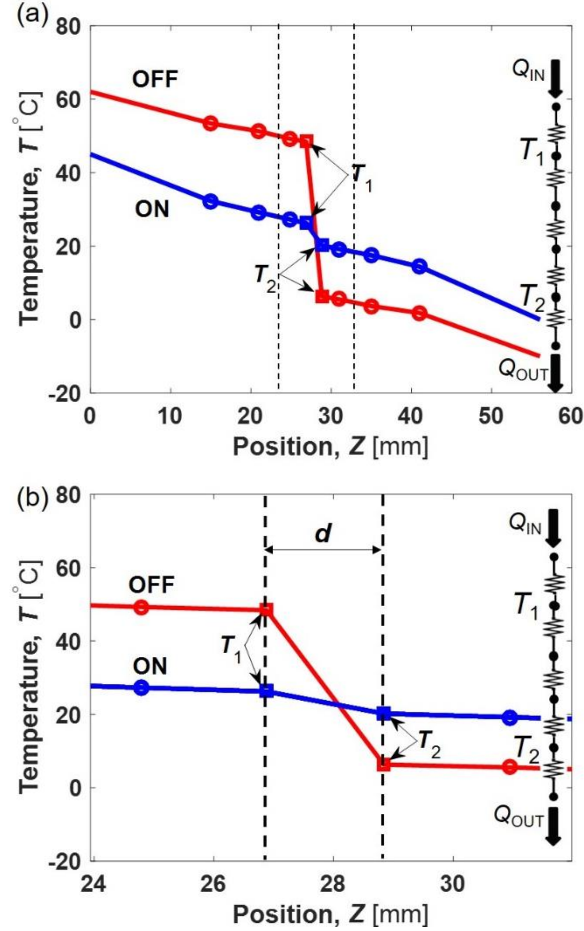

Figure 2.2 (a) Exemplary data for a 1 M/L NaOH aqueous solution filled thermal switch with a 1.96 mm thick channel in the ON/OFF states. The temperatures T_1 and T_2, and heat transfers Q_{IN} and Q_{OUT} were calculated based on the circle-marked temperatures measured by six thermistors, using the 1-D heat transfer model. (b) Temperature distributions across the channel denoted by the dashed line area in (a).

Table 2.1 Thermal resistances and switching ratios for different channel dimensions and conditions in the ON and OFF states.

Channel	Channel Condition	Channel Thickness, d [mm]	R_{ON} [K/W]	R_{OFF} [K/W]	Switching Ratio, $\psi = R_{OFF} / R_{ON}$
A	Wet	0.90	1.9 ± 0.10	29.8 ± 2.21	15.6 ± 1.4
B	Wet	1.96	3.3 ± 0.09	30.7 ± 3.48	9.4 ± 1.1
C	Wet	2.80	4.1 ± 0.13	33.3 ± 3.27	8.1 ± 0.8
A	Dry	0.90	2.2 ± 0.18	158.7 ± 11.52	71.3 ± 7.6
B	Dry	1.96	3.1 ± 0.07	167.6 ± 1.41	54.4 ± 1.3
C	Dry	2.80	4.0 ± 0.05	109.9 ± 2.99	27.4 ± 0.8

Table 2.1 shows high contrast between the effective thermal resistances of the ON/OFF states for both wet and dry channels having different channel geometries. Figure 2.3 shows the heat flow rate through the switch as a function of the temperature difference across the switch (Fig. 2.1, $\Delta T = T_1 - T_2$) for different channel geometries in both ON (blue lines) and OFF (red lines) states. The inverse slope of each line fit to the data is defined as the effective thermal resistance ($R = \Delta T/Q$). For wet channels (Fig. 2.3a), the thermal resistance increased with increasing channel thickness in both ON and OFF states. For dry channels (Fig. 2.3b), the same trend appeared in the ON state, however, the thickest dry channel in the OFF state (Fig. 2.3b, line C) had the lowest effective thermal resistance. Natural convection resulting from buoyancy effects inside the channel may account for the channel-size dependence of the OFF-state thermal resistance. Indeed, the Rayleigh number, an indicator of buoyancy-driven fluid motion in the channel, is 4217 for Wet Channel A with $\Delta T = 50°C$, and 54,952 for Wet Channel C with $\Delta T = 50°C$. The supplementary information provides additional analyses of heat transfer in the channel, including interfacial thermal resistance between the droplet and channel wall, and natural convection in the channel. Analysis of the interfacial thermal resistance at the liquid metal/Shapal interface revealed an estimated equivalent NaOH layer thickness of ≈ 11 µm.

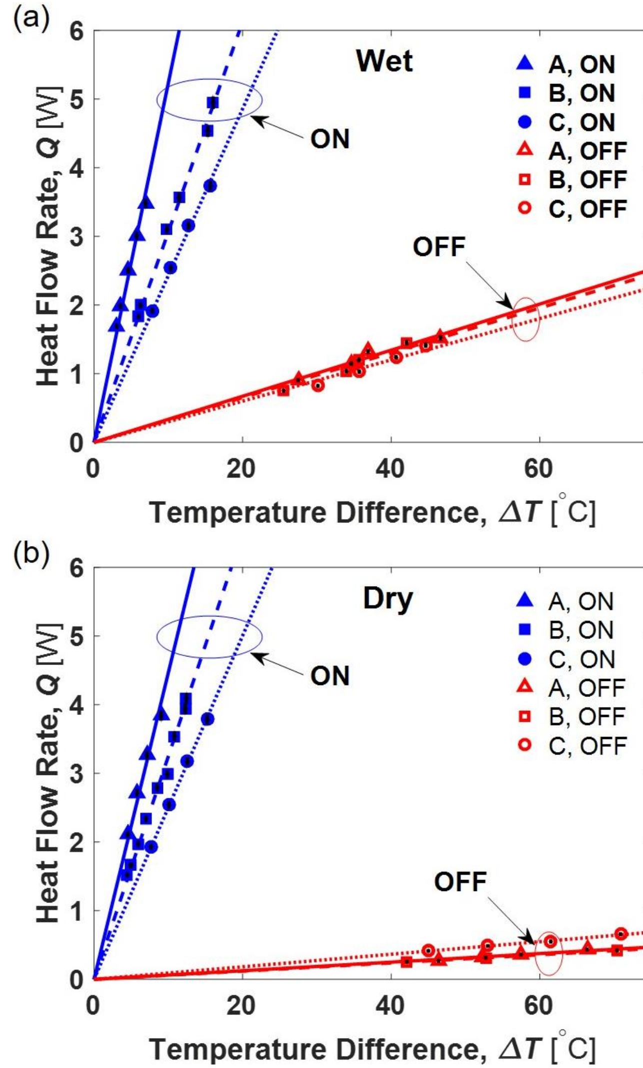

Figure 2.3 Heat flow rate vs temperature difference for (a) wet and (b) dry channels with variable thickness d (d_A = 0.90 mm, d_B = 1.96 mm, and d_C = 2.80 mm), in thermal switches having 5 mm wide and 20 mm long channels. "Wet" denotes channels filled with a 1 M/L NaOH aqueous solution and a liquid metal droplet, while "dry" denotes channels filled with a NaOH vapor and a liquid metal droplet.

In order to quantify the thermal switch performance and to gain an understanding of the underlying physics governing thermal switch design and optimization, we analyzed the switching ratio:

$$\psi = \frac{R_{\mathrm{OFF}}}{R_{\mathrm{ON}}} = \frac{\left(\frac{\Delta T}{Q}\right)_{\mathrm{OFF}}}{\left(\frac{\Delta T}{Q}\right)_{\mathrm{ON}}}, \tag{2.1}$$

where R_{OFF} and R_{ON} are the thermal switch effective thermal resistances, and ΔT and Q are the temperature difference and heat flow rate. Figure 2.4 shows the measured switching ratios as a function of channel thickness for all channels tested. Error bars were calculated using the propagation of error technique based on measurement errors and slope deviations from Figs. 2.2 and 2.3 (see Supplementary Information, section V). Thermal switches with dry channels had much higher switching ratios than those with wet channels due to the lower thermal conductivity of NaOH vapor (0.03 W/m·K) when compared to 1 M/L NaOH aqueous solution (0.6 W/m·K). For both dry and wet channels, the switching ratio decreased with increasing channel thickness, owing to the contributions of interfacial thermal resistance and natural convection inside the channels. For wet channels, the maximum measured switching ratio was 15.6 ± 1.4 at a corresponding heat flux of ≈9 ± 0.1 W/cm^2 in the ON state when the heat source was ≈50 ± 0.1 °C. For dry channels, the maximum measured switching ratio was 71.3 ± 7.6 at a corresponding heat flux of 10 ± 0.1 W/cm^2 in the ON state when the heat source was 55 ± 0.1 °C. The results demonstrate the capability of liquid metal droplet thermal switches to actively manipulate heat transfer with relatively high heat flow rates at low temperatures (< 100°C).

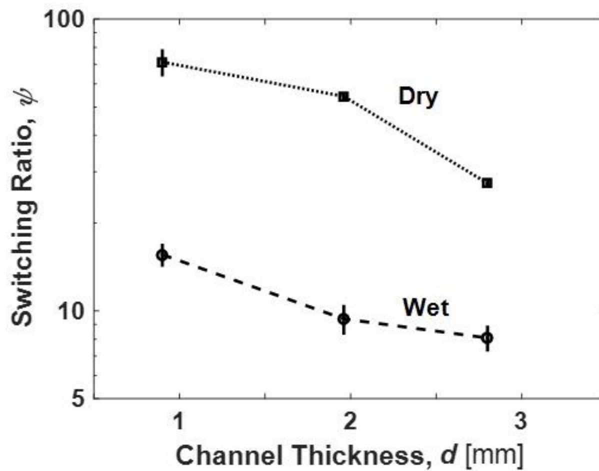

Figure 2.4 Switching ratio (ψ) as a function of channel thickness for dry and wet channels. Dry and thin channels show superior performance with switching ratios > 70. See Table 1 for specific values of switching ratios.

2.4 Discussion and conclusions

Liquid metal droplet actuation is an important aspect of integrating of our thermal switch with millimeter scale electronics. In the present study, actuation of the 8 mm long Galinstan slug in a 5 mm wide and 2 mm thick closed PDMS channel filled with 1 M/L NaOH aqueous solution was attained with 1 V/cm electric fields supplied with tungsten electrodes inserted at the axial channel ends. Using electrostatic actuation, switching speeds of ~5 sec were achieved, with negligible generation of bubbles at the tungsten electrodes. To avoid bubble formation at higher electric fields, hydraulic actuation of the droplet slug was also implemented (see Supplementary Information, section VI). Furthermore, dry channel thermal switches were actuatable with gravity simply by tilting the channel at a small angle (≈5°). The relative ease and versatility of actuation stems from the presence of the thin (≈10 μm) lubricating wetting layer of NaOH solution between the metal slug and the channel wall, which acts to minimize friction. Although demonstrated here with electrical, hydraulic, and gravitational actuation forces, future work should further investigate the underlying physics governing liquid metal slug motion in an attempt to identify the limiting actuation frequencies and required power. The timescale to move the droplet is comparable to the other thermal time constants in the system. For the three channels tested, the thermal time constants of the liquid metal droplet, liquid-filled channel, and vapor-filled channel were 0.13 – 0.88 s, 4.5 – 15.6 s, and 6.0 – 14.0 ms, respectively. The supplementary information contains additional analyses of the system time constants.

Compared with previous thermal switch devices [10], [11], our work differs by utilizing the contact material (liquid metal droplet) as the actuation object to bridge or break the heat flow path between hot and cold reservoirs flexibly. While the measured switching ratios are large, there is

still room for improvement via the tailoring of the interfacial thermal resistances in the ON state and suppressing natural convection in the OFF state. To further increase the performance, careful selection of working materials such as higher conductivity liquid metals and concurrent lower thermal conductivity lubricating fluids, must be undertaken with a key focus on compatibility due to robustness considerations for thermal switches in real life application. Our devices survived ≈100 hours in steady experimental testing conditions. Long term device failure occurred due to evaporation of the NaOH electrolyte. In the future, packaging of the thermal switch should be explored to prevent evaporation or leakage. Furthermore, we suspect that the chemical stability of the liquid metal droplet in the channel may also affect long term operation.

In summary, this work demonstrates a novel millimeter scale thermal switch based on the motion of a liquid metal droplet in a fluid filled channel. Thermal resistances and switching ratios for various fabricated thermal switch devices having both wet and dry solutions and differing thicknesses were measured and analyzed. Experimental results show that switching ratios as high as 15.6 for wet channels and 71.3 for dry channels are possible, promising for applications in thermal management systems. As an important component in thermal circuit system design, the thermal switch developed here may unlock new approaches for thermal management and circuit topologies. When integrated with power electronics, a cooling system, and perhaps a thermal buffer element such as a phase change material, the thermal switch could allow active management of heat flows and isothermalization of electronics, leading to improvements in performance or systems reliability. The thermal switch also has the potential for use in, and enhancement of, energy storage and energy conversion systems, such as thermal batteries or solar thermal systems [19]. This work provides a framework for the development of millimeter-scale thermal switches capable of spatial and temporal thermal dissipation control.

2.5 References

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CHAPTER 3: AN INTEGRATED LIQUID METAL THERMAL SWITCH FOR ACTIVE THERMAL MANAGEMENT OF ELECTRONICS

3.1 Introduction

Power electronics having increased volumetric and gravimetric power density are required for multiple applications such as mobile systems in all-electric or plug-in hybrid electric vehicles [1]–[3]. In these applications, electrical systems are replacing mechanical systems with an increasing demand for more compact power electronic devices which can meet the electrical request while reducing integration penalty [4]–[6]. The utilization of wide bandgap semiconductor materials such as silicon carbide (SiC) and gallium nitride (GaN) with higher carrier mobility and maximum junction temperature capability are key enablers for realizing dense electronics packaging and increasing the power processing capability [7]–[9]. However, the high level of integration with passive components and compact layout to reduce the volume and weight of the system creates electro-thermal obstacles for realizing the full potential of wide bandgap devices [10]. The induced electro-thermal-mechanical considerations as well as stresses can be a limiting factor in the design and reliability of electrical systems [11]. Electronic devices operating with variable losses can generate spatially and temporally varying hot spots, which cannot be mitigated with traditional thermal management approaches [12].

Thermal management devices with excellent cooling performance, such as spray cooling, jet impingement, two phase cooling, cold plates, or phase change materials, can remove the heat from hot spots efficiently [11], [13]–[15]. Yet, these conventional methods can be stymied by the

temperature variation between multiple electronic devices on the same module. Previous research has shown that over-temperature and thermal-cycling induced failures are the most common failure modes for power electronic modules (PEM) [16]–[18]. The thermomechanical stresses in the PEM damage the interfaces and connections between semiconductor components, which reduces reliability due to thermomechanical failures [16]. Active thermal management methods are required to mitigate such fatigue-based failures and improve reliability by limiting thermomechanical stresses.

The thermal switch is a desired component for active thermal management of power systems [19]. A liquid metal thermal switch can control the effective thermal conductivity and turn the heat transfer "ON" or "OFF" by moving the liquid metal droplet in a channel. Electronic applications utilizing pulsed power, having non-uniform heat dissipation, or temporally varying temperature distributions, would all benefit from the implementation of thermal switches due to the capability of controlling heat transfer and temperature distributions temporally and spatially [20]–[22]. Furthermore, thermal switches have potential to control heat transfer and reduce spatial temperature inhomogeneity, a pervasive problem in electronics leading to reliability issues. However, integration and characterization with active electronic devices is required in order to evaluate the efficacy of the thermal switch in more representative PEM conditions.

This work develops the liquid metal thermal switch technology through integration and heat transfer characterization with GaN electronic devices. We fabricated and integrated the thermal switch with a single GaN device, and characterized the wet and dry thermal switch heat transfer performance. Furthermore, we integrated the thermal switch with two GaN devices and studied the ability to use the switch to achieve device-to-device isothermalization by moving the liquid metal droplet to different locations at different power levels along a wet channel. We showed that

the thermal switch can enable GaN device isothermalization for a variety of power dissipations, resulting in lower thermomechanical stresses and higher long term reliability. The successful demonstration of our thermal switch provides an approach to achieve temperature distribution homogenization in PEMs, with application to both low and high power electronics.

3.2 Thermal switch design and fabrication

Figure 3.1(a) shows a schematic of the thermal switch concept [19], while Figure 3.1(b) shows a thermal switch integrated with a single GaN device mounted on a PCB. When the thermal switch is in the ON mode, the liquid metal droplet ($k_{\text{Galinstan}} \approx 16.5$ W/m·K) enables efficient heat transfer from the GaN device (heat source) to the coolant (heat sink) at the front. In the OFF mode, the liquid metal droplet is moved away, breaking the efficient heat transfer to the coolant. The channel is filled with a low thermal conductivity electrolyte solution ($k_{\text{electrolyte}} \approx 0.6$ W/m·K) or electrolyte vapor ($k_{\text{vapor}} \approx 0.03$ W/m·K). We refer to the electrolyte-filled channel as wet and the vapor-filled channel as dry. To ensure 1-D operation, the sides of the thermal switch device are thermally insulated by a low thermal conductivity silicone ($k_{\text{silicone}} = 0.15$ W/m·K). To better understand the heat flows during operation and to guide our prototype design, we developed a corresponding 1-D thermal resistance circuit shown in Fig. 3.1(c). The heat dissipation Q from the GaN device transfers to the front side coolant (Q_{front}) and to the back side ambient air (Q_{back}).

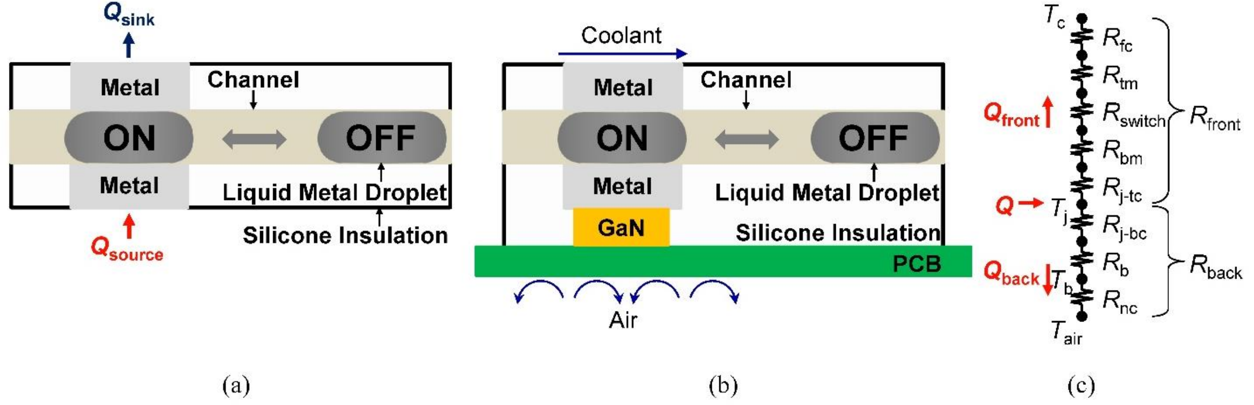


Figure 3.1 Schematic of the thermal switch integrated with a gallium nitride (GaN) electronic device. (a) The liquid metal droplet can move from left (ON) to right (OFF) in the channel. (b) Heat from the GaN device (Q) is removed from the top via forced convection (Q_{front}) to cooling water and from the bottom via natural convection (Q_{back}) to ambient air (23 ± 1ºC). (c) Schematic of the 1-D thermal resistance circuit for a single GaN device with integrated thermal switch. See Table 1 for characteristic values in the resistance network. Gravity points from top side to the bottom side.

Table 3.1 summarizes the thermal circuit parameters. Based on the 1-D heat transfer model, maximizing the heat transferred to the front side (Q_{front}) yields better thermal switch performance in terms of switching ratio. Reducing the impact of the metal conductor thermal resistances, R_{tm} and R_{bm}, was important for minimizing the front side thermal resistance $R_{\text{front}} = R_{\text{fc}} + R_{\text{tm}} + R_{\text{switch}} + R_{\text{bm}} + R_{\text{j-tc}}$. Two metal conductors were designed accordingly to be thin and broad to reduce thermal resistance. The thermal resistance circuit allowed us to calculate critical parameters and heat flows from measured values (Q, T_{c}, T_{j}, T_{b}, and T_{air}). Based on the junction temperature T_{j} and a back-calibration experiment (Section 3.3), the back side heat transfer Q_{back} and thermal resistance R_{back} were determined. The PCB spreading thermal resistance R_{b} and the natural convection thermal resistance R_{nc} were calculated by $R_{\text{b}} = (T_{\text{j}} - T_{\text{b}}) / Q_{\text{back}}$ and $R_{\text{nc}} = R_{\text{back}} - R_{\text{b}}$. The front side heat transfer rate Q_{front} and thermal resistance R_{front} were calculated by $Q_{\text{front}} = Q - Q_{\text{back}}$ and $R_{\text{front}} = (T_{\text{j}} - T_{\text{c}}) / Q_{\text{front}}$. With R_{tm}, R_{bm}, and $R_{\text{j-tc}}$ as known constants, the switch thermal resistance R_{switch} and the forced convection thermal resistance R_{fc} were calculated based on our previous works [19],

[23]. The total thermal resistance $R_{total} = R_{front} \parallel R_{back}$ was calculated by $(T_j - T_{air}) / Q = (T_j - T_c) / Q$, since the coolant temperature T_c was set to 24 ± 1°C, which was equivalent with the ambient air temperature T_{air}. Using the 1-D heat transfer analysis (Table 3.1), we designed the thermal switch to effectively transfer heat away from the GaN device in the ON mode, and to prevent heat transfer from the GaN device in the OFF mode.

Table 3.1 Experimental and calculated parameters used in the thermal resistance circuit

Parameter	Definition	Wet ON	Wet OFF	Dry ON	Dry OFF
Q [W]	Device power	1.72	2.01	1.73	1.87
R_{fc} [K/W]	Forced convection thermal resistance	18.2±2.0	18.2±2.0	18.2±2.0	18.2±2.0
R_{tm} [K/W]	Top metal conductor thermal resistance	0.2			
R_{switch} [K/W]	Switch thermal resistance	1.7±0.08	42.9±3.11	1.8±0.14	121.5±12.64
R_{bm} [K/W]	Bottom metal conductor thermal resistance	0.9			
$R_{j\text{-}tc}$ [K/W]	Junction to top case thermal resistance	0.45			
$R_{j\text{-}bc}$ [K/W]	Junction to bottom case thermal resistance	3.9			
R_b [K/W]	Printed circuit board (PCB) thermal resistance	5.6±4.9	7.5±2.3	4.0±4.9	7.9±1.8
R_{nc} [K/W]	Natural convection thermal resistance	42.0±6.9	40.9±3.1	43.6±7.0	40.4±2.5
R_{front} [K/W]	Sum of front side thermal resistances	21.4±2.0	62.7±3.7	21.5±2.0	141.2±12.8
R_{back} [K/W]	Sum of back side thermal resistances	51.4±6.1	52.3±2.8	51.4±6.1	52.2±2.3
R_{total} [K/W]	Total thermal resistance $R_{front} \parallel R_{back}$	15.1±1.3	28.5±1.1	15.2±1.3	38.1±1.2
T_c [°C]	Coolant temperature	24.0±1.5			
T_j [°C]	Junction temperature	50.1±1.6	81.4±1.6	50.2±1.6	95.4±1.6
T_b [°C]	Maximum temperature on PCB backside	45.3±2.0	68.9±2.0	46.2±2.0	79.3±2.0
T_{air} [°C]	Air temperature	24.0±1.5			

Figure 3.2 outlines the fabrication process. First, the top layer was prepared by casting silicone liquid (Sylgard 184) into a mold containing the 1 mm thick top metal (Shapal) (Figs 3.2a and 3.2b). The bottom layer was prepared in a similar manner, starting with the PCB and bottom metal (Shapal) (Figs. 3.2c and 3.2d). After solidification, the glass layer was removed, and the parts were bonded together as shown in Fig. 2(e). NaOH aqueous solution (1M/L) and the liquid metal droplet (Galinstan) were injected into the channel using separate syringes as shown in Fig. 3.2(f). The NaOH aqueous electrolyte was selected to reduce the oxide layer around the liquid metal droplet [19]. To create a dry channel, the aqueous solution was subsequently removed using a clean syringe.

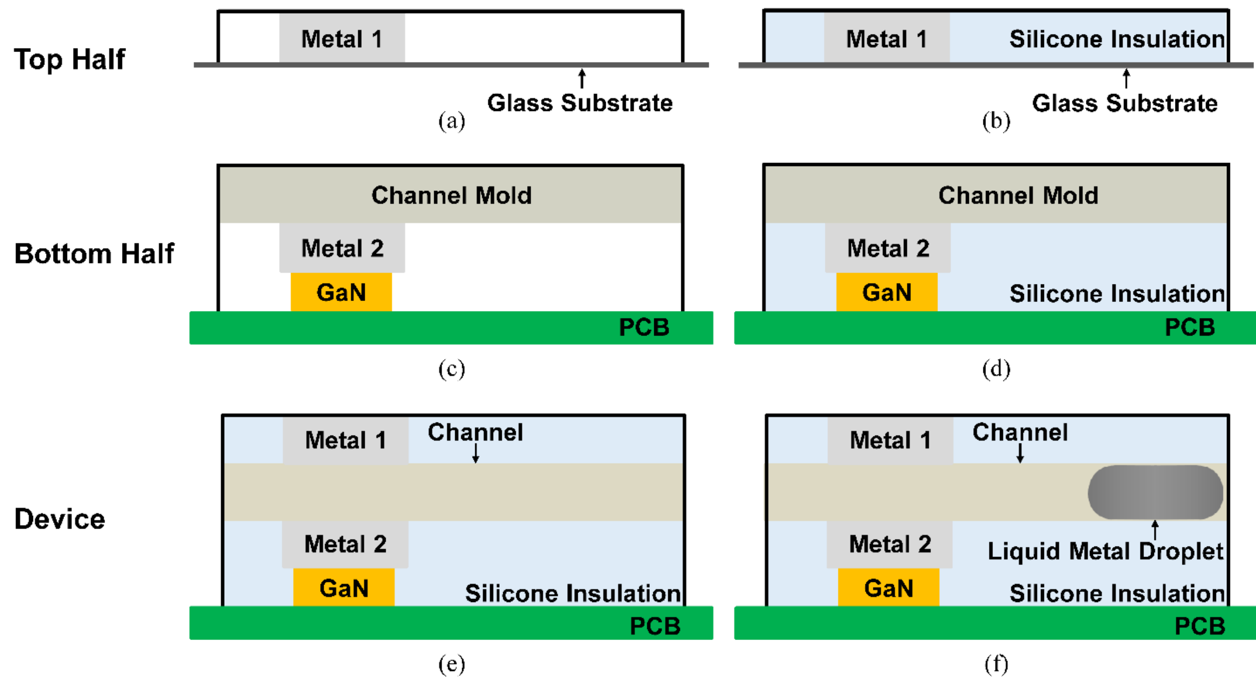


Figure 3.2 Fabrication process for the thermal switch and its integration with the PCB. (a) and (b) The top half was fabricated by casting silicone around the top metal electrode. (b) and (c) The bottom half was fabricated by casting silicone around the bottom electrode and PCB. (e) and (f) The pieces are assembled and the metal droplet is inserted into the channel.

3.3 Single device measurements

Figure 3.3 shows a schematic of the experimental setup. The PCB with dimensions of 40 mm x 40mm x 1.6 mm has two top-cooled EPC 2034 GaN devices each with dimensions of 2.6 mm x 4.6mm x 0.7 mm soldered onto the board, as shown in Fig. 3.3(a). Figure 3.3(b) shows the integrated thermal switch consisting of a channel having dimensions of 1 mm x 5 mm x 30 mm, a liquid metal droplet having a length of 10 ± 0.5 mm, and two metal conductors (Shapal Hi-M) having dimensions of 1 mm x 5 mm x 10 mm. The 1 mm thick metal elements were selected to avoid corrosion and ensure low junction-to-coolant thermal resistance by using a material with thermal conductivity of 92 W/(m·K) [19]. The test device in Fig. 3.3(c) was fixed to an acrylic fixture, with both sides exposed to ambient air (24 ± 1℃). The front side (thermal switch side) of the device was cooled convectively by water at room temperature (24 ± 1°C), which was pumped by a chiller (9712A11C, Polyscience) at a flow rate and Reynolds number of 3.8 LPM and 7000. The back side (PCB side) was spray painted black (1678830, Rust-Oleum) to ensure a high emissivity and exposed to ambient air. An infrared camera (A655sc, FLIR) captured thermal images of the painted PCB surface to acquire the back side temperature profile. A voltage source (E3620A, Agilent) provided a 5V gate voltage to the GaN device. A power supply (6033A, Agilent) was biased as a current source to provide a constant drain current depending on the power dissipation requirements for the device. Measuring the on-state resistance for each device was shown through calibration to be a straightforward way to determine the junction temperature for the GaN transistors. A current meter (34410A, Agilent) was utilized to measure the drain current and a voltage meter (34410A, Agilent) was attached via Kelvin connections to the GaN device to measure the drain-to-source voltage signal. The on-state electrical resistance for the GaN device was acquired by Ohm’s law.

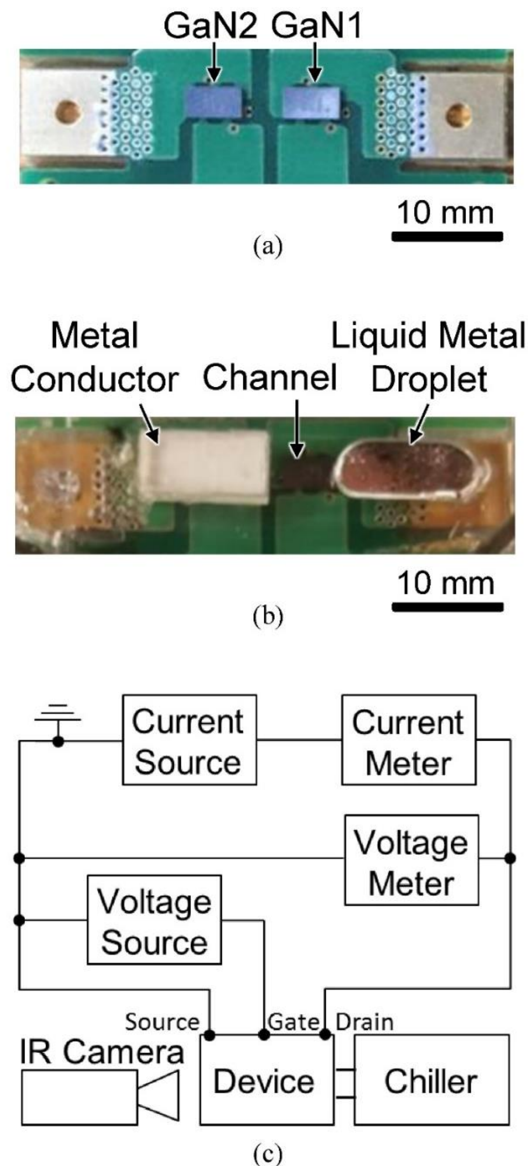


Figure 3.3 Magnified top view photograph of the (a) PCB showing two GaN devices side by side and (b) integrated thermal switch device. The color change from (a) to (b) was due to light interaction with the silicone insulation covering the entire PCB top side. (c) Schematic of the experimental setup used to characterize the thermal performance of the device connected to the chiller via a customized manifold.

Prior to testing the thermal switch, benchmarking experiments with no switch were conducted to characterize the performance of the GaN devices and provide better estimates for the 1-D thermal resistance model (Table 3.1). The reference tests utilized identical mounting points and orientations as the integrated switch experiments (Fig. 3.1). A power of 140 mW was applied

to the left side GaN device (GaN2) with 0 W applied to the right device (GaN1). After the system reached the thermal steady state (≈ 30 minutes), an infrared (IR) image of the PCB back side surface was taken. To overcome the difficulty in predicting two-dimensional heat transfer effects using the 1- D resistance model, a computational finite element analysis simulation was developed in Comsol Multiphysics. Figure 3.4 shows the experimental and simulated temperature distributions on the PCB back side. The simulation geometry included the GaN devices, the multi-layer PCB, and cabling connected to the electronics. The GaN2 device shown in Fig. 3.3(a) dissipated heat, creating a hot spot on the opposite side of the PCB, as shown in Fig. 3.4. The GaN heat dissipation was set to be the input parameter and varied in the simulations. The boundary condition for the model was set to be natural convection with ambient temperature of 25°C quiescent fluid (air). The excellent agreement between experiment and simulation demonstrated that the simulation was successful at predicting the heat spreading effects inside the PCB and could be used to determine key resistances in the 1-D thermal network.

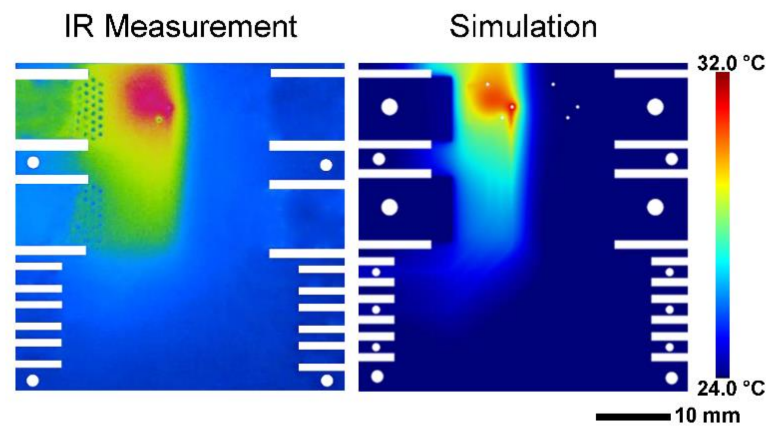


Figure 3.4 Steady state infrared image (left) and finite element analysis thermal simulation (right) of the PCB back side (side exposed to ambient air). The left side GaN2 device is powered at 140 mW while the right side GaN1 device is off. The maximum temperature was 31°C for both simulation and experiment. Gravity is pointing in the downward direction. For actual experiments, gravity points out of the page (towards the back side, Fig. 3.1). The temperature error was ±2.0°C stemming from the calibrated IR thermal measurement.

In order to determine the back side thermal resistance R_{back}, we performed a calibration experiment by sandwiching two identical PCBs symmetrically front to front, thereby eliminating front side heat transfer (adiabatic front side). In the calibration case, the back side heat transfer rate Q_{back} equals the device power Q due to symmetry. The symmetric GaN devices were powered at levels ranging from 60 mW to 810 mW. For each power, the drain to source voltage and current values were recorded after the system reached steady state, from which the junction temperature T_j was acquired afterwards. The drain-to-source electrical resistance of the GaN device increases with increasing junction temperature, with a unique correlation for each GaN device due to variability in the mounting during fabrication. The GaN junction temperature as a function of electrical resistance was calibrated with a temperature interval of 5°C. The back side thermal resistance was calculated as $R_{back} = (T_j - T_{air}) / Q$, which was the sum of the junction-to-bottom-case thermal resistance $R_{j\text{-}bc}$, the PCB thermal resistance R_b, and the natural convection thermal resistance R_{nc}. Figure 3.5 shows that the back side resistance decreases with increasing device power due to more efficient heat spreading into the PCB at higher powers. The calculated value for R_{back} (Table 3.1) was used hereafter to evaluate parameters in the thermal resistance circuit (Fig. 3.1c).

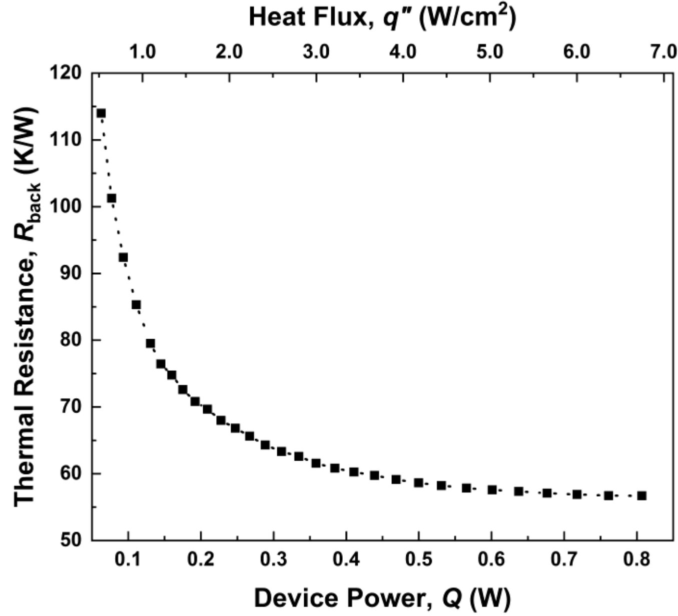


Figure 3.5 Measured back side thermal resistance ($R_{back} = R_{j\text{-}bc} + R_b + R_{nc}$) as a function of the total device power Q and device heat flux q". The heat flux was defined as $q" = Q / A$, where A is the GaN device face area having dimensions of 2.6 mm × 4.6 mm. The dotted line represents the trend line of back side thermal resistance.

3.4 Single device results and discussion

To test the efficacy of the thermal switch, we integrated a dry switch with the aforementioned GaN PCB design. Figure 3.6 shows thermal IR images of the PCB back side after integration of the PCB with the thermal switch. The left side device was powered with 750 mW while the right side device was unpowered (0 W). Figure 3.6(a) shows the significant presence of heat spreading into the PCB layer and to the surroundings when the thermal switch was in the OFF mode. The maximum temperature was located close to the GaN2 device, from which the heat propagated into the PCB along the copper traces within the PCB. Figure 3.6(b) shows the zoomed-in images of the dotted area in Fig. 3.6(a) when the thermal switch is in the OFF and ON modes. The PCB temperature in the OFF mode exceeded that in the ON mode by 13ºC due to the thermal switch breaking or bridging the heat transfer pathway to the front side coolant. The IR images provided

good qualitative and quantitative measures of the integrated thermal switch capacity to manipulate the heat transfer pathways from the GaN devices.

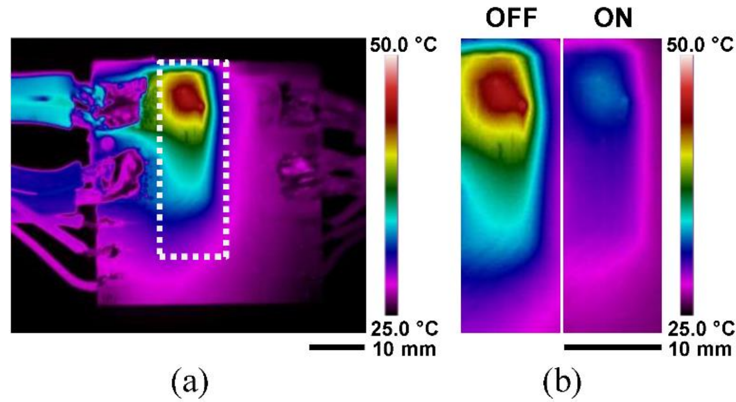
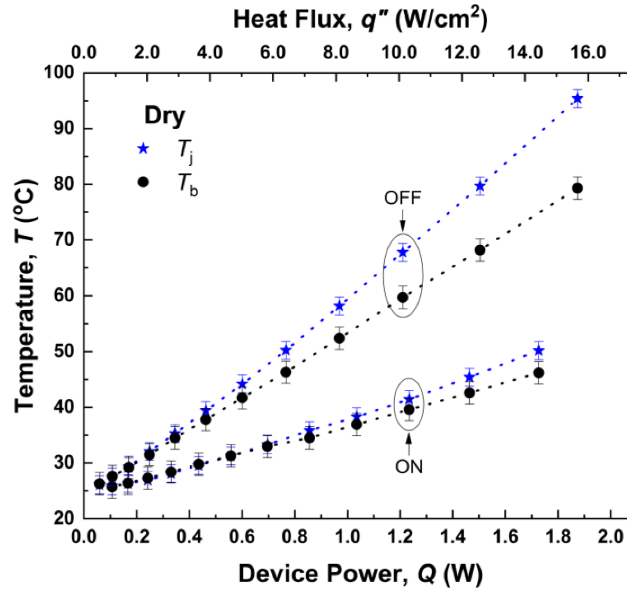


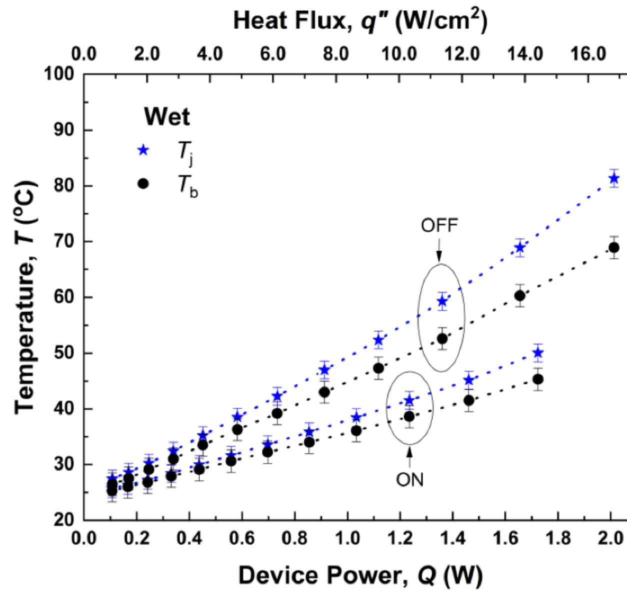
Figure 3.6 (a) Infrared image of the integrated device (PCB back side). (b) Zoomed-in images of the dotted area in (a) when the thermal switch was in the OFF (left) and ON (right) modes. The left side device (GaN2) was powered with 750 mW and the right side device (GaN1) was unpowered. The PCB temperature T_b error was ±2.0°C stemming from the calibrated IR thermal measurement.

To quantify the thermal switch performance and ability to control heat flow, we characterized the GaN device junction temperature for the ON and OFF modes at variable GaN power dissipation levels. Figure 3.7 shows the measured junction temperature of the GaN device integrated with a wet or dry thermal switch as a function of power dissipation. The junction temperature always exceeded the PCB temperature due to its closer proximity to the heat generating region. The ON mode junction and PCB temperatures were always lower than the OFF mode due to the better heat dissipation through the thermal switch and lower front side thermal resistance. In the OFF mode, the dry channel junction and PCB temperatures exceeded those of the wet channel due to the higher thermal resistance of the vapor-filled dry channel, resulting in worse heat dissipation to the front side when compared to the back side. Using the temperature and power measurements presented

in Fig. 3.6, we were able to analyze the thermal resistances of the integrated thermal switch and quantify the integrated device performance.



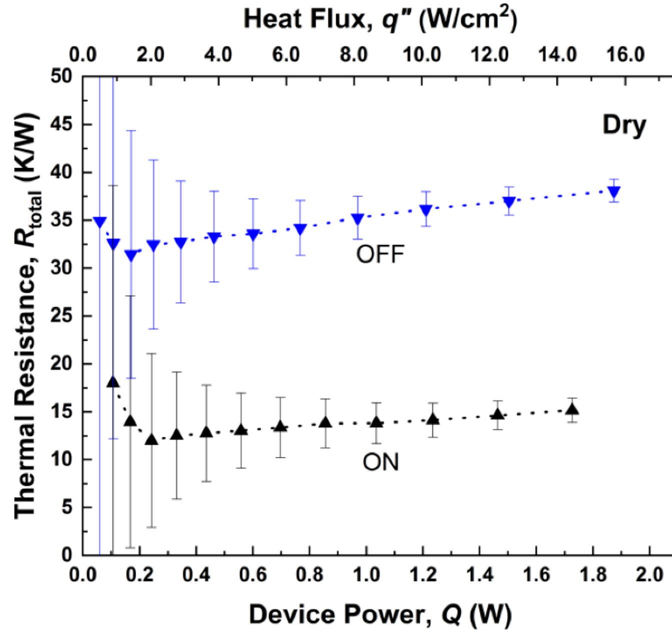
(a)



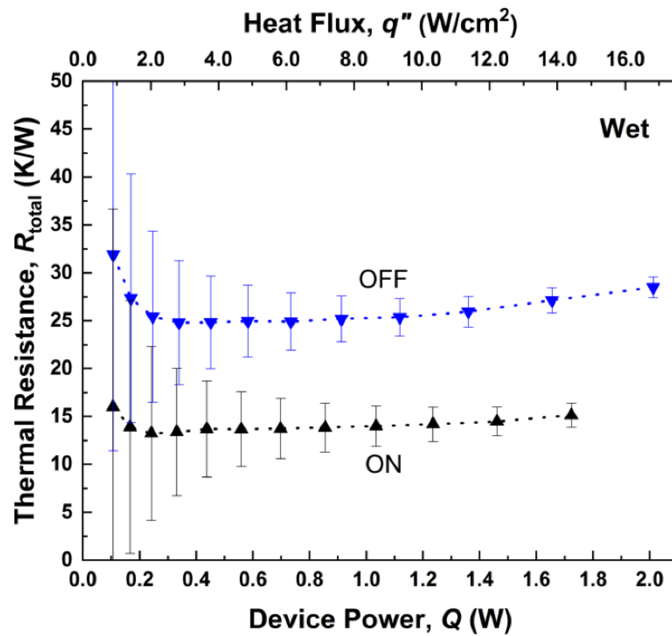
(b)

Figure 3.7 Device junction temperature (T_j , blue star symbols) and PCB temperature (T_b, black circle symbols) as a function of device power dissipation (Q) and heat flux (q”), for a (a) dry and (b) wet thermal switch in OFF and ON modes. Dotted lines represent trend lines for the junction and PCB temperatures. The junction temperature error of ±1.6°C was estimated from error propagation of the K-type thermocouple (±1.5°C) and the electrical resistance calibration curve regression for the GaN junction temperature (±0.6°C). The PCB temperature T_b error was ±2.0°C stemming from the calibrated IR thermal measurement.

Figure 3.8 shows the total thermal resistances obtained from combining the experimental results with our 1-D heat transfer model. The total thermal resistance was defined as $R_{total} = R_{front} \| R_{back} = (T_j - T_{air}) / Q = (T_j - T_c) / Q$. For the integrated dry channel thermal switch device, the total thermal resistance was 35 K/W in the OFF mode and 15 K/W in the ON mode. For the integrated wet channel thermal switch device, the total thermal resistance was 27 K/W in the OFF mode and 15 K/W in the ON mode. As expected, the OFF mode thermal resistances were always higher than the ON mode due to the lower thermal conductivity of the electrolyte or vapor compared with the Galinstan droplet. The dry channel OFF mode total thermal resistance was higher than the wet channel OFF mode total thermal resistance due to the lower thermal conductivity of the vapor compared with the electrolyte. The ON mode total thermal resistances were similar for both dry and wet channels due to the identical arrangement of the Galinstan droplet, which enables a low thermal resistance pathway to the front side for heat dissipation to the coolant in both cases. The total thermal resistances varied moderately with the device power due to heat spreading, especially when the thermal switch was in the OFF mode.



(a)

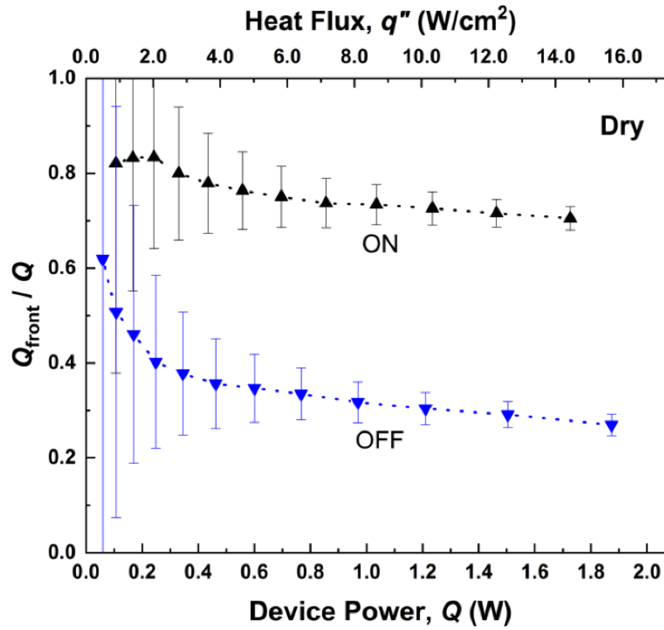


(b)

Figure 3.8 Total thermal resistance (R_{total}) of the integrated thermal switch as a function of Q and q" for a (a) dry or (b) wet channel. Dotted lines represent trend lines of the total thermal resistance. The errors were estimated by a propagation method from the junction temperature error (±1.6°C) and the ambient air or coolant temperature error (±1.5°C).

To better understand the heat flow pathways, we analyzed the heat transfer rate through the front side of the thermal switch (Q_{front}). Figure 3.9 shows the ratio of the heat transfer rate through

the front side to the total heat dissipation rate (Q_{front} / Q) as a function of device power Q and heat flux q" for dry and wet switches. In the OFF mode, the dry channel had a higher thermal resistance than the wet channel, resulting in a lower Q_{front} / Q. Both dry and wet channels effectively prevented heat transfer to the front side (≈30% for the dry channel and ≈50% for the wet channel). In the ON mode, the dry and wet channel front side thermal transport was governed by conduction through the Galinstan droplet, which had negligible thermal resistance compared to back side thermal conduction, resulting in similar Q_{front} / Q for both dry and wet configurations. The liquid metal droplet in the channel transfers > 70% of generated heat to the front side. Figure 3.9 shows that the front side heat transfer ratio decreased with increased device power due to elevated heat spreading and heat loss through the back side of the PCB. The front side heat transfer analysis demonstrates the ability of the thermal switch to manipulate thermal transport from the GaN device.



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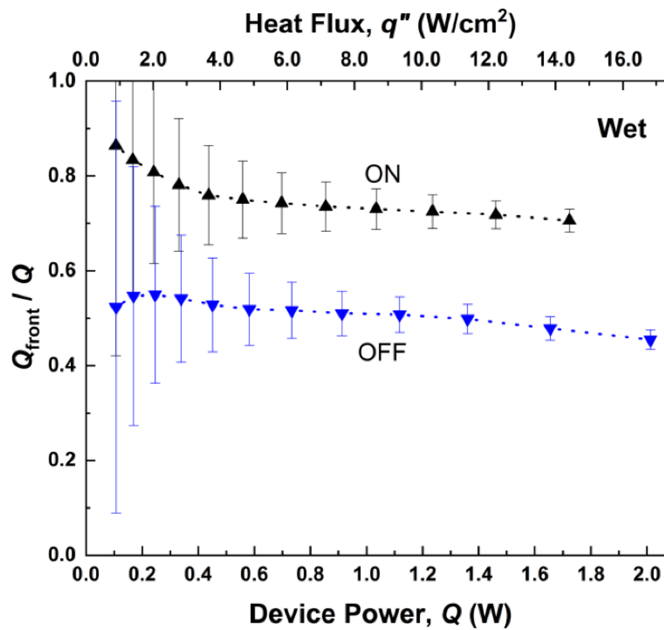
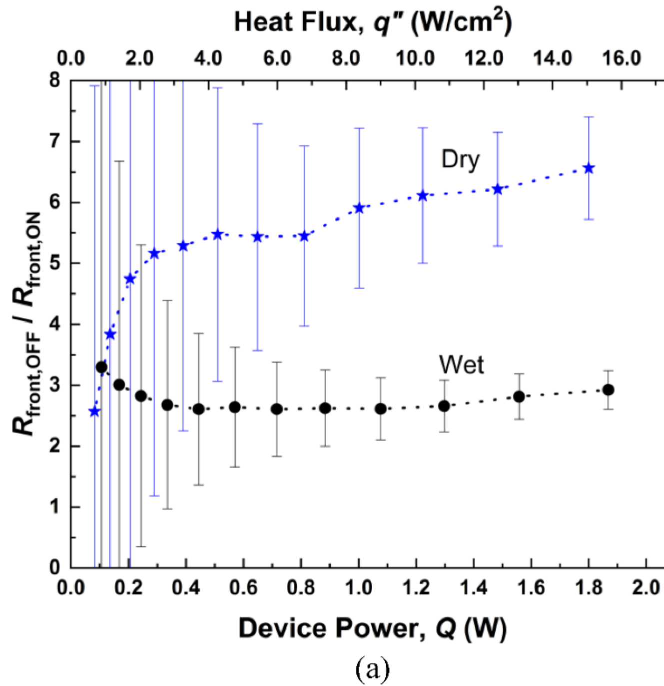


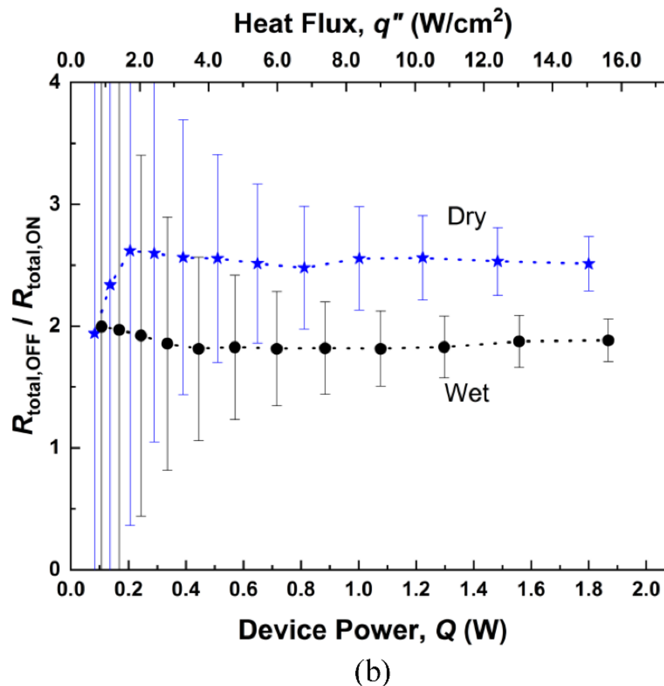
(b)

Figure 3.9 Front side heat transfer ratio to the total heat dissipation rate (Q_{front} / Q) through the integrated thermal switch as a function of Q and q” for a (a) dry or (b) wet channel. Dotted trend lines show the trend of the heat transfer ratio. The errors were estimated by a propagation method from the junction temperature error (±1.6°C) and the ambient air or coolant temperature error (±1.5°C).

Figure 3.10 shows the thermal switching ratios defined by the front side heat transfer ($R_{front,OFF}$ / $R_{front,ON}$) and by the total heat transfer ($R_{total,OFF}$ / $R_{total,ON}$) for wet and dry channels as a function of device power and heat flux. The switching ratio quantifies the capability of the thermal switch to manipulate heat transfer [19]. The front side switching ratio was approximately 6 for the dry channel and 3 for the wet channel. The total switching ratio was approximately 2.5 for a dry channel and 2 for the wet channel. The dry channel device had a higher switching ratio than the wet channel due to the larger thermal resistance of the dry channel in the OFF mode. For both dry and wet channels, the front side switching ratio was higher than the total switching ratio due to the presence of the back side thermal pathway which acts to dilute the heat transfer selectivity. By integrating a dry or wet thermal switch with a single GaN device, the heat transfer can be manipulated from the front side to the back side or vice versa by switching ON or OFF as needed. It is important to note, the magnitude of the thermal switching ratio will be geometry and orientation dependent. For example, depending on the design of the PCB as well as the packaging of multiple PCBs, the back side thermal transport pathway can be reduced further, giving rise to higher switching ratios.



(a)



(b)

Figure 3.10 (a) The front side thermal switching ratio $R_{\text{front,OFF}}$ / $R_{\text{front,ON}}$ and (b) the total switching ratio $R_{\text{total,OFF}}$ / $R_{\text{total,ON}}$ as a function of the device power Q and heat flux q". Dotted trend lines show the trend of the switching ratio. The errors were estimated by a propagation method from the junction temperature error (±1.6°C) and the ambient air or coolant temperature error (±1.5°C).

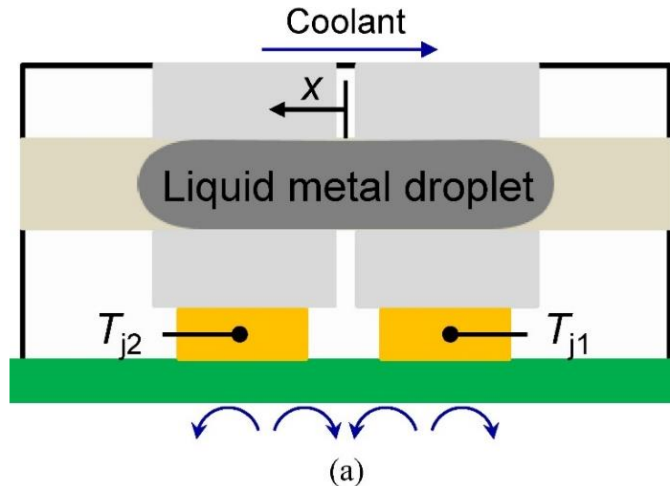
From the perspective of the front side, which is designed to remove the majority of the heat through the ON mode thermal switch, Table 3.1 reveals that the major thermal resistance is the

forced convection thermal resistance. The forced convection by the coolant transfers heat from the thermal switch to the chiller heat sink. The heat transfer coefficient depends mainly on the flow rate and the flow regime of the coolant. To reduce the forced convection thermal resistance and enhance the switching ratio, we can elevate the coolant flow rate, induce the turbulent flow regime, or disturb the flow. The addition of fin structures to the metal conductor contacting the coolant flow could disturb the flow, enlarge the cooling area, and improve the heat transfer near the contact surface. The reduced ON mode thermal resistance has the potential to improve the thermal switch performance further and magnify the switching ratio.

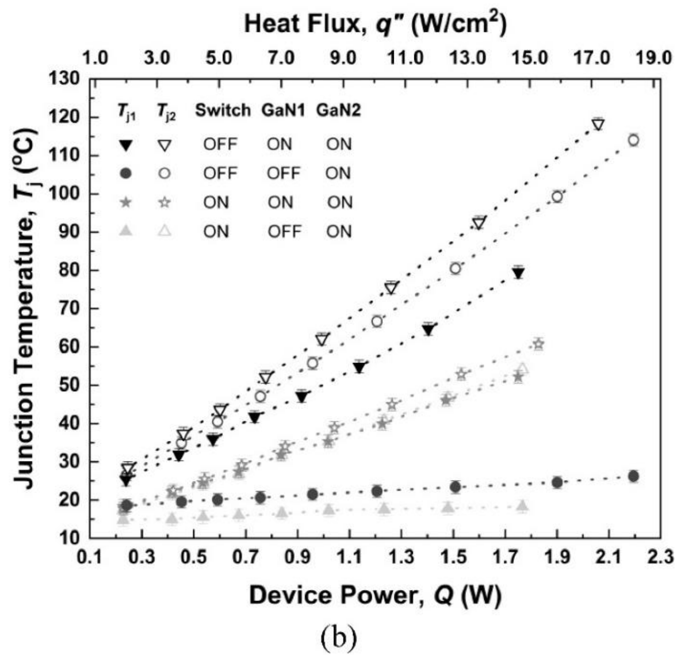
3.5 Demonstration of two devices isothermalization

Having demonstrated the ability to control heat flow from a single PCB-mounted GaN device, we attempted to demonstrate the ability of the thermal switch to maintain two independent GaN devices at a constant temperature via switch control. High power density electronic systems having homogeneous temperature distributions are desired from thermo-mechanical stress and reliability standpoints [24]. Non-isothermal operation of multiple devices on a PCB can lead to thermo-mechanical stress buildup and reliability concerns [25]. Furthermore, isothermalization reduces the heat concentration on the device, spreading the heat transfer from the hot device to the cold device, enabling the more efficient utilization of the heat rejection system [21], [26]. To characterize the isothermalization performance of the integrated thermal switch device, we used the same GaN devices (Fig. 3.3a) and experimental testbed (Fig. 3.3c) with modification to the thermal switch design to be able to conform to two GaN devices instead of one. By precisely controlling the location of the thermal switch in the channel, we could allow for variable thermal pathways to the front side coolant for each switch, and hence temperature equilibration at some optimum set point depending on the GaN device temperature mismatch.

Figure 3.11 shows a schematic of the thermal switch integrated with two GaN devices mounted on the PCB. The liquid metal droplet had dimensions of 1 mm x 5 mm x 22 mm and covered the two GaN devices at the same time. The liquid metal droplet was actuated to move along a wet channel by gravity in the x direction via rotation of the PCB. When the liquid metal droplet resided in the channel covering both GaN devices, as depicted in Fig. 3.11(a), the thermal switch was in the ON mode and the droplet location was defined as $x = 0$. When the liquid metal droplet was moved out of the channel (far from the GaN devices), the thermal switch was in the OFF mode and the droplet location was $x = \infty$. Figure 3.11(b) shows the junction temperatures of the two GaN devices as a function of device powers with the droplet position ranging from $x = 0$ (ON) to $x = \infty$ (OFF). When the left side GaN2 device was powered at 0.2 to 2.2 W and the right side GaN1 device at 0W, the junction temperature T_{j2} was always lower than when both GaN devices were powered at 0.2 to 2.2 W. The concentrated heat flux from GaN2 was reduced due to heat spreading through the liquid metal droplet (Switch ON) or the electrolyte (Switch OFF) in the channel. When both the left side GaN2 and the right side GaN1 devices were powered at 0.2 to 2.2 W, GaN2 always had a higher junction temperature than GaN1 for both the thermal switch in the ON or OFF mode. The temperature difference at identical power levels indicated that the device fabrication or the soldering process was not identical. The presence of a non-uniform temperature distribution at the same power level for multiple independent devices is a common occurrence in electronic systems that can potentially lead to elevated thermomechanical stresses and long-term failure. The non-uniform junction temperatures provided a reference to characterize the thermal switch isothermalization performance by moving the liquid metal droplet along the channel to differing positions.



(a)



(b)

Figure 3.11 (a) Schematic of the integrated thermal switch with two GaN devices mounted on the PCB. (b) Junction temperatures of the two GaN devices (T_{j1} and T_{j2}) as a function of Q and q". The coolant temperature was kept at 5 °C by the chiller to achieve better cooling efficiency. Dotted trend lines show the trend of the junction temperature. The errors were estimated by the junction temperature error (±1.6°C).

Figure 3.12 shows the isothermalization performance of the integrated thermal switch. The normalized temperature difference was defined as $\phi = 2\ (T_{j2} - T_{j1})\ /\ (T_{j2} + T_{j1})$, and acted as a quantifiable measure of the non-uniformity of the junction temperatures between the GaN1 and GaN2 devices. Using the same testbed, we conducted the experiment and powered both GaN

devices at the same power (Q = 1.4 W or Q = 2.1 W). When the liquid metal droplet was removed from the electrolyte filled channel ($x = \infty$), the thermal switch was in the OFF mode. The normalized temperature difference ϕ was 0.173 and 0.160 with the GaN devices powered at 1.4 W and 2.1 W. The higher device power enhanced the temperature uniformity due to elevated heat spreading through the channel. When the liquid metal droplet moved from x = - 7.2 mm to x = + 7.2 mm, ϕ reduced further via efficient heat spreading through the metal droplet. The normalized temperature difference achieved isothermal operation ($\phi = 0$) at x = 6.2 mm, indicating that GaN1 and GaN2 were at the same temperature. Our demonstration shows that the thermal switch is capable of dynamically balancing heat transfer and achieving isothermalization of multi-GaN platforms by switching the liquid metal droplet to fixed positions after integration.

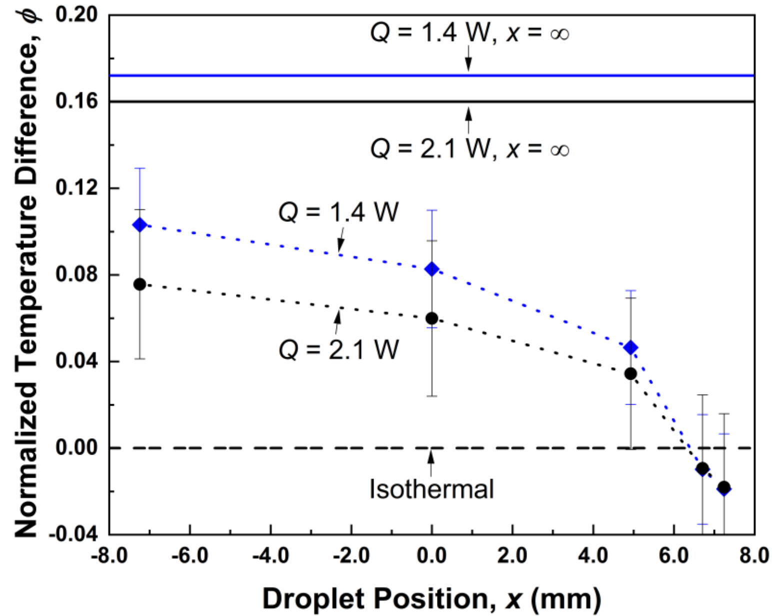


Figure 3.12 Normalized GaN junction temperature difference $\phi = 2\,(T_{j2} - T_{j1}) / (T_{j2} + T_{j1})$ as a function of the liquid metal droplet position x at two different device powers (Q). The $x = 0$ location is defined in Fig. 3.11(a), and represents when the droplet resides in the center of the channel. Dotted trend lines between experimental points show the trend of the normalized temperature difference. Solid lines represent experimental data. The errors were estimated by a propagation method from the junction temperature error (±1.6°C).

The integrated thermal switch platform presented here is translatable to other materials. Although demonstrated here on GaN and focused on power conversion, the thermal switching concept can be used in Si devices, SiC devices, as well as passive components such as inductors and capacitors depending on the PCB layout and design needs. For more complicated applications with irregular heat spikes or thermal cycling, the thermal switch can be integrated together with other thermal management methods, such as phase change materials to store/release energy temporally. Given the centimeter size scale of the integrated thermal switch, inertia becomes a design consideration that must be acknowledged. In our prototype, the maximum switching speed was approximately 1 Hz. Depending on the device needs, smaller more agile thermal switches can be developed with faster response time and lower inertia.

3.6 Conclusions

We measured the thermal management performance of the dry and wet liquid metal thermal switches integrated with a single and two GaN devices. For the single GaN device, we demonstrated that the thermal switch can manipulate the heat transfer effectively. When the GaN device dissipated a heat flux of 15 W/cm^2, the dry thermal switch was able to actively control heat transfer conducting 11 W/cm^2 in the ON mode with the GaN device at 51 °C, and 4 W/cm^2 in the OFF mode with the GaN device at 95 °C. When integrated with two GaN devices, the thermal switch was capable of isothermalizing the two electronic devices with a heat flux of 18 W/cm^2 by the movement of the liquid metal droplet in the wet channel. This work shows a direction to achieve active thermal management on multiple devices via a millimeter scale liquid metal thermal switch. The proposed thermal management design promises applications on enhancing power electronics reliability by addressing temperature mismatch between devices. Our work not only demonstrates the successful integration of a liquid metal thermal switch with a multi-GaN device

platform, it develops the design guidelines for the rational development of millimeter scale thermal switches for electronics applications.

3.7 References

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CHAPTER 4: HEAT SPREADER THERMAL SWITCH FOR POWER CONVERTER ISOTHERMALIZATION

4.1 Introduction

Reliability constraints of power electronic devices are important concerns for the automotive and aerospace industries due to safety requirements [1], [2]. The main reliability challenges come from high-power-density products used in extreme temperature applications and transient operation [3]. Reliability issues due to thermo-mechanical stresses contribute to more than 50% of power electronic stress failures. The majority of failure events occur due to the breakdown of fragile semiconductor components and failure of interconnects between dissimilar materials [1], [3]–[5]. Various thermal management methods can be used to manage thermal energy in semiconductor devices [6]–[9], including air-cooled heat sinks, liquid-cooled microchannel cold plates, pumped two-phase flow cold plates, heat pipes, vapor chambers, liquid spray cooling, and phase change materials [6], [8]. Established thermal management methods mainly focus on managing junction temperatures and do not focus on reducing temperature gradients and concurrent thermal stresses. To address thermo-mechanical stress concerns due to cooling constraints, designers typically focus on circuit layout, component location optimization, or engineering thermal pathways [10]–[12]. Other approaches to mitigate thermo-mechanical stress focus on strategies to reduce temperature swings using resistive heaters or tuning drive signals and device heat losses based on feedback from real-time temperature measurements [12]–[18]. For example, doped silicon, silicide, and metalized tungsten resistive heaters have been integrated and used to stabilize chip temperatures by using heating compensation [16]. However, on-chip fabrication of microscopic heaters alongside devices is necessary to have instant temperature

response [17]–[19]. Moreover, thermal insulation trenches are required to minimize heat leakage. Compared to conventional approaches, a component such as a thermal switch between the converter and heat sink has the potential to be an alternative, simple and passive way to reduce temperature gradients and thermal stresses.

Thermal switches have been used in cryogenic refrigeration, thermal computing, and spacecraft applications where active control of heat transfer is required [20]–[22]. The thermal switch, analogous to an electrical switch, is used to improve heat transfer when the switch is in the ON state and to reduce heat transfer when the switch is in the OFF state [23]. Different types of thermal switches such as magneto-mechanical thermal switches, liquid bridge thermal switches, and variable conductance heat pipes (VCHP) have been developed for various applications utilizing conduction, convection, and radiation heat transfer [24]–[28]. The VCHP can control the thermal conductance and the evaporator temperature of the heat pipe by heating a reservoir of vapor and non-condensable gas [28]. However, the controllability is affected significantly by reservoir size and ambient temperature. Precise evaporator temperature control requires precise, rapid, and active control of reservoir heat input, which undermines applications requiring transient responses at short time scales (< 10 s). Published research on thermal switches mostly focus on controlling heat transfer at the micrometer to nanometer scale. The relatively small size of previous thermal switches prevents their use with power electronic devices which have relatively large active components (mm to cm scale). There is a need for cm-scale thermal switches that can be used for power converter applications that require both heat removal for managing device junction temperature as well as reduction of temperature gradients between active or passive devices and their substrates.

Here, we develop a heat spreader thermal switch consisting of a stainless steel (SS) heat spreader and a copper (Cu) thermal switch. The thermal switch is designed to isothermalize silicon carbide (SiC) devices by improving heat transfer from hot SiC devices and reducing heat transfer from cold SiC devices. By moving the Cu switch embedded in the SS spreader channel from cold SiC devices to hot SiC devices, the thermal resistance from hot SiCs was reduced by efficient heat transfer through the Cu switch. Meanwhile the thermal resistance from cold SiC devices increased due to the presence of the air channel. To enhance the thermal switch controllability, we analyzed the effects of materials and switch geometry to help design a thermal switch prototype based on three-dimensional (3D) finite element method (FEM) predictions. The thin SS heat spreader with a relatively low thermal conductivity is able to confine lateral heat spreading, which is necessary for heat flow controllability through the thermal switch. The Cu switch with a relatively high thermal conductivity reduces the thermal resistance in the ON state and air in spreader channel ensures high thermal resistance in the OFF state. The shape and dimensions of thermal switch are designed considering the power converter topology, power density, temperature gradients, and the response speed relevant to system thermal time constant. We fabricated and integrated the thermal switch with a 60 Hz, 3.5 kW DC/AC power converter. We demonstrate the isothermalization of SiC devices with the converter operating at different conditions by reducing the case temperature difference of the SiC devices from 5°C to 0°C. Furthermore, we use a 3D finite volume method (FVM) simulation to develop an understanding of heat transfer mechanisms, validate the experimental results, and analyze key parameters affecting system performance.

4.2 Concept and design

Figure 4.1 shows the concept of the solid heat spreader thermal switch integrated with two discrete SiC devices (SiC1 and SiC2) connected to the converter printed circuit board (PCB). The

solid heat spreader thermal switch consists of an SS heat spreader and a Cu thermal switch that can move along the air channel embedded in the SS spreader. The heat spreader was constructed of SS 304 material (k_{SS} = 15.9 W/(m·K)), which was rationally selected as the spreader material in order to confine the lateral heat transfer and enhance the temperature controllability of the thermal switch when the spreader conducts heat losses Q_1 and Q_2 from SiC1 and SiC2 to the thermal switch. When the thermal switch is integrated symmetrically with the SiC devices, as shown in Fig. 4.1(a), heat losses ($Q_1 > Q_2$) are transferred to the aluminum (Al) heat sink efficiently, which leads to junction temperature differences between SiC1 and SiC2 ($T_{j,1} > T_{j,2}$). To reduce the temperature difference, the Cu thermal switch is moved closer to the hot SiC1 device by a distance defined as x in Fig. 4.1(b). The Cu thermal switch with thermal conductivity of k_{Cu} = 385 W/(m·K) improves heat conduction from the hot SiC1 device, while the low thermal conductivity air (k_{Air} = 0.024 W/(m·K)) beneath the cold SiC2 device residing in the SS channel reduces heat conduction. By moving the thermal switch to a specific position designed for specified working conditions of the converter, the SiC junction temperature difference can be eliminated.

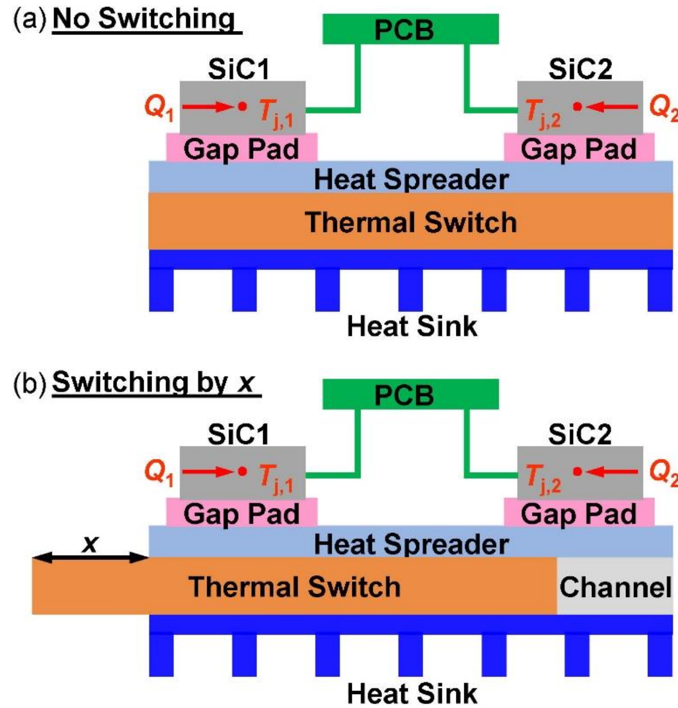

Figure 4.1 Schematic of the solid heat spreader thermal switch integrated with two SiC devices when the Cu thermal switch (a) resides in the air channel and (b) is moved to position x along the channel. Devices SiC1 and SiC2 dissipate Q_1 and Q_2, respectively ($Q_1 > Q_2$), which results in the junction temperature difference ($T_{j,1} > T_{j,2}$) for the condition depicted in (a). The SS heat spreader spreads heat from the SiC devices to the Cu thermal switch. The thermal switch can be moved within the air channel embedded in the SS spreader to transfer heat more efficiently from SiC1 and less efficiently from SiC2 as depicted in (b) in order to isothermalize SiC1 and SiC2 ($T_{j,1} = T_{j,2}$). Once spread through the SS spreader and Cu switch, heat is dissipated to a coolant via a heat sink.

The solid heat spreader developed here was tailored to isothermalize a three-level (3-L) T-type power converter. Figure 4.2(a) shows the circuit topology of the power converter. The 3-L T-type converter is widely used in low- or medium-voltage applications and has advantages over other two-level converters such as simple operation, lower conduction and switching losses, and superior converter output voltage quality [29], [30]. The SiC MOSFETs, used in high-power-density high-efficiency power converters applications such as solar inverter and motor drives [30]–[32], were used as demonstration devices. Each phase of the converter has four SiC devices (C2M0160120D, Cree) shown in Fig. 4.2(a). Two of the devices form a common-source (CS)

configuration (Type 1) while the other two form a half-bridge (HB) configuration (Type 2). The hot SiC devices in the HB configuration withstand the full DC bus voltage, while the cold SiC devices in the CS configuration only block half of the DC bus voltage. In addition, the operating conditions such as switching frequency of these two configurations are different, leading to different device heat losses $Q_1 > Q_2$, as depicted in Fig. 4.1. The different heat losses result in different junction temperatures between the SiC devices when cooled by a homogeneous heat sink without thermal switch integration. Figure 4.2(b) shows the converter efficiency as a function of converter power when the converter works at unity power factor. The heat losses of all components are calculated to obtain the converter efficiency using a precise circuit loss model [30]. The calculated peak efficiency is 98.2% when the converter works beyond 0.6 kW. The circuit topology and heat loss calculations provide a way to obtain heat losses Q_1 and Q_2 of hot SiCs and cold SiCs when the power converter works at different powers and temperatures in our experiments.

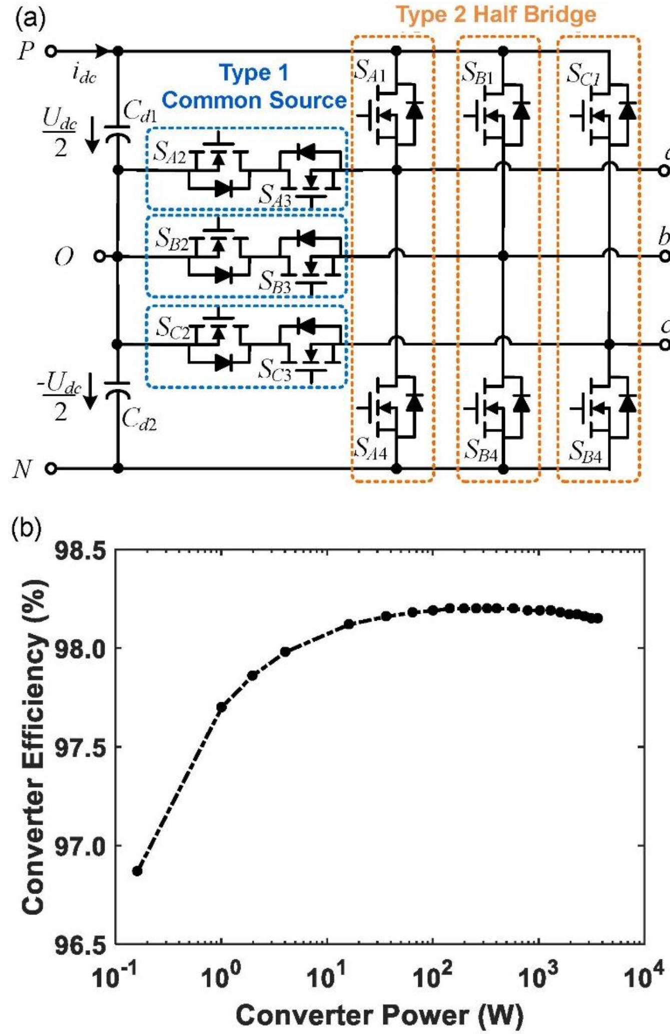

Figure 4.2 (a) Schematic of the three-level T-type converter topology. Cold SiC devices in the type 1 common source dissipate less heat than hot SiC devices in the type 2 half bridge due to their lower voltage load and switching frequency. (b) Efficiency of the T-type converter as a function of operating power with a unity power factor load and 20 kHz switching frequency at 25°C.

To design the heat spreader thermal switch, we used 3D FEM simulations in COMSOL Multiphysics 5.4.0. Figure 4.3 shows the temperature predictions of the integrated heat spreader thermal switch with four SiC devices on one phase of the 3-L T-type converter. The heat spreader had dimensions of 107 mm × 100 mm × 10 mm with 1 mm thick spreader and 9 mm thick air channel, and the thermal switch had dimensions of 107 mm × 80 mm × 9 mm, designed according to the converter size requirement. The 3D FEM model was built to study the thermal performance

of the switch when the converter worked at different conditions. Temperature-dependent heat losses Q_1 and Q_2 from the hot and cold SiC devices were obtained from a precise circuit model [30] and were modeled as volumetric heat sources in the FEM thermal simulations. The heat sink beneath the thermal switch was cooled by air at temperature T_{Air} = 25°C with an effective spatially-averaged forced convection heat transfer coefficient of h = 100 W/(m^2·K) as the bottom boundary condition. Fins were not included at the bottom convective boundary condition as the area enhancement stemming from the fins was lumped in with the higher than average effective heat transfer coefficient used. The black-anodized Al heat sink (394-2AB, Wakefield-Vette) has a thermal conductivity of k_{Al} = 220 W/(m·K), with a 5 mm thick base, and 2 fins per inch that were 1.5 mm thick and 33 mm long to provide sufficient heat spreading for efficient air cooling. Other surfaces of the integrated assembly were assumed to undergo natural convection with the surrounding air with a spatially averaged heat transfer coefficient of 10 W/(m^2·K). The thermal contact resistance between the heat spreader and the thermal switch was estimated to be 500 (mm^2·K)/W based on the 300 μm thick gap on each side filled with silicone oil lubricant having a thermal conductivity of 0.6 W/(m·K) [33]. The thermal impedance between the SiC device and the heat spreader was simulated by the 150 μm thick silicone pad which has a thermal conductivity of 0.9 W/(m·K) [34]. The Kapton reinforced silicone pad was necessary as an electrical insulation medium. Hot SiC devices (SiC1 and SiC4) were simulated as volumetrically distributed heat sources with the same high heat loss. Whereas, cold SiC devices (SiC2 and SiC3) were heat sources with the same low heat loss. A fine mesh with high element quality was generated and grid independence was checked. For example, when the Cu switch was in the spreader channel symmetrically without movement, a mesh with 228,223 elements was generated with a 0.63 skewness. A nonlinear solver solved for the steady-state temperature distribution with convergence

after 4 iterations and a residual of $< 4 \times 10^{-5}$. The grid independence was checked by using two finer meshes with 724,988 and 2,680,326 elements, showing maximum temperatures of 43.94°C and 43.96°C, with variances of < 0.1°C compared to 43.86°C using the coarse mesh. For the preliminary design of the heat spreader thermal switch, heat transfer of the single phase was assumed to be independent of the other two phases of the converter. When the thermal switch was placed symmetrically in the spreader channel at position $x = 0$, hot SiC1 and SiC4 had maximum case temperatures of 44°C, higher than the 37°C case temperatures of cold SiC2 and SiC3, as shown in Fig. 4.3(a). To minimize the temperature difference of 7°C, the thermal switch was moved along the spreader channel to $x = 27$ mm. Improved heat conduction from the hot SiC1 and SiC4 devices as well as reduced heat conduction from cold SiC2 and SiC3 devices resulted in isothermalization between the devices, which all approached 44°C (Fig. 4.3b). Side-view temperature profiles shown in Fig. 4.3(c) and Fig. 4.3(d) revealed that the temperature gradient in the Cu thermal switch was significantly smaller than that of the SS air channel. The change of temperature gradients indicated how the thermal switch manipulated heat transfer pathways from the SiC devices to the heat sink. The temperature predictions of the FEM simulations show that the solid heat spreader thermal switch design is capable of eliminating temperature differences between SiC devices by moving the Cu thermal switch to a specific position.

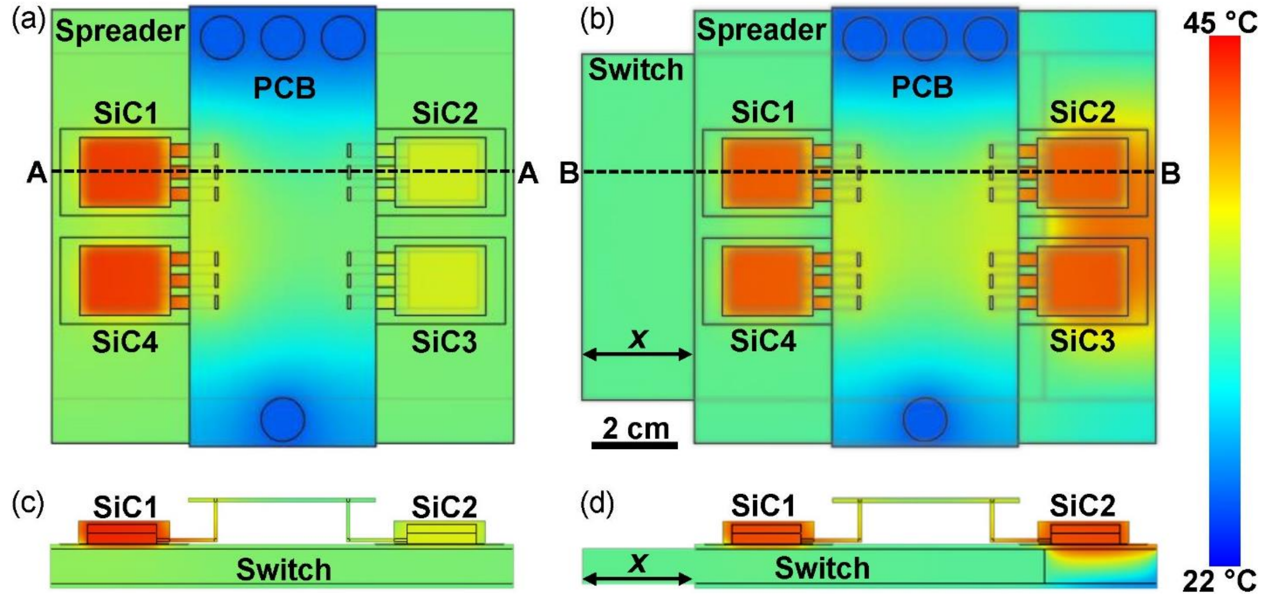

Figure 4.3 Top-view temperature distributions of the power converter single phase integrated with the thermal switch obtained from 3D FEM simulations when the thermal switch resides in the channel at (a) $x = 0$, and (b) $x = 27$ mm. When the thermal switch moves from $x = 0$ to 27 mm, the hot SiC devices (SiC1 and SiC4) decrease slightly in temperature due to more heat spreading from the thermal switch. However, the cold SiC devices (SiC2 and SiC3) increase in temperature due to larger thermal impedance resulting from the SS air channel. The simulation assumes a converter power of 2.4 kW with hot SiC devices dissipating $Q_1 = 4.7$ W and cold SiC devices dissipating $Q_2 = 1.7$ W. Side-view temperature distribution of cross sections (c) A-A and (d) B-B. The air-side heat sink is not shown for clarity.

Figure 4.4(a) shows FEM simulation results of the temperature difference between the hot and cold SiC devices as a function of the thermal switch position (x). The temperature difference was defined as $\Delta T = T_{\text{hot}} - T_{\text{cold}}$, where T_{hot} and T_{cold} represents the average maximum junction temperatures of the hot SiC devices (SiC1 and SiC4) and the cold SiC devices (SiC2 and SiC3), respectively. Hot SiC devices SiC1 and SiC4 operate at the same conditions with approximate junction temperatures, while cold SiC devices SiC2 and SiC3 operate at the same conditions with approximate junction temperatures. When the power converter operated at 2.4 kW, and the heat sink was cooled by air forced convection, ΔT decreased from 7°C to 0°C by moving the thermal switch to $x = 27$ mm. The temperature difference was eliminated due to improved heat conduction from hot SiC devices and reduced heat conduction from cold SiC devices through the heat spreader

thermal switch to the heat sink. Moving the thermal switch beyond the optimum point ($x > 27$ mm) resulted in a negative temperature difference, indicating that the less efficient heat transfer from the cold SiC devices (SiC2 and SiC3) through the air channel increased T_{cold} to exceed T_{hot}. The trends of T_{cold} and T_{hot} are shown in Fig. 4.4(b). However, ΔT showed a local minimum at $x = 43$ mm, becoming positive at $x > 77$ mm due to the less efficient heat transfer from the hot SiC devices (SiC1 and SiC4). The first isothermal position at $x_1 = 27$ mm was preferred for experimental testing when compared to the second ($x_2 = 77$ mm), since the SiC devices were 3°C colder due to more heat spreading from the thermal switch shown in Fig. 4.4(b). When the thermal switch moved beyond 30 mm, the majority of the heat loss from cold SiC devices transferred through the spreader, device surfaces, leads, and PCB by natural convection instead of the thermal switch. Therefore, switch movement beyond 30 mm did not significantly affect heat transfer and junction temperatures of cold SiC devices. Moreover, FEM simulations with a solid Al spreader having same dimensions with our heat spreader thermal switch were conducted as a reference. Simulation results show that heat spreading through the Al spreader was sufficient and addition of thickness caused negligible temperature changes. Compared with an Al spreader, the heat spreader thermal switch eliminated the temperature difference at a penalty of increasing the junction temperature by 4°C.

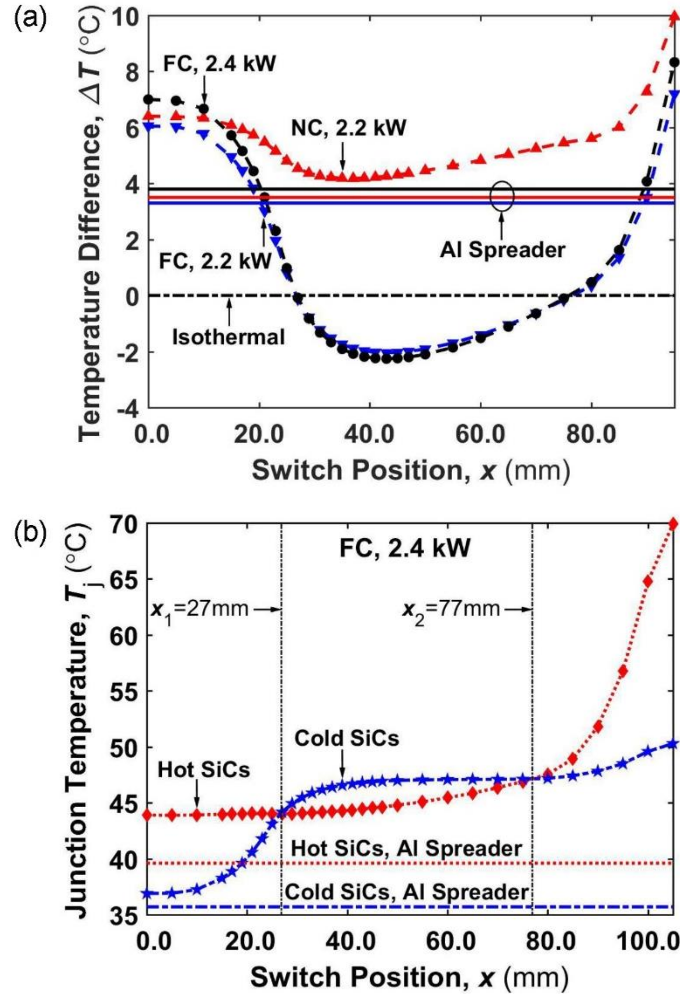

Figure 4.4 (a) 3D FEM simulation results showing the SiC device temperature difference ($\Delta T = T_{\text{hot}} - T_{\text{cold}}$) as a function of switch position (x) when the converter operates at different powers, where T_{hot} and T_{cold} represent the average junction temperatures of hot SiC devices (SiC1 and SiC4) and cold SiC devices (SiC2 and SiC3), respectively. Dashed lines represent trend lines. Solid lines represent the temperature difference present with a solid Al spreader and heat sink. (b) Absolute temperatures of hot and cold SiC devices as a function of switch position (x) when the power converter operates at 2.4 kW cooled by forced convection of ambient air. The results were obtained with 3D FEM simulations. The switch position x = 0 is shown in Fig. 4.3(a), and represents the case when the Cu block resides symmetrically under the SiC devices with the spreader channel filled with the Cu switch.

To understand how the converter power level affects device isothermalization, we simulated a second case where the power converter operated at 2.2 kW. The simulations showed similar trends of temperature difference due to the similar heat transfer mechanisms (Fig. 4.4a). Interestingly, the FEM simulations showed that when the converter was cooled by natural

convection of air using the same heat spreader with heat sink and a convective heat transfer coefficient of 10 W/(m^2·K) instead of 100 W/(m^2·K), the temperature difference could not be eliminated by moving the thermal switch. The reason for the loss of temperature control using the thermal switch is due to the increased heat transfer from top-side natural convection, and reduced heat transfer through the thermal switch itself, limiting the impact of Cu position SiC junction temperatures. The presence of forced convection on the back side ensures that the majority of heat losses are conducted through the thermal switch, resulting in enhanced device temperature control. The results indicate that the developed thermal switch operates with higher efficacy when the thermal resistance from junction to coolant (through the switch) is minimized, and parasitic losses away from the switch are eliminated. For the 2.2 kW converter power case, the temperature difference was minimized to 4.2°C when the thermal switch was at x = 37 mm. In order to benchmark our thermal switch results to a conventional solution (solid heat sink with no switch), we conducted additional FEM simulations for a solid Al heat sink. The FEM results showed that although an all Al heat sink results in lower device case temperatures (Fig. 4.4b), the temperature difference between hot and cold SiC devices ranged from 3.3°C to 3.8°C (Fig. 4.4a). The solid Al heat sink results point to the need for integration of a thermal switch in order to manipulate heat transfer and achieve device-to-device isothermalization.

Furthermore, the FEM simulations point to the need for rational selection of the thermal switch spreader material in order to enable device-to-device temperature control. Although utilization of a homogeneous high thermal conductivity heat sink reduces both device-to-device temperature difference as well as absolute junction temperature, it fails to eliminate or provide any control of device-to-device temperature difference. Indeed, past studies have shown that static temperature gradients and cyclic temperature swings can be key failure points for devices

operating in the field for years [2], [35], demonstrating the need for thermal switching and careful selection of the heat spreader material. In our case, SS was chosen due to its ability to limit lateral conduction from the hot to cold SiC devices, and better parallelize the heat flow patch from the device junction to the coolant on the back side. Similarly, the thin heat spreader with 1mm thickness was designed to reduce lateral heat spreading from the SiC devices and enhance normal heat transfer to the thermal switch. In essence, our heat spreader is a poor spreader by design in order to enable temperature control.

Figure 4.5 shows the FEM simulation results of spreader effects on thermal switch performance when the converter operated at 2.4 kW with air forced convection. Here, we investigated thermal conductivity (k) and thickness (d) of the heat spreader. The effect of three 1mm thick spreaders with thermal conductivities of k = 4, 40, and 220 W/(m·K) on SiC junction temperatures as a function of switch position was explored in Fig. 4.5(a). The poor spreader increased temperatures of both hot and cold SiC devices, meanwhile, provided an opportunity to isothermalize SiC devices when the thermal switch was moved to 25 mm or 80 mm. However, the spreader with a highest thermal conductivity showed negligible controllability of device temperatures when moving the thermal switch. The spreader with a mediate thermal conductivity had advantages of both decreased absolute temperatures and minimum temperature difference. The minimum temperature difference ΔT indicates the heat spreader controllability of the hot and cold SiC devices. The achievable minimum temperature difference ΔT as a function of the spreader thermal conductivity is shown in Fig. 4.5(b). The minimum ΔT increased with spreader thermal conductivity due to enhanced lateral heat spreading from hot SiC devices to cold SiC devices. Lower minimum ΔT implies better capability of the heat spreader to increase T_{cold} and decrease T_{hot}, which thus ensures better tolerance to achieve isothermalization by moving the thermal

switch. SS 304 was chosen as the spreader material not only to decrease absolute device temperatures but also to provide a tolerance of -2.3°C minimum ΔT for experiments. Moreover, the effect of the SS 304 spreader thickness on temperatures of hot and cold SiC devices is shown in Fig. 4.5(c). The use of a thicker spreader (d = 8 mm) hindered temperature controllability by stemming normal heat transfer and enhancing lateral heat spreading through a broader lateral area, compared with our thin spreader (d = 1 mm). Figure 4.5(d) shows the trend of achievable minimum ΔT increasing with the spreader thickness. Our SS heat spreader was designed to be 1 mm thick considering both minimum ΔT and easiness of manufacturing.

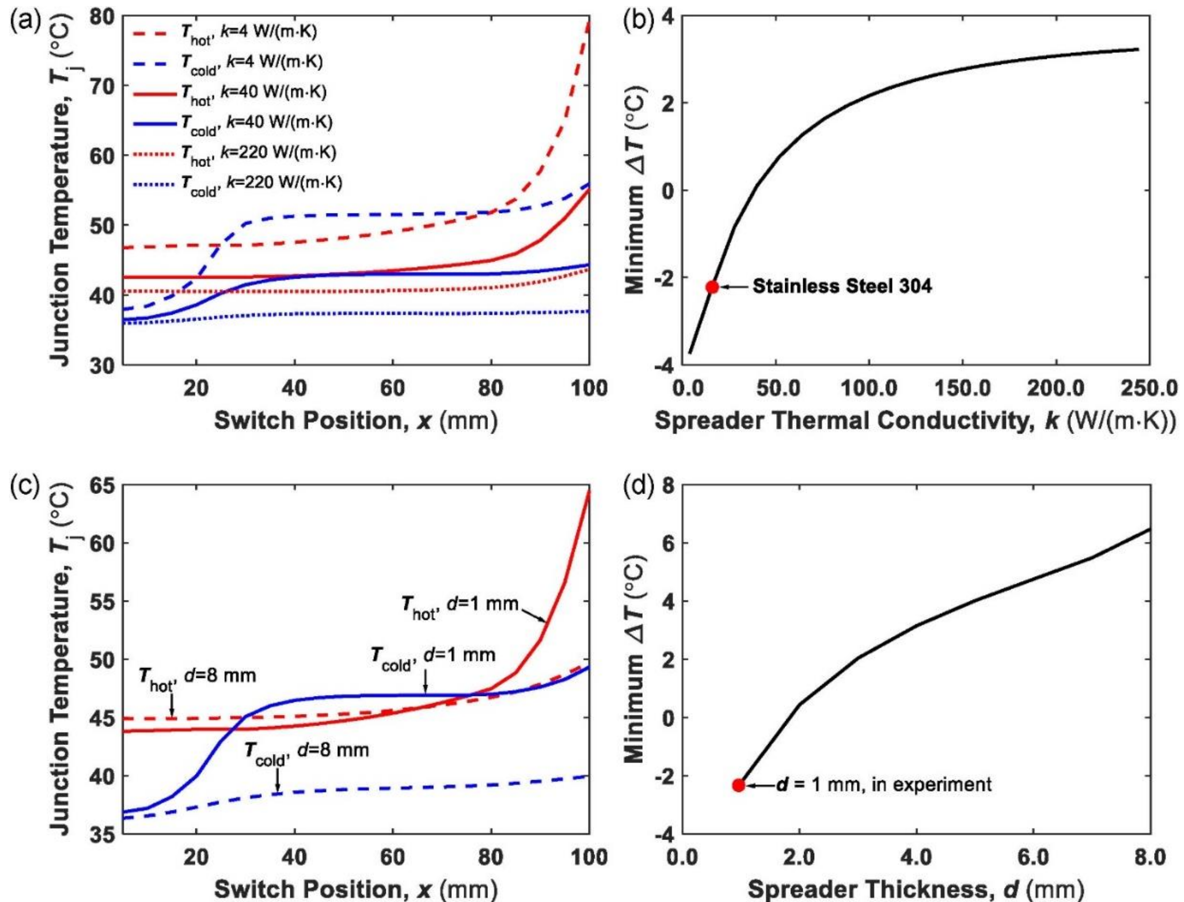

Figure 4.5 The effects of heat spreader parameters on thermal switch performance. (a) SiC junction temperatures T_j and (b) minimum achievable temperature difference ΔT as a function of the spreader thermal conductivity k. (c) SiC junction temperatures T_j and (d) minimum achievable temperature difference ΔT as a function of spreader thickness d. Simulations used converter power of 2.4 kW with forced convection air cooling.

4.3 Experiments and finite volume method simulations

Figure 4.6 shows the thermal switch before and after integration with a single phase of the power converter along with a schematic of the experimental setup. The Cu thermal switch was embedded in the SS heat spreader and could move along the channel with a distance of x shown in Fig. 4.6(a). A thin layer (≈300 μm) of commercial lubricant (93744, Super Lube) was applied to the interface of the thermal switch and the heat spreader to facilitate easy sliding movement. Due to the good wettability, we did not observe lubricant pump out of the interface during cyclic movement of the thermal switch in our experiments. Nevertheless, for real applications requiring long-time field operation, a risk of lubricant pump out exists; in which case lubricant re-supply needs consideration. Thermal interface materials were attempted to be used as a replacement of the lubricant, with limited efficacy due to the lack of lubricity (high viscosity) needed to enable smooth motion of the Cu switch. The low thermal conductivity (≈ 0.6 W/(m·K)) of the lubricant resulted in a large interfacial thermal resistance and increased isothermal temperatures, which will be discussed later in the finite volume method (FVM) simulations. Figure 4.6(b) shows a schematic of the experimental setup. The power converter converted a DC voltage from a DC power supply (XR 375-26.5/380+HS+LXI, Magna-Power Electronics) to three-phase AC voltage applied to an AC load consisting of capacitors, inductors, and resistors. Three-level space-vector modulation (SVM) controlled the converter to generate 60 Hz output voltages with 20 kHz switching frequency. The SVM control scheme was implemented with a digital signal processing (DSP) unit (Texas Instruments, TMS320F28335). An infrared (IR) camera (A655sc, FLIR) was used to obtain the temperature profile of phase A (ΦA) integrated with our thermal switch as shown in Fig. 4.6(c). The integrated thermal switch and the other two phases without thermal switches (ΦB and ΦC)

were each cooled by single and independent Al heat sinks (394-2AB, Wakefield-Vette). Airflow at a volumetric flow rate of 35.9 CFM at the room temperature was delivered by independent fans (8500DP, ebm-papst Inc.) rotating at 3200 RPM beneath each heat sink (not shown in Figure 4.6). The fan speed was chosen based on the rated speed which resulted in turbulent flow between the fins. Prior to running experiments, a hot wire anemometer was used to measure the fan speed between each phase at the center of the fan, showing a deviation of <2% from phase-to-phase. Mounting of the thermal management was achieved using a commercial gap pad (SIL-PAD 400, BERGQUIST) having thermal conductivity of 0.9 W/(m·K) and thickness of ≈ 200 μm. The hot SiC devices in ΦB spread a certain amount of heat to the adjacent cold SiC devices (SiC2 and SiC3) in ΦA, which reduced the measured hot-to-cold device temperature difference (ΔT) in our experiments. The dashed blue box (Fig. 4.6c) indicates the IR imaging region, which focused on four SiC devices (SiC1, SiC2, SiC3, and SiC4). The heat spreader thermal switch was integrated with ΦA and the conventional Al heat sink using four socket screws, which were assembled using a torque of 0.042 N·m with a torque screwdriver (S0-24, Seekonk) for SiC device safety and consistency of compression force. After the thermal switch was moved to a certain position x and the system reached thermal steady state, thermal images were recorded for analysis. Prior to imaging, the IR camera was calibrated to ensure accurate device emissivity using a small piece of highly emissive black tape adhered directly on the SiC device. After adhering the black tape, the converter was turned on gradually with SiC device temperature ranging from 25 to 70°C in 5°C increments, enabling accurate characterization of the temperature-dependent SiC case emissivity. The detectable temperature difference of the IR camera is as small as 50 mK, good enough for to provide a consistent temperature comparison between hot and cold SiC devices. It is necessary to point out that we only demonstrated thermal switch integration with ΦA since the other two phases

have a similar circuit layout and heat loss profile. The hot SiC devices on the left side of *Φ*B spreads heat to adjacent phase A and warms up cold SiC devices (SiC2 and SiC3) shown in Fig. 4.6(c). The heat transfer pathway from *Φ*B will be addressed in later using 3D FVM simulations of *Φ*A by tuning the junction-to-bottom thermal impedances of SiC2 and SiC3.

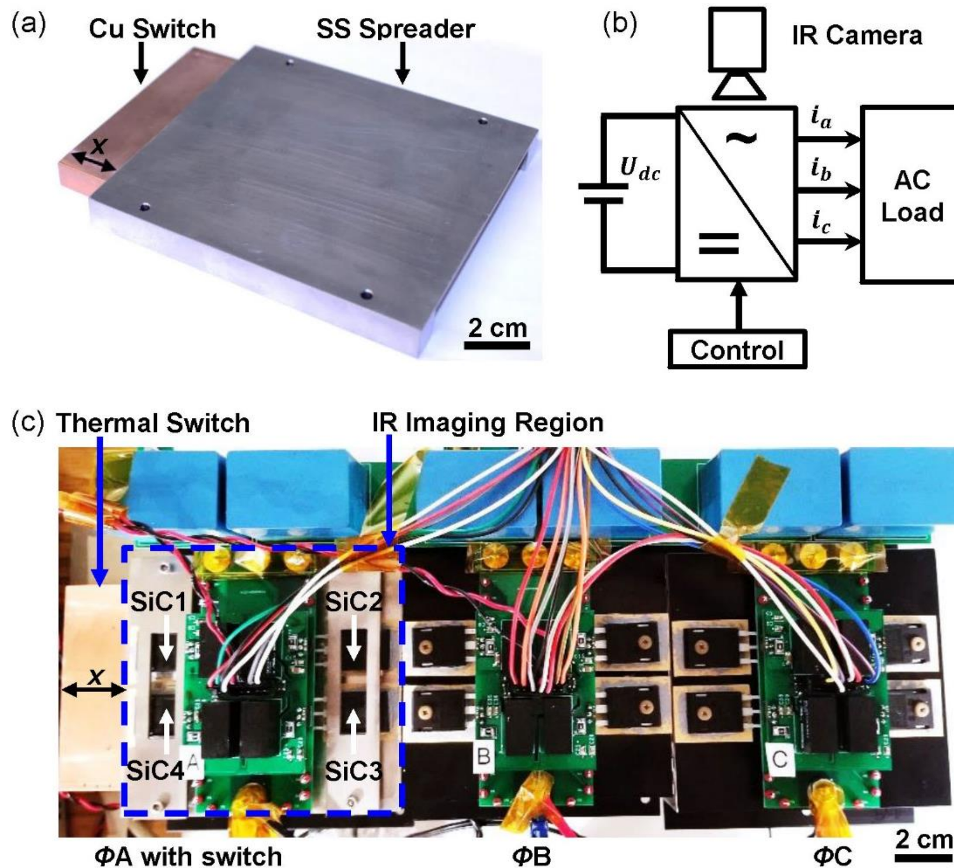

Figure 4.6 (a) Isometric view of the manufactured heat spreader thermal switch showing the Cu switch at the $x = 20$ mm position. (b) Schematic of the experimental test rig used to characterize the performance of the thermal switch integrated with the prototype three-phase T-type converter. (c) Top-view photograph of the integrated thermal switch with the three-phase T-type converter. Phase A (*Φ*A) was integrated with the thermal switch and a conventional Al heat sink beneath it (not shown). Phase B (*Φ*B) and phase C (*Φ*C) were not integrated with the thermal switch and were instead cooled by conventional Al heat sinks (394-2AB, Wakefield-Vette).

Figure 4.7 shows the zoomed-in *Φ*A thermal images when the Cu thermal switch was moved to different positions. For these experiments, the power converter operated at 2.4 kW with the Al

heat sink beneath the thermal switch cooled by air forced convection. The power level was limited below 3 kW because the SiC devices used in our experiments have an alternating current rating of 19 A that decreases to 10 A when the device temperature increases to 120°C. The case temperatures of the hot SiC1 and SiC4 devices decreased slightly as x increased due to more efficient heat spreading through the thermal switch. On the contrary, the case temperatures of cold SiC2 and SiC3 increased with increasing x due to less efficient heat transfer through the SS air channel after the Cu thermal switch moved further away from the devices. The hot and cold SiC devices had the same case temperature of 41.5°C when the thermal switch moved to $x = 20$ mm. The hot area in the center of each thermal image consisted of the ΦA gate drivers, which consisted of the common-mode filter, isolated power supply, logic circuity, and driver circuity. The gate drivers had a constant temperature profile and were not affected by the Cu thermal switch movement due to the gate driver being suspended on top of the phase leg circuit PCB, eliminating physical contact with the thermal switch. From the thermal images, T_{Hot} was obtained by averaging the maximum temperatures of SiC1 and SiC4 devices and T_{Cold} was obtained by averaging the maximum temperatures of SiC2 and SiC3 devices.

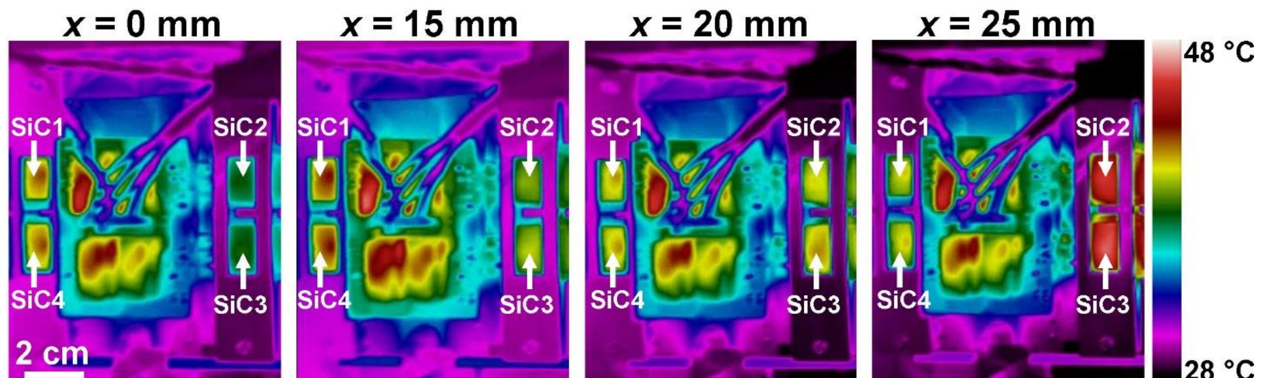

Figure 4.7 Top-view IR images of ΦA (Fig. 4.6c) with the Cu thermal switch at different positions (x). The converter was operated at a power input of 2.4 kW while the Al heat sink beneath the thermal switch was cooled by forced convection of airflow using a fan.

In order to verify the experimental results, model the thermal pathways of the prototype, and study the key parameters that dominate isothermalization capability of the heat spreader thermal switch, a separate 3D finite volume method (FVM) simulation was developed (Fig. 4.8). Computational fluid dynamics (CFD) FVM simulations were used to model the heat and mass transfer, since the heat transfer coefficient distribution was highly non-uniform due to the non-uniform velocity of the air delivered by a fan perpendicularly to heat sink fins. The CFD FVM model consisted of ΦA of the power converter, the SS heat spreader, the Cu thermal switch, and the Al heat sink cooled by the airflow from a fan (Fig. 4.8a). To simulate forced convection, a cabinet containing the whole assembly and the air as the working fluid was built, but not shown for clarity. The cabinet had four side walls 110 mm away from the assembly, one bottom opening 110 mm away from the bottom heat sink, and one top opening 500 mm away from the top PCB. The airflow field delivered by the fan from the bottom opening was computed by solving the coupled Navier-Stokes equations, heat equation, and the characteristic equation of the fan volume flow rate versus pressure drop characteristics. Prior to running the simulations, meshing of the solid and air domains was done separately to reduce mesh complexity. The PCB mounted SiC devices, the heat spreader thermal switch, and heat sink were meshed as separate parts to avoid mesh bleeding due to high aspect ratios of the PCB, SiC device leads, and gap pads. The mesh density of the PCB mounted SiC devices was 5 times that of the heat spreader thermal switch, and 10 times the heat sink and air domain. Grid independence was checked by comparing simulation results with finer meshes. After 100 iterations, the computation converged with residuals less than 1×10^{-4}. A turbulent solver using the two-equation turbulence model was applied with Reynolds number $Re > 50{,}000$. The thermal properties of air such as density and thermal conductivity were modeled to be temperature dependent. The remaining materials in the simulation domain were

modeled assuming constant properties. A side view of the FVM model domain is shown in Fig. 4.8(b), labeling the key thermal contact resistances: $R_{spreader\text{-}switch}$ between the heat spreader and the thermal switch, and $R_{switch\text{-}HS}$ between the thermal switch and the heat sink. The thermal contact resistances dominated the thermal impedances from the heat spreader thermal switch and affected the heat transfer performance adversely. Heat transfer pathways from the SiC device junction are affected by the thermal resistances from the junction to the six surfaces of the package, as shown with a simplified thermal resistance diagram in Fig. 4.8(c). Real SiC devices were not easy to model due to the complicated internal SiC chip structure, wires to the three leads, metal spreader, and plastic package. For steady-state thermal modeling, the dominant parameters were the thermal resistances which were obtained from the SiC device manufacturer datasheet [36], eliminating the need to model the entire device structure using heat generation at the junction node. Therefore, only the SiC junction-to-side ($R_{j\text{-}s}$), junction-to-top ($R_{j\text{-}t}$), and junction-to-bottom ($R_{j\text{-}b}$) thermal resistances were modeled in our 3D FVM simulations by referring to the SiC device datasheet and experimental results. In the real experiments, heat transfer in ΦA of the power converter was affected by adjacent ΦB hot SiC devices shown in Fig. 4.8(c), which acted to increase the temperatures of the cold SiC devices in ΦA. Our FVM model focused on the thermal switch integrated ΦA to save computational time and cost. To simulate the heat transfer pathways from adjacent ΦB, the thermal resistance $R_{j\text{-}b}$ of the cold SiC devices neighboring hot SiC devices in ΦB was iterated by fitting with experimental results. Heat losses calculated from a precise circuit loss model were applied to the junction nodes of SiC devices, modeled as heat sources. With thermal resistances and heat losses as input parameters, the temperature distribution and air velocity field were solved with the FVM simulation. A combination of FVM simulations and

experimental results determined the key parameters to analyze thermal performance of the thermal switch to isothermalize SiC devices.

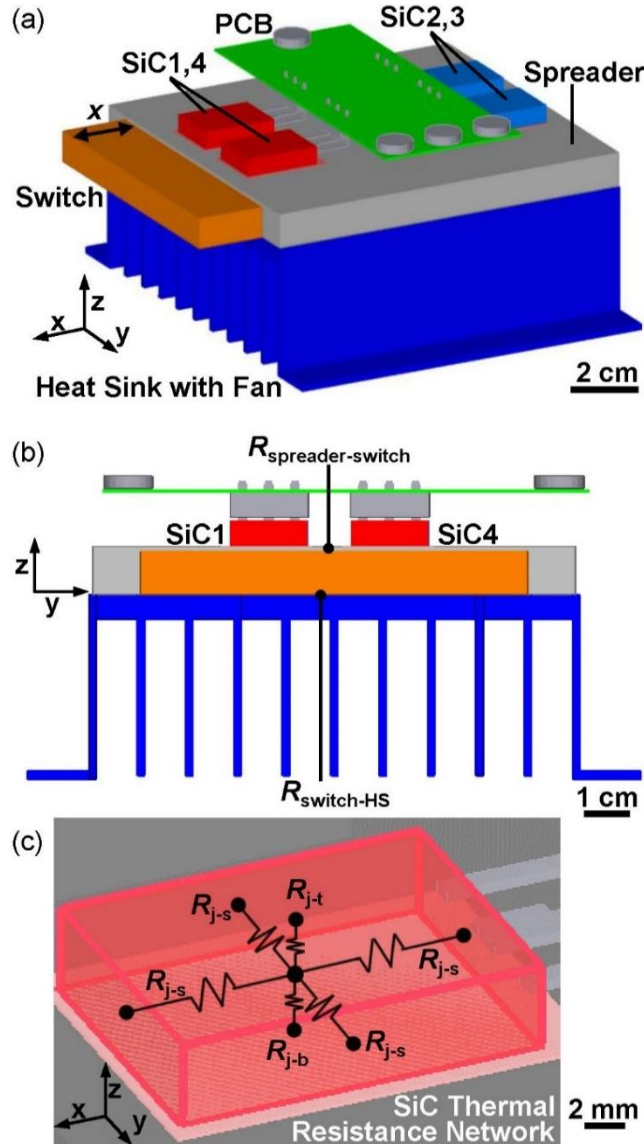

Figure 4.8 (a) 3D Finite-volume-method (FVM) simulation model built to analyze the heat transfer of *Φ*A of the power converter integrated with the thermal switch, including the external air-side heat dissipation mechanism. The fan, having a known volumetric flow rate versus pressure drop relation (8500DP, ebm-papst Inc.), is not shown for clarity. (b) Side-view of the FVM model depicted in (a) showing the key thermal contact resistances between the heat spreader and the thermal switch ($R_{spreader-switch}$) and the thermal switch and the heat sink ($R_{switch-HS}$). (c) Simplified thermal resistance network of a single SiC device showing the effective thermal resistances from the junction to the six surfaces of the device package. Relevant thermal resistances were obtained from the manufacturer datasheet [36].

Table 4.1 summarizes the heat losses and thermal resistances when the power converter operated at different conditions. In case i, the power converter was operated with an input power of 2.4 kW. The heat loss Q_1 from each hot SiC device and Q_2 from each cold SiC device were analyzed by a real-time loss model with converter power, switching frequency, and temperatures as input parameters [30]. In case ii, the input power of the converter decreased to 2.2 kW, which lowered heat losses Q_1 and Q_2. In case iii, the fan was turned off and the heat sink was cooled by air natural convection, while the power converter operated at 2.2 kW. Comparing case iii with case ii having the same converter power, the temperature-dependent heat losses increased owing to the higher conduction losses of the less efficient SiC devices [30], since the temperatures of the SiC devices increased due to less efficient heat removal from natural convection (case iii). The thermal contact resistances $R_{\text{spreader-switch}}$ and $R_{\text{switch-HS}}$ were estimated from previous work [33] and determined by fitting our 3D FVM results with our experimental results. The thermal resistances of the SiC device were obtained from the manufacturer datasheet [36]. However, the junction-to-bottom thermal resistance $R_{\text{j-b,cold}}$ of the cold SiC devices was variable in order to account for the heat transfer pathway from the adjacent hot SiC devices of ΦB , which warmed up the cold SiC devices of ΦA. The effect of the added heat transfer pathway was facilitated by more lateral heat spreading and less heat sink cooling due to natural convection, resulting in larger $R_{\text{j-b, cold}}$ in case iii when compared to cases i and ii.

Table 4.1 List of heat losses and thermal resistances.

Case	Power, P [kW]	Cooling Method	Q_1 [W]	Q_2 [W]	$R_{\text{spreader-switch}}$ [(mm^2·K)/W]	$R_{\text{switch-HS}}$ [(mm^2·K)/W]	$R_{\text{j-t}}$ [K/W]	$R_{\text{j-s}}$ [K/W]	$R_{\text{j-b, hot}}$ [K/W]	$R_{\text{j-b, cold}}$ [K/W]
i	2.4	Air Forced Convection	4.7	1.7						1.2
ii	2.2	Air Forced Convection	4.1	1.5	500	500	6	12	0.4	1.2
iii	2.2	Air Natural Convection	4.3	1.6						2.0

The FVM simulation results of case i are shown in Fig. 4.9, utilizing key parameters from Table I in the model. The hot SiC1 and SiC4 devices had average case temperatures of 42°C, approximately equivalent to the SiC2 and SiC3 devices when the thermal switch was moved to x = 20 mm (Fig. 4.9a). The heat losses from the SiC devices was transferred mostly from the heat spreader thermal switch to the heat sink, partially through the Cu electrical connections to the PCB, and partially from the package to the surrounding ambient air at 25°C via natural convection. Figure 4.9(b) shows the temperature profile of cross section A-A depicted in Fig. 4.9(a). The thermal switch conducted heat more efficiently from hot SiC devices; however, the air channel embedded in the SS heat spreader conducted heat less efficiently from cold SiC devices, resulting in a larger temperature gradient in the channel under SiC2 (Fig. 4.9b). The Al heat sink beneath the thermal switch transferred the heat convectively to the airflow indicated by the black arrows. The movement of the thermal switch caused asymmetric airflow around ΦA of the converter. The precise FVM models developed here matched experimental results well, enabling us to predict thermal performance of the thermal switch, and design thermal switches for different electronics designs.

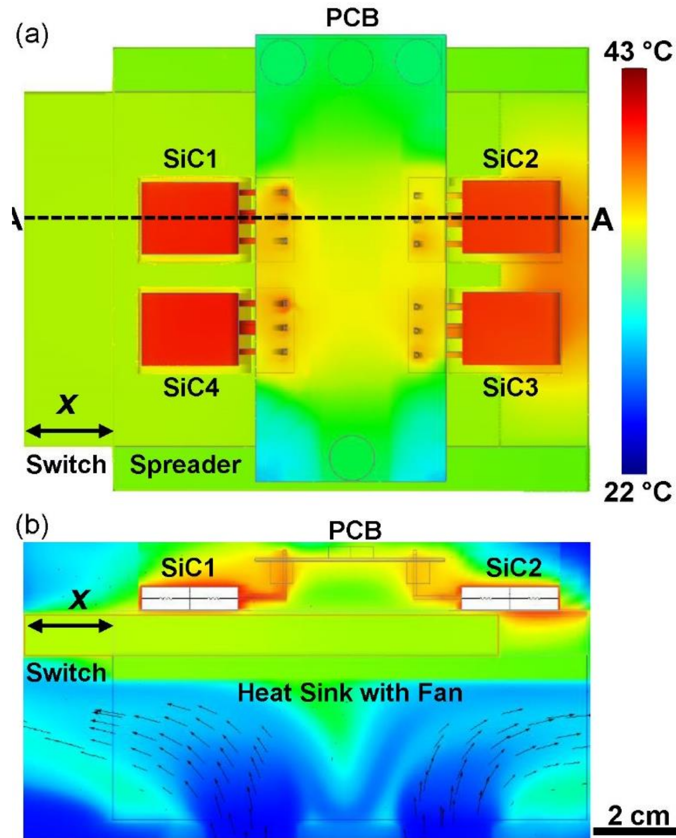

Figure 4.9 (a) Top-view FVM simulation temperature distribution of ΦA with thermal switch at x = 20 mm to isothermalize SiC devices. The simulated converter operated at 2.4 kW with the heat sink cooled by forced convection. (b) Front view of cross section A-A, showing the converter and air temperature distributions. Black arrows represented the airflow velocity, with the maximum arrow size representing 6 m/s. Flow asymmetry arose due to the asymmetric shape of the thermal switch, which blocked airflow on the left side. Heat transfer coefficient was not applied as the boundary condition, while the thermal transport within the fluid domain was resolved in the CFD numerical simulation, which evaluated an average heat transfer coefficient ≈ 100 $W/(m^2 \cdot K)$ in terms of the base area of heat sink.

4.4 Results and discussion

Figure 4.10 shows experimental and simulation temperature results of hot and cold SiC devices as a function of thermal switch position for cases i, ii, and iii (Table I). The excellent agreement between simulations and experiments indicated that the developed FVM simulation was successful at predicting the thermal switch performance and hence was used to analyze key thermal resistances in the integrated assembly. For case i depicted in Fig. 4.10(a) and case ii in Fig. 4.10(b),

the hot SiC device temperatures decreased slightly with increasing switch position. However, the cold SiC device temperatures increased slowly for $x < 15$ mm, rapidly for 15 mm $< x <$ 40 mm, and slowly again for $x > 40$ mm, which indicated that the switching effect was most obvious when the thermal switch was moved in close proximity to the cold SiC devices. When the thermal switch moved to $x = 20$ mm, the hot SiC devices had the same temperature as the cold SiC devices. The similar temperature trend of hot and cold SiC devices was demonstrated for case iii (Fig. 4.10c). However, the isothermalization position of the thermal switch was reduced to $x = 17$ mm due to the less efficient heat transfer from natural convection. Experimental and simulation results demonstrated that the solid heat spreader thermal switch is capable of achieving isothermalization of SiC devices by moving the switch to different positions tailored for this particular power converter operating at different working conditions.

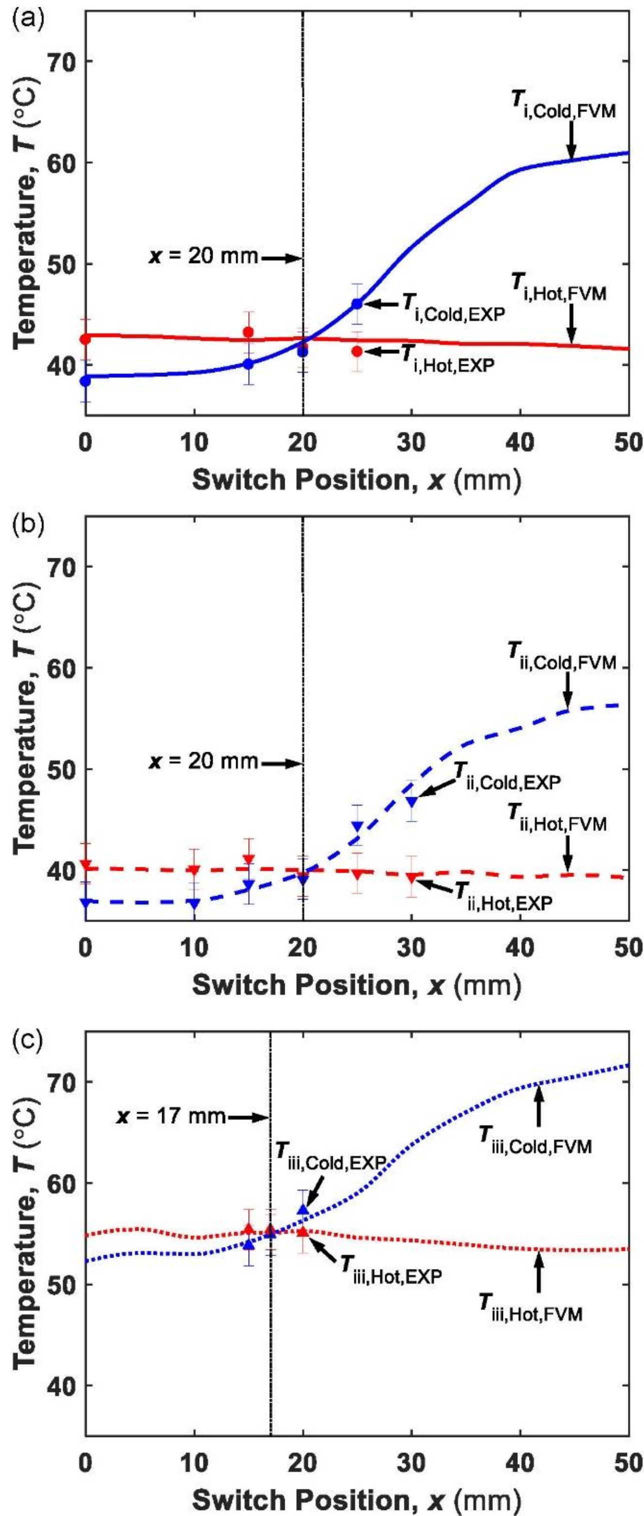

Figure 4.10 Hot SiC device (SiC1, SiC4) and cold SiC device (SiC2, SiC3) temperatures as a function of Cu switch position (*x*) for (a) Table 1, case i, (b) Table 1, case ii, and (c) Table 1, case iii. The lines represent predictions obtained from FVM simulations. The data points represent experimental results. The error in experiment temperature measurement was ± 2.0°C stemming from the calibrated IR thermal measurement.

For future real-world applications such as SiC traction drive systems, much higher powers must be considered. We used our 3D FVM model to predict the heat spreader thermal switch performance when the power converter operates at higher powers. Figure 4.11 shows the predicted temperature results of hot and cold SiC devices as a function of switch position when the power converter operates at 3.5 kW and 5.0 kW. Forced convection of ambient air was applied to cool down the system. The power level of 5.0 kW is the maximum input power our converter can process theoretically, considering the SiC current derating as a function of temperature. Similar trends of hot and cold SiC device temperatures are shown in Fig. 4.11(a) for 3.5 kW and Fig. 4.11(b) for 5.0 kW compared with 2.4 kW in Fig. 4.10(a). However, the thermal switch isothermalization position moves slightly further away from cold SiC devices with 20 mm for 2.4 kW, 21 mm for 3.5 kW, and 21.5 mm for 5.0 kW. The predications indicate that in order to achieve isothermalization and reliability considerations, implementation of our thermal switch is beneficial for power converters working with transient or cycling loads.

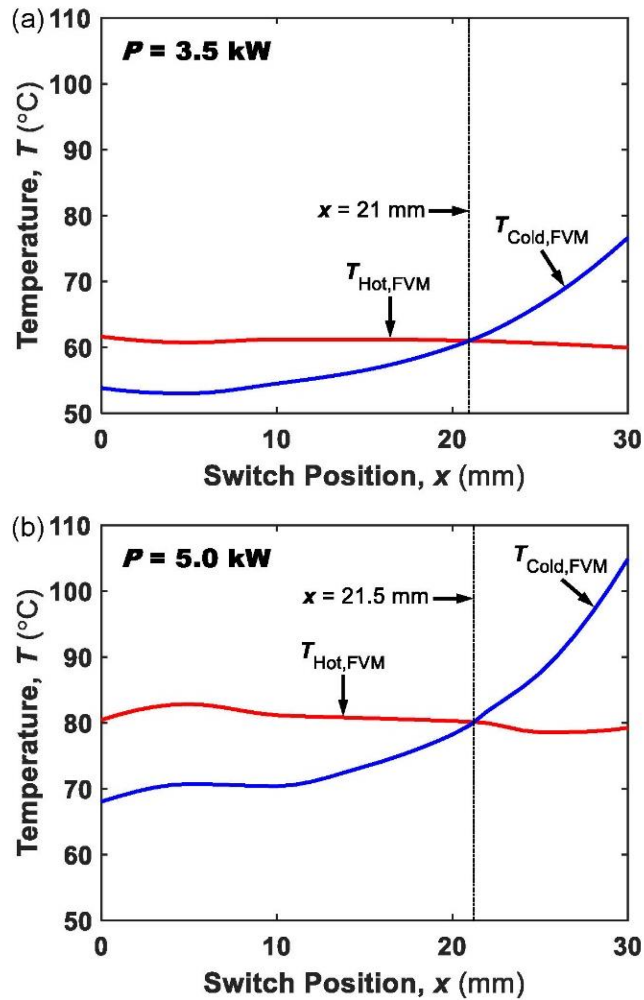

Figure 4.11 Hot SiC device (SiC1, SiC4) and cold SiC device (SiC2, SiC3) temperatures as a function of Cu switch position (x) for converter powers of (a) 3.5 kW, and (b) 5.0 kW, obtained from FVM predictions. The power converter system was cooled by forced convection with air to a back-side Al heat sink.

The successful demonstration studied here shows the advantage of using a thermal switch to reduce the temperature difference between SiC devices when compared to conventional fixed thermal management methods. By realizing device-to-device isothermalization, the thermal switch can be utilized as a tool in converter designs to tune individual component temperatures and achieve greater temperature uniformity, which helps improve system reliability. For example, converter components have optimal operating temperatures governed by set objectives such as reliability and power density [37], [38]. The thermal switch can be an efficient tool to maintain

components working at optimal temperature ranges. For non-planar converters designed by three-dimensional packaging principles [12], overall thermal integration with a thermal switch is able to reduce highly localized temperatures by sharing heat among components and achieve meaningful improvements in reliability while maintaining high power density. In addition, the low-cost SS material, the comprehensive design, and straightforward manufacture and integration make the thermal switch applicable to multiple electronics platforms other than wide band gap power semiconductor power converters. The relatively easy scale up indicates that the thermal switch can be customized for both low and high power applications. Moreover, the integrated thermal switch design demonstrated here is flexible for other shapes or materials.

To actuate the thermal switch for isothermalization of power converters operating in transient applications, actuation approaches need to be considered. A plethora of power dense actuation systems exist, such as electrical, pneumatic, hydraulic, magnetic, or electro-mechanical [39]–[46]. Selection and integration is a key design parameter. For the application scenarios studied in this work, the power converter operated at a static power with a constant power factor during long time durations. Thus, the thermal switch was kept in a static position to achieve device-to-device isothermalization. However, when the converter works in a transient fashion, thermal switch motion is necessary for isothermalization. To respond to changing power levels of the converter, the actuator and the control system must be designed accordingly to keep both precise actuation distance as well as speed. The response speed is important for thermal switch reliability. The co-design of the actuation system with the converter system is required to minimize volume and mass, while maximizing power density and reliability for future thermal switch applications. Despite the significant number of advantages, the thermal switch has some disadvantages such as additional weight to the electronic system and added junction-to-coolant thermal impedance. The resulting

gravimetric power density reduction and heat load increase must be considered as the main tradeoff with lower thermal stresses and greater reliability when designing future electronic systems.

Both simulations and experiments showed that the thermal switch was most effective at manipulating heat transfer when moving close to the heat-dissipating SiC devices. Future designs should focus on changing the thermal conductances near the heat sources. Further work is needed on power density enhancement by reducing the thermal switch mass by removing extra material further away from heat sources. Thus, the specific power density can be enhanced and the energy cost for thermal switch actuation can be reduced. In addition to the steady thermal switch operation shown here, the active heat spreader thermal switch is able to enable isothermalization of SiC devices continuously by moving the thermal switch even if the power converter works in transient conditions. For example, the movement of the thermal switch can be programmed to be periodic when the power converter works under a cyclic loading condition. Active feedback control can be used to modulate the thermal switch position for highly transient and non-periodic drive cycles. Such real-time heat transfer control is currently not possible with nonhomogeneous heat exchangers or modular heat sinks with fixed structures. Furthermore, high-frequency movement of the thermal switch for transient applications may lead to degradation and pump out of the thermal interface material. Future work on reliability of the thermal switch is required to ameliorate these concerns. Lastly, the thermal switch can also be combined with other thermal management methods such as phase change materials to stabilize electronics temperature temporally and enable overall downsizing of the entire thermal management system.

4.5 Conclusions

We studied the isothermalization performance of a solid heat spreader thermal switch to reduce the temperature differences between hot and cold SiC devices of a three-level T-type power

converter. The spreader switch consists of a Cu thermal switch embedded in a SS heat spreader. When the converter was operated at 2.4 kW, each hot SiC device dissipated 4.7 W at a steady case temperature of 43°C, while each cold SiC device dissipated 1.7 W at a case temperature of 38°C. The thermal switch reduced the temperature difference from 5°C to 0°C by improving junction-to-coolant heat transfer from the hot SiC devices and reducing heat transfer from cold SiC devices when the switch was moved to the position of 20 mm. When the converter operated at 2.2 kW, the temperature difference was reduced to 0°C by moving the thermal switch to 20 mm, and with the heat sink cooled by natural convection, a switch position of 17 mm resulted in isothermalization. Detailed 3D FEM and FVM simulations were developed to investigate the converter heat transfer mechanisms. The simulation results were validated by single phase prototype experiments, and were used to analyze key parameters dominating isothermalization performance of the thermal switch. The validated FVM simulations were used to predict thermal switch performance at higher converter powers and represent a good starting point for future electro-thermal co-design. This work shown here not only demonstrates the capability of our thermal switch to isothermalize active components on a particular power converter design, it provided design guidelines for thermal switch configuration and integration for future electronics applications.

4.6 References

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CHAPTER 5: A COMPOSITE PHASE CHANGE MATERIAL THERMAL BUFFER BASED ON POROUS METAL FOAM AND LOW-MELTING-TEMPERATURE METAL ALLOY

5.1 Introduction

The widespread use of active electronic devices and pulsed power applications has created the need for passive thermal management that can handle transient operation while maintaining mass and volume constraints [1]–[5]. Thermal management solutions are typically sized based on peak power loads, which leads to bulky heat transfer equipment, resulting in low gravimetric and volumetric power densities [5], [6]. Instead, a thermal buffer analogous to a thermal accumulator offers passive thermal management capable of absorbing and conducting heat when devices generate peak heat loads. During transient peak power dissipation, the buffer can absorb the heat, conducting it to a smaller thermal dissipation system at a slower rate when peak conditions are not present. The cooling capacity of the thermal buffer is characterized by the geometric average of the energy density (the latent and sensible heat) and the power density (the effective thermal conductivity), by analogy with the thermal effusivity [7]. High cooling capacity thermal buffers can respond to heat spikes quickly and absorb a large amount of heat in a short time, which can protect devices from exceeding allowable temperatures, reduce temperature oscillations, and prolong device lifetimes [3], [8].

Phase change materials (PCMs) present a unique opportunity to develop high cooling capacity thermal buffers by absorbing or releasing latent heat during phase change. Unfortunately, most common PCMs have a relatively low intrinsic thermal conductivity k compared with that of

metals, for example paraffin waxes (≈ 0.2 W/(m·K)), salt hydrates (≈ 0.6 W/(m·K)), or metal alloys (≈ 20 W/(m·K)), which limits the PCM thermal buffer power density and cooling capacity [7], [9], [10]. The cooling capacity can be increased by creating a composite material consisting of a high thermal conductivity matrix which contains a PCM. Past approaches have attempted to disperse nanoparticles or porous conductors having high thermal conductivity directly into PCMs, or develop heat sinks better suited for transient heat loads by surrounding fins with PCM or filling PCM between the gaps of fins [2], [4], [7], [11]–[16]. Although enhancing the effective thermal conductivity via the addition of a higher thermal conductivity matrix improves buffer power density, it comes at a cost of energy density due to the tradeoff with PCM volume fraction. The tradeoff between power and energy density has motivated researchers to seek improved PCM/conductor hybrid structures [2], [7], [11], [17], [18]. Similarly, there is a need for advances in modeling and design methods that enhance understanding and development of thermal buffers. The majority of past work relies on design rules derived from the one-dimensional Neumann-Stephan problem, however there is a need for analysis that accounts for thermal contact resistance, heterogeneous heat transfer pathways, and complicated geometries or boundary conditions. Furthermore, designers of thermal management solutions desire reduced order models and figures of merit such as cooling capacity and time constant.

This paper reports a composite PCM thermal buffer consisting of Field's metal (32.5% Bi, 51% In, 16.5% Sn) infused in a porous copper (Cu) foam matrix. We focused on Field's metal PCM due to its relatively high intrinsic thermal conductivity (≈ 19 W/(m·K)) [19]. Two types of copper foams with average pore diameters of 300 μm and 500 μm were selected due to their ease of scalable manufacturing in addition to high interconnectivity and effective thermal transport capacity. We analyzed six samples for which the independent parameters were thickness (1 mm to

4 mm) and Cu volume fraction (0.05 to 0.2), allowing us to elucidate the roles of thermal conduction, energy storage, and interfacial thermal resistance. To understand our experimental results, we use finite element method (FEM) simulations to validate the measurements and resolve the underlying physical phenomena.

5.2 Concept, fabrication and experiments

Figure 5.1 shows the concept of the composite PCM thermal buffer. The transient heat flux q''_{IN} generated from the heat source (heating block, Fig. 5.1a) is partially stored by the thermal buffer and partially conducted to the heat sink (q''_{OUT}, cooling block, Fig. 5.1a). Heat loss due to natural convection and thermal radiation is negligible compared to the 1D conduction in the solid, and the Biot number is ~ 0.001 across the width of the conductor. To investigate the thermal buffer response to a transient heat load, we implemented a 1D transient heat transfer model using FEM. A pulsed heat flux of 15 W/cm^2 was applied to the initially isothermal assembly through the heating block top boundary, with the cooling block bottom boundary maintained at 58°C. Figure 5.1(b) shows predicted temperature distributions at different times. The PCM melting front (melting point of 60°C) propagates from the hot interface (top Cu-PCM) to the cold interface (bottom Cu-PCM). The thermal buffer stores thermal energy at the rate of $q''_{STORED} = q''_{IN} - q''_{OUT}$ as shown in Fig. 5.1(c). In the phase change region (1.6 s < t < 17.1 s), the high energy storage rate q''_{STORED} results in a stabilized output heat flux q''_{OUT} as well as a slow temperature increase, compared to regions without phase change. During the initial stage of PCM melting (t < 5 s), the energy storage rate increases rapidly with the input heat flux q''_{IN} due to the large latent heat. However, the energy storage rate drops slowly after t = 5 s due to decreasing power density from the increasing thermal resistance between the hot interface and the melting front which moves towards the cold interface. When the PCM is completely melted at t = 17.1 s, the energy storage

rate reduces to a low level due to the small sensible heat capacity (300 J/(kg·K)) compared with the latent heat (34,213 J/kg). The output heat flux q''_{OUT} increases moderately during PCM phase change, increasing sharply after phase change is complete due to elimination of heat absorption. The energy absorption and storage during phase change indicates that the composite PCM thermal buffer is capable of absorbing a large amount of thermal energy from the pulsed heat load with a limited temperature rise.

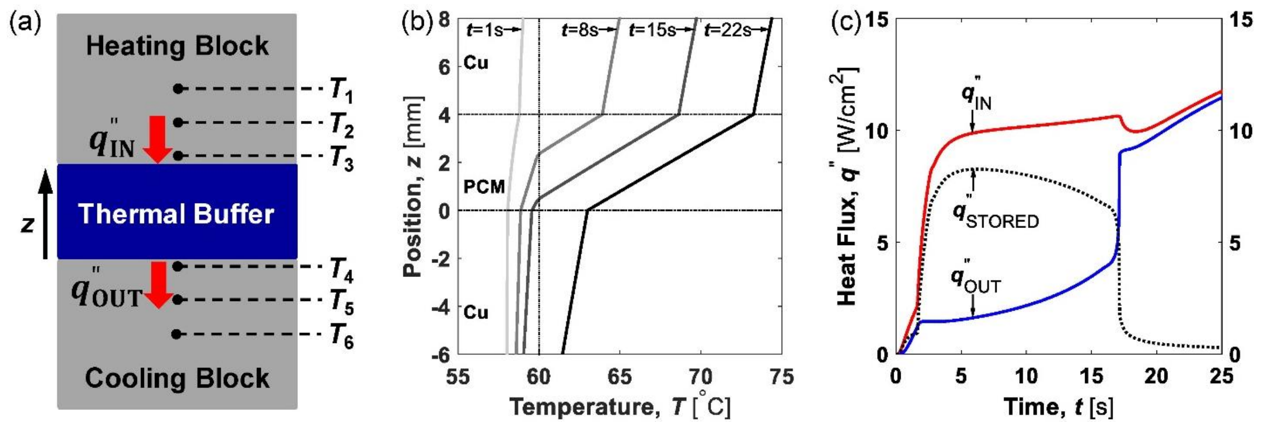

Figure 5.1 (a) Schematic of the PCM thermal buffer concept showing 1D transient heat transfer from a heat source (heating block) to a heat sink (cooling block). (b) Transient temperature profiles obtained with FEM simulations of the PCM thermal buffer. Heating begins at $t = 0$ s and from the top boundary ($z = 24$ mm) of the heating block. The bottom boundary ($z = -20$ mm) of the cooling block was maintained at 58 °C. (c) Simulated heat fluxes into the thermal buffer (q''_{IN}), out from the thermal buffer (q''_{OUT}), and stored in the thermal buffer (q''_{STORED}).

Figure 5.2 shows the composite PCM thermal buffer fabrication process and characterization setup. Field's metal (Roto144F, RotoMetals) was infused into the porous Cu foam (Fig. 2a left, CU-M-01-FM, American Elements) in a tube furnace (TF55035COMA-1, Thermo Scientific), forming the composite PCM (Fig. 5.2a right). Use of a tube furnace flowing H_2/Ar forming gas was necessary to reduce the Field's metal and the Cu foam, enabling effective wetting of the PCM in the porous network. To ensure complete fill of the Cu foam with the Field's metal, the infused Cu foam was cut in multiple locations using a scalpel after infusion, demonstrating no presence of

voids or gas bubbles inside the matrix due to the high wettability [20] of reduced Cu foam with extremely wetting reduced Field's metal. Two pieces of the final composite PCMs were placed side by side, forming the thermal buffer sample used for thermal measurements. To fabricate thermal buffer samples having different thicknesses, two or three Cu samples were stacked together and infused with Field's metal to form a solid interface. Figure 5.2(b) shows the experimental setup used for thermal measurements. The thermal buffer sample was placed between the heating block and the cooling block with extra Field's metal as the thermal interface material. Two cartridge heaters (CSH-101100/120V, OMEGA) connected to a power supply (N5752A, Keysight) generated pulsed heat loads to the heating block. Water coolant was circulated through the cooling block at a flow rate of 3.8 LPM and Reynolds number $Re_D \approx 12,700$, which resulted in a high convective heat transfer coefficient of $h \approx 3500$ W/(m^2·K). The heating and cooling blocks were made of Cu and painted black (1678830, Rust-Oleum) to ensure a high spectrally averaged emissivity (≈ 0.94) for infrared (IR) thermal measurements (A655sc, FLIR). Three thermistors (LSMC700A010KD002, Selco Products) with an accuracy of ± 0.1 °C were inserted into each Cu block to measure temperatures T_1 through T_6. Temperature measurements were recorded using FLIR software for thermal videos and a data acquisition system (USB-1608G, Measurement Computing) for thermistor temperatures at a sample rate of 1 Hz to analyze the thermal performance as a function of time.

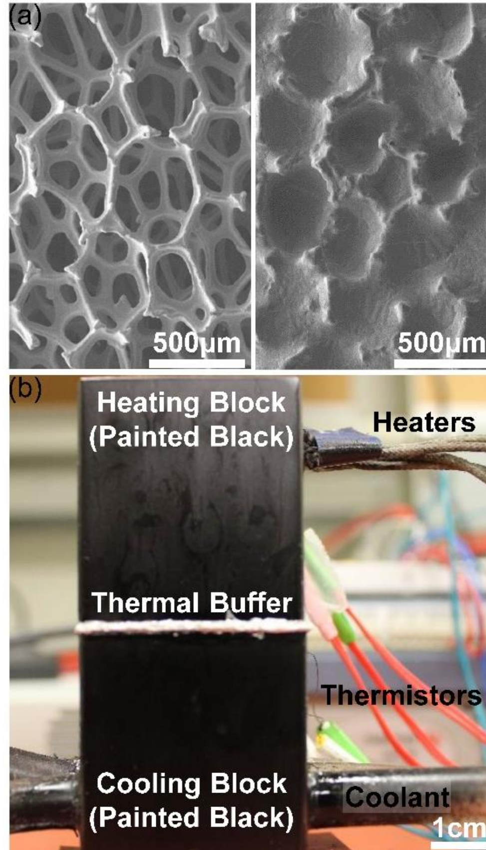

Figure 5.2 (a) Scanning electron microscopy (SEM) images of the porous Cu foam (left), and composite phase change material (right). (b) The experimental setup used to characterize the thermal buffer samples. A schematic of the image is shown in Fig. 5.1(a).

5.3 Experimental results

Figure 5.3 shows exemplary IR thermal measurement results of a 40 mm x 40 mm x 1.45 mm sample with a Cu volume fraction of 0.13. Four thermal images were magnified in Fig. 5.3(a) to show the temperature distributions at t = 0 s, 60 s, 120 s, and 180 s. The heating process began at t = 0 s when a transient high power of 186 W was supplied instead of the background steady-state power of 112 W. The thermal buffer completed phase change from solid to liquid before t = 180 s. The z-axis temperature profile in Fig. 5.3(b) of each image was evaluated by averaging temperatures across the width of the sample. The temperature distributions in the heating and cooling Cu blocks indicated the transient input and output heat transfer rates and were

approximately linear due to the high intrinsic thermal diffusivity of Cu (α = 111 mm^2/s). However, the temperature profiles near the PCM-Cu interfaces were distorted, showing local maxima, due to the interfaces between the thermal buffer and the heating and cooling Cu blocks. The temperature profiles measured from both thermistors and IR images were analyzed to characterize the heat transfer rates and thermal performance.

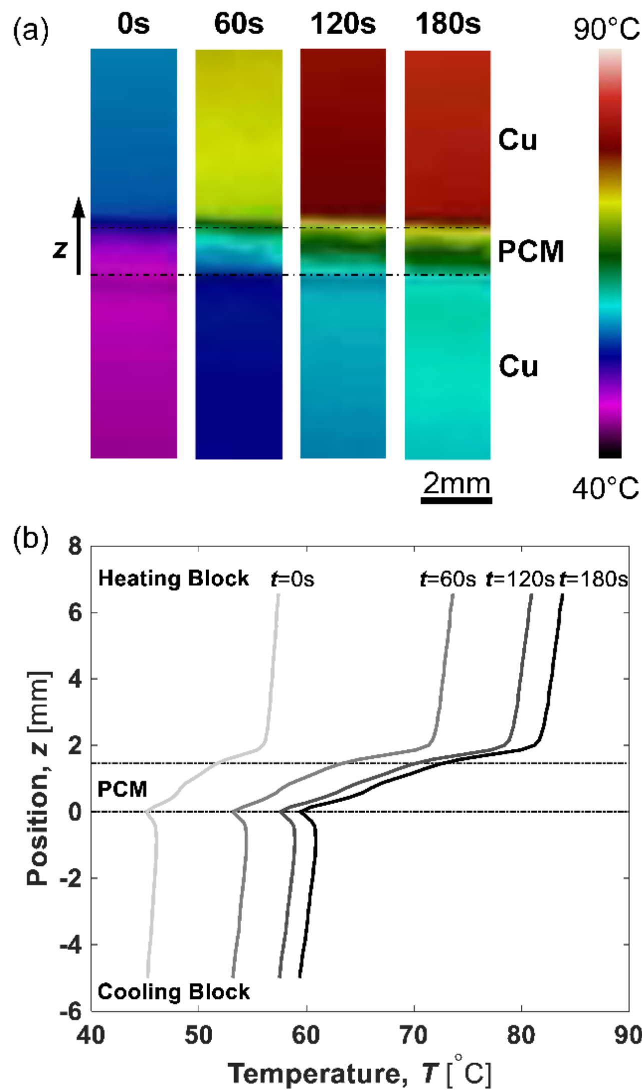

Figure 5.3 (a) IR images of the thermal buffer showing the z-axis temperature distributions at different times. (b) Measured temperature profiles of the PCM thermal buffer, heating block, and cooling block evaluated from thermal images in (a). The error in the IR temperature measurement was estimated to be ± 2 ºC. Initial time (t = 0 s) is the time when the power supply generates a transient high power spike and the heating process begins.

Figure 5.4 shows the thermal performance of the buffer sample as a function of time during successive heating and cooling cycles. Figure 5.4(a) shows heat transfer rates into the thermal buffer Q_{IN}, out from the thermal buffer Q_{OUT}, and supplied power Q_{SUPPLY} as a function of time. Figure 5.4(b) shows the transient temperature T_{HOT} at the hot interface between the thermal buffer and the heating block and the transient temperature T_{COLD} at the cold interface between the thermal buffer and the cooling block. Heat transfer rates Q_{IN} and Q_{OUT} as well as interface temperatures T_{HOT} and T_{COLD} were calculated from thermistor temperature measurements T_1 through T_6 by solving Fourier's law. During heating, the thermal buffer initiated phase change when T_{HOT} exceeded the melting point T_{MELT} ($\approx$ 60 °C) and ended phase change when $T_{COLD} > T_{MELT}$. During cooling, the thermal buffer initiated phase change when $T_{COLD} < T_{MELT}$ and ended phase change when $T_{HOT} < T_{MELT}$. The grey shaded bands in Fig. 5.4 represent the operating regions where phase change occurred. The high energy storage rate during phase change is shown via the greater difference between Q_{IN} and Q_{OUT} in the phase change region when compared to the no phase change region in Fig. 5.4(a). The phase change region and region of no phase change were used to calculate the latent heat and sensible heat from the experimental measurements. Using the conservation of energy, we calculated the sensible and latent energy storage components, and obtained FOMs for the varying composite PCM thermal buffer designs. At steady state, with no heat absorption or release by the thermal buffer, the heat transfer rates Q_{IN} and Q_{OUT} were nearly equal and slightly lower than the supplied power Q_{SUPPLY} due to the heat loss to the ambient. We calculated the effective thermal conductivity from an energy balance on the observed heat transfer rates, and used FEM models to further explore the phase change heat transfer and determine FOMs.

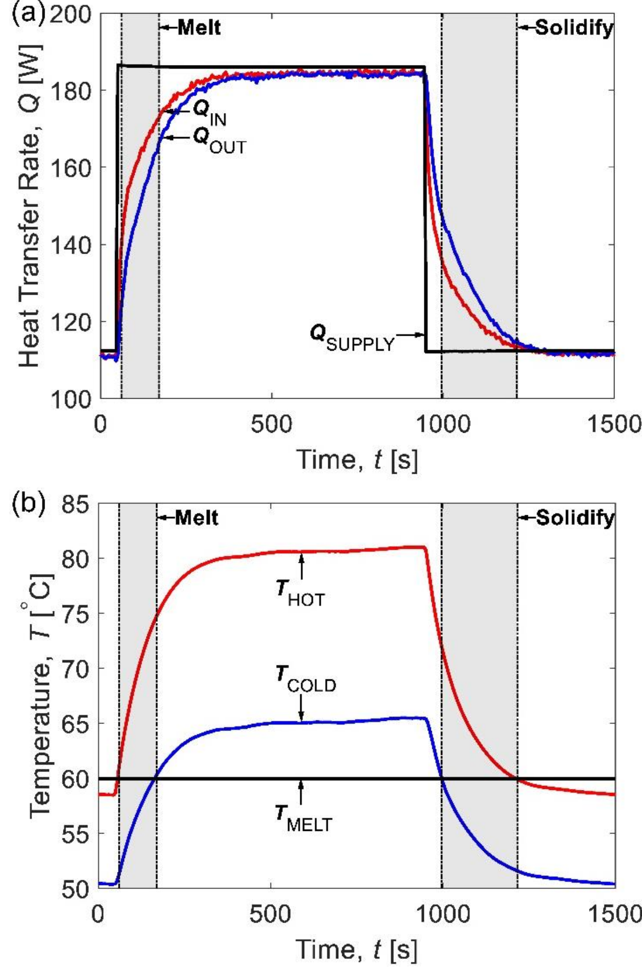

Figure 5.4 Measurements of the PCM thermal buffer performance. (a) Heat transfer rate to the heating block Q_{SUPPLY}, into the thermal buffer Q_{IN}, and out from the thermal buffer Q_{OUT} as a function of time t during successive heating and cooling cycles. (b) Measured hot interface temperature T_{HOT} and the cold interface temperature T_{COLD} versus time t during successive heating and cooling cycles. The grey shaded regions demark when phase change occurs. The errors of Q_{IN} and Q_{OUT} were approximately ± 6 W.

Table 5.1 shows the FOMs and thermophysical properties obtained from experimental results and FEM simulations for all 6 samples. The effective cooling capacity, which represents heat absorption and conduction capability of the thermal buffer was evaluated by [7], [18]:

$$\eta_{eff} = (k_{eff} \cdot E_{eff})^{1/2}, \tag{5.1}$$

where E_{eff} is the effective thermal buffer energy density calculated as $E_{eff} = H_{V,eff} + C_{V,eff} \cdot \Delta T_{MELT}$. $H_{V,eff}$ is the effective latent heat, and $C_{V,eff}$ is the effective volumetric sensible heat capacity, which

represents the energy storage ability of the thermal buffer. The term ΔT_{MELT} is the difference between the PCM melting temperature and the ambient temperature ($\Delta T_{MELT} = T_m - T_{ambient}$). The effective thermal conductivity was calculated by considering measured temperatures at steady state during no phase change:

$$k_{eff} = (d \cdot (q''_{IN} + q''_{OUT}))/(2(T_{HOT} - T_{COLD})). \quad (5.2)$$

To characterize the effective operation time associated with the thermal buffer, we define a time constant τ as the period when the temperature difference $T_{HOT} - T_{COLD}$ across the buffer changes 95% of the total variance during cooling or heating. Buffer properties E_{eff}, $C_{V,eff}$, and $H_{V,eff}$ were evaluated using Q_{IN} and Q_{OUT} and T_1 through T_6 by applying energy conservation within the buffer.

The thermal buffers have cooling capacity η_{eff} as high as 72 kJ/(m^2·K$^{1/2}$·s$^{1/2}$) (Table I), significantly better than 45 kJ/(m^2·K$^{1/2}$·s$^{1/2}$) for aluminum-paraffin or 8 kJ/(m^2·K$^{1/2}$·s$^{1/2}$) for pure paraffin wax buffers [7], [10]. The six samples shows comparable η_{eff} despite the variation in Cu volume fraction and thickness, due to the tradeoff between E_{eff} and k_{eff}. The effective energy density was as high as E_{eff} = 398 MJ/m^3, of which 185-319 MJ/m^3 was latent and 1.9-4.8 MJ/(m^3·K) was sensible. Thermal buffers with lower Cu volume fraction at 0.06 (A1, A2, A3) had higher E_{eff} due to the larger amount of PCM contributing a larger latent heat. The sensible heat accounts for less than 20% of E_{eff} for ΔT_{MELT} = 35 °C. The effective thermal conductivity of our thermal buffer was measured to be k_{eff} = 9.5-14.1 W/(m·K), and was affected by thermal contact resistance at interfaces as well as the volume fraction of the high thermal conductivity Cu. All samples have thermal contact resistance at the top and bottom surface, and some samples have additional internal thermal resistances at the interfaces between adjacent Cu sections. The thermal contact resistance is in the range 33 (mm^2·K)/W to 74 (mm^2·K)/W. The time constant τ is in the range of 124 s to 359 s and depends on thermal buffer thickness. The thermal time constant of

thermal buffers is significantly larger than that of a single PCM-filled pore (~ 0.1 s). Thicker samples have larger time constants due to larger amounts of PCM. Thicker samples also had lower thermal conductance than thin samples, which reduced their ability to absorb power spikes, thus presenting a tradeoff between the time constant and the maximum power. The experimental FOMs differed less than 10% from the FEM simulations (Table 5.1).

Table 5.1 FOMs and thermophysical properties from experiments (EXP) and simulations (FEM) for different samples having distinct thermal buffer dimensions and Cu volume fractions.

Sample	Cu Volume Faction, ϕ_{Cu}	Sample Thickness, d [mm]	Method	η_{eff} [kJ/(m²·K^1/2·s^1/2)]	E_{eff} [MJ/m³]	k_{eff}* [W/(m·K)]	τ [s]	$C_{V,eff}$ [MJ/(m³·K)]	$H_{V,eff}$ [MJ/m³]
A1	0.06	1.25	EXP	62	398	9.5	285	4.8	230
			FEM	59	362	9.5	292	1.9	294
A2	0.06	2.08	EXP	59	334	10.4	238	2.9	234
			FEM	62	366	10.4	238	2.1	293
A3	0.06	3.75	EXP	61	337	10.9	359	4.3	185
			FEM	63	363	10.9	310	2.1	290
B1	0.13	1.45	EXP	72	364	14.1	124	4.1	221
			FEM	70	344	14.1	228	2.1	269
B2	0.13	2.70	EXP	65	386	10.9	297	1.9	319
			FEM	61	343	10.9	304	2.2	267
B3	0.13	3.95	EXP	57	317	10.1	328	2.4	232
			FEM	59	342	10.1	336	2.2	264

* k_{eff} was obtained experimentally and includes the interface contact thermal resistance on both sides of the sample.

5.4 Discussion and conclusions

We analyzed the theoretical thermal conductivity and tradeoffs between the high thermal conductivity of the Cu matrix and the latent heat of the Field's metal by solving the Neumann-Stephan problem with St < 0.5 and expressing η_{eff} as a function of ϕ_{Cu} by the geometric average of k_{eff} and E_{eff} (Eq. 5.1). The effective thermal conductivity of the composite PCM was calculated using the differential effective-medium (DEM) approximation [21], assuming that the Cu matrix

remains connected homogeneously and neglecting thermal contact resistance. The effective energy density E_{eff} was calculated using the weighted linear combination of the thermal properties [7]. The maximum theoretical cooling capacity is 223 kJ/($m^2 \cdot K^{1/2} \cdot s^{1/2}$), about 5X higher than the theoretical value for an Al-wax hybrid heat sink [10] at 45 kJ/($m^2 \cdot K^{1/2} \cdot s^{1/2}$) and 28X higher than paraffin wax [7] at 8 kJ/($m^2 \cdot K^{1/2} \cdot s^{1/2}$). The maximum cooling capacity corresponds to Cu volume fraction of 0.83, effective thermal conductivity of 297 W/(m·K), and energy density 167 MJ/m^3.

Future research on thermal buffers may consider improvements as follows. The thermal contact resistance should be reduced if possible, perhaps by smoothing the surfaces or modifying the fabrication method to achieve good contact between the buffer and adjacent structures [22]. Improved thermal buffers may have anisotropic properties, perhaps by leveraging recent advances in Cu nanowires [23]. To enable the integration of thermal buffers with devices such as power electronics, multi-physics FEM simulations of heat transfer with phase change are required to predict buffer performance as a function of pulsed power rates and duty cycles. These simulations would also allow buffers to be tailored according to critical operating temperatures. Finally, the buffer samples demonstrated here are homogeneous, however spatially varying volume fractions of PCM and metal matrix could enable new performance characteristics [24].

In summary, we demonstrated a composite PCM thermal buffer utilizing a low-melting-point Field's metal PCM infused into a Cu metal foam. Experiments and simulations explored heat transfer for varying thermal buffer thicknesses and Cu volume fractions. And we found good agreement between measured and modeled heat transfer performance. The thermal buffers exhibited high cooling capacities up to 72 kJ/($m^2 \cdot K^{1/2} \cdot s^{1/2}$) and thermal time constants as high as 359 s. Our buffers provide a passive thermal management solution for devices generating pulsed heat loads by reducing the need for dynamic control and size of the thermal dissipation system.

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CHAPTER 6: PHASE CHANGE MATERIAL HEAT SINK FOR TRANSIENT COOLING OF HIGH-POWER DEVICES

6.1 Introduction

Heat transfer in phase change materials (PCMs) and its application to electronics thermal management has been extensively investigated [1]–[7] with research focusing on the dynamics of melting and solidification [8]–[10], development of new materials [11]–[16], and methods to characterize these materials and devices [17]–[19]. Electronics thermal management is a compelling application for PCMs due to their ability to absorb transient heat loads without large temperature or volume changes [20]–[27]. Research on PCM-based thermal management has focused on links between heat transfer fundamentals and cooling performance [28]–[32], as well as novel architectures and cooling concepts [33]–[36].

A thermal buffer is a device that uses PCM to absorb heat and can aid the cooling of electronic devices during transient heat dissipation by stabilizing device temperature and reducing cyclic thermal stresses [37]–[41]. A thermal buffer may offer significant benefits for power electronics, for which temperature-induced stresses account for the majority of failures [42]–[44]. Devices that dissipate heat intermittently, such as cell phones and personal computers, are particularly at risk to these failures [45], [46]. Often, these types of devices are designed with cooling systems that can dissipate heat at peak heating, leading to excessive size and mass of the thermal management system [47]–[49]. PCM based thermal management offers the potential to buffer pulsed heat loads and enhance power density [24], [50].

A key technical limitation for PCM thermal management is the relatively low thermal conductivity of PCMs based on organic materials (< 1 W/(m·K)) or metal alloys (<30 W/(m·K))

[24], [30], [51] compared to conventional heat sinks that are typically made from metals with much higher thermal conductivity. Composite PCM heat sinks, which are heat sinks that incorporate a PCM and at least one other material, can overcome this limitation. One approach for a composite PCM heat sink is to disperse nanoparticles, carbon fibers or graphite flakes, or metal structures into the PCM as a heat conducting matrix [52]–[57]. Heat transfer can also be enhanced by integrating the PCM with extended surfaces of high thermal conductivity material, which provide heat transfer pathways into the PCM [58]–[60]. Recent studies have explored different combinations of materials and structures for composite PCM heat sinks [60]–[63]. Composite PCM heat sinks can also be made using heat pipes or vapor chambers, which can deliver heat at a nearly constant temperature [64]–[66]. While composite PCMs offer increased cooling, they also result in a reduction in the thermal energy that can be stored, because the sensible heat capacity of the matrix is much lower than the latent heat of the PCM. Thus, the design of high-cooling-capacity PCM heat sinks requires a balance between cooling power and energy density.

This paper reports the development of a composite PCM heat sink and its application to circuit board mounted gallium nitride (GaN) devices. The main element of the heat sink is a composite PCM thermal buffer consisting of a eutectic metal alloy having high volumetric latent heat (315 MJ/m^3) and a copper (Cu) foam matrix having high intrinsic thermal conductivity (384 W/(m·K)). We use measurements, modeling, and simulations to investigate transient cooling of top-cooled or bottom-cooled GaN devices.

6.2 Design concept and finite element simulations

Figure 6.1(a) shows the working concept of the PCM heat sink integrated with a top-cooled GaN device mounted on a printed circuit board (PCB). Heat flows from the GaN device through the pyramidal-shape Cu heat spreader and into the thermal buffer. The thermal buffer is a

composite PCM consisting of a Cu foam (volume fraction ϕ_{Cu}) and a Field's metal PCM. Field's metal is a eutectic metal alloy with a melting temperature 60°C and a mass fraction of 32.5% bismuth (Bi), 51% indium (In), and 16.5% tin (Sn). The PCM heat sink is connected to the GaN device through a thermal interface material (TIM). Heat dissipated from the GaN device flows into the heat spreader and the thermal buffer, melting the PCM of the thermal buffer at 60°C. Excess heat flows through the fins and is dissipated by convective cooling.

We built a 3-D finite element method (FEM) model to simulate heat transfer and phase change in the PCM composite heat sink using COMSOL Multiphysics 5.4.0. Here we describe the FEM model and results for one device to illustrate the concept of operation and provide additional simulation results later. At the bottom of the heat sink is a 3 mm-tall pyramidal spreader with 9 x 7.5 mm^2 base and 16 x 16 mm^2 top. The middle section consists of the composite PCM thermal buffer with Cu volume fraction $\phi_{Cu} = 0.04$, thickness d = 5.6 mm, and width w = 15 mm. The composite PCM thermal buffer is contained in an enclosure with side walls of thickness 0.5 mm. At the top is a second heat spreader and a conventional array of Cu fins. The fin array is 14 mm wide, has a 2.6 mm thick base, and has 100 cylindrical fins per square inch that are 1.2 mm thick and 4 mm long. The fin array is cooled by air at temperature T_{air} = 22°C with a spatially averaged forced convection heat transfer coefficient of 85 W/(m^2·K) based on air flow velocity of 0.84 m/s delivered by a fan. Other surfaces of the integrated assembly undergo natural convection with ambient air. The thermal contact resistance R_{TIM} between GaN and spreader is 1.8 K/W, which is equivalent to a 440 μm thick thermal interface material with conductivity of 1 W/(m·K) [67], [68].

Heat transfer and phase change in the thermal buffer are modeled as follows. The thermal properties of the thermal buffer region are 24.9 W/(m·K) for effective thermal conductivity, 7922 kg/m^3 for effective density, 290 J//(kg·K) for effective heat capacity, and 38 kJ/kg for effective

latent heat using effective medium theory [28]. The thermal properties are considered isotropic and constant with the temperature variation except for the phase change region. Solid-liquid phase change of the composite PCM is modelled using the apparent heat capacity method, in which the heat capacity is a function of temperature during a small temperature range near the melting temperature. We set the phase change temperature range between 57.5 °C and 62.5 °C. This approach to modeling the phase change was validated in our previous publication. [28]. The volume expansion during phase change is negligibly small. Natural convection in the liquid phase was neglected because the Rayleigh number within the thermal buffer is very low ($Ra_d \leq 397$), which is further suppressed by the porous Cu structure [68]. The initial temperature of the assembly is in equilibrium with surrounding air at 22°C, and the GaN device generates heat at Q = 5 W starting from initial time t = 0 s.

Figure 6.1(b) shows FEM predictions of the temperature distribution in the device at different times (t = 150s, 200s and 250s). The white curve is the melting temperature contour and approximately indicates the boundary between liquid and solid phases, which propagates from the heat spreader to the top of thermal buffer. The temperature profile in the PCB is relatively constant compared with the PCM heat sink, which indicates quasi-steady thermal transport in the PCB.

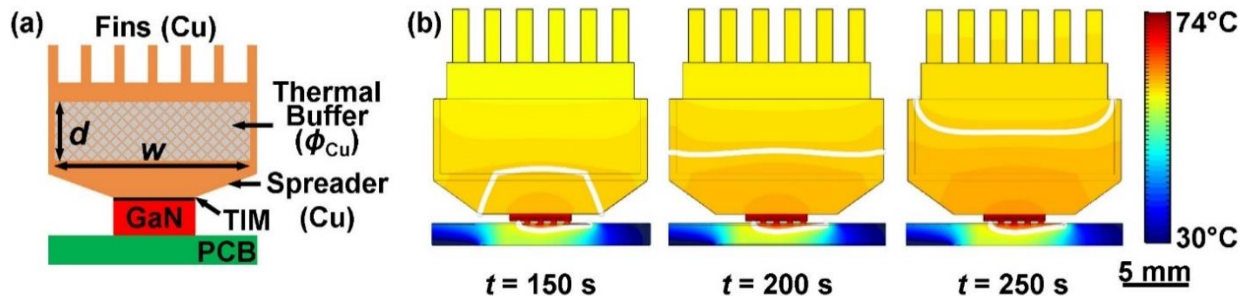

Figure 6.1 (a) Schematic of the PCM heat sink integrated with a top-cooled GaN device mounted on a printed circuit board (PCB). The PCM heat sink consists of the thermal spreader (inverted pyramid), the thermal buffer, and the fin array. (b) Temperature predictions showing the cross-sectional temperature distributions at different times. The white curves represent the melting temperature (T_{melt} = 60°C).

Figure 6.2 shows FEM predictions for the PCM heat sink and two reference designs that allow us to evaluate the PCM heat sink by comparison. The first reference design is a solid Cu heat sink with the same geometry as the PCM heat sink and made from solid Cu ($\phi_{Cu} = 1$). The second reference is the fin array from the top of the PCM heat sink that is fixed directly to the GaN device without the pyramidal heat spreader or the thermal buffer. Figure 6.2(a) shows the GaN junction temperatures (T_j) as a function of time for the three devices. The PCM heat sink maintains the device junction temperature at ≈74°C for 250 s, while the other devices have a smooth temperature rise until they reach steady state. The solid Cu reference has a large heat capacitance compared to the fin array, which causes a slower temperature change for the solid Cu reference. Figure 6.2(b) shows the predicted heat transfer rates from the GaN device to the top heat sink (Q_t) and bottom PCB (Q_b). The heat transfer rate from the top of the device Q_t was calculated at the interface between the GaN device and heat sink. The bottom heat transfer rate Q_b was calculated from an energy balance by $Q = Q_t + Q_b$. The PCM heat sink shows a nearly constant heat transfer rate during phase change, owing to the large latent heat capacitance of the thermal buffer. The FEM predictions show that the PCM heat sink can absorb a large amount of heat and delay the device junction temperature rise compared with the solid Cu heat sink or the fin array.

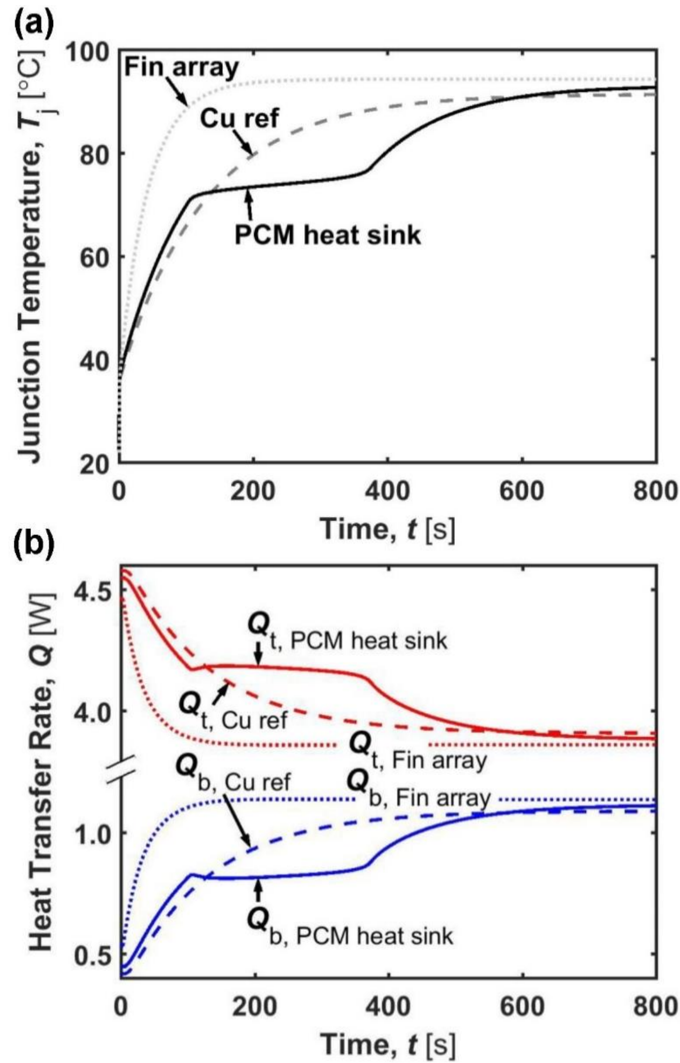

Figure 6.2 Performance predictions of the PCM heat sink, solid Cu reference (Cu ref), and fin array. Finite element predictions of (a) GaN junction temperatures and (b) heat transfer rates to the top (Q_t) and bottom (Q_b) of the GaN device as a function of time. The PCM heat sink has relatively flat heat transfer rates during phase change, maintaining a relatively constant junction temperature.

6.3 Experiments

We fabricated five thermal buffer samples for the PCM heat sinks using methods described in our previous work [28]. Briefly, using a porous Cu foam (CU- M-01-FM, American Elements) inserted into a heat spreader case machined from solid Cu, we infused Field's metal (Roto144F, RotoMetals) in a tube furnace (TF55035A-1, Thermo Scientific) at 320°C for 3 hours. A commercial Cu fin array (SLF-1, ENZOTECH) was mounted on the thermal buffer and fused

together in a similar way. During infusion of PCM and Cu, forming gas (5% H_2 in Ar) was flowed through the tube furnace continuously to reduce the Cu foam and Field's metal and avoid oxidation, enabling effective wetting and complete filling of the PCM in the porous Cu structure [28].

Dimensions and properties of the thermal buffer portions of the PCM heat sinks are summarized in Table 6.1. The thermal buffers ranged in thickness from 2.8 mm to 6.0 mm and Cu volume fraction ranged from 0.04 to 0.09. The effective thermal conductivity k_{eff} of the composite PCM was calculated using the differential-effective-medium (DEM) approximation which was validated by FEM simulations of the porous Cu foam filled with PCM in our previous work [28]. The effective sensible heat capacity is c_{eff}. The effective latent heat H_{eff} is the enthalpy change of the PCM during phase change. Both c_{eff} and H_{eff} were calculated using the mass weighted combination of Cu and Field's metal thermal properties. The total effective energy density E_{eff} is the energy the thermal buffer can store and is defined as a sum of latent and sensible heats with a temperature change from 22°C to the melting point (60°C). The effective cooling capacity is the capability of heat absorption and was calculated by analogy with effusivity as $\eta_{eff} = (k_{eff} \cdot E_{eff})^{1/2}$ [28], [69].

Table 6.1 Thermophysical properties of the thermal buffer samples at room temperature.

Sample	d [mm]	ϕ_{Cu}	k_{eff} [W/(m·K)]	c_{eff} [J/(kg·K)]	H_{eff} [kJ/kg]	E_{eff} [MJ/m^3]	η_{eff} [kJ/(m^2·K$^{1/2}$·s$^{1/2}$)]
A1	2.8	0.039	24.7	289	38	390	98
A2	5.6	0.043	25.4	290	38	389	99
A3	4.2	0.041	25.0	290	38	389	99
B1	2.9	0.090	33.6	295	36	376	112
B2	6.0	0.093	34.1	295	36	375	113

Figure 6.3 shows photographs of two PCM heat sinks integrated with either top-cooled or bottom-cooled GaN devices. The top-cooled device was an EPC 2034 (Efficient Power Conversion) having a surface area of 2.6 mm x 4.6 mm and connected to the heat sink with a TIM (Arctic Silver 5, Arctic Silver) having a thermal conductivity of 8.9 W/(m·K) reported by the manufacturer. The bottom-cooled device was a GS66508B (GaN Systems Inc.) having a surface area of 7.0 mm x 8.4 mm was soldered on the front-side PCB with Cu thermal vias. The PCM heat sink was mounted on the back of the PCB connecting to the back-side thermal vias using the same TIM. The heat sink was cooled by forced convection with ambient air (22°C) delivered by a fan with a maximum flow rate of 1.89×10^{-4} m^3/s and velocity of 0.84 m/s. A voltage source (E3620A, Agilent) provided a gate voltage of 5 V for top-cooled GaN device and 6 V for bottom-cooled GaN device. Operating in the conduction mode, the GaN device was powered by a power supply (6033A, Agilent) generating a pulsed current. The device current was controlled to be constant by controlling the DC power supply. A digital multimeter (34410A, Agilent) measured the drain-to-source voltage. To determine the junction temperature, calibration with the ON-state resistance was conducted with temperature interval of 5°C [70]–[73]. The GaN junction temperatures were obtained by mapping the drain-to-source resistance acquired by Ohm's law to the junction temperature.

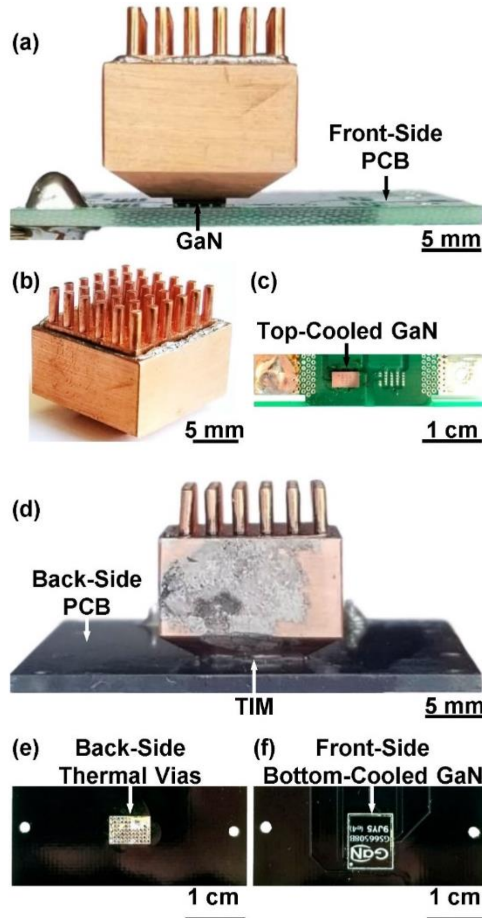

Figure 6.3 Photographs of two PCM heat sink integrated devices. (a) Top-cooled GaN device with PCM heat sink; (b) Isometric view of the PCM heat sink showing the fin array on top; and (c) Top view showing the GaN device mounted on the PCB with PCM heat sink removed. (d) Bottom-cooled device; (e) Backside view of the Cu thermal vias in the PCB prior to PCM heat sink integration; (f) Front side of the PCB showing the bottom-cooled GaN device.

In order to understand the heat transfer within the PCB, we first measured the baseline heat transfer characteristics of the PCB without a heat sink to obtain the bottom thermal resistance (R_b) from the junction temperature to the ambient air through the device bottom. Figure 6.4 shows experiment schematics, the corresponding thermal resistance circuits, and results for the top-cooled and bottom-cooled GaN architectures. The top part of the GaN mounted PCB was insulated with fiberglass ($k_{fiberglass}$ = 0.04 W/(m·K)) as shown in the schematic (Fig. 6.4). The PCB bottom side experienced natural convection to ambient air at 22°C. Powered at different currents, the GaN

device dissipated different heat losses Q. When the system reached steady state, the current and voltage signals were recorded to obtain the junction temperature T_j and calculate Q. The bottom thermal resistance R_b was calculated as $R_b = (T_j - T_{air}) / Q$. The experiment and simulation results show that R_b decreased as a function of Q for $Q < 0.2$ W and then remained constant at $Q > 0.2$ W due to efficient heat spreading in the PCB [74]. When device power was greater than 0.2 W, the bottom thermal resistance was R_b = 65 K/W for top-cooled GaN devices and R_b = 150 K/W for bottom-cooled GaN devices.

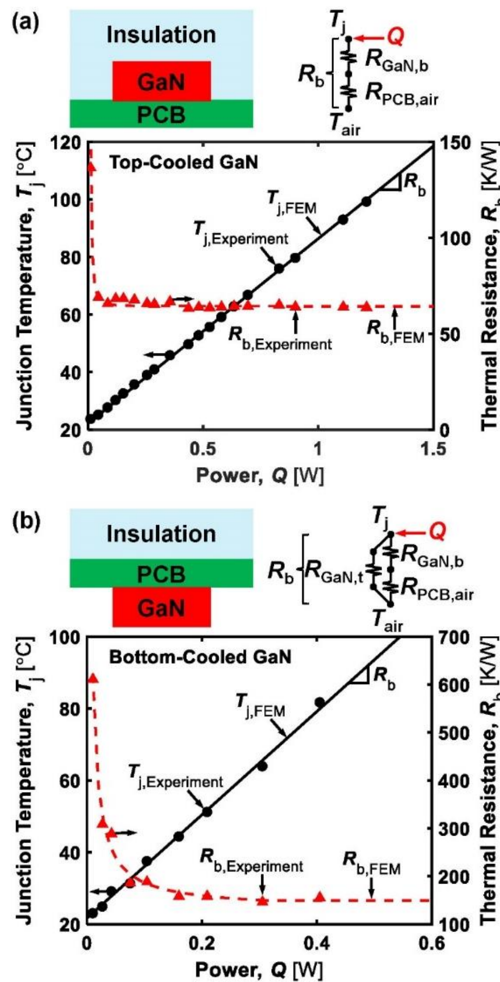

Figure 6.4 Schematic, thermal resistance circuit, and experimental results used to determine the bottom side thermal resistance R_b for (a) top-cooled GaN devices and (b) bottom-cooled GaN devices mounted on the PCB. Error bars not shown because they are smaller than the plotted data points.

We conducted experiments with five PCM heat sinks each designed with different thermal buffers for transient cooling of GaN electronics and compared experiments with FEM simulations. The FEM simulations solved for the junction temperature T_j, top-side heat transfer rate $Q_{t,FEM}$, and bottom-side heat transfer rate $Q_{b,FEM}$, where the heat source input was taken from the measured heat dissipation Q. Figure 6.5 shows the experiment and simulation results when the PCM heat sink with thermal buffer sample A2 (Table 6.1) was integrated with the top-cooled GaN device operating at a transient current of 22.0 A. The junction temperature increases rapidly until phase change begins, slows during PCM phase change, and then increases after phase change is complete. The heat dissipation Q increased with time because the drain-to-source electrical resistance Ω_{DS} increased with junction temperature. The bottom-side heat transfer rate $Q_{b,exp}$ was calculated as $(T_j - T_{air}) / R_b$. The top-side heat transfer rate was calculated using an energy balance $Q_{t,exp} = Q - Q_{b,exp}$. The difference between experimental result $Q_{t,exp}$ and simulation result $Q_{t,FEM}$ was less than 5%. The good agreement between experiments and simulations demonstrates the validity of the FEM simulations and allows us to use these simulations for further analysis.

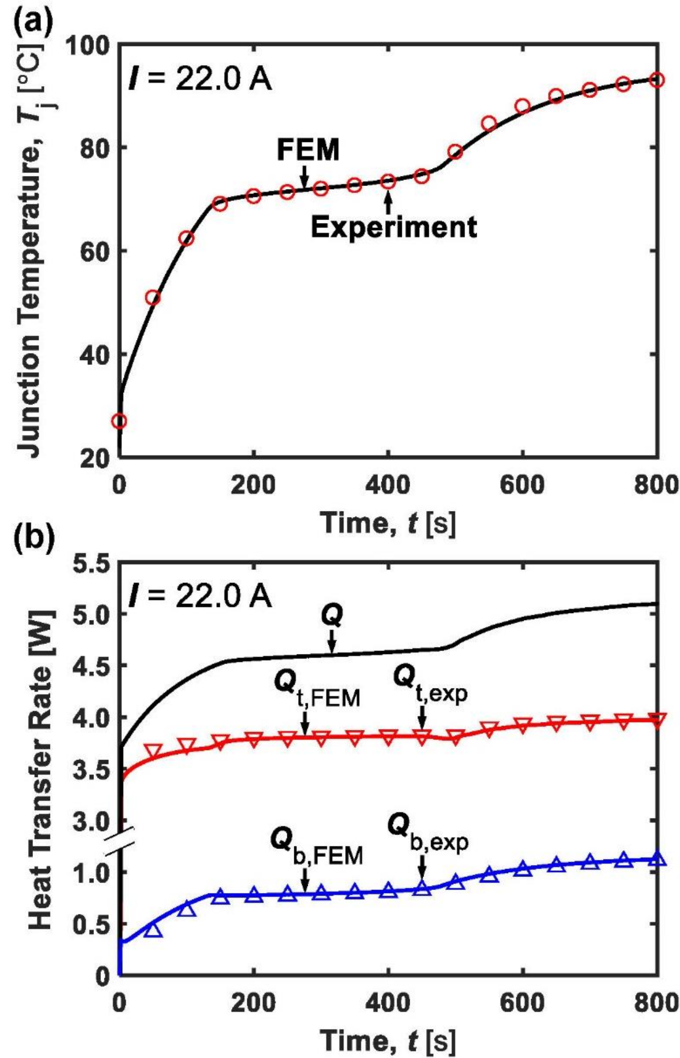

Figure 6.5 Measurements (symbols) and FEM predictions (lines). (a) GaN junction temperature (T_j) as a function of time for the top-cooled GaN and heat sink with thermal buffer A2 and powered at I = 22.0 A. (b) Device heat dissipation (Q), top-side heat transfer (Q_t), and bottom-side heat transfer (Q_b) as a function of time for the top-cooled GaN device powered at I = 22.0 A. The error in the experimental junction temperature measurement was ± 1.1°C and is smaller than the size of the data points.

6.4 Thermal resistance-capacitance circuit modeling

We developed a thermal resistance-capacitance (RC) circuit model to rapidly analyze different designs. Figure 6.6(a) shows the thermal RC circuit model for transient operation of the top-cooled GaN device. The transient heat load Q is generated at the GaN junction node and transferred to the top side (Q_t) and bottom side (Q_b), which results in the junction temperature T_j.

The thermal resistance of the middle portion of the device R_m is the sum of the GaN junction-to-case-top thermal resistance ($R_{GaN,t}$), and the TIM thermal resistance (R_{TIM}). The thermal resistance R_t is the sum of the spreader thermal resistance ($R_{Spreader}$), the thermal buffer resistance (R_{TB}), and the conductive and convective thermal resistance of the fin array ($R_{Fins,air}$). The thermal resistance R_b is the sum of the GaN junction-to-case-bottom thermal resistance ($R_{GaN,b}$) and the PCB conductive and air convective thermal resistance ($R_{PCB,air}$) shown in Fig. 6.4(a). A thermal capacitance C represents the sum of Cu spreader, thermal buffer and fin array thermal capacitances, which is ~5X larger than the PCB thermal capacitance (neglected in our circuit). Consisting of both sensible and latent heat capacity, C as a function of temperature increases by >10X during phase change due to the large enthalpy change around the melting temperature. A similar thermal RC circuit model was built for the cooling architecture of bottom-cooled GaN devices (Fig. 6.6b). Compared with the top-cooled GaN RC circuit model shown in Fig. 6.6(a), R_m was modified to include the thermal resistance of the Cu vias (R_{Vias}) between the bottom of the GaN and TIM as well as the junction-to-bottom-case thermal resistance ($R_{GaN,b}$).

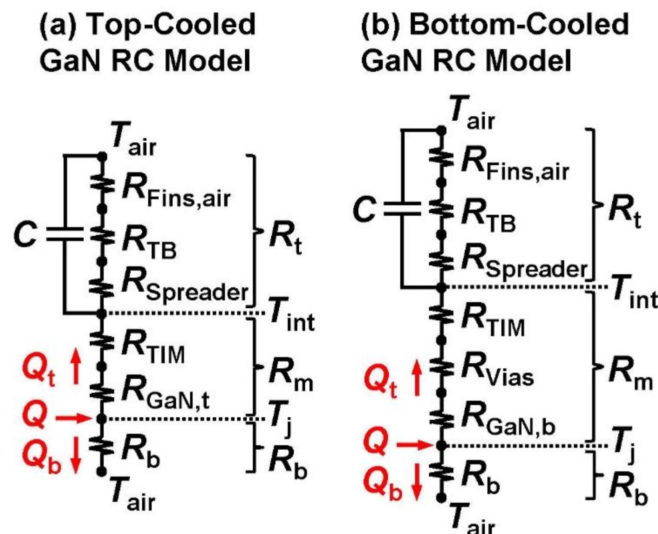

Figure 6.6 Reduced-order thermal resistance-capacitance (RC) circuits of the integrated PCM heat sink with (a) top-cooled and (b) bottom-cooled GaN devices.

Table 6.2 summarizes the key model parameters used in our analysis including thermal resistances, thermal capacitances, and latent heats. These parameters were obtained from experiments conducted on the top-cooled GaN device at $I = 22.0$ A cooled by the five PCM heat sinks, the top-cooled GaN device at $I = 22.5$ A cooled by heat sink with thermal buffer A2, and bottom-cooled GaN device at $I = 7.5$ A cooled by heat sink with thermal buffer A2. The bottom-side thermal resistance R_b was obtained from the previous experiments (Fig. 6.4). The thermal resistance from the GaN junction to the heat sink was calculated as $R_m = (T_j - T_{int}) / Q_t$, when T_{int} reached 60°C with melting onset. And the Cu spreader thermal resistance is negligible by $R_{Spreader} \approx d_{Spreader} / (k_{Cu} \cdot w^2) < 0.1$ K/W. The top side heat transfer was calculated as $Q_t = Q - (T_j - T_{air}) / R_b$. At steady state, the top side thermal resistance is $R_t = [(T_j - T_{air}) / Q_t] - R_m$. The thermal buffer thermal resistance is $R_{TB} = d / (k_{eff} \cdot w^2)$, which assumes constant thermal properties estimated using effective-medium theory. Sensible heat capacitances of the heat spreader ($C_{Spreader}$), fin array (C_{Fins}), and thermal buffer (C_{TB}) were calculated by multiplying the individual heat capacities by mass. The latent heat L_{TB} is the total latent energy of the Field's metal PCM. For heat transfer without phase change, the total thermal capacitance $C = C_{Spreader} + C_{TB} + C_{Fins}$. During phase change, $C = C_{Spreader} + C_{TB} + C_{Fins} + (L_{TB} / \Delta T)$, where $\Delta T = (R_{TB} / R_t) \cdot (T_{int} - T_{air})$ is the temperature change of the thermal buffer during phase change. The value of R_b is 4X that of R_t for top-cooled GaN devices and 10X that of R_t for bottom-cooled GaN devices, and consequently most of the heat flows through the top side. The forced convection thermal resistance $R_{Fins,air} = R_t - R_{TB} - R_{Spreader}$ dominates the top-side heat transfer due to the geometry of the air-cooled fin array. The thermal resistance R_m is dominated by the TIM contact resistance (~ 1 K/W) for top-cooled GaN devices and Cu thermal vias through the PCB (~ 5 K/W) for bottom-cooled GaN devices.

Mounting (soldering) variability between the different top-cooled GaN devices resulted in slightly different values of R_m and R_t.

Table 6.2 RC model parameters for different devices and measurements.

GaN	I [A]	Sample	R_b [K/W]	R_m [K/W]	R_t [K/W]	R_{TB} [K/W]	$C_{Spreader}$ [J/K]	C_{Fins} [J/K]	C_{TB} [J/K]	L_{TB} [J]
Top-Cooled	22.0	A1	65	1.6	15.3	0.5	2.3	2.3	1.5	190.8
		A2		2.3	15.5	1.0	2.6	2.4	2.7	380.0
		A3		2.0	15.5	0.7	2.4	2.4	2.1	285.7
		B1		1.8	13.9	0.4	2.3	2.3	1.6	187.1
		B2		2.0	15.3	0.8	2.5	2.4	3.2	386.0
Top-Cooled	22.5	A2	65	2.6	16.4	1.0	2.6	2.4	2.7	380.0
Bottom-Cooled	7.5	A2	150	6.6	16.0	1.0	2.6	2.4	2.7	380.0

Using the defined RC circuit model parameters, we calculated the device junction temperature as a function of time. The top-side heat transfer rate including heat storage rate and conduction rate is calculated as:

$$Q_t = C \cdot \mathrm{d}(T_{int} - T_{air}) / \mathrm{d}t + (T_{int} - T_{air}) / R_t \,. \tag{6.1}$$

The interface temperature between heat spreader and thermal buffer is calculated by:

$$T_{int} = T_j - (R_m \cdot Q_t) \,. \tag{6.2}$$

The junction temperature is calculated as:

$$T_j = T_{air} + (R_b \cdot Q_b) \,. \tag{6.3}$$

According to energy conservation:

$$Q = Q_t + Q_b \,. \tag{6.4}$$

With C, T_{air}, R_t, R_m, and R_b as known parameters, Q obtained from experiments as an input heat loss, and initial condition $T_{int} = T_j = T_{air}$, the four coupled equations (Eqns. 6.1-6.4) are solved to find T_j, T_{int}, Q_t, and Q_b. Numerical solutions were found using an implicit (backward) Euler

method. To account for the dependence of C on phase change, we express C as a function of temperature as follows:

$$C = C_{\mathrm{Spreader}} + C_{\mathrm{TB}} + C_{\mathrm{Fins}} \text{, while } T_{\mathrm{int}} < T_{\mathrm{m}} \text{,}$$
$$C = C_{\mathrm{Spreader}} + C_{\mathrm{TB}} + C_{\mathrm{Fins}} + (L_{\mathrm{TB}} / \Delta T) \text{, while } T_{\mathrm{m}} \leq T_{\mathrm{int}} < T_{\mathrm{m}} + (Q_{\mathrm{t}} \cdot R_{\mathrm{TB}}) \text{,} \tag{6.5}$$
$$C = C_{\mathrm{Spreader}} + C_{\mathrm{TB}} + C_{\mathrm{Fins}} \text{, while } T_{\mathrm{int}} \geq T_{\mathrm{m}} + (Q_{\mathrm{t}} \cdot R_{\mathrm{TB}}) \text{.}$$

During melting, the energy stored in thermal buffer must meet the criterion: $\int[Q_{\mathrm{t}} - (T_{\mathrm{int}} - T_{\mathrm{air}}) / R_{\mathrm{t}}]\, \mathrm{d}t < L_{\mathrm{TB}} + (C \cdot \Delta T)$, until the melting process is complete when: $\int[Q_{\mathrm{t}} - (T_{\mathrm{int}} - T_{\mathrm{air}}) / R_{\mathrm{t}}]\, \mathrm{d}t = L_{\mathrm{TB}} + (C \cdot \Delta T)$. The calculations for the solid Cu reference are performed in the same method as defined above, except that C is a constant sensible heat capacitance of the Cu reference, and R_{t} is the Cu reference thermal resistance.

Figure 6.7 shows example RC solutions with experimental results for PCM heat sink with thermal buffer A2 (Table 6.1) integrated with a top-cooled GaN device powered at $I = 22.5$ A and $I = 22.0$ A. The junction temperatures calculated from the RC circuit model agree very well with the measured values, showing a maximum difference of less than 5%, which helps to measure the validity of the RC model. The RC model accurately predicts the temperature plateau which corresponds to material phase change as well. When the GaN device was powered at $I = 22.0$ A and $I = 22.5$ A, the phase change times were 321 s and 288 s obtained from experiments, with the difference of 4 s from 325 s and 292 s predicted by the RC model. The RC circuit model was simplified based on the FEM model and experiments. The lumped thermal capacitance C of the heat sink thermal buffer was assumed since the Biot number (Bi = 0.002) was less than 0.01. The equivalent thermal capacitance of latent heat was calculated as $L_{\mathrm{TB}} / \Delta T$ which is similar to the apparent heat capacity method used for the finite element simulations. The bottom thermal

resistance R_b was relatively constant at $Q > 0.2$ W due to the quasi-steady heat transfer and efficient heat spreading through the PCB.

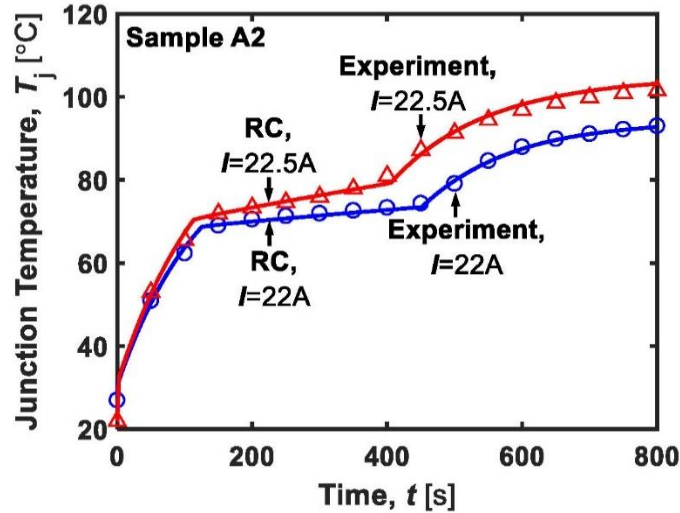

Figure 6.7 GaN device junction temperature (T_j) as a function of time (t) obtained using the RC model (lines) and experimental measurements (points) for PCM heat sink with thermal buffer A2. The top-cooled GaN device is powered at $I = 22.5$ A or $I = 22.0$ A. The error in the experimental junction temperature measurement was ± 1.1°C and is smaller than the symbol size.

6.5 Results and discussion

Figure 6.8 shows experimental results and RC circuit model solutions of GaN junction temperatures as a function of time. Figure 6.8(a) shows results of PCM heat sinks with thermal buffers A1 and B2 integrated separately with top-cooled GaN devices powered at $I = 22.0$ A. Solid Cu heat sinks having identical dimensions as PCM heat sinks were also investigated and are labeled as Cu reference. The thickest (6.0 mm) thermal buffer sample B2 (Table 6.1) with a higher $\phi_{Cu} = 0.09$ had a longer melting time when compared to the thinnest thermal buffer A1 (Table 6.1) due to higher latent heat. Compared with the Cu references, the PCM heat sinks reduced the temperature increase of the junction temperatures during phase change. Figure 6.8(b) shows the top-cooled GaN device junction temperatures for PCM heat sink with thermal buffer A2 and the

Cu reference powered at different currents ranging from I = 22.0 A to 23.5 A. At higher currents, the junction temperature increased more rapidly, with the thermal buffer initiating phase change earlier and having a shorter melting time. Figure 6.8(c) shows the bottom-cooled GaN device junction temperatures of PCM heat sink with thermal buffer A2 (Table 6.1) and the Cu reference powered at different currents ranging from I = 7.5 A to 8.0 A. Compared with the top-cooled GaN devices, the bottom-cooled GaN devices operated at lower currents due to the higher drain-to-source electrical resistance Ω_{DS}. For example, operating at 4.6 W total loss, the top-cooled GaN device had a current of I = 22.0 A while the bottom-cooled GaN device had a current of I = 8.0 A. With the same device operating power, the PCM heat sink integrated with the top-cooled GaN had a longer melting time due to smaller overall thermal resistances compared with the bottom-cooled GaN. Overall, compared with the Cu references, the PCM heat sinks delayed the increase in GaN junction temperatures by absorbing heat during melting.

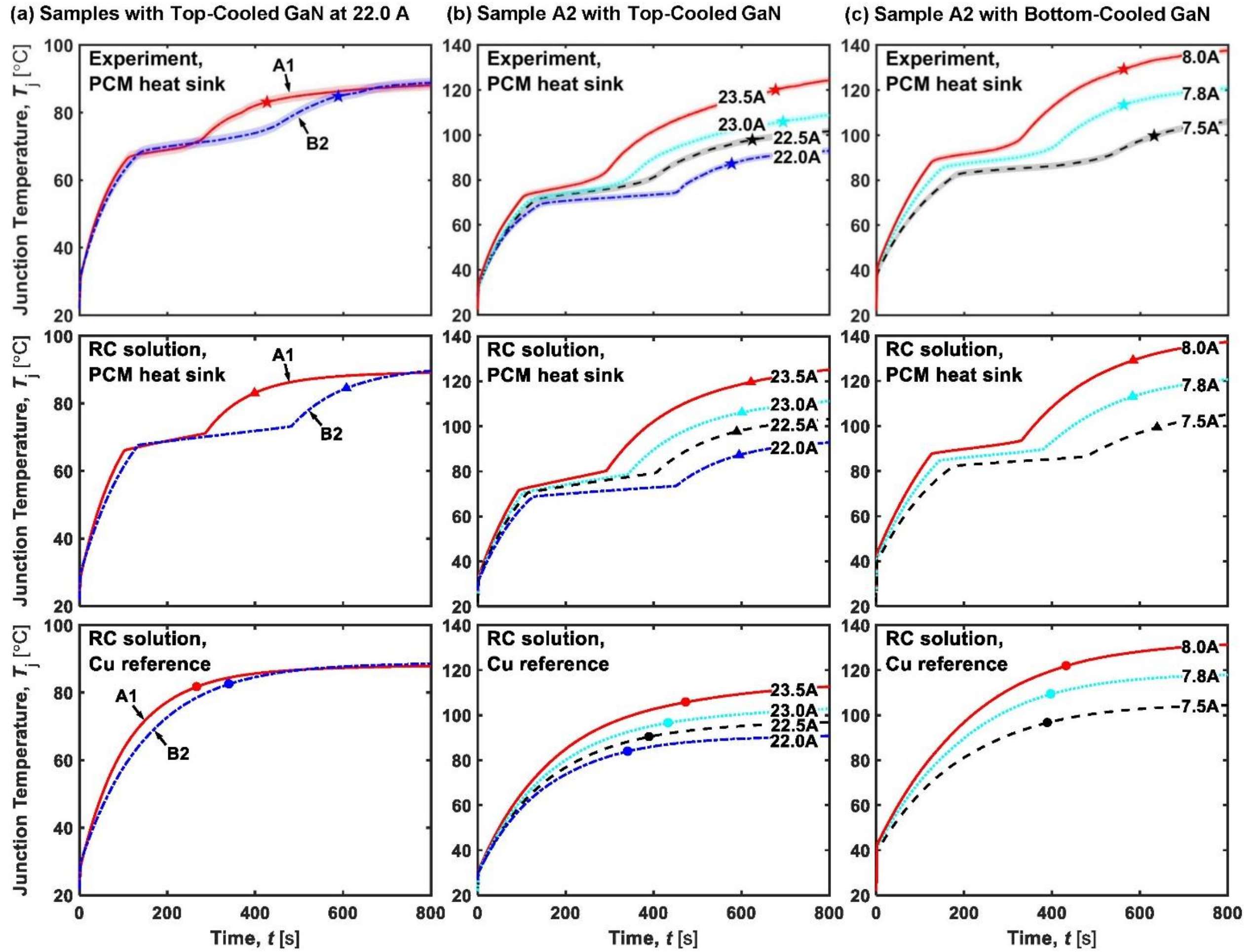

Figure 6.8 GaN device junction temperatures as a function of time obtained from experiments and the RC model for the PCM heat sink and the solid Cu reference for: (a) Samples A1 or B2 integrated with top-cooled GaN devices powered at 22.0 A; (b) Sample A2 integrated with a top-cooled GaN device; and (c) Sample A2 integrated with a bottom-cooled GaN device. The markers represent the characteristic times (τ). The shaded bands along the experimental curves indicate the junction temperature measurement error of ± 1.1 °C.

A key performance metric is the period during which the thermal buffer can absorb heat. We define a characteristic time τ as the time when the junction temperature increased by 90% of the total steady-state GaN junction temperature change ($T_{j,SS} - T_{air}$). Figure 6.8 shows τ as demarcations by solid data point symbols. Heat sinks with larger thermal capacitances had longer characteristic times, and the PCM heat sinks outperform the Cu reference designs. Since GaN devices are less efficient at higher T_j and heat loss Q increases with T_j, this resulted in higher $T_{j,SS}$

and longer τ as a function of current level I for Cu references shown in Fig. 6.8(b, c). However, the τ for PCM heat sinks changed differently as a function of I, since the melting time τ_{melt} decreases as a function of Q and I.

We use the RC circuit model to compare our PCM heat sink with the Cu fin array. Before modeling the transient thermal performance, we performed experiments to characterize the thermal resistance of the fin array. Figure 6.9(a) shows junction temperatures of the top-cooled GaN device as a function of time when integrated with the fin array and powered at different currents. Figure 6.9(b) shows predictions for the bottom-cooled GaN device using the fin array powered at different currents. The junction temperatures of the fin array cooled devices increase more rapidly with shorter characteristic times compared with the Cu reference heat sinks due to smaller thermal capacitances. Compared with our PCM heat sink, the fin array has a faster temperature rise in a shorter time, which is expected.

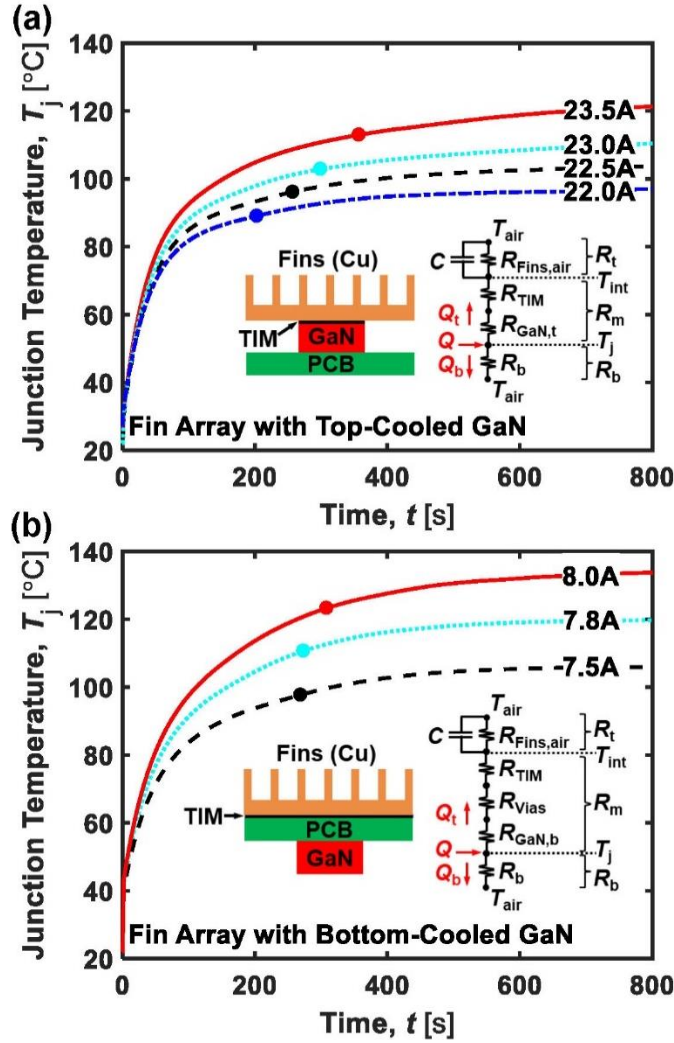

Figure 6.9 (a) Top-cooled and (b) bottom-cooled GaN device junction temperatures as a function of time obtained using the RC circuit model for Cu fin array. Insets: RC circuits and schematics of the fin array mounting orientations (not to scale).

Table 6.3 summarizes the characteristic times obtained from experiments (τ_{exp}), and RC circuit model solutions for the corresponding PCM heat sinks (τ_{RC}), the Cu reference (τ_{ref}), and for the fin array (τ_{Fins}). For PCM heat sinks with different thermal buffer samples integrated with top-cooled GaN devices powered at I = 22.0 A, the heat dissipation Q was approximately 4.6 W with a heat flux of 38 W/cm^2 at the GaN surface. The characteristic times τ_{exp} and τ_{RC} were longer when the thermal buffer was thicker and had a larger latent heat L_{TB}. Compared with the Cu reference and the fin array, τ_{exp} and τ_{RC} of the PCM heat sinks were approximately 60% to 70% higher than

τ_{ref} and 90 to 200% higher than τ_{Fins}, depending on the thermal buffer sample. When the top-cooled GaN device was powered at a current of I = 22.5 A, the heat dissipation Q was approximately 4.9 W with a heat flux of 41 W/cm^2. The PCM heat sink with thermal buffer A2 had characteristic times τ_{exp} and τ_{RC} 60% higher than τ_{ref} and 150% higher than τ_{Fins}. For the bottom-cooled GaN device powered with I = 7.5 A, the heat dissipation Q was approximately 3.9 W with a heat flux of 6.6 W/cm^2. Characteristic times τ_{exp} and τ_{RC} of PCM heat sink with thermal buffer A2 were 62% higher than τ_{ref} and 135% higher than τ_{Fins}. The measured characteristic time τ_{exp} and the characteristic time τ_{RC} found from the RC circuit model agree well, showing a maximum difference of 7%. The characteristic times represent the time scale of our thermal buffers to absorb transient heat loads, demonstrating a significantly improved transient cooling performance when compared to conventional fin array.

Table 6.3 Time constants for thermal buffer samples.

GaN	I [A]	Sample	τ_{exp} [s]	τ_{RC} [s]	τ_{ref} [s]	τ_{Fins} [s]
Top-Cooled	22.0	A1	426	399	267	203
		A2	578	595	341	
		A3	483	491	307	
		B1	361	385	226	
		B2	589	608	340	
Top-Cooled	22.5	A2	625	589	390	257
Bottom-Cooled	7.5	A2	632	639	390	269

The FEM simulations and RC circuit models are in good agreement with measurements. While the FEM simulations provide the transient temperature distributions, the RC circuit model enables rapid predictions and design iterations. The RC circuit models are approximately 4 orders of magnitude faster to compute when compared to the highest resolution FEM simulations.

The properties of the thermal buffer is a key issue for both the FEM and RC circuit modeling. The effective medium theory was valid for our simulations because the length scales in micrometer of both pores and skeletons of the copper foam were small and the Fourier number (Fo) was large enough for uniform thermal diffusion between Cu and PCM [75], [76]. However, for PCMs embedded in porous structures, the effective medium theory with a one-temperature energy equation cannot predict phase change accurately if either natural convection in the liquid phase is important, or if a large difference in thermal properties between the PCM and the matrix induce large temperature gradients at small Fo. If either of these conditions becomes relevant, then direct simulations of porous structures or two-temperature methods with interstitial convection are required [77]–[79].

6.6 Conclusions

This paper investigates heat transfer in a PCM heat sink and its cooling performance when integrated with circuit board mounted GaN devices. We developed a composite PCM thermal buffer with high cooling capacity up to 113 $kJ/(m^2 \cdot K^{1/2} \cdot s^{1/2})$ and integrated this thermal buffer with a heat sink. Five PCM heat sink devices were fabricated and tested with working GaN devices that dissipated heat flux as high as 50 W/cm^2. We demonstrated the PCM heat sink operation with two different cooling architectures for top-side cooling and bottom-side cooling, and showed that the PCM heat sink devices reduced the device junction temperature by 10-20 °C during phase change compared to a solid Cu reference heat sink. Three-dimensional FEM simulations and reduced-order thermal RC circuit analyses were used to analyze transient cooling performance and guide heat sink design. The FEM and thermal RC circuit methodologies developed here can facilitate future optimizations of PCM heat sinks for other electronics applications.

6.7 References

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CHAPTER 7: CONCLUSIONS AND RECOMMENDATIONS

7.1 Conclusions

This dissertation reports fundamentals and applications of thermal switches and thermal buffers to control heat transfer in electronic packaging for improved power density and reliability. We first propose a millimeter-scale liquid metal droplet thermal switch capable of modulating between high and low thermal conductances actively by moving the droplet with electrochemical actuation. The findings show that the channel thickness and the channel medium of a reducing liquid or vapor affect the switching ratio by changing thermal resistances in ON and OFF states. The thick channel has a thick droplet and a large thermal resistance in ON state. The thick channel facilitates natural convection in the liquid and vapor, which reduces the OFF state thermal resistance and the switching ratio. The relatively low thermal conductivity of the vapor enhances the switching ratio from 15.6 of a liquid filled channel to 71.3 at a heat flux of 10 W/cm^2 by increasing the OFF state thermal resistance. The interfacial thermal resistance between the droplet and calorimeter blocks increases the ON state thermal resistance and decreases the switching ratio. This work provides an insight in the fundamentals of millimeter-scale liquid metal thermal switches and demonstrates measurements of switching ratios.

We integrate the liquid metal thermal switch with one or two GaN transistors mounted on a printed circuit board. Moved to different positions, the thermal switch can control heat transfer from different pathways at a series of GaN power levels by measuring device temperatures and calculating heat transfer rates. To investigate the heat transfer physics, a 1D reduced thermal resistance circuit in conjunction with 3D FEM simulations is developed, showing good agreement with experimental results. The thermal switch can control a heat flux of 11 W/cm^2 in the ON state

or 4 W/cm^2 in the OFF state, when the GaN transistor dissipates 15 W/cm^2 at 51 °C or 95 °C. The thermal switch can control heat transfer from two GaN devices and eliminate the temperature mismatch from >10 °C to 0 by precisely moving the droplet position.

We develop a solid Cu thermal switch for isothermalization of a 3 kW DC/AC power converter consisting of SiC devices. Hot SiC devices dissipate more heat than cold SiC devices due to higher operating frequency and voltage loads. The spatially inhomogeneous heat dissipation and the induced temperature gradients are challenges for system reliability due to thermomechanical stresses. Integrated with the Cu thermal switch, hot SiCs have more efficient heat transfer through the high thermal conductivity Cu than cold SiCs have through the air channel in a heat spreader. By moving the thermal switch from cold SiCs to hot SiCs, the temperature difference between SiC devices is reduced to zero. For different converter operation powers from 2.2 kW to 5 kW, isothermalization requires the switch to move from 20 mm to 21.5 mm demonstrated by experiments and finite volume method simulations. This work provides design guidelines for thermal switch configuration and integration with power electronics application.

To provide temporal control of heat transfer and reduce temperature swings of power electronics during transient operation, we investigate phase change materials and develop a high-power thermal buffer. Composite PCMs consisting of a high-latent-heat PCM embedded in a high-thermal-conductivity matrix are desirable for thermally buffering pulsed heat loads by rapid absorption and release of thermal energy at a constant temperature. A Field's metal PCM melting at 60 °C is infused into a Cu foam with high intrinsic thermal conductivity, forming a composite PCM with enhanced thermal conductivity [≈ 40 W/(m·K)] and high volumetric latent heat (≈ 300 MJ/m^3). The effective medium theory is used to evaluate the thermophysical properties of the composite PCM, validated by experiments and FEM simulations. The composite PCM thermal

buffers with Cu volume fractions from 0.05 to 0.2 have high cooling capacities up to 72 $kJ/(m^2 \cdot K^{1/2} \cdot s^{1/2})$. The cooling capacity of the thermal buffer is 9X higher than pure paraffin waxes and 2X higher than aluminum-paraffin composites. The high cooling capacity is promising for passive thermal management of electronic devices generating pulsed heat losses to suppress temperature swings and avoid overdesign of cooling systems.

Finally, we integrate the composite PCM thermal buffer with a Cu spreader and a fin array heat sink for transient cooling of power electronics. The PCM heat sink is integrated with a circuit board mounted GaN device. Both top-cooled and bottom-cooled GaN devices are studied for different cooling architectures. The device junction temperature is reduced by 10-20 °C during phase change by the PCM heat sink compared with a conventional Cu heat sink. The cooling time constant is increased up to 2X, depending on the device power which is as high as 6 W. A FEM model and a reduced-order thermal RC circuit model are developed to validate experiments and guide the design of future PCM heat sinks.

7.2 Recommendations for future work

The research described in this thesis can be extended in three main directions for future work. First, thermal switches and thermal buffers with better FOMs can be developed by using advanced materials or novel structure designs. Other characteristics of thermal devices like response speed and energy storage remain to be explored for more comprehensive evaluation. Second, circuit of thermal devices including thermal switches, thermal buffers, thermal diodes, and thermal resistors and capacitors can be developed for more complicated and smarter thermal control. Third, spatial and temporal control of heat transfer is desired not only for power electronics cooling but also for many other applications, such as temperature control in space and biomedical technologies and sustainable energy generation in concentrating solar power plants.

7.2.1 High contrast thermal switch with precise rapid switching and thermal response

Although our thermal switch has high switching ratios and capability to achieve isothermalization between power electronics devices, the dynamic behavior was not studied. Several actuation methods have been proposed for several types of thermal switches, including electrochemical actuation, electrowetting, light-triggered, and magnetic approaches [1]–[6]. However, control of the liquid metal droplet speed and position could be improved. The switching time $\tau_{switch} \sim L/U$ depends on the actuation method, the switch design and materials. The thermal response time $\tau_{thermal} \sim R \cdot C$ depends on thermophysical properties of materials and the thermal contact resistance. Some applications require quick response of a thermal switch, which means τ_{switch} and $\tau_{thermal}$ should be considered and designed to be as small as possible.

Our thermal switches can be used for active control of transient heat transfer. By moving the thermal switch close to or away from the heat source, the source temperature can be tuned as a function of time. Moreover, continuous switching of thermal conductance instead of binary ON/OFF states may be preferable in applications requiring to cycle between three or more temperatures [7], [8].

7.2.2 Thermal circuits with thermal switches and thermal buffers

Thermal circuits based on thermal switches, thermal buffers, thermal diodes and regulators may offer new capability for adaptive and optimal heat rejection. For example, previous research demonstrated that thermal switches and diodes are able to reduce power consumption and enhance cooling performance by modulating heat transfer during solid-state refrigeration cycles [9]. However, the key challenge is how to select thermal components and tune parameters of each component for optimal performance of thermal circuits in a given application. Computational methods like reduced-order models of thermal circuits or FEM simulations could provide

approaches for rapid iterations and optimization. For example, a software design tool based on the 3D thermal resistance-capacitance network was developed to optimize PCMs in electronics packaging [10]. Future research can utilize computational resources to study nonlinear mechanisms of thermal circuits and explore potential applications.

7.2.3 Thermal energy storage and research opportunities of phase change materials

PCMs have been used in thermal energy storage and energy conversion systems for decades [11]–[14]. Composite PCM materials enable thermal storage with both high heat capacity and high cooling power – a combination of physical properties that was not previously possible [15], [16]. These advancements introduce fundamental technical issues including understanding of relevant heat transfer mechanisms, materials properties, and modeling of multi-physics behavior required to translate fundamental mechanisms into new applications. Heat transfer fundamentals of PCMs including non-equilibrium phase change, boundary effects, solidification, the role of microstructures, and non-Fourier thermal conduction at high heat fluxes and short time scales are important to design PCMs for enhanced thermal performance. An understanding of PCM physical properties at the atomic or molecular levels and their relationship with composition and microstructure remains to be revealed. Finally, cost, durability and reliability issues remain challenges to elevate PCM lab research into applications.

7.3 References

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