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Memory Module Design for High-Temperature Applications in SiC CMOS Technology

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy in Engineering with a Concentration in Electrical Engineering

by

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Abstract

The wide bandgap (WBG) characteristics of SiC play a significant and disruptive role in the power electronics industry. The same characteristics make this material a viable choice for high-temperature electronics systems. Leveraging the high-temperature capability of SiC is crucial to automotive, space exploration, aerospace, deep well drilling, and gas turbines. A significant issue with the high-temperature operation is the exponential increase in leakage current. The lower intrinsic carrier concentration of SiC (10^{-9} cm^{-3}) compared to Si (10^{10} cm^{-3}) leads to lower leakage over temperature. Several researchers have demonstrated analog and digital circuits designed in SiC. However, a memory module is required to realize a complete electronic system in SiC that bridges the gap between data processing and data storage. Designing memory that can process massive amounts of data in harsh environments while consuming low power opens doors for future electronics.

A novel static random-access memory (SRAM) cell is designed and implemented in a SiC 1 µm triple well CMOS process for high-temperature applications in this work. The prevalent issues encountered during SiC fabrication and the uncertainties in device performance led to 6T SRAM cell design modifications that enable adaptability to the worst and the best cases. However, design trade-offs are made in the design size, the number of transistors, number of I/Os, and the cell's power consumption. The novel SRAM cell design mitigates the effect of poor p-type contacts after the device fabrication by controlling the cell's drive strength via an additional pull-up network. The design also includes two parallel access transistors and separate wordlines that control both access transistors. This individual control enables post-fabrication tunability in the cell ratio (CR) and the pull-up (PR) ratio of the cell. It also allows tuning the access transistors' effective width during a data read operation, and a data write operation, independently. Along with the SRAM cell

design, the conventional latch-based sense amplifier is also designed in the SiC CMOS process to realize the monolithic memory IC modules.

The SRAM cell performance is evaluated on the basis of static noise margin (SNM), write SNM (WSNM), read SNM (RSNM), leakage current, and read access time over a wide temperature range (25ºC to 500ºC) on three uniquely processed wafers. The noise margins measured on Wafer #2 show a lower leakage current of ~500 nA at 500ºC with the supply voltage of 10 V. The SNM of 6.07 V is measured at 500ºC with a 10 V of power supply. The read access time at 400ºC is ~7.5 μs at a supply voltage of 10 V.

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Dedication

I dedicate this work to my daughter Manal and my rest of the family. Thank you so much. It could not have happened without you all.

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1 Introduction

1.1 Background and Motivation

Electronic systems capable of withstanding high temperature environments are in high demand in various applications such as logging-while-drilling (LWD) systems and embedded electronics which are in the core of gas turbine engine controls. Designing memory that can process massive amounts of data in harsh environments while consuming low power opens doors for next generation, smart, high temperature electronic systems.

Decades of research and development of wide bandgap (WBG) semiconductors has paved the way for implementation of these materials in high temperature, high frequency, high voltage, and radiation hardened applications. Silicon carbide (SiC) and gallium nitride (GaN) are the two most commonly used and produced WBG semiconductor materials. SiC has emerged as the most mature of the WBG semiconductors with the release of commercial 6H-SiC bulk substrates in 1991 and 4H-SiC substrates in 1994 [1].

Leveraging the high temperature capabilities of SiC ICs is crucial to automotive, aerospace, deep well drilling, and wireless telemetry systems [2]. Although building blocks for extreme environment data acquisition have been demonstrated in [3], a memory module is necessary to enable data storage and therefore a more robust electronic system. Therefore, this work highlights the design challenges of SiC CMOS monolithic ICs and the need of having a memory module that can operate at temperatures above 400°C along with its peripheral circuitry. The evolving nature of the SiC CMOS process and the resulting process variation encourages the design of a new memory cell. The Static Random Access Memory (SRAM) cell is designed by using a triple-well, 1 µm single poly, single metal (1P1M) SiC CMOS process fabricated at Fraunhofer IISB in

Erlangen, Germany. In addition, various sense amplifier architectures are designed and will be the focus of this work.

1.2 Literature Review

The most prominent issue in conventional silicon based high temperature electronics is leakage current, which increases exponentially with temperature. SOI technology has been widely used for high temperature operation due to its lower leakage capability gained from the reduced junction area beneath the transistor as a result of the buried oxide layer, however, the maximum operating temperatures are limited to 300°C due to the same leakage problems. Therefore, high temperature electronics present a unique challenge to the design of CMOS logic and memory circuits. SRAM modules are the most important component in the modern high-performance System-on-Chips (SoCs) designed to operate at high temperatures. There is a strong market demand for such products. In 1996, Honeywell introduced the High Temperature Electronics products for commercial use, mainly targeting aerospace applications. They presented the world's first commercially available 32 kB SRAM module to operate at 225°C. In competition with Honeywell, Texas Instruments (TI) also launched a commercial product line for High Reliability Components for Extreme Environments which was initially targeting oil-drilling applications. Later on, the products advanced with the radiation hardness capabilities and also was used for space exploration applications. TI introduced the world's first 32 MB Flash memory module that can operate at 210°C. Commercially available products encourages the researchers to stretch the operating temperature range beyond 250°C. In [4], R. Cojbasic and Y. Leblebici showed the reliable operation for 6T SRAM up to 260°C. They realized 6T SRAM in 0.18 µm SOI CMOS process and proposed a D-Latch type 6T-SRAM cell. The proposed SRAM showed better operating frequency than the conventional SRAM over temperature with the tradeoff being the

extra transistors in the D-Latch. In 2013, Kim, et al. presented an 8T SRAM module operating at 300°C [5]. They used a 1 µm SOI CMOS process to realize the design. Due to the high leakage currents at high temperatures, read operations failed because the bitlines could not sustain the charging voltage. In order to mitigate this, they added a sensing margin enhancement technique in the sense amplifiers by having a current source node on the bitlines. In [6] and [7], temperature-aware low-voltage SRAM is demonstrated at 25°C to 300°C and realized in a 1 µm SOI CMOS process. Similar to [5], an increase in sensing margin is implemented with the dynamic control source node on the bitlines. Gogl, et al., [8] presented a 1kbit EEPROM to operate at 250°C, with the significance of this work being the integration of a floating gate process in the SOI technology, which the author called SIMOX technology. Tai-Hua, et al., [9] explained the leakage problems in a bulk silicon process and demonstrated a radiation-hardened SRAM design that can operate at 225°C. The article published from this thesis [10] is the first implementation of SiC CMOS-based 6T SRAM cell, the cell operated at 500°C. However, the fabrication challenges in SiC CMOS, especially low resistive ohmic contacts, have deteriorated the cell's performance. Table 1 compares the operating temperatures, maximum frequency, and total power consumption performances of the aforementioned high-temperature memory literature.

Table 1. Si/SOI SRAM Cell Performance Comparison at High Temperatures

	Honeywell	**TI**	**[4]**	**[4]**	**[5]**	**[6]**	**[7]**	**[8]**	**[9]**	**[10]**
Process			SOI CMOS 0.18µm	SOI CMOS 0.18µm	1µm SOI	1µm SOI	1µm SOI	1.6µm SIMOX Technology	Bulk Si 0.13µm	SiC CMOS 1µm
SRAM Topology		Flash	D-Latch	6T	8T	8T	8T	EEPROM	6T	6T
Tj_{MAX}	**225°C**	**210°C**	**275°C**	**260°C**	**300°C**	**300°C**	**300°C**	**250°C**	**200°C**	**300°C**
f_{MAX}	20MHz	12MHz	10MHz	5MHz	1MHz	1MHz	15MHz	-	-	~1kHz
P_{TOT}	100mW		410mW	1120 mW	1mW	35.5 mW	25.56 mW	-	-	4.52 mW @ 400°C
Size			-	-	560µm^2	-		1200µm^2		10792µm^2
								Additional steps needed		

The conventional silicon CMOS process is prone to leakage currents at high temperatures. Leakage currents are comprised of diode diffusion currents, which are proportional to intrinsic carrier concentration (n_i). The thermally generated carrier concentration exceeds that due to dopants, and control of carriers in the device is lost at sufficiently high temperatures. In Si, the bandgap decreases by 0.083 eV between 25°C and 300°C. These factors combine to raise the intrinsic carrier concentration in Si to approximately 10^{16} cm^{-3} at 300°C [9]. Due to these considerations, high bandgap semiconductors such as SiC and GaN are more suited for high-temperature operations. Research into SiC began with power electronics being the central focus. Power semiconductors made from silicon carbide are capable of withstanding voltages up to 10 times higher than ordinary silicon. This, in turn, has several implications for system complexity and cost. The proliferation of electronic products throughout the world means many types of devices that must operate in variable or harsh conditions, such as higher temperatures. Silicon carbide shines here as well. There has been a growing demand for high-temperature capable circuitry in a multitude of other applications.

SiC is particularly suited for these applications due to its intrinsic carrier concentration being approximately 19 orders of magnitude lower than silicon [11]. This leads to SiC transistors having lower leakage current than bulk silicon devices and is paramount in achieving high-temperature operation. The maximum operating temperatures of bulk silicon and silicon-on-insulator (SOI) are limited to approximately 150°C and 300°C, respectively [12], [13]. With SiC ICs, this boundary is extended to over 500°C for both analog and digital circuitry [14]-[16]. So far, there is no work other than [10] reported on the CMOS memory design and realization of SiC memory. However, literature surveys showed considerable interest in the SiC-based memory designs. An article published in Physics World in November 1992 [17] shows the promises that

SiC memory can make for the future of electronics. Another article [18] describes the potential of SiC as a memory material by demonstrating the electronically-passivated SiC-SiO_2 interface. In 2018, Elgebra, et al., [19] validates the potential of developing memory architectures in the 4H-SiC BJT process. The authors proposed the 4T-SRAM cell and characterized the design with the help of models. Thus, no actual memory cell has been fabricated.

In [20], SiC JFET process technology with two levels of metal interconnects demonstrated a 4x4 SRAM array and ÷2/÷4 clock generator. The successful test for two SRAM chips proves that the SiC JFET technology is reliable at 500ºC. However, the supply voltage requirements, including the positive voltage of 25 V and negative voltage of -25 V, make this technology less attractive. And, it is not easy to use this type of SRAM in existing electronic system approaches that are widely adopted and use CMOS technology. Similar to Table 1, a comparison of performance metrics is extracted from the SiC SRAM design literature as shown in Table 2.

Table 2. SiC SRAM Cell Performance Comparison at High Temperatures

	[19]	**[20]**	**[10]**	**This work**
Process	SiC BJT	SiC JFET	SiC CMOS 1 µm	SiC CMOS 1 µm
SRAM Topology	4T	6T with resistors	6T	Novel 6T
Tj_{MAX}	**500°C**	**500°C**	**300°C**	**500°C**
f_{MAX}	9.9 MHz	*30 Hz	~1 kHz	133 kHz
P_{TOT}	NA	*12.125mW	4.52 mW @ 400°C Vdd=20 V	2200 µW @ VDD=10 V
Size	Simulated work	*62128 μm^2	10792 μm^2	31320 μm^2

**Values are estimated from the given information & pictures in the article.*

1.3 Research Objective and Problem Definition

Fabrication of low voltage SiC ICs is an ongoing challenge. Due to the stronger bonds of SiC between silicon and carbon atoms, diffusion rates are very low. Therefore, the only option to add dopants in the wafer is to use ion implantation. Annealing is required as a subsequent step to repair the damage that occurs during ion implantation. Recursive ion implantation followed by

annealing leads to permanent damage in parts of the SiC crystal structure that impacts the performance of a device. Processing of low resistance ohmic contacts is another challenge in SiC. Achieving high active p+-doping concentrations in 4H-SiC through ion implantation remains a challenge due to compensation with ion-implantation generated defects. The interface state between SiC/SiO_2 generates trapped charges in the conduction band of SiC, and due to this intermediate trapped charge the threshold of the device shifts significantly at room temperature and as well as at high temperatures. Also, due to the high energy ion implantation, the polysilicon must be deposited after the implants eliminating the opportunity to make a self-aligned device.

Designing a circuit in SiC to meet the certain specifications is difficult due to the fabrication challenges. Furthermore, the process characteristics changes from one fabrication run to another run given the lack of process control currently available in SiC. Threshold voltage variation that leads to unwanted transistor mismatch is a primary source for huge variation in voltage offsets in the differential pair of an operational amplifier, for example. Conventional silicon processes also deal with the threshold variation and other process related variations, but their impact is not as significant. Additionally, the process control and PDK support helps the designer to simulate the design over every possible corner with local and global variation parameters, along with Monte Carlo simulations.

This research's prime focus is to develop an SRAM memory module that can operate at high temperatures (>400ºC) and consume low power. Due to the process variation and run-to-run changes in the SiC process, designing a circuit to meet the specifications is challenging. Therefore, an adaptable, robust SRAM cell is designed that can be tuned to particular performance metrics regardless of run-to-run changes and process variations. The SiC technology used in this work offers a high threshold PMOS (~7.5V), limiting the operating voltages to be higher than the

PMOS's threshold, which resulted in higher power consumption than expected. However, as the operating temperature increases, the threshold voltage drops for both PMOS and NMOS. Therefore, the SRAM design leverages this intrinsic effect, and careful sizing of the transistors with an informed estimation is determined to operate the memory at lower voltages of ~6 V.

1.4 Key Contributions

The key contributions of this research as described in this dissertation are:

- Developed the SiC PDK, tailored to Cadence Virtuoso suite
- Developed physical design rule checks (DRC and LVS) codes, custom-built for Mentor Graphics CalibreDRC & CalibreLVS
- Device characterization to enable the SiC IC design efforts
- Design, implementation, and characterization of first SiC CMOS 6T SRAM cell
- Design, implementation, and evaluation of various sense amplifiers
- Design, implementation, and characterization of novel SiC SRAM cells to mitigate design challenges introduced by the SiC fabrication technology.

1.5 Overview of the Dissertation

This dissertation is organized into seven chapters. Chapter 1 covers the motivation and the background of high-temperature memory design in SiC. This chapter also includes the literature review to give the readers insight into current technological development in high-temperature memory designs. The author concludes this chapter with the key contributions, problem statement, and research objective. Chapter 2 describes state-of-the-art SiC-based integrated circuit technologies, emphasizing the SiC integrated circuit process used in this work. Moreover, the design enablement in SiC, fabrication challenges, and the device characteristics are also

incorporated in this chapter. Following that, in Chapter 3, the first design of the SiC-based SRAM cell and various sense amplifier architectures are described. The shortcoming of the process technology used is addressed in Chapter 4 by developing the new SRAM cell that mitigates the fabrication challenges at the design level without going through another design cycle. Chapter 4 also includes the RUN #2 sense amplifier designs and their results. Chapter 5 defines the DC and transient testing methodology of the new SRAM cell and its testplan with the sense amplifiers. Chapter 6 contains the measurement results from multiple samples under various test configurations to successfully demonstrate the SRAM cell's functionality. Finally, conclusions and future work are given in Chapter 7. An Appendix contains device characterization results, the MATLAB code, and a brief B1500 tutorial written in the course of completing this work.

2 State of the Art: SiC-based Integrated Circuit Technologies

2.1 SiC Bipolar Integrated Circuit Technology

A SiC bipolar process for low voltage designs is being developed at the Electrum Lab at KTH in Stockholm, Sweden [21]. The developed bipolar process is completely ion-implantation free and therefore suffers less from surface interface traps. Emitter, base, and collector mesas are created by dry etching of CVD-grown epitaxial layers. The silicidation of contacts to P-type and N-type regions are performed in separate steps due to difficulty in forming a good ohmic contact in P-type SiC. This process only has NPN devices and no PNP device. The NPN devices exhibit a room temperature gain of approximately 100. However, the gain drops as temperature increases. The process has shown working analog and digital circuits above 500°C. The main weaknesses of the SiC BJT process are the excess standby power consumption and the lack of PNP transistors to realize complementary circuit designs. KTH is also working on developing a CMOS process but the PMOS devices have a very high threshold (currently ~ 22 V at the time of this writing). KTH also developed the process module to integrate ferroelectric materials into their CMOS process, which in future can be the basis of a memory cell.

2.2 SiC JFET Integrated Circuit Technology

The SiC JFET technology reported in [22] and [23] has three primitive devices: the non-planar depletion mode N-type JFET, a resistor (i.e., the N-type channel layer of a JFET), and a capacitor in between two metal layers. Circuits fabricated in this process are capable of operating at temperatures of up to 800°C and with reliable functionality for more than 1000 hours under bias at temperatures above 500°C [22], [23]. However, designing circuits in this technology specifically a memory cell, is challenging without the P-type device. Moreover, the need for a dual power

supply, meaning positive and negative voltage output rails, is undesirable or infeasible in many applications. Also, the fabrication turnaround time for this process is over 1 year.

2.3 SiC CMOS Integrated Circuit Technology

Cree began developing a 4H-SiC all-NMOS process as reported in [24]. Raytheon also started developing a CMOS process although it ultimately decided to close its foundry. As a result, SiC low power CMOS technology is still in the developmental phase and facing some daunting difficulties in the fabrication process. There are two main primary issues. First, the effective inversion-channel mobility is substantially lower than the theoretical value and secondly the thermally grown SiC-SiO_2 interface exhibits a higher density of interface states than a traditional silicon process. Due to these issues, SiC low power MOSFETs are prone to threshold voltage shifts, gate leakage, and gate oxide failures. Nevertheless, there have been many reports demonstrating the potential and usefulness of SiC CMOS IC technology. In comparison to the bipolar and JFET processes previously discussed, the SiC CMOS process is superior since it offers low power consumption and a full rail-to-rail output swing.

2.4 Fraunhofer's SiC 1 µm CMOS 1P1M Process Technology

The SiC integrated circuits designed for this research are fabricated at the Fraunhofer Institute for Integrated Systems and Device Technology (Fraunhofer-IISB) in Erlangen, Germany. Fraunhofer-IISB focuses on developing lateral P-type and N-type MOSFETs that can operate at high-temperature where the conventional silicon process cannot operate. They developed a technology computer-aided design (TCAD) model to achieve their goal, but did not develop the process design kit (PDK) that is necessary to realize a complex circuit topology or even a circuit design with many transistors. Consequently, during this thesis research, work to develop a SiC

PDK tailored to the Cadence Virtuoso platform and physical design verification rule checks for Mentor Graphics Calibre (DRC ad LVS) was required. As a result, two 20 mm × 15 mm reticles, each for 100 mm wafers, were designed over three years using this PDK and design rule checker. The PDK development effort also helped in increasing the device portfolio of Fraunhofer's technology.

2.5 SiC Design Enablement

2.5.1 PDK Development

Generally, semiconductor foundries generate the transistor and passive component models for each process for use in the IC design tools such as Cadence Virtuoso. Circuit designers use these models to design integrated circuits. Before submitting the design layout to the foundry, the layouts are verified for the technology-specific Design Rule Checks (DRC), Layout Vs. Schematics (LVS) checks, and Parasitics Extraction (PEX) simulations. The PDK combines all the device models and physical verification checks into a set of files. Thus, the designer uses the PDK to design, simulate, layout, and verify the design before releasing the chip for fabrication. The accuracy of the PDK, particularly the design verification, is considered crucial and increases the chances of a successful first-pass tapeout.

The design, simulation, and layout part of the Fraunhofer PDK is built for the Cadence Virtuoso platform. The physical design rule checks are tailored for Mentor Graphics tools: CalibreDRC and CalibreLVS. Cadence Virtuoso and Calibre tools allow interoperability; hence the PDK is set up to run Calibre tools under the Cadence Virtuoso environment. The design flow and the libraries and rules sets are created to support these two platforms. Following are the components of the PDK that were developed:

- A primitive design library (Cadence Virtuoso)
    - Device parameters
    - PCells
    - Symbols
- Technology data (Cadence Virtuoso)
    - Layer definition files, layer names, layer and purpose pairs
    - Display attributes (Colors)
    - Process constraints
- Physical Verification decks (Mentor Graphics: CalibreDRC and CalibreLVS)
    - DRC
    - LVS
- Simulation models of primitive devices (HSPICE)
    - Transistors
    - Diodes.

Fraunhofer provided the technology-specific design rules in an Excel sheet with the minimum dimensions and overlapping layer requirements for all seven layers of the process. The design rules translated into Standard Verification Rule Format (SVRF), a programming language for Mentor Graphics semiconductor design tools [25]. The technology file needed for Cadence Virtuoso to set up Fraunhofer technology's environment is created using a programming language called SKILL [26], [27]. The number of layers, display attributes, via layers, type of contacts, layer purpose, etc., are defined in the technology file.

Developing the PDK also helped extend the portfolio of the primitive devices, as the foundry was only focused on developing MOSFETs. With the help of PDK, several passive

devices, different laterally-diffused metal oxide semiconductor (LDMOS) structures, bipolar transistors (BJT), diodes [28], optocoupler structures, and electrostatic discharge (ESD) devices [30] were designed and tested successfully after the tapeout. Hence, the PDK development contributed to elaborating the true potential of the SiC technology and the capability to have higher density circuits for various applications.

2.5.2 Fabrication of 1 μm CMOS 1P1M Process Technology

Fabrication of low voltage SiC devices is not as mature as conventional silicon technology. Due to the requirement of higher ionization levels for adding dopants, incomplete ionization at room temperature, and slow diffusion rates, SiC fabrication typically relies on ion implantation and annealing at a high temperature. “High-temperature annealing needs to be done after every implant that leads to unwanted crystal structure destruction in parts of the SiC wafer. In addition to these challenges, the existing manufacturing capabilities result in high wafer costs and a longer lead time for the delivery of fabricated SiC wafers. It should be noted that significant investments are being made to rapidly expand the manufacturing capacity.”[28]

The fabrication started with the commercially available Cree N-type 4H-SiC wafers. At first, the P-type epitaxial layer is grown on the wafers. Subsequently, alignment marks were processed to align the subsequent masks with the wafer. A total of eleven masks were used to process the following layers: ALIGN, NWELL, PWELL, P+, N+, ACTIVE, POLY, POLYVIA, NOHM, POHM, and METAL. Wells and diffusion layers were deposited through ion implantation. After the implantation, the poly layer is patterned. Subsequently, the N+ and P+ ohmic contacts were formed on the wells to create a low resistance contact to the metallization layer. The P+ ohmic contact formation suffered from a high contact resistance; the foundry claimed

that it is due to the unintentional over-etching of the NWELL region. To provide a comparison, the measured resistivity of the N+ region is 0.0017 mΩ·cm2 whereas the P+ region has a resistivity of 44 mΩ·cm2, which is a significant increase for the same size contacts. This resulted in undesirable performance for the PMOS devices [28]. Thus, the foundation of this research was established to mitigate the impact of inadequately performing PMOS devices.

2.5.3 SiC Circuit Design Approach for RUN #1

The RUN #1 circuits were designed from old Raytheon process models [29] because, at the time of RUN #1 tapeout, Fraunhofer did not have any device models. Instead, they provided SiC sample MOSFET devices having channel lengths of 3 µm, 5 µm, and 10 µm with a fixed width of 100 µm for each. To develop a basic MOSFET model, wide/long, narrow/long, wide/short, and narrow/short MOSFET dimensions are required [29]. The sample devices have an oxide thickness of 25 nm, and their processing modules are also different than the selected modules for RUN #1. Based on the sample die's measurement data, the PFET to NFET ratio is estimated to be 5:1. Coincidently, Raytheon's process also used a 5:1 ratio for the inverter. Therefore, the circuits in RUN #1 were designed with Raytheon's model. The intention of RUN #1 was primarily to characterize the Fraunhofer process and develop models for future fabrication tapeouts. It took Fraunhofer a year to return the fabricated wafers once the designs were delivered for fabrication.

2.5.4 Characterization Results of SiC MOSFETs from RUN #1

"The RUN #1 CMOS devices with varying widths and lengths were characterized over the temperature range of 25°C to 300°C. The Fraunhofer-IISB's SiC CMOS technology supports a minimum channel length of 0.8 µm. However, the yield for smaller channel length devices was

heavily affected by the mask sets' misalignment. Therefore, the devices with smaller channel lengths (for example, 0.8 µm and 1 µm) were not characterized.

The cross-sections of the NMOS and PMOS devices are shown in Fig. 1 and 2, respectively. The NMOS device can be isolated by forming a PWELL inside an NWELL, as shown in Fig. 1. This isolation gives a designer the flexibility to cascode several NMOS devices while still connecting each device's body and source terminals. This eliminates the body effect and the corresponding threshold voltage increase.

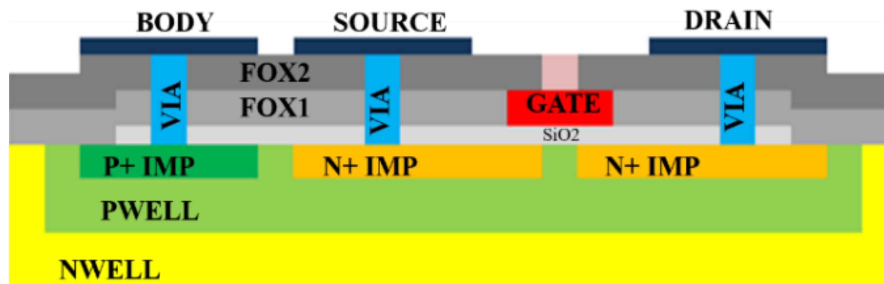

Fig. 1. Cross-section of a SiC NMOS device. The NWELL layer is an isolation layer between the PWELL and the P-type epitaxial layer.

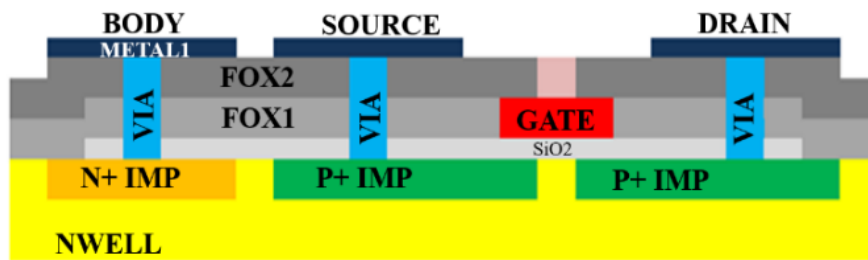

Fig. 2. Cross-section of a SiC PMOS device.

A channel width of 20 µm is selected for representing the DC output characteristics and small-signal parameters of both the NMOS and PMOS transistors. Output characteristics of the SiC NMOS and PMOS devices are shown in Fig. 3 and 4, respectively. These devices have a channel length of 1.5 µm. The drain-source voltage (V_{DS}) is swept from 0 V to 20 V with a step size of 0.5 V with a gate-source voltage (V_{GS}) varying from 3 V to 19 V with a step size of 2 V.

The drain current increases over temperature for NMOS and PMOS devices, which is due to increasing channel mobility and intrinsic carrier concentration. As previously mentioned, the P+ regions of PMOS drain and source contacts were over-etched during fabrication. Instead of forming an ohmic contact, a diode contact was formed, which can be observed from the linear region of the output characteristics plot shown in Fig. 4 for a PMOS device.

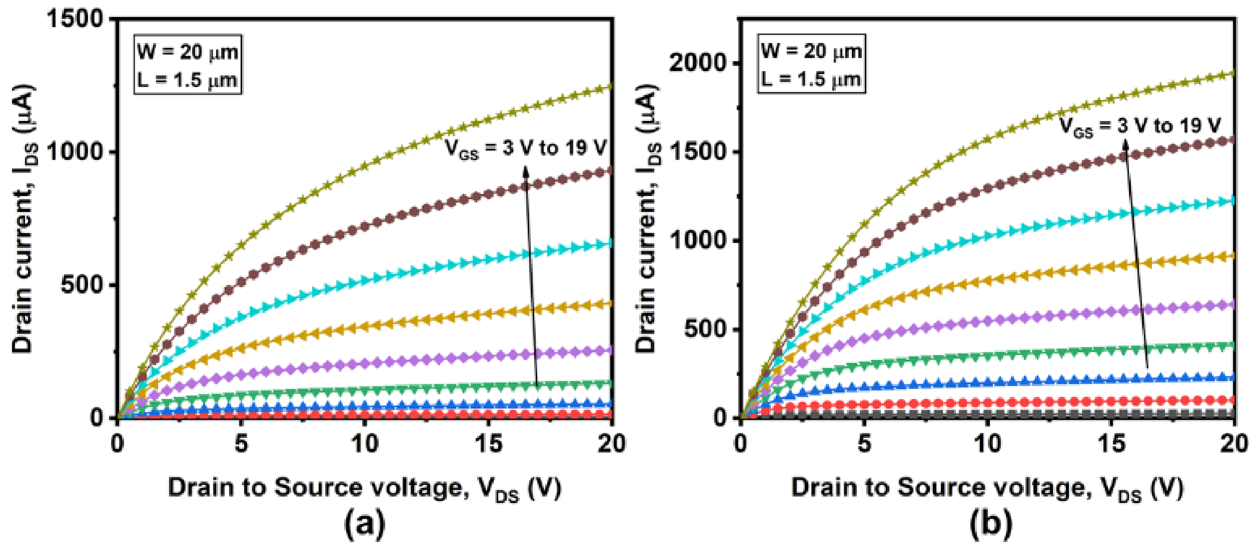

Fig. 3. Output characteristics of SiC NMOS at temperatures of (a) 25°C and (b) 300°C.

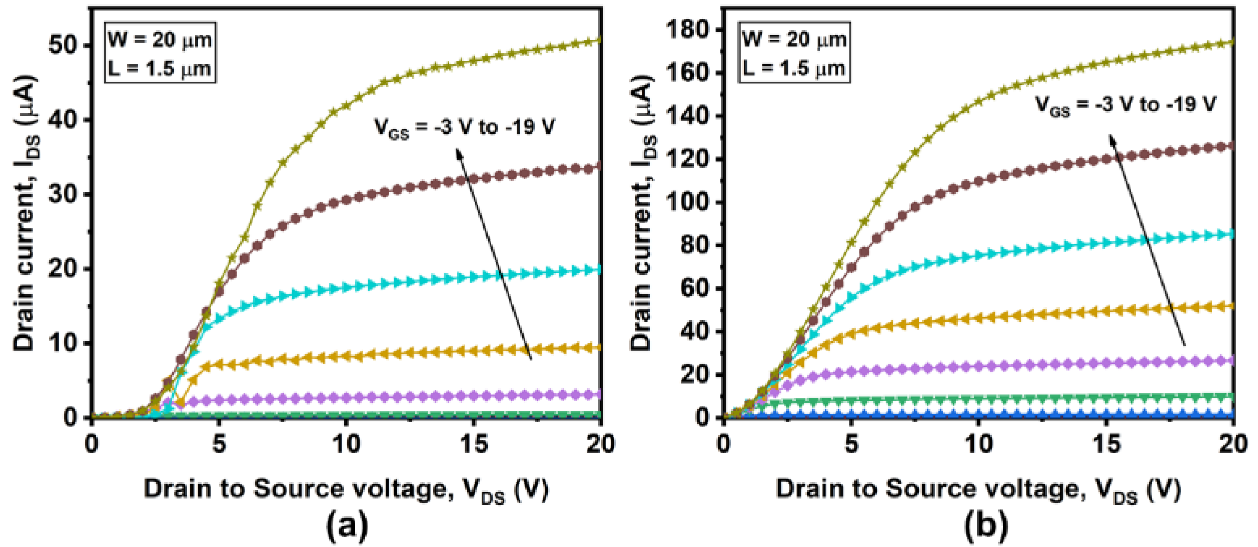

Fig. 4. Output characteristics of SiC PMOS at temperatures of (a) 25°C and (b) 300°C.

The transconductance (g_m) of NMOS and PMOS devices is shown in Fig. 5 (a) and (b), respectively. Measured results show the increase in g_m with the increase in temperature, which contradicts the conventional silicon-based MOSFETs. This inconsistency is primarily due to the thermally grown SiC oxide, which is prone to higher levels of interface state densities, charge trapping, and other effects. These interface trapped charges release additional carriers at higher temperatures, which cause an increase in the drain current. The g_m drops at higher V_{GS} for both NMOS and PMOS due to reduced effective carrier mobility [31].

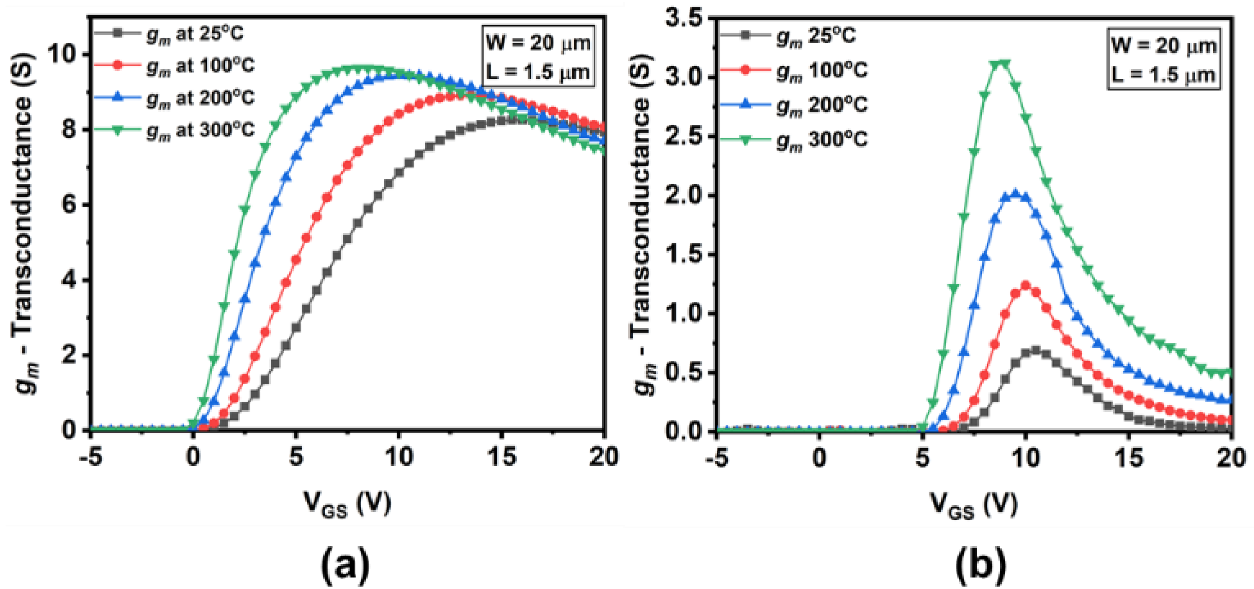

Fig. 5.(a)Transconductance variation over the temperature for NMOS (b)Transconductance variation over the temperature for PMOS.

However, the drop in transconductance at higher V_{GS} is sharper for the PMOS devices than for NMOS devices. To better understand this behavior, the I_D vs. V_{GS} (at V_{DS} = 2 V) plot for the SiC PMOS are provided in Fig. 6. As V_{GS} increases above 8 V in Fig. 6, the drain current starts to saturate. This behavior is a result of the previously mentioned poor P+ contact formation during fabrication that results in the PMOS drain/source contacts having high resistance and limiting the drain current as V_{GS} increases." [28]

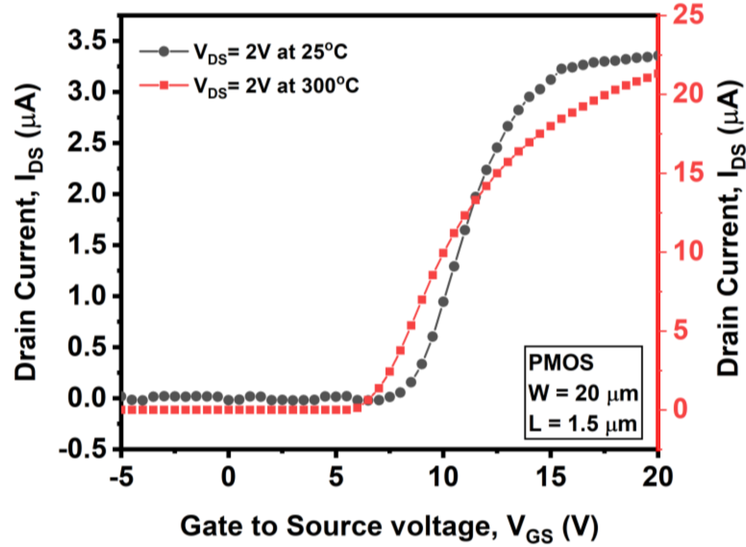

Fig. 6. I_{DS} vs V_{GS} for PMOS with channel width = 20 µm and channel length = 1.5 µm.

Due to the developing nature of Fraunhofer's SiC CMOS technology, the RUN #1 efforts revealed several issues related to the fabrication of different modules in the process. The resulting PFET to NFET ratio was 25:1 at room temperature for a 1.5 µm channel length device. Table 3 shows the PFET to NFET ratio with increasing channel lengths. The PFET to NFET ratio decreased for larger device sizes, indicating that the contacts were the primary source of this issue.

Table 3. The PFET to NFET Ratios for Various Channel Lengths and a Fixed Width of 20 µm

Temperature (°C)	Size (W/L) (µm)	PFET (µA)	NFET (µA)	Ratio
25	20/1.5	50	1250	25
200		174	1960	11.15
25	20/2	41.6	690	16.6
200		136	1250	19.19
25	20/4	25	235	9.4
200		77	512	6.65
25	20/6	18.4	141	7.69
200		54.2	322	5.94
25	20/10	13.5	78.3	5.80
200		36	185	5.13

Additional results from RUN #1 and RUN #2 are added in Appendix A. It includes the wafer maps for RUN #1 MOSFETs for 1.5 µm and 2 µm channel length devices. It also shows the playback for BSIM 4.7.0 compact model with the measured data. The exercise of compact model

fitting was accomplished to support the circuit design efforts for RUN #2. Unfortunately, the circuit's performance did not match with the simulated performance because the several process changes were made between RUN #1 and RUN #2 to attempt to correct problems. The comparison between RUN #1 and RUN #2 devices is also shown in Appendix A.

3 Design of an SRAM in RUN #1

3.1 Introduction to SRAM and Sense Amplifiers

Static random-access memory (SRAM) is a type of semiconductor memory. It stores each bit by adopting bistable latching circuitry (such as a flip-flop). It retains data remanence, but in the traditional sense, it is still volatile. When the memory is not powered on, the data will eventually be lost. Because of positive feedback in an SRAM cell design, it does not need periodic data refreshing. The data from SRAM can be read/written faster, but it requires more area and its dynamic power can be significant depending on the memory size and frequency. It is usually used for the CPU cache. There are some advantages and disadvantages of SRAM memory, which have been listed below:

- Advantages: simplicity (without performing a refresh circuit), performance, reliability, low idle power consumption.
- Disadvantages: price, density, high operational power consumption.

On the other hand, SRAM used at a slightly slower speed, such as in applications with moderately clocked microprocessors, consumes very little power and consumes almost negligible power at idle, around a few microwatts.

The SRAM IP block is divided into four main sub-blocks: Memory/bit Cell, Sense Amplifier, Row Decoder, and Column Decoder. In RUN #1, bit cells and sense amplifiers were implemented. There are a couple of topologies for designing SRAM bit cells, such as 6 transistor (i.e., 6T), 7 transistor, 8 transistor, and 9 transistor topologies. For RUN #1, the 6T SRAM bit cell topology was chosen because it has fewer transistors and utilizes less area than other topologies. The schematic of the 6T SRAM cell is shown in Fig. 7. It consists of two CMOS inverters (M1 & M2, M3 & M4) and two NMOS *access* transistors (M5 & M6). The CMOS inverters are connected

in a cross-coupled fashion (i.e., a latch) and form a bistable circuit, and the access transistors form a "make or break" path between storage latch outputs and read-write circuits by connecting it to bitlines. The SRAM cell has two bitlines that control both the input and output of data from the cell.

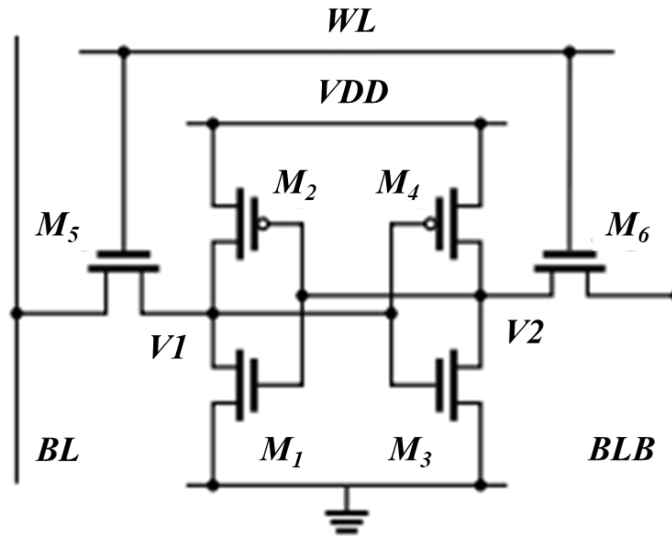

Fig. 7. 6T SRAM bit cell.

The SRAM cell operates in three modes: standby, read, and write modes. In standby mode, access transistors are turned off by grounding the Wordline (WL), so the latch retains its stored value for an indefinite time as long as the power supply is there. The WL selects the cell and allows values to be read from or written to the cell. In read mode, the sense amplifier is used to measure the differential voltage between the two bitlines. These bitlines are pre-charged to the supply voltage. When access transistors turn on, one of the bitlines starts to discharge through the pull-down transistor of the inverter that is latched to zero potential. There are two main categories of sense amplifiers Differential Mode sense amplifiers (also known as *voltage* sense amplifiers) and Non-Differential Mode sense amplifiers (also known as *current* sense amplifiers). Generally, voltage sense amplifiers are used because they are reliable and straightforward. Furthermore, they

are more area efficient than current-mode sense amplifiers. The performance of voltage sense amplifiers is dependent on the bitlines' capacitance. Larger bitline capacitance makes large RC time delays for the system, and because of this delay, the time taken by the bitlines to generate differential voltage is also high. Typically, a 300 mV to 500 mV differential voltage is enough for the sense amplifier to detect the value and latch the output.

A variety of differential voltage sense amplifiers are in use, such as the Simple Differential Voltage Amplifier and Full Complementary Positive Feedback Voltage Sense Amplifier. A schematic for the Full Complementary Positive Feedback Voltage Sense Amplifier is shown in Fig. 8. It is selected for implementation in RUN #1 and consists of two cross-coupled inverters (M4 & M7, M3 & M6), which use positive feedback to cause latching behavior. The Pre-Charge circuitry includes M1, M2, and M0, which charge the bitlines before the read operation. The read enable transistors (M5 and M8) are used to isolate the cross-coupled inverters when the SRAM cell is in the hold state. In addition to that, it does not require active current mirrors and a biasing circuit, which makes this sense amplifier a better choice for high-temperature environments. There are other amplifier variations, but this one is the most straightforward and reliable choice.

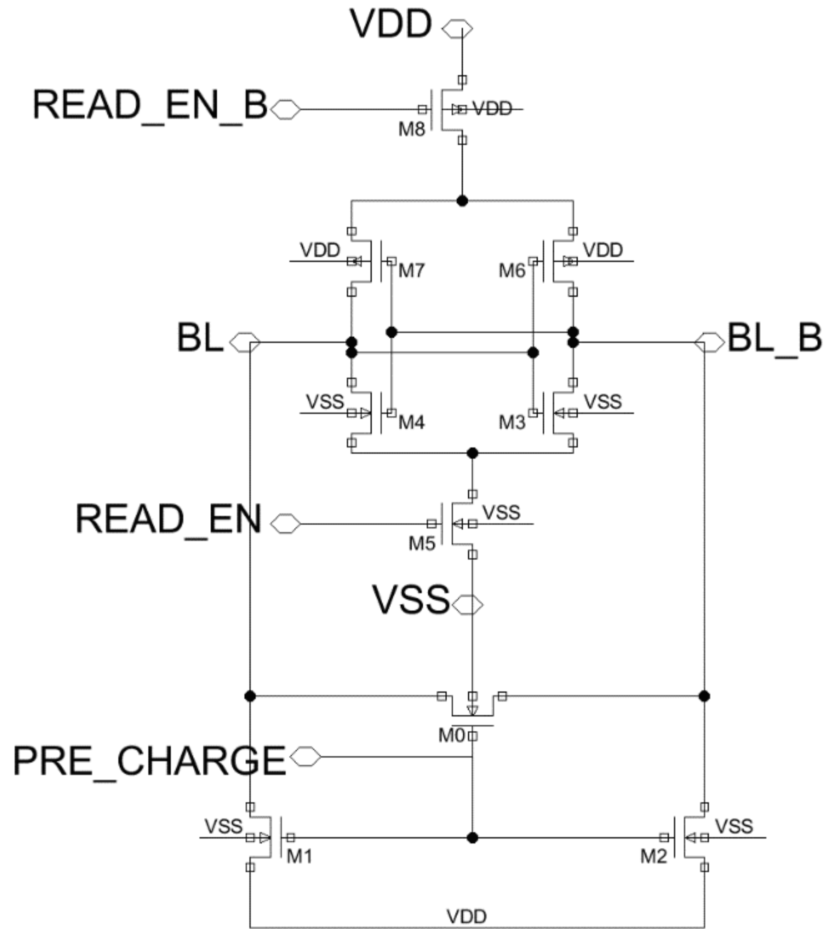

Fig. 8. Full complementary positive feedback sense amplifier.

3.2 SRAM Test Structures in RUN #1

"Stability and cell area are the two important aspects for SRAM cell design. Cell stability is usually defined using static noise margin (SNM), which is the maximum DC noise voltage that can be tolerated by the cell without having any effects on the stored bit. The bit cell is most vulnerable to static noise voltage when it is in the read mode. This is due to pre-charged bit lines being connected to the storage nodes that can increase the potential of the storage nodes with a logic '0' value and cause a stored bit to flip to a logic '1'. To perform a nondestructive read operation, the ratio of current driving strength for the access transistor as compared to the pull-down transistor must be carefully selected. This is critical to avoid unintentionally increasing the

voltage of the storage node when it ideally has a logic ‘0’. The ratio between the access transistor and pull-down transistor is termed cell ratio (CR), which is expressed below.

$$Cell\ Ratio = \frac{W_{PD}/L_{PD}}{W_{AD}/L_{AD}}$$

W_{PD}, L_{PD}, W_{AD}, L_{AD} are the widths and lengths of the pull-down and access transistors, respectively.

Like CR, there is another sizing parameter referred to as the pull-up ratio (PR). This term refers to the ratio of the pull-up transistor to the access transistor. The restoring strength (current driving capability) of the pull-up transistor must be higher than the strength of access transistors for a cell to perform a write operation. An expression for the PR is provided below. W_{PU} and L_{PU} are the width and length of the pull up transistors, respectively.

$$Pull\ Up\ Ratio = \frac{W_{PU}/L_{PU}}{W_{AD}/L_{AD}}$$

Due to the nature of the fabrication process and the early development phase of SiC integrated technology, multiple variants of SiC SRAM cells have been implemented for fabrication in RUN #1. Different values of CR (0.5, 1, 1.5, 2, 2.5) and PR (1, 2, 3, 4, 5, 6) are selected in order to determine the optimal cell size from the various performance parameters measured over temperature for each cell. SNM values for the different combinations of CR and PR are calculated using the model developed by Seevinck, et. al. [32]. Each cell variant is designed using minimum length NMOS and PMOS transistors (L = 1 μm). Fixed width NMOS (W = 4 μm) is used in the cross-coupled inverters, where the width of the PMOS increases to increase the pull-up ratio from 2:1 to 12:1.

Layouts for the cells are optimized for this process, but are affected by the limitation of the availability of only a single metal layer for routing. Thus, poly has been used as a second routing

layer. Poly is a more resistive routing layer (R_{sh} = 15 Ω/□.) and an effort was made to minimize its use in the various layouts. Two different layouts are designed to have reduced dimensions. Fig. 9 shows both the layouts with their dimensions. The shown SRAM cells have a CR = 0.5 and PR = 6.0. In order to make bitline routing less resistive, only the metal layer is used. The downside to these layout decisions is that the power rails of a cell are routed on poly wherever bitline is crossing."[10]

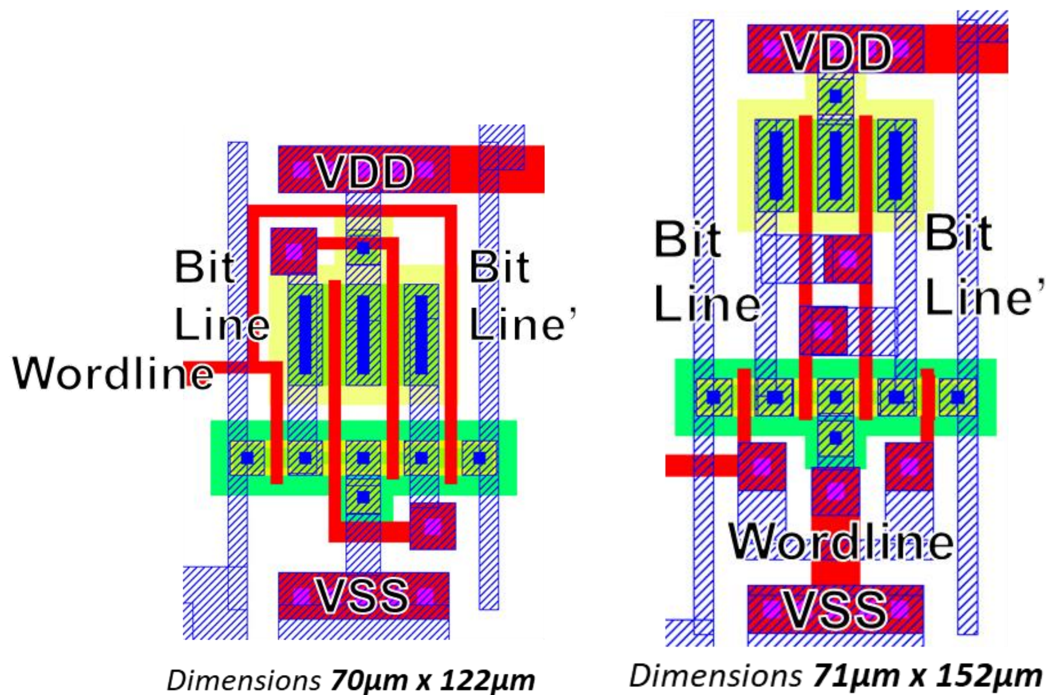

Fig. 9. SRAM cell layouts.

3.3 DC & Transient Measurements

In all the combinations of CR and PR, the pull-down network always dominates, and the pull-up network cannot pull the node to VDD. In the implemented cell designs, the minimum CR is equal to 0.5, which means the pull-down network is at its lowest drive strength, and the maximum PR is set to 6.0. A PR of 6.0 indicates that the pull-up network is the strongest. CR and PR values are selected based on the PMOS to NMOS ratio of 5:1 and 6:1. However, due to the

unexpected drive strength ratios of fabricated PMOS and NMOS being 23:1 at 25°C and 10:1 at 300°C, the pull-up strength is lower for all the implemented CR and PR combinations. The CR of 0.5 means the pull-down transistor (M1 and M3 in Fig. 7) is at it's minimum size (4 μm / 1 μm) and the access transistor (M5 and M6 in Fig. 7) is two times the size (8 μm / 1 μm) of pull-down transistor. The PR of 1 means that the pull-up transistor (M2 and M4 in Fig. 7) is at the same size (8 μm / 1 μm) as access transistor. The increase in the size of the pull-up transistor, increases the PR. For the PR of 2 the pull-up transistor is two times the size (16 μm / 1 μm) of the access transistor. Likewise, for PR of 3 it is three times (24 μm / 1 μm) and so on. Fig. 10 shows the SNM results for the CR of 0.5 with varying PR at 25°C and 300°C. The V1 is the voltage that is swept from 0 V to 20 V at the gate of the inverter (M3 and M4) of the SRAM cell shown in Fig. 7. The V2 is the voltage measured at the output of the inverter (M3 and M4). The result captured from the voltage sweep is the voltage transfer characteristics (VTC) of the first inverter (M3 and M4). The SNM for the SRAM is measured from the two back-to-back inverters. The VTC is plotted as V2 vs. V1, where V2 is on the vertical axis, and V1 is on the horizontal axis. The second inverter (M1 and M2) is identical to the first inverter, therefore first inverter VTC is used again but the axes are swapped. Now, the V2 is on the horizontal axis, and V1 is on the vertical axis. The back-to-back VTC of the inverters is called butterfly plot and the diagonal of the largest square that fits within the back-to-back DC characteristics is the value of the SNM. The MATLAB code is developed (see Appendix C) to extract the value of the SNM from the butterfly curve. At high temperatures, the device performance gets better. Therefore, a minor increase in the pull-up network's performance can be noticed in Fig. 10. Also as the PR is increasing the eye of the butterfly plot is also increasing, resulting in higher SNM values.

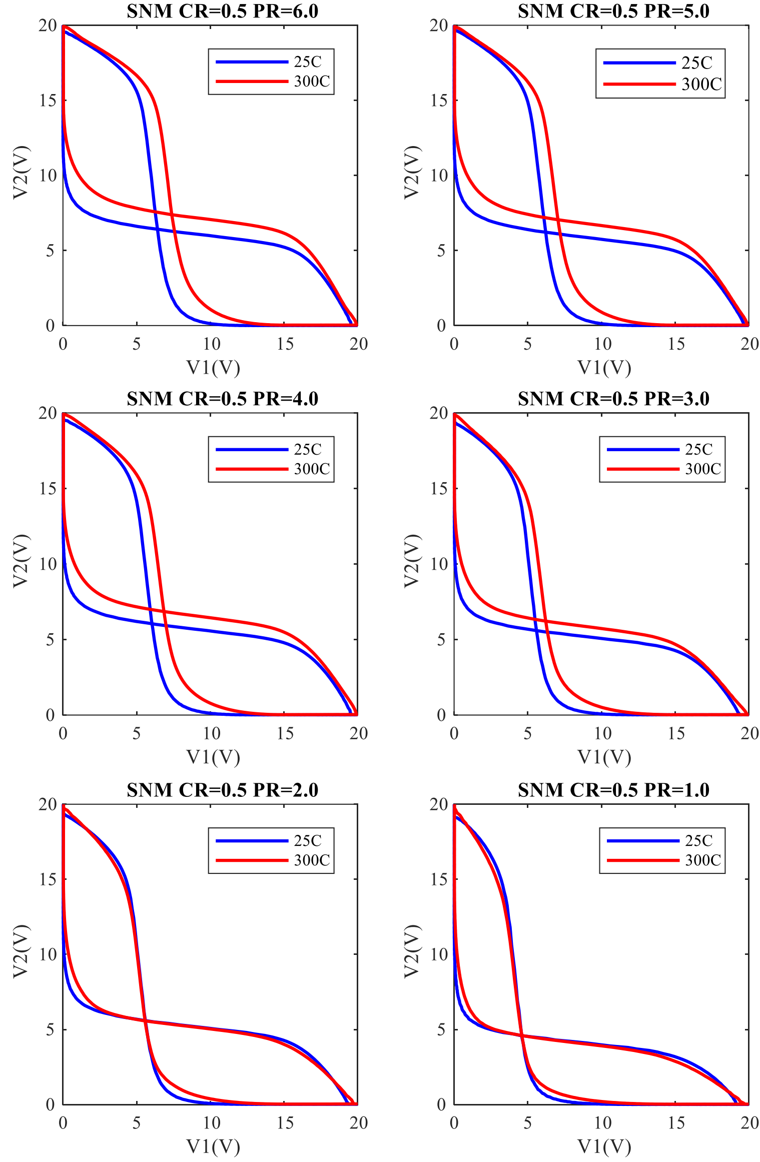

Fig. 10. SNM at 25°C and 300°C.

All the measurements are performed on a Signatone probe station. A Keysight B1500 DC curve tracer has been used for sweeping the input voltages. Room temperature measurements were performed on all the SRAM cells, and then high-temperature measurements were subsequently performed. At temperatures above 300°C, the threshold voltage of NFETs dropped below 1 V, and the threshold of PFETs lowered down to -4 V from -8 V (at room temperature), which results in

lower SNM for the cells. A lower threshold for NFETs leads to the storage node being pulled down stronger than the PFETs can pull it up.

An SNM of 4.71 V at 25°C and 4.65 V at 300°C demonstrates that the cell is capable to sustain this much of noise voltage at the supply voltage of 20 V. The noise can be triggered from the read or write operation. From Fig. 10, it can be seen that the implemented cells have the capability to hold the stored data at high temperatures, and the cross-coupled inverters are retaining their bistable states. An RSNM of 1.94 V at 25°C and 1.90 V at 300°C for CR=0.5 and PR=6.0 shows some robustness against the noise generated from precharged bitlines during the read operation. But the RSNM values are not sufficient, and there is a room for improvement to guarantee a proper read operation without disrupting the stored bits. The WSNM cannot be evaluated because of the unanticipated poor drive strength of PFETs. The performance of the SRAM cell is expected to improve significantly with the improvement in the SiC CMOS process.

Table 4. The SNM and RSNM at CR=0.5

PR	SNM(V)		RSNM(V)	
	25°C	300°C	25°C	300°C
1	4.31	4.28	1.58	1.51
2	4.39	4.27	1.65	1.62
3	4.46	4.3	1.77	1.72
4	4.51	4.42	1.83	1.79
5	4.57	4.53	1.85	1.82
6	4.71	4.65	1.94	1.90

The test structure used for transient analysis has the CR = 0.5 and PR = 6.0. The test structure schematic is shown in Fig. 11. This analysis aims to check the operation of access transistors and the storing capability of the SRAM cell at elevated temperatures. Measurements were conducted on a high-temperature probe station from room temperature to 500°C.

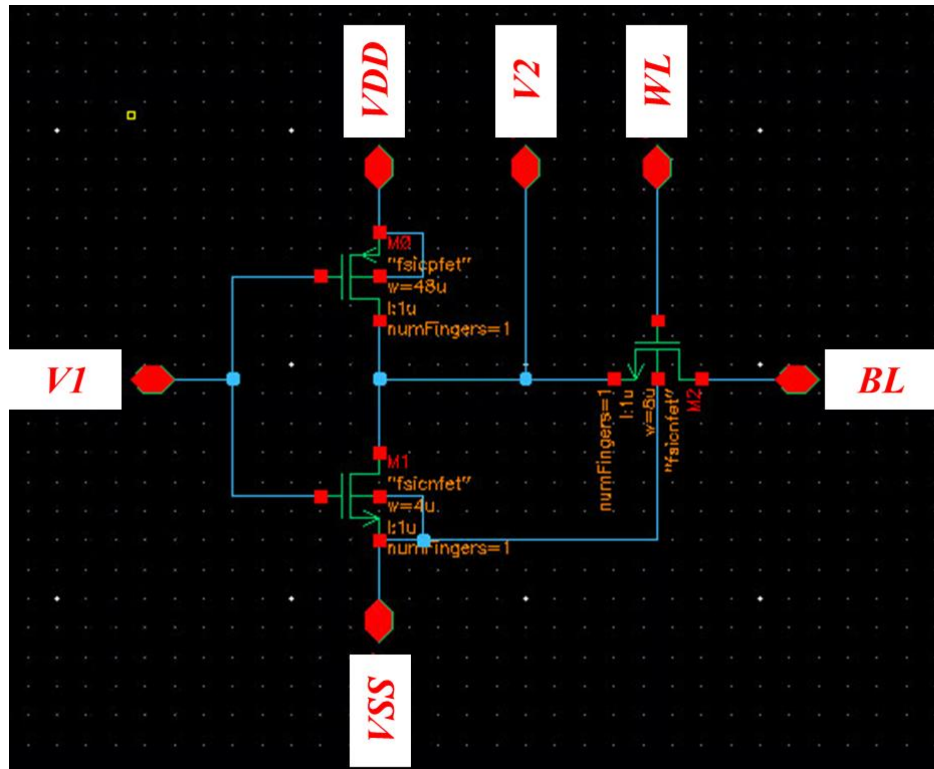

Fig. 11. Half SRAM cell structure.

During the initial test setup, the stored bit flips whenever the wordline was asserted. This was due to the 13 pF load of the oscilloscope on the V2 pad of the test structure. Later, a pico-probe was connected at the output because it has only 0.1 pF of load. To see the functionality of the access transistors, four equal width pulses were triggered onto the wordline. During the first pulse, the V1 node was set to logic 0, resulting in logic 1 at V2. When the wordline triggers, the bitline copies the signal from the V2 node. Similarly, the second pulse of wordline V1 was set to 1, which resulted in logic 0 at V2. At this instance, the bitline is already discharged to 0 V before the wordline triggers, and it stays logic 0 when the wordline triggers. The bitline signal is connected to a cell through the access transistors, and whenever that transistor turns on, it passes the signal from the cell to the bitline. Due to the poor PMOS drive strength, the bitline node cannot be pulled to the VDD rail. However, as the temperature increases, the rail voltage of the bitline

also increases. The V2 signal showed an offset with the increase in temperature due to the pico-probe amplifier DC offset. Fig. 12 shows the captured results at probe station with temperatures between 25°C to 500°C.

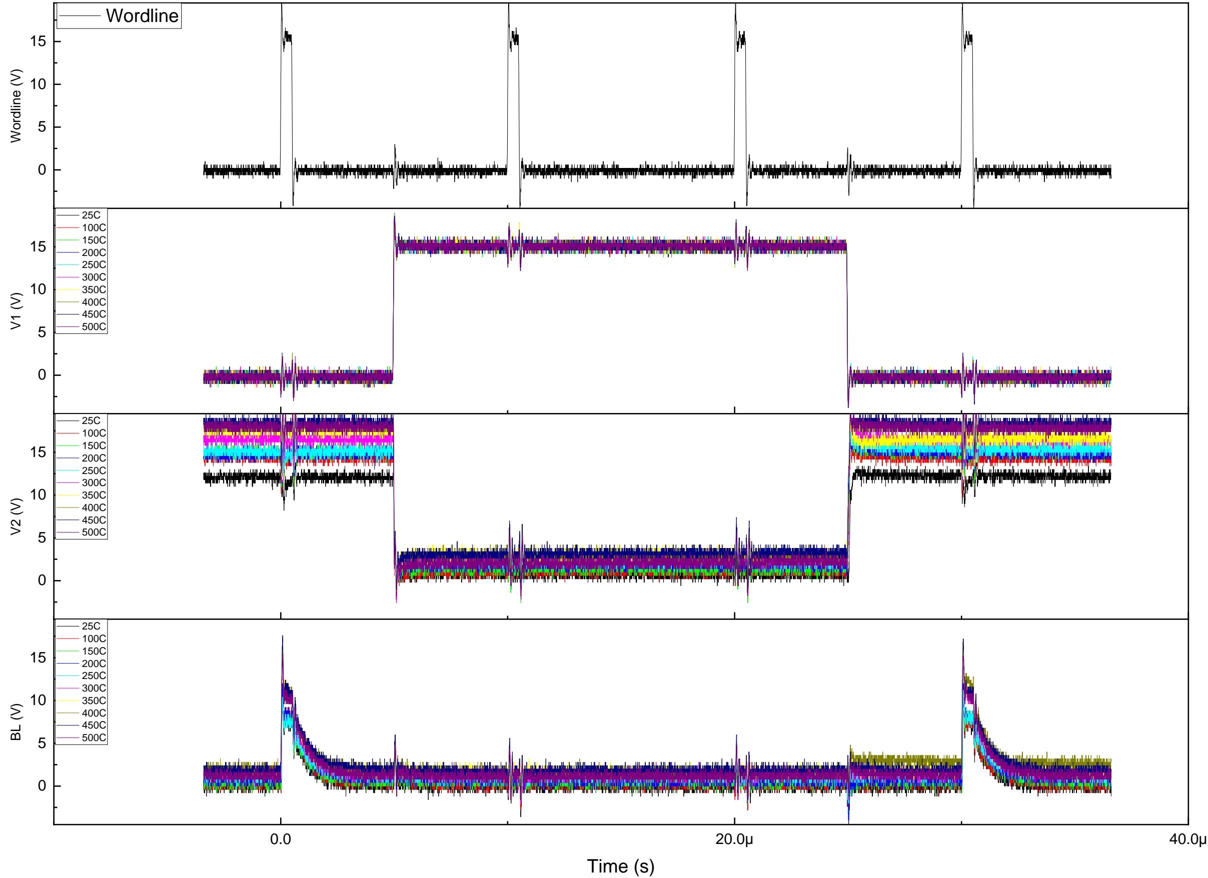

Fig. 12. Transient analysis of an SRAM Cell on the probe station at various temperatures.

4 The Novel SiC SRAM Cell Design in RUN #2

4.1 Process Module change from RUN #1 to RUN #2

RUN #1 measurement results revealed several issues related to the fabrication of different modules in the process. The lessons learned from RUN #1 were considered to improve the fabrication process of RUN #2. For the RUN #2 fabrication, foundry personnel decided to start with NWELL implants as the first ion implantation module in order to avoid P+ implants over-etching. They also optimized the hard mask etching sequence. Additional process control modules are added in RUN #2 to avoid oxide residual during the formation of gate vias and also to monitor the formation of the ohmic contacts.

The RUN #2 processing started with twelve wafers with various wafer splits, as shown in Table 5. After the completion of all the ion implantation modules, six wafers were set aside as a backup. Four wafers received a lower NWELL doping of 3E15 cm^{-3} that is expected to decrease the threshold voltage of PFETs. In RUN #1, the NWELL doping concentration was set to 5E15 cm^{-3}. P-doped polysilicon is selected for four wafers, and of these four wafers, two received the RUN #1 doping, and the other two received the adjusted NWELL doping.

In RUN #1, an N-doped polysilicon was used. Changing to P-doped polysilicon type was estimated to increase the V_{THN} of NFETs by 1 V and decrease the V_{THP} magnitude of PFETs by 1 V. Altering to P-doped poly resulted in higher interconnect resistance due to its larger sheet resistance value of 40 Ω/□ compared to 15 Ω/□ for n-doped poly. For P-doped poly wafers, local polycided interconnections were used to minimize the interconnect trace resistance. Aluminum and platinum metallization options were added in an effort to evaluate the high-temperature characteristics of each.

Table 5. Wafer Split for 12 100 mm SiC Wafers for RUN #2

<table>
<tr><th>Wafer</th><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th><th>8</th><th>9</th><th>10</th><th>11</th><th>12</th></tr>
<tr><td>Isolation Type</td><td colspan="12">field oxide</td></tr>
<tr><td>Gate Oxide</td><td colspan="12">50 nm</td></tr>
<tr><td>PASS0 Doping Reference</td><td>X</td><td>X</td><td></td><td></td><td></td><td></td><td colspan="6" rowspan="8">These wafers are in processing</td></tr>
<tr><td>Adjusted NWELL Doping</td><td></td><td></td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>Polycided (TiSi) Local Interconnection</td><td>X</td><td></td><td>X</td><td></td><td>X</td><td></td></tr>
<tr><td>P-doped Polysilicon</td><td>X</td><td>X</td><td>X</td><td>X</td><td></td><td></td></tr>
<tr><td>1 Layer Al and 1 Layer PolySi</td><td></td><td>X</td><td></td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>1 Layer Pt and 1 Layer PolySi</td><td>X</td><td></td><td>X</td><td></td><td></td><td></td></tr>
<tr><td>Passivation</td><td>X</td><td>X</td><td>X</td><td>X</td><td></td><td></td></tr>
</table>

4.2 Proposed SiC SRAM Cell for RUN #2

Given the significant changes from RUN #1 to RUN #2, new cell designs with additional pull-up strength and access transistors were created. The schematic for a novel SRAM cell is shown in Fig. 13. The issues encountered in RUN #1 and the uncertainty in the device performance of RUN #2 encouraged the design of an SRAM cell that is adaptable to the worst and the best cases. However, the tradeoff is made in the design size, number of I/Os, and the power consumption of the cell.

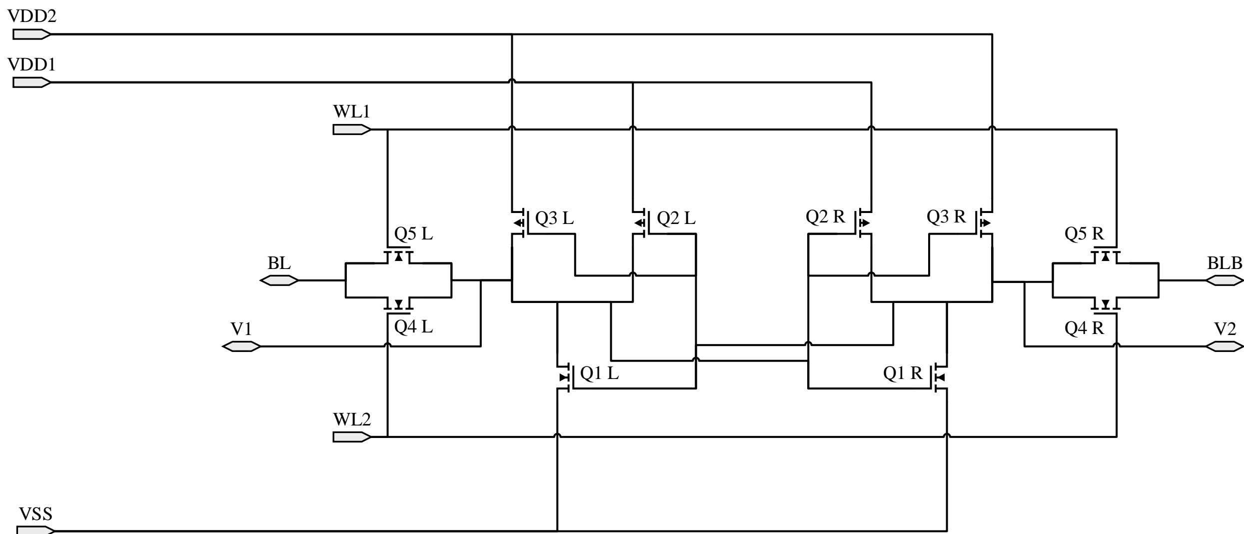

Fig. 13. Novel SiC SRAM cell for RUN #2.

The designed cell consists of an additional PFET in the inverters of the standard 6T SRAM cell, labeled as Q3 L and Q3 R in Fig. 13. These two transistors are connected to a separate supply, VDD2, offering flexibility to tune the drive strength for the pull-up network of the SRAM cell. Since the performance of the PFETs in RUN #2 was unknown, this design approach supports both worst and best cases in terms of PFET's performance. The pull-up and pull-down networks must be precisely scaled to retain the stored bit in the SRAM cell. In addition to that, the access transistors are the key to perform the read and write operations. Due to unknown PFET behavior, parallel access transistors are added in the design (Q4 R, Q5 R, Q4 L, and Q5 L) controlled from two separate wordlines (WL1 and WL2). This allows for additional flexibility in the read and write operations without going through another design iteration. Two test structures are designed with different access transistor sizing; Table 6 shows the transistor sizing of the designed cell.

Table 6. Novel SRAM Cell Transistor Sizes

Transistor	Q1 L	Q2 L	Q3 L	Q4 L	Q5 L	Q1 R	Q2 R	Q3 R	Q4 R	Q5 R
TS1 Widths (μm)	5	50	50	8	8	5	50	50	8	8
TS2 Widths (μm)	5	50	50	5	5	5	50	50	5	5

The layout of the cell designed in RUN #2 is shown in Fig. 14. The trade-off is made in the cell area, and it is at least two times larger than RUN #1 SRAM cell. The availability of only one metal layer in the process made the layout a challenge. Therefore, to keep the cell density smaller, the poly layer is used as a second routing layer. Even though the poly layer has higher resistance, it is used to route the power nets. The metal layer is used to route the bitlines because they need to be less resistive to perform read and write operations faster.

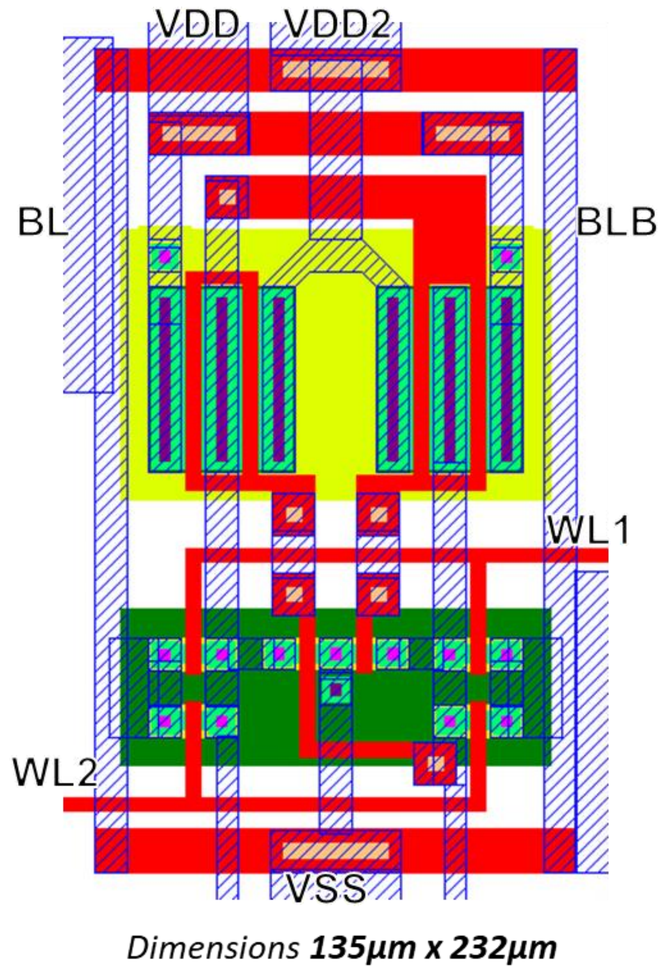

Fig. 14. Novel SiC SRAM cell layout in RUN #2.

4.3 High-Temperature Sense Amplifier Architectures

Voltage sense amplifier architectures are designed in RUN #2. A conventional CMOS latch type sense amplifier (shown in Fig. 8) and an improved latch type sense amplifier (shown in Fig. 15) were designed and characterized at high temperatures using a probe station.

The improved latch type voltage sense amplifier (Fig. 15) operates in two phases, charging and intentional discharging. In the first phase, the bitlines that are connected to SRAM cells are charged to VDD through Qp1, Qp2 and Qp3. In the second phase, the bitlines discharge through the SRAM cell depending on the data bit stored in that SRAM cell. The difference in the bitline

voltages is detected by the cross coupled connected inverters Qp8-Qn3 and Qp9-Qn4. The bitlines connected to Qp4 and Qp5 disconnect once the Qn5 transistor switches on. In a conventional sense amplifier, the bitlines completely discharge through the sense amplifier which result in long read times. However, in an improved latch type architecture the read times are lower because the bitlines does not discharge through the sense amplifier. The results measured at probe level for the improved latch type sense amplifier are shown in Fig. 16. The design is characterized from room temperature to 500°C. The pre-charge signal is asserted low for 30 µs to charge the bitlines to VDD. At room temperature the bitlines charging time is around 20 µs. As the temperature increases to 500°C the significant reduction in charging time is evident. The bitlines are connected to the 13 pF load of an oscilloscope that mimics the load of the bitlines when connected with the SRAM array. If the sense amplifier is connected with the SRAM cell the wordline signal should be triggered after the bitlines are charged to VDD. After the pre-charge cycle is completed, the Enable Signal (SE) is triggered high and the difference in the bitlines is detected by the cross-coupled inverter. The difference between the two bitlines is not visible in the presented data. But the decrease in BL signal over time indicated that the BL signal is lower than the BLB signal. Hence the OUT signal switched low when the SE signal goes high, OUTN is the complementary of OUT so it stays high.

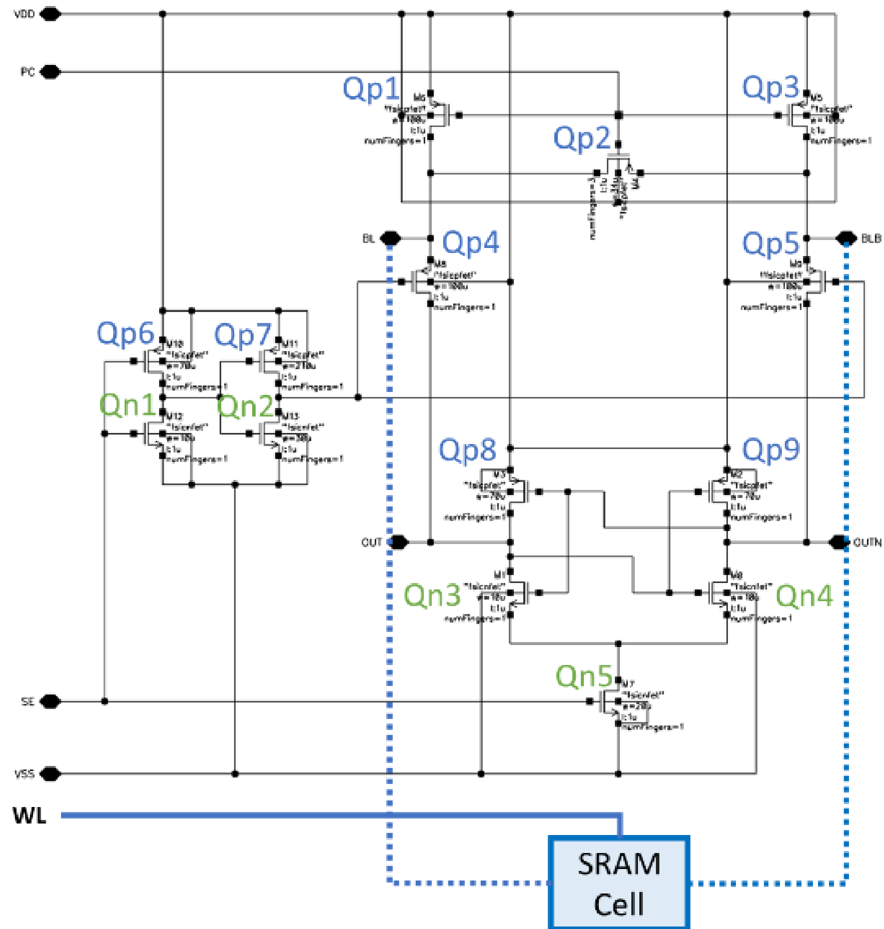

Fig. 15. Improved latch type sense amplifier.

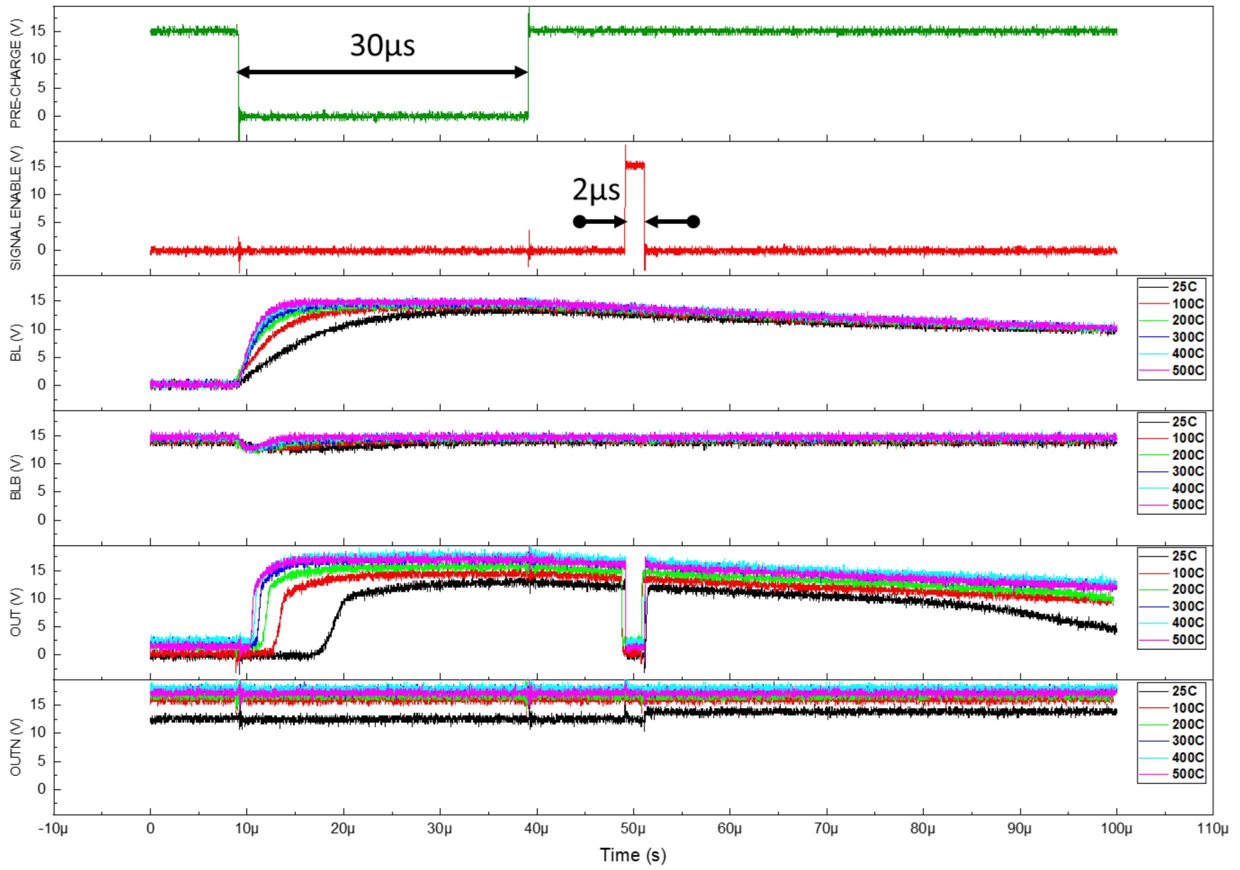

Fig. 16. Probe level measurements of an improved latch type sense amplifier.

5 Test-plan for SRAM & Sense Amplifiers

The testplan for the designed SRAM is of utmost importance. Therefore, a considerable amount of time was spent in the development of the testplans. Noise margin is the SRAM cell's most essential characteristic and is widely accepted as the Figure-of-Merit (FOM) across all the conventional and non-conventional process technologies. Hence, the SRAM cell design in RUN #2 is characterized for noise margins and data retention voltages (DRV). The RUN #2 wafers are comprised of multiple wafer splits, and an SRAM cell is characterized on all the splits except those deposited with platinum metallization. The cell is evaluated by three different noise margins, namely, Static Noise Margin (SNM), Read Static Noise Margin (RSNM), and Write Static Noise Margin (WSNM). The testplans are developed to characterize the SRAM cell and provide an in-depth understanding of the wafer splits and qualify the SiC process for the memory's design and development. Another vital piece of the testplan is understanding the cell's characteristics at high temperatures (500°C).

The test setup includes a probe station that has the capability of high-temperature measurements, Keysight's B1500 DC Curve tracer, and power supply. The high-temperature probe station is rated to operate from room temperature to 600°C. There is also a chiller connected with the probe station that helps regulate the set temperature, and it is also used for the rapid cooldown of the chuck. The test setup is shown in Fig. 17. The Device Under Test (DUT) is placed on the chuck and via manipulators connected to different equipment pieces. At high-temperatures, the manipulator's probe tip tends to increase in resistance because of oxidation; hence in this test setup, the resistance of the probe tips is checked every time the temperature is increased. The probe tips are replaced whenever their resistance increases above 0.5 Ω. At and above 200°C, the probe tips extend due to thermal expansion. Due to that, the probe positions that worked at room temperature

do not work and extend into the die, destroys the pads, and the die is not useful anymore. Therefore, before probing the die at high-temperature, probe tips are left floating for approximately ~ 20 minutes at 500°C to go through the thermal expansion process. The Keithley's B1500 DC curve tracer comprises six Source Measurement Units (SMU) and a Capacitance Measurement Unit (CMU). The SMU connected to the DUT inputs is configured as a voltage source while the SMU connected to the DUT output is configured as a current source to measure the voltage. A detailed and concise tutorial was also developed on how to use the B1500 DC curve tracer for this work and is included in Appendix B. This tutorial may help a new user understand the key features of the B1500 DC curve tracer's testing capabilities without going through the manufacturer's extensive manual.

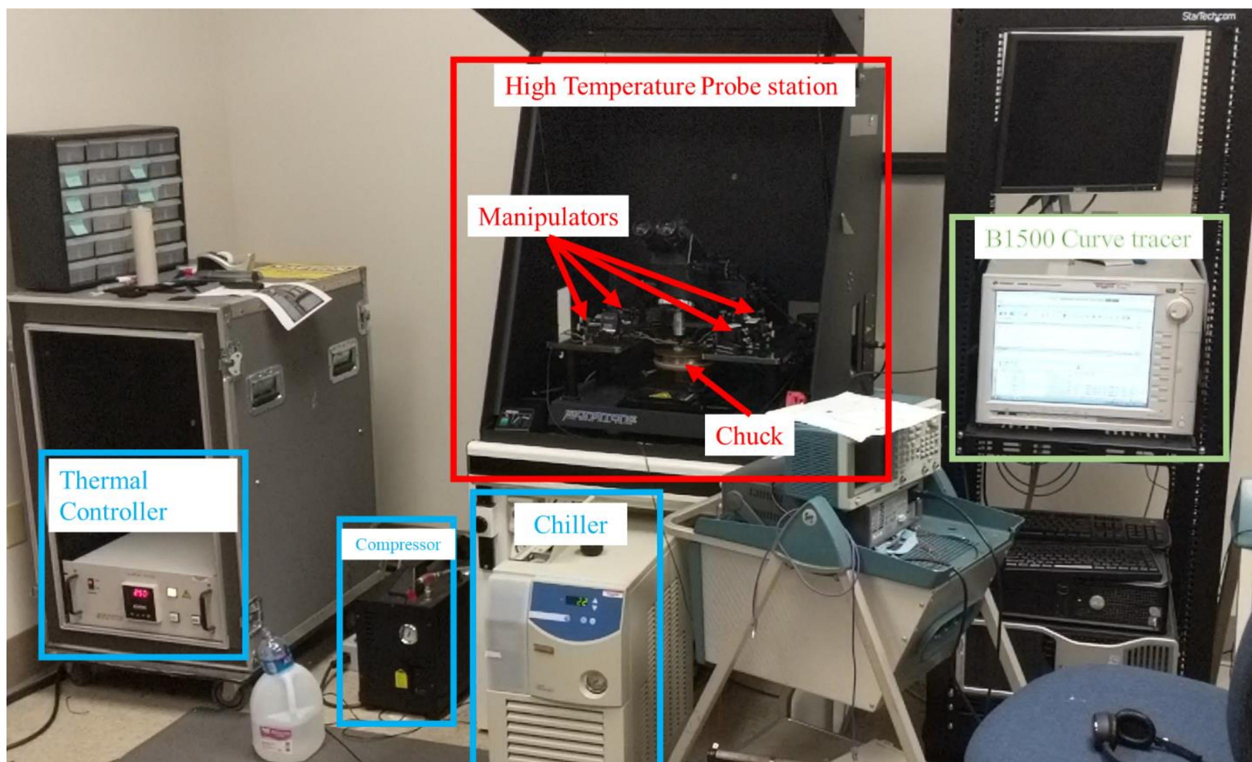

Fig. 17. High temperature probe level test setup.

5.1 Testplan for DC Characterization of the Memory Cell

As the proposed SRAM cell has two supply voltages, and two wordline signals (WL1 and WL2), the testplan is different than the usual SRAM testplan. For SNM, six testplans were developed. In testplan #1, VDD1 and VDD2 are set to a DC voltage of 20 V (later on 15 V and 10 V) and V1 is swept from zero to VDD as the output voltage is measured on V2. The rest of the I/O pins are shorted with VSS or set to zero volts. During testplan #1, the transistors and nets not contributing electrically in the SNM are gray, as shown in Fig. 18. The SRAM schematic during testplan #2 is shown in Fig. 19. V2 is swept from zero to VDD as the output voltage is measured on V1. The SNM parameter is extracted from the Voltage Transfer Characteristics (VTC) of an inverter. Since the SRAM cell has two inverters connected in a cross-coupled configuration, it is typically unnecessary to measure both the inverters separately in conventional process technology, allowing only one VTC curve to produce the SNM value. However, in the SiC process, it is essential to measure both inverter's VTC because of a single metal layer and process variability.

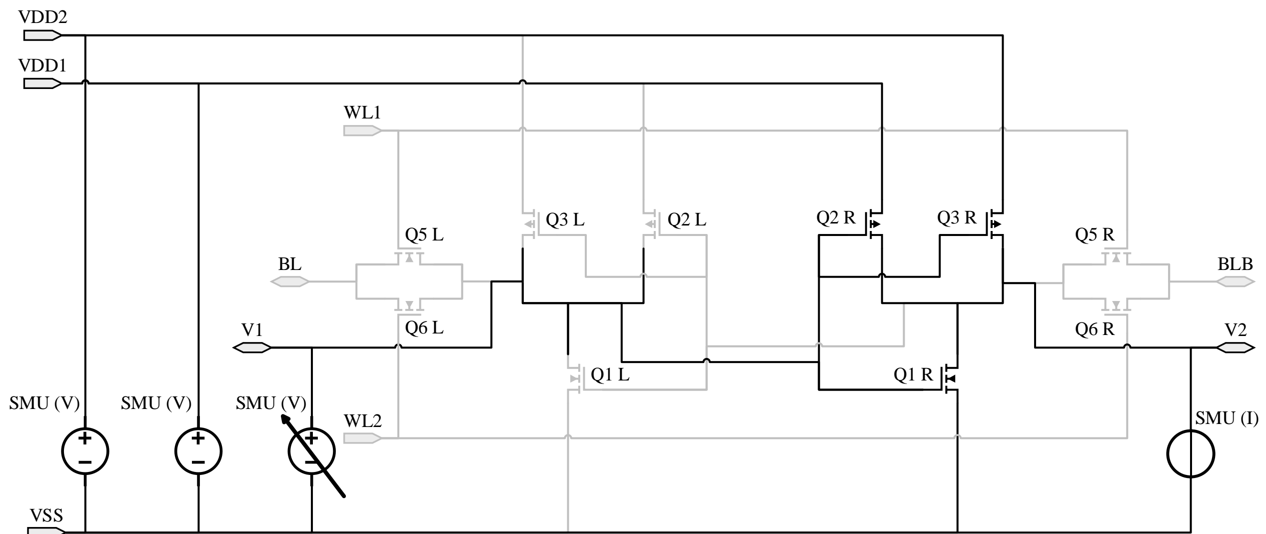

Fig. 18. SNM testplan #1, VTC of the right side inverter.

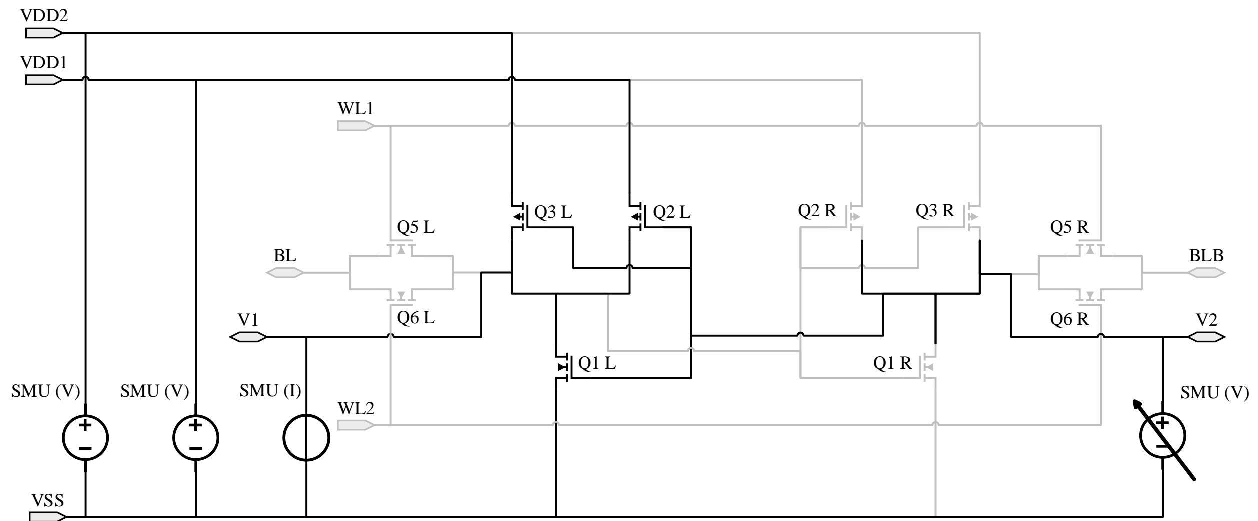

Fig. 19. SNM testplan #2, VTC of the left side inverter.

Testplan #3 and testplan # 4 are depicted in Fig. 20 and Fig. 21, respectively. Like testplan #1 and testplan #2, wordline I/Os and bitline I/Os are grounded. In addition to that, VDD2 is also set to ground which disables one PMOS in the schematic. It is expressed in Fig. 20 by setting the color to the gray of Q3 R. Similarly, in Fig. 21, Q3 L is not effective during the test.

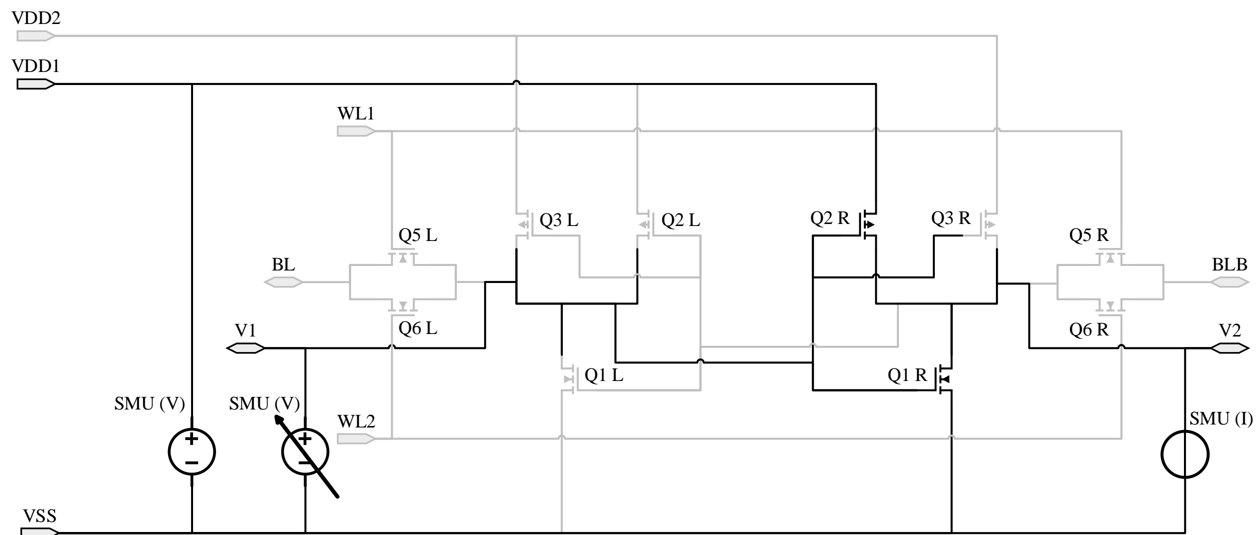

Fig. 20. SNM testplan #3, VTC of the right side inverter with only VDD1.

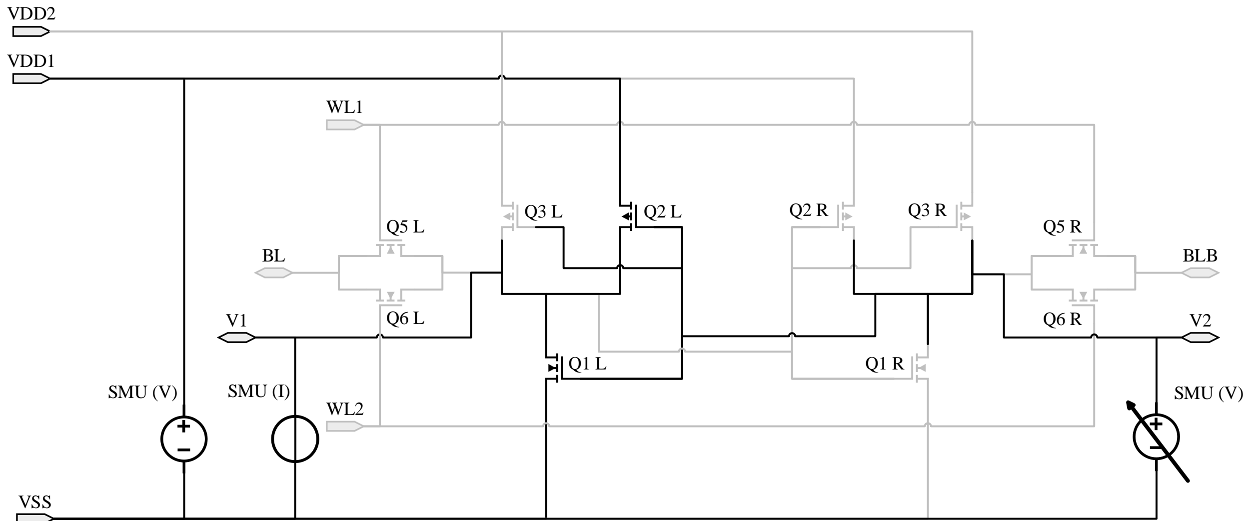

Fig. 21. SNM testplan #4, VTC of the left side inverter with only VDD1.

In testplan #5 and testplan #6, only VDD1 is set to ground along with the wordline and bitline nodes. VDD2 is connected with the voltage source that enables the PMOS that was disabled in testplan #3 and #4. Fig. 22 and Fig. 23 shows the schematic during testplan #5 and testplan #6, respectively. The SNM testplans are configured so that DRV can also be measured. The DC curve tracer is programmed to run the tests sequentially; first, it runs the test with a VDD of 20 V, followed by tests at 15 V, and 10 V. The measured data then post-processed to capture the DRV plots for SNM.

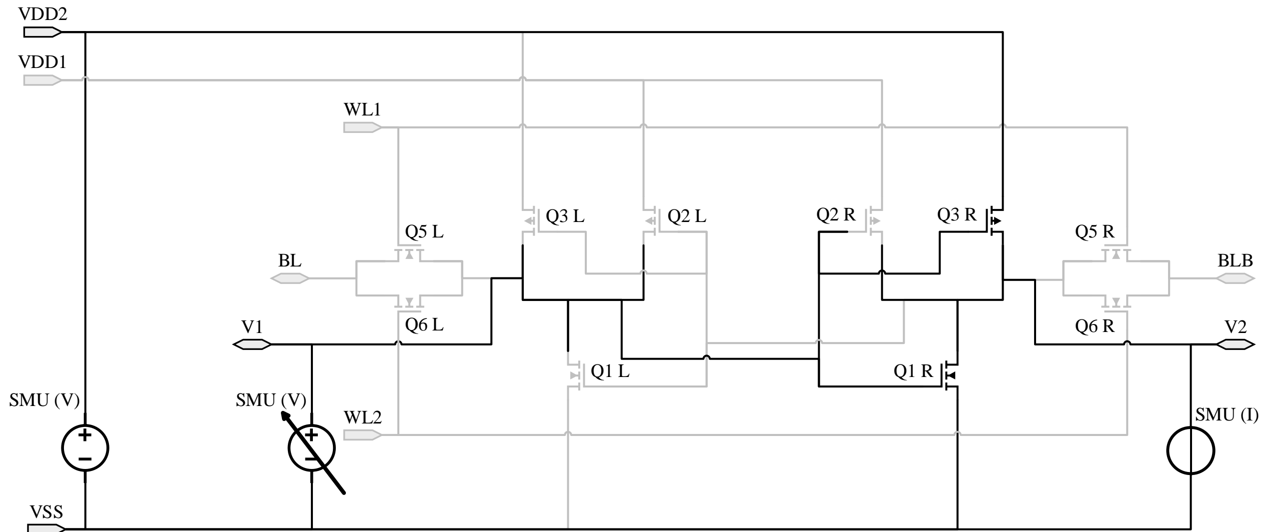

Fig. 22. SNM testplan #5, VTC of the right side inverter with only VDD2.

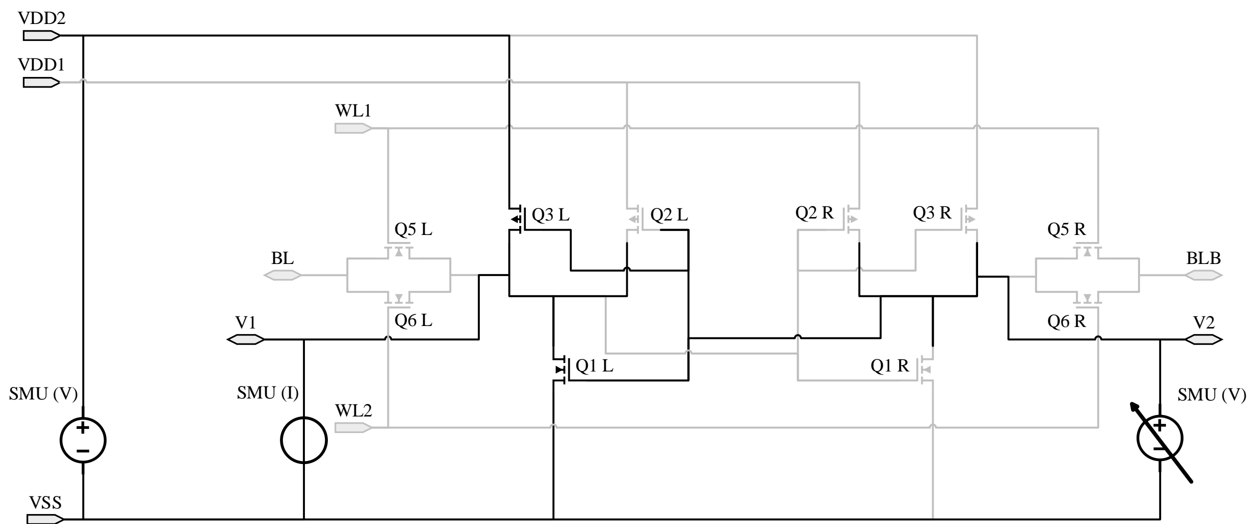

Fig. 23. SNM testplan #6, VTC of the left side inverter with only VDD2.

For the RSNM measurement of the right side of an SRAM, BLB is set to logic ‘1’ via SMU 5 and, BL is swept from ‘0’ to ‘1’ logic by SMU 4. The output voltage is measured at V2 by configuring SMU 4 as a current source. The current is set to zero, which acts as an infinite resistance on V2. The test setup to measure RSNM on the right side of the designed SRAM and all the possible configurations during the read mode are illustrated from Fig. 24 to Fig. 32. A similar test setup is implemented to measure the RSNM parameter from the left side of the SRAM.

Similarly, to the SNM testplans, the RSNM testplans are also configured to do DRV by programming the DC curve tracer. The measured data are then post-processed to capture the DRV plots for RSNM.

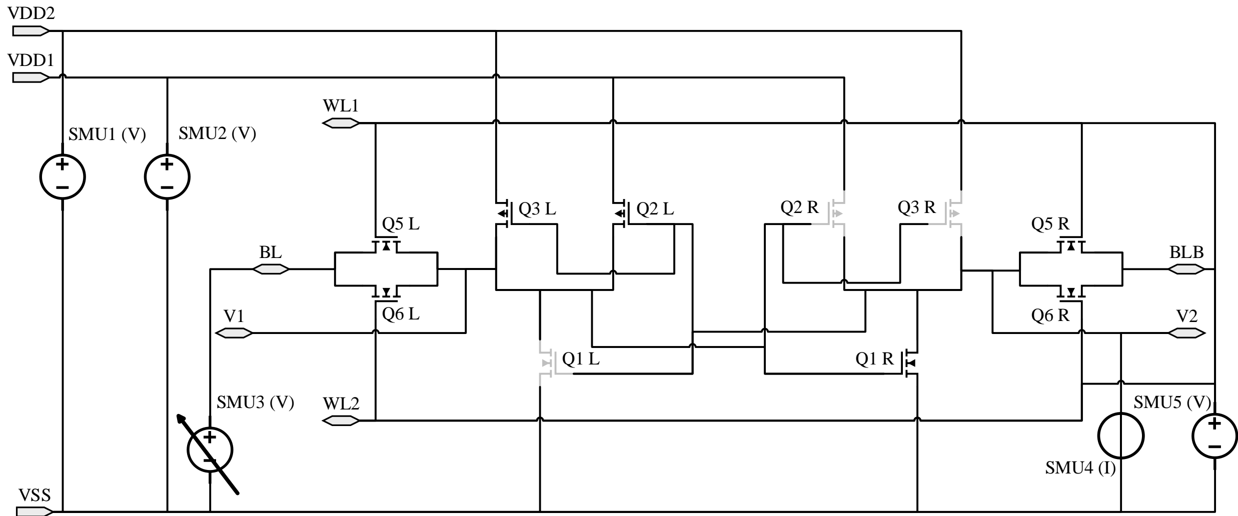

Fig. 24. RSNM testplan #1, right side with both wordlines active.

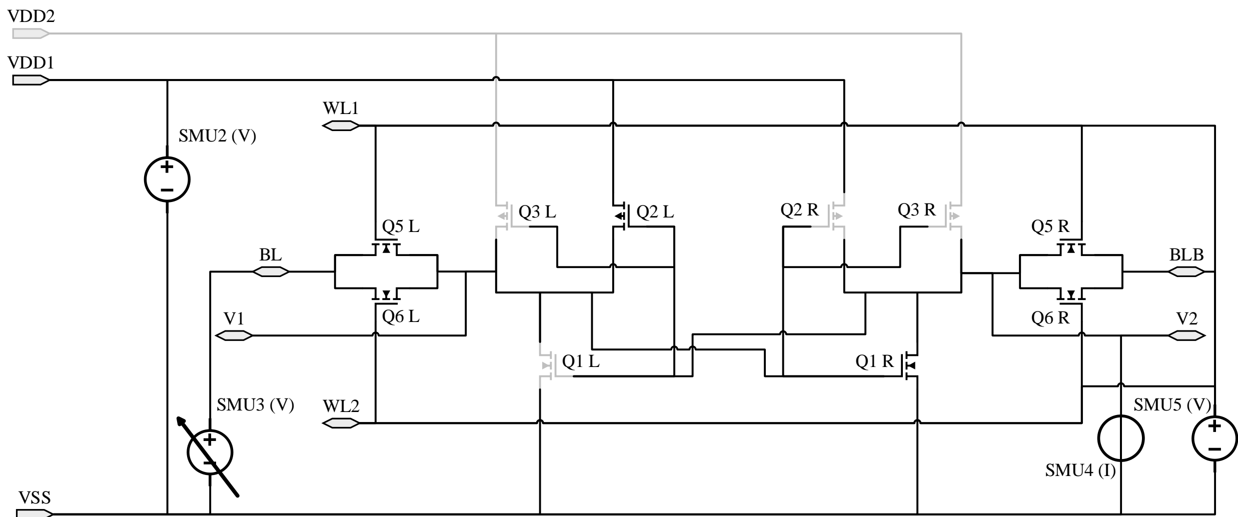

Fig. 25. RSNM testplan #2, right side with only VDD1, both wordlines are active.

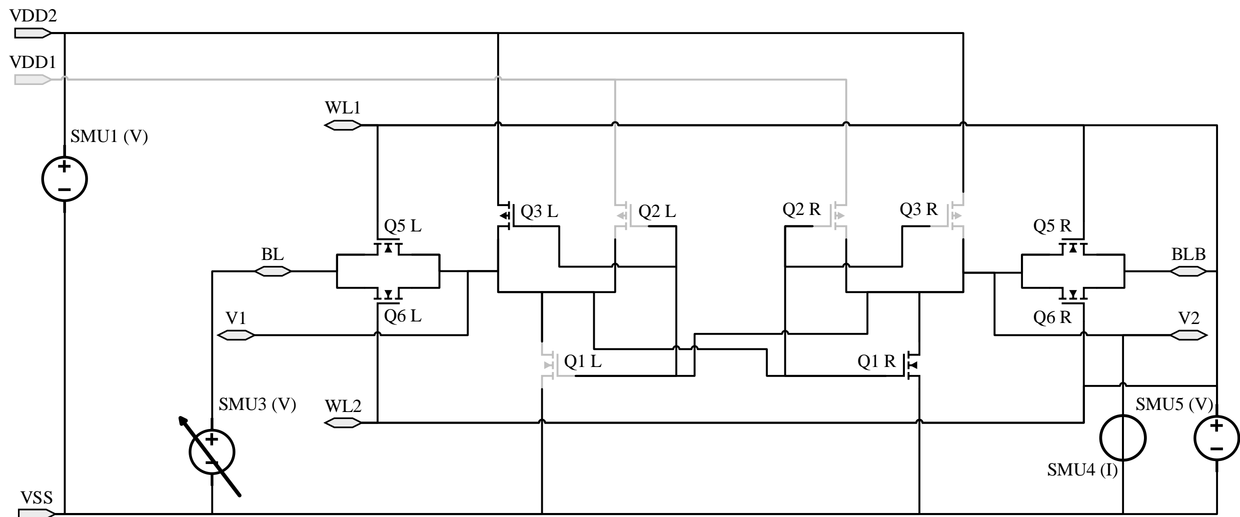

Fig. 26. RSNM testplan #3, right side with only VDD2, both wordlines are active.

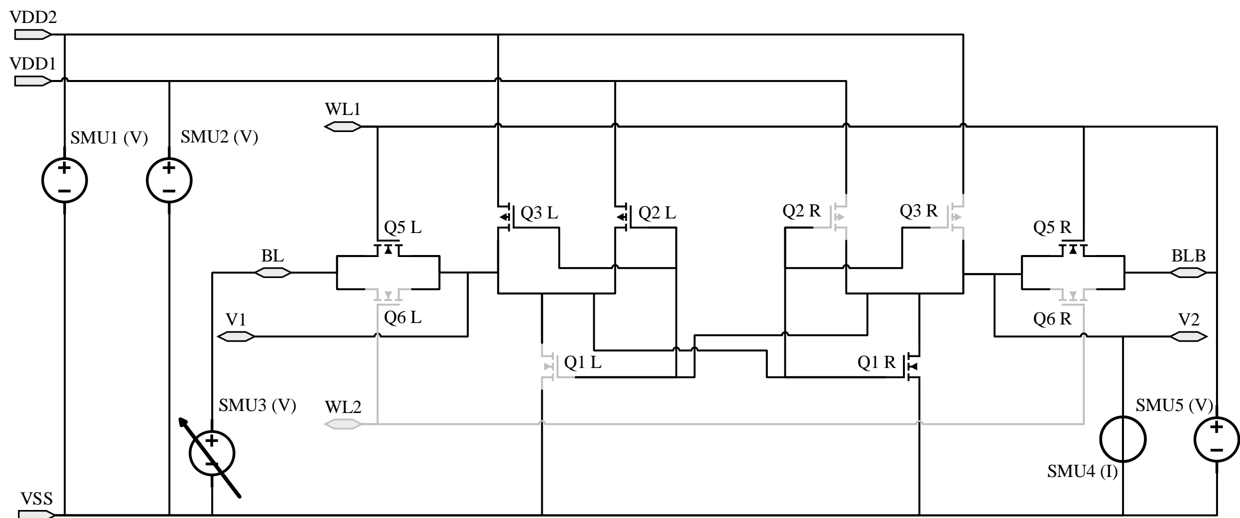

Fig. 27. RSNM testplan #4, right side with only WL1 active.

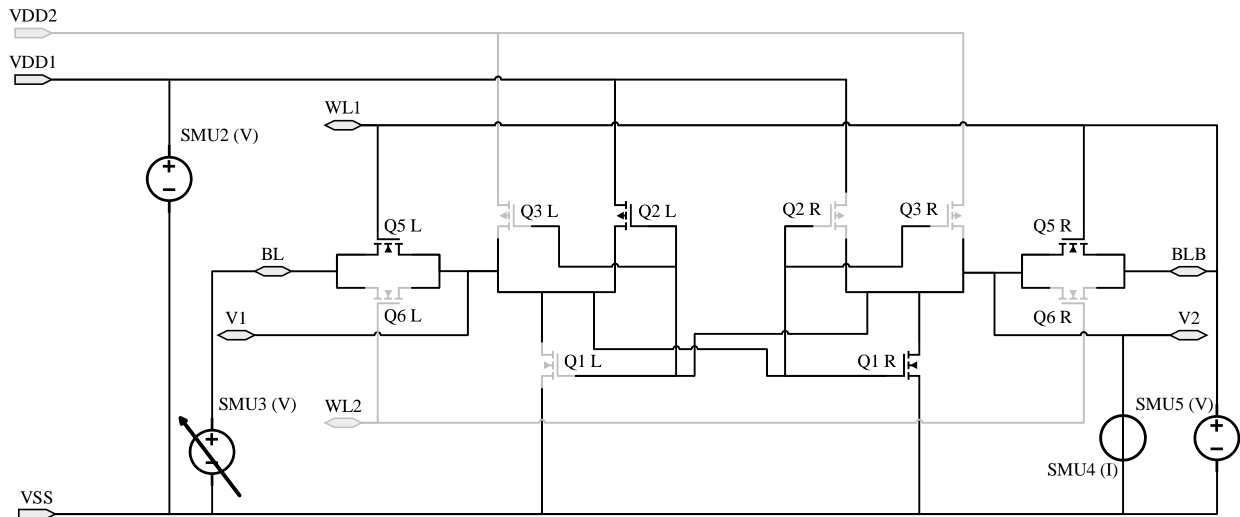

Fig. 28. RSNM testplan #5, right side with only WL1 and VDD1 active.

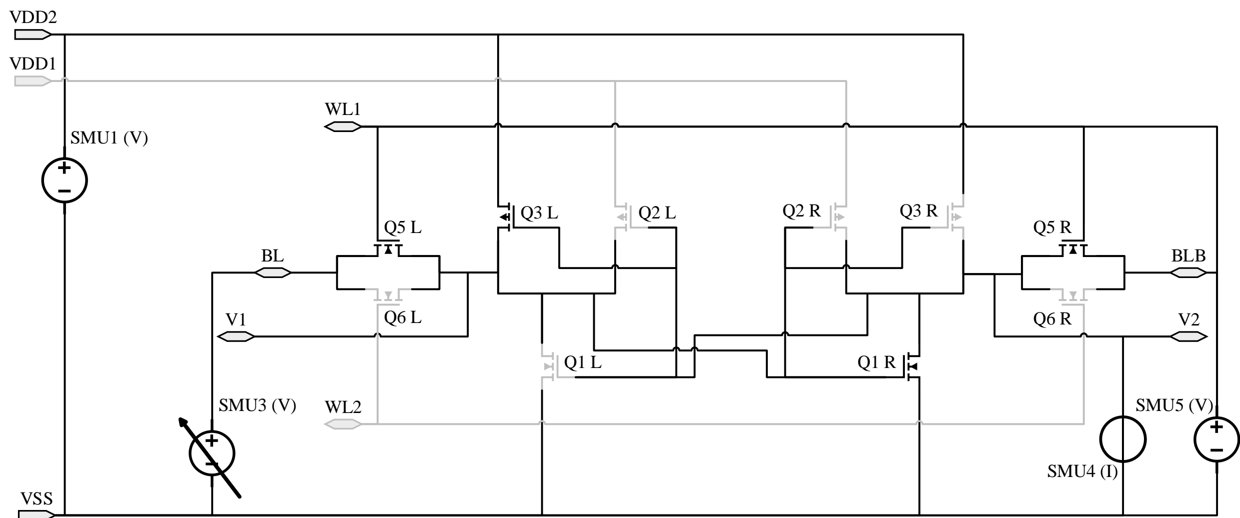

Fig. 29. RSNM testplan #6, right side with only WL1 and VDD2 active.

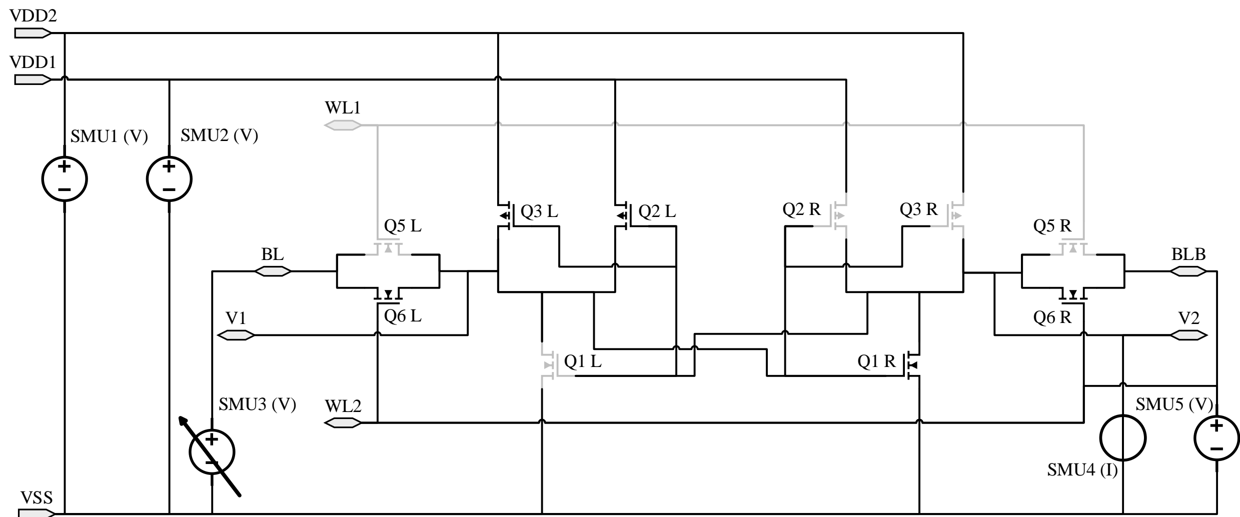

Fig. 30. RSNM testplan #7, right side with only WL2 active.

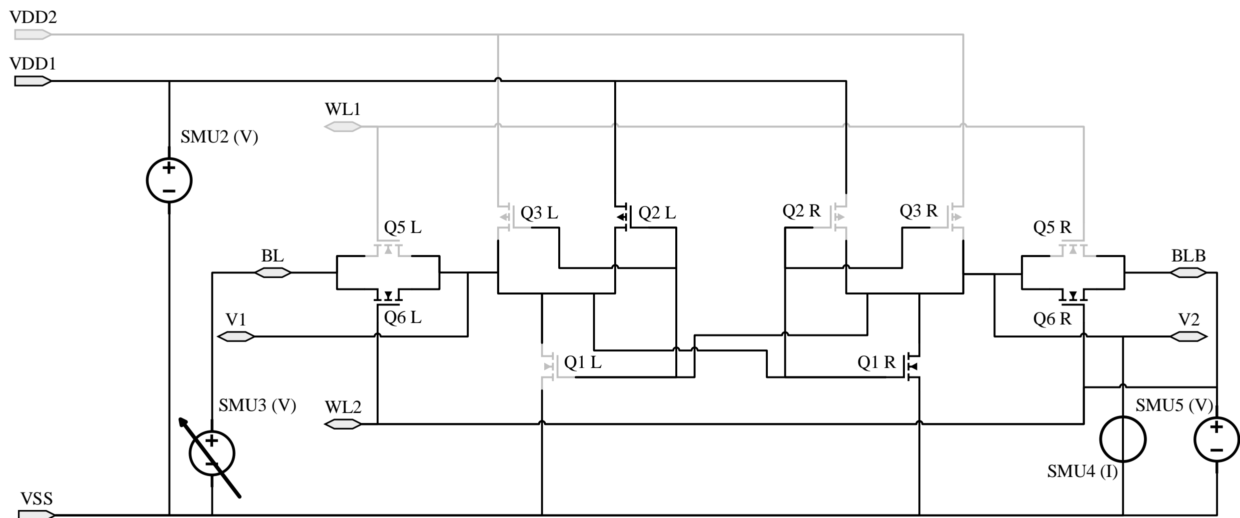

Fig. 31. RSNM testplan #8, right side with only WL2 and VDD1 active.

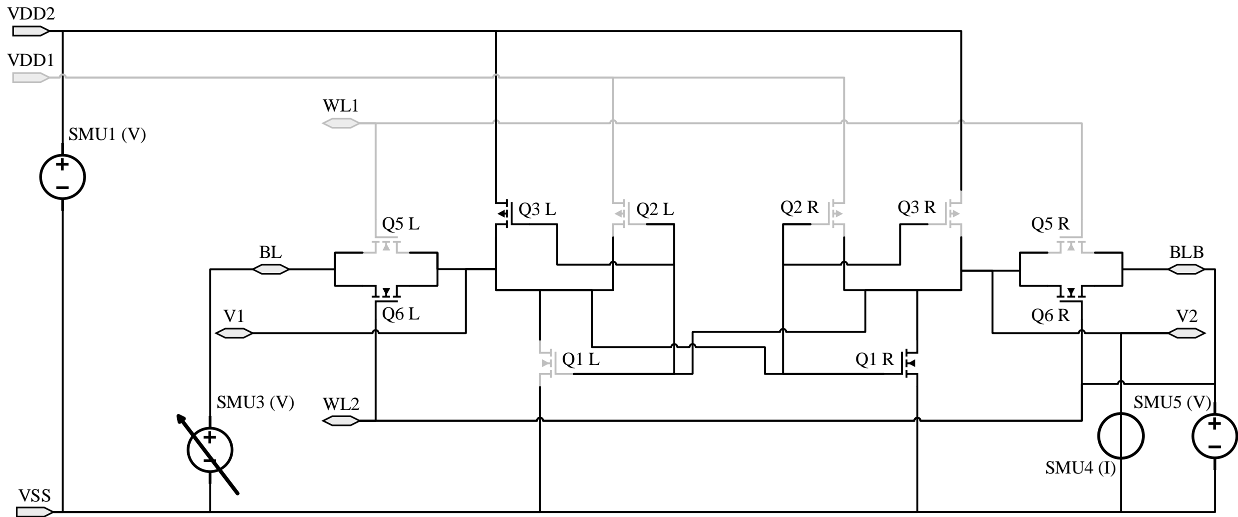

Fig. 32. RSNM testplan #9, right side with only WL2 and VDD2 active.

The WSNM test setup is similar to the RSNM test setup; except that BLB is tied to logic '0' when measuring the write margin of the right side of the cell, as shown in Fig. 33. BL is also swept from logic '0' to '1' via SMU 3, and the output is measured at V2. All the other possible test setups and configurations are similar to RSNM testplans, and therefore, they are omitted here. The DC curve tracer is also programmed in WSNM testplans to capture the DRV data, and later post-processed to obtain DRV for WSNM.

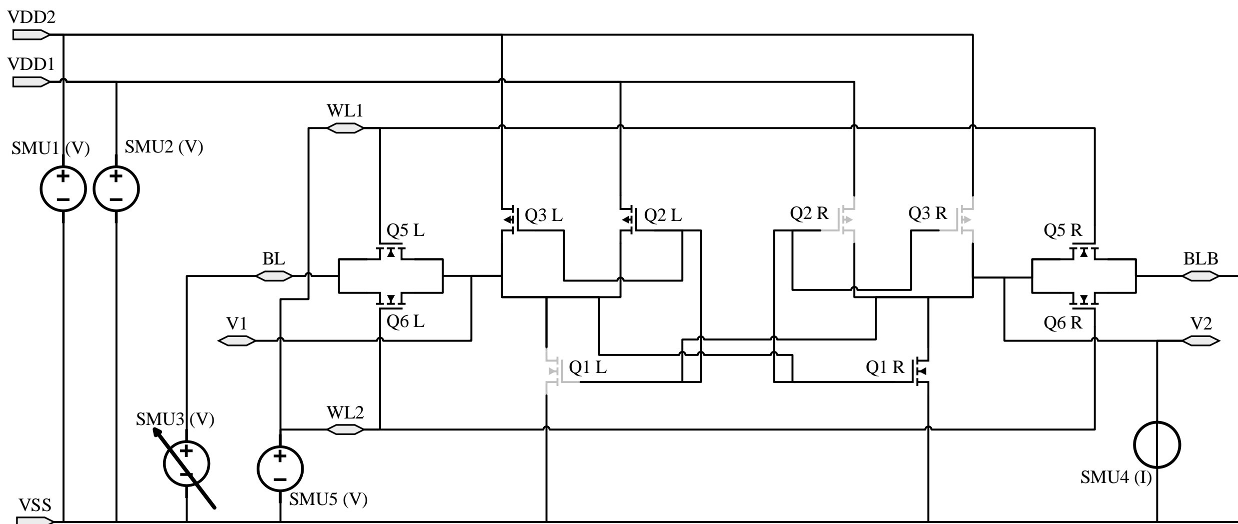

Fig. 33. WSNM testplan #1, right side with both wordlines active.

5.2 Test-plan for the Sense Amplifiers

To check the functionality of two different types of sense amplifiers, two testplans are created. The testplan for the first architecture is shown in Fig. 34, along with the test setup. The test is performed on the high-temperature probe station; other pieces of equipment used in the test setup are the function generator, power supply, and oscilloscope. The function generator has two channels; channel 1 is used to generate a pre-charge (PC) signal, a 30 µs active low pulse, and channel 2 generates a short 5 µs active high pulse for sense enable (SE) port. The function generator is programmed to assert PC pulse first and then adds a delay of 10 µs, afterward assert a SE pulse. The delay of 10 µs between the two pulses is enough to generate a difference in the voltages at BL and BLB nodes, latching the cross-coupled inverters.

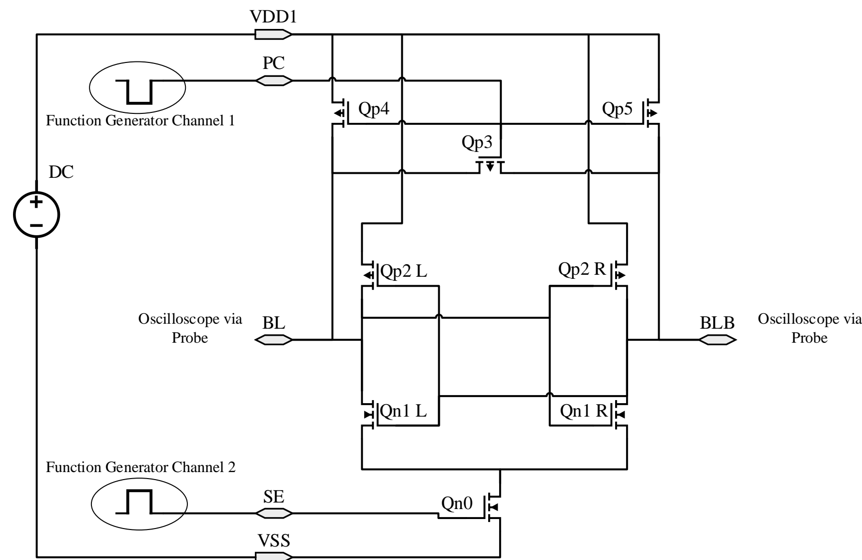

Fig. 34. Test setup for conventional sense amplifier.

The second architecture is the improved variant for the conventional sense amplifier. In its test setup, active probes are used at the output ports because they are connected to the cross-coupled inverters. The rest of the equipment and their settings are the same as mentioned in the

previous testplan. The test setup for the improved conventional sense amplifier is shown in Fig. 35.

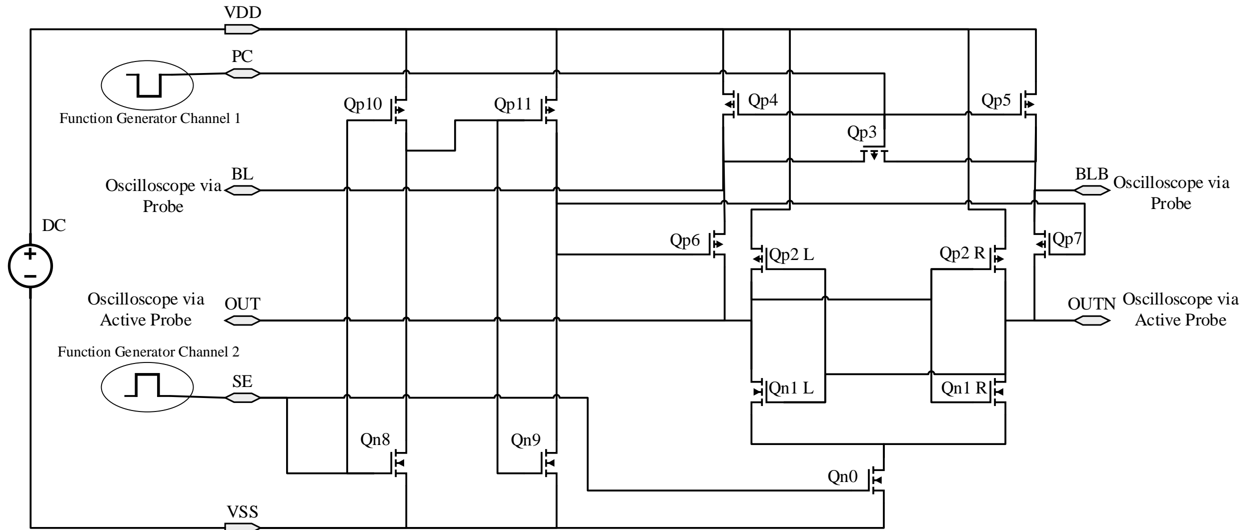

Fig. 35. Test setup for improved conventional sense amplifier.

5.3 Test-plan for the Transient Characterization of the Memory Cell

Generally, the SRAM cell's transient characteristics are performed with the sense amplifier, and the data write buffers. The data write buffers are used to set complementary logic ‘1’ or ‘0’ on the two bitlines; e.g., if the user wants to write ‘1’, the data write buffer assert logic ‘1’ on BL and logic ‘0’ on BLB; vice versa if the user wants to write ‘0’. The data write buffer circuit is not implemented in this work; instead, a power supply is used to toggle the bitlines that perform the write operation. The write operation is straightforward and does not impose any difficulty and challenge in the design and implementation. On the contrary, the read operation is challenging because there is a possibility of flipping the data. Hence, care must be given to the read operation.

The read operation is performed through the sense amplifier. The improved variant of the sense amplifier is used with the SRAM cell to test the read operation. The SRAM cell and sense amplifiers are die attached and wirebonded on two different 68-pin quad flat package (QFP) leaded

chip carriers (LDCC). Afterward, these packages are soldered to the Rogers board. The hotplate is used to characterize the system at high temperatures. The targeted temperature is 500ºC, but the Rogers board and the solder cannot sustain this high temperature. A cutout is made in the center of the Rogers board, and heat is applied directly to the chip carrier through a copper finger that is placed on the hotplate.

The electrical test setup includes the power supply, two function generators, oscilloscope, multimeter, and a computer. The power supply is used to apply DC voltage to the cell and the amplifier. The two wordline signals for the SRAM cell are generated from the function generator. Both channels of the function generator are set to trigger 2 µs active high pulse at the same instance. The signal enable, and pre-charge signals are generated the same way as mentioned in section 5.2. The trigger option in the function generators is used to synchronize these four signals. The pre-charge signal asserts first for 25 µs, the wordline signals assert after a delay of 5.05 µs and in the last signal enable goes high for 10 µs after a delay of 1 µs. The timing sequence to execute the read operation is shown in Fig. 36.

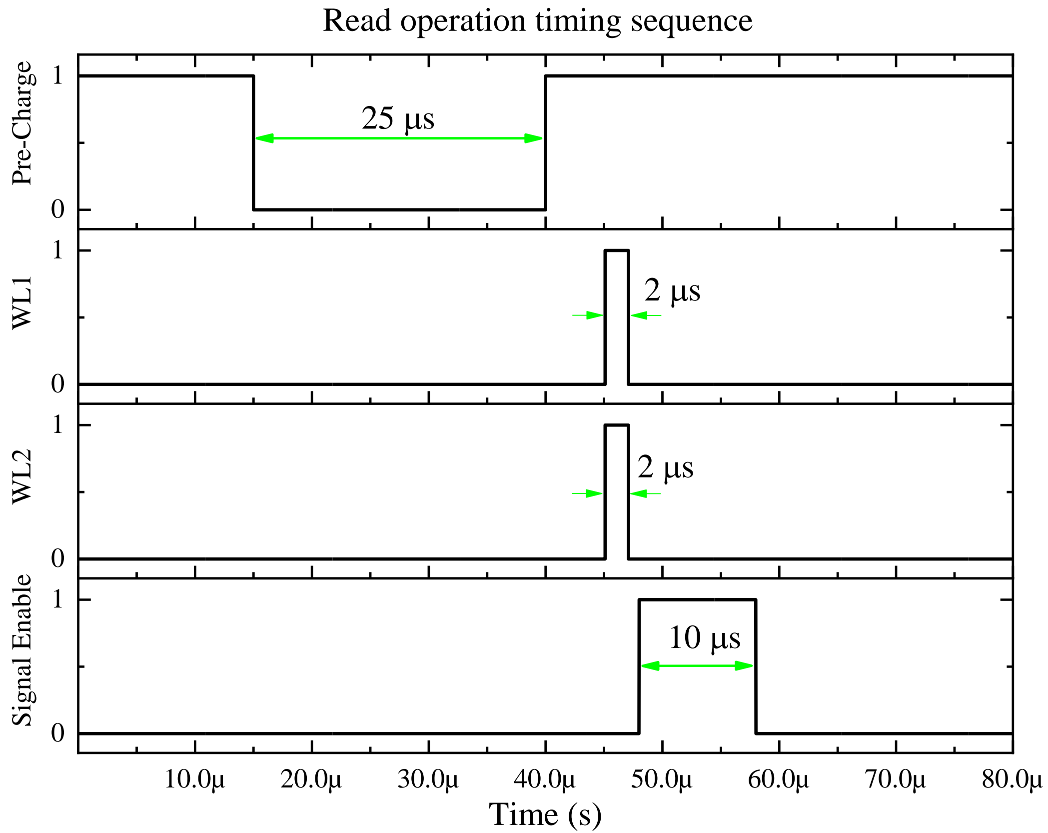

Fig. 36. The timing sequence of the signals required for the read operation.

The SRAM and sense amplifier signals such as two wordlines, pre-charge, signal enable, bitlines, and output signals are monitored on the oscilloscope. The oscilloscope used in this test setup has four analog channels and 16 digital channels. Therefore, to see all the signals, both analog and digital ports are used. The signals generated from function generators are monitored on the digital ports, and the bitlines and output signals are monitored on the analog channels. This test setup requires many jumper wires and connections; thus, a multimeter is used to check the connectivity and voltage levels at different test setup points to ensure that the connections are fine. The desired parameters from this test setup are the read access time and the output voltage levels. The illustration of the test setup is shown in Fig. 37. And the actual test setup is shown in Fig. 38.

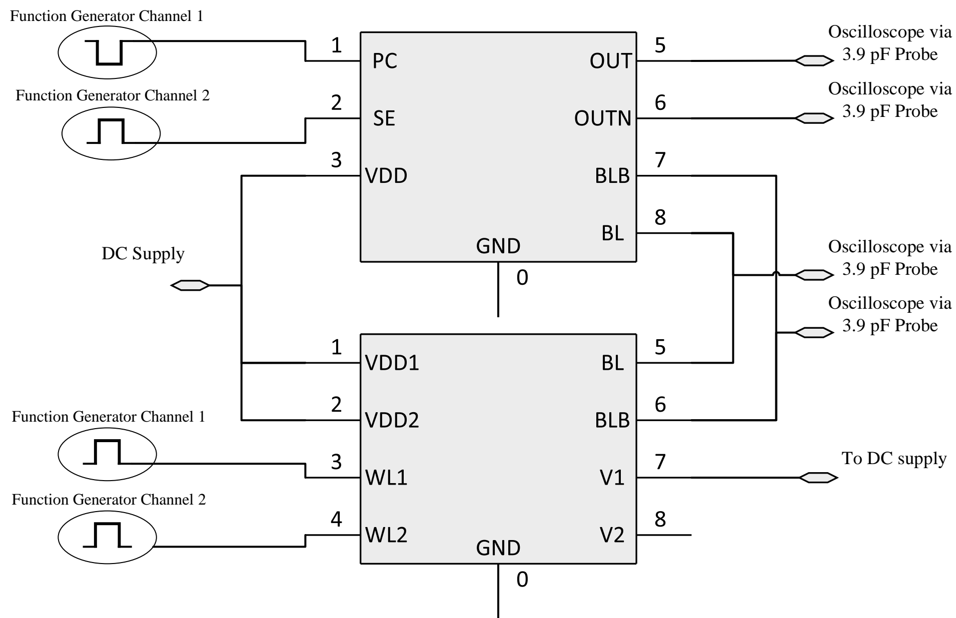

Fig. 37. The illustration of test setup for transient characterization.

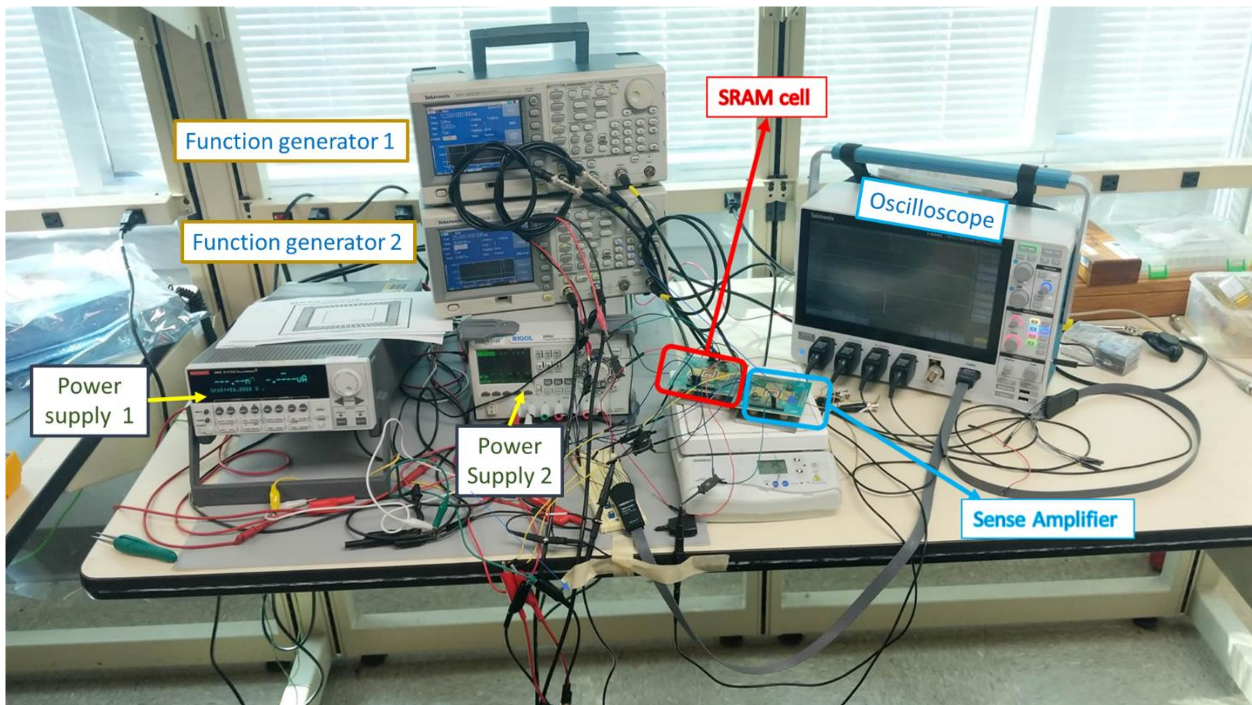

Fig. 38. The actual test setup for transient characterization.

6 Results and Analysis

The results obtained from the testplans explained in the previous chapter are presented in this chapter. This chapter includes the DC and transient characteristics for the proposed SRAM design. The sense amplifier performance influences the SRAM's transient characteristics; hence, it is the memory module performance evaluation and not only the SRAM.

6.1 Static Noise Margin

The discussion of SNM testplans included in chapter 6 is summarized in Table 7. The SNM is measured for three uniquely processed wafers, with voltage levels of 20 V, 15 V, and 10 V. Furthermore, each voltage level is further evaluated at 25°C, 250°C, and 500°C for all three wafers.

Table 7. The Summary of the SNM Testplans

	VDD1	VDD2	V1	V2	WL1,WL2,BL,BLB
Testplan #1 (TP1)	ON	ON	V sweep	V Out	NC
Testplan #2 (TP2)	ON	ON	V Out	V sweep	NC
Testplan #3 (TP3)	ON	OFF	V sweep	V Out	NC
Testplan #4 (TP4)	ON	OFF	V Out	V sweep	NC
Testplan #5 (TP5)	OFF	ON	V sweep	V Out	NC
Testplan #6 (TP6)	OFF	ON	V Out	V sweep	NC

NC=No connection

SNM plots are very well adopted for graphical analysis of the SRAM. It shows the tolerance of an SRAM cell to noise before it risks losing the memorized bit. SNM is a straightforward measurement that can be represented with just one number, which means that it does not identify any dynamic noise that may have flipped the bit. But, since it is just one number, it is easy to compare values and get a feel when the SNM operating conditions might cause trouble to the stored bit. The SNM for the SRAM is measured from the two back-to-back inverters. Both the inverters are characterized for their Voltage Transfer Characteristics (VTC). The VTC from the first inverter is plotted as VOUT vs. VIN, where VOUT is on the y-axis, and VIN is on the x-

axis. The axes are swapped for the VTC of the second inverter; VOUT is on the x-axis, and VIN is on the y-axis. The diagonal of the largest square that fits within the back-to-back DC characteristics is the value of the SNM. Since the SRAM design reported in this work is in an emerging process, it is significantly more prone to Process Voltage Temperature (PVT) variations. Also, the harsh conditions such as 500°C operating temperatures are beyond the SRAM cell's capability that is achievable in a conventional silicon process. Therefore, the VTC of the two inverters are not symmetric. The SNM value is measured from the smallest of the two possible squares (one on each side of the cross-over point).

The SNM plot shown in Fig. 39 compares the results between wafer 2, wafer 4, and wafer 6 at room temperature with a VDD of 20 V. The plot is created from the TP1 and TP2 data. Ideally, the cross-over point is at the mid-level of the supply voltage. Wafer 6 SNM is very close to the ideal plot since it is the closest wafer split to the PASS0 wafers. Furthermore, the device models used for the PASS1 tapeout were developed from the PASS0 devices. Wafer 4 and Wafer 2 were deposited with P-type poly to increase the NMOS threshold and decrease the magnitude of the PMOS threshold. Hence, the shift in the cross-over point due to the threshold is prominent in Fig. 39. The center point for the SNM of wafer 2 and wafer 4 shifts towards VDD, which means the PMOS threshold has decreased and the NMOS threshold increased. The NWELL doping between wafer 2 and wafer 4 is slightly different, which created a minor change in the center point between the two wafers. Based on the results shown, the PMOS threshold on wafer 2 is lower than the PMOS threshold on wafer 4, and the NMOS threshold is similar for both wafer 2 and wafer 4 because there was no change in the PWELL doping concentration.

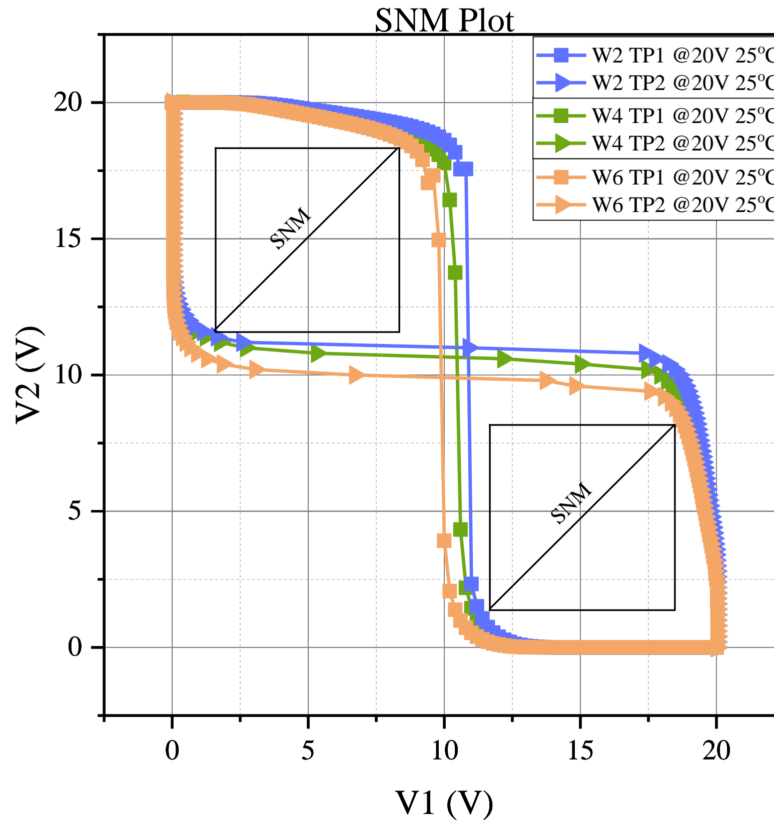

Fig. 39. SNM plots from TP1 and TP2.

The value of the SNM is calculated by rotating the plot (i.e., Fig. 39) 45° counterclockwise. The data is converted to the polar coordinates by using Eq. (1); and to rotate the data, 45° is added to the converted theta. Finally, the data is converted back to Cartesian coordinates by using Eq. (2). The 45° rotated data is shown in Fig. 40. The difference between the minima and maxima is the value of the SNM [32]. MATLAB is used to automate the data rotation, and the code is shown in the Appendix C.

$$r = \sqrt{x^2 + y^2} \qquad \theta = \tan^{-1}\frac{y}{x} \tag{1}$$

$$x = r * cos\theta \qquad y = r * sin\theta \tag{2}$$

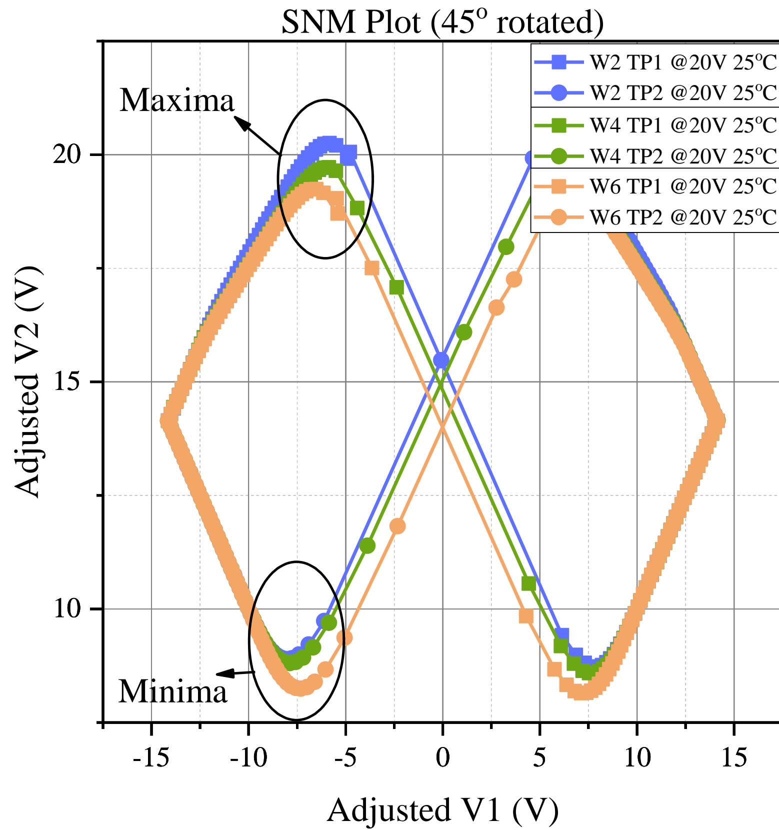

Fig. 40. 45° rotated SNM plot.

The data captured from TP1 and TP2 at 250°C and 500°C with a VDD of 20V are shown in Fig. 41. The SNM plots at 500°C have never been reported in the literature. The high-temperature data is measured at 500°C first and then at 250°C. For wafer 6, the cross-over point moves upwards with the increasing temperature. However, the cross-over point for wafer 2 and wafer 4 does not follow a similar trend, even though these wafers encounter a similar threshold shift as seen in wafer 6. The test conditions are the same as the sample die from each wafer are placed side-by-side and tested together.

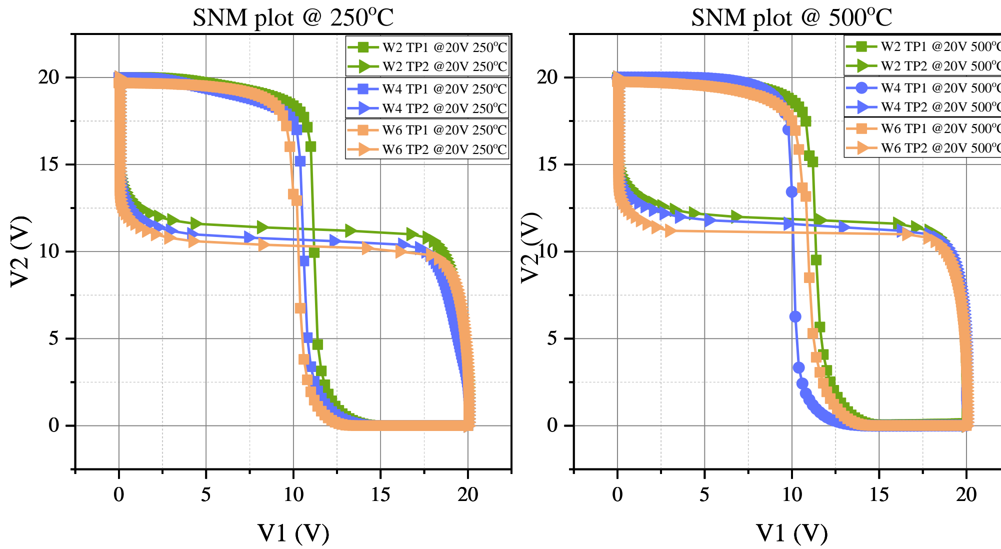

Fig. 41. SNM plot at 250°C and 500°C.

The difference in the trend is due to the failure of wafer 2 and wafer 4 devices at 250°C. All three wafers worked at 500°C for at least 3 hours, but wafer 2 and wafer 4 stopped working after temperature cycling. Hence, at 250°C new die from wafer 2 and wafer 4 were used for the characterization. This failure's potential cause is the poly module because this is the first time the foundry processed a P-type poly in their SiC process. Wafer 6 was deposited with an N-type poly module, and the foundry is using it widely in its SiC processes. Thus, after temperature cycling, wafer 6 did not show any signs of failure. The high-temperature SNM data from TP1 and TP2 is shown in Table 8, analyzed from the MATLAB code.

Table 8. Temperature Dependency on SNM at VDD =20 V

	25°C	**250°C**	**500°C**
Wafer 2	11.35	10.46	10.16
Wafer 4	10.91	10.21	9.21
Wafer 6	10.99	10.54	10.42

The SNM data from TP3 and TP4, at a VDD of 20 V for Wafer 6 are shown in Fig. 42. The region of interest highlighted in the figure is due to the poor P-type contacts. If the P-type contacts are ohmic, then the SNM plot in Fig. 42 must look like the SNM plot shown in Fig. 39.

In this process, the P-type MOSFETs performance is significantly impacted by the non-ohmic contacts. Due to this, a significant voltage drop across the PMOS's source to drain is evident. Therefore, to overcome the contacts' non-ohmic behavior, an additional PMOS transistor is added in the SRAM cell, which makes this cell unique and adds the flexibility to control the SNM of the cell.

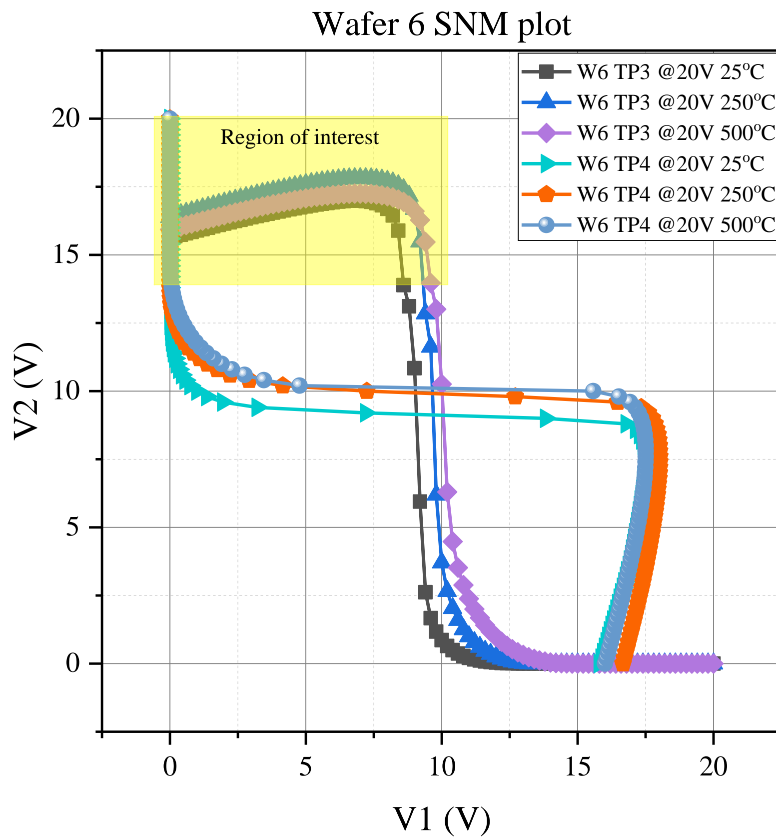

Fig. 42. SNM plot from Wafer 6 at a wide range of temperatures.

Interestingly, the voltage drop in the region of interest is reducing with the increase in V1 voltage. The general understanding is that the voltage drop due to non-ohmic contacts are constant; however, the results shown in Fig. 42 contradicts this assumption. One way to investigate this change is to use MOSFET square law equations but deriving these equations to account for the

poor p-type contacts is tedious and not worthy of an effort. The second option is to use the device models that can incorporate the non-ohmic contacts of the PMOS. The foundry provided the SPICE models generated through TCAD; this model's general approach is described in [33]. The output curve of the PMOS from the model is shown in Fig. 43. The model can show the Schottky behavior in the cut-off and linear region of the PMOS. Since these models are generated from TCAD, they are good for observing different fabrication effects such as doping concentrations on the MOSFET's I-V characteristics. The other known limitations of this model are that there is no model for the body diode, the subthreshold region is overestimated, and there is no model for the gate leakage current. Furthermore, no noise characterization is modeled, and no dynamic characteristics such as gate-drain and gate-source are modeled either. In addition to that, these models are developed for 6 µm channel length devices. Hence, these models are not much use for circuit-level simulations. Regardless of all the limitations in the models, an LTspice simulation for the SRAM cell is created to reproduce the measured results. The channel length used in the simulation is 6 µm, but the transistors' width is increased to reflect the same PMOS to the NMOS ratio in the fabricated cell. The simulation results are shown in Fig. 44. The V2 voltage is the VTC of an SRAM cell and as expected, due to the model limitations, results similar to the measured data could not be reproduced; as the voltage drop is only evident at a V1 of 3 V up to the cross-over point.

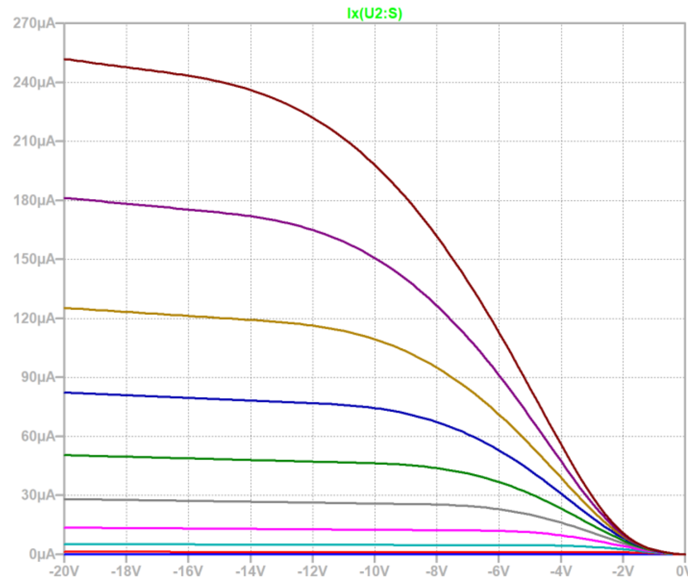

Fig. 43. PMOS Output curve at 25°C from foundry provided model.

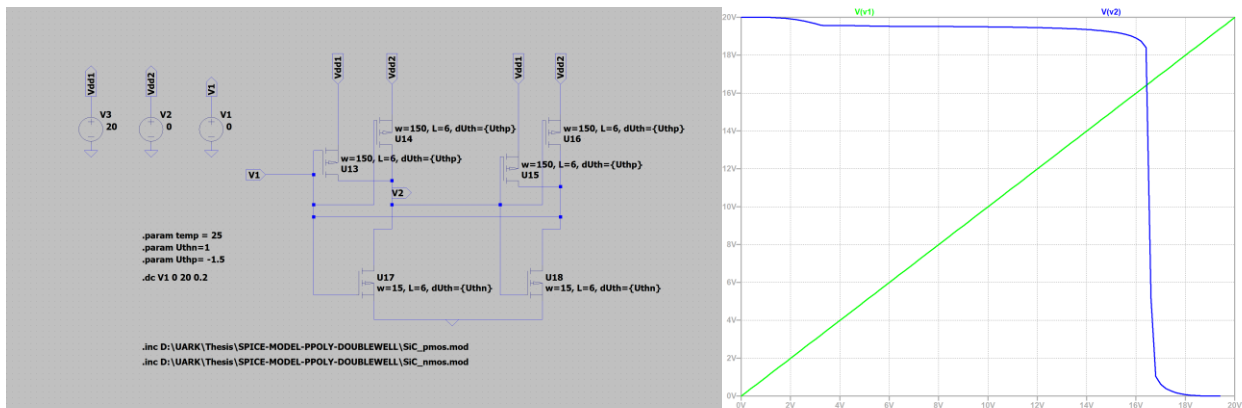

Fig. 44. Testbench and VTC results from foundry provided SPICE models.

To explain the voltage drop in the SNM plots, the graphical method to generate the VTC is adopted [34]. The nature of the VTC can be deduced by superimposing the PMOS and NMOS I-V characteristics. Such representation is called a load-line plot. The I-V characteristics of the PMOS is transformed onto the NMOS coordinates. The input voltage V1 and the output voltage V2 and NMOS drain current I_D are selected as the variables. The PMOS I-V can be translated into these variables by following the set of equations mentioned below:

$$I_D(PMOS) = -I_D(NMOS)$$

$$V_{GS}(NMOS) = V1\,; V_{GS}(PMOS) = V1 - VDD$$

$$V_{DS}(NMOS) = V2\,; V_{DS}(PMOS) = V2 - VDD$$

The load-line curve for the PMOS is obtained by mirroring about the x-axis and by a horizontal shift over VDD. This procedure is outlined in Fig. 45.

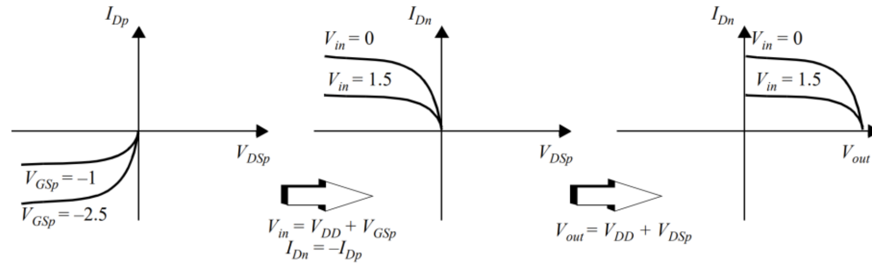

Fig. 45. Transformation of PMOS I-V to common coordinate set [34].

After superimposing PMOS I-V data to the common coordinates to NMOS, the obtained plot is shown in Fig. 46. The PMOS and NMOS data is adjusted to fit the transistor size used in the SRAM cell. The PMOS size is 50 µm / 2 µm and NMOS size is 5 µm / 2 µm in the cell. The test structures for PMOS and NMOS measured for this analysis have the size of 20 µm / 2 µm. Therefore, the 20 µm / 2 µm data is scaled to match the transistors size of the cell. The PMOS data is multiplied by 2.5 and the NMOS data is divided by 4 with the consideration that the device characteristics scale linearly with the width of the transistor.

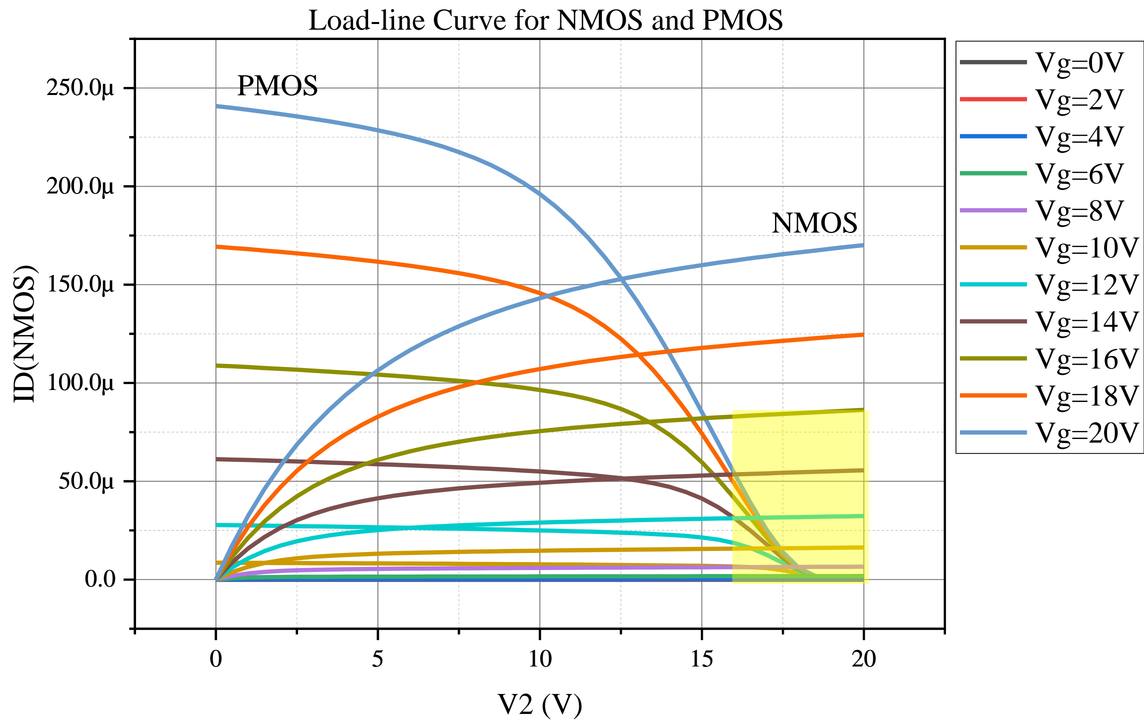

Fig. 46. Load curves for NMOS and PMOS transistors. The yellow region represents the effect of poor p-type contacts in PMOS.

For the DC operating points to be valid, the currents through the NMOS and PMOS devices must be equal. This means that the dc points must be located at the intersection of corresponding load lines. As can be observed in the highlighted region in Fig. 46, the PMOS cut-off region is at zero current for about 2 V due to the non-ohmic contacts. The intersection points in the highlighted region for Vg = 0, 2, and 4 of an NMOS are occurring at almost zero currents, and the current conduction in PMOS is starting around 18 V. Although the I-V data is adjusted to the size of the cell, it is sufficient to show the reason of the voltage drop in the measured data. Graphically, all the observations extracted from the load-line plot are translated into the VTC, shown in Fig. 47. The extracted data does not have the similar voltage drop due to the scaling of I-V data. However, the decrease in voltage drop with the increase in V1 phenomena matches with the measured data.

The drop in V2 voltage is due to the increase in source-drain saturation voltage ($V_{DS,Sat}$). Due to the soft transition from the linear to saturation region the change in $V_{DS,Sat}$ is not very prominent.

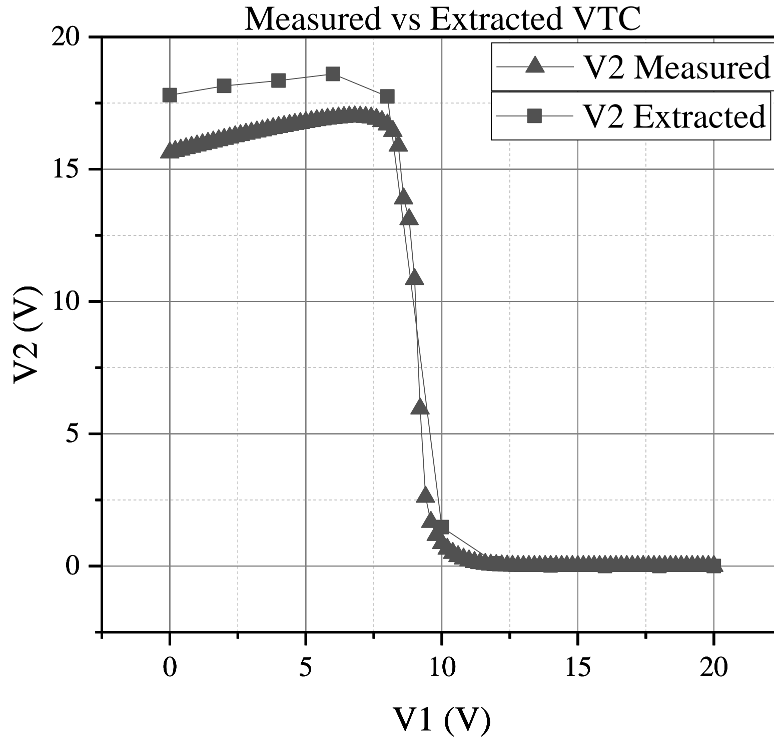

Fig. 47. Measured vs. Extracted VTC.

The SNM results from TP5 and TP6 exhibit similar characteristics as seen from TP3 and TP4. Therefore, they are omitted here.

6.2 Read Static Noise Margin

Read operation is the most vulnerable to noise, and the degradation in RSNM results in a destructive read operation. The designed cell has a pair of access transistors (Tx_{Access}) connected on each bitline, allowing different cell configurations. The cell is characterized using all the configurations mentioned in the testplans covered in Chapter 4. In order to get accurate measurements similar to SNM, both right and left inverters are measured for RSNM. Table 9

shows the testplans for the right side of the inverter; the same testplans are used to measure the RSNM for the left side of the inverter.

Table 9. Summary of the RSNM Testplans

	VDD1	VDD2	V1	V2	WL1,	WL2,	BL,	BLB
Testplan #1 (TP1)	ON	ON	NC	V Out	ON	ON	V sweep	ON
Testplan #2 (TP2)	ON	OFF	NC	V Out	ON	ON	V sweep	ON
Testplan #3 (TP3)	OFF	ON	NC	V Out	ON	ON	V sweep	ON
Testplan #4 (TP4)	ON	ON	NC	V Out	ON	OFF	V sweep	ON
Testplan #5 (TP5)	ON	OFF	NC	V Out	ON	OFF	V sweep	ON
Testplan #6 (TP6)	OFF	ON	NC	V Out	ON	OFF	V sweep	ON
Testplan #7 (TP7)	ON	ON	NC	V Out	OFF	ON	V sweep	ON
Testplan #8 (TP8)	ON	OFF	NC	V Out	OFF	ON	V sweep	ON
Testplan #9 (TP9)	OFF	ON	NC	V Out	OFF	ON	V sweep	ON

NC=No connection

The RSNM data is measured on all the testplans, but only TP1 and TP4 (or TP7) data are discussed here; TP4 and TP7 have identical results. The data from VDD1 or VDD2 (i.e., TP2, TP3, TP5, TP6, TP8, and TP9) are ignored because with a single VDD; the PMOS drive strength is weak due to the poor P-type contacts. With the help of illustration (Fig. 48), the effect on RSNM from two parallel access transistors (Tx_{Access}) is shown. Consider that the right side of the SRAM is holding a logic '0' stored bit, the bitlines are charged to logic '1', and the wordlines are asserted for both Q4 R and Q5 R. Subsequently, the bitline (BLB) potential drops because of the I_{Sink} through Q1 R and will create a potential at node V2. The discharge rate dictates the amount of potential at node V2; a slow discharge lowers the voltage at node V2, and a faster discharge drops the voltage rapidly. Both fast and slow discharge can cause the destructive read; hence, the access

transistors' proper sizing is essential in the SRAM design. It is important to have multiple design iterations, followed by tapeouts, for SRAM cell design, even in mature process technologies.

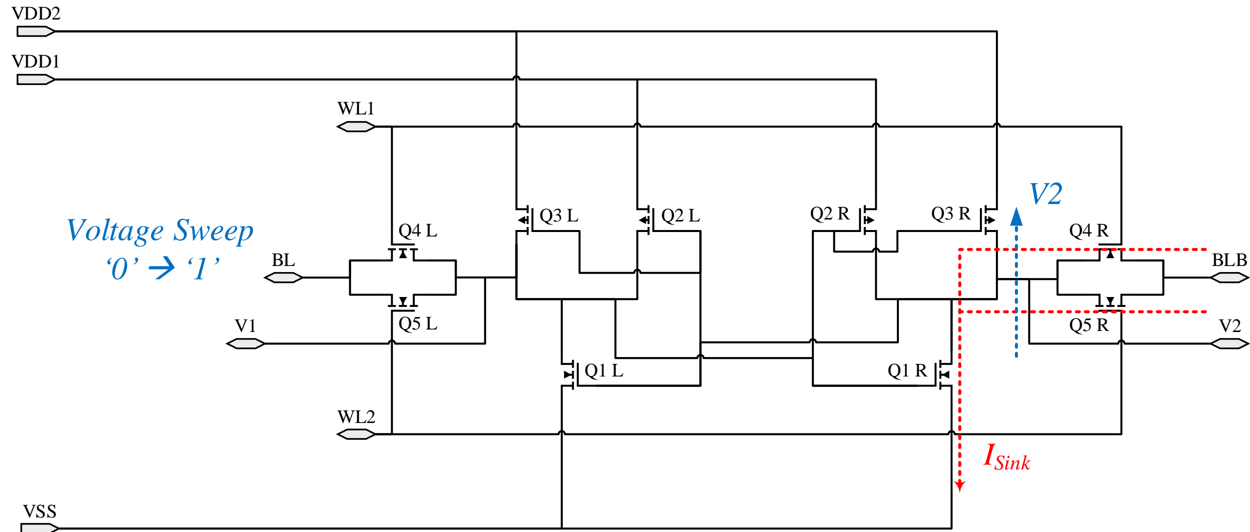

Fig. 48. RSNM illustration.

The RSNM plots at 25°C and 500°C from Wafer 6 are shown in Fig. 49. As the width of the Tx_{Access} is increasing, the area of the eye in the plot is decreasing. The data is measured for two different test structures to see the effect of the Tx_{Access} width. The width of the Tx_{Access} in the first test structure (TS1) is 8 µm; if only one wordline is active (WL1 or WL2), the effective width is 8 µm, and if both wordlines are active, then the width becomes 16 µm. The second test structure (TS2) has a width of 5 µm for the Tx_{Access}. And when both wordlines are active, then the width is 10 µm. The highest RSNM value is observed at TS2, when only one wordline is active, which corresponds to a width of 5 µm. The data at 500ºC shows erratic behavior between left and right inverters, the effect of an increase in the width is not following the same trend as it is on the left side of the inverter. One of the potential causes of this behavior is the temperature cycling that occurred while conducting these measurements, causing the devices to deteriorate.

Table 10 summarizes RSNM across all three wafers and shows the dependency of RSNM on temperature and the changing width of Tx_{Access}. The value of RSNM is extracted via the MATLAB code, and all three wafers depicted that the highest RSNM value is with the smallest Tx_{Access}.

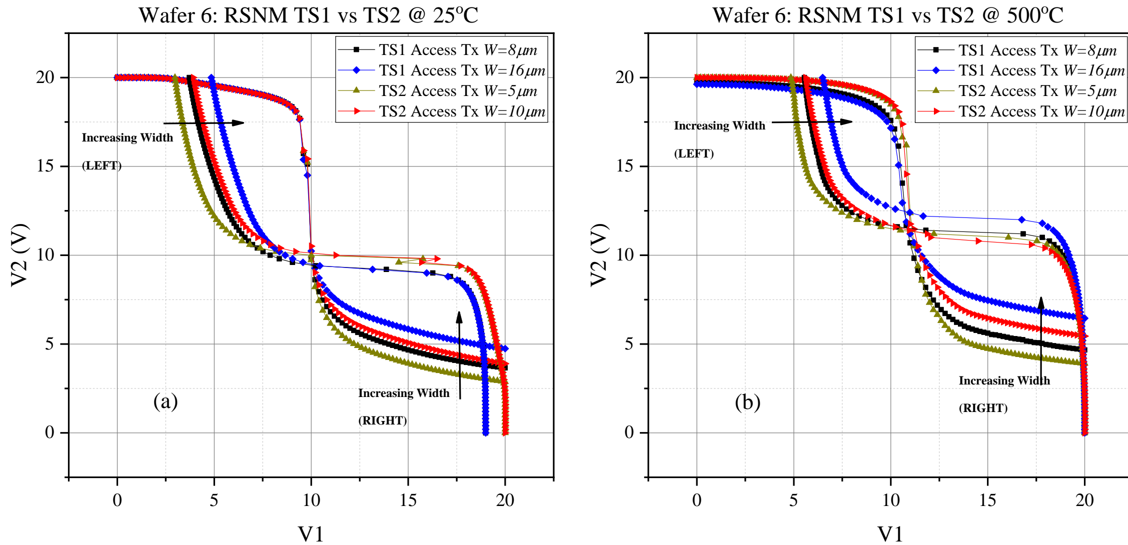

Fig. 49. RSNM plots (a) At 25°C (b) At 500°C.

Table 10. RSNM for Wafers 2, 4, and 6 at 20V with Varying Temperatures

		25ºC	**250ºC**	**500ºC**
Wafer 2	TS1 W=8um	6.6213 V	6.448 V	6.6796 V
	TS1 W=16um	6.1436 V	5.9965 V	NA
	TS2 W=5um	7.6817 V	7.3016 V	6.6018 V
	TS2 W=10um	6.6915 V	5.7867 V	6.2143 V
Wafer 4	TS1 W=8um	6.5351 V	6.0608 V	5.8707 V
	TS1 W=16um	6.0427 V	5.3307 V	5.6373 V
	TS2 W=5um	7.57 V	6.0308 V	6.702 V
	TS2 W=10um	6.8442 V	5.5403 V	6.3128 V
Wafer 6	TS1 W=8um	5.9869 V	6.2522 V	5.4501 V
	TS1 W=16um	5.247 V	5.4603 V	5.2182 V
	TS2 W=5um	7.26 V	6.89 V	6.2197 V
	TS2 W=10um	5.7126 V	5.8693 V	6.0192 V

6.3 Write Static Noise Margin

In write mode, the cell needs to flip the stored bit from '0' to '1' and '1' to '0'. It is contradictory to the read mode. The goal is to avoid the flipping of a stored bit in the read mode, and therefore the Tx_{Access} are sized accordingly. Based on the RSNM results, the best size is the smallest Tx_{Access}. However, the smallest transistor limits the write operation. Hence, the size of the Tx_{Access} needs to be adjusted for the proper write operation. Generally, this is the reason for having multiple iterations for the SRAM cell design. Table 11 shows all the testplans developed to measure WSNM, but only TP1 and TP4 (or TP7) results are discussed here. The data is characterized for different Tx_{Access} widths; the WSNM plots from wafer 6 at room temperature and 500ºC are shown in Fig. 50. Similar to RSNM, the width of Tx_{Access} has a significant impact on the WSNM. The WSNM decreases with the decrease in the width of Tx_{Access}.

Table 11. Summary of the WSNM Testplans

	VDD1	**VDD2**	**V1**	**V2**	**WL1,**	**WL2,**	**BL,**	**BLB**
Testplan #1 (TP1)	ON	ON	NC	V Out	ON	ON	V sweep	OFF
Testplan #2 (TP2)	ON	OFF	NC	V Out	ON	ON	V sweep	OFF
Testplan #3 (TP3)	OFF	ON	NC	V Out	ON	ON	V sweep	OFF
Testplan #4 (TP4)	ON	ON	NC	V Out	ON	OFF	V sweep	OFF
Testplan #5 (TP5)	ON	OFF	NC	V Out	ON	OFF	V sweep	OFF
Testplan #6 (TP6)	OFF	ON	NC	V Out	ON	OFF	V sweep	OFF
Testplan #7 (TP7)	ON	ON	NC	V Out	OFF	ON	V sweep	OFF
Testplan #8 (TP8)	ON	OFF	NC	V Out	OFF	ON	V sweep	OFF
Testplan #9 (TP9)	OFF	ON	NC	V Out	OFF	ON	V sweep	OFF

NC=No connection

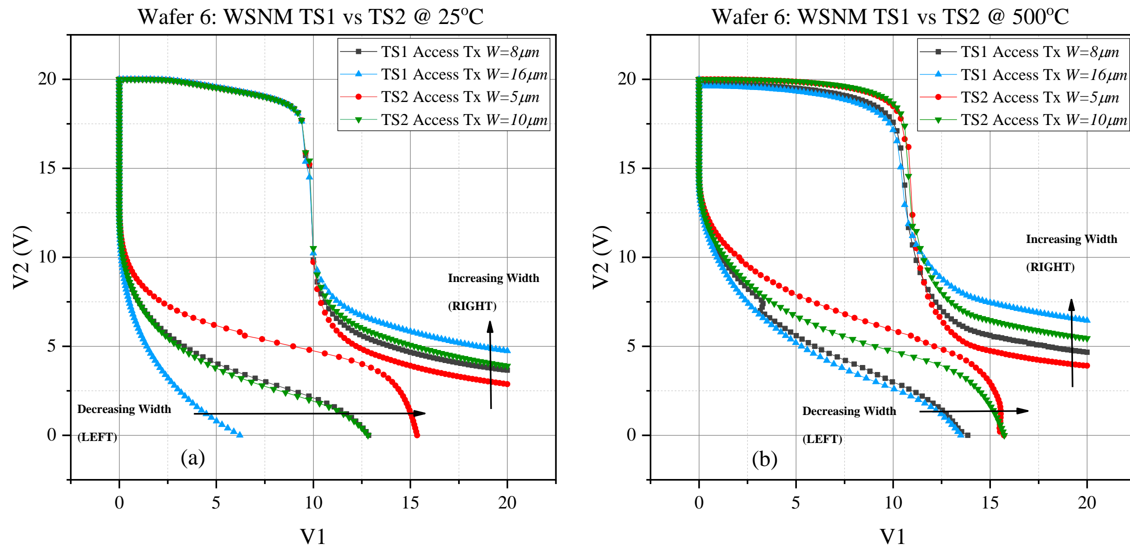

Fig. 50. WSNM plots (a) At 25°C (b) At 500°C.

As mentioned in the testplans section, the right inverter output is connected to the logic '1' via Tx_{Access}; therefore, it is the same configuration as in the RSNM testplan. The left inverter is connected to logic '0' through Tx_{Access}, which means it tries to keep the inverter output to logic '0' while the left side inverter's input is sweeping from logic '0' to logic '1'. Thus, the left inverter plots in Fig. 50 depict this behavior. The WSNM from all three wafers at varying temperatures is listed in Table 12. All three wafers show better WSNM with a larger width of Tx_{Access}; wafer 6 results are better compared to wafer 2 & 4. Wafer 2 and Wafer 4 show a negative WSNM, which means the write operation cannot be performed on the cell with a smaller width of Tx_{Access}. Based on the results achieved from WSNM and RSNM, the better cell configuration for high temperature and at low temperature is TS2 when both wordlines are active. Due to the SRAM cell's design flexibility, another possible configuration is where the read operation can be performed with only one wordline active. And for a write operation, both wordlines are used.

Table 12. WSNM for Wafer 2, 4, and 6 at 20 V with Varying Temperatures

		25ºC	**250ºC**	**500ºC**
Wafer 2	TS1 W=8um	2.5578 V	2.9749 V	2.1615 V
	TS1 W=16um	7.1937 V	7.1301 V	5.9865 V
	TS2 W=5um	-0.9222 V	-0.1524 V	0.2826 V
	TS2 W=10um	3.7551 V	3.9543 V	3.3309 V
Wafer 4	TS1 W=8um	2.3422 V	1.4735 V	0.8266 V
	TS1 W=16um	7.2708 V	6.3353 V	6.0216 V
	TS2 W=5um	-0.6907 V	-1.7803 V	-3.7002 V
	TS2 W=10um	4.0499 V	2.499 V	3.2371 V
Wafer 6	TS1 W=8um	4.9358 V	2.7198 V	4.8334 V
	TS1 W=16um	9.2204 V	7.4266 V	7.1955 V
	TS2 W=5um	1.422 V	-0.161 V	1.1629 V
	TS2 W=10um	5.6351 V	3.6647 V	3.9679 V

6.4 Data Retention Voltage

The data retention voltage (DRV) of an SRAM is the minimum supply voltage at which its cell can retain its state. The characterization of DRV is vital, and from its minimum value, the SRAM array's power consumption in hold state can be estimated. For the designed cell, SNM is measured at 20 V, 15 V, and 10 V at different temperatures for all three wafers. The DRV results at room temperature and 500ºC from wafer 6 are shown in Fig. 51. Similar to SNM data discussed in Section 6.1, the increase in temperature shifts the metastable point or crossover point towards the right, which is due to the lowering of the PMOS threshold magnitude and lowering of the threshold of NMOS. Table 13 shows the DRV for all the three wafers at varying temperatures; with the increase in temperature the SNM decreases on all the different supply voltages.

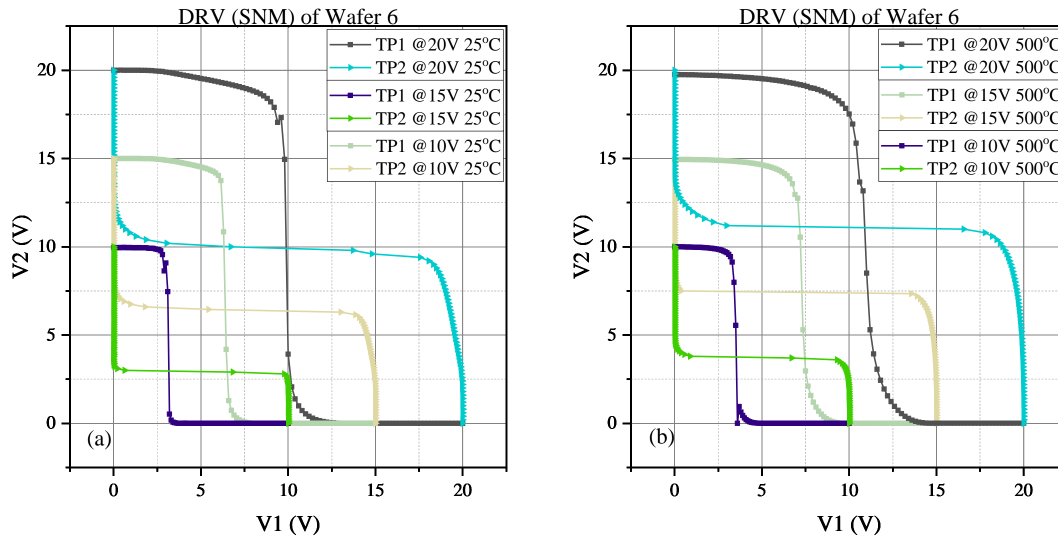

Fig. 51. DRV (a) At 25°C (b) At 500°C.

Table 13. DRV (SNM) at Varying Temperatures

		25°C	**250°C**	**500°C**
Wafer 2	10 V	6.4962 V	6.2426 V	6.0708 V
	15 V	8.8524 V	8.4709 V	8.1563 V
	20 V	11.35 V	10.46 V	10.16 V
Wafer 4	10 V	6.3621 V	5.9606 V	5.3229 V
	15 V	8.735 V	8.0534 V	7.3066 V
	20 V	10.91 V	10.21 V	9.21 V
Wafer 6	10 V	6.4563 V	6.1543 V	5.8831 V
	15 V	8.5005 V	8.3179 V	8.634 V
	20 V	10.99 V	10.54 V	10.42 V

From the DRV data, the quiescent current and the peak current of the bit cell are also extracted. The quiescent current (I_{DDQ}) is relatively low compared to the peak current (I_{PEAK}); because the quiescent current is during the steady-state when there is no transition on the stored bit and either NMOS or PMOS in the bit cell's inverter is ON. The peak current is when the transition from logic '1' to '0' or '0' to '1' occurs; both NMOS and PMOS are in saturation during this transition.

The dependency of I_{PEAK} and I_{DDQ} on temperature is shown in Fig. 52. The y-axis is changed to a log scale to represent the current values better. As expected, the minimum I_{PEAK} and I_{DDQ} for each wafer is at 10 V and 25ºC. And as the temperature increases the currents also increase. The I_{PEAK} comparison between Wafer 2, Wafer 4, and Wafer 6 are very close to each other, and are shown in Fig. 52(a). On the other hand, the I_{DDQ} shows subtle differences across three wafers. The highest leakage current is observed on Wafer 6, as shown in Fig. 52(b); this is due to the lower threshold voltage of the NMOS transistors. The minimum I_{DDQ} of 300 pA at 10 V is also noticed on Wafer 6, but this result is an outlier. Because the test setup (particularly the probe station and its peripheral components) thermal and chuck vibration contributed to the current noise, the noise floor was found to be ~7 nA. Based on the I_{DDQ} data, Wafer 2 is selected for further DC and all the transient analyses. The W2 shows the smallest I_{DDQ} at 10 V and 500°C. Another representation of I_{PEAK} and I_{DDQ} with respect to supply voltage is shown in Fig. 53.

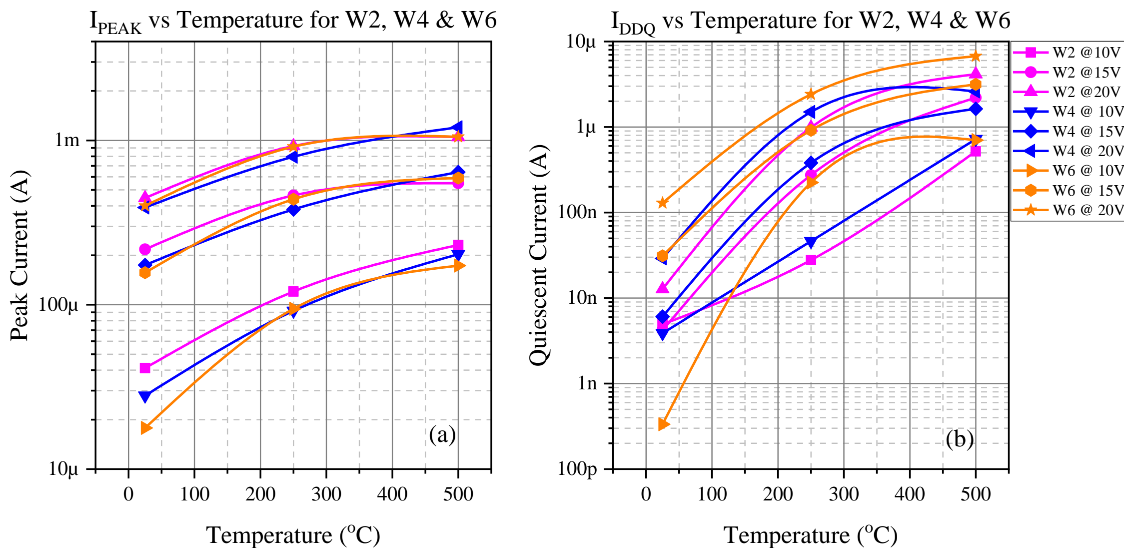

Fig. 52. W2, W4, and W6 comparison between (a) I_{PEAK} vs. Temperature and (b) I_{DDQ} vs. Temperature.

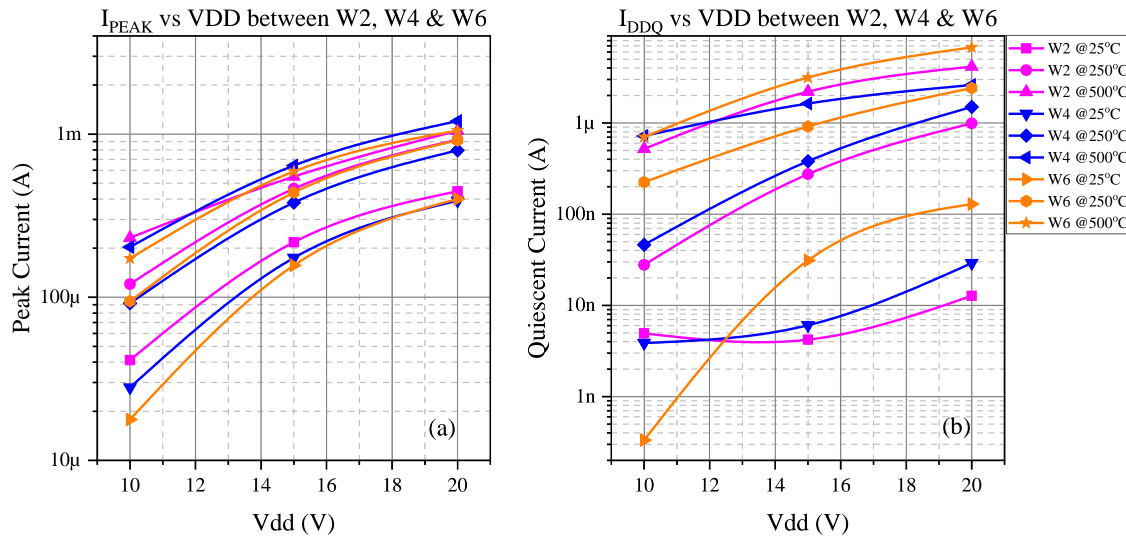

Fig. 53. W2, W4, and W6 comparison between (a) I_{PEAK} vs. VDD and (b) I_{DDQ} vs.VDD.

The probe station's test setup has a significant noise due to the vibration from the compressor, thermal controller, vacuum pump, and other peripherals connected during the test for high-temperature measurements. Therefore, the minimum supply voltage for DRV tests was restricted to 10 V on the probe station. However, due to the decrease in the PMOS threshold's magnitude at high temperatures, the supply voltage can be lowered. This is one of the SRAM design goals; so that the power consumption can be minimized. Unfortunately, the probe station could not support this test; therefore, a different test setup was built. In this test setup, W2 samples are die attached and wirebonded onto a 68-pin quad flat pack (QFP) leaded chip carriers (LDCC). At room temperature, the SNM is measured at 7.5 V and is shown in Fig. 54. Compared to SNM at 10 V and 25ºC (Table 13), the SNM is reduced by 74.5 % at a 7.5 V supply voltage. The cell still holds its positive feedback characteristics with a voltage drop (V_{DROP}) of ~500 mV when V1 is between 0 V and 725 mV, as shown as regions of interest in Fig. 54. And the I_{PEAK} and I_{DDQ} at 7.5 V are 3 µA and 1.9 nA, respectively. Hence, a considerable reduction in current consumption is evident in comparison to the 10 V supply voltage.

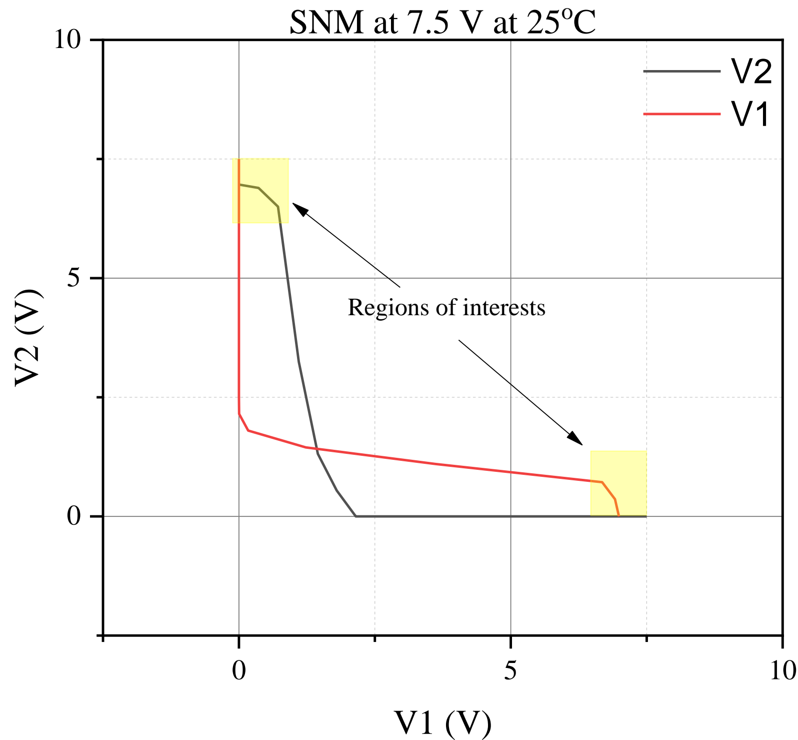

Fig. 54. SNM from Wafer 2 at 7.5 V and 25°C.

An attempt to reduce the supply voltage below 7.5 V is performed, but the V_{DROP} of ~500 mV increases with the decrease in supply voltage. In Table 14, the V_{DROP} at different supply voltage is listed, along with the measured voltage (V_{MEAS}) at V2 when V1 is set to 0 V. Two factors are contributing to the V_{DROP}; the first one is the threshold voltage of the PFET, which is ~6.5 V for W2 wafer. Secondly, the poor p-type contacts. The room temperature data shows that the SRAM cell retains its positive feedback behavior up to 7 V of the supply voltage. And it is not operational below 7 V and lost its feedback characteristics. However, the high-temperature data collected on the packaged part shows that the SRAM cell works at the supply voltage of 6.5 V. Unfortunately, the I_{PEAK} and I_{DDQ} during high-temperature measurements could not be captured

due to the minimum current resolution of the power supply (0.01 A). Still, it can be calculated based on the currents' exponential trend shown in Fig. 52 and Fig. 53.

Table 14. Voltage Drop with Varying Supply Voltage

Supply Voltage (V)	25°C		200°C		450°C	
	V_{MEAS} (V)	V_{DROP} (V)	V_{MEAS} (V)	V_{DROP} (V)	V_{MEAS} (V)	V_{DROP} (V)
5.5	0.05387	5.44613	NA	NA	0.0291	5.4709
6	1.2251	4.7749	2.675	3.325	3.481	2.519
6.5	4.95	1.55	5.896	0.604	6.135	0.365
7	6.418	0.582	6.87	0.13	6.913	0.087
7.5	6.988	0.512	7.241	0.259	7.305	0.195
10	9.976	0.024	9.987	0.013	9.909	0.091

6.5 Transient Analysis

The detailed testplan and procedure of transient measurements are explained in Section 5.3. In this section, high-temperature transient waveforms during the read operation are shown, with varying supply voltages. Fig. 55 shows the read operation when the stored bit is at logic ‘0’, OUT and OUTN are the sense amplifier's outputs. BL and BLB are connected between SRAM and sense amplifier. These bitlines (BL and BLB) act as an input/output net; during the read operation, the voltage difference generated on the bitlines is detected by the sense amplifier. The sequence of digital signals' assertion (WL1, WL2, PC, and SE) is the key to do a correct read operation. Typically, an embedded circuit (the firing circuit) that takes care of these digital signals is designed along with the SRAM cells/array. The firing circuit includes several buffers and digital logic to generate precise pulses of different durations. The firing circuit's design complexity is not tricky, but the design requires very well-fitted device models to control the delay chain precisely. The urge to design this circuit was discouraged because of the suitable models' unavailability and the significant shifts in the process technology.

Fig. 55 to Fig. 60 shows the read operation for logic ‘0’ and logic ‘1’ at supply voltages of 10 V, 7.5 V, and 6 V. In all the figures, the SRAM read operation window is marked as the white arrow. Before and after this region, the sense amplifier's output is undefined and shaded in gray. The read operation starts with charging the bitlines that occur by asserting a pulse on the PC node of the sense amplifier. Once the bitlines are charged, the access transistors are switched on for a short while to generate the potential difference between the two bitlines. The bitline connected to the stored bit ‘0’ discharges and the other bitline retains its voltage because it is connected to the stored bit ‘1’. The sense amplifier SE node is switched on to detect this voltage difference and latch the cross-coupled inverter, and the output is measured at the OUT and OUTN of the sense amplifier.

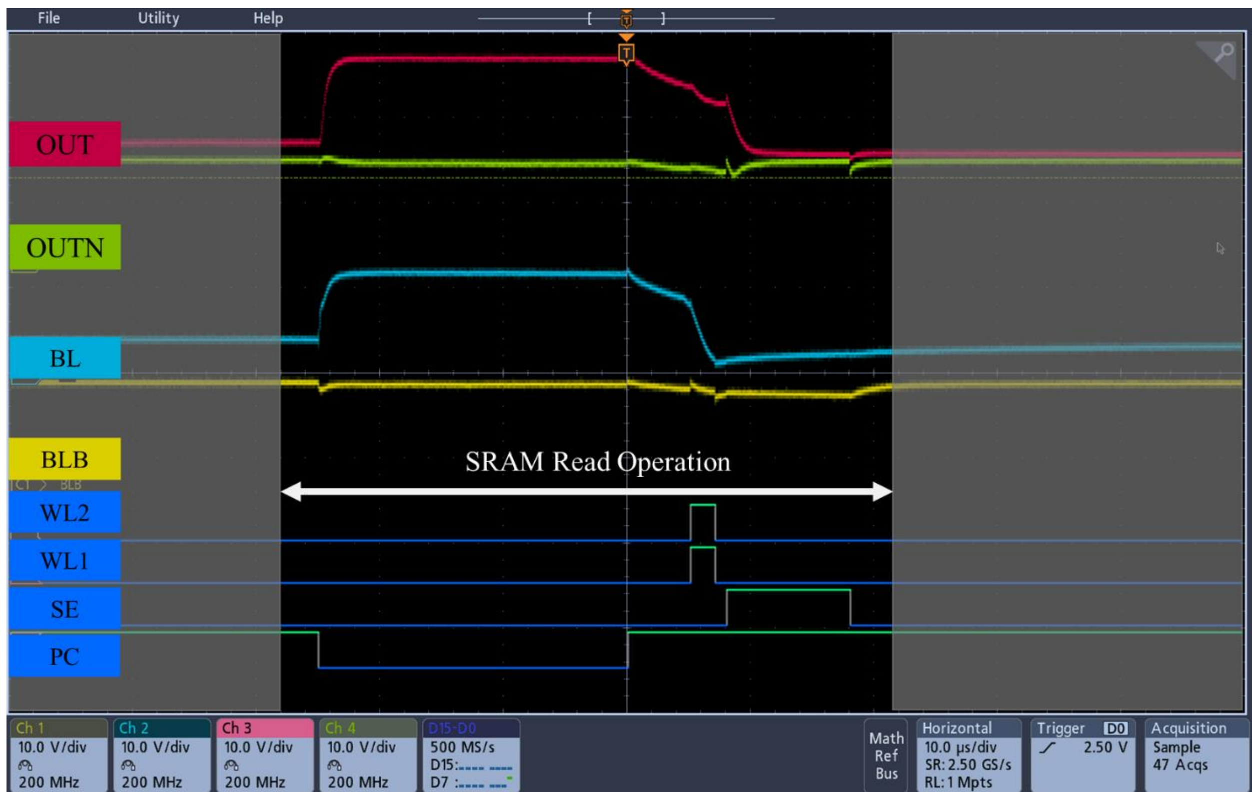

Fig. 55. Reading logic '0' at VDD=10 V and Temperature=400°C.

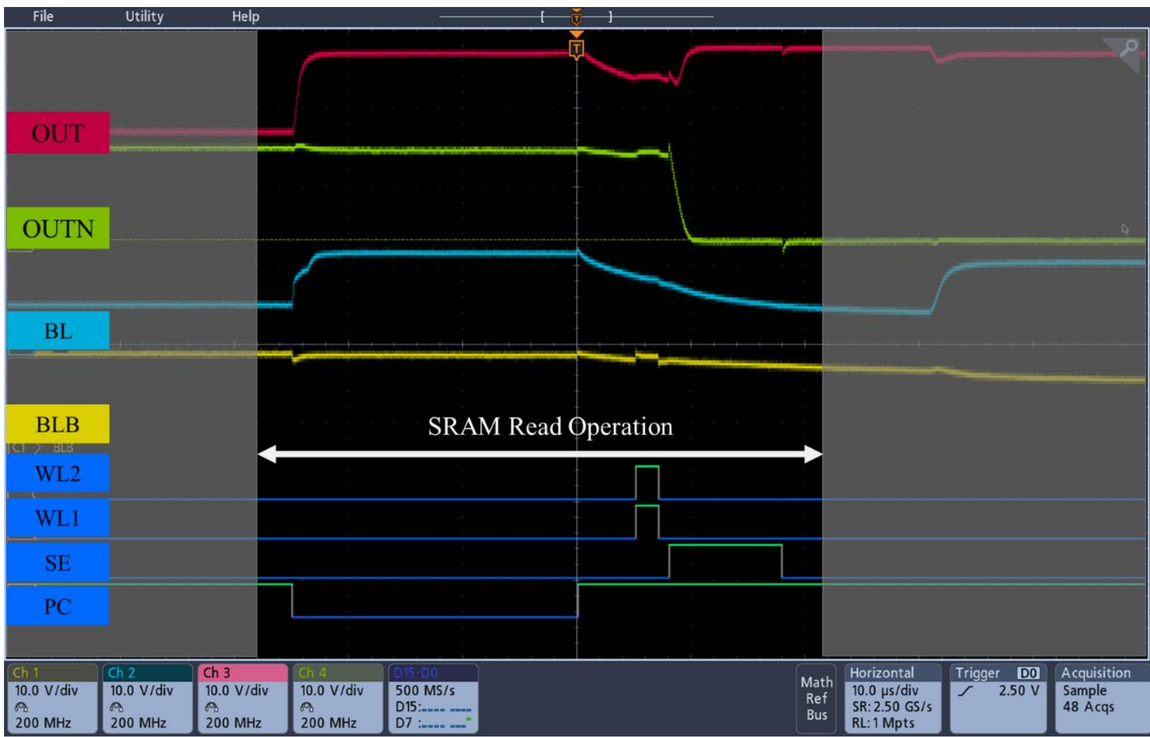

Fig. 56. Reading logic '1' at VDD=10 V and Temperature=400°C.

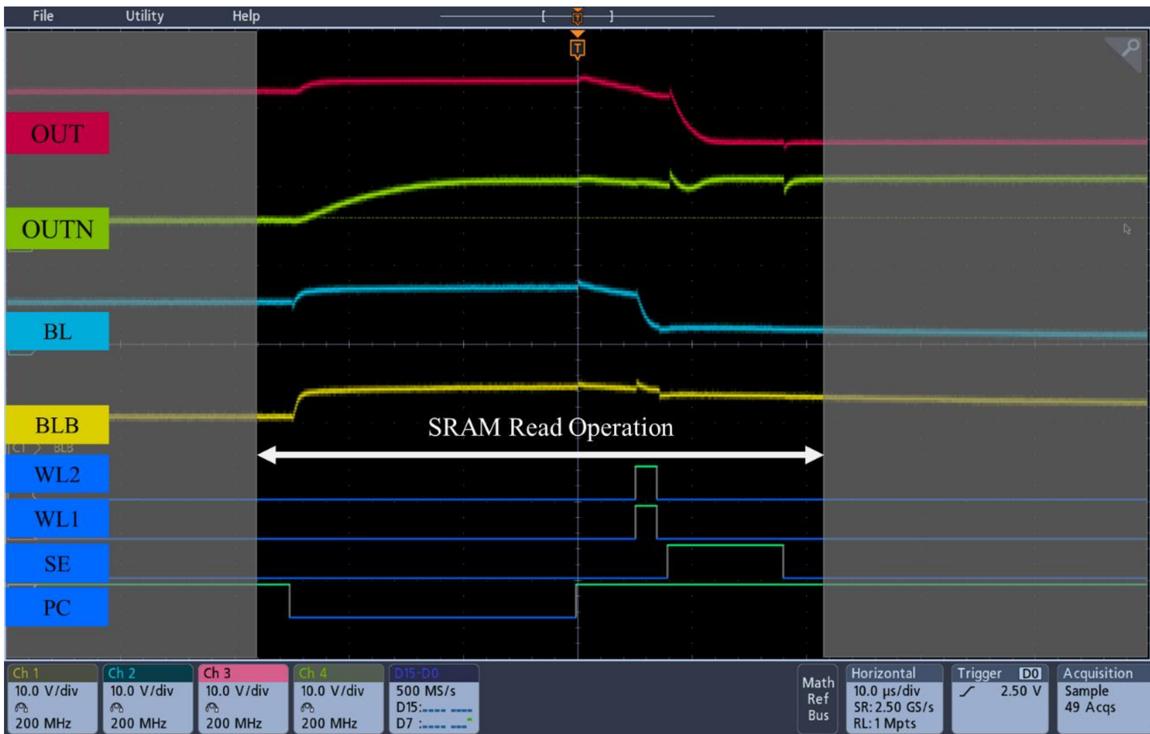

Fig. 57. Reading logic '0' at VDD=7.5 V and Temperature=400°C.

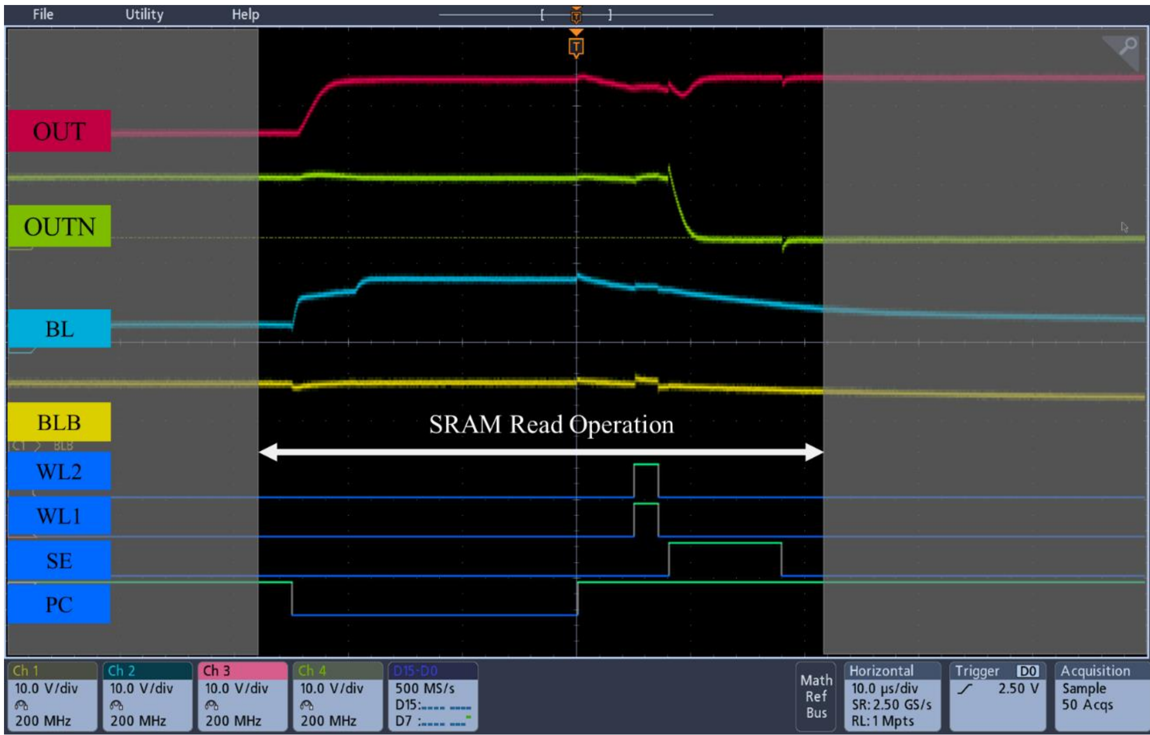

Fig. 58. Reading logic '1' at VDD=7.5 V and Temperature=400ºC.

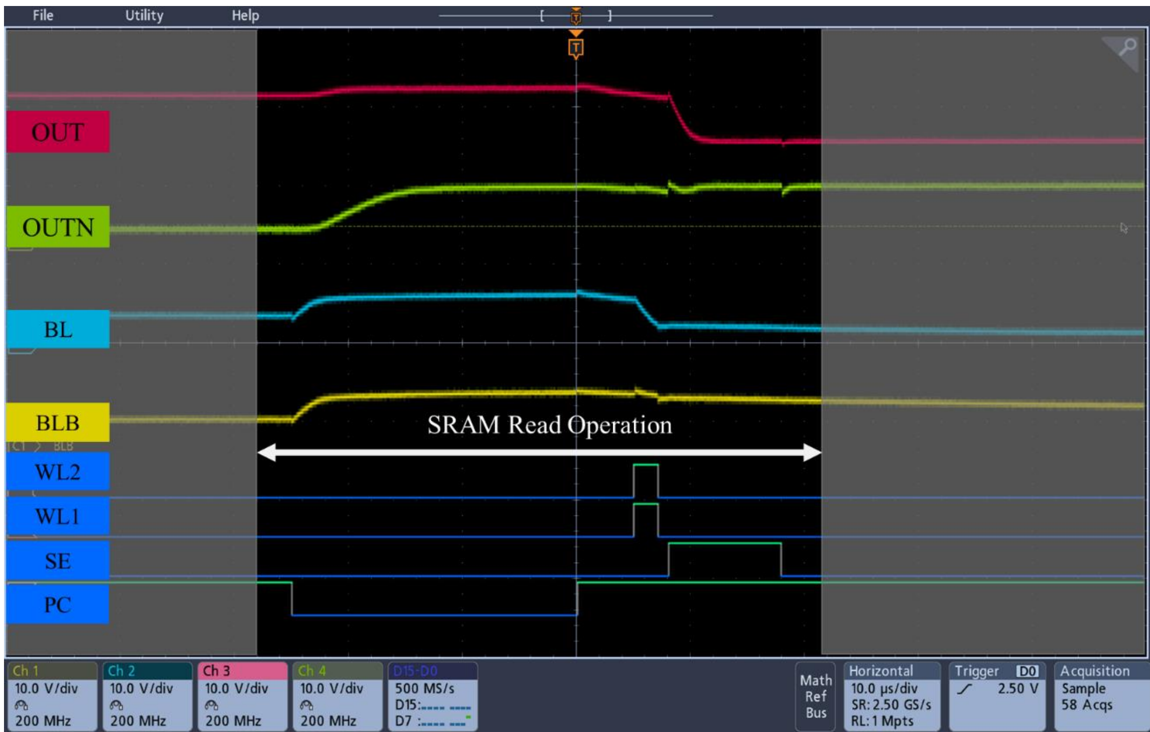

Fig. 59. Reading logic '0' at VDD=6 V and Temperature=400ºC.

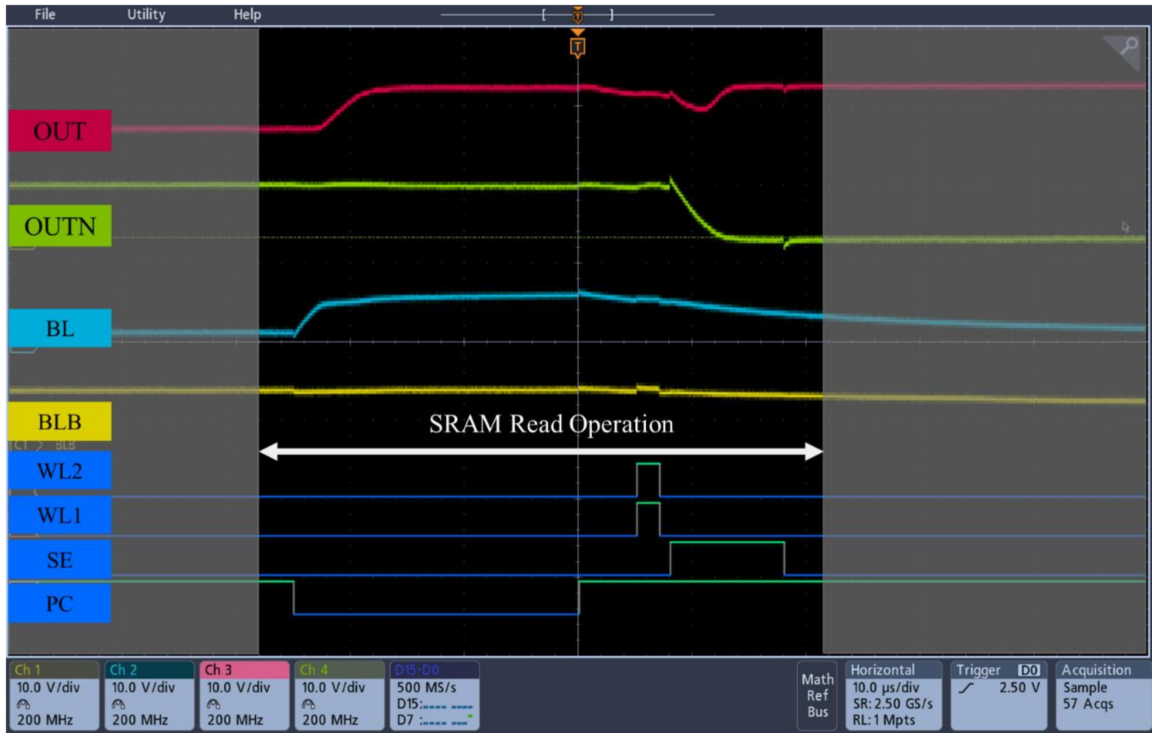

Fig. 60. Reading logic '1' at VDD=6 V and Temperature=400°C.

The transient data shown above has a fixed read access time of ~45 µs at all temperatures and voltage supplies because the function generator's digital signals are kept the same for all the measurements. The above tests intend to check the functionality of the SRAM cell and the sense amplifier. Therefore, no optimization has been done to the digital signals. However, the actual read access time for the memory differs with varying supply voltage and temperatures. And, it is calculated from the measured data. The equation generated to calculate the access time is determined by considering the time required to charge the bitlines ($Bitlines_{CHARGE\ TIME}$), the time required to generate enough potential difference between the bitlines ($Bitlines_{TIME\ TO\ VD}$), and the time required to latch the sense amplifier ($Latch_{TIME}$).

$$Access\ Time = Bitlines_{CHARGE\ TIME} + Bitlines_{TIME\ TO\ VD} + Latch_{TIME} \quad (3)$$

Table 15. Read Access Time at Varying Supply Voltage and Temperature

Supply Voltage	25ºC	250ºC	400ºC
10 V	~10 µs	~6.5 µs	~7 µs
7.5 V	~10.2 µs	~6.9 µs	~7.5 µs
6 V	NA	NA	~7.4 µs

The reliability of the SRAM cell is another very important FOM. Typically, memory manufacturer follows memory reliability standards defined by the Joint Electron Device Engineering Council (JEDEC) [35], etc. The manufacturer performs very rigorous reliability testing for their memory products by conducting more than a thousand read and write cycles. To perform multiple read and write cycles, the industry uses automatic testing equipment (ATE). Since this work is implemented on an unmatured technology, therefore a less rigorous reliability test was conducted.

At 400ºC, the 100 read cycles are executed continuously at supply voltages of 7.5 V, 6.5 V, and 6 V, shown in Fig. 61, Fig. 62, and Fig. 63, respectively. The amplitude of the complementary outputs of the sense amplifier is captured via data logging software. For the supply voltage of 7.5 V and 6.5 V, the read operation was 100% successful with no data read error. However, with the supply voltage of 6 V, a few of the data read cycles produced the wrong data. Also, the output voltage levels are not close to the VDD and VSS. The data read error observed at 6 V of supply voltage is due to the combined effect of poor p-type contacts and the threshold voltage of PFET. In conclusion, the designed cell is reliable at the supply voltage of 6.5 V or above.

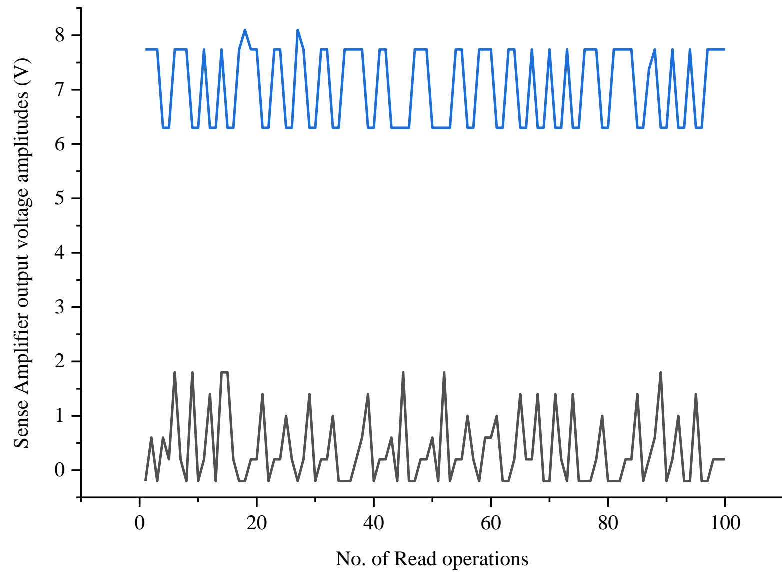

Fig. 61. At VDD=7.5 V and temperature=400ºC.

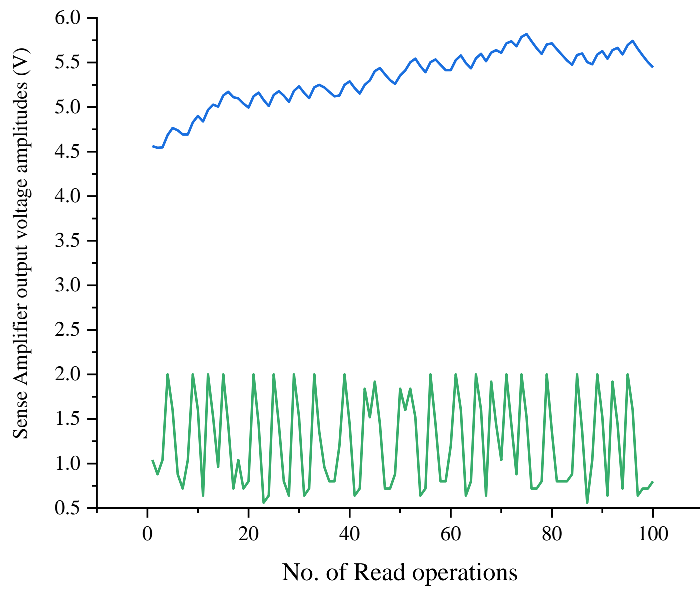

Fig. 62. At VDD=6.5 V and temperature=400ºC.

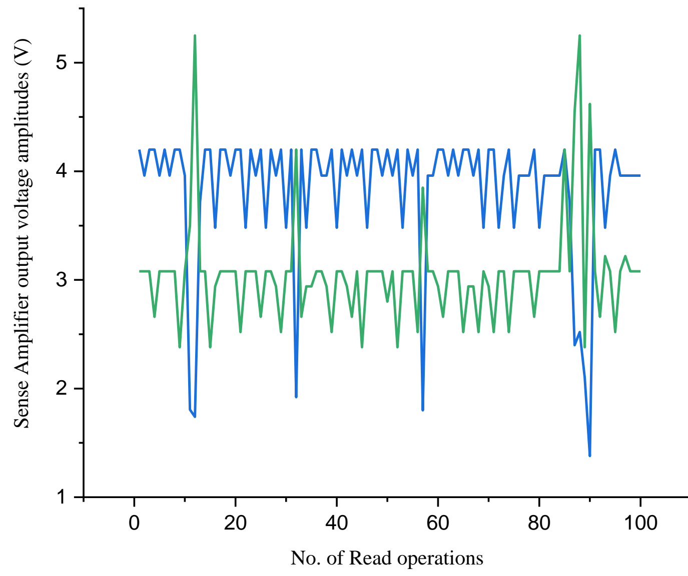

Fig. 63. At VDD=6 V and temperature=400ºC.

7 Conclusions and Future Work

7.1 Conclusions

This research presents an SRAM memory cell design and test that enables SiC CMOS technology to realize a complete and high-density electronic system for high-temperature applications. This work introduces the first SiC CMOS SRAM cell capable of operating at 500ºC with nano ampere current consumption and supply voltage of 6.5 V. The SRAM cell designed in this research is a novel SRAM architecture that is capable of reducing the effect of the inadequate SiC low voltage lateral MOSFET characteristics, which occurs due to the prevalent challenges in the SiC CMOS fabrication process.

The SRAM cell's DC characteristics at 500ºC reported in this work have never been reported in the literature. Also, the transient analysis of the SRAM cell and the sense amplifier at 400ºC established a new mark for high-temperature memory design. The SRAM cell's adaptability helps mitigate the SiC process challenges and the unexpected process variations with the expense of a few extra transistors and pins. The reliability analysis of the SRAM and sense amplifier shows that the data stored in a cell retains its state at high-temperature (400ºC) during hold state and data read operations. The read access time of ~7.5 μs at 400ºC is calculated from the transient data. This read time translates into maximum operating frequency of 133 kHz for this SRAM.

Other contributions noted in this work are the development of the SiC PDK, including the physical design rule checks for CalibreDRC and CalibreLVS. SiC device characterization for the IC design effort. This work also reported the first implementation and characterization of sense amplifier designs in SiC CMOS technology which performs at 500ºC and outperforms the existing sense amplifiers implemented in traditional silicon/silicon-on-insulator processes.

7.2 Future Work

The SiC CMOS technology can disrupt the high-temperature electronics domain, but it the fabrication challenges need to be overcome. The work presented in this thesis proves that the technology can operate at 500ºC; however, new design approaches must be considered. The SRAM cell and the sense amplifier results obtained during this research encourage implementing a complete 1 kB or more SRAM array along with all the peripheral circuitry. The memories are very high-density circuit blocks; therefore, more than one metal routing layer would help implement the SRAM array. The SiC CMOS technology also needs a promising attempt to lower the threshold voltage magnitude for PFET so that the memory can be operated at low voltages to reduce power consumption.

References

[1] R. Kirschman, "Status of Silicon Carbide (SiC) as a Wide Bandgap Semiconductor for High Temperature Applications: A Review," *IEEE High-Temperature Electronics*, doi: 10.1109/9780470544884.ch69, 1999.

[2] R. Cojbasic, O. Cogal, P. Meinerzhagen, C. Senning, C. Slater, T. Maeder, A. Burg, and Y. Leblebici, "FireBird: PowerPC e200 based SoC for high temperature operation," in *Proceedings of the IEEE 2013 Custom Integrated Circuits Conference (CICC)*, San Jose, CA, pp. 1–4, Sept. 2013.

[3] A. Rahman et. al., "A Family of CMOS Analog and Mixed Signal Circuits in SiC for High Temperature Electronics," *2015 IEEE Aerospace Conference*, Big Sky, MT, pp. 1-10, 2015.

[4] R. Cojbasic and Y. Leblebici, "Design of high-temperature SRAM for reliable operation beyond 250°C," *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, Lisbon, 2015, pp. 2545-2548, doi: 10.1109/ISCAS.2015.7169204

[5] Kim, Tony Tae-Hyoung and Ngoc Le Ba, "A low voltage 8-T SRAM with PVT-tracking bitline sensing margin enhancement for high operating temperature (up to 300°C)," *2013 IEEE Asian Solid-State Circuits Conference (A-SSCC)* (2013): 233-236.

[6] T. T. Kim and N. Le Ba, "Design of a Temperature-Aware Low-Voltage SRAM With Self-Adjustable Sensing Margin Enhancement for High-Temperature Applications up to 300 °C," in *IEEE Journal of Solid-State Circuits*, vol. 49, no. 11, pp. 2534-2546, Nov. 2014, doi: 10.1109/JSSC.2014.2338860.

[7] N. Le Ba and T. T. Kim, "Design of Temperature-Aware Low-Voltage 8T SRAM in SOI Technology for High-Temperature Operation (25 %C–300 %C)," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, no. 8, pp. 2383-2387, Aug. 2017, doi: 10.1109/TVLSI.2017.2686600.

[8] D. Gogl, H. -. Fiedler, M. Spitz and B. Parmentier, "A 1-Kbit EEPROM in SIMOX technology for high-temperature applications up to 250/spl deg/C," in *IEEE Journal of Solid-State Circuits*, vol. 35, no. 10, pp. 1387-1395, Oct. 2000, doi: 10.1109/4.871314.

[9] Tai-Hua Chen, L. T. Clark and K. E. Holbert, "Memory design for high temperature radiation environments," *2008 IEEE International Reliability Physics Symposium*, Phoenix, AZ, 2008, pp. 107-114, doi: 10.1109/RELPHY.2008.4558870.

[10] A. Abbasi, R. C. Murphree, S. Roy, M. Suggs, J. Fraley, H. A. Mantooth, J. Di, T. Erlbacher, "High Temperature Memory Design, Implementation, and Characterization in 1µm SiC CMOS Technology," in *Additional Conferences (Device Packaging, HiTEC, HiTEN, & CICMT)*, vol. 2019, no. HiTen, pp. 000011-000015, July 2019.

[11] H. Kappert, N. Kordas, S. Dreiner, U. Paschen, and R. Kokozinski, "High Temperature SOI CMOS Technology and Circuit Realization for Applications up to 300°C," *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, Lisbon, pp. 1162–1165, 2015.

[12] J. M. Hornberger, E. Cilio, R. M. Schupbach, A. B. Lostetter and H. A. Mantooth, "A High-Temperature Multichip Power Module (MCPM) Inverter utilizing Silicon Carbide (SiC) and Silicon on Insulator (SOI) Electronics," *2006 37th Power Electronics Specialists Conference*, Jeju, S. Korea, pp. 1-7, 2006.

[13] S. Kargarrazi, H. Elahipanah, S. Rodriguez, and C. Zetterling, "500 °C, High Current Linear Voltage Regulator in 4H-SiC BJT Technology," in *IEEE Electron Device Letters*, vol. 39, no. 4, pp. 548-551, April 2018.

[14] J. Holmes, A. M. Francis, I. Getreu, M. Barlow, A. Abbasi, and H. A. Mantooth, "Extended High-Temperature Operation of Silicon Carbide CMOS Circuits for Venus Surface Application," *Journal of Microelectronics and Electronic Packaging*, pp. 143-154, 2016.

[15] S. Roy et al., "A SiC CMOS Digitally Controlled PWM Generator for High-Temperature Applications," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 10, pp. 8364-8372, Oct. 2017.
doi: 10.1109/TIE.2017.2694413

[16] R. C. Murphree, S. Ahmed, M. Barlow, A. Rahman, H. A. Mantooth, and A. M. Francis (2016) A CMOS SiC Linear Voltage Regulator for High Temperature Applications. *Additional Conferences (Device Packaging, HiTEC, HiTEN, & CICMT)*: vol. 2016, no. HiTEC, pp. 000106-000111, May 2016.

[17] H. Weaver, "Silicon carbide promises longer memories for the future" in *Physics World*, vol. 5, no. 11, pp. 22-23, Nov. 1992.doi: 10.1088/2058-7058/5/11/23

[18] S. Dimitrijev, "Nonvolatile random-access memories in silicon carbide," *2003 IEEE Conference on Electron Devices and Solid-State Circuits (IEEE Cat. No.03TH8668)*, Hong Kong, China, 2003, pp. 405-409, doi: 10.1109/EDSSC.2003.1283560.

[19] H. Elgabra, A. Siddiqui and S. Singh, "Bipolar SRAM Memory Architecture in 4H-SiC for Harsh Environment Applications," in *IEEE Transactions on Electron Devices*, vol. 65, no. 8, pp. 3221-3228, Aug. 2018, doi: 10.1109/TED.2018.2849061.

[20] P. G. Neudeck, D. J. Spry, M. J. Krasowski, N. F. Prokop, G. M. Beheim, L. Chen, C. W. Chang, "Year-long 500°C Operational Demonstration of Up-scaled 4H-SiC JFET Integrated Circuits," in *Journal of Microelectronics and Electronic Packaging*, vol. 5, no.4, pp. 163-170, 1 October 2018.

[21] L. Lanni,B. G. Malm, C.-M. Zetterling, and M. Östling, "A 4H-SiC Bipolar Technology for High-Temperature Integrated Circuits," *Journal of Microelectronics and Electronic Packaging*, vol. 10, no. 4, pp. 155-162, 2013.

[22] P. G. Neudeck, D. J. Spry, L. Chen, N. F. Prokop and M. J. Krasowski, "Demonstration of 4H-SiC Digital Integrated Circuits Above 800 °C," in *IEEE Electron Device Letters*, vol. 38, no. 8, pp. 1082-1085, Aug. 2017.

[23] D. J. Spry, P. G. Neudeck, L. Chen, D. Lukco, C. W. Chang and G. M. Beheim, "Prolonged 500 °C Demonstration of 4H-SiC JFET ICs With Two-Level Interconnect," in *IEEE Electron Device Letters*, vol. 37, no. 5, pp. 625-628, May 2016.

[24] N. Ericson, S. Frank, C. Britton, L. Marlino, S.-H. Ryu, D. Grider, A. Mantooth, M. Francis, R. Lamichhane, M. Mudholkar, P. Shepherd, M. Glover, J. Valle-Mayorga, T. McNutt, A. Barkley, B. Whitaker, Z. Cole, B. Passmore, and A. Lostetter, "A 4H Silicon Carbide Gate Buffer for Integrated Power Systems," in *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 539-542, Feb. 2014.

[25] Mentor Graphics Corporation, Standard Verification Rule Format (SVRF) Manual, Calibre 2006.1, Feb. 2006.

[26] Cadence Design Systems, SKILL Language Reference, Product Version 6.40, August 2005

[27] T. J. Barnes, "SKILL: a CAD system extension language," *27th ACM/IEEE Design Automation Conference*, Orlando, FL, USA, 1990, pp. 266-271, doi: 10.1109/DAC.1990.114865.

[28] A. Abbasi et al., "Characterization of a Silicon Carbide BCD Process for 300°C Circuits," *2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Raleigh, NC, USA, 2019, pp. 231-236, doi: 10.1109/WiPDA46397.2019.8998920.

[29] S. Ahmed (2017). Modeling and Validation of 4H-SiC Low Voltage MOSFETs for Integrated Circuit Design. Theses and Dissertations Retrieved from https://scholarworks.uark.edu/etd/1945

[30] P. Lai et al., "Investigation of ESD Protection in SiC BCD Process," *2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Raleigh, NC, USA, 2019, pp. 405-409, doi: 10.1109/WiPDA46397.2019.8998959.

[31] R. J. Baker, CMOS: Circuit Design, Layout, and Simulation. Hoboken, NJ: Wiley, 2010

[32] E. Seevinck, F. J. List, and J. Lohstroh, "Static-Noise Margin Analysis of MOS SRAM Cells," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 5, pp.748-754, Oct. 19

[33] M. Albrecht, F. J. Klüpfel and T. Erlbacher, "An Iterative Surface Potential Algorithm Including Interface Traps for Compact Modeling of SiC-MOSFETs," in *IEEE Transactions on Electron Devices,* vol. 67, no. 3, pp. 855-862, March 2020, doi: 10.1109/TED.2020.2967507.

[34] J. Rabaey,"Digital Integrated Circuits: A Design Perspective: 1st (First) Edition", Prentice Hall, 1996.

[35] JEDEC standards "www.jedec.org"

Appendix A

I. RUN #1 Results and their Curve Fitting to Compact Model BSIM 4.7.0

This section contains the measured device characteristics from RUN #1. The width of each measuring device is 20 μm unless stated otherwise. Measured and playback values from extracted parameters are shown for the I_{DS} vs. V_{DS}, I_{DS} vs. V_{GS}, and C-V characteristics.

- Threshold voltage (V_{TH}) wafer maps of NFETs and PFETs
    - Shown for 25ºC and 200ºC as well as for channel lengths of 1.5 μm and 2 μm
- I_{DS} vs. V_{DS} characteristics of NFETs and PFETs for channel lengths of 2 μm and 20 μm
- I_{DS} vs. V_{GS} characteristics of NFETs and PFETs for channel lengths of 2 μm and 20 μm
- The C-V characteristics of NFETs and PFETs with a channel length of 1 μm, a width of 300 μm per finger, and a total of 74 fingers. The effective width of the device tested is, therefore, 22,200 μm.

The V_{TH} maps of NFETs for channel length of 1.5 μm and 2 μm are shown in Fig. 64 and Fig. 65. A constant current technique is used to measure the threshold voltage. Specifically, the threshold voltage is measured from the I_D vs. V_{GS} characteristics when I_D = 100 nA and V_{DS} = 500 mV. The results show that as temperature increases, threshold voltage decreases. Similarly, the threshold voltage increases with increasing channel lengths. The observation of threshold voltage increasing with increasing channel lengths is also made in [1], [2]. The V_{TH} maps of PFETs for channel length of 1.5 μm and 2 μm are subsequently shown in Fig. 66 and Fig. 67. As with the NFETs, the magnitude of the V_{TH} of the PFETs decreases with increasing temperature.

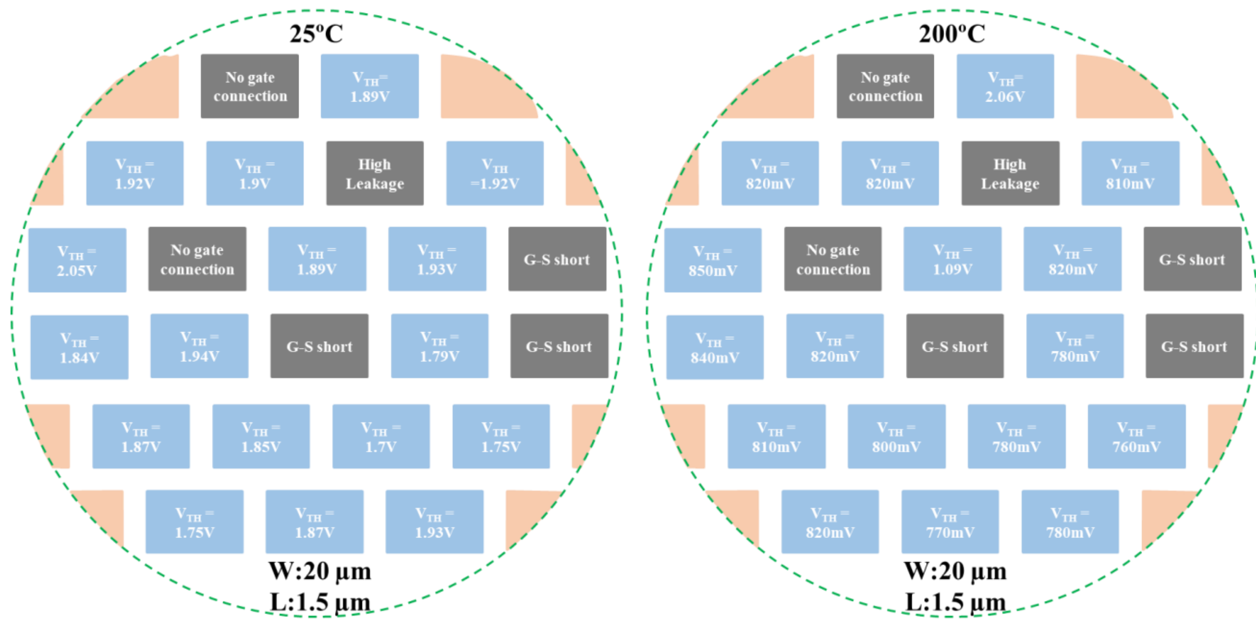

Fig. 64. The NFET V_{TH} wafer map at room temperature and for channel lengths of 1.5 µm and 2 µm. The width of each device tested is 20 µm.

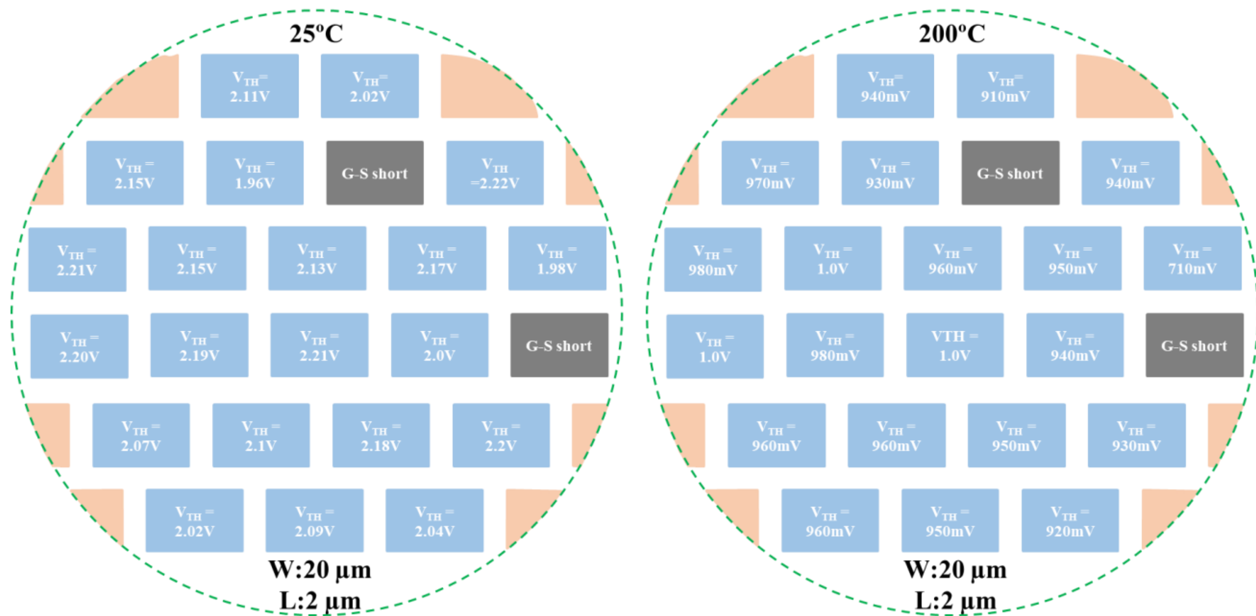

Fig. 65. The NFET V_{TH} wafer map at 200 °C and for channel lengths of 1.5 µm and 2 µm. The width of each device tested is 20 µm.

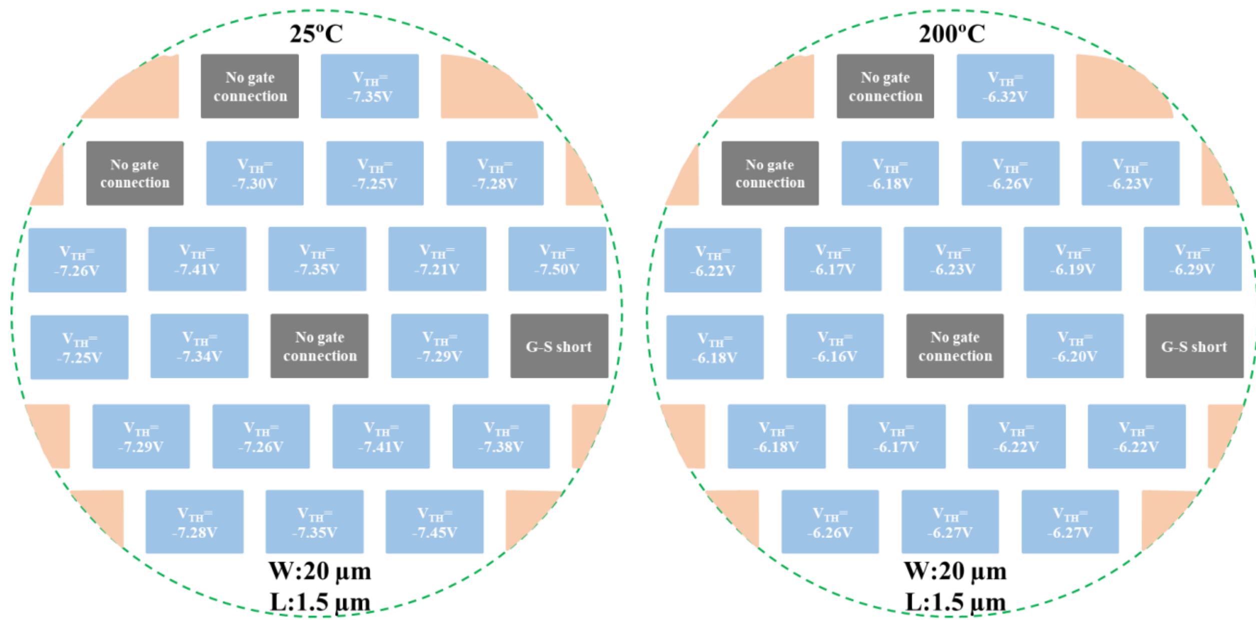

Fig. 66. The PFET V_{TH} wafer map at room temperature and for channel lengths of 1.5 µm and 20 µm. The width of each device tested is 20 µm.

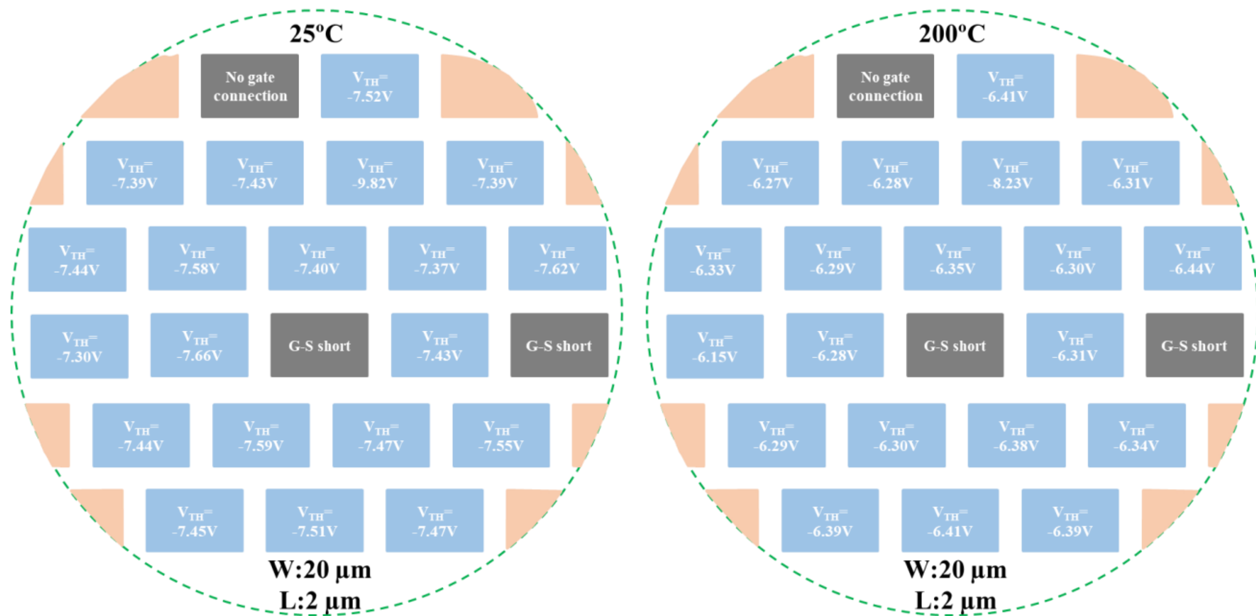

Fig. 67. The PFET V_{TH} wafer map at 200 °C and for channel lengths of 1.5 µm and 20 µm. The width of each device tested is 20 µm.

The wafer maps shown in Fig. 64 to Fig. 67 indicate that yield issues are present. The yield percentage for a single transistor does improve with an increasing channel length as expected. A total of six 1.5 µm channel length NFETs failed whereas two failed for a channel length of 2 µm. The device failures observed included gate-source shorts, no gate connection, or high leakage.

The output (I_D vs. V_{DS}) and transfer (I_D vs. V_{GS}) characteristics of an NFET with a channel length of 2 µm are shown in Fig. 68 and Fig. 69, respectively. The output and transfer characteristics for an NFET with a channel length of 20 µm are also shown in Fig. 70 and Fig. 71. The room temperature C-V characteristics of a 22,200 µm by 1 µm NFET are shown in Fig. 72. The compact model playbacks are shown by the solid line while the measured parameters are indicated by either squares or dots.

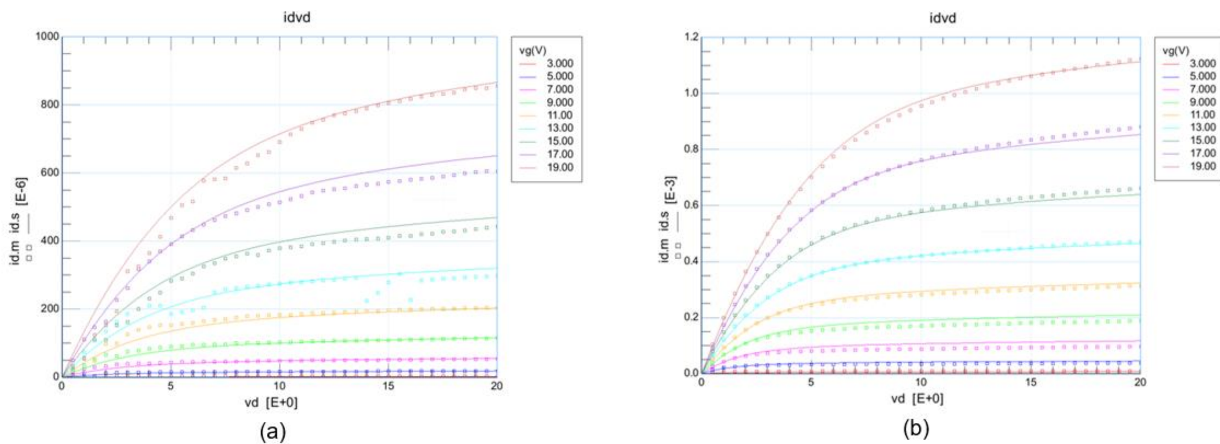

Fig. 68. The output characteristics of a 20 µm / 2 µm NFET at (a) room temperature and (b) 200ºC. The V_G is swept from 3 V to 19 V at each temperature.

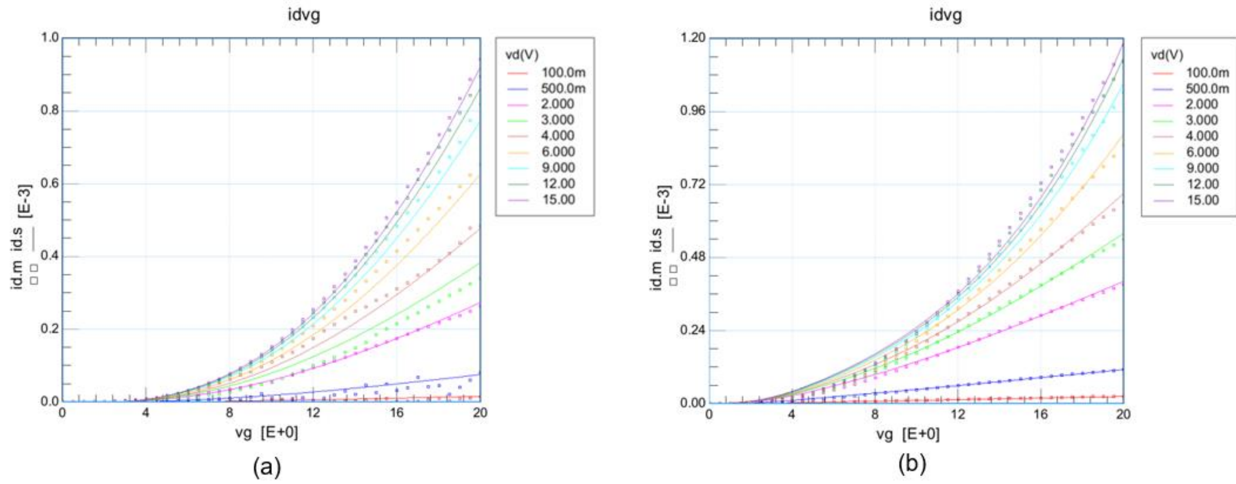

Fig. 69. The transfer characteristics of a 20 µm / 2 µm NFET at (a) room temperature and (b) 200ºC. The V_D is swept from 100 mV to 15 V at each temperature.

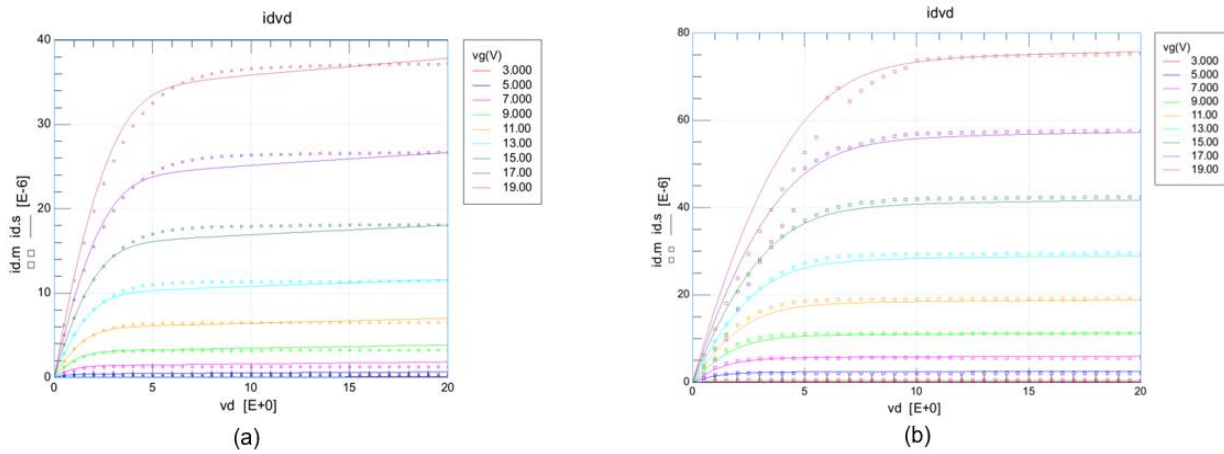

Fig. 70.The output characteristics of a 20 µm / 20 µm NFET at (a) room temperature and (b) 200ºC. The V_G is swept from 3 V to 19 V at each temperature.

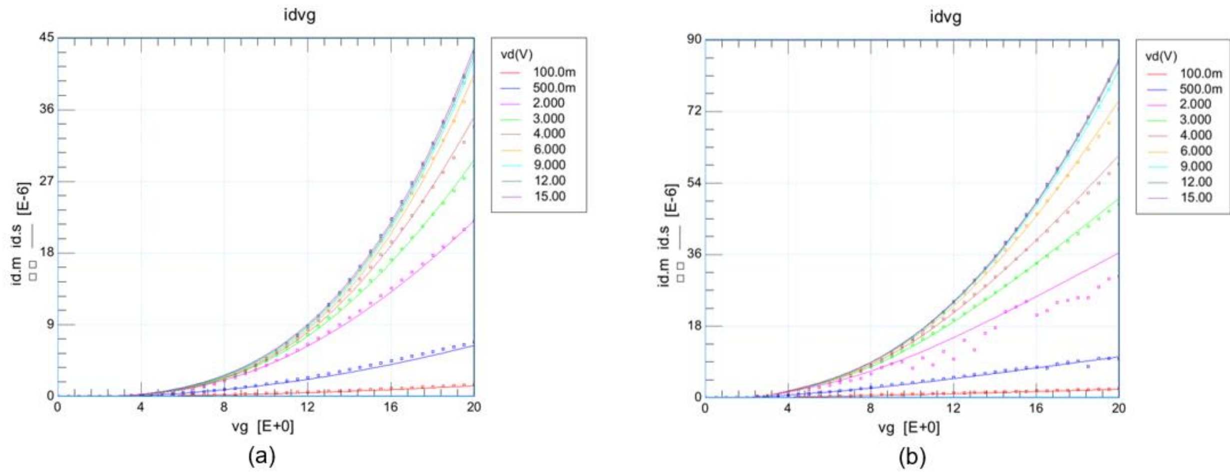

Fig. 71. The transfer characteristics of a 20 µm / 20 µm NFET at (a) room temperature and (b) 200ºC. The V_D is swept from 100 mV to 15 V at each temperature.

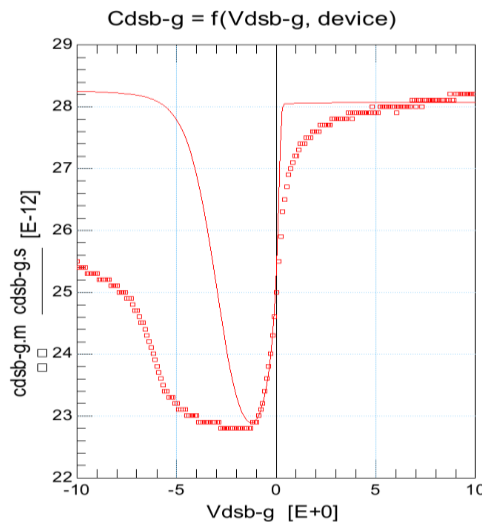

Fig. 72. The total gate capacitance ($C_{g\text{-}dsb}$ vs. $V_{g\text{-}dsb}$) of a 22,200 µm / 1 µm NFET measured at room temperature.

The output and transfer characteristics of a 20 µm by 2 µm PFET are provided in Fig. 73 and Fig. 74. Similar to the NFETs, the PFET measurement results show an increase in drive strength with increasing temperature. The output and transfer characteristics of a 20 µm by 20 µm PFET are subsequently in shown in Fig. 75 and Fig. 76. As demonstrated by the NFET

measurement results, the output resistance of the PFET is improves significantly with the increased channel length. The C-V characteristics of the PFET measured at room temperature are shown in Fig. 77.

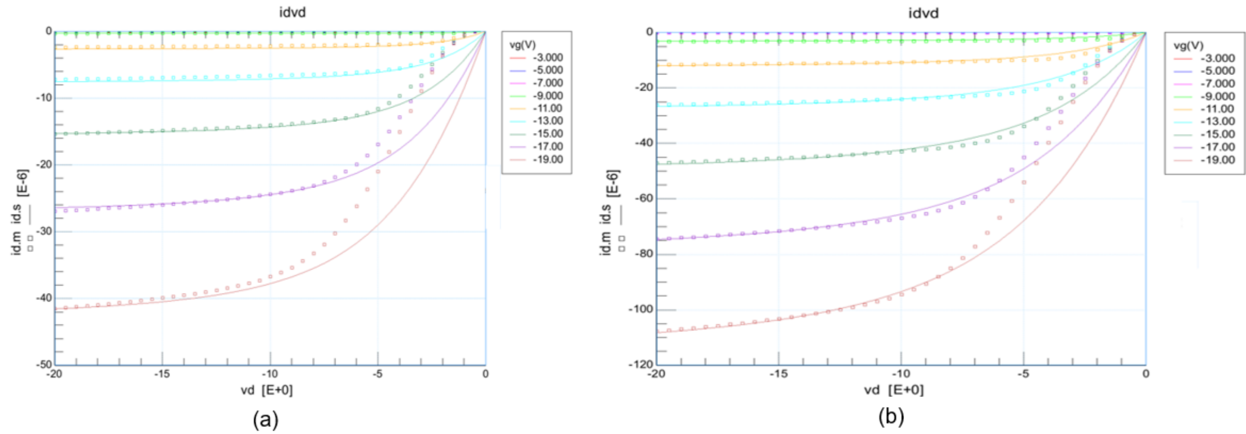

Fig. 73. The output characteristics of a 20 µm / 2 µm PFET at (a) room temperature and (b) 200 °C. The V_G is swept from -3 V to -19 V at each temperature.

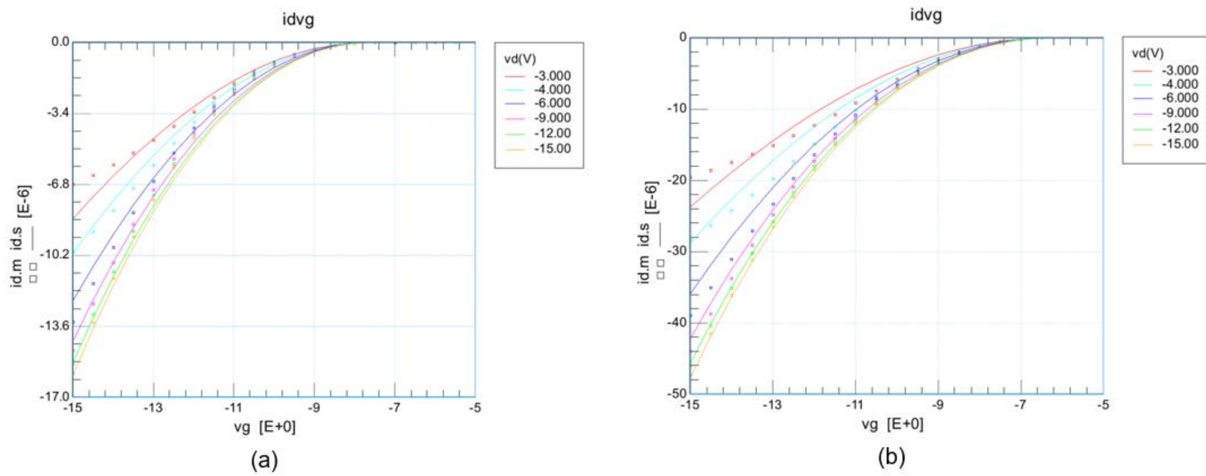

Fig. 74. The transfer characteristics of a 20 µm / 2 µm PFET at (a) room temperature and (b) 200°C. The V_D is swept from -3 V to -15 V at each temperature.

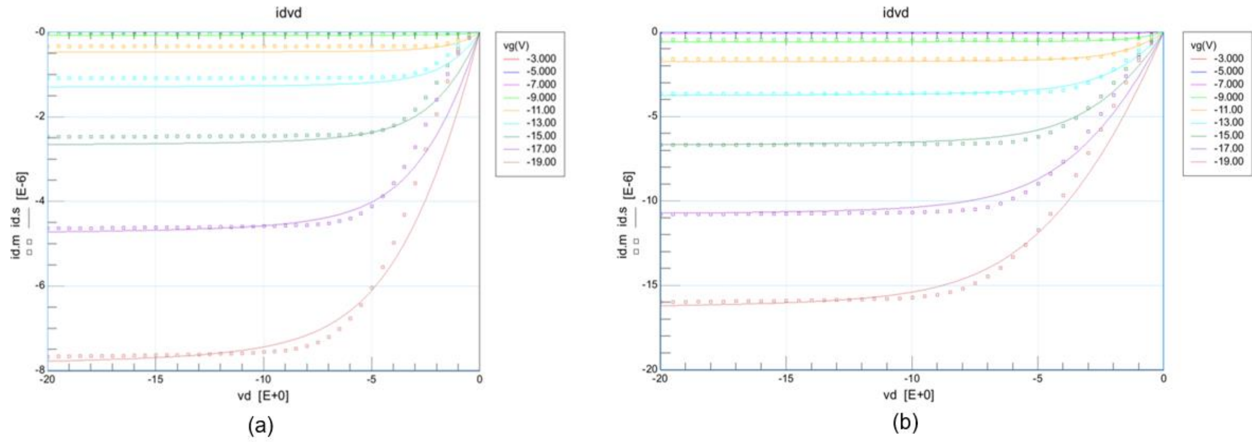

Fig. 75. The output characteristics of a 20 µm / 20 µm PFET at (a) room temperature and (b) 200ºC. The V_G is swept from -3 V to -19 V at each temperature.

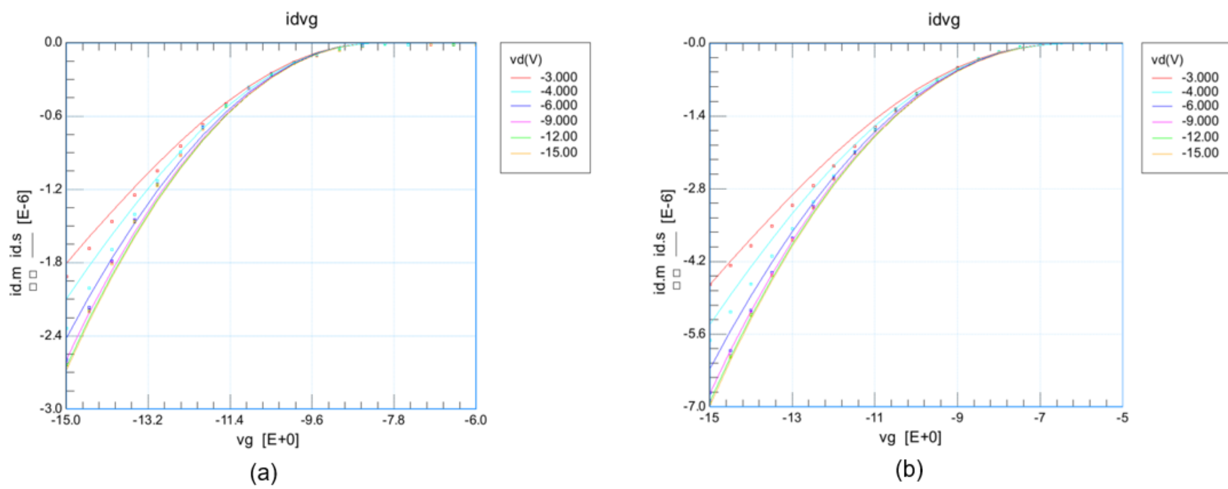

Fig. 76. The transfer characteristics of a 20 µm / 20 µm PFET at (a) room temperature and (b) 200ºC. The V_D is swept from -3 V to -15 V at each temperature.

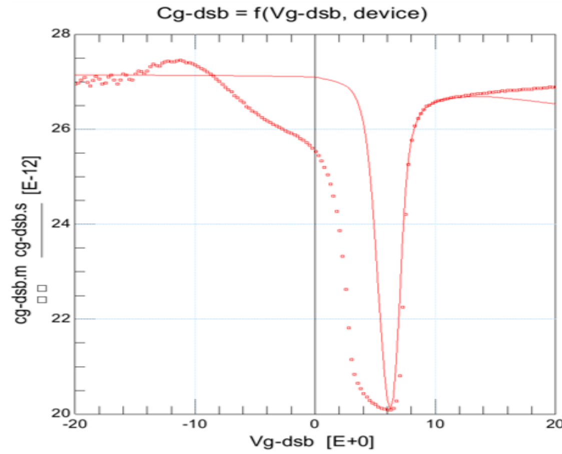

Fig. 77. The total gate capacitance ($C_{g\text{-}dsb}$ vs. $V_{g\text{-}dsb}$) of a 22,200 μm / 1 μm PFET measured at room temperature.

II. RUN #2 results and their comparison with RUN #1

Results captured through probe level testing involved DC characterization of the NFET/PFET structures and TLM structures to find the sheet resistance and contact resistances. The output and transfer characteristics from the NFET are almost the same as in RUN #1. However, the PFET showed improvements in the current drive capability of at least 2 times than RUN #1. Unfortunately, the P-type ohmic contact showed the same Schottky type behavior noticeable in the triode region of the PFET.

TLM measurements showed lower sheet resistance for PPLUS and NPLUS regions, and based on the foundry; they are close to the expected value. Hence, the over-etching of the PPLUS region is avoided in this run with the help of additional process control monitoring. Table 16 and Table 17 shows the TLM measurements comparison from RUN #1 and RUN #2 for sheet resistances and contact resistances, respectively. As the comparison shows that the sheet resistances are better in RUN #2, but contact resistances for both PPLUS and NPLUS regions are higher. Higher NPLUS

contact resistance did not affect the device behavior as it is still in the micro-ohms range. However, the increase in PPLUS contact resistance showed Schottky behavior.

Table 16 Sheet Resistances Comparison from RUN #1 and RUN #2

	Sheet Resistance (Ω) at room temperature	
	RUN #1	**RUN #2**
PPLUS region	83.2×10^{3}	65.9×10^{3}
PPLUS region	76.3×10^{3}	52.9×10^{3}
NPLUS region	1.17×10^{3}	0.916×10^{3}
NPLUS region	1.12×10^{3}	0.942×10^{3}

Table 17 Contact Resistances Comparison from RUN #1 and RUN #2

	Contact Resistance (Ωcm^2) at room temperature	
	RUN #1	**RUN #2**
PPLUS region	0.0892	2.40
PPLUS region	0.0868	1.50
NPLUS region	4.27×10^{-6}	26.9×10^{-6}
NPLUS region	4.22×10^{-6}	17.4×10^{-6}

For the DC characteristics of the MOSFETs, the devices with a width of 20 µm with varying lengths from 1 µm to 20 µm are characterized at room temperature. Fig. 78. and Fig. 79. shows the output characteristics of PFET and NFET, respectively. Fig. 78(h). and Fig. 79(h). shows the variation of threshold voltage with varying lengths for PFET and NFET, respectively. The threshold voltage is measured with the constant current method. In RUN #2, adjusted NWELL doping was used to lower the magnitude of the PFET threshold. The NWELL implantation modification did not yield any significant shift of threshold voltage for the PFET. Foundry claimed that this is due to the difficulty to control low doping concentrations with the implantation tool they have available.

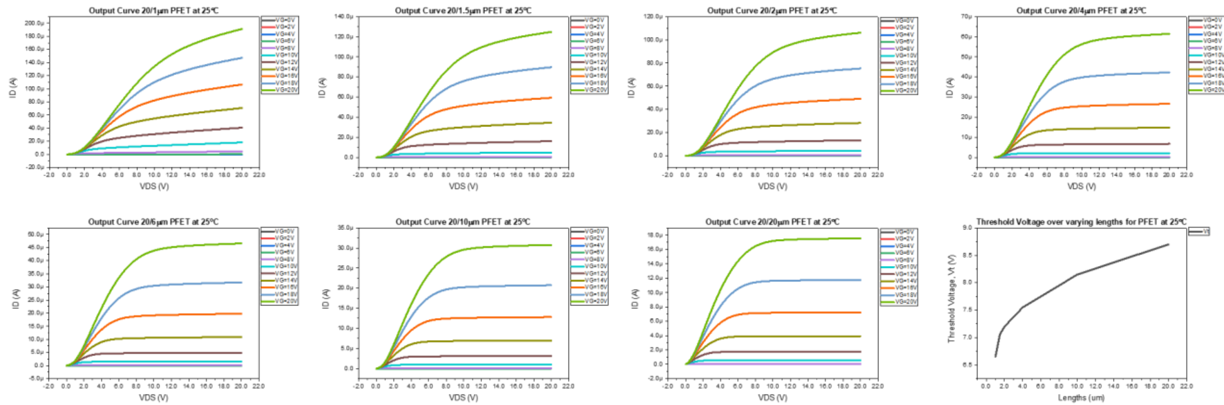

Fig. 78. Output characteristics of the PFET for the width of 20 µm and lengths of (a) 1 µm (b) 1.5 µm (c) 2 µm (d) 4 µm (e) 6 µm (f) 10 µm (g) 20 µm. (h) is the threshold voltage variation for varying lengths.

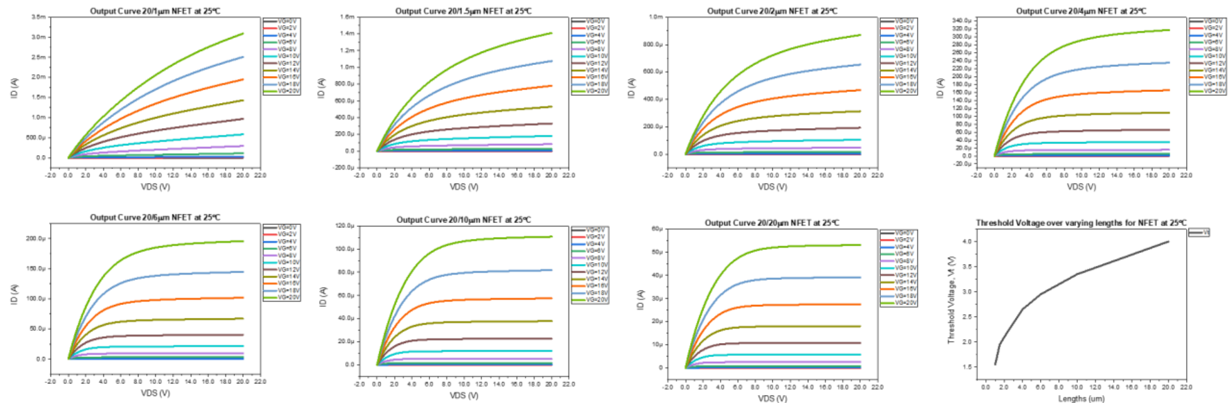

Fig. 79. Output characteristics of the NFET for the width of 20 µm and lengths of (a) 1 µm (b) 1.5 µm (c) 2 µm (d) 4 µm (e) 6 µm (f) 10 µm (g) 20 µm. (h) is the threshold voltage variation for varying lengths.

For the DC characterization of the MOSFETs at high temperature, W/L = 20 µm/2 µm sized devices are selected. Data is collected at 200°C and 500°C on the high-temperature capable probe station. Measured data is compared with RUN #1 results. Fig. 80 shows the output characteristics comparison between RUN #1 and RUN #2 at room temperature, at 200°C, and at 500°C for the PFET. The lower sheet resistance of PPLUS shows an increase in the PFET current drive in RUN #1. Fig. 81 shows the NFET output characteristics comparison between RUN #1 and RUN #2.

NFET also shows an improvement in the current drive at room temperature, at 200°C, and 500°C due to lower sheet resistance, as seen from Table 16.

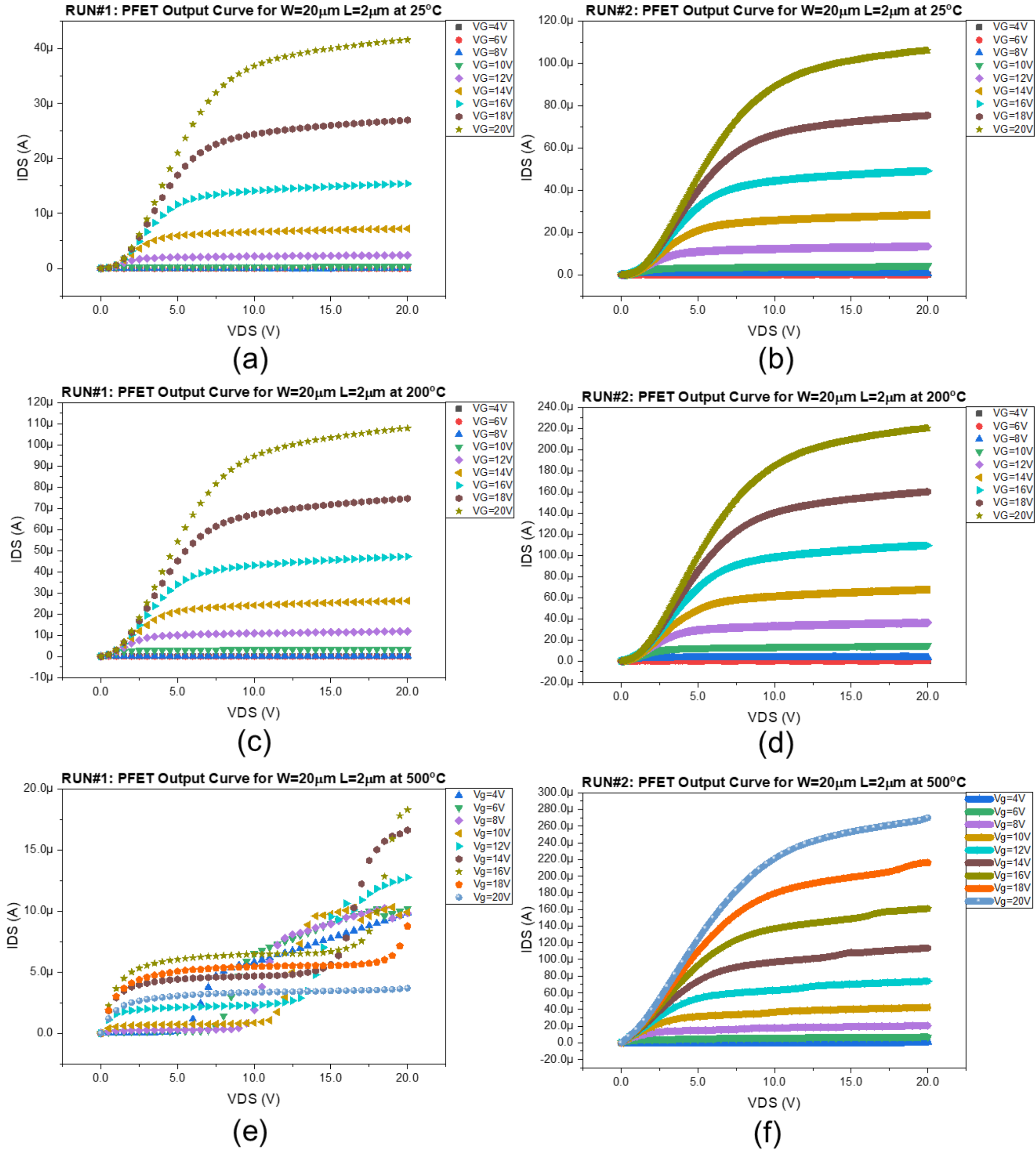

Fig. 80. RUN #1 and RUN #2 comparison for the PFET device of 20 µm / 2 µm at (a), (b) 25°C and (c), (d) 200°C and (e), (f) 500°C.

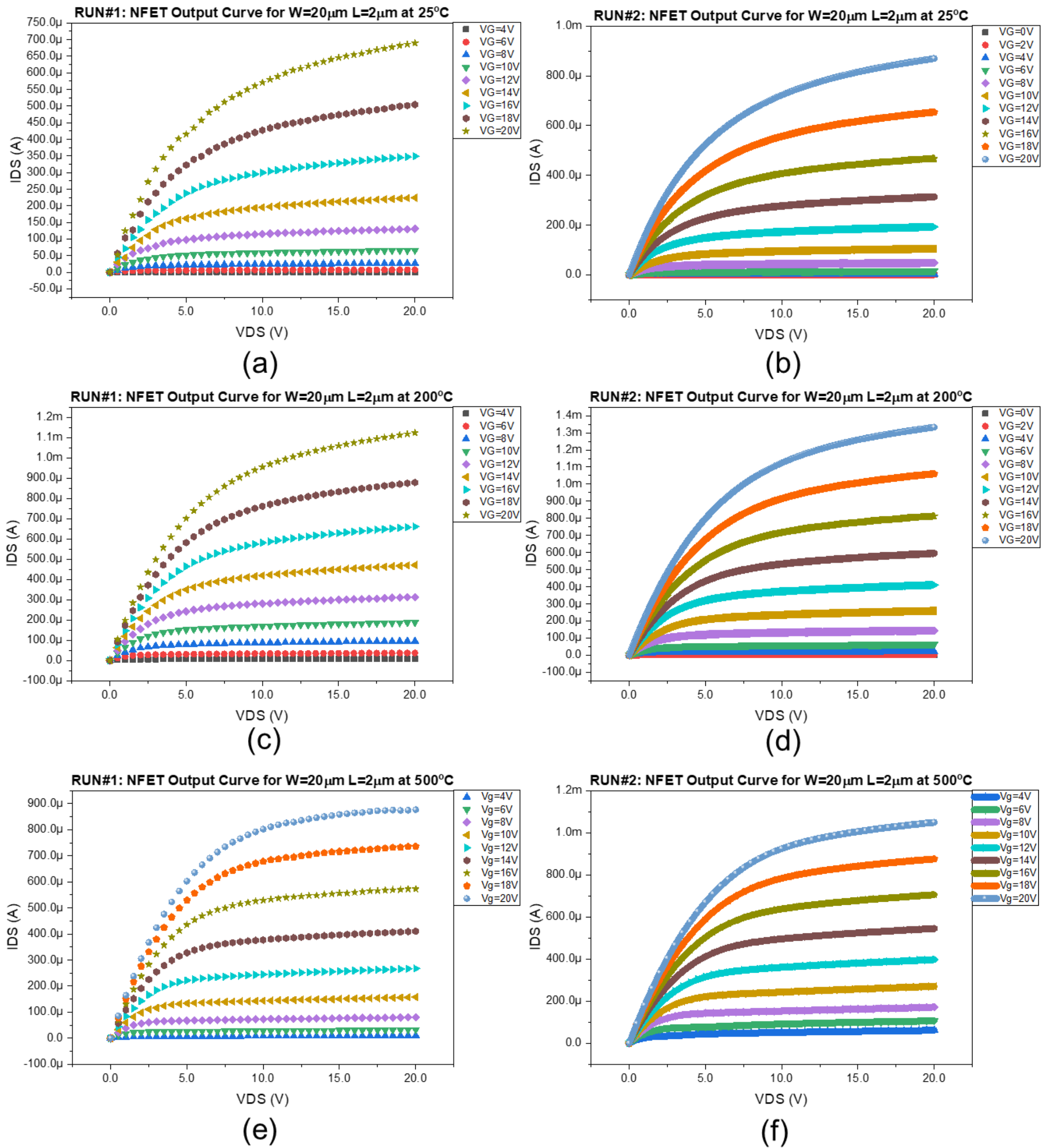

Fig. 81. RUN #1 and RUN #2 comparison for the NFET device of 20 µm / 2 µm at (a), (b) 25°C and (c), (d) 200°C and (e), (f) 500°C.

References

[1] Z. H. Liu, C. Hu, J. Huang, T. Chan, M. Jeng, P. K. Ko, and Y. C. Cheng, "Threshold voltage model for deep-sub micrometer MOSFETs," *IEEE Transactions on Electron Devices*, vol. 40, no. 1, pp. 86–95, Jan. 1993.

[2] S. Ahmed, “Modeling and Validation of 4H-SiC Low Voltage MOSFETs for Integrated Circuit Design,” Ph.D. dissertation, Department of Electrical Engineering, University of Arkansas, Fayetteville, AR, 2017.

Appendix B

Keysight B1500A Tutorial

1 B1500A Semiconductor Device Analyzer

In B1500A, we have 6 SMU's and 1 Multi-frequency capacitance measurement unit (MFCMU). B1500A can accommodate 10 SMU's; among them, 1 slot is reserved for Ground Unit (GNDU), and 1 slot is reserved for MFCMU.

- 2 High Power SMU's (HPSMU), each covers 2 slots.
- 2 High-Resolution SMU's (HRSMU), each covers 1 slot.
- 2 Medium Power SMU's (MPSMU), each covers 1 slot.
- 1 Multi-frequency Capacitance Measurement Unit (MFCMU). It covers 1 slot.

HPSMU goes up to 200V/1A with the 4-quadrant operation, and the minimum measurement resolution is 10fA/2µV.

HRSMU goes up to 100V/0.1A with the 4-quadrant operation, and its minimum measurement resolution is 1fA/0.5µV.

MPSMU goes up to 100V/0.1A with the 4-quadrant operation, and its minimum measurement resolution is 10fA/0.5µV.

MFCMU is used for AC impedance measurement such as C-V, C-f, C-t. Its frequency range is between 1kHz to 5Mhz with a minimum resolution 1mHz.

See the Data Sheet manual for their complete specifications.

2 Connection Guide

B1500A modules have triaxial output connectors except for the MFCMU unit, and it has BNC output connectors. All the grey cables are triaxial, and they came with B1500A, use them carefully.

- There is one ground cable, it has a label on it that says GROUND, and this cable is only meant to connect with GNDU, not with any other SMU, and DO NOT connect any other triaxial cable with GNDU. The GNDU cable can handle the maximum GNDU current of 4.2 A, but standard triaxial cables are only rated to 1 A. (See Configuration and Connection Guide page 3-3).
- Never connect the Guard terminal to any output, including circuit common, chassis ground, or any other guard terminal. Doing so will damage the SMU (See Configuration and Connection Guide page 3-5).

We have three Probe Stations, Cascade Microtech with triaxial connectors, SemiProbe, which has BNC connectors, and Signtatone with RCA connectors. In order to connect B1500A with cascade, you can simply use grey wires and make the connection between the two. If the Design Under Test (DUT) has 4 or less terminals and testing temperatures will be between -55C to 125C, use Cascade. If DUT has more I/O than SemiProbe, use triaxial to BNC adaptors to make a connection between Semiprobe and B1500A.

3 EasyEXPERT

EasyEXPERT is the user interface for B1500A (see EasyEXPERT documents for complete understanding). EasyEXPERT main window is shown in Fig. 82. On the left side, *Application Test* (Red) and *Classic Test* (Yellow) are highlighted. *Application Test* has almost all the device

characterization test already defined; Keysight called them *Test Definitions*. But in the *Classic Test,* you need to set all the parameters manually.

3.1 Application Test

In Application Test, different devices are categorized by their technology name, such as CMOS, BJT, etc. (see User's Guide Volume 2, pg 9-3 for a complete list of categories). The green box in Fig. 82 shows the Category area. Each category has a set of libraries where Test Definitions are defined for that particular technology, and the orange box shows the Libraries. In Fig. 82, the Id-Vd library is selected, which is in the CMOS category.

The blue box highlights Device ID and Count on the top right side. EasyEXPERT uses these two for naming the data files. The number of count increase with every measurement. Set Device ID as Die_*_C*R*_<Type of Characterization>, it's just an example. Change it as per your requirement. The *device Parameter* area has Polarity, it is set to Nch for NFET device, and it can be set to Pch for PFET device. Setting it to Pch EasyEXPERT changes the polarities for the Gate terminal and flips the Y-axis.

In Fig. 82, the Vd-Id Test definition is selected for NFET (for PFET change *NCH* to *PCH* in *Device Parameters area* → *Polarity*). Four SMU's are used in this test definition; Drain of the NFET is connected to SMU6:MP (Medium Power), which is set as Primary Sweep. Sub is connected to SMU5:MP, which is a constant at 0V. Gate is connected to SMU4:HR (High Resolution), which is a Secondary sweep. And Source is connected to SMU3:HR, which is common to all. In this example, the Drain terminal of the device is connected to SMU6 on the back side of Keysight and that is why SMU6 is selected here, but if the Drain terminal is connected to SMU4 and SMU4 needs to be selected here instead of SMU6. The same scenario is valid for all other terminals of NFET.

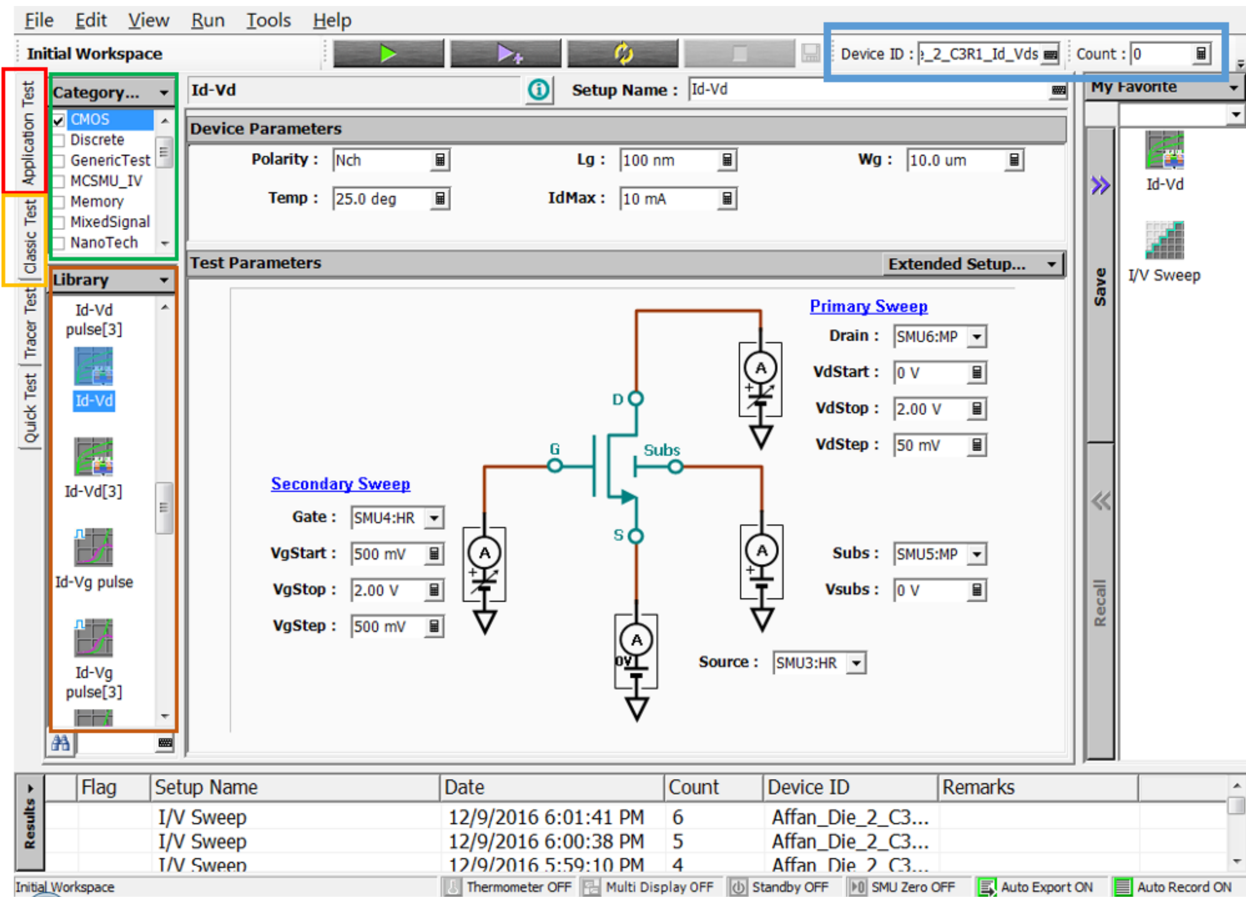

Fig. 82. Main window.

3.2 Edit Test Definition

By default, the voltage values set in Test Definitions are between 0V and 5V, but some processes like the SiC process need 12V or 15V to operate. So it needs some editing in the test definitions. Following are the steps to open and change the test definitions:

a. Select the Test Definition that you need to edit and click on Library.

b. Click Open (as shown in Fig. 83)

c. You will see a similar window, as shown in Fig. 84. The Id-Vd Test Definition is opened in this figure, and VgStart is selected (bottom red box). In properties, Min and Max's values are

defined, Max is set to 5V to get higher voltage than 5V set this to your required Max value. For example, for the Raytheon SiC process, we can set it to 15V.

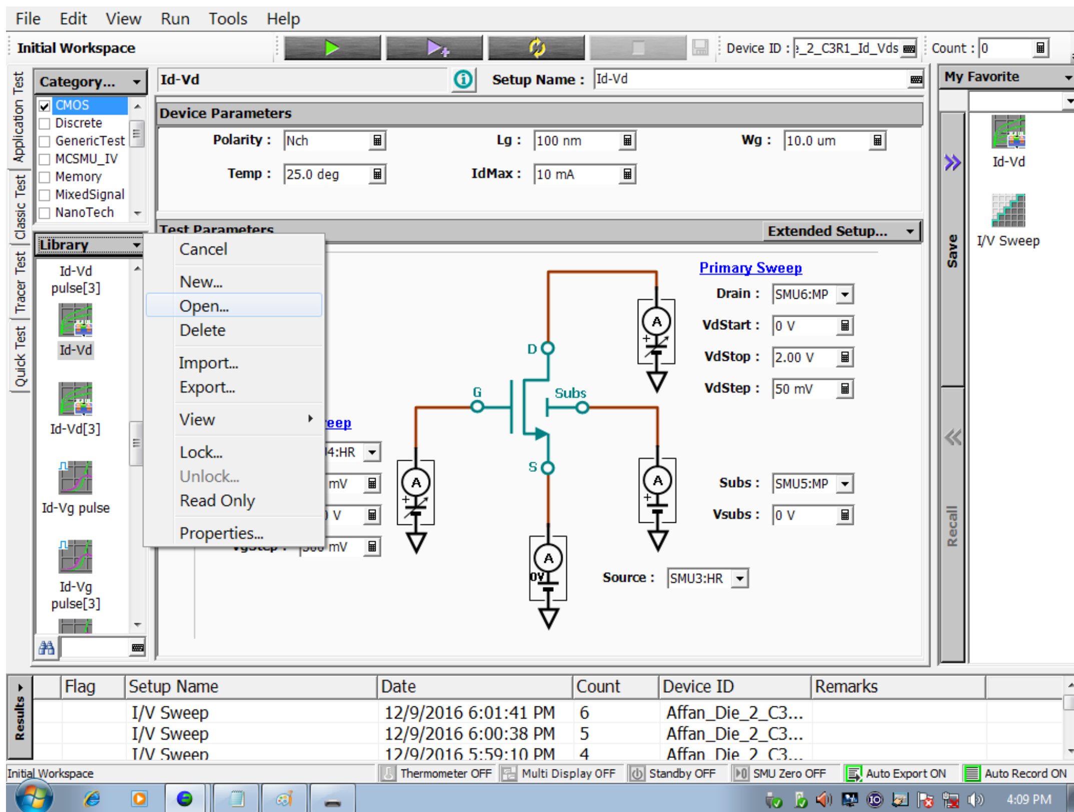

Fig. 83. Edit test definition.

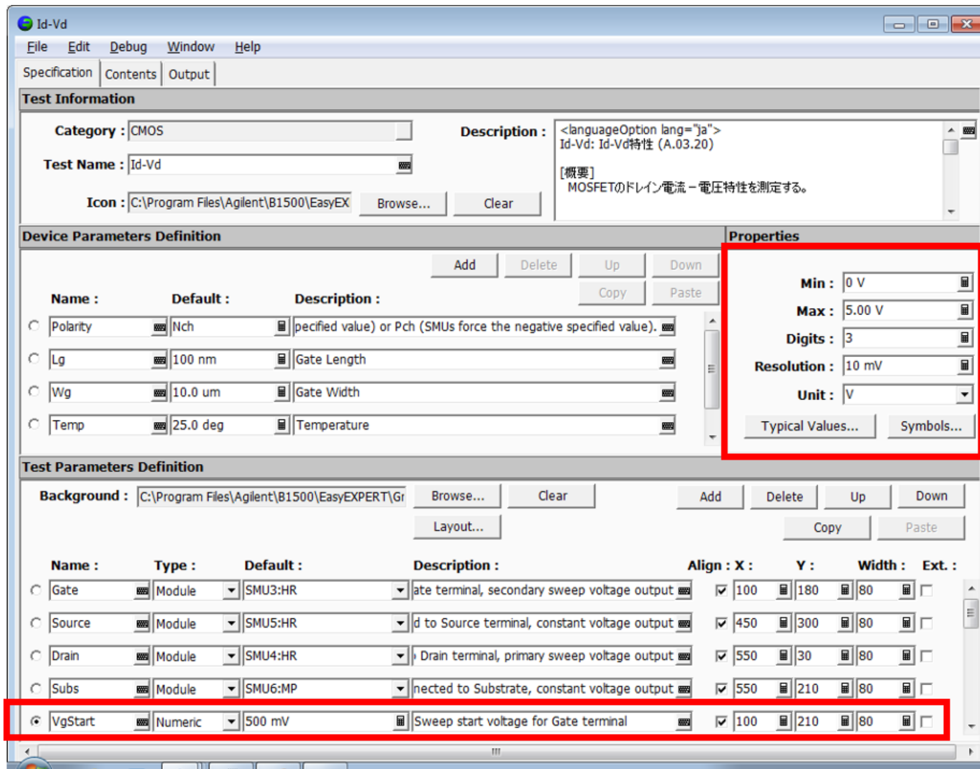

Fig. 84. Id-Vd test definition.

3.3 Classic Test

In the Classic Test, all the parameters need to be set manually, unlike the Application Test. In Classic Test, there are several categories based on the type of characterization, such as I/V Sweep, C-V Sweep, etc. (see EasyEXPERT User's Guide Volume 1 for complete detail).

Fig. 85 shows the I/V Sweep classic test window. Channel tab is selected in this figure; here user adds and deletes the SMUs based on the requirement, adds labels for voltage and current, which is useful to read logged data, select the mode for each SMU and select the function for each SMU. Here mode for SMU2 is selected as COMMON, which means it is GND/COMMON to all other SMUs. SMU6 is selected as VAR1, which means that the user can set this SMU for sweeping. SMU's with the function set as CONST means constant value they can not be used for sweeping, user need to specify the constant value to them.

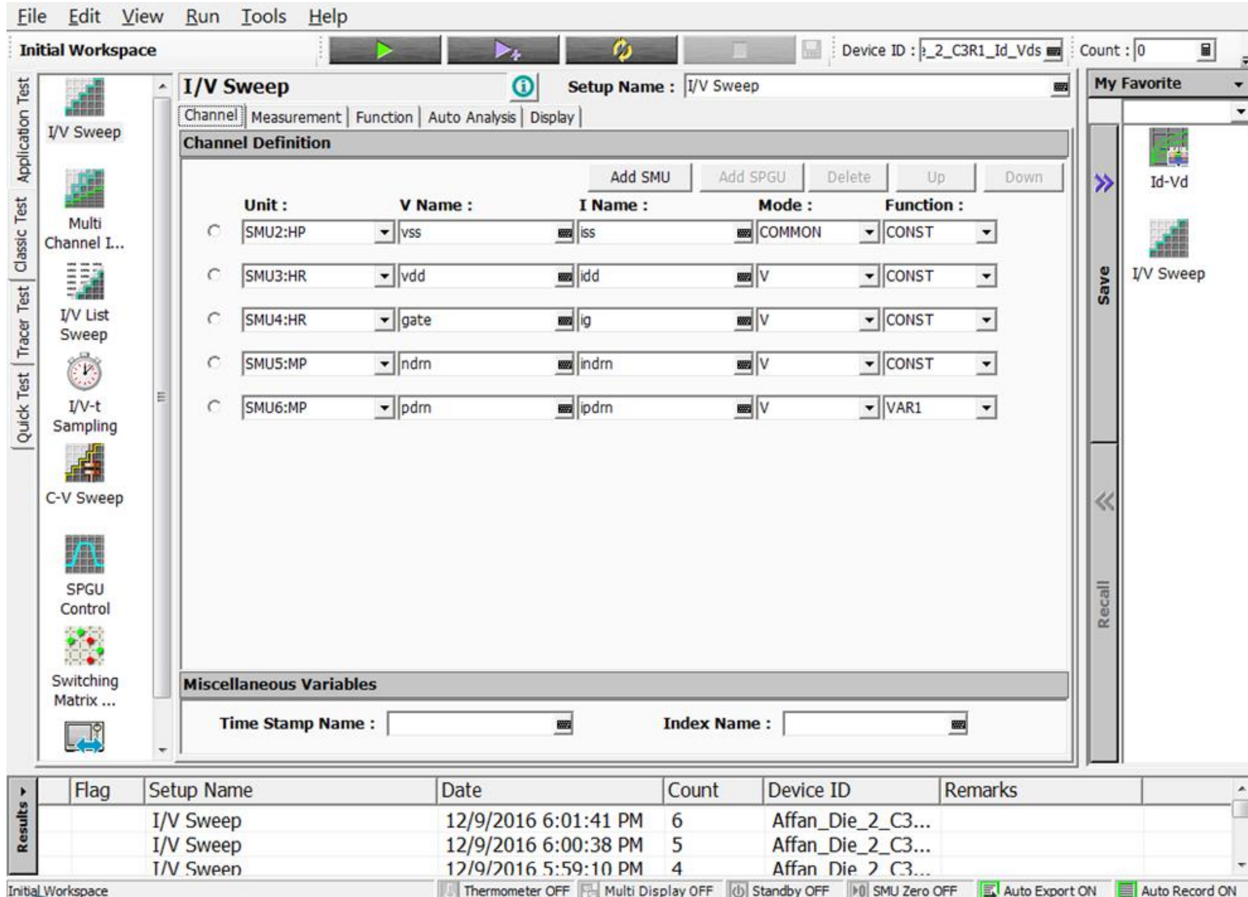

Fig. 85. I/V sweep classic test.

Fig. 86 shows the measurement tab where the user set the sweeping and constant values. The highlighted area in orange shows the VAR1 (Primary) and VAR2 (Secondary); sweeping parameters are needed to be defined here. In this figure, VAR1 is sweeping from 0 to 250mV with a step size of 2.5mV (i.e., 101 steps), and VAR2 is sweeping from 0 to 250mV with a voltage step of 50mV (i.e., 6 steps). The Green highlighted area shows the area where constants need to be defined. Compliance value is the maximum amount of current or voltage that can be drawn through that particular SMU. These values should be set according to DUT if your device is capable of drawing 1mA max. So set this value to 1mA; this will avoid damaging the device in case of some mishap.

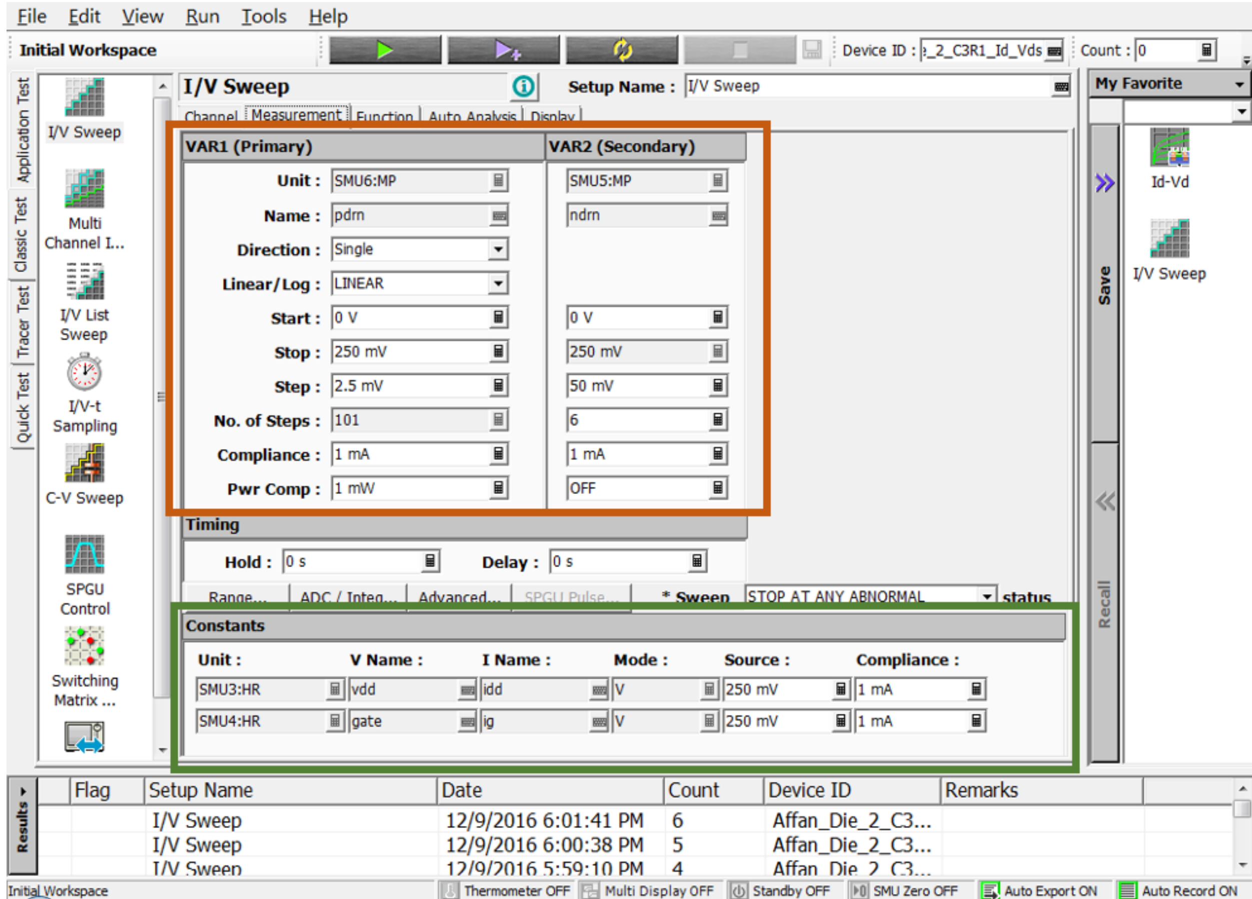

Fig. 86. I/V sweep measurement tab.

4 Export Data

Measured data can be automatically saved through EasyEXPERT. It's a nice feature when a massive amount of data needs to be captured. Users can save data in CSV form by enabling data export in EasyEXPERT. Waveform images can also be saved in png, BMP, etc., by enabling image capture.

To enable automatic data export, follow these steps:

a. Goto EasyEXPERT main window

b. Click File → Export → Data → Options → Auto Export (Fig. 87)

c. A new window will open ("Test Results Data Auto Export" as shown in Fig. 88); check Enable Automatic Data Export and set the folder where the data needs to be saved.

d. Select File type as CSV.

e. In the same window, check Enable automatic data export as an image file and set the folder. Images can be saved in the same data folder that is selected in step c.

f. Sometimes an image does not capture completely (no idea why), so check the captured image every time you run a test. And if it does not capture, then save it manually by going to File in Graph Window (as shown in Fig. 89) and then click on Save Image.

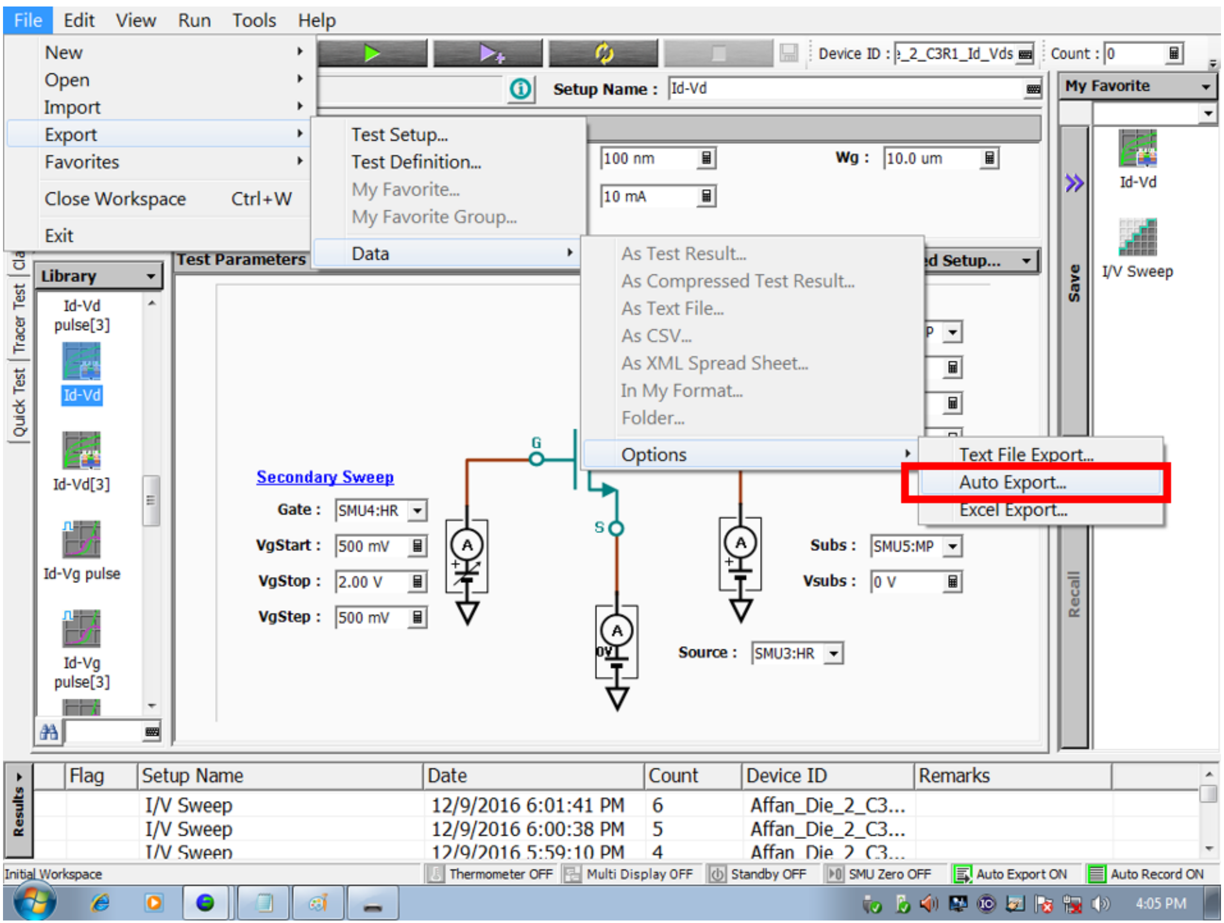

Fig. 87. To enable automatic data export.

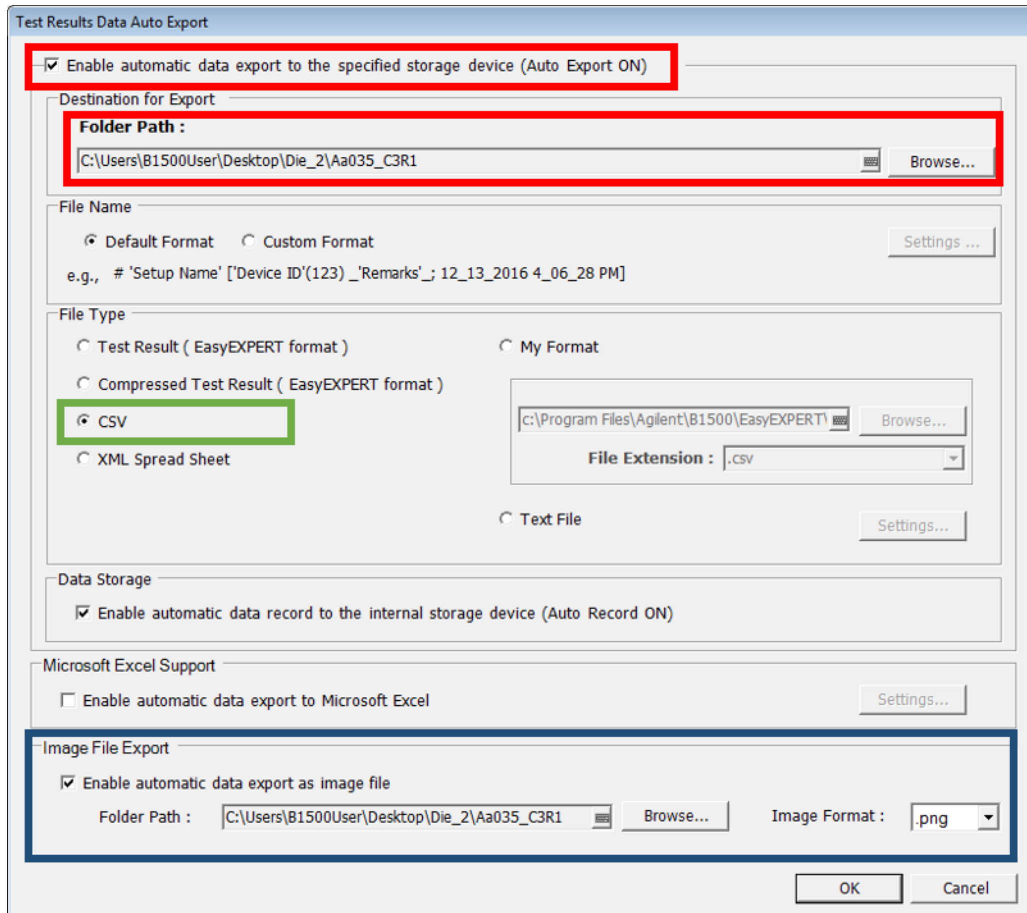

Fig. 88. Test results data auto export.

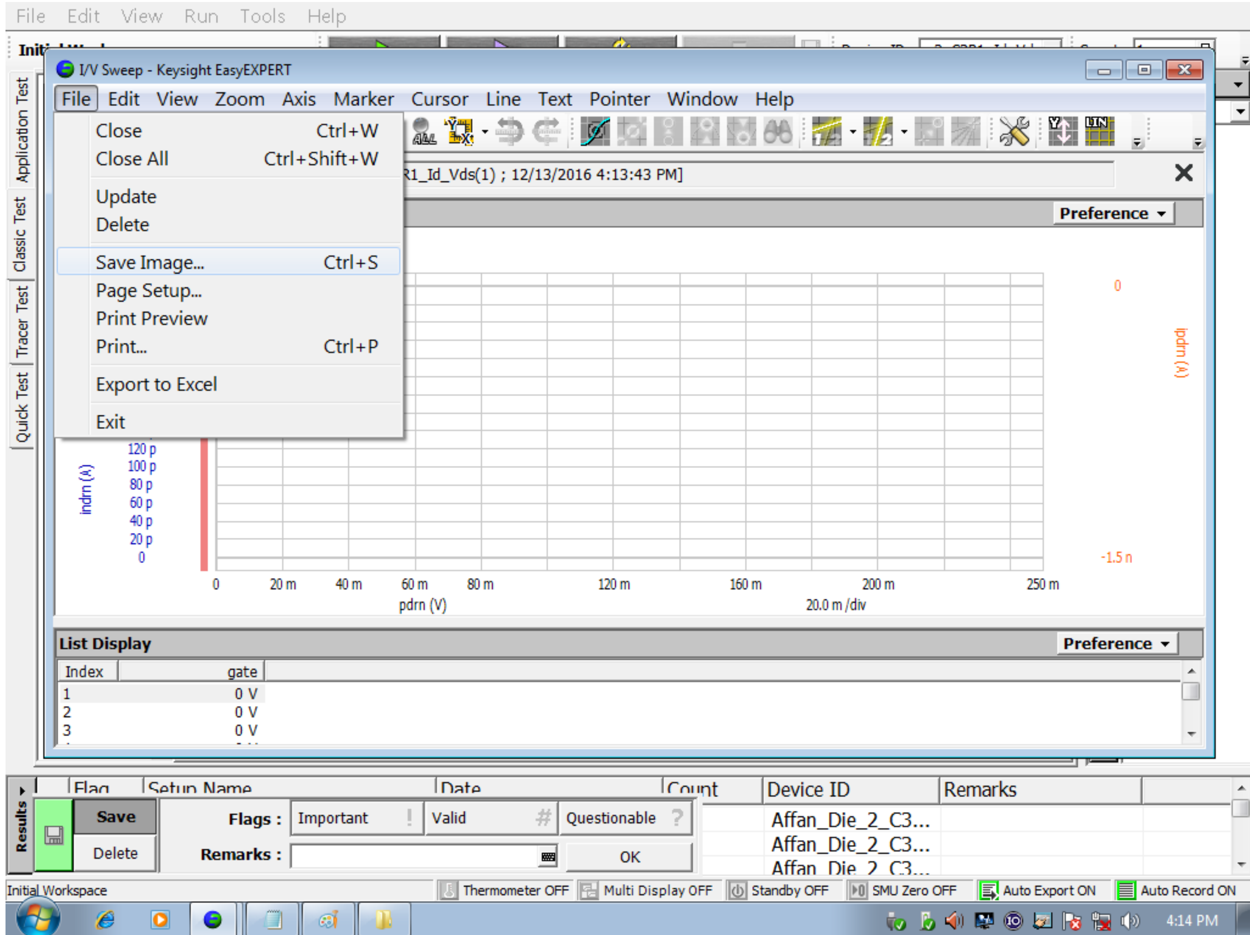

Fig. 89. Graph window.

Appendix C

Matlab codes for extracting SNM, RSNM, WSNM from the measured data.

SNM

```
[th1, r1] = cart2pol(V1_L, V2_R);
[x1, y1] = pol2cart(th1+pi/4, r1);
[th2, r2] = cart2pol(V2_L, V1_R);
[x2, y2] = pol2cart(th2+pi/4, r2);
Min_1=min(y1);Max_1=max(y1);Min_2=min(y2);Max_2=max(y2);
hold on;plot(x1,y1);plot(x2,y2);
SNM1=Max_2-Min_1
SNM2=Max_1-Min_2
```

RSNM

```
[th1, r1] = cart2pol(V1_L, V2_R);
[x1, y1] = pol2cart(th1+pi/4, r1);
[th2, r2] = cart2pol(V2_L, V1_R);
[x2, y2] = pol2cart(th2+pi/4, r2);
[Min_y1,Idx]=min(y1);
Min_x1=x1(Idx);
Min_y2=interp1(x2,y2,Min_x1);
hold on;
plot(x1,y1);
plot(x2,y2);
plot([Min_x1,Min_x1],[0,20],'k--');
```

WSNM

```
[th1, r1] = cart2pol(V1_L, V2_R);
[x1, y1] = pol2cart(th1+pi/4, r1);
[th2, r2] = cart2pol(V2_L, V1_R);
[x2, y2] = pol2cart(th2+pi/4,r2);
```

```
a=y1(30:101,:);
[Min_y1,Idx]=min(a(:));
Min_x1=x1(Idx+29);
Min_y2=interp1(x2,y2,Min_x1);
hold on;plot(x1,y1);plot(x2,y2);
plot([Min_x1,Min_x1],[0,20],'k--');
SNM1=Min_y1-Min_y2
```