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Design and Assembly of High-Temperature Signal Conditioning System
on LTCC with Silicon Carbide CMOS Circuits

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy in Engineering with a concentration in Electrical Engineering

by

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May 2021
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This dissertation is approved for recommendation to the Graduate Council.

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Abstract

The objective of the work described in this dissertation is to develop a prototype electronic module on a low-temperature co-fired ceramic (LTCC) material. The electronic module would perform signal conditioning of sensor signals (thermocouples) operating under extreme conditions for applications like gas turbines to collect data on the health of the turbine blades during operation so that the turbines do not require shutdown for inspection to determine if maintenance is required. The collected data can indicate when such shutdowns, which cost $1M per day, should be scheduled and maintenance actually performed. The circuits for the signal conditioning system within the prototype module must survive the extreme temperature, pressure, and centrifugal force, or G-force, present in these settings. Multiple fabrication runs on different integrated silicon carbide (SiC) process technologies have been carried out to meet the system requirements. The key circuits described in this dissertation are a set of two-stage op amp topologies and a voltage reference, which were designed and fabricated in a new SiC CMOS process. The SiC two-stage op amp with PFET differential input pair showed 48.9 dB of DC gain at 500°C. The voltage reference is the first in SiC CMOS technology to employ an op amp-based topology. The op amp circuit in the voltage reference is a two-stage topology with an NFET differential input pair that uses the indirect compensation technique for the first time in a SiC CMOS process to provide 42.5 dB gain at 350°C. The designed prototype module implemented with these circuits was verified to provide signal conditioning and signal transmission at 300°C. The signal transmission circuit on the module was also verified to operate with a resonant inductive wireless power transfer method at a frequency of 11.8 MHz for the first time. A second prototype module was also developed with a previously fabricated set of circuits in a 1.2 μm SiC CMOS process. The second module was successfully tested (with wired power supply) to operate at 440°C inside a probe station and also

verified for the first time to sustain signal transmission (34.65 MHz) capability inside a spin-rig at a rotational speed of 10,920 rpm, which corresponds to approximately 16,000 Gs. All designed modules have dimensions of 68.5 mm by 34.3 mm to conform to the physical size requirements of the gas turbine blade.

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Chapter 1. Introduction

1.1. Motivation

There is a need for increased efficiency and reduced emissions from applications like combustion engines or natural-gas driven power generators due to their impact on global greenhouse gas emissions. In the case of the gas-fueled power generators, the system uses turbines that have multiple components that operate under extreme temperature (>> 350°C), pressure/G-force (> 10,000 RPMs or 16,000-Gs), and a corrosive environment resulting in degradation of these components. These degradations will lead to the failure of critical components like the turbine blades and eventually affect the power generation system's efficiency and increase the cost of producing electric power. To counter these issues, research and development of long-term monitoring capability of the turbines' components are necessary. Such effort would require sensors with signal conditioning, power supply, and interfacing electronics to operate under the gas turbines' harsh ambient conditions. Established process nodes on bulk silicon or silicon-on-insulator (SOI) can provide excellent electrical performance. However, at temperatures above 350°C compounded with 16,000 G force (due to high rotation speed), silicon electronics cannot sustain such conditions. The intrinsic carrier concentration of silicon rises significantly at high temperatures, causing high leakage current to flow, resulting in channel flooding, excess carriers, and thermal runaway to eventual device damage. SOI process nodes can handle up to 300°C, above which the SOI circuits' functionality and reliability degrade [1]. Besides, sustaining the combination of the temperature and high G-force will be challenging for SOI devices.

Wide-bandgap materials and the research in silicon carbide (SiC) integrated electronics [2] can provide the platform to design the sensor front-end electronics that can operate at the extreme ambient conditions. SiC electronics can provide the capability to perform long-term component

health monitoring for gas-powered generator systems. Siemens has implemented Chromel-Chromel thermocouple sensors inserted on the gas turbine blades to monitor the component's health. However, such thermocouples' sensed signal is in 10s to 100s of millivolts in range and therefore requires a signal conditioning system to boost the sensed signal. In addition to that, modulation schemes and signal transmission capability are also necessary as receiving the conditioned sensed signal through a wired medium will result in signal loss. Finally, the signal conditioning circuits require power to operate. Henceforth, the supportability of power delivery through both wired and wireless mediums must be present with limited wire feedthrough paths.

Previously, such sensor electronic systems [3], [4] have been designed on ceramic modules using a SiC JFET process from the NASA Glenn Research Center [5]. The developed sensor electronic system using the SiC JFET circuits was tested at high-temperature. However, no literature was found mentioning the electronic system operating under high rotational speeds or high G-force of above 10,500 RPM. Additionally, the JFET signal conditioning system lacked an op amp for sensor signal amplification, instead used only a differential amplifier which makes the gain of the amplifier difficult to control. In the op amp case, the gain can be controlled by using a ratioed resistor under closed-loop. The Glenn Research Center has performed more than a decade of research in developing the SiC JFET devices and has shown SiC circuits operating at 500°C for long hours [6-8]. However, the process does suffer from long fabrication times along with lacking the compatibility of a complementary device, requires dual-rail supplies, and is incapable of incorporating any compact digital circuit block for mixed analog-digital (i.e., mixed-signal) circuits. Other reported SiC processes include a bipolar process from KTH and the, now defunct, SiC CMOS process (called HiTSiC®) from Raytheon Systems Limited in the United Kingdom (RUK).

The SiC bipolar circuits from KTH have previously shown the capability of operating at 500°C. However, similar to the JFET, the process only supports a non-scalable NPN device and, due to the bipolar nature, exhibits high power dissipation [9-13]. The wafer-to-chip turn-around time for this bipolar process is approximately eight months.

The SiC CMOS process from Raytheon UK (RUK), in collaboration with the University of Arkansas (UA), demonstrated analog and complex mixed-signal circuits capable of operating at temperatures above 350°C [14-17]. The op amps in the Raytheon process had shown functionality at 400°C, and digital circuits like the ring oscillator had shown to sustain operation for 30 hours at 470°C. However, with the Raytheon SiC foundry's shutdown back in 2017, a renewed interest in developing another SiC CMOS process technology has grown. Later on, the UA IC-MSCAD team collaborated with the Fraunhofer IISB foundry to develop the process flow, form design rules, and create integrated circuits with higher density and temperature sustainability on a new SiC CMOS process [18]. Therefore, the target with a newly developed SiC CMOS process would be to support the design and operation of the electronic modules or systems to perform signal conditioning of sensed signals under the extreme ambient specifications.

1.2. Design Approaches

As the research is directed towards a signal conditioning system design on LTCC material using the advantages of SiC integrated circuits operating at temperatures of 350°C and above, three design approaches, based on three different process-technologies, have been investigated to realize the signal conditioning system with wired and wireless power delivery. Fig. 1 shows the top-level block diagram of the three design approaches.

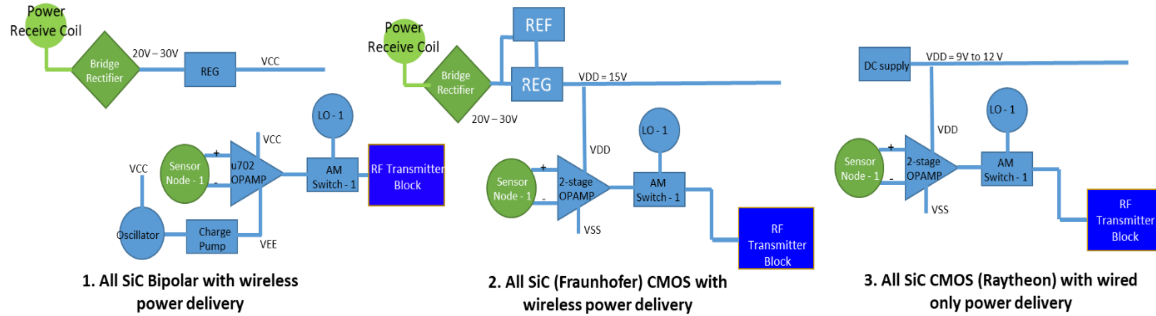


Fig. 1. Top-level design approaches for signal conditioning system: (i) SiC bipolar based, (ii) 1.5 µm new SiC CMOS (Fraunhofer) based, and (iii) 1.2 µm old SiC CMOS (Raytheon) based.

The first two design approaches are intended to operate with both wired and wireless power supplies, whereas the third approach would only support wired power supply. The third design approach uses the old SiC CMOS process from Raytheon that lacks the reference circuit that would meet the requirement for the regulator circuit. The regulator circuit on the Raytheon process requires separate biasing circuitry for the internal op amp which would mean insertion of additional components. The system is intended to operate above 400°C while sustaining functionality after thermal cycling. This means the signal conditioning system needs to function at room temperature after a successful operation at high-temperature. The first two design approaches would facilitate the fabrication of new circuits to support wireless power delivery, shown in Table I. The first design approach involves the complete signal conditioning system design in a SiC bipolar process that requires dual (positive and negative voltage rails) supplies. This is necessary to lower the common-mode of the sensor amplifier (op amp) in order to amplify low voltage signals from thermocouple sensors. To realize the negative rail, a charge pump and oscillator circuit are required. The positive rail will be provided from the regulator, which stabilizes the rectified output from the rectifier circuit. The SiC bipolar circuits are intended to operate at 500°C as the process has previously shown circuits that operated at 500°C. For the second design approach on the new SiC CMOS process, a new reference and regulator circuit are designed to regulate the rectified

output. The circuits on this new SiC CMOS process are designed on two separate metallizations - (i) Aluminum (Al) and (ii) Platinum (Pt) - with the latter intended to operate at temperatures up to 500°C with repeatability of circuit functionality after thermal cycling. The aluminum metallization circuits are intended for operation at 350°C.

Table I. Initial System Specification of the Circuits for the Signal Conditioning System

Specs	Design Approach 1	Design Approach 2	Design Approach 3
	Range/Value (unit)	Range/Value (unit)	Range/Value (unit)
Rectified Supply	20-30 V	20-30	-
Regulated VDD/VCC	10 V	15 V	9-12 V
VSS/VEE	- 4V	0 V	0 V
Max. Operable Temperature	450°C – 500°C	400°C - 450°C	350°C (Al) 450°C – 500°C (Pt)
Reference Voltage for Regulator	4.5 V – 5 V	3.5 V – 4.5 V	-
System current consumption	30 mA	30 mA	10 mA
Center frequency for FM modulation	30 - 40 MHz	30 - 40 MHz	30 - 40 MHz

1.3. Research Objectives

In addition to designing integrated circuits in SiC bipolar and the new CMOS process technologies, the broader objective of this research was to develop and assemble a signal-conditioning system on a low-temperature co-fired ceramic (LTCC) module using SiC circuits that could be embedded with the sensors on the turbines or combustion engines of gas-fueled power generators. The electronic module should operate both at high-temperature and high rotational speeds/G-force to

allow continuous monitoring of the key components within the turbine system. The application requirements pose significant challenges in selecting the circuit components to design the signal conditioning system including: transmit/receive the sensed signal, passive parts, epoxy materials, and wiring. Assembly methods and techniques to deliver power over the wireless medium to the circuits was also a challenge. The purpose of this research involves addressing these challenges in the following steps:

a. Selection of SiC process (KTH-Bipolar or Fraunhofer-CMOS) and carry out fabrication runs in two phases – (i) first tapeout intended to characterize the device structures to understand the issues and limitation of the process. (ii) second tapeout intended to utilize the results from device characterization to design SiC analog circuits for fabrication
b. Test and characterize the fabricated circuits over temperature for functionality and performance analysis. Based on the results, select the circuits to implement the signal conditioning system
c. Design the signal conditioning module with signal transmission capability in two phases – (i) Implement the first module with the proven and functional circuits from Raytheon SiC CMOS, or HiTSiC®, process, and (ii) Implement the second module design with recently fabricated circuits from KTH-Bipolar and Fraunhofer-CMOS processes
d. Establish the setup to receive the signal from the module and also the method to deliver power to the circuits on the module
e. Establish the assembly method to attach the components and wiring to the module to support high-temperature and high rotational speed testing

1.4. Key Contributions

The dissertation establishes few key contributions to the research areas of high-temperature SiC CMOS circuit design and high-temperature telemetry module design in LTCC material. These important contributions discussed in this dissertation are listed below:

a. Design of low quiescent signal conditioning circuits in SiC bipolar process technology
b. Design different multi-stage op amp topologies in a new SiC CMOS process technology
c. Design the first op amp based reference circuit in SiC CMOS process
d. Design multiple electronic modules on LTCC material with SiC circuits from Raytheon and Fraunhofer to implement the signal conditioning system with signal transmission capability
e. Successful testing of the signal conditioning system on the Raytheon LTCC module at temperature up to 440°C and rotational speed of 10,920 RPM
f. Layout methods on LTCC modules to implement wireless power transfer resonant inductive coupling
g. Develop wire-assembly methods on LTCC modules to support spin testing at high-speed and high-temperature
h. Verification of wireless power transfer with SiC CMOS circuits
i. Published two articles [21], [36] and one under revision [37] in reputed peer-reviewed journals on topics related to the research described in Chapter 2 and Chapter 3 of this dissertation.

Table II and Table ***III*** show the summarized measured specifications of the different versions of the Raytheon and Fraunhofer modules. Both modules are designed with dimensions of 68.5 mm by 34.3 mm. Raytheon module-1 had multiple via openings resulting in the module not being used for system assembly, testing, or verification.

Table II. Measured Results of the Raytheon Modules

Supports wired power delivery	**Raytheon Module-2**	**Raytheon Module-3**	**Comments**
Applied supply range	9 - 12 V	9 - 12 V	
Current Draw at 25°C	4 mA	6 mA	
LC-tank oscillator source resistance	2.4 kΩ	1.6 kΩ	
Transmission center frequency	34.25 MHz	34.94 MHz	
High-speed test	Failed at 10,124 RPM	Passed at 10,920 RPM	
Temperature test	Functioned at 350°C	Functioned at 440°C	The second iteration of module-2 failed to provide signal transmission above 410°C due to higher source resistance (the first iteration got damaged during high-speed testing). Module-3 operated at 440°C due to lower source resistance
System function repeatability at room temperature after thermal cycling	Passed for full system	Passed for full system	
Lowest sensor input signal applied to detect frequency deviation	50 mV	50 mV	The signal applied to the signal conditioning op amp (op amp input offset is below 30 mV for op amps on both the modules)

Table III. Measured Results of the Fraunhofer Module

Supports wired and wireless power delivery	**Fraunhofer Module-1**	**Fraunhofer Module-2**	**Fraunhofer Module-3**	**Comments**
Rectified supply	20 V	20 V	20 V	(maximum can go up to 25 V due to minimizing leakage current)
Current Draw at at 25°C	19 mA	19 mA	21 mA	
LC-tank oscillator source resistance	1.6 kΩ	1.6 kΩ	1.5 kΩ	
Transmission center frequency	failed	34.25 MHz	34.94 MHz	The transmission circuit failed to operate on the module-1
High-speed test	-	-	-	Fraunhofer modules not tested at high-speed
Temperature test	Op amp failed and regulator output unstable at 350°C	Full system functioned at 300°C	Individual circuits functional at 350°C	Module-2 provided the full system functionality with modulated signal transmission. Tested at 300°C due to use of 95/5 Pb/Sn solder
System function repeatability at room temperature after thermal cycling		Passed for full system	Passed (for individual blocks)	Failure of the signal conditioning op amp die
Lowest sensor input signal applied to detect frequency deviation		50 mV	50 mV	The signal is applied to the signal conditioning op amp. Op amps on module-2 and module-3 have 1.8 V and 0.6 V of input offset respectively

1.5. Dissertation Outline

The main contents of this dissertation are divided into four chapters:

- Chapter 2: Silicon Carbide Process Selection and Device Characterization

- Chapter 3: Overview of Designed Silicon Carbide Circuits in the Fraunhofer CMOS Process
- Chapter 4: Silicon Carbide Signal Conditioning System Prototypes on LTCC
- Chapter 5: LTCC Module Test Results

Chapter 2. SiC Process Selection and Device Characterization

This chapter focuses on detailing the two SiC processes investigated to design the circuit blocks required to realize the extreme environment signal conditioning system. Two fabrication runs with the SiC bipolar process from the KTH Electrum lab were completed, with each run taking approximately eight months of turnaround time from submission to completion (i.e., wafer-to-chip). The first bipolar run (or PASS0) focused on developing functional analog circuit blocks (op amp, charge pump, regulator, and reference circuit) with a low quiescent current. The second bipolar run (or PASS1) focused on improving the circuit performance from PASS0.

Similar to the bipolar run, the SiC CMOS process from Fraunhofer IISB was used for two fabrication runs, with the first tape-out (PASS0) requiring 18 months of wafer-to-chip turnaround time and the second tape-out (PASS1) requiring nine months. The PASS0 run was intended to establish the SiC CMOS fabrication flow and characterize fabricated devices for high-temperature operation. The PASS1 run focused on improving the fabrication flow, minimizing the shortcomings observed on the PASS0 run, and design fundamental analog circuit blocks (op amp, reference generator, voltage regulator, and oscillators).

2.1. SiC Bipolar Process: KTH PASS0 and PASS1 Fabrication Runs

The SiC bipolar fabrication is ion implantation-free. All the necessary base, collector, and emitter nodes on the transistor are formed by etching each layer. Both the PASS0 and PASS1 followed the same fabrication steps. The complete fabrication flow for this bipolar process, including the routing metallization, has been illustrated in detail in the literature [19], [20]. The description of the circuit operation and performance over temperature from PASS0 are also detailed in the literature [21], [22]. This dissertation paper will not describe the fabrication flow/steps for the SiC

bipolar process and the PASS0 circuit performance. Instead, this section will briefly describe the designed circuits for PASS1 and discuss the reason for the circuits' post-fabrication failure.

The PASS1 run, similar to PASS0, used CREE's 100 mm 4H-SiC wafers. Two wafers were fabricated in the PASS1 run. Each wafer has 58 reticles diced on 10 mm × 5 mm individual die. Each of these reticles is later sub-diced in two 5 mm × 5 mm die for testing and characterization. The images for the two 5 mm × 5 mm diced die are shown in Fig. 2. All the diced 5 mm × 5 mm die include non-scalable 40 µm × 15 µm NPN structures. All the circuits are designed using this 40 µm × 15 µm NPN device, which imposes fairly strict limitations. Fig. 3 shows the mapping of the NPN transistor current gain variation across the two PASS1 wafers. Fig. 4 (Left) shows the die image of the NPN transistor. The probing/connection pads on the NPN transistor are 100 µm × 100 µm. The resulting current gain for most NPN structures from the PASS1 run is comparatively lower than PASS0, which provided a current gain of greater than 90. The NPN structures from wafer #1 showed higher current gain compared to wafer #2. The die with the transistor current gain of 84 was selected to characterize the current gain variation over temperature. Fig. 4 (Right) shows the NPN transistor current gain variation over temperature.

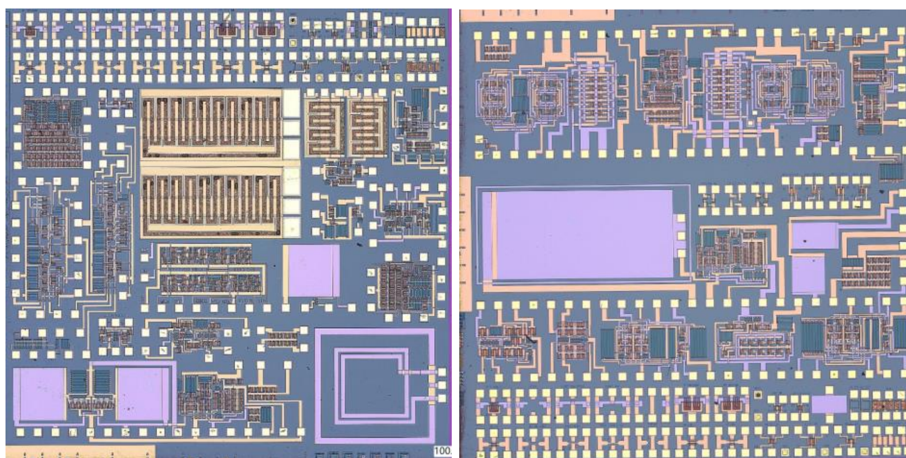
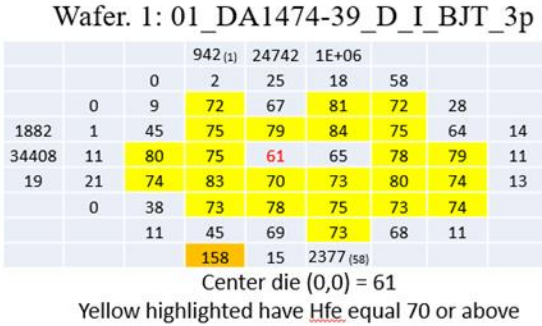


Fig. 2. Die micrograph of the complete 10 mm by 5 mm reticle from SiC BJT PASS1 run.

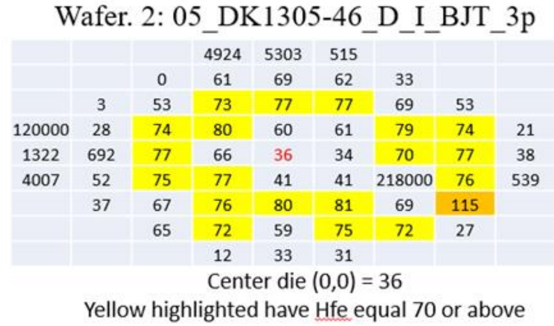
Wafer. 1: 01_DA1474-39_D_I_BJT_3p



			942 (1)	24742	1E+06			
		0	2	25	18	58		
	0	9	72	67	81	72	28	
1882	1	45	75	79	84	75	64	14
34408	11	80	75	61	65	78	79	11
19	21	74	83	70	73	80	74	13
	0	38	73	78	75	73	74	
		11	45	69	73	68	11	
			158	15	2377 (58)			

Center die (0,0) = 61
Yellow highlighted have Hfe equal 70 or above

Wafer. 2: 05_DK1305-46_D_I_BJT_3p



			4924	5303	515			
		0	61	69	62	33		
	3	53	73	77	77	69	53	
120000	28	74	80	60	61	79	74	21
1322	692	77	66	36	34	70	77	38
4007	52	75	77	41	41	218000	76	539
	37	67	76	80	81	69	115	
		65	72	59	75	72	27	
			12	33	31			

Center die (0,0) = 36
Yellow highlighted have Hfe equal 70 or above

Fig. 3. Wafer map showing the SiC BJT current gain variation for the two PASS1 wafers

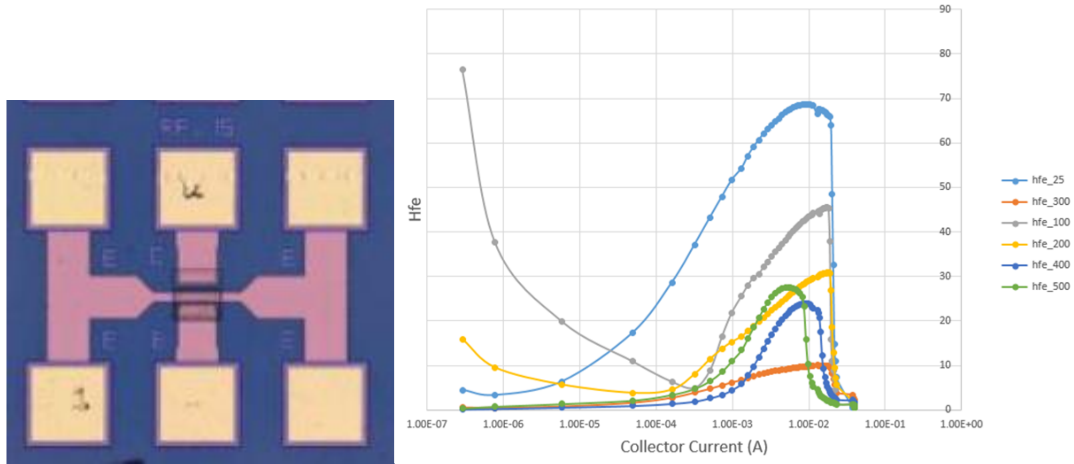


Fig. 4. (Left) Die image of the 40 µm by 15 µm SiC NPN transistor, (Right) current gain variation of the NPN device over temperature.

The current NPN transistor's current gain decreases until 300°C, after which it starts to increase. This behavior was also observed in PASS0 NPN devices and is caused due to occurrence of two opposing phenomena over temperature. As the temperature increases from room temperature to 300°C, the emitter injection efficiency drops as more ionization takes place in the base, resulting in the drop of current gain. The drop in the emitter efficiency is due to the increase in base doping (in standard silicon base doping is kept lower to minimize recombination of emitter injected electrons) as temperature increases causing the probability of emitter injected carrier (electron) to recombine in the base to increase. However, at temperatures above 300°C, the complete ionization has already taken place but the carrier lifetime begins to increase which causes the base recombination rate to decrease resulting in a slightly improved current gain.

As addressed earlier, the designed circuits in PASS1 were meant to be improved versions of the PASS0 circuits, although the bipolar fabrication was clearly not repeatable and did not improve, or even remain the same, from PASS0 to PASS1. Nonetheless, the key circuit blocks include –

1. The voltage regulator, designed to provide 12 V regulated output at 40 mA load current. The input supply variation over which the regulator was expected to operate safely was 20 to 40 V. This is due to the V_{CE} (collector-to-emitter) breakdown for the NPN devices in both PASS0 and PASS1 was approximately 45 V.
2. The voltage reference circuit with a diode clamp network was designed to provide 3.1 V reference output for a supply voltage range of 12 V to 20 V. The additional diode clamping network limits the supply voltage from crossing over 20 V.
3. The multi-stage op amp was designed with Darlington input pair NPN transistors to increase the op amp's input impedance. The high input impedance limits sourcing current to the op amp input nodes. It is necessary for sensing applications where the thermocouple sensors cannot source current above 10 nA.
4. The negative charge pump circuit was designed to provide a negative supply rail as the SiC bipolar process requires a dual-rail supply to attain a low common-mode range for signal conditioning op amps.

None of the circuits from PASS1 provided functionality during post-fabrication testing. The cause for the failure was traced to the large-valued collector resistors' improper fabrication [21], which were used as passive loads for all the circuits. The schematic view of Fig. 5. Schematic view of the multi-stage SiC Bipolar op amp with Darlington input pair. The layout view of Fig. 6. Layout view of the multi-stage SiC Bipolar op amp with Darlington input pair is shown in Fig. 6. The load resistor values (R_{TEST1} and R_{TEST2}) are indicated in the figures. During post-fabrication

measurements on this circuit, the measured load resistor values are significantly low. The measured values are given in Fig. 6. Layout view of the multi-stage SiC Bipolar op amp with Darlington input pair. The rest of the failed circuits showed similar problems. Fig. 7 and Fig. 8 show the schematic and layout view, respectively, for the voltage regulator circuit where the same issue with the collector resistor showing much lower values. The cause of failure of these collector resistors was traced to the incomplete etching of the collector layer on the resistor locations. As the resistors are laid out in a serpentine format using individual unit resistors, each of those unit resistors must be isolated from any nearby devices. To verify whether the isolation is formed correctly or not, after the collector layer's etching process, a pn-junction check for isolation is usually carried out. However, during the two PASS1 wafers' fabrication, such verification steps were not performed, and subsequently, the issues with shorted resistors went unnoticed.

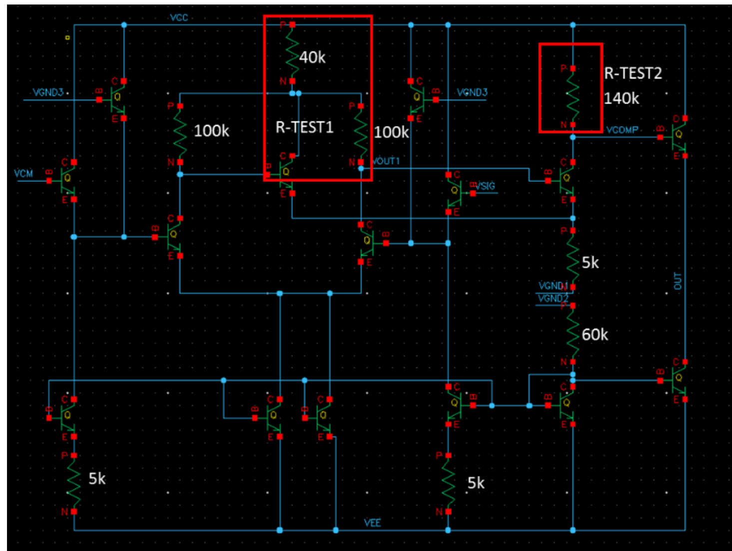


Fig. 5. Schematic view of the multi-stage SiC Bipolar op amp with Darlington input pair

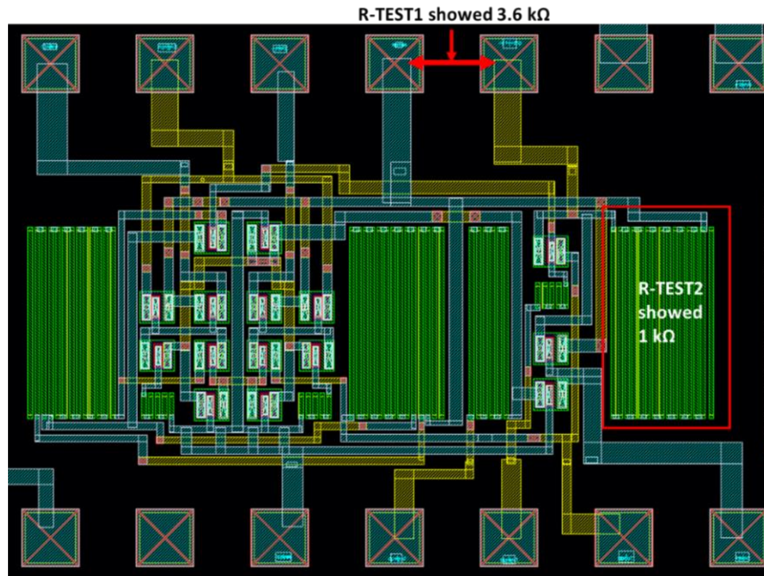


Fig. 6. Layout view of the multi-stage SiC Bipolar op amp with Darlington input pair

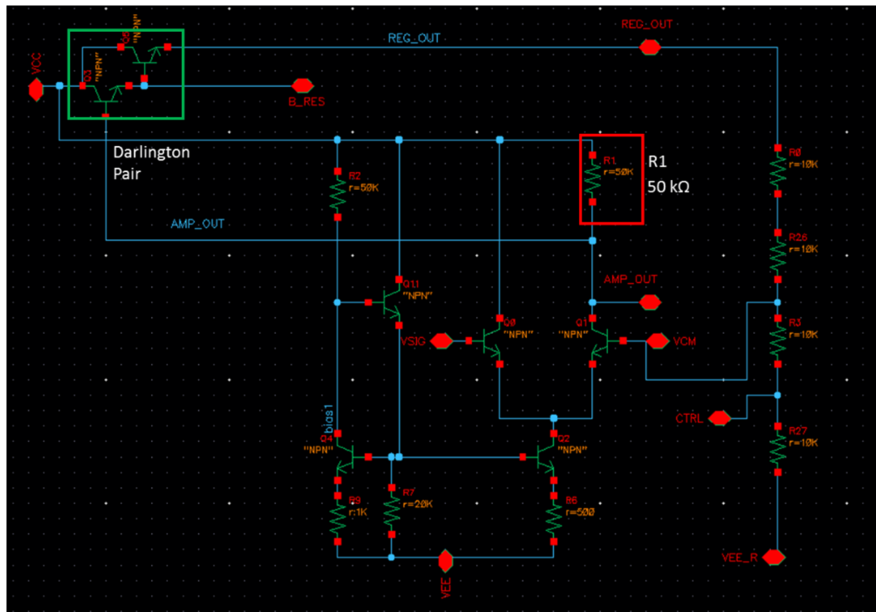


Fig. 7. Schematic view of the SiC Bipolar linear regulator to provide 12 V, 40 mA output

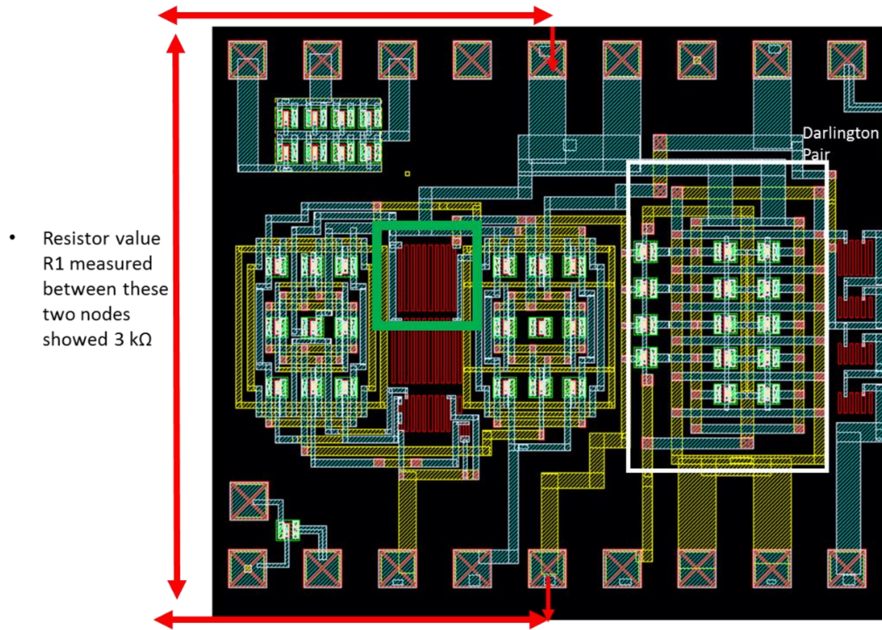


Fig. 8. Layout view of the SiC Bipolar linear regulator to provide 12 V, 40 mA output

2.2. SiC CMOS Process: Fraunhofer PASS0 and PASS1 Fabrication Runs

The first fabrication run, PASS0, included six wafers to establish the design rules and validate the fabrication flow. The critical challenges in the fabrication of SiC CMOS devices to standard silicon CMOS are high-energy ion implantation and the high temperature annealing. Due to the higher bandgap energy and strength of SiC bonds in the lattice structure, the standard diffusion techniques for well or channel doping are no longer viable. Ionization energies as high as 540 keV for PWELL implantation and 810 keV for NWELL implantation are required to attain desired doping depths on the SiC wafers. Nitrogen and aluminum dopants were to create the n-type and p-type doping. The high-energy ionization leads to crystal defects, and to minimize those defects, high-temperature annealing at 1700°C is necessary. Similar to the bipolar run, both the Fraunhofer fabrication runs used Cree's N-type 100 mm 4H-SiC wafers for fabrication. Before starting the fabrication at the facility, an n+-buffer layer and a p-type (Al) epitaxial layer were grown on the wafers from Ascatron. Ten masks set were used for processing the PASS0 run. The included mask

layer names are as follows: ALIGN, NWELL, PWELL, P+, N+, ACTIVE, POLY, POLYVIA, OHMIC CONTACTs (one layer for both n/p-type contacts), and METAL-1. In the PASS1 run, two other masks were included - POLYCIDE (for poly silicidation with titanium) and PASSIVATION. The initial doping concentration levels for the wells in PASS0 were selected by the foundry using TCAD simulations to attain 50 V of blocking capability between the NWELL and PWELL/P-epi.

The PWELL and the P+ regions were patterned first, followed by the NWELL and N+ regions to fabricate the transistors. The lithography sequence caused a reduction in P+ doping levels during the etching procedure for NWELL patterning. In PASS0, 500 nm thick n-type polysilicon was deposited on all the wafers. Before the polysilicon layer deposition, a 400 nm thick field oxide layer was formed using thermal oxidation at 1400°C. The ohmic contacts for the P+ and N+ regions in the drain/source/body connections were formed via 2.6% of Nickel-Aluminum (Ni-Al) silicidation [23], [24]. All transistor structures had a minimum via-opening of 9 μm^2. Both PASS0 and PASS1 had a single layer of metallization deposited through the chemical vapor deposition (CVD) process. Two metallization options for routing and bond pad formation were explored – (i) Titanium-Aluminum stack and (ii) Platinum-Titanium stack. The aluminum metallization used the resist based etching method for patterning, and the platinum metallization used the lift-off method. Bond pads for probing the transistor structures were 100 μm × 100 μm in dimensions.

2.2.1 Transistor Characterization from Fraunhofer PASS0 Run

Initial characterization was performed at the wafer-level through measuring the threshold variation across the wafer. The second wafer, or wafer #2, was selected to plot the change in threshold for a 20 μm × 1.5 μm PFET and NFET device at room temperature. Fig. 9 shows the wafer map and the respective change in threshold voltage for both PFET and NFET devices. The critical concern is

the low threshold of the NFET devices and the high threshold voltage of the PFET devices. The SiC transistors are expected to operate at high temperatures. However, with the NFET threshold being initially low, this threshold would drop significantly at higher temperatures, resulting in an unacceptable noise margin in applications such that the devices might turn on too easily. Additionally, for PFET devices with a high threshold, any cascode amplifier approach would require a larger supply voltage headroom to allow transistors to operate safely in the saturation region.

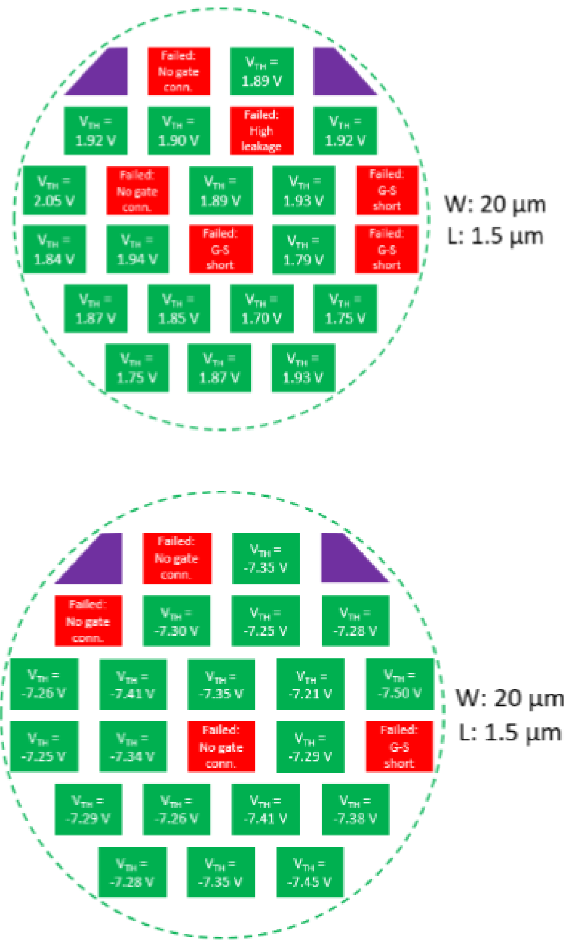


Fig. 9. Wafer map on V_{TH} variation of 20 µm by 1.5 µm NFET (top) and PFET (bottom) devices from Fraunhofer SiC CMOS PASS0 run.

Further characterization included measuring the output transfer characteristics for the 20 µm × 1.5 µm NFET and PFET devices from the PASS0 wafer #2 using Keysight Curve Tracer. The measured gate-oxide breakdown voltage for the transistor devices is 25 V at 10 pA of gate leakage current. Hence, the input or output DC characteristic curves were performed by sweeping the V_{DS} (drain-source) and V_{GS} (gate-source) voltages up to 20 V. Fig. 10 shows the NFET I-V plots for the applied V_{GS} 0 V to 19 V and V_{DS} of 0 to 20 V. For the PFET, the applied V_{GS} and V_{DS} are 0 V to -19 V and 0 V to -20 V, respectively. The PFET-to-NFET drain-current ratio is approximately 1:25 when both the devices are operating at a gate-source voltage of 19 V. The maximum drain current for the PFET devices is expected to be lower than the NFET devices due to higher threshold and lower hole mobility. However, the P-to-N drain-current ratio for the PASS0 run is significantly worse than expected. In a standard silicon process, this ratio is often 1:2 or at worst 1:3, and in the case of the previous SiC CMOS process from Raytheon, the ratio was 1:5. Table IV shows the drain current ratio at room temperature for various channel lengths with a fixed gate-source voltage. The drain current ratio tends to improve as channel length increases, primarily due to the reduction in short channel effects at higher channel lengths. The PFET I-V characteristics show a non-ohmic behavior (red circled) at lower drain-source voltage, which indicates that the P+ ohmic contacts on the PFET are not properly silicided during fabrication. The sheet resistance and contact resistance values for the P+ and N+ region for the six PASS0 wafers at room temperature are shown in Table V. The P+ contact resistivity is high. Typically, the contact resistivity for P+ contacts is expected to be within 0.5 to 1 $m\Omega \cdot cm^2$ in standard silicon process technologies. The N+ contact resistivity is, however, significantly lower in comparison.

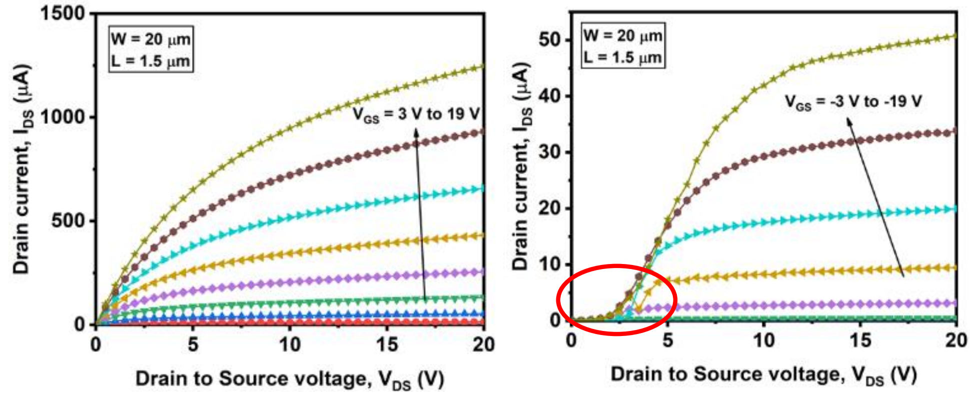


Fig. 10. NFET (Left) and PFET (Right) I-V plots from PASS0 wafer #1.

Table IV. PFET-to-NFET Drain Current Ratio from PASS0 Run for Different W by L Sizing

W/L (μm/ μm)	I_D-P (μA)	I_D-N (μA)	Ratio
20/1.5	50	1250	1:25
20/2	41.6	690	1:17
20/4	25	235	1:10
20/6	18.4	141	1:8
20/10	13.5	78.3	1:6

Table V. Contact Resistivity/sheet Resistance for n+ and p+ Regions of all the PASS0 Wafers

N+ in PWELL	W1	W2	W3	W4	W5	W6
R-sheet [kΩ/sq]	1.15	1.20	1.17	1.20	1.20	1.12
Contact-resistivity [μΩ·cm^2]	1.72	0.9	0.59	0.9	4.2	4.2

P+ in NWELL	W1	W2	W3	W4	W5	W6
R-sheet [kΩ/sq]	89.4	112.1	91.6	159	83.2	76.3
Contact-resistivity [mΩ·cm^2]	44.3	8280	162	58.5	89.2	86.8

2.2.2 PASS0 Circuit Characterization and HSpice Model Parameter Extraction

The PASS0 included basic analog (two-stage op amp) and digital (standard logic gates and ring oscillators) circuit blocks designed with the minimum sized devices. Due to the unexpected poor

performance of the minimum-sized PFETs, the analog circuits failed to operate. Some digital logic gate circuits performed poorly for the same reason. Others failed due to the circuits' PFETs not being isolated. All the PFETs were fabricated within the same NWELL resulting in the wrong body-node connection for logic circuits with two cascaded PFETs.

The curve fitting and parameter extraction on the PASS0 device were performed on the IC-CAP tool. The tool utilizes BSIMv4 models to generate model parameters values from the measured transistor characteristics. The literature [25] details the steps to perform the parameter extraction tasks. Fig. 11 shows the IC-CAP plot for the 20 µm × 1.5 µm NFET's measured output I-V curves with I-V curves from the model. In the case of the PFETs, the curve fitting method did not include the non-ohmic diode effect observed at lower V_{DS}. It is to be noted that the PASS1 fabrication run incorporated a number of changes concerning the fabrication of the PFETs, which would diminish the accuracy of the fit model. Regardless, the model with the extracted parameter would serve as a preliminary foundation to design the basic functional analog CMOS circuit blocks for PASS1 to develop an extreme environment signal conditioning system. The parameters were extracted for the following transistor (PFET and NFET) sizing –

1. For NFET: Length = 1 µm, 1.5 µm, 2 µm, 4 µm, 10 µm, 20 µm
2. For NFET: Width = 3 µm, 5 µm, 10 µm, 20 µm, 100 µm
3. For PFET: Length = 1 µm, 1.5 µm, 2 µm, 4 µm, 10 µm, 20 µm
4. For PFET: Width = 7 µm, 10 µm, 20 µm, 100 µm

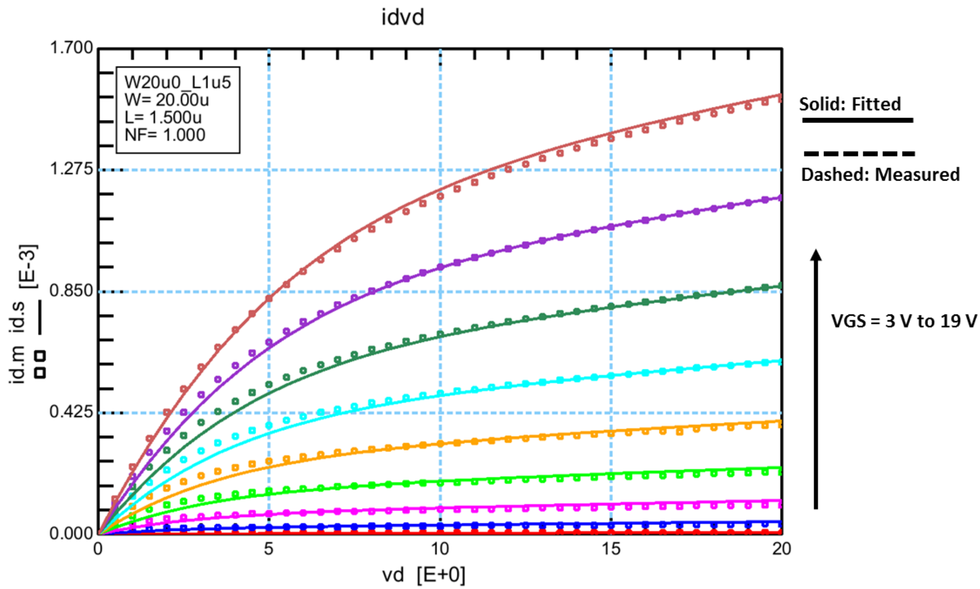


Fig. 11. IC-CAP plot showing the fitted I-V and the measured I-V curve for the 20 µm by 1.5 µm NFET device

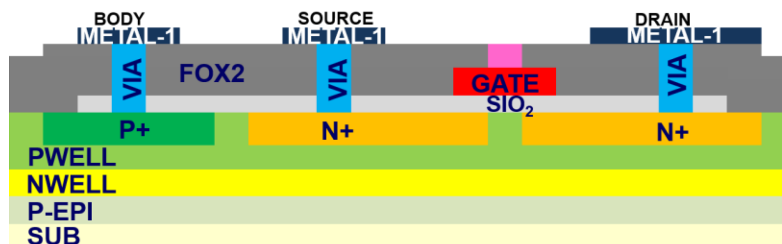
A model netlist file in HSPICE was created to combine all the extracted parameters from the different transistor sizing. The HSPICE file allowed simulation of the designed circuits for the PASS1 fabrication with the HSPICE simulator in the Cadence™ ADE tool. As mentioned earlier, the PASS1 run would incorporate significant changes in the fabrication steps. The objective of simulating the circuits with PASS0 parameters was to observe the circuits' functionality with the sizing selection of the transistors. It also has to be mentioned that the PASS1 circuits were not subjected to any post-layout simulations with parasitic extracted models due to their unavailability.

2.2.3 Changes in PASS1 Fabrication

The PASS1 fabrication run produced another six 100 mm 4H-SiC wafers, similar to PASS0. For PASS1 fabrication, the intention was to lower the PFET devices' threshold and, on the flip-side, increase the threshold of the NFET devices to improve the PFET-to-NFET drain-current ratio. This was attempted in two steps – (i) reducing the NWELL doping from 5E15 /cm^2 to 3E15 /cm^2 [26], and (ii) changing the n-type polysilicon to p-type to increase the NFET threshold voltage by +1 V

and lower the PFET threshold by +1 V. However, the p-type polysilicon has three times higher the sheet resistance of n-type polysilicon. The high sheet resistance would impact circuit performance as the polysilicon acts as the second routing layer. To lower the sheet resistance of p-type poly silicidation on the polysilicon, a titanium-silicide (TiSi) layer was suggested [27]. The down side to this approach is that it would introduce new processing steps that were not performed in the PASS0 run. The suggested TiSi layer was therefore decided to be applied on three wafers only. The fabrication sequence was also changed for PASS1 with NWELL implantation performed before P+ implantation to improve the P+ contact resistivity by reducing the chances of over-etching of the P+ region. The Ni-Al silicidation concentration was kept the same as PASS0 for both the N+ and P+ contact regions. The NFET and PFET devices for PASS1 also included an NWELL isolation layer to provide electrical isolation for the transistors and reduce body effect issues. The cross-sectional diagrams for the SiC NFET and PFET for PASS1 in Fig. 12 show the NWELL isolation layer.

The circuits block in the PASS1 were designed using specific transistor sizing (20/1.5, 20/2, and 20/4), with multiple “fingers” being used to increase the effective width of an FET device as necessary. The drain-current ratio between PFETs and NFETs was expected to be 1:5 with the process changes made for PASS1. However, the devices with smaller channel lengths were expected to exhibit variations due to short channel effects.



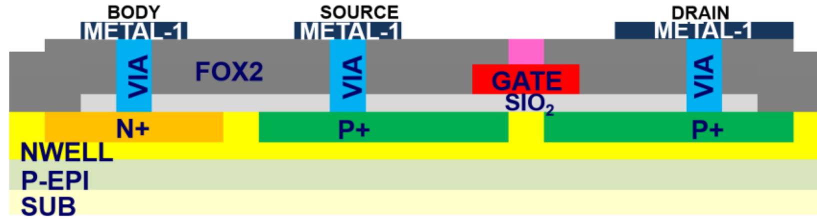


Fig. 12. Cross-section of NFET (top) and PFET (bottom) for PASS1

As the PASS1 run includes various changes over the PASS0 run, processing of the PASS1 wafers were performed in different wafer splits. Table VI shows the split plan for the PASS1 wafers. Wafer#1 and #2 had the same PASS0 doping profiles for the transistors. Wafer#1 and wafer#3 used platinum metallization that is intended to perform circuit functionality testing at 500°C temperatures. As mentioned earlier, the polysilicidation is performed only on the three wafers #1, #3, and #5.

Table VI. PASS1 Wafer Splits

PASS1 wafer #	**1**	**2**	**3**	**4**	**5**	**6**
Modified NWELL doping			X	X	X	X
PASS0 doping	X	X				
P-type poly	X	X	X	X		
N-type poly					X	X
Poly silicidation	X		X		X	
Metal-1 (Al, Pt)	Pt	Al	Pt	Al	Al	Al
Passivation	X	X	X	X		

2.2.4 Transistor Characterization from Fraunhofer PASS1 Run

Post fabrication, the NFET and PFET devices from wafer #3, wafer #4, and wafer #6 were characterized over temperatures on the probe station. Fig. 13 shows the variation in the threshold for NFET and PFET devices from each of these wafers, with the 20 µm / 2 µm dimensions, over the temperature range of 25°C to 500°C.

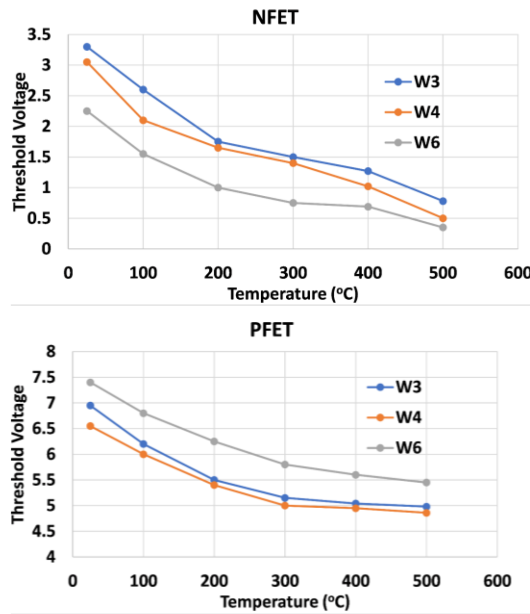


Fig. 13. Threshold voltage (V_{TH}) variation over temperature for NFET (top) and PFET (bottom) from PASS1 wafers #3, #4, and #6.

As expected, for each wafer, the threshold voltage for NFET and PFET devices drops due to increased carrier concentration at higher temperatures. The key phenomenon to notice from Fig. 13 is the increase in the NFET threshold voltage and decrease in the PFET threshold voltage for wafer #3 and wafer #4 compared to wafer #6. The deposition of the p-type polysilicon, therefore, provided the expected results. The PFET and NFET threshold voltages on wafer #6 are comparable to the PASS0 results as the transistors on wafer #6 still uses n-type polysilicon. Therefore, lowering the NWELL doping did not drop the PFET device's threshold, which is unusual.

The output I-V characteristics over temperature, for the 20 µm × 2 µm PFET, from wafer #3 and wafer #4 are shown in Fig. 14-Fig. *17*. For the NFET, the output characteristics plots are shown in Fig. 18-Fig. 21. The PFET-to-NFET drain current ratio for both wafers has improved to approximately 1:8 in comparison to the PASS0 value of 1:17 for the same sized transistors. However, the drain-current ratio's progress is not satisfactory compared to previous devices from the Raytheon SiC CMOS process (Appendix-1). The transistors on both the wafers show an

increase in the drain current as temperature increases. This is due to the increase in intrinsic carrier concentration and the higher rate of threshold drop. It can be shown using the I-V plots and square-law equations that the effective mobility for the PFET and NFET increases at higher temperatures. For PFET, the mobility (μ_p) increased by 2.5 times as temperature increased from 25°C to 500°C. In the case of the NFET, the mobility (μ_n) increased by 1.7 times as temperature increased from 25°C to 500°C. However, it does not reflect on the real electron or hole channel mobility behavior. The I-V plots also show non-ohmic behavior at lower V_{DS} on the PASS1 PFET devices. The P+ contacts are still non-ohmic. The root cause could be the small, 3µm × 3µm, VIA opening area for the P+ contact region, or the Ni-Al material for the silicidation process. A possible replacement to Ni-Al could be titanium-aluminum (Ti-Al) [28]. At the time of writing this dissertation, the Fraunhofer IISB had already started investigating Ti-Al-based silicidation to form better P+ contacts on SiC wafers. The P+ contact resistivity for PASS1 wafers #3, #4, and #6 were measured from the transfer-length measurement or TLM structures and are shown in Table VII.

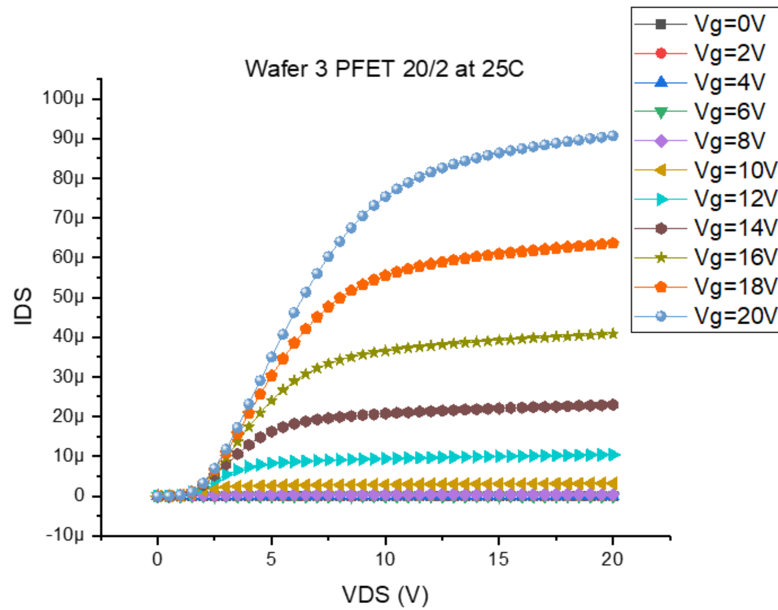


Fig. 14. PASS1 wafer #3 I-V plots for 20 µm × 2 µm PFET at 25°C.

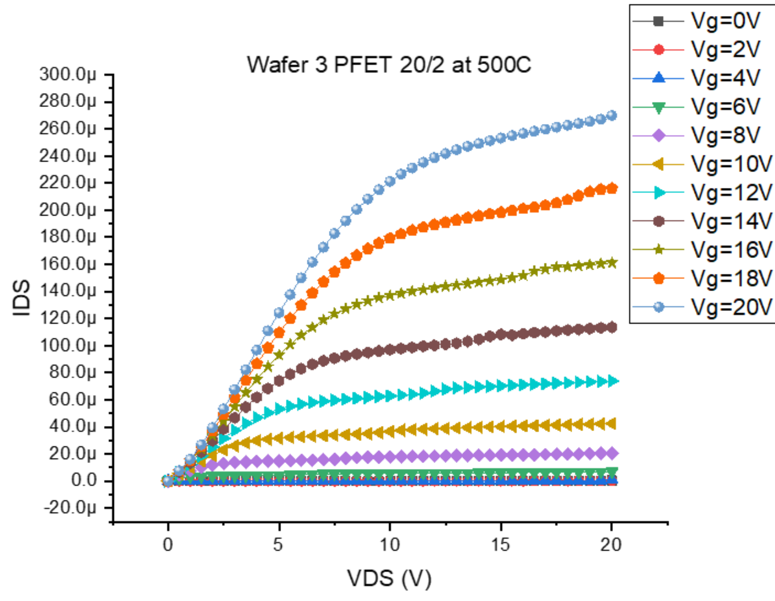


Fig. 15. PASS1 wafer #3 I-V plots for 20 μm × 2 μm PFET at 500°C.

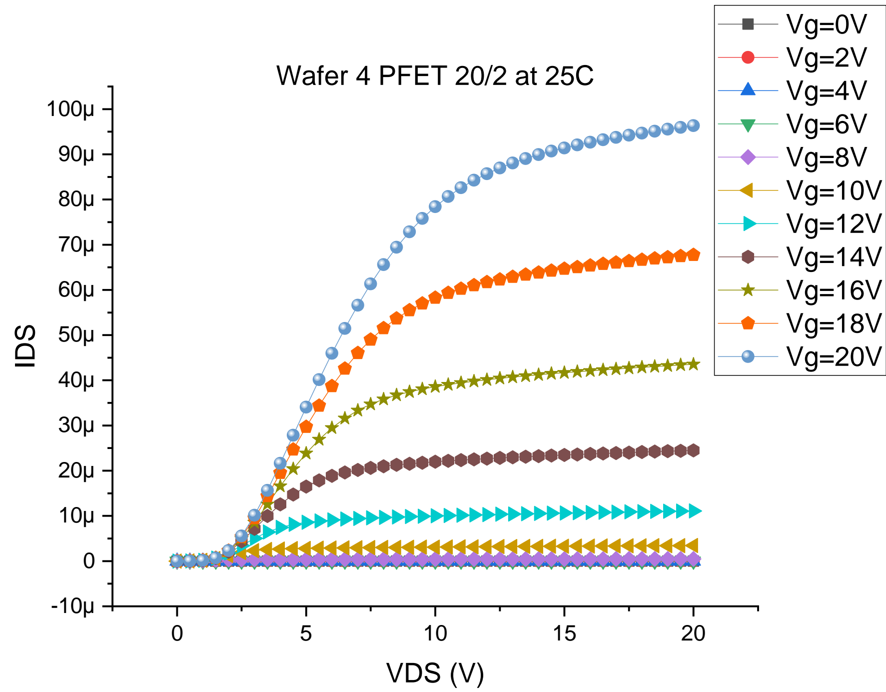


Fig. 16. PASS1 wafer #4 I-V plots for 20 μm × 2 μm PFET at 25°C.

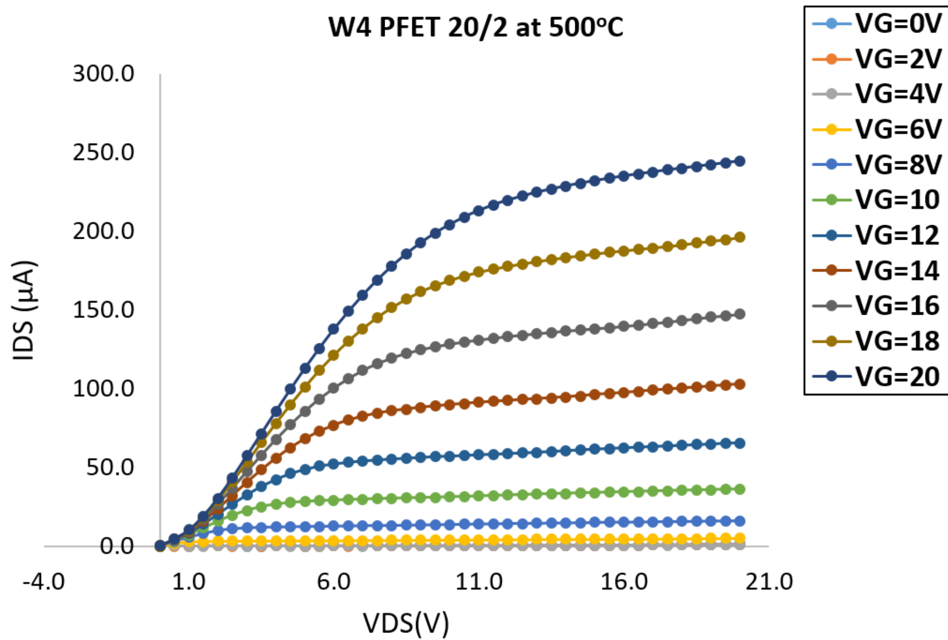


Fig. 17. PASS1 wafer #4 I-V plots for 20 µm × 2 µm PFET at 500˚C.

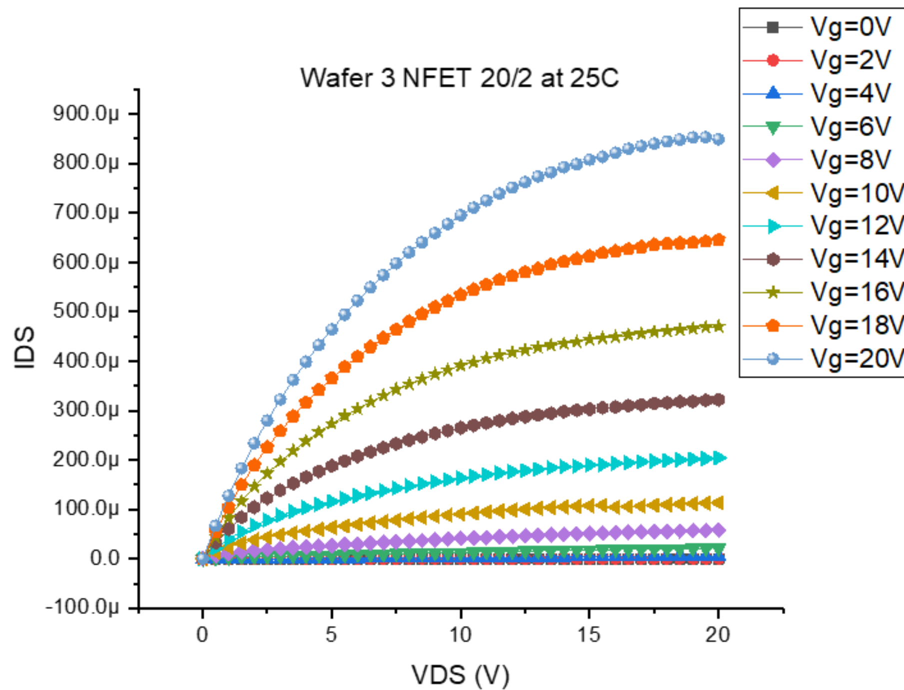


Fig. 18. PASS1 wafer #3, I-V plots for NFETs at 25˚C.

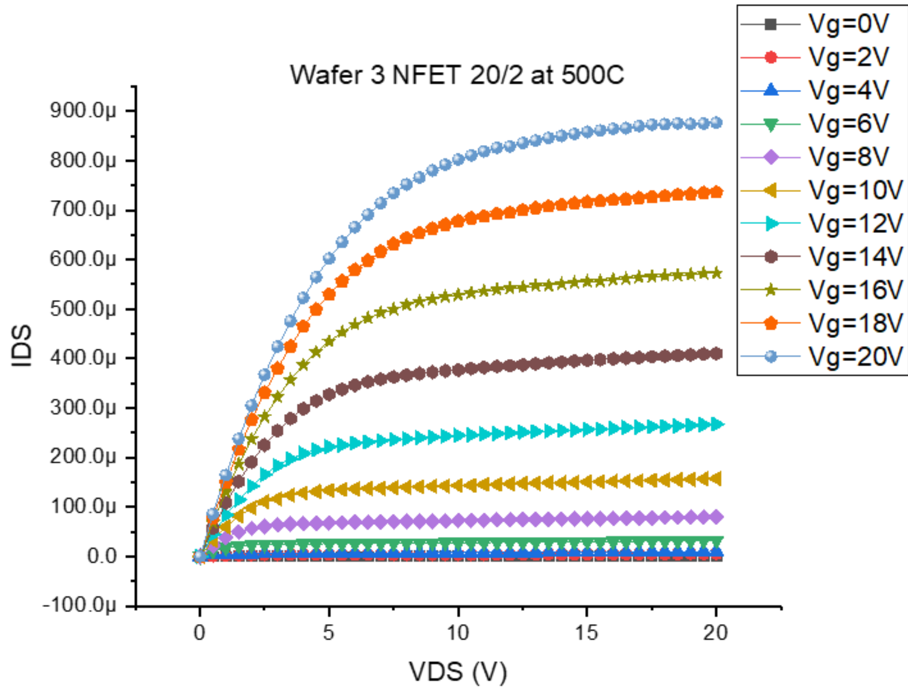


Fig. 19. PASS1 wafer #3, I-V plots for NFETs at 500˚C.

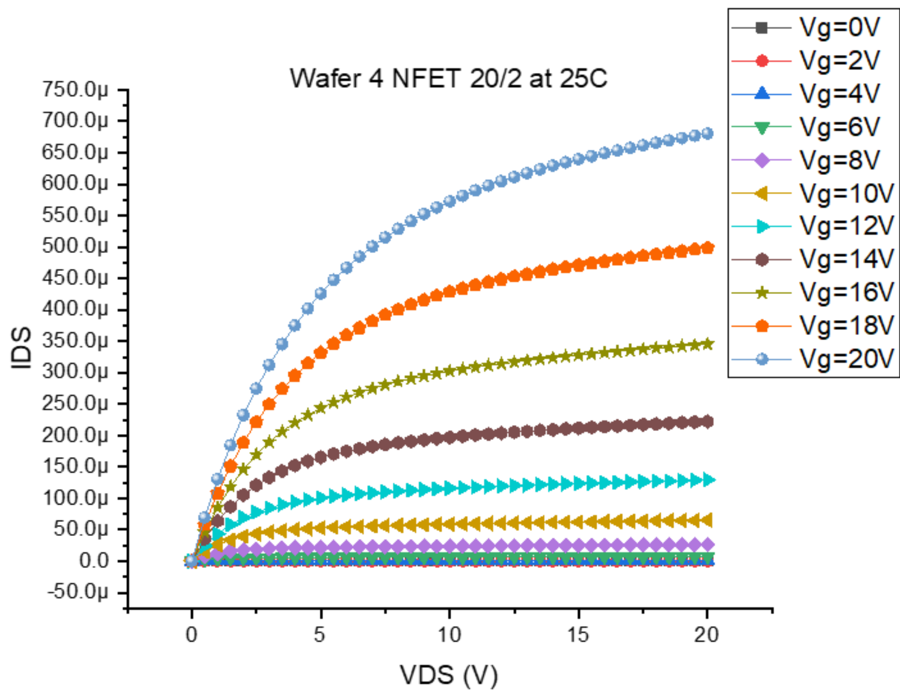


Fig. 20. PASS1 wafer #4, I-V plots for NFETs at 25˚C.

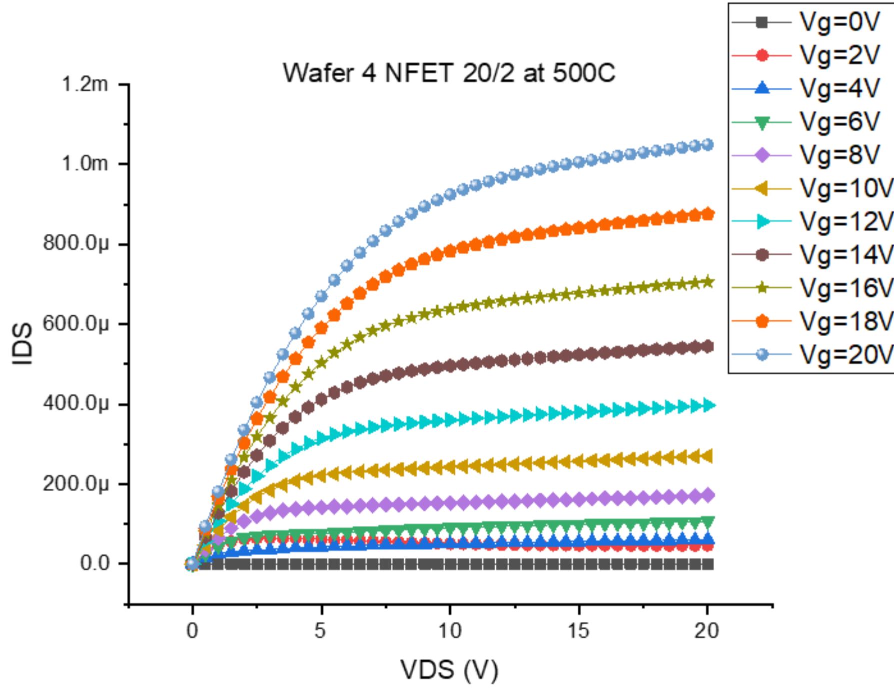


Fig. 21. PASS1 wafer #4, I-V plots for NFETs at 500°C.

Table VII. Contact Resistivity of P+ Region from PASS1 Wafers

Wafer #	Contact Resistivity (mΩ·cm²)
3	8206.93
4	8825.62
6	47813.74

The concerning observation from Table VII is the noticeably high contact resistivity for the P+ region for the PASS1 run. It is essential to mention that the fabricated circuits on the PASS1 run were designed to operate at a quiescent current under 1 mA. Therefore, any voltage drop across the highly resistive P+ contacts will be negligible.

The output characteristics for wafer #2 PFET and NFET devices, with 20/2 µm sizing, at 25°C and 500°C were also measured. The maximum drain current for the NFET device showed no significant change compared to wafer #3 or #4. However, the maximum drain current for the PFET device (for example, at V_{GS} = 20 V, I_{Drain} = 75 µA) was less compared to the wafer #3 and #4 PFETs

(measured I_{Drain} = 95 µA @ V_{GS} = 20 V). The reason for this variation is the lowering of the NWELL doping on wafer #3 and #4, which in the case of wafer #2 is not included.

Alongside the threshold variation and DC output characteristics, the transistor transconductance (G_m) was also measured for the PASS1 PFET and NFET structures. Fig. 22 and Fig. 23 show the PFET and NFET transconductance vs. V_{GS} (swept across 0 to 20 V) plots over temperature for 20/2 µm device dimensions (from wafer #4), respectively. The fixed V_{DS} across the PFET and NFET device during the transconductance measurement plot was kept at 1.2 V and 0.5 V, respectively. The applied V_{DS} is higher to avoid the initial non-ohmic region of the PFET, as seen in Fig. 10 and Fig. 14-Fig. *16*. The 300°C and above plots show distortion for both the devices due to the mechanical noise induced from the movement of the test die on top of the thermal chuck. Although the probe station chuck is equipped with vacuum support, at high-temperatures above 300°C, maintaining the probe-tips placed on the test die pads becomes difficult.

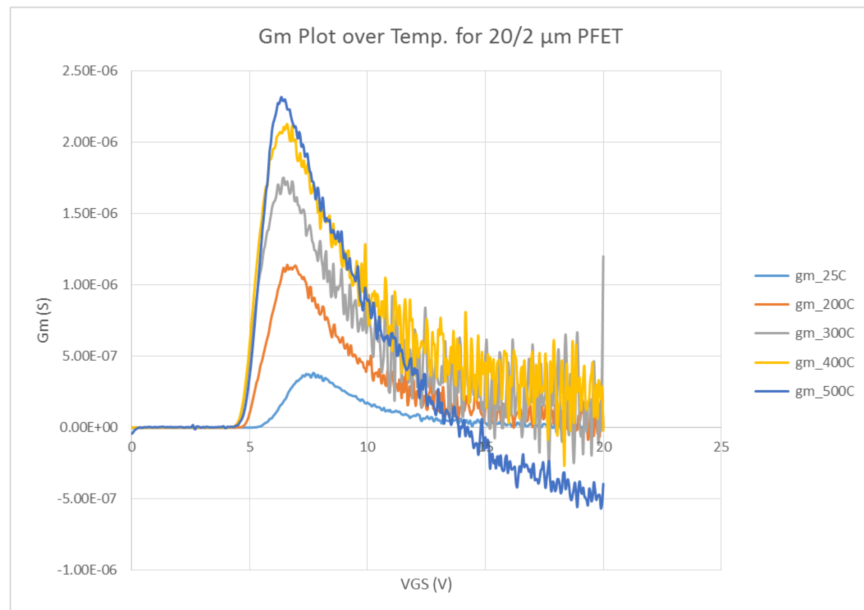


Fig. 22. PASS1 20 µm × 2 µm PFET transconductance over temperature.

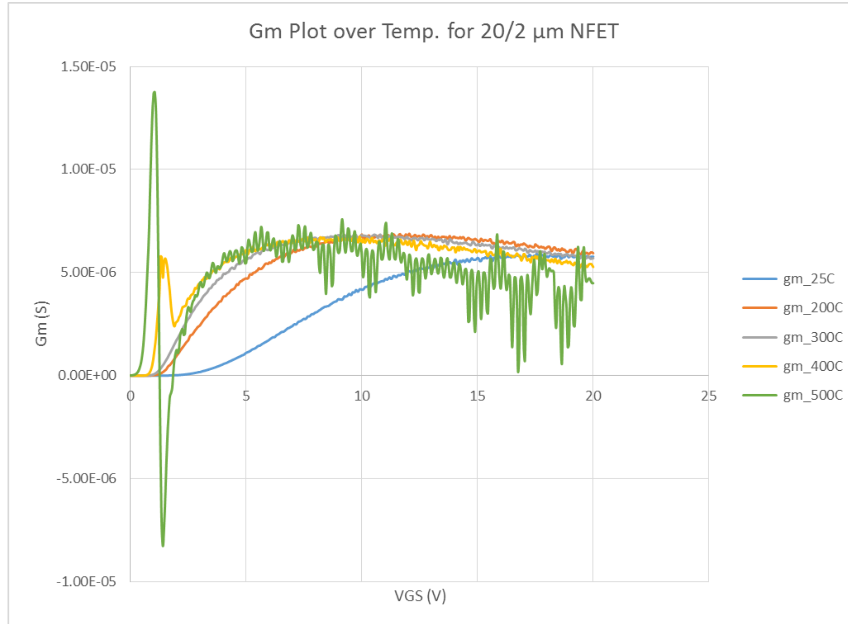


Fig. 23. PASS1 20 µm × 2 µm NFET transconductance over temperature.

The transconductance value is a crucial parameter for designing analog circuits. It provides the transistor's intrinsic gain and allows the designer to set the biasing current or biasing voltage necessary to enable the transistor to operate in amplification mode. The transconductance plots for both the transistors increase with temperature. The behavior correlates with the output characteristics. The G_m plot for the NFET significantly increases as temperature rises from 25°C to 200°C. As the temperature continues above 200°C (at $V_{GS} < 11$ V), the transconductance increases at a lower rate. The initial sharp increase in the G_m can be correlated to the threshold variation plot in Fig. 13, where the threshold for the NFET abruptly drops between the temperature range of 25°C to 200°C. Post the 200°C temperature, the change in the threshold voltage is linear with the change in temperature. In the PFET device, the increase in transconductance with the rise in temperature is almost linear. At higher $V_{GS,}$ the transistors' transconductance value starts to drop, which is expected as the devices enter the linear or triode region of operation [29], [30]. This drop occurs sharply for the PFET device when the applied V_{GS} crosses 7 V. This limits the applied bias

voltage range for the PFET devices. For analog circuit applications, it will be optimal to use the gate-source bias voltage to the PFET devices within the range of 6.5 V to 9 V. For the NFET device, this applied V_{GS} range has to be within 2.5 V to 7.5 V.

Finally, the NWELL to PWELL/P-epi breakdown voltage for the PASS1 transistor devices was measured at 35 V for a leakage current of 1 μA. The breakdown voltage parameter is essential to know as it sets the maximum voltage level under which the SiC CMOS devices within a circuit can safely operate.

Chapter 3. Design of Silicon Carbide Circuits in the Fraunhofer CMOS Process

This chapter will showcase the high temperature analog circuits designed in the Fraunhofer SiC CMOS process from the PASS1 run. The circuit on the PASS1 run were designed with higher PFET-to-NFET drive ratio due to the poor input-output characteristic behavior of the PFETs from the PASS0 run along with the low threshold of the NFETs. The transistor characterization results from the PASS0 run were discussed in the previous chapter,which provided the platform to design the circuit with necessary transistor sizings to attain functionality. Additionally circuit failure issues like the missing NFET isolation layer has been addressed in all the designed circuits, discussed in this chapter. The chapter will describe about the circuit topologies selected for op amps and voltage reference circuit desige satisfy. The latter part of this chapter will show the measurement results from the circuits' functionality and high temperature testing.

3.1. Operational Amplifiers: Design Approach and Simulation

Operation amplifiers (op amps) are the fundamental building blocks in the analog IC domain. A typical 3-stage op amp is composed of a differential amplifier, followed by a secondary gain stage and, finally, a buffer or drive stage. The requirement of the buffer stage depends on the op amp output load specification (resistive or capacitive). Fig. 24. Schematic of the two-stage op amp with PFET differential input pair designed on the Fraunhofer SiC CMOS PASS1 run and Fig. 25. Schematic of the two-stage op amp with NFET differential input pair designed on the Fraunhofer SiC CMOS PASS1 runshow the two schematics of the two-stage, unbuffered CMOS op amps (with transistor sizing) designed in the Fraunhofer SiC CMOS process. The op amp in Fig. 24 has the differential stage formed with PFET device pairs, whereas the one in Fig. 25 has the NFETs for the differential pair. The second stage for both the op amps is a common-source stage. The two op amps do not use a buffer stage as both the op amps are expected to drive a capacitive load of

less than 13 pF. The 13 pF is usually the capacitance value associated with oscilloscope probes. These op amps are designed for low-frequency operation. Hence, the open-loop gain is the critical parameter of interest. Additional pad-outs were inserted into the op amp circuit layouts for placing external capacitors for compensation and to guarantee stability.

The PFET differential pair two-stage op amp [31] is designed using multi-finger transistors, with fixed sizing of 20/2 µm. The transistors Q1-Q2 form the differential pair, Q4-Q5 act as the active load, and Q3-Q9 are the current source transistor. The active load transistors are sized at 0.25 times the width of the differential pair transistors. The sizing factor is higher than the measured PFET-to-NFET sizing ratio of 0.125 in Chapter 2. The transistor sizing on the circuits is selected with the expectation that the necessary modifications made in the PASS1 run would substantiate noticeable improvement on the PFETs and provide the drain-current ratio of 1:4 or 1:5 between the P-to-N devices.

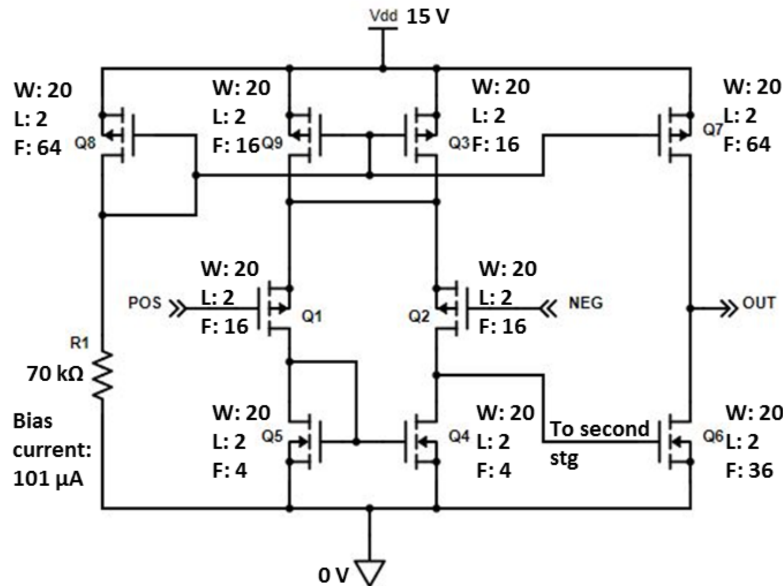


Fig. 24. Schematic of the two-stage op amp with PFET differential input pair designed on the Fraunhofer SiC CMOS PASS1 run

The common-source transistor, Q6, on the second stage has Q7 as the active load. The sizing of these transistors dictates whether the op amp would exhibit systematic offset. To minimize the possibility of the systematic offset, the V_{GS} across Q6, during differential voltage of 0 V, has to be at a specific value that allows the current-sourcing through the Q7 to match the current-sinking through the Q6. The Q7 transistor is sized twice the Q6 to satisfy that criterion. Regardless, the op amp is expected to show some offset due to the device mismatches. As mentioned earlier, for compensation, additional pad-outs are inserted in the op amp design. The PFET input pair two-stage op amp utilizes Miller compensation through a compensation capacitor that is to be connected externally. In addition to the compensation capacitor, a zero-nulling resistor is also required to avoid any right-hand zero in the frequency response of the circuit. The bias resistor of 70 kΩ is also to be provided externally.

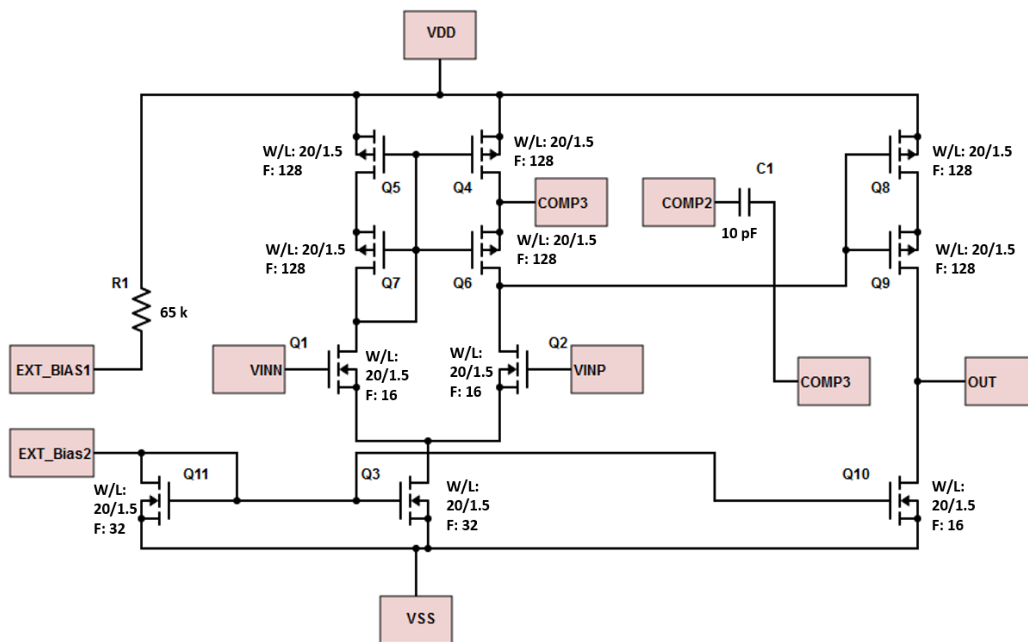


Fig. 25. Schematic of the two-stage op amp with NFET differential input pair designed on the Fraunhofer SiC CMOS PASS1 run

The NFET differential pair two-stage op amp [29] is similarly designed using multi-fingered transistors with fixed sizing of 20/1.5 μm for the NFET transistors, Q1 and Q2 as the differential pair with the second stage utilizing the PFET, Q8-Q9, in the cascode common-source configuration. The transistor, Q3, acts as the constant current source, sinking the necessary bias current for the first stage. The transistors Q4-Q7 cascode current mirror form the active load. The transistors are designed and sized in a split-length method, which allows implementing long channel FETs using equal length devices. The technique is used in this op amp to apply the indirect feedback compensation technique. This method has previously not been attempted for SiC CMOS circuits. The indirect compensation requires a compensation capacitor but avoids the requirement for any zero-nulling resistor as, during high-frequency operation, a feedback current from the output node can pass through the compensation capacitor to the drain node of the input differential pair transistor, Q2, via the transistor, Q6, indirectly, as the direct connection between the drain node of the Q2 and the op amp output no longer exits. Due to the split length method, the effective W/L for Q4 and Q6 is 20/3. With the sizing of Q2 set to 20/1.5 μm, the effective width of the PFET active load is therefore sized four times the width of the input differential NFET devices. The bias resistor of 65 kΩ is to be set externally. The second stage common-source PFETs are also sized to provide four times the width of the current source transistor, Q10.

The advantage of the op amp with PFET differential pair is the low common-mode operation compare to the NFET differential pair. In the PFET op amp case, the minimum input common-mode is equal to 0 V (considering single rail supply). For the NFET op amp, the minimum common-mode is similar to $V_{DSAT\text{-}Q3} + V_{THN}$. In signal conditioning systems for thermocouple sensors, using the PFET op amp is suitable as the sensor terminal can therefore directly be fed to

the op amp input without requiring additional bias circuits to set the high common-mode (as in the case of the NFET op amp).

As indicated earlier, the open-loop gain for the abovementioned op amps is the key parameter of interest. The low-frequency op amp gain can be calculated by taking the product of the gain of the first stage and the second stage, as given in the equation below,

$$A_{OL} = g_{m-Q2} * (r_{O-Q2}||r_{O-Q3/Q4})* g_{m-Q6/Q9} * r_{O-Q7/Q10}$$

Here the r_O is the transistor output resistance, which is equal to $1/_{\sigma I_{DS}}$. Based on the output characteristics shown in Chapter 2, it is expected that the output resistance for both the PFET and NFET transistors would drop as operating temperature rises. However, with the increase in the transconductance at higher temperatures for the PFETs, the overall open-loop gain for the op amp with PFET differential pair is thereby should improve at elevated temperature. The PFET device transconductance increases by nine times, whereas output resistance drops three times for the same temperature shift of 25°C to 500°C. In the case of the NFET differential pair op amp, the transconductance does not significantly improve after 300°C. At higher operating temperatures, the overall gain should therefore remain the same. However, there will be an initial increase in the op amp DC gain when the temperature increases above 25°C.

The schematic in Fig. *26* shows another standard two-stage op amp with the PFET input differential pair based folded-cascode first stage [30]. The second stage is composed of a class-AB output buffer to provide a rail-to-rail output swing. The sizing of transistors for each stage is shown on the schematic. The cascode stage biasing transistors (Q22 – Q25 and Q18 – Q21) provide the higher output resistance allowing the folded cascode amplifiers to have higher gain than the standard differential amplifiers with active loads. However, the trade-off to that is the requirement

of a larger supply headroom. The cascode stage has transistors Q36 and Q37 acting as floating current sources. The drain and source nodes of the Q36 provide the input to the gates of the class-AB output stage transistors Q26 and Q27. The drawback to the class-AB buffer is the shift in the DC level (closer to the VDD rail) of the op amp due to the overall drop in voltages on the drain and source nodes of the Q36 transistor. The transistors Q16 and Q17 form the cascoded current source to provide the bias current (1 mA) to the PFET input pair transistors Q14 and Q15. The open-loop gain equation for the folded cascode op amp can be found in the literature [30].

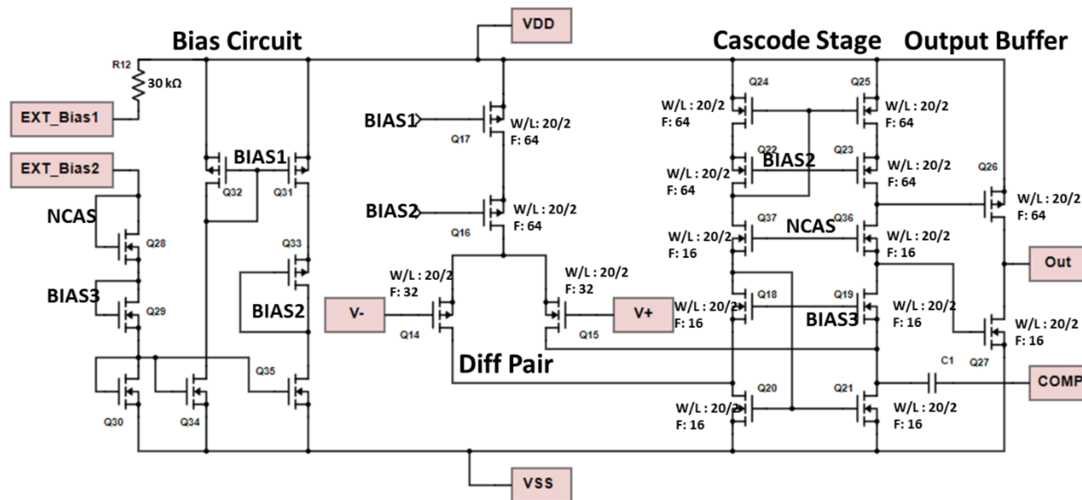


Fig. 26. Schematic of the two-stage folded-cascode op amp with PFET differential input pair and class AB buffer output, designed on the Fraunhofer SiC CMOS PASS1 run

Like the previous op amps, the bias resistor R12 and compensation capacitor C1 are connected externally.

All of the op amps mentioned above were simulated using the extracted model from the PASS0 characterization results. As explained earlier, the simulation results do not reflect the correct behavior of the designed circuits because of the process changes being made. Instead, it exemplifies the worst-case scenario on whether the transistors' associated sizing can deliver functionality with the PASS0 transistor models. The op amps' low-frequency gain is the critical

parameter of interest due to the suitability in the sensing application (for example, the Siemen's Chromel-Chromel thermocouple sensor for turbine blades). AC analysis on the Cadence ADE environment was performed on the op amps. The DC gain from the simulation results for the three op amps is shown in Table VIII. The DC gain should be higher in actual circuit measurement due to the anticipated improvements on the PFET devices from the PASS1 fabrication run.

Table VIII. Simulated DC for the Fraunhofer SiC CMOS PASS1 Designed Circuits Using PASS0 Models

Op amp Topology	Gain (dB)
Two-stage PFET Input Pair	27
Two-stage NFET Input Pair with Indirect Compensation	32
Folded Cascode Two-stage with PFET Input Pair	35

3.2. Voltage Reference Circuit: Design Approach and Simulation

Designing a voltage reference circuit independent of input supply and temperature is important as it is a crucial circuit component for voltage regulator design, which provides regulated supply to the onboard or on-chip circuits. There are two key blocks for designing a temperature-independent reference circuit – the proportional to absolute temperature (PTAT) block and the complementary to absolute temperature (CTAT) block [29]. The PTAT provides a reference voltage/current that increases proportionally to the temperature, and the CTAT does the opposite. Combining the two blocks can result in an output voltage with a minimal temperature coefficient (TC) and, therefore, would exhibit minimalistic variation across temperature. The schematic of the designed voltage reference circuit in the Fraunhofer SiC CMOS process is shown in Fig. 27.

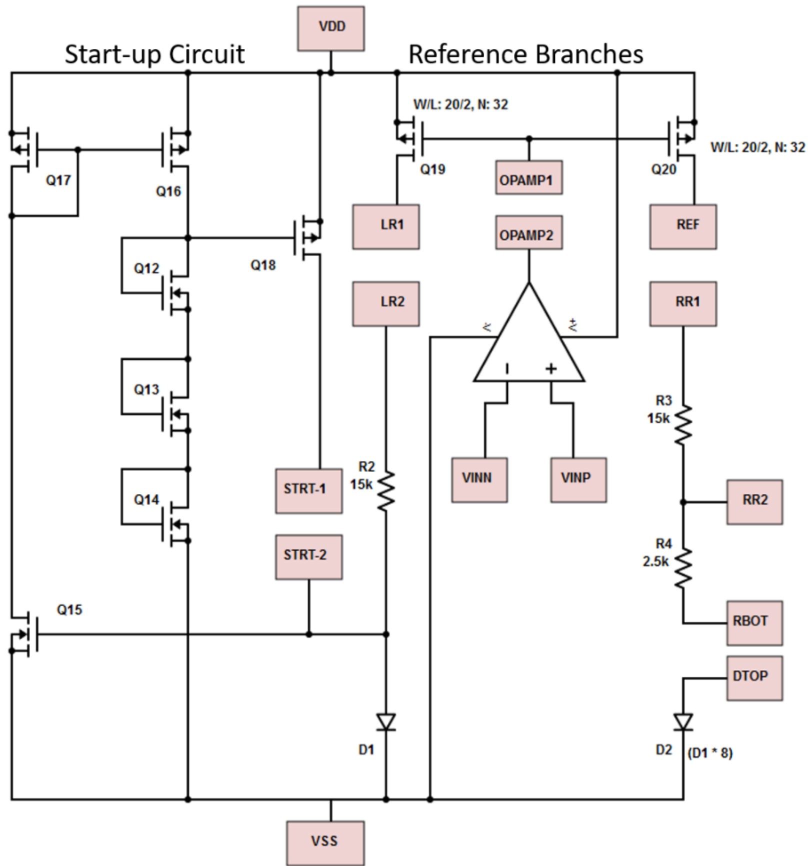


Fig. 27. Schematic of the voltage reference circuit designed in the Fraunhofer SiC CMOS PASS1 run.

The reference voltage branch in the circuit is composed of the PFETs, Q19-Q20, providing the PTAT current on the unit with resistors R4 and the diode, D2. The diode, D2, provides the CTAT voltage. The PFETs are identical in size with dimensions of 20/2 µm and 32 fingers. The diode, D2, has the combination of 8 diodes (50 by 50 µm dimensions) in parallel; hence the voltage drop across D2 would be smaller than the diode, D1. The diodes are PWELL-to-N+ in nature, and the resistors are N+ implants. The difference between the diode voltages will be dropped across the resistor R4. The branch voltages at nodes RR2 and STRT-2 will be connected to the input of the op amp. The resistors R2 and R3 in each branch should be equal to ensure the V_{DS} across Q19 and Q20 are the same. The output node of the op amp connects to the gates of the PFETs, Q19-Q20. These two nodes are intentionally separated to check the op amp circuit functionality before the

complete reference circuit testing. In actual testing, the two nodes will be connected via wirebonds. The op amp regulates the branch current when the supply voltage starts to change. The op amp in the reference circuit uses the two-stage NFET differential pair topology, shown in Fig. 25. Schematic of the two-stage op amp with NFET differential input pair designed on the Fraunhofer SiC CMOS PASS1 run. Hence, the op amp's inverting and non-inverting nodes would have to be equal or greater than 4 V for the NFETs on the differential stage of the op amp to be at saturation and therefore operate to regulate the gates of the PFETs. The combined parallel PWELL-to-N+ diodes, referred to as 'D2', would have the forward drop dependent on the amount of current passing through the reference output branch. The PWELL-to-N+ diode test structure with a larger area (262 μm × 9 μm with 21 fingers) was tested under probe-station and showed a forward drop of 5.6 V at 300 μA of forwarding current. This forward voltage drop would further increase with lower current density, which is true in the case of the diodes used in the reference circuit. This increased forward drop would shift the voltage on the non-inverting node, 'RR2', on the op amp and eventually elevate the reference output voltage. Assuming 300 μA of current flowing across R3and R4, would create a voltage drop of (17.5kΩ*0.3mA) 5.25 V, resulting in the reference output voltage of 5.25 + 5.60 = 10.85 V. In reality, this output reference voltage will be higher than 10.58 V. To minimize the issue, large area diodes can be used (to increase current density) on the reference circuit; however, the trade-off will be the large design area. The cause of the high forward drop is the poor non-ohmic P+ contacts on the PWELL.

The start-up section on the reference circuit must avoid any scenario where the gates of the PFETs, Q19-Q20, remain at high potential causing zero current to pass through the reference branches and stopping the circuit from operating. The start-up circuit provides the initial current to the diode, D1 (by connecting the STRT-1 and STRT-2 nodes), as the supply voltage (VDD) starts to ramp

up. When the diode displays a voltage drop, the op amp output pulls down, causing the PFETs, Q19-Q20, to turn ON. The reference branch resistors are all on-chip and are implemented with N+ implant resistors with a negative temperature coefficient (TC) and sheet resistance of approximately 900 Ω/sq. The resistors initially exhibit negative TC for the temperature range of 25°C to 300°C. Once the temperature crosses 300°C and above, the TC turns positive as resistance increases. This non-uniform behavior is due to the release of thermally excited excess carriers from incomplete ionization during implantation of the N+ resistors. As the temperature keeps increasing, these excess carriers cause degradation in mobility due to thermal scattering, subsequently increasing the sheet resistance.

The voltage reference circuit was not simulated due to the absence of fitted models for the diodes.

3.3. Fraunhofer SiC CMOS Circuits: Die Micrographs of the Circuits

As mentioned in Chapter 2.2, the Fraunhofer PASS1 devices and circuits were fabricated on a 100 mm SiC wafer. The full wafer includes 24 copies of 20 mm by 15 mm reticles subdivided into 4.8 mm by 4.8 mm blocks. Each block is populated with different circuits. Adjacent blocks are separated by 200 µm to allow sub-dicing of the blocks. The circuits on the sub-diced blocks were tested on the same probe station where the PFET and NFET devices were characterized Fig. *29* shows the die micrographs of the op amps and the reference circuit. The two-stage NFET differential pair op amp was laid out on the same section as the reference branch. Table IX shows the layout area for the circuits along with the actual pad counts. The number of pad-outs or pin-outs are higher than what is shown in the schematic. The extra pads are included in the circuits' layout to add testability and keep pad-outs for off-chip capacitors to check the feasibility of the on-chip capacitors.

A regulator circuit with an NFET pass transistor was also designed on the PASS1 run. The regulator was intended to operate over a supply voltage range of 20 V to 50 V. However, based on the measured NWELL-to-PWELL breakdown of 35 V, the fabricated regulator circuit was tested for 20 V to 25 V of supply. The details of the regulator circuit schematic, die micrograph, and test results are provided in Appendix-1. The regulator, the PFET differential pair op amp, and the reference circuits have later been used to design the Fraunhofer module. All the die pads on the circuits are 100 µm × 100 µm in dimensions. Wafer #3 and #4 were initially selected to test the circuits for functionality and high-temperature behavior. All the circuits from wafer #3 failed to operate. Performing focused-ion-beam (FIB) analysis [32] on wafer #3 showed the failure point to be the missing titanium layer above the polysilicon layer, as seen in Fig. 28.

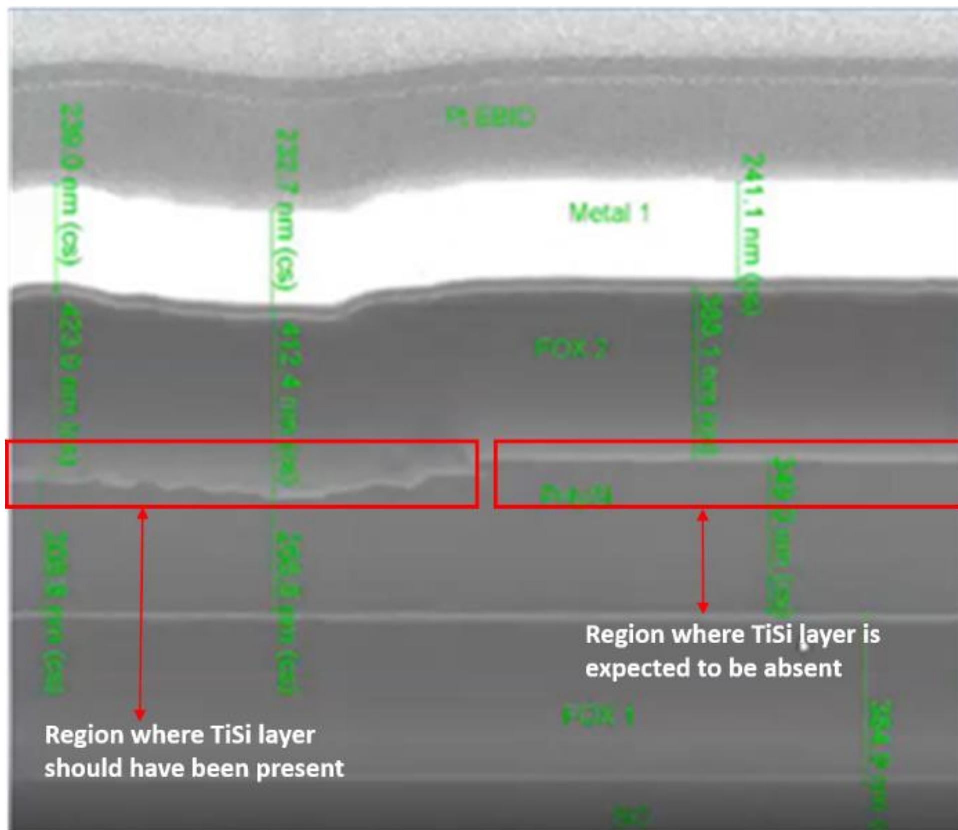
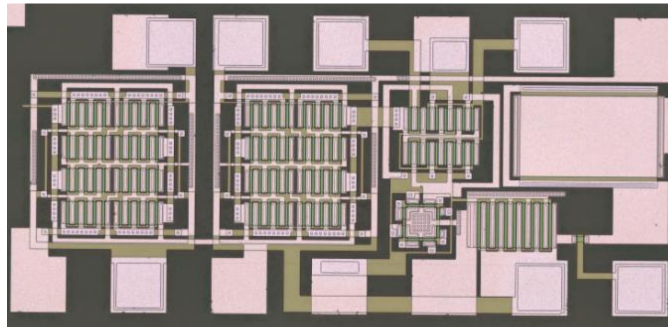
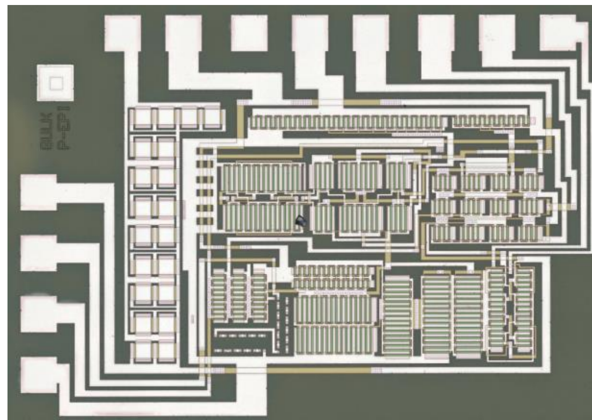


Fig. 28. FIB image on wafer#3 indicating the place where the titanium layer is absent over the polysilicon layer.

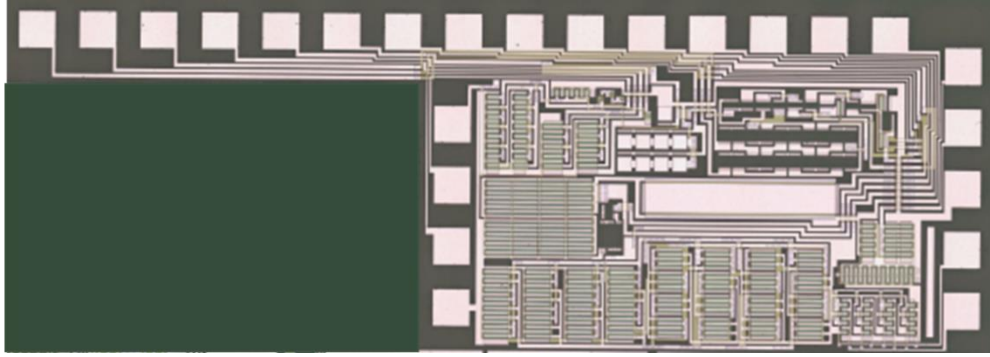
As described in Chapter 2, one of the modifications in PASS1 wafer #3 was the addition of the poly-silicidation with the titanium layer to reduce the sheet resistance of the p-type polysilicon. In wafer #4 this poly-silicidation process was not added as part of the wafer split (shown in Table VI). Without the titanium layer, the routed polysilicon layer formed open connections with the first/top metal layer, ultimately failing the circuits. Thus results from the circuit measurements in this dissertation paper are only shown for wafer #4.



(a)



(b)



(c)

Fig. 29. Die micrographs of (a) PFET two-stage op amp, (b) folded-cascode two-stage op amp, and (c) voltage reference with the NFET two-stage op amp.

Table IX. Layout Area and Pad Counts for the Fraunhofer SiC CMOS PASS Circuits

Circuit Type	Layout Area	No. of Pin-Outs
Two-stage PFET Input Pair	1180 μm × 570 μm	14
Two-stage NFET Input Pair with Indirect Compensation (without PADS)	1237 μm × 561 μm	8
Folded Cascode Two-stage with PFET Input Pair	1901 μm × 1300 μm	11
Voltage Reference	1816 μm × 1100 μm	20

3.4. Fraunhofer SiC CMOS Circuit Measurement Results

3.4.1 Two-stage PFET Differential Pair Op amp

The two-stage op amp with PFET differential input pair was tested first due to the circuit's suitability for the signal conditioning system. In an open-loop configuration, the op amp circuit was tested on the probe station at 15 V supply with 100 Hz, 20 mV amplitude sinusoidal signal provided from the function generator to the non-inverting terminal of the op amp. The DC common-mode voltage overlapping the sinusoidal was set to 50 mV. To set the bias current, the op amp used an external resistor of value 70 kΩ. For compensation, a 33 pF ceramic capacitor was used. The inverting input had to be set at 0.29 V, as the op amp showed 0.24 V of input offset. The input-referred offset for the op amp was measured by applying DC voltage at the two input

terminals and taking the input voltage difference when the op amp output DC level starts shifting close to zero. Theoretically, the op amp output should be zero when the differential voltage between the inputs is zero. The op amp output captured on the oscilloscope is shown in Fig. 30. Input-Output waveforms on the oscilloscope for the two-stage PFET differential input pair op amp at 25°C. .

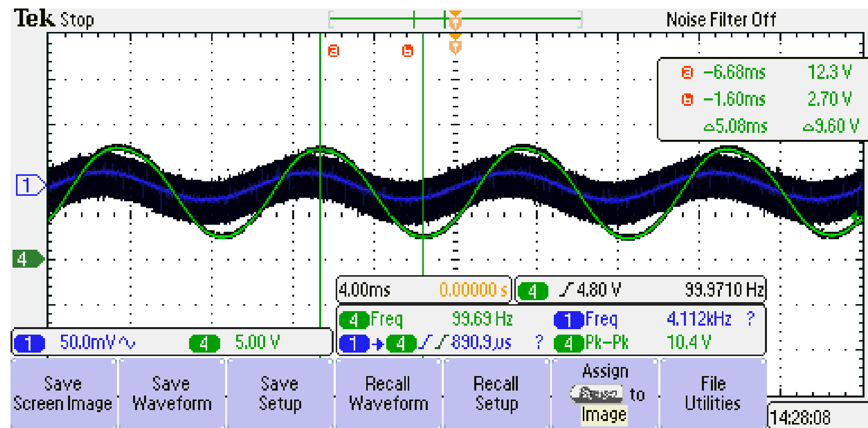


Fig. 30. Input-Output waveforms on the oscilloscope for the two-stage PFET differential input pair op amp at 25°C.

The open-loop gain can be calculated from the ratio of the input to output signal amplitude by using the equation, $\boldsymbol{AOL} = \mathbf{20log}\left({V_{OUT-amp}}/{V_{IN-amp}}\right)$. The calculated open-loop gain from the measured waveform at 25°C is 47.6 dB. The op amp circuit in the same configuration was tested at 500°C for a very brief period of time (due to the difficulty in maintaining the probe station tips intact on the op amp die pads). The output waveform at 500°C operation is shown in Fig. *31*. The open-loop DC gain was calculated using the same equation as above, and the resulting value was 48.9 dB. Thus, the op amp gain improves at higher temperatures as expected.

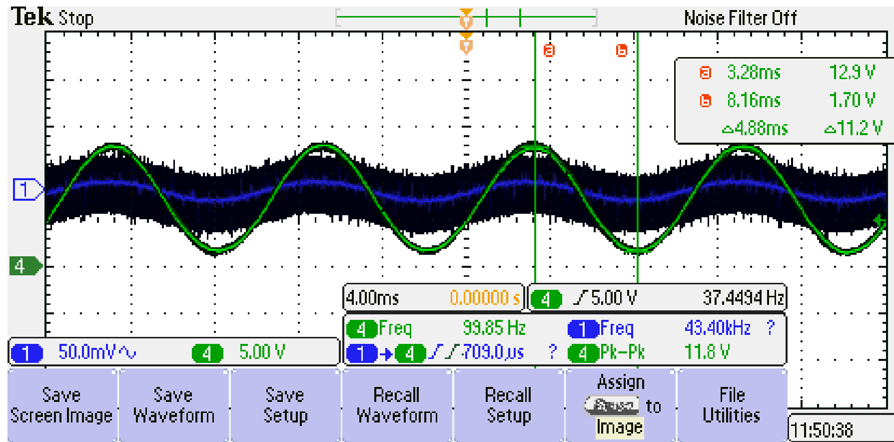


Fig. 31. Input-Output waveforms on the oscilloscope for the two-stage PFET differential input pair op amp at 500˚C.

The op amp offset voltage lowered as the temperature increases. At 500˚C, the offset voltage dropped down to 0.03 V. Once the temperature testing was complete, the op amp was re-tested at 25˚C. With the op amp re-tested at room-temperature, the input-referred offset shifted down to 0.18 V, showing that the SiC transistors on the op amp experience thermal aging.

The initial offset for the SiC two-stage op amp with PFET differential pair from wafer #4 is relatively high. Four additional op amp circuits (same topology) from three different reticles within wafer #4. The input offset value for each of the op amps is shown in the Fig. *32* wafer map. It can be seen that the input offset voltage for the op amp varies between 0.24 V to 1.2 V.

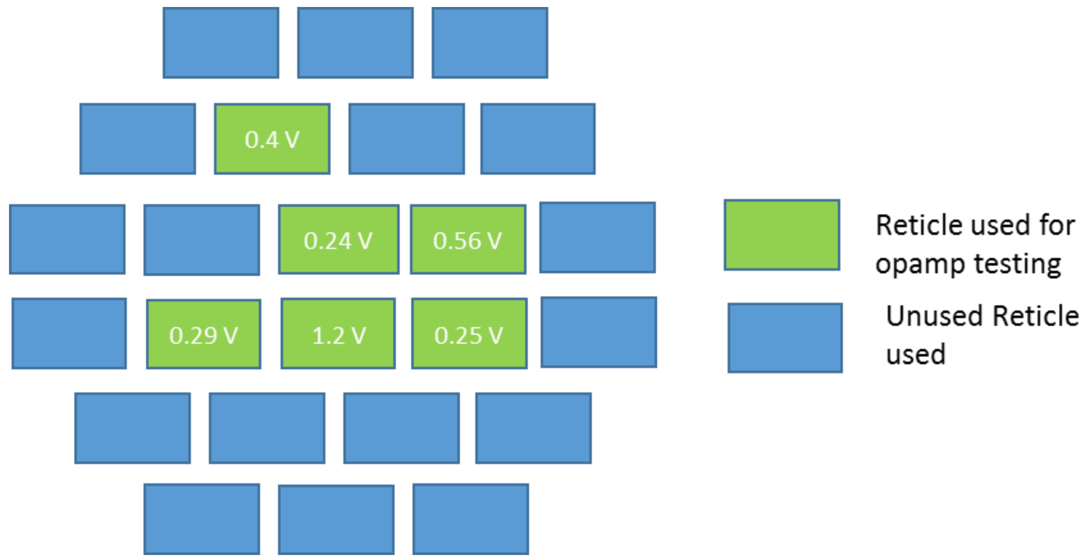


Fig. 32. Wafer #4 map indicating offset variations on the five tested op amps with PFET differential input pair.

The op amp unity-gain bandwidth was also measured. However, the measurement technique itself cannot be deemed accurate or satisfactory. Due to the lack of a network-analyzer with low-frequency bode plot analysis capability, the function generator with 25 MHz sinusoidal waveform capacity was used. A frequency varying sinusoidal signal, with 100 mV amplitude, was applied to the op amp's non-inverting node. At different frequency points, the op amp output amplitude was noted from the oscilloscope, and the respective gain was calculated. The frequency where the op amp's output signal amplitude became the same as the input signal amplitude was considered the unity-gain bandwidth (UGB) of the op amp. The measured UGB was approximately 67 kHz.

3.4.2 Two-stage NFET Differential Pair Op amp

The two-stage op amp with NFET differential pair was tested on the board level rather than on the probe station due to the difficulty in keeping the probe tips landed on the circuit die pads. The board was designed on Rogers 4350 material, and the setup for temperature testing utilized a ceramic chip carrier where the test die was attached using sintered silver epoxy (curing procedure provided in the Appendix-2), which has a temperature rating of 343°C. This adds the limitation to

test the circuits over 350°C. Testing at temperatures above 350°C can still be performed for a brief period.

To find the open-loop gain, the op amp was tested at 15 V supply with 100 mV, 1 kHz, sinusoidal signal overlapped on the DC common-mode voltage of 4 V. At 15 V supply, the quiescent current on the op amp, with no input signal provided, was less than 1 mA. This quiescent goes up to 2 mA at 20 V supply voltage. The sinusoidal signal was applied to the non-inverting node. The inverting node used the summation of the DC common-mode voltage and the measured input offset voltage that the op amp exhibits. The biasing resistor of 65 kΩ was provided externally. Three op amps die from three wafer #4 reticles before the testing with the sinusoidal input was tested to check the input offset variation. The measured offset voltages for each op amp die as follows, Die-1: 1.82 V, Die-2: 0.55 V, and Die-3: 0.09 V. The op amp on Die-3 is from a center reticle; hence the lower input offset voltage is expected. The op amp on Die-1 was selected for the open-loop gain measurement testing on the PCB level.

Fig. *33* and Fig. *34* show the oscilloscope waveforms for the op amp output at 25°C and 350°C when tested with the sinusoidal input signal. At 25°C, the open-loop gain was measured from the amplitudes of the input and output signals using the equation shown in Section 3.4.1.

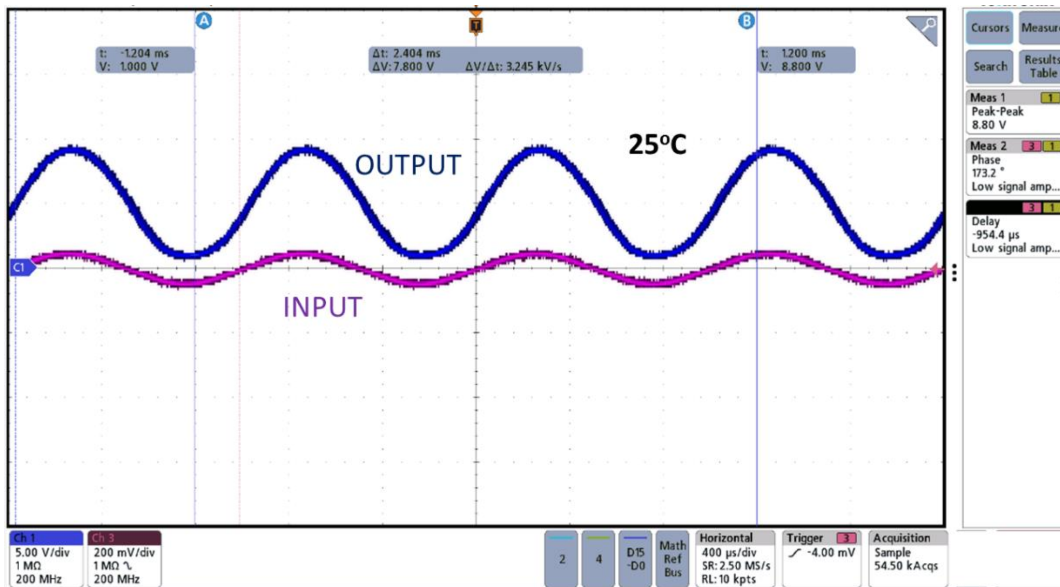


Fig. 33. Input-Output waveforms on the oscilloscope for the two-stage NFET differential input pair op amp at 25°C.

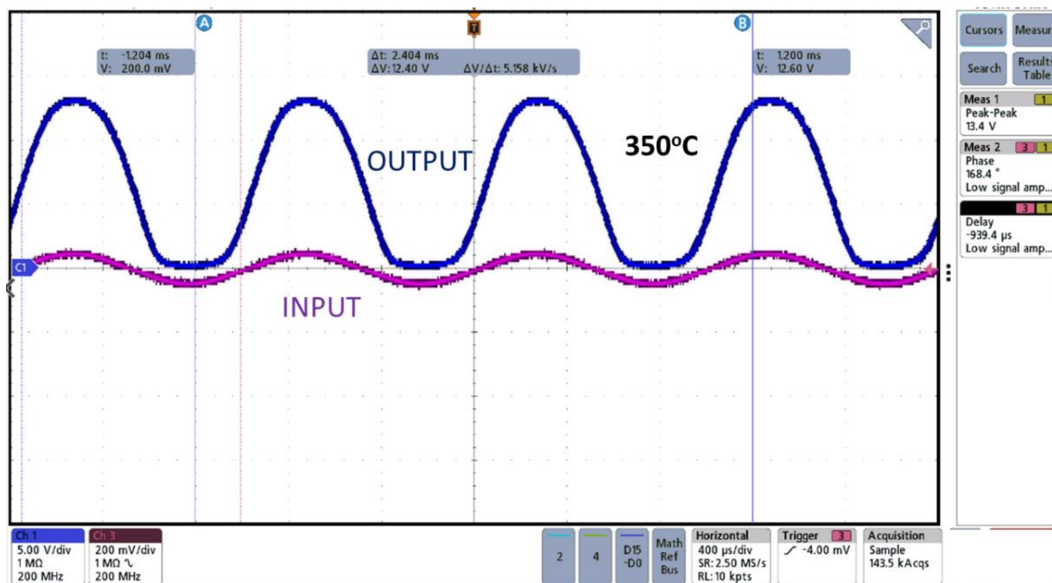


Fig. 34. Input-Output waveforms on the oscilloscope for the two-stage NFET differential input pair op amp at 350°C.

The DC gain for the NFET differential pair two-stage op amp is 38.9 dB at 25°C. At 350°C, the output almost saturates. Therefore the open-loop DC gain would have to be greater than 42.5 dB. As the temperature was increased, the initial input offset voltage (for this Die-1) of 1.82 V started to drop down, all the way to 0.34 V at 350°C. The unity-gain bandwidth (UGB) of the op amp

measured at 25°C was approximately 480 kHz. The UGB of the NFET op amp is higher than that of the PFET op amp, which is expected due to the higher transconductance of the NFET devices.

3.4.3 Two-stage Folded-Cascode Op amp

The folded cascode op amp was similarly tested on the Rogers 4350 PCB. The initial input offset voltage at 25°C and 15 V supply were measured to be 0.13 V on the op amp die under test. For the open-loop DC gain, the function generator was used to provide 50 mV, 1 kHz sinusoidal signal superimposed on a 1-V DC voltage. The biasing resistor of 30 kΩ and the ceramic capacitor of 10 pF for compensation was provided externally. The measured UGB at room temperature was approximately 30 kHz. The low bandwidth of the folded-cascode would mean the 3-dB cut-off frequency of the circuit is even lower, resulting in the circuit being applicable for only very low-frequency signal amplification. Based on the test results, the folded-cascode op amp has been left unused for the Fraunhofer module. The op amp output saturated for the 50 mV input signal, as shown Fig. *35*. The input signal from the function generator cannot be lowered below 20 mV, and with a saturated output signal, the op amp DC gain will be challenging to measure. The cascode op amp was tested under the non-inverting closed-loop configuration with externally placed feedback resistors of 500 kΩ and 5 kΩ to provide the closed-loop gain of 40 dB. The resulting input/output waveforms are shown in Fig. *36*.

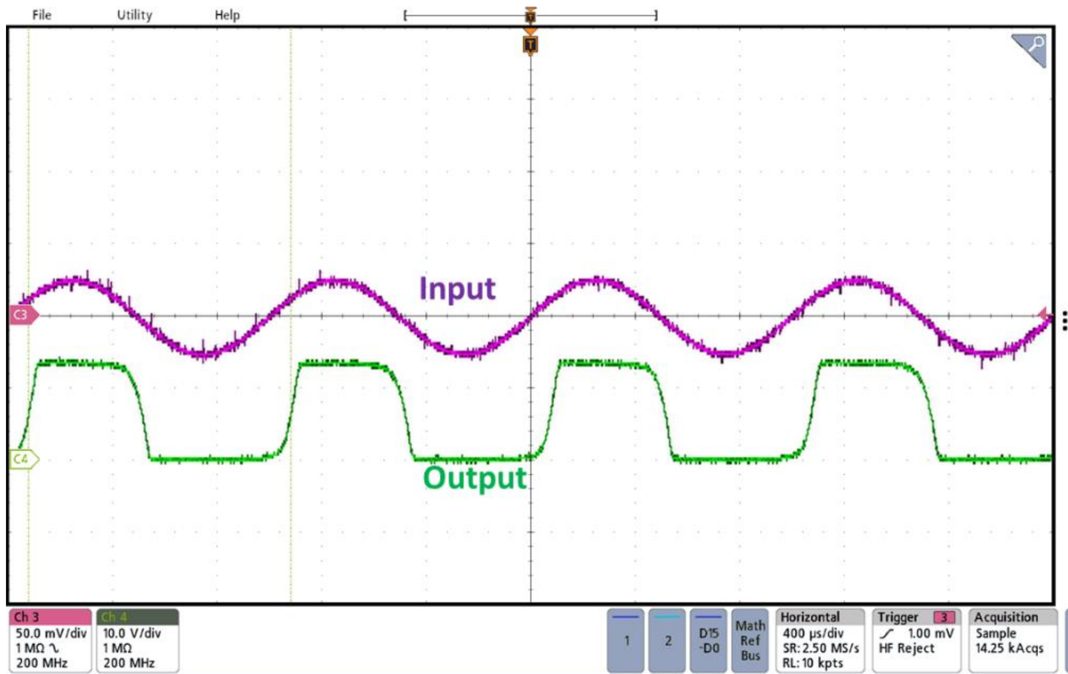


Fig. 35. Oscilloscope Input-Output waveforms for the two-stage folded-cascode op amp in an open-loop configuration.

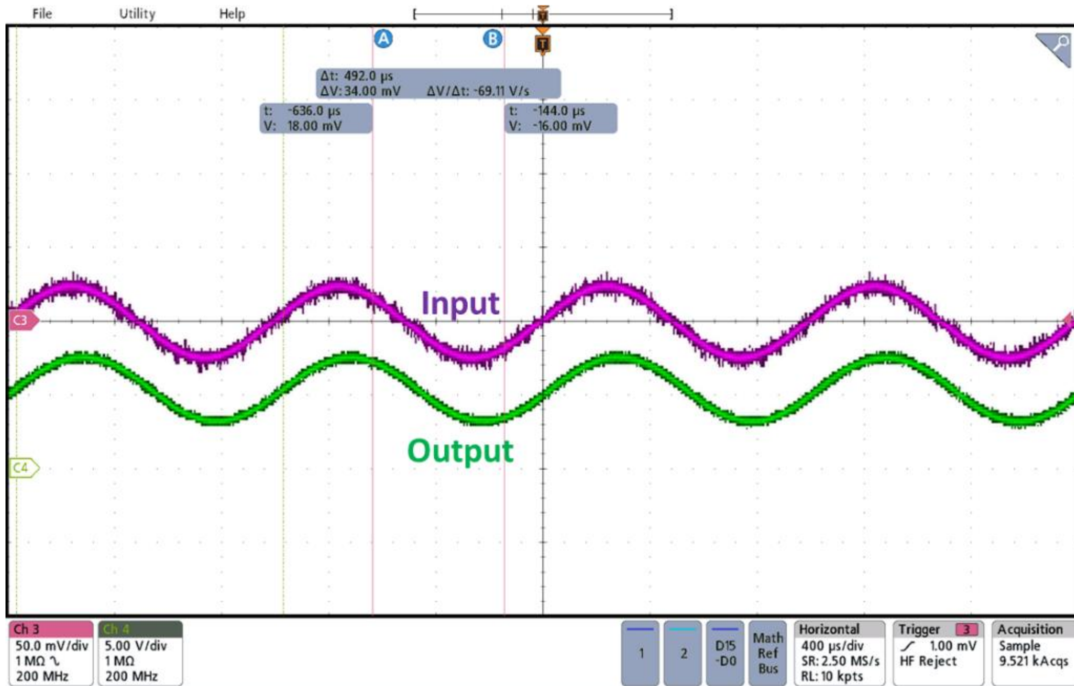


Fig. 36. Input-Output waveforms on the oscilloscope for the two-stage folded-cascode op amp under closed-loop

The output swing can be seen to be 5 V_{PK-PK} indicating the op amp is stable under the closed-loop application.

3.4.4 Voltage reference Circuit

In Section 3.2, it was pointed out that the reference circuit is expected to provide above 10.85 V at the reference output for 20 V supply. This value is significantly high and cannot be directly used in a regulator circuit. Hence, during the implementation of the voltage reference circuit in the Fraunhofer module, the reference output voltage must be scaled down using a resistor divider circuit composed of external resistor parts. For the reference circuit test, the external resistor ratio has to be set based on measured output on the specific reference (for example: at 15 V reference output, the resistor can be 110 kΩ and 30 kΩ to provide 3.2 V of reference output).

Initial testing on the reference circuit at 25°C involved measuring the reference output variation over the change in the supply voltage. The Fraunhofer PASS1 run's circuits are intended to operate under 15 V supply on the Fraunhofer module. The supply voltage is expected to be provided from a regulator circuit whose input would vary between 20 V to 30 V. This variation in the input supply to the regulator circuit would also be experienced by the reference circuit. In standard silicon processes, the availability of Zener diodes can clamp the main supply rail, which can then be fed to the reference. This results in the reference circuit operating at a lower supply rail compared to the regulator circuit's main input supply. In the SiC CMOS process, such Zener diodes are not available. Hence, the reference circuit will see the main supply rail and its variation. The drawback of this can be understood by looking into the reference circuit schematic in Fig. 27, where the source node of the two PFETs (Q19-Q20) is connected to the VDD rail. As the NWELL body node of these PFETs is also connected to the VDD rail, the NWELL to the PWELL body node of the NFETs within the reference circuit that are connected to the VSS (or 0 V) will observe high reverse potential when the applied VDD rail is 35 V. This would increase the current passing through the supply trace/rail of the reference circuit resulting in overheating of the trace.

Additionally, if the gate nodes of the PFETs that are to be connected to the two-stage op amp stay at 0 V while the supply rail (VDD) is increasing, then there is the possibility that gate oxide breakdown may occur. Therefore, the voltage reference circuit was tested for supply variation of 20 V to 30 V, provided from a laboratory DC power supply.

The output from the reference circuit and the respective scaled-down output from the resistor divider, measured through the digital multimeter, are shown in Table X. The current consumption for the reference circuit is also shown in the table. The overall current draw at 25°C with 20 V and 30 V supply is 9 mA and 33 mA, respectively. This is excessively high considering the NFET differential pair two-stage op amp showed current consumption of less than 1 mA at 20 V supply. Therefore, this excess current draw is due to the high leakage current between the NWELL (of the PFET) and the PWELL (of the NFET) connected to the P-epi of the die. The reference circuit was tested over temperature at the PCB level due to the high number of pins on the circuit. The supply voltage was kept at 20 V during temperature testing. Table XI. shows the variation at the scaled-down reference output. The reference voltage drops at a higher temperature due to the rate of change in the CTAT voltage across the diode being higher than the change in the PTAT current across the branch resistors.

Additionally, the on-chip resistors on the reference branch have a negative temperature coefficient that further complements the reference output voltage drop. The variation of the reference circuit output will impact the output of the regulator circuit in this process. The change in the regulator output voltage with respect to the reference voltage (V_{REF}) is provided by using the equation, $\Delta \boldsymbol{V_{REG}} = \Delta \boldsymbol{V_{REF}} * (\boldsymbol{1} + \frac{\boldsymbol{R_1}}{\boldsymbol{R_2}})$, here, R_1 and R_2 are the fixed feedback resistors. Assuming the

feedback resistor ratio of 4, the drop of 0.66 V on the reference output (Table X) would cause the regulator output voltage to drop by 0.66*(1+4) = 3.3 V.

Table X. Output Voltage of the Reference Circuit vs. Input Supply at 25°C

Input Supply (VDD)	Reference output (V)	Resistor divider output (V)	Current Draw (mA)
20	15.78	3.35	9
21	16.28	3.45	11
22	16.70	3.53	13
23	17.14	3.6	15
24	17.20	3.63	17
25	17.14	3.6	19
26	16.65	3.49	21
27	16.60	3.47	23
28	15.80	3.39	26
29	15.56	3.32	30
30	15.03	3.18	33

Table XI. Reference Circuit Output (scaled down) Over Temperature for VDD = 20 V

Temperature (°C)	Reference Output Voltage (scaled down) at VDD = 20 V	Current Draw (mA)
25	3.35	9
150	2.91	10
250	2.71	12
350	2.69	12.5

Chapter 4. Silicon Carbide Signal Conditioning System Prototypes on LTCC

This chapter will describe the design and assembly considerations for the two signal conditioning prototypes implemented with the SiC CMOS circuits from the Raytheon UK (RUK) and Fraunhofer process. Each prototype shown in this chapter is fabricated on low-temperature co-fired ceramic (LTCC) material (DuPont^{TM} GreenTape^{TM}9k7) [33]. The chapter details each prototype module's different iterations and the assembly methods introduced to allow testability of the modules under different setups, like laboratory bench-top, thermal chuck on a probe station, and high-speed spin rig.

4.1. RUK LTCC Module Schematic

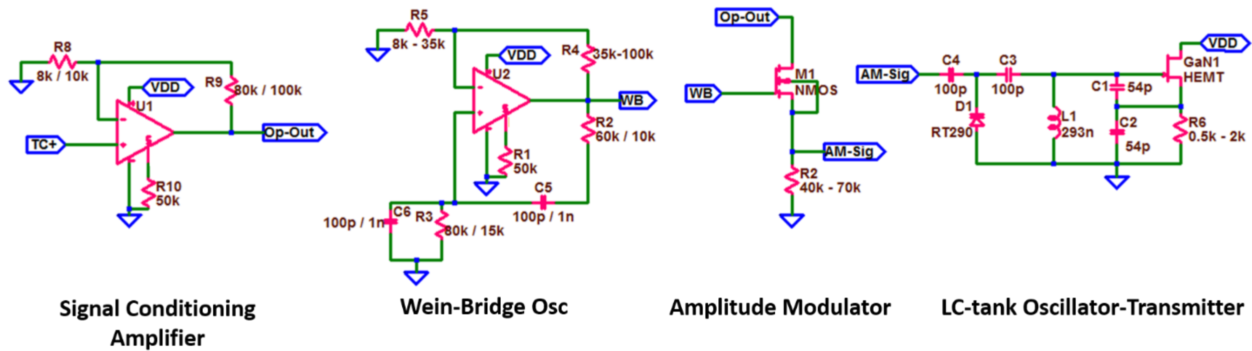


Fig. 37. RUK LTCC module schematic.

The RUK LTCC module schematic diagram is shown in Fig. 37. The system is divided into two sections: (i) signal conditioning op amp section and (ii) data-transmission section. The signal conditioning op amp is realized with a two-stage PFET-differential input pair op amp in a closed-loop configuration with a gain set to 11 via the resistors R8 and R9. The op amp circuit has been tested over temperature, with detailed results and performance specifications that can be found in Appendix-3. The data transmission section is sub-divided into two segments: the Wein-Bridge oscillator based amplitude modulator and the frequency modulator. The amplitude modulator is

realized with a SiC transistor (M1) and source resistance, R6, in the source follower configuration. The transistor's (M1) gate node is derived from the Weinbridge (WB) oscillator, which is designed using the two-stage op amp with the same specification as the signal conditioning op amp. The M1 is a 20/1.2 μm NFET device with specific parameters provided in Appendix-1. The required biasing for both the op amps is provided through external resistors (not shown in the schematic diagram). The WB oscillator's output frequency is a function of the combined R-C values of the external passive components – R2, R3, C5, and C6. The closed-loop gain for the oscillator's op amp has to be greater than 3 to sustain oscillation and is set by the resistor values of R4 and R5. The WB oscillator output frequency can therefore be found by the following equation,

$$f_{WB} = \frac{1}{2\pi\sqrt{R_2R_3C_5C_6}}$$

The frequency modulator is composed of an LC-tank Colpitts oscillator connected to a CREE indium gallium nitride (InGaN) LED varactor (reverse breakdown at 5 V). The LC-tank components have parasitic resistances; hence a depletion-mode GaN transistor is required to provide the negative impedance to sustain oscillation. Previously such a negative impedance Colpitts oscillator with wide-bandgap semiconductors has been shown to operate in the literature [34]. The oscillator's loop gain depends on the transconductance of the GaN transistor and the source resistance, R1. The inductor (L1) is designed in the module with a two-conductor thick-film gold layer in square-planar spiral coil format. The inductance value is derived from the modified Wheeler formula, as shown below,

$$L = K_1\mu_0\frac{n^2d_{avg}}{1+k_2\rho}.$$

Here the K_1 and K_2 are the layout dependent coefficients of values 2.34 and 2.75, respectively, μ0 is the permeability, d_{avg} is the average {defined as 0.5*(d_{out}+d_{in}), where d_{out} is the outer diameter and din is the inner diameter}, and ρ is the fill ratio, defined as {(d_{out}-d_{in})/(d_{out}+d_{in})}. The number of turns, turn width and the turn spacing provide the outer and inner diameter, which are selected to derive 293 nH of inductance. The thickness of the spiral inductor trace does not impact the inductance value; however, in an oscillator application, skin depth becomes an issue at higher frequencies. The skin depth depends on the property of the conductor material used to implement the spiral inductor and the frequency of operation. The following equation can determine the skin depth value,

$$\boldsymbol{\sigma = \sqrt{\frac{\rho}{\pi f_o \mu_r \mu_o}}}$$

With gold as the conductor material and an operating frequency range of 34 to 80 MHz, the resulting skin depth would be limited to 13 µm. Two mil (50.8 µm) thick gold traces have been used to implement the module's spiral inductor. The tank capacitors, C1 and C2, are 54 pF in value. The DC coupling capacitors are valued at 100 pF each. The varactor capacitance (D1) ranges between 170 to 180 pF, for a tuning voltage range of 1 V. The Colpitts oscillator output frequency can be derived from the following equation,

$$\boldsymbol{f_{osc} = \frac{1}{2\pi\sqrt{LC_T}}}\text{ , where } \boldsymbol{C_T = \frac{C_1C_2}{C_1+C_2} + \frac{D_1C_3}{D_1+C_3}}$$

The overall system will be powered externally via high-temperature rated wires with a decoupling capacitor (not shown in the schematic) on the module to minimize noise ripple generated from the external supplies. The module's operating principle is as follows – the signal conditioning amplifier

will amplify the sensed signal within the extreme ambient (e.g., thermocouple sensor). The amplified signal would then be amplitude modulated with a WB oscillator and SiC transistor in source-follower mode. The amplitude modulated signal will shift the varactor capacitance connected to a Colpitts oscillator to form a frequency modulated signal, which will be transmitted to a remotely located receiver via the oscillator's inductor. The transmission signal strength can be increased by lowering the value of the source resistance, R1. However, this will increase the overall current consumption by the complete system.

4.2.RUK LTCC Module Simulation Results

The signal conditioning op amp and the amplitude modulator on the RUK module system shown in Fig. 37 were simulated using the temperature binned models, specifically developed for the Raytheon UK process SiC CMOS process technology. The simulation results are shown in Fig. *38*.

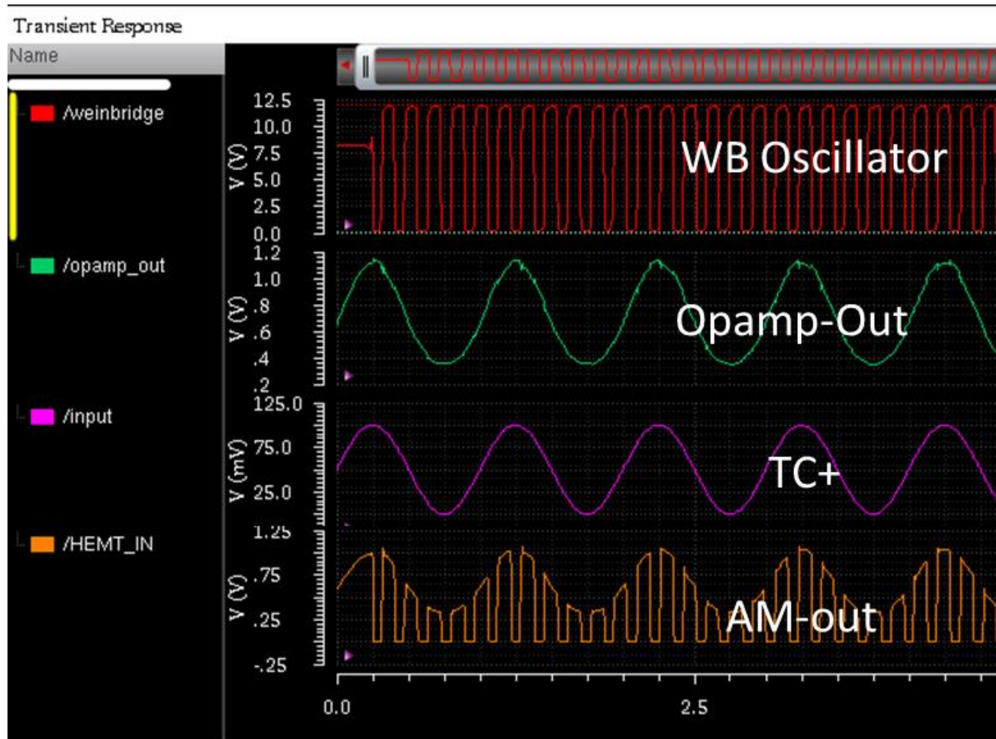


Fig. 38. Simulation results for the RUK signal conditioning op amp and amplitude modulator circuit.

The simulation was performed with 1 kHz, 100 $mV_{pk\text{-}pk}$ sinusoidal signal, applied to the TC+ node of the sensor op amp. The biasing current in the simulation was equal to 98 µA. The feedback resistors in the non-inverting configuration were 50 kΩ and 5 kΩ, respectively. The op amp output DC level was 0.6 V as the common-mode voltage for the op amp is set to 0 V. The closed-loop gain on the op amp was 18.5 dB, lower than the expected theoretical gain of 20.82 dB. The Wein-Bridge oscillator output frequency was 6.15 kHz. The bridge oscillator frequency is lower due to the loading effect at the op amp output due to feedback resistors. The amplitude modulator circuit sampled the op amp output with around 80 mV of difference (for the peak amplitude), which is due to the drain-to-source voltage drop across the AM NFET (M1) pass transistor.

The simulation for the frequency modulator section on the module was simulated on LTSpice with depletion-mode JFET, to verify the operability of the architecture due to the absence of SPICE

model for the GaN HEMT. The InGaN varactor model was not available. As a result, simulation for the varactor was performed by using a simple capacitor with its capacitance varying by 10 pF to replicate the change in varactor capacitance. The schematic for the LC-tank oscillator simulation is shown in Fig. 39.

Fig. 39. Frequency modulator schematic in LTSpice to verify the LC-tank oscillator architecture.

The capacitance of C4 in the schematic above varies from 170 pF to 180 pF, resulting in the deviation in frequency. The change in capacitance will come from the difference in the voltage on the InGaN varactor device's cathode terminal. The simulated FFT plot for the schematic in Fig. 39 is shown in Fig. 40. The frequency deviation between the transmitted signal peaks is 188 kHz for a change in capacitance value of 10 pF. The information is critical to understand in the case of utilizing an external receiver system to detect the frequency modulated output from the RUK module. Standard receivers have demodulators built into them, which has limitations in the range of bandwidth at which it can demodulate. If the frequency deviation is higher than the receiver's demodulator bandwidth, then accurate signal detection will not be possible.

Fig. 40. Simulated FFT plot of the output of the LC-tank oscillator in Fig. 39.

4.3. RUK LTCC Module Layout

The RUK LTCC module layout is shown in Fig. 41, with six pads in the bottom left. The AC+ and AC- have been kept to add provision if an AC power supply source is used, however as the system does not incorporate a regulator or reference circuit, those pads have not been used in the module assembly or testing. The VDD and GND pads connect to dc power supplies, and the TC+ connects to the positive sensor node. The negative node of the sensor will be connected to the GND (ground) pad. The layout includes 20 layers of LTCC (Each LTCC layer is 240 µm thick) for cavity implementation and three layers of conductors for routing. The cavity layers in the layout are implemented using a Python script. Each cavity is set to the dimension of the SiC die, or passive component and the depth of the cavity is set to 4 times the respective thickness of the passive or SiC die. The excess depth on the cavity is added to consider the epoxy that will be added to the cavity to attach the components. The InGaN varactor chip has 95 µm thickness, so no cavity is provided for the part. A minimum of ten mils or 254 µm diameter VIA sizing has been used to connect the routing layers. The cavities allow placing the passive components, the SiC and GaN

devices on the module. To realize connectivity between the die and passive pads to the pads/traces on the module, 1-mil (25.4 µm) thick gold or aluminum wirebonds have been used. Gold is more suitable for the wirebonding purpose due to compatibility as all the conductor traces on the module are formed of gold material. Along with that, gold has a high melting point.

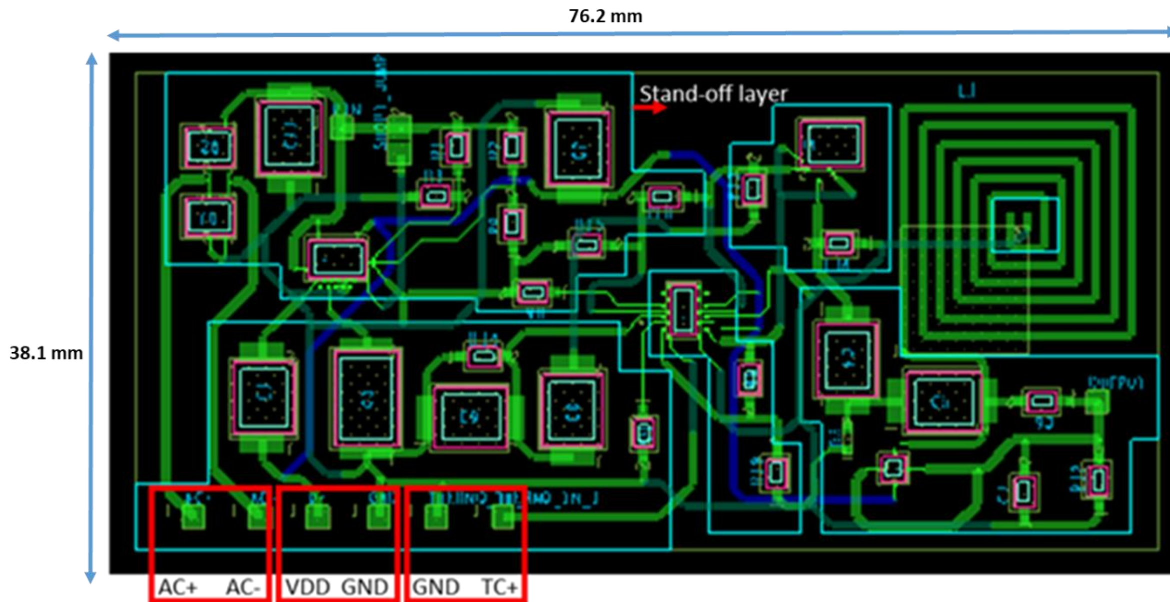


Fig. 41. The layout of the RUK LTCC module.

The module layout is designed for the dimensions of length = 68.58 mm, width = 34.3 mm, and height = 5.08 mm. The associated constraint with the module dimensions is generated from the ceramic matrix composite (CMC) housing, which is necessary to hold the LTCC module. The CMC housing structure comprises a base structure and a top cover to enclose the module and therefore protect from any external effects during the module's operation at high-temperature, high pressure, or high-speed rotation. The physical image of the complete CMC housing structure can be seen in Fig. 42. The two drill holes on the CMC housing base account for wire feed-through to connect to the external power supply and sensor node. It has to be noted that the layout dimensions shown in Fig. 41 are scaled up compared to the derived dimensions from the CMC housing base

structure due to the post-firing shrinkage that occurs in the LTCC fabrication procedure. The CAD layouts for LTCC modules are normally designed by scaling the dimensions up to 9 % of the actual area to mitigate the shrinkage issue.

The first six layers of the LTCC module have been used to create a stand-off layer (Fig. 41) to protect the wirebonds from getting damaged by the CMC top cover. Two different approaches have been used, the first one - forming the stand-off within the entire module, and the second one – creating the stand-off around the perimeter of the design. The LTCC module layout with the second approach is shown in Fig. 43. The second approach provides much more flexibility in terms of placing the components and connecting wirebonds. Additionally, the second approach also minimizes the probability of having VIA openings. This can be understood by following the lamination step of the fabrication procedure of LTCC modules. Each LTCC sheet is placed over the other in a sequential format in the lamination step before firing at 900°C. Each sheet has a different punch-through to incorporate the component cavity depth, routing VIAs (filled with gold paste) and the stand-off layer. The cavity depth varies as the components' thickness is different, and as the module dimensions are small, the components are placed close to each other. With these issues, the chances of getting non-uniformity during lamination of the LTCC sheets increase. This would introduce air gaps between sheets, which could result in the routing VIA hole (or punch-through) on a top sheet not to form contact with the VIA hole on the bottom sheet and inadvertently cause VIA opening. In the second approach, with the stand-off layer only covering the perimeter, the chances of non-uniformity are reduced.

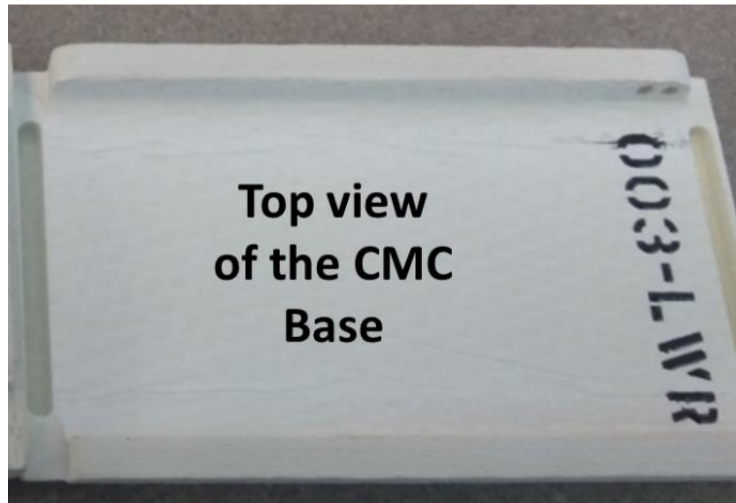


Fig. 42. (Top) complete CMC housing structure, and (bottom) CMC base structure where the LTCC module sits.

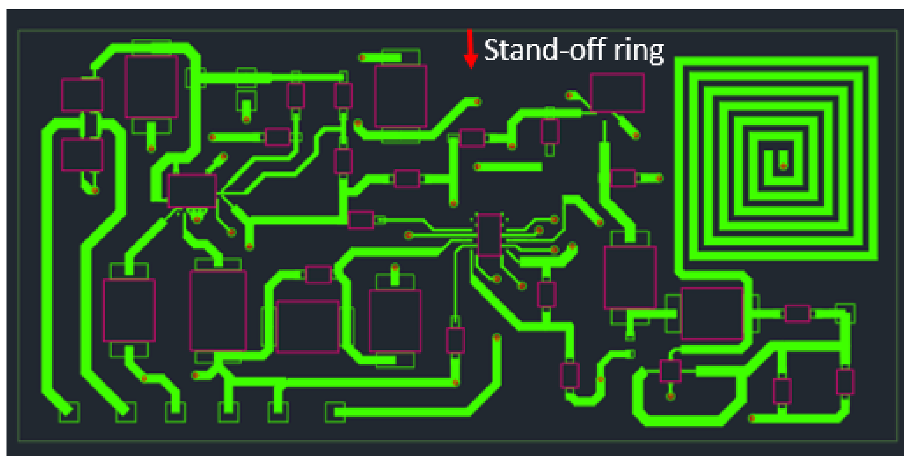


Fig. 43. The second layout of the RUK LTCC module with a stand-off layer designed on the outer periphery.

To accommodate the maximum cavity depth, eight LTCC sheets/layers have been used. The final six LTCC sheets provide structural rigidity for the module. Fig. 44 shows the fabricated RUK

module-1 with the stand-off routed over the inner module area. The module showed multiple VIA openings, as marked by red-circle on the figure.

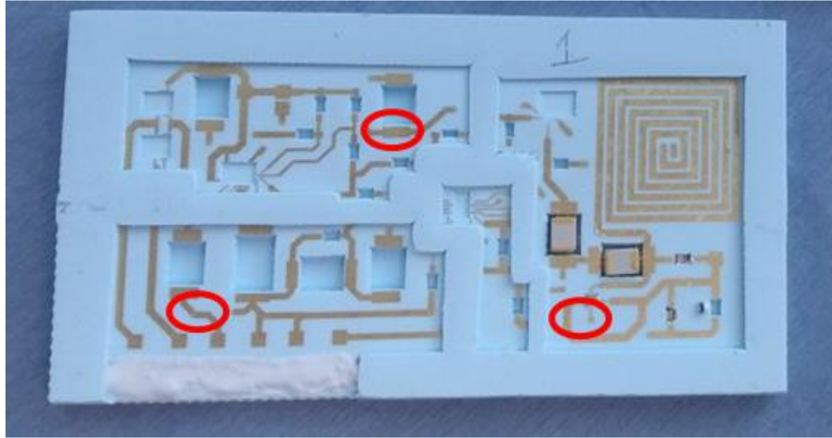


Fig. 44. Fabricated RUK LTCC module-1 with stand-off layer routed over the inner area of the module (red circled sections indicate places with VIA opening).

4.4. RUK LTCC Module Assembly

The two wholly assembled modules (#2 and #3), with RUK circuits and the stand-off routed on the module's outer periphery, are shown in Fig. *45*. The modules did not present any via openings like the one shown in Fig. 44. The capacitor and resistor components are all rated at 500°C temperature. The capacitors have gold termination for the connecting pads. However, the resistor has two termination pad options – gold and platinum-gold. The gold terminated resistor parts have been selected due to the ease of wirebonding. The wirebonder utilizes an ultrasonic technique to form the first bond and wedge technique for the second bond. To properly create gold wirebonds, the gold traces and gold die/termination pads on the module and the components, respectively, are required to be primarily heated up at temperatures around 125°C to 135°C. However, in the platinum-gold pads, this temperature has to be increased to 180°C.

The passive components and the active SiC and GaN devices/circuits, apart from the GaN LED varactor, are attached to the module by dropping non-conductive 940 HT ceramic epoxy (white

substance on Fig. *45*). The curing method for processing the ceramic epoxy can be found in Appendix-2. The list of the passive components used for the RUK module-2, with their respective footprint-size code, are shown in Table XII. The tolerance level for all the passive parts is within 0.5%. It is to be noted that any capacitor with a higher voltage rating (> 50 V) and capacitance value would occupy a larger footprint area on the module.

The connecting pads on the second version of RUK module-2 have a different assembly approach compare to the first version of the RUK module-2. This is because the first version is intended to be tested at high temperatures under a probe station equipped with a thermal chuck. The second version is assembled to be tested on a spin-rig (capable of rotating at 11,000 rpm) equipped with slip-rings to support wire feed-thru for power delivery. The second version has 0.1 mm diameter standard tin-plated copper wires connected to the module gold pads via sintered silver epoxy. To ensure the wires do not rip-off or move during spin testing, ceramic epoxy has been deposited on top of the wire. There is another option to perform wire assembly on the gold pads of the module through tack-welding. However, that process requires curing the gold pads with silver paste at 900°C before component assembly. Directly attempting to arc-weld or resistance weld would result in the destruction of the thick gold pads.

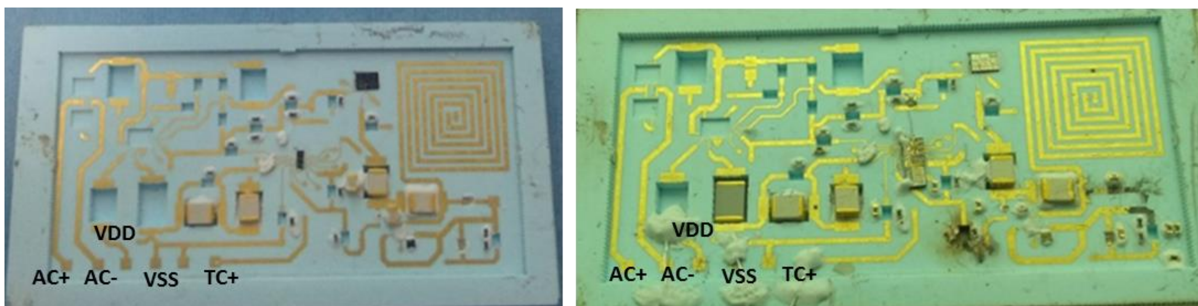


Fig. 45. RUK LTCC module-2 (for high-temperature test –left) and (spin test -right) with assembled components

Table XII. Passive Components for the RUK Module and Their Footprint Codes

Component Label (from Fig.)	Measured Value	Unit	Footprint Code	Maximum voltage-rating (V)
C1-C2	992.5 – 998.7	pF	1209	300
C3-C4	99.4 – 100.3	pF	1209	300
C5-C6	54.2-54.3	pF	0402	50
R1	2.54	kΩ	0402	-
R2-R3	10.01-15.02	kΩ	0402	-
R4-R5	40.1	kΩ	0402	-
R6	70.05	kΩ	0402	-
R7-R8	10.05-100.03	kΩ	0402	-
Biasing resistors	50	kΩ	0402	-
Decoupling capacitor to minimize supply ripple	10	nF	1812	100

The GaN LED varactor has been attached to the module using sintered silver epoxy. This is because the LED has a vertical orientation with the cathode pad formed at the bottom and the anode pad at the top. To connect the cathode pad to the trace on the module, conductive epoxy is therefore mandatory. Additionally, the LED varactor has a minimal dimension of 270 μm × 270 μm, making the part challenging to pick, place and attach to the epoxy. A small commercial vacuum tip (AirTip^{TM}) with 5 mils (127 μm) diameter has been used to pick and place the varactor part.

As mentioned in Section 4.1, the RUK module has 20 LTCC layers, resulting in the module's overall height at 4.8 mm. This is problematic as the CMC base structure's height to the top of the CMC cover structure is 5.08 mm. The CMC cover has to contact the stand-off ring on the module so that the module, while completely enclosed in the CMC housing, does not move. To confirm the stand-off ring is flush with the CMC top cover, a fabric composed of fiber-glass, as shown in

Fig. 46, has been used underneath the module and the CMC base structure to provide that extra height. The prepping procedure of the fiber-glass fabric can be found in Appendix-2.

Fig. 46. Image of the Nextel fiber-glass fabric on the base of the CMC housing structure.

The second module's complete assembly with fiber-glass fabric placed underneath the CMC base is shown in Fig. 47. The wires are fed through the drill holes on the CMC housing base structure (Fig. 42).

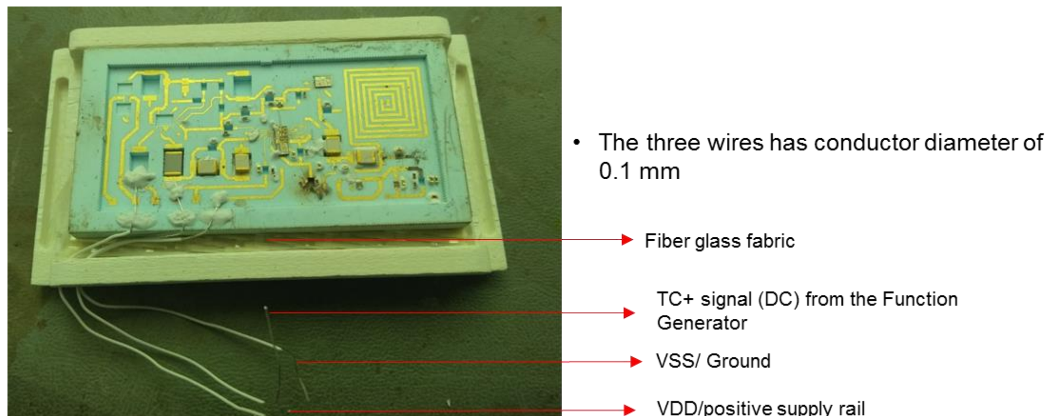


Fig. 47. Wire assembly on the RUK LTCC module and placement on the CMC housing structure (housing top cover (or lid) not shown in the image).

4.5. Fraunhofer LTCC Module Schematic

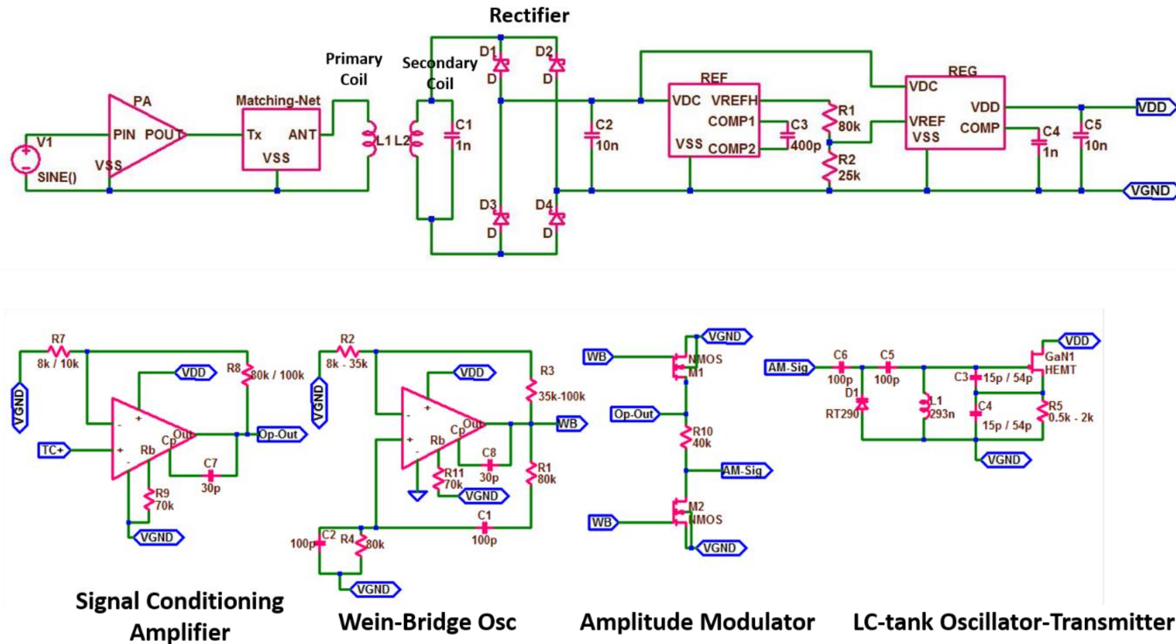


Fig. 48. Schematic of the Fraunhofer LTCC module.

The schematic for the Fraunhofer LTCC module is shown in Fig. 48. The schematic can be divided into two sections – (i) the wireless power transfer/delivery section, via resonant inductive coupling method [35] that is composed of the bridge-rectifier, regulator, and voltage reference circuit blocks (ii) the signal conditioning system. In addition to the wireless power supply section, the Fraunhofer module also has the provision to support the wired power supply. To accommodate the module's wireless power transfer mechanism, the bridge rectifier circuit is designed using SiC Schottky diodes with a forward voltage drop as low as 0.65 V. The bridge rectifier input will be derived from a resonant circuit composed of a wire coil inductor and a capacitor. The power transfer frequency is to be tuned within the range of 5 MHz to 15 MHz. The exact frequency will depend on the implemented wire coil inductor and the capacitor. To smooth out the bridge rectifier output, a 10 nF capacitor has been used. As the rectified output would vary depending on the proximity of the inductor coil on the module and power delivery antenna, a voltage regulator is required to

provide stable output for powering the signal conditioning circuits. The SiC voltage regulator circuit, in connection to the SiC voltage reference circuit, provides that regulated output of 15 V to the signal conditioning system. The SiC voltage reference circuit includes additional external capacitors to compensate for its internal two-stage NFET differential input pair op amp, which are not shown in the schematic diagram. The signal conditioning system's design and operating principle remained the same, as shown in the RUK module. The signal conditioning op amp is composed of a two-stage SiC op amp with a PFET input differential pair. The Wein-Bridge (WB) oscillator is designed with another two-stage SiC op amp. Similar to the RUK module, the two-stage signal conditioning op amp is set in a non-inverting closed-loop configuration with a gain of 11. The RC–network values on the WB oscillator utilize smaller footprint capacitors (100 pF with 0805 footprint code) to save design area. The amplitude modulator circuit is modified to use two n-channel transistors instead of the single transistor in the common-drain configuration. This would result in the amplitude-modulated output in the Fraunhofer module being in the opposite phase to the WB oscillator output. The architecture for the sensed signal transmitter circuit has been kept the same as the RUK module. The spiral inductor for the Colpitts oscillator has the same dimension to provide 293 nH of inductance. However, the tank capacitor values have been changed to a range of 10 pF to 25 pF to obtain a higher transmission frequency. This is to minimize coupling between the power transfer coil and the conditioning system’s signal transmission inductor. The DC blocking capacitors are kept at the same value of 100 pF.

All of the SiC circuits in the Fraunhofer module are designed on the 1 μm Fraunhofer process with aluminum metallization. The results for the Fraunhofer process's regulator circuit are shown in Appendix-3. The circuit suffers from a low phase margin at higher temperatures and requires high output load capacitance. However, using high-value capacitors would increase the footprint area

and violate the CMC housing structure's module design area constraint (see Section 4.3). The transistors in the Fraunhofer process are in the development stage, and results from the circuit testing in Chapter 3 show that the circuit behavior would not satisfy the complete functionality of the signal conditioning system implemented on the Fraunhofer module. However, the module design allows the team to test the functionality of other sub-sections of the system at high temperature and understand the methods to implement the resonant coil inductor for realizing the wireless power transfer mechanism.

4.6. Fraunhofer LTCC Module Layout

The initial Fraunhofer module layout can be seen in Fig. 49. The layout area is scaled by 9% of the specified area constraint to incur the post-fire LTCC shrinkage, similar to the RUK module. The layout consists of 20 LTCC layers for cavity and VIA punch-thru and the three conductor layers for routing, like the RUK module. The Fraunhofer module's layout is denser than the RUK module due to a higher number of component usage. The SiC ICs are diced into smaller areas, and most passive capacitor parts (apart from the decoupling capacitors) are selected with 0805 footprint sizing code to minimize layout space. The footprint code for the resistor parts remained the same as the RUK module. The cavity thickness for each die is defined by the die thickness and the additional depth required to add the epoxy material for attachment. The ‘S-Diode’ section on the module layout refers to the Schottky diode, a vertical device (similar to the GaN varactor) with the anode terminal on the top and the cathode terminal on the bottom. To make contact with the anode, the base of the Schottky diode’s cavity has the third routing conductor layer over it. The module layout accommodates both the stand-off ring and the cavity for inductive coil (for wireless power transfer). The inductive coil has 16 layers of cavity depth. Similar to the RUK module, the first six layers provide the depth for the stand-off ring. There are multiple test pads along connecting pads

on the bottom-left of the module to allow connectivity to sensor nodes and support wired power supply in the absence of the wireless power transfer mechanism. The resonant inductor coil cavity is 0.4 mm wide. The cavity allows placing a bare-wire-based coil. The other and more suitable option is to deposit conductive material paste (like silver) on the cavity to form the coil. The inductor coil cavity can be wider to lower the wire resistance; however, this would increase the module area. To ensure connectivity from the top-conductor on the module to the inductive coil, a conductor trace has been placed above the sixteenth LTCC layer, and multiple VIAs have been run down from the top conductor to that trace.

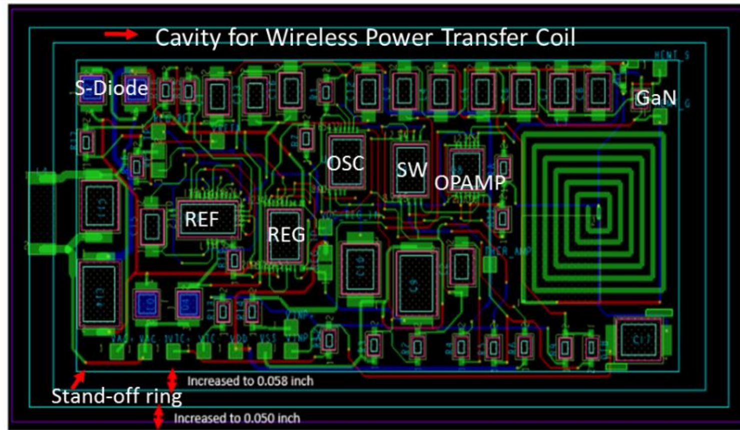


Fig. 49. The layout of the initial version of the Fraunhofer module.

The fabricated module based of the initial layout is shown in Fig. 50. It can be seen that the coil cavity opening over the horizontal axis is skewed, and the stand-off ring width is uneven in all corners. The trace on the sixteenth LTCC layer is also missing resulting in the placement of wire or deposit of conductive material paste being impossible. The observation from the first fabricated board resulted in removing the stand-off ring on the next modified layout, as seen in Fig. 51. There are two modifications – (i) modified layout has the trace on the sixteenth LTCC layer, partially extended, to make contact to the wire coil, (ii) modified layout extends that trace on the sixteenth LTCC layer throughout the cavity ring to allow deposition of conductive silver paste to form the

coil. In addition to these modifications, four VIAs of 1 mil diameter have been run down from the top conductor to this coil trace. There is also a side-wall or stand-off ring added on the outer periphery of the module.

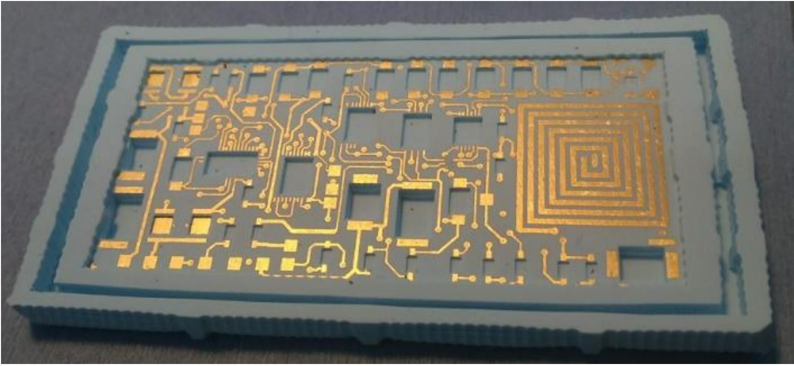


Fig. 50. The initial version of the fabricated Fraunhofer module.

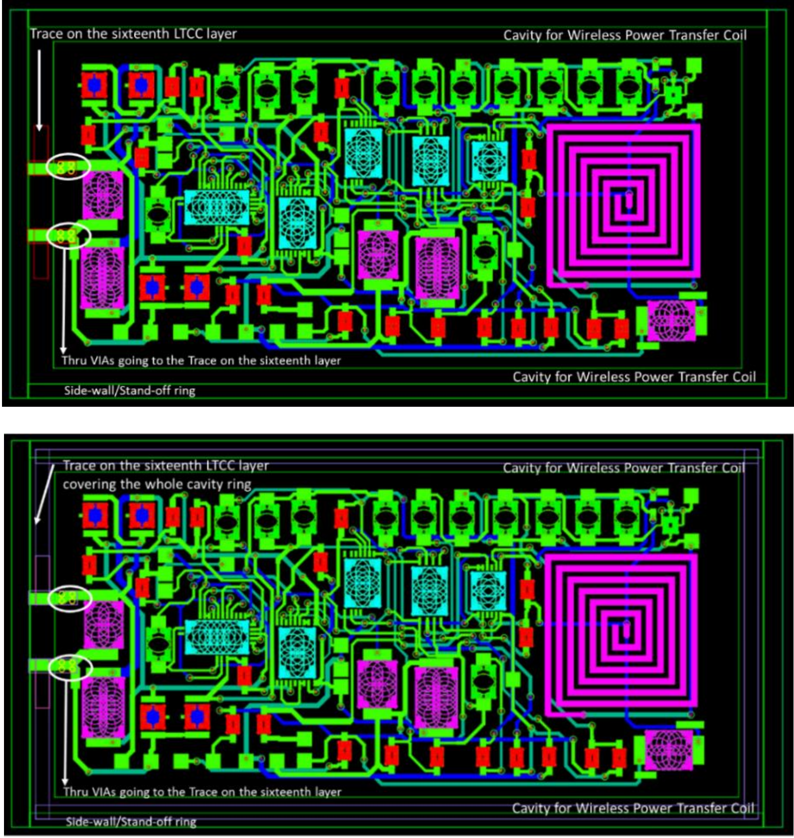


Fig. 51. Two modified layouts for the second version of the Fraunhofer module.

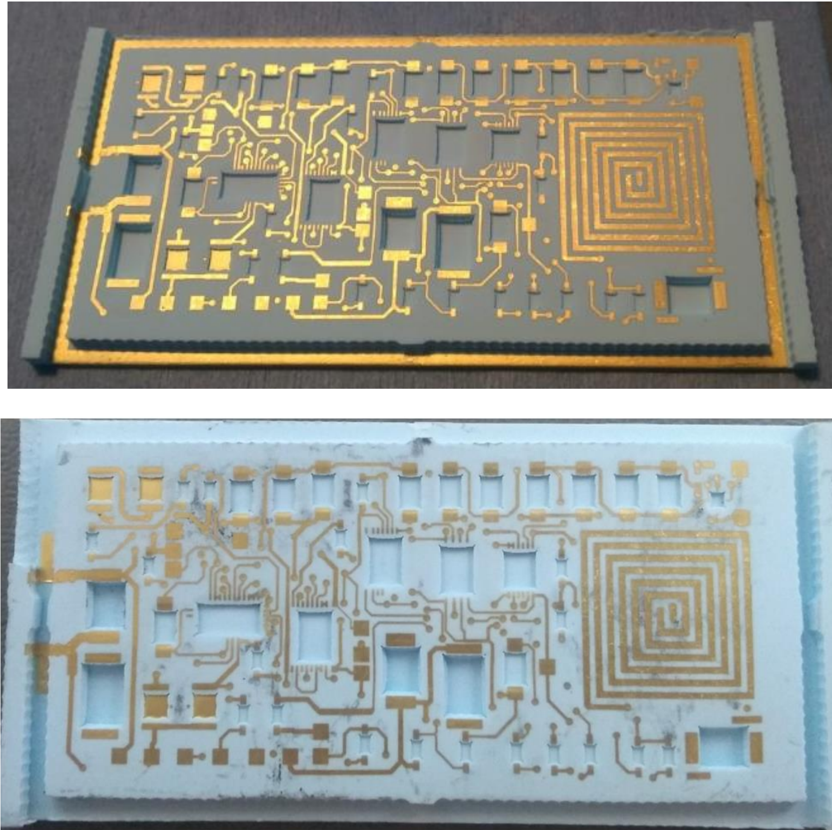


Fig. 52. (Top) Thick-film gold trace for depositing silver paste for creating power receiving coil (module-1), and (bottom) partial gold trace to assemble wire coil for wireless power reception (module-2)

The resulting fabricated module (#1 and #2) images are shown in Fig. 52. It can be seen in Fig. 52 (top) that the trace on the sixteenth LTCC layer of module-1 has been formed, but the stand-off ring, across the horizontal plane of the module's outer periphery, no longer exits. The same problem is repeated on the other module-2 in Fig. 52 (bottom). The missing stand-off ring's width across the horizontal plane is 1.4 mm is relatively small to sustain the post-firing stress. This would mean the wirebonds on the components and the traces will be damaged once the CMC housing enclosure is applied. However, these modules have been used to assemble and wirebond the Fraunhofer circuits to test the wireless power transfer system's functionality and signal conditioning system at bench-top and under probe station setup.

To ascertain the stand-off ring for wirebond protection, another modification on the layout of the Fraunhofer module has been performed (module-3). The trace associated with the inductive coil for wireless power transfer has been opted to print on the back of the module-3, freeing up space to accommodate a wider (3.43 mm) stand-off ring. As the back of the module-3 does not include any components, the coil trace width has also increased to 5.2 mm. This would lower I-R drop across the coil during wireless power transfer as now wider wires can be used. However, the trade-off here is the removal of the cavity for the inductor coil, which would mean depositing conductive paste to form the coil or utilizing a bare wire as the receive coil will no longer be viable options. Instead, the trace at the back of module-3 will be the receive coil. A gap underneath the connecting pads has been introduced to allow easier access for wire connectivity and feedthrough. The cavity depth for the components has also been modified. As the Fraunhofer module is much denser than the RUK module, and as mentioned earlier with the issues of VIA opening due to varying depth within cavities in close proximity, the cavity depths for the components are distributed in two categories – (i) components with a thickness lower than four LTCC layers will have same depth, (ii) components with a thickness lower than eight LTCC layers will have the same depth. The trade-off will be the increased cavity depth for certain components resulting in increased wirebonding complexity. The image of the Fraunhofer module-3 after fabrication is shown in Fig. 53. The bottom view of the module shows a wide gold trace coil for wireless power reception. The top view does show the successful fabrication of the stand-off layer.

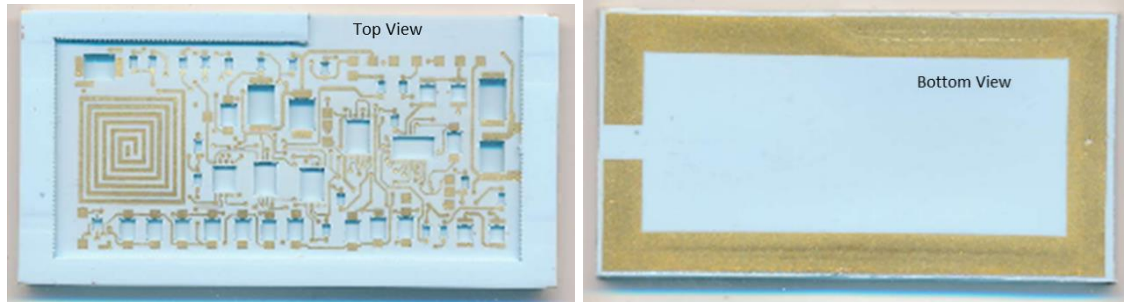


Fig. 53. The third version of the Fraunhofer module with wider gold trace on the back of the module for power reception coil.

4.7. Fraunhofer LTCC Module Assembly

The module-1 in Fig. 52 (top), with the one mil thick gold trace coil covering the outer cavity, has been assembled first to verify the circuit blocks composing the signal conditioning system. The post assembled image of the module is shown in Fig. 54.

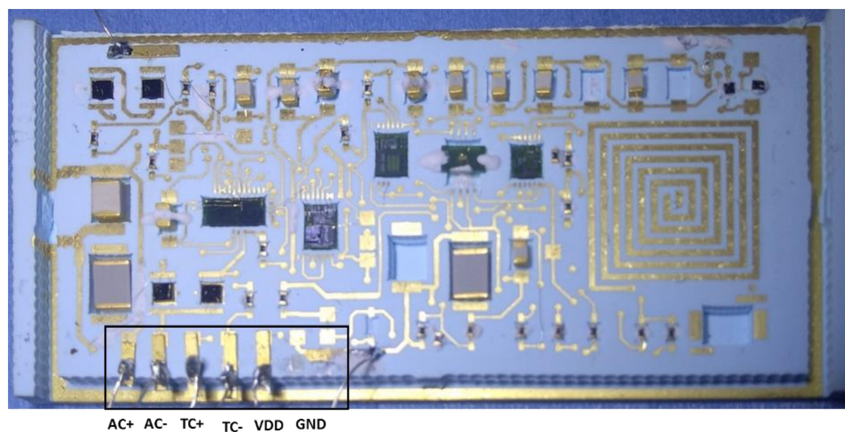


Fig. 54. Fraunhofer module-1 (with the complete thick gold trace on the outer periphery) after complete assembly.

It can be noticed that module-1 includes gold-plated frames on the section of the printed pads on the module. These gold-plated frames are attached with sintered silver epoxy to the printed gold pads on the module. This allows the assembled module to be tested both at bench-top, by soldering bare wires to the gold-plated frames, and probe station setup, by landing the probing tips on the frames. All the components, except the SiC Schottky diodes and LED varactor, have been attached

to the respective cavities using the 940HT ceramic epoxy, similar to the assembly method for the RUK modules. The diode and the varactor component have been attached to the module with the sintered silver epoxy. The Schottky diodes forming the bridge rectifier circuit section have not been tested on this module. The Fraunhofer module-2, as shown in Fig. 52 (bottom), has been assembled with another set of SiC Schottky diodes to check the operability of the rectifier circuit. The fully assembled (including the bridge rectifier and the power receive coil) second Fraunhofer module is shown in Fig. 55. The figure shows the inductor coil constructed on the module connected with the 1 nF capacitor to form the resonant circuit, along with the 0.75 cm thick power transmission coil. The coil is made with a 0.4 mm (26 AWG) diameter nickel wire. The inductance value on the coil, measured with an LCR meter, is 150 nH. As mentioned earlier, the lower thickness wire selection is due to the module area constraint; the trade-off of using such thinner wire is the high series resistance (1 Ω for this 0.4 mm wire coil). The two ends of the coil are attached to the extended gold trace on the sixteenth LTCC layer with silver epoxy and 95/5 Pb-Sn solder. For an actual application like the gas turbine blade, additional ceramic epoxy has to be used on top of the inductor coil to hold the wire in place from extreme pressure or G-force.

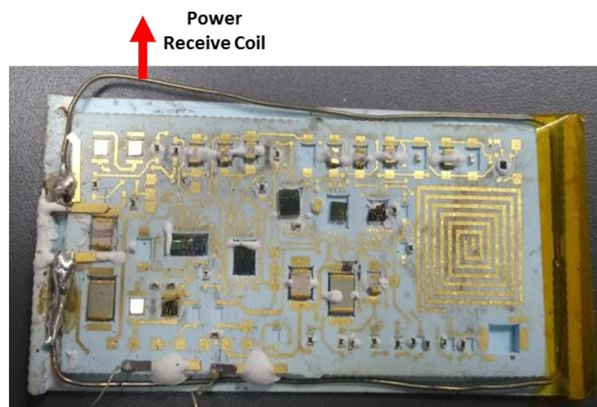


Fig. 55. Fraunhofer module-2 after assembly of the components and the power receiver coil to test/validate the full-bridge rectifier and wireless power transfer method.

The complete assembled Fraunhofer module-3 is shown in Fig. 56. It can be noticed from Fig. 56 that the traces on the top of the cavity for the Schottky diodes are missing as the cavity for the Schottky diodes in this module-3 punches through an extra LTCC layer that provides the surface for the third conductor layer. In regards to the missing trace, the diodes are placed on the first conductor layer traces. As module-3 includes stand-off, placing the diode components on the top surface of the module (where the first conductor traces are located) will not cause any damage to the wirebonds.

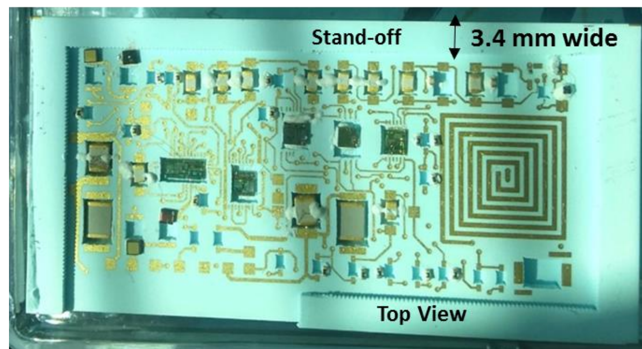


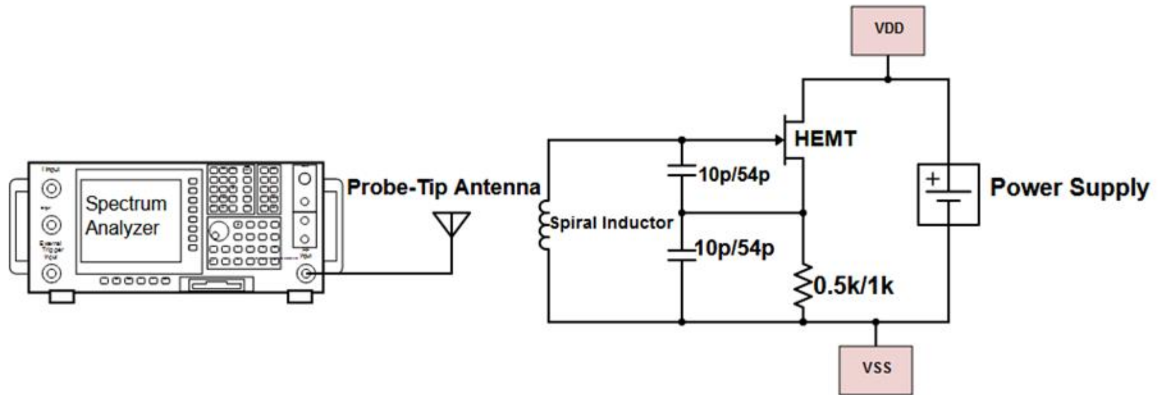
Fig. 56. Fraunhofer module-3 with stand-off layer and receive coil on the back of the module.

Chapter 5. LTCC Module Test Results

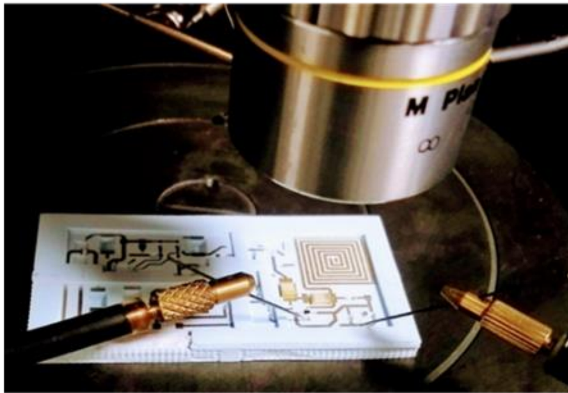
5.1. Colpitts Oscillator Testing on the RUK and Fraunhofer Modules

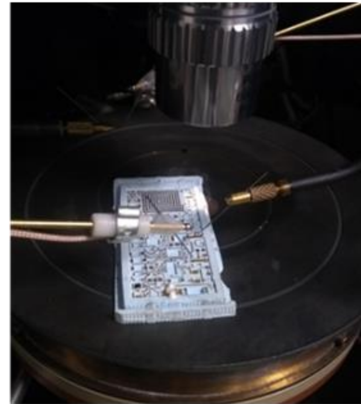
The first phase of testing on both the RUK and Fraunhofer modules involved the functionality and high-temperature testing of the Colpitts oscillator section using the unwanted modules – RUK module-1 (Fig. 44) and initial Fraunhofer module (Fig. 50). The Colpitts oscillator on the RUK module-1 is implemented with a tank capacitance value of 54 pF to achieve an oscillating output in the range of 30 to 40 MHz. The Colpitts oscillator on the Fraunhofer module was implemented with a 10 pF tank capacitance to achieve an oscillating frequency of 75 to 85 MHz. The Colpitts oscillator on both modules has been tested on the Signatone™ probe station, equipped with a thermal chuck capable of reaching 500°C temperature. The schematic for the test setup configuration of the Colpitts oscillator is shown in Fig. *57* (a). Fig. *57* (b) shows the probe station setup images for both the modules. Two probe arms with manipulators were connected to the module's VDD and VSS pads (Fig. *45*) to power the Colpitts oscillator circuit. The VDD and VSS probe connections were coming from an external power supply. Both the modules only include the assembly of the Colpitts oscillator during the testing. The transmitted signal from the oscillator's spiral inductor is detected on a spectrum analyzer through a coaxial cable antenna connected to a banana jumper plug, as shown in Fig. 58. The complete signal conditioning system on the RUK module is intended to operate within the supply range of 9 V to 12 V and on the Fraunhofer module, between 12 V to 15 V. Thus, both the oscillators are initially tested with the supply voltage of 12 V. The source resistances on the RUK and Fraunhofer module oscillators are set at 1 kΩ and 0.5 kΩ, respectively, for this test. With a noise floor at -105 dBm, the spectrum analyzer showed a peak (-17.4 dBm) at the center frequency of 80.31 MHz, as shown in Fig. 59,

for the Colpitts oscillator on the Fraunhofer module. In the RUK module, the peak (-45 dBm) has been observed at the center frequency of 34.94 MHz, as shown in Fig. 60.



(a)





(b)

Fig. 57. (a) Test setup configuration schematic for the Colpitts oscillator testing on the modules, (b) Probe station setup for testing the Colpitts oscillator both the RUK and Fraunhofer modules at 500°C.

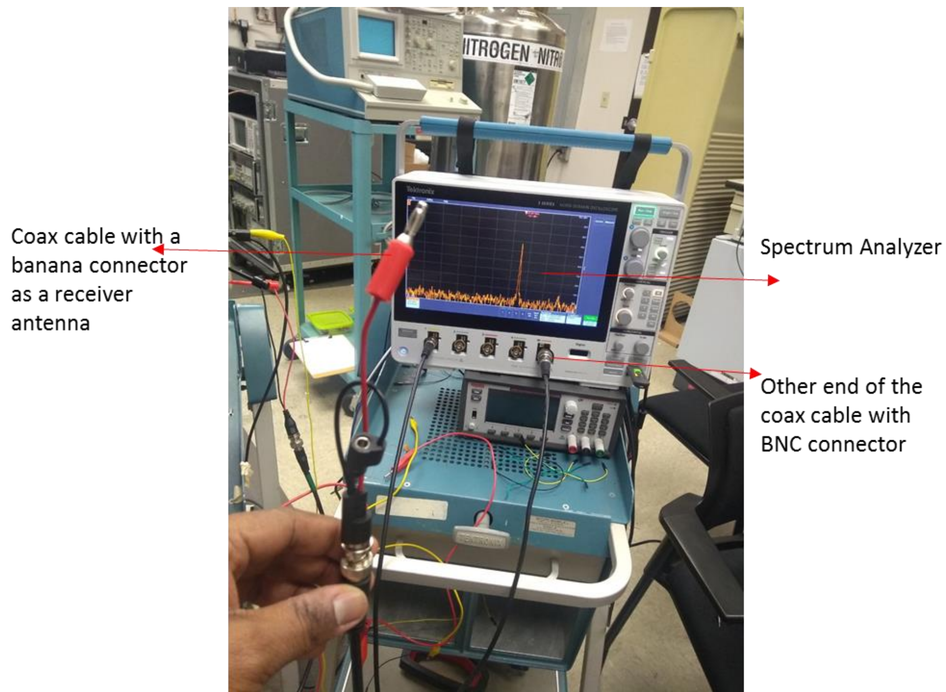


Fig. 58. A banana connector hooked to a coaxial cable with BNC termination acting as an antenna to receive the transmitted signal from the Colpitts oscillator.

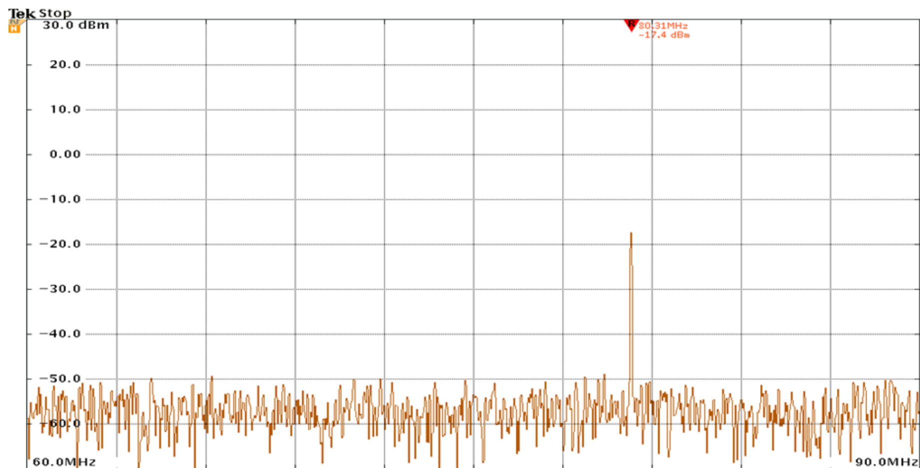


Fig. 59. Colpitts oscillator (Fraunhofer module) output signal centered at 80.31 MHZ detected on the spectrum analyzer.

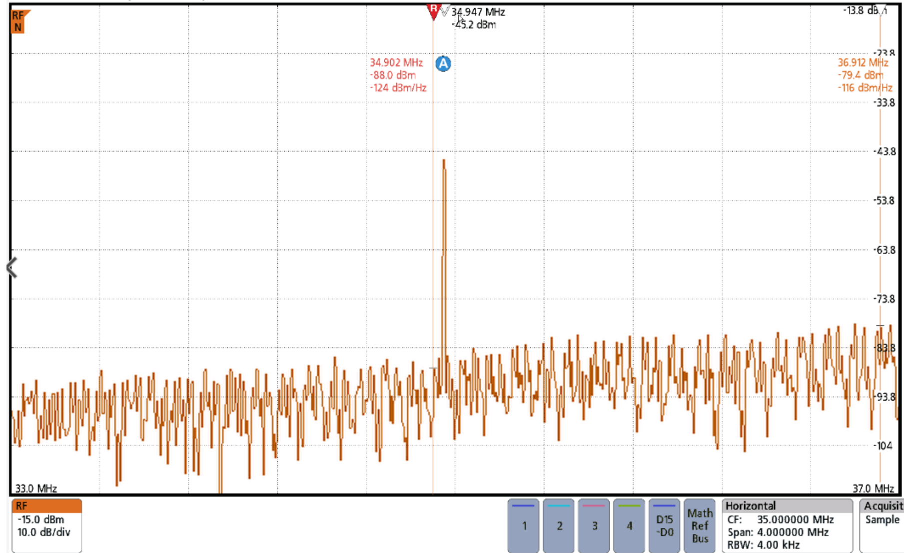


Fig. 60. Colpitts oscillator (RUK module) output signal centered at 34.94 MHz detected on the spectrum analyzer.

The signal strength or peak on the spectrum analyzer can be improved if the antenna is designed to match the oscillating frequency. However, the test's goal is to check if the oscillator's signal is strong enough to be detected. As the module is intended to operate at extreme temperatures, the oscillator has also been tested at 500°C to check the center frequency deviation. It is to be noted that this test was carried out prior to the complete assembly of the modules. Hence, the LED varactor component was not assembled during this test. The varactor is attached to the module with sintered silver epoxy with a temperature rating of 343°C. The thermal chuck on the probe station provided the high temperature. At 500°C (as measured from the probe station's thermal controller), the spectrum analyzer output is shown in Fig. 61. The signal peak (-29.2 dBm) is now observed at 81.03 MHz. The degradation of the signal strength is due to the high spiral inductor's parasitic resistance at higher temperatures. The center frequency varied by less than 1% over temperature, which is noteworthy. The current consumption increased from 18 mA to 22 mA during this test, which is high and can be detrimental at prolonged high-temperature operations. However, it is due to the low source resistance value used for this test. The source resistance in the

final assembled modules is set to 2.5 kΩ resulting in much lower current consumption for the overall system.

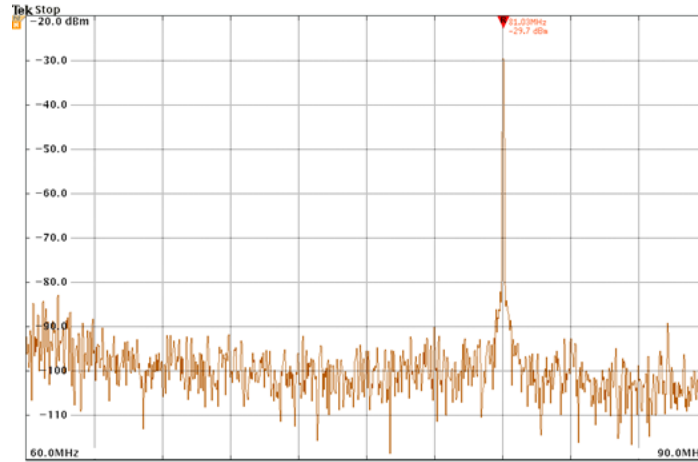
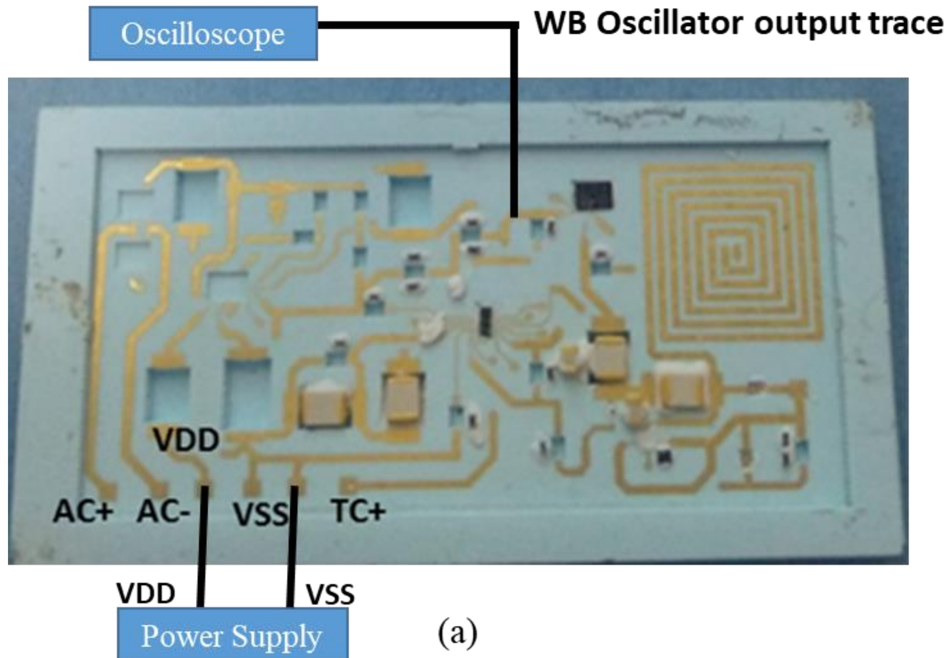


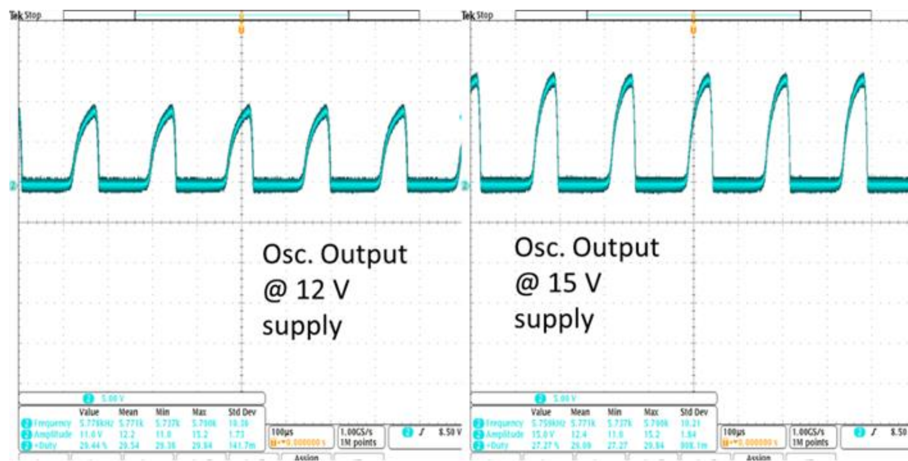
Fig. 61. Colpitts oscillator output signal detected on a spectrum analyzer at 500°C.

5.2. RUK Module Individual Blocks and System Testing

With the Colpitts oscillator setup verified, the other blocks on the signal conditioning system are to be tested to confirm operability. The assembled modules in Fig. *45* were used to test the system functionality on the probe station. Four probe arms with manipulators were required to carry out the testing. Fig. 62 (a) shows the test setup configuration for detecting the Wien-bridge oscillator output from the RUK module. Fig. 62 (b) shows the Wien-Bridge (WB) oscillator's output waveform at 12 V and 15 V supply voltage (applied to the VDD pad on the module) on an oscilloscope. The WB oscillator output is saturated due to the high closed-loop gain (5) set on the WB op amp. It can be noticed the output frequency of the oscillator does not shift at a supply voltage above 12 V. However, as the RUK module is intended to operate at high temperatures, it is also expected for the WB oscillator output frequency to not fluctuate significantly over temperature. Table XIII shows the WB oscillator output frequency variation over supply voltage and temperature. The output frequency at 25°C is close to the simulated frequency.



(a)



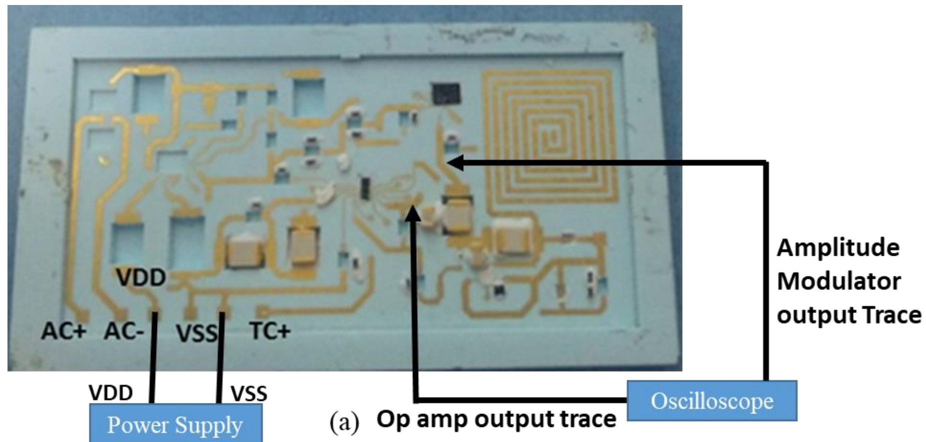
(b)

Fig. 62. (a) Test setup to detect the Wien-Bridge oscillator output on the RUK module, (b) Wien-bridge (WB) oscillator output.

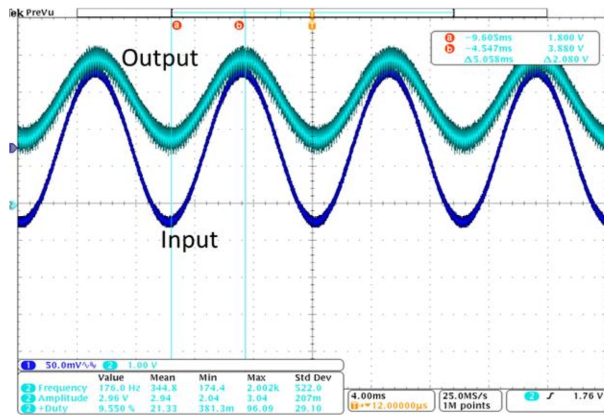
Table XIII. WB Oscillator Output Across Temperature and Supply Voltage

Supply Voltage (V)	$F_{WB\text{-}OSC}$ @ 25°C (kHz)	$F_{WB\text{-}OSC}$ @ 350°C (kHz)
9	5.13	5.65
10	5.46	5.7
11	5.71	5.73
12	5.78	5.75

The test setup configuration to detect the signal conditioning op amp and amplitude modulator output is shown in Fig. 63 (a). The signal conditioning op amp in a closed-loop configuration is tested with a 100 Hz, 200 $mV_{Pk\text{-}Pk}$ sinusoidal signal. This sinusoidal signal is applied on the non-inverting node (the TC+ pad on the module) of the op amp from the function generator. The resulting output waveform is shown in Fig. 63 (b), with an output peak-to-peak value of 2.08 V. The DC level of the op amp, however, was set to 2.8 V (higher than the simulated value), which is due to the selected op amp die showing an offset of 1 V on the non-inverting node (TC+). As a result, -1 V was superimposed on the 200 mV sinusoidal signal at the TC+ node. The op amp bias current was also lower (60 μA) than the simulated value of (98 μA). The op amp output connects to the amplitude modulator transistor in the source follower configuration, whose output waveform is shown in Fig. 64. The amplitude modulator is correctly tracking the op amp output waveform shown in Fig. 63 (b). The amplitude modulator output varies the LED varactor capacitance resulting in a frequency modulated output to be transmitted from the Colpitts oscillator, which can be observed on the spectrum analyzer, as shown in Fig. 65, indicating two peaks. It is to be noted that the gap between the two peaks will increase if the amplitude of the input signal on the signal conditioning op amp increases. The frequency modulated signal detected using the same setup used for detecting the Colpitts oscillator output, as shown in Fig. 58.



(a)



(b)

Fig. 63. (a) Test setup to detect the op amp and amplitude modulator output on the RUK module, (b) RUK SiC op amp output for a sinusoidal input on the RUK module.

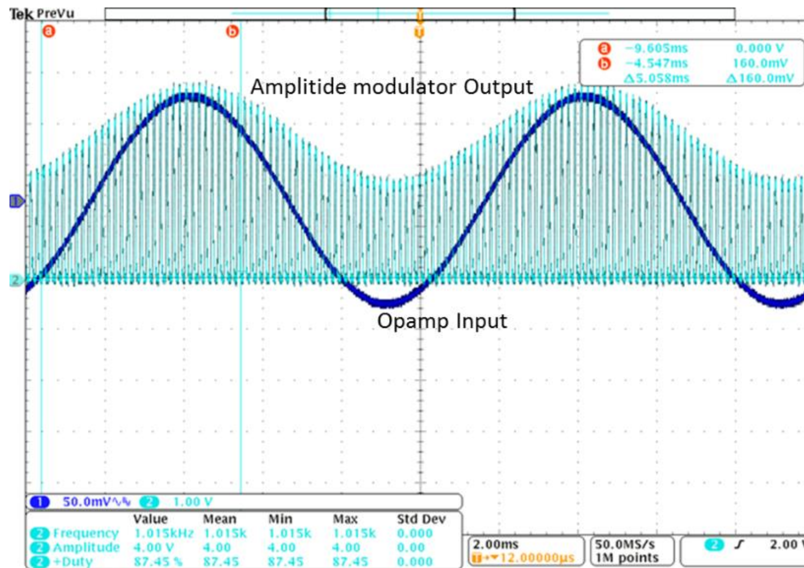


Fig. 64. Amplitude modulator output on the RUK module.

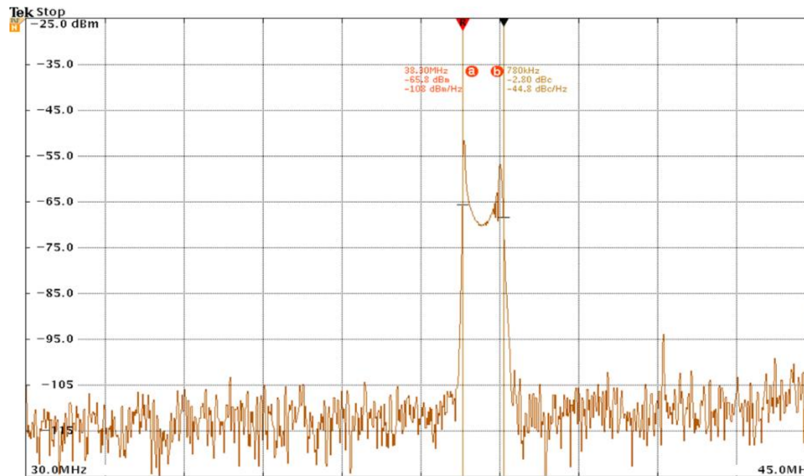


Fig. 65. Frequency modulated signal from the RUK module detected on the spectrum analyzer.

5.3. Receiver Set-up for Signal Detection from the LTCC Modules

With the signal conditioning system functioning as expected, it is necessary to map the transmitted frequency modulated output to the variation in the amplitude on the input node of the signal conditioning op amp. As the op amp input will be coming from a sensor within an extreme environment, it is mandatory to have the receiver system demodulate the transmitted signal. To realize the receiver, a highly-sensitive telemetry receiver system (Appendix-4) with a tuning range of 63 MHz to 78 MHz and a bandwidth of 75 kHz has been selected. However, the RUK module transmits at a center frequency of 34.94 MHz, so to shift the transmission frequency from the RUK module to the tuning range of the receiver, a down converter has been designed using a commercial mixer and VCO. The bench-top setup of the receiver system is shown in Fig. 66. The mixer circuit with the VCO shifts the received signal frequency from the module to the intermediate frequency (IF), which falls in the tuning range of the receiver. The VCO requires a 10 V supply voltage (VDD) and 12 V of tuning voltage (VT) to produce a 101.6 MHz oscillating signal at its output. The receiver module was tuned at the intermediate frequency of 66.7 MHz. Fig. 67 shows the front side of the receiver tuned at the IF-frequency. The receiver module has a tuning knob that allows

for manual adjustment to the IF frequency with an RF level indicator showing the strength of the received signal.

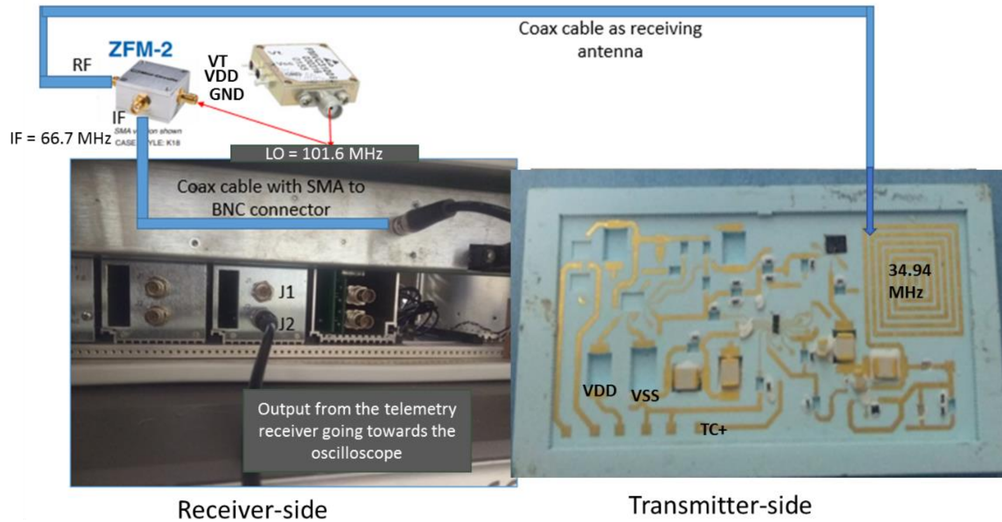
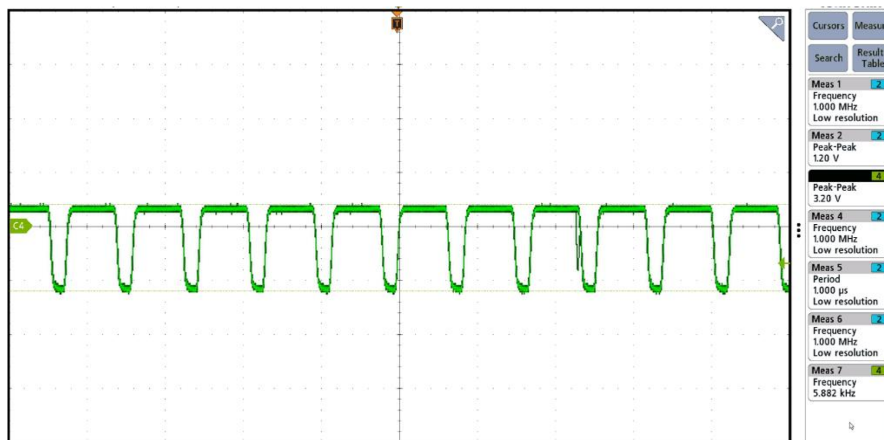


Fig. 66. Bench-top setup of the receiver module to demodulate the FM signal from the RUK module.

Fig. 67. Front-side view of the receiver unit locked at the intermediate frequency (IF).

The output from the telemetry receiver can be observed on the oscilloscope. The signal frequency from the telemetry receiver output should match the frequency of the WB oscillator. To verify the receiver system functionality, a low DC voltage of 100 mV has been applied to the signal conditioning op amp input at a supply voltage of 12 V. The low DC voltage resembles the output

of a thermocouple sensor, which produces an EMF voltage that is fairly DC in nature. Fig. *68* (top) shows the telemetry receiver's output waveform for 100 mV DC input signal on the signal conditioning op amp. The demodulated signal has an amplitude of 3.2 V with a frequency of 5.88 kHz, close to the WB output frequency. As the op amp input signal value is increased (from 100 mV to 150 mV), it can be noticed that the amplitude of the signal from the telemetry receiver also increases (to 4.48 V), as shown in Fig. 68. Demodulated output from the receiver unit (top) for 100 mV input to the RUK SiC op amp and (bottom) 150 mV input to the RUK SiC op amp. (bottom) for an input DC signal of 150 mV. Therefore, the corresponding change in 50 mV of the input signal results in 1.28 V of change in the demodulated output, producing a mapping scale with a ratio of around 1:26. This is beneficial as the voltage level change on the sensed signal that is connected to the transmitter side can now be mapped to the voltage level change on the receiver side.



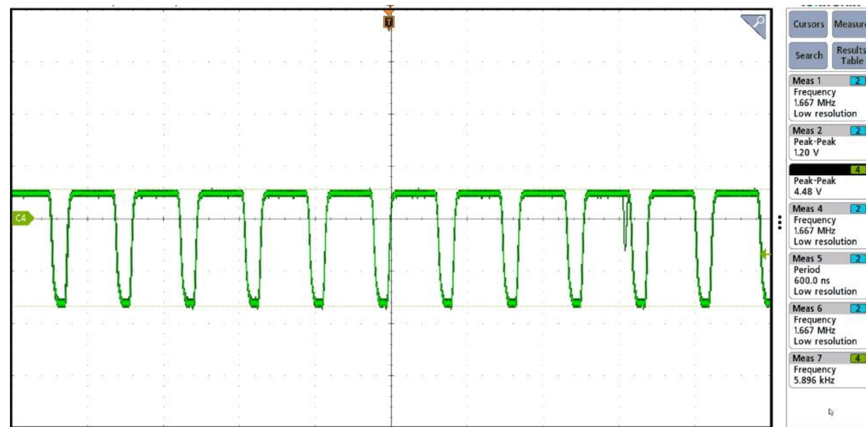


Fig. 68. Demodulated output from the receiver unit (top) for 100 mV input to the RUK SiC op amp and (bottom) 150 mV input to the RUK SiC op amp.

There is a downside to this receiver system due to its limited bandwidth of 150 kHz. With the op amp input DC signal increasing greater than 150 mV, the receiver output will distort as the FM modulator's frequency deviation increases due to an increased shift in the varactor capacitance. At 200 mV DC input to the signal conditioning op amp, the resulting distorted output from the receiver equipment can be seen in Fig. 69. Observed distortion of the demodulated output for 200 mV applied input to the RUK SiC op amp. Such distortion is difficult to comprehend as accurately received signal amplitude cannot be attained.

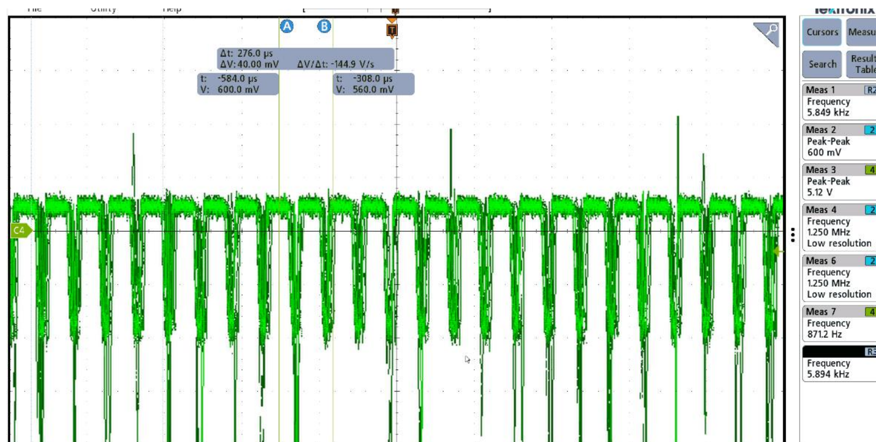


Fig. 69. Observed distortion of the demodulated output for 200 mV applied input to the RUK SiC op amp.

To further illustrate the distortion issue, the Colpitts oscillator equations in Chapter 4 can be used to derive that a 10 pF change in capacitance on the varactor would cause the center frequency of the oscillator to shift by 104 kHz, which exceeds the bandwidth of the receiver. To address the problem associated with distortion, a few modifications can involve lowering the gain of the signal conditioning op amp (currently set at 11) or lowering the source resistance of the amplitude modulator. Another option is to use a real-time spectrum analyzer with demodulating feature to allow direct retrieval of modulating signal without distortion.

With this receiver setup, the RUK module shown in Fig. 45 has been subjected to high temperatures up to 350°C on a probe station. The input DC signal to the op amp and the supply voltage have been kept constant at 50 mV and 9 V, respectively, for the testing to avoid any distortion issue. The resulting received signal frequency at 25°C and 350°C is 5.89 kHz and 6.12 kHz, with the signal amplitude varying between 2.48 V to 2.88 V. The module has been tested at 350°C with the 12 V supply and 100 mV to the op amp input. The signal amplitude increased to 3.55 V at 350°C compared to 3.2 V at 25°C. This variation can be traced to the transmitter side, where the decrease in the channel resistance at higher temperatures of the SiC transistor used in the amplitude modulator would increase the voltage drop across the source resistance of the amplitude modulator. This will change the modulator output and inadvertently change the varactor capacitance, causing the amplitude of the demodulated output from the receiver to increase. The variation in the amplitude over room temperature to 350°C is 400 mV. Using the earlier mapping scale of 1:26 for the transmitter-to-receiver side, the 400 mV change on the receiver side would correspond to around 15 mV of change in the sensed signal on the transmitter side. This would mean that during sensing application, any small change detected by the sensor (for example – a thermocouple sensing the slight temperature change of a gas turbine blade) will not be accurately

translated at the receiver side if the respective sensed signal varies within 15 mV from its previous sensed value. However, significant change within the sensor (for example – the thermocouple sensing the large change in temperature of a gas turbine blade) can be translated at the receiver end.

5.4. Spin Testing on the RUK Module

Earlier sections have mentioned gas turbine blades as one of the desired extreme environment applications for inserting the SiC modules. In applications like gas turbines, the modules are expected to experience high centrifugal force or G-Force, as the turbine blades rotate at very high speed. To verify the SiC module's applicability in such an environment, spin-testing at a rotational speed above 10,000 rpm has been carried out on the RUK module with the CMC housing enclosure. The assembly of the CMC housing enclosure with the module has been described in Chapter 4. The goals of the spin testing are to check the following attributes within the module:

1. Gold wirebond durability under the high-G force
2. SiC die functionality under stress at high rotational speeds
3. RF or signal transmission at high G-force or rotational speeds
4. The durability of the die attachment and wire assembly epoxies at high-G

A specialized spin rig has been utilized at the Aerodyn Engineering facility in Indiana to perform the spin test. The spin rig has the capability of reaching 14,000 revolutions per minute (rpm). The rig is equipped with the slip-ring feature to allow external wire feedthrough to the module under spin test and a rotating disk to mount the module. The spin-rig can also be fitted with a heater to provide the temperature. However, the RUK module and the SiC circuits on the module have already been tested at high-temperature. Besides, incorporating the heater into the spin rig would

require the cabling assembly on the module and the slip-ring system to change. Thereby, to avoid further complexity, only the spin-testing at high-G force is carried out.

The spin test is performed on the first iteration of RUK module-2. The module-2, shown in Fig. 47 (right), included the complete system. However, the module failed to pass the functionality testing in terms of signal transmission and frequency modulation during spin testing. The Colpitts oscillator was unable to function and transmit any signal. However, the signal conditioning op amp and the WB oscillator still operated. Due to the transmitter section not working, spin testing on this module is only performed to check the wirebond and module's durability at high-G force. The spin test rig image with the CMC housing (with the module) mounted on the frame is shown in Fig. 70. The frame holding the CMC housing is attached to the spin/rotating disk with Hexa-screws that are pasted with Loctite™ prior to tightening. This protects the threads on the hex screws from damage during high-speed rotations. A 20 foot-long bare wire (green color), serving as the receiving antenna, is fixed and placed 2 inches from the module. There is a counterweight bracket placed opposite to the CMC housing to balance the load on the spin disk during rotation. The radius from the spin disk center to the end of the CMC housing is 4.8 inches. This is important to calculate the G-force value from the applied RPM value.

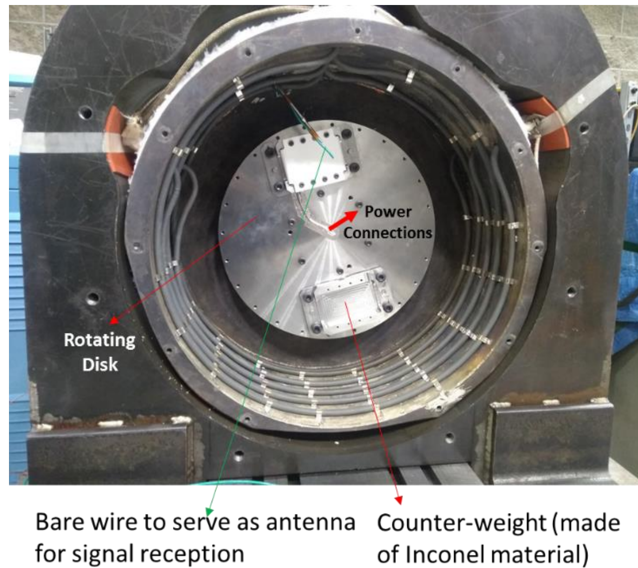


Fig. 70. Spin-rig setup with the CMC housing (RUK module inside) mounted on the bracket attached to the spinning disk.

The spin disk is rotated up to 10,124 rpm, which is around 14,000 G-force. After the spin-test, the CMC housing remains intact. However, multiple cracks have been observed on the tested RUK module-2, as shown in the images in Fig. 71. The cause behind the cracks is due to the module's non-uniform placement on the CMC housing and the mounting frame, resulting in non-uniform stress on the edges of the module spinning.

Fig. 71. Visible cracks on the RUK module post-spin-testing.

In addition to the cracks, two wirebond tears have also been observed, as shown in Fig. 72. However, no visible wirebond tears have been observed on any of the SiC or GaN die components.

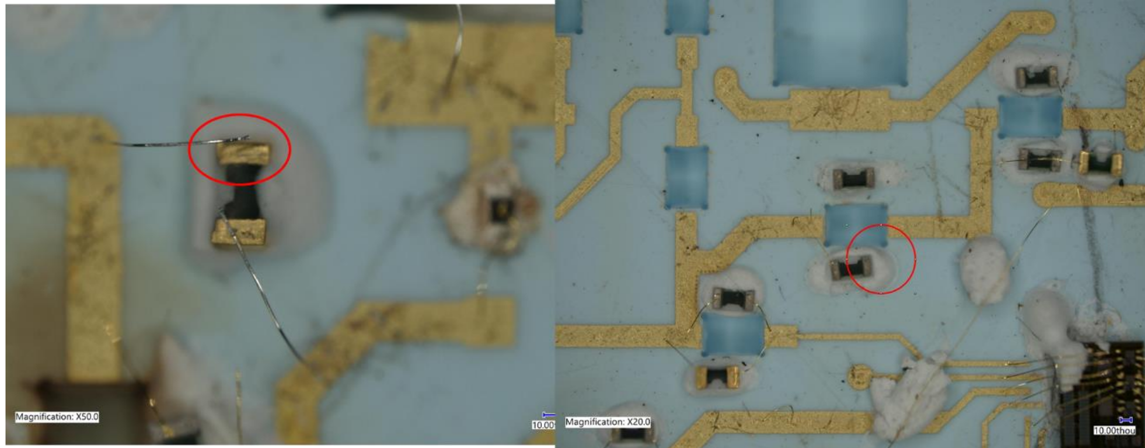


Fig. 72. Visible wirebond tear on the RUK module post-spin-testing.

The observations from the spin testing of module-2 resulted in the quick assembly of another module (#3). The newly assembled module-3 includes the amplitude modulator and frequency modulator circuits. The signal conditioning op amp is not added in this second spin-testing module as the signal modulation, and signal transmission (with frequency modulation) circuits are the key features to test under the spin-testing environment. To replicate frequency modulation on the module using the varactor device, the AM modulator's transistor drain node (check the M1 transistor in Fig. 37) connection is modified. Instead of connecting to the signal conditioning op amp output, which is not wirebonded on the new module-3 (Fig. 73), the drain node is now fed from a resistor divider network (10:1 ratio) that itself is derived from the supply voltage. This would mean at 8 V and 9 V supply, the AM modulator's transistor drain node would see 0.72 V and 0.81 V. The amplitude of the output from the AM modulator would change as the voltage on the drain node changes. This variation replicates the change in the signal conditioning op amp output. With the amplitude of the AM modulator changing, the varactor device capacitance would vary, resulting in the transmission of the FM modulated signal to work.The module-3 requires three wire connections (VDD, VSS and TC+) that are fed to the module through slip-rings. The image of the assembled RUK module-3, along with the block diagram of the setup for the slip-ring

connectivity to test the module inside the spin-rig is shown in Fig. 73. To avoid system failure due to wirebond tear, two wirebonds have been made for the passive component terminal/node. It can be seen that only two wires (VDD and VSS) are used due to the signal conditioning op amp not wirebonded out. The wire assembly is performed in the same way as described in Chapter 4.

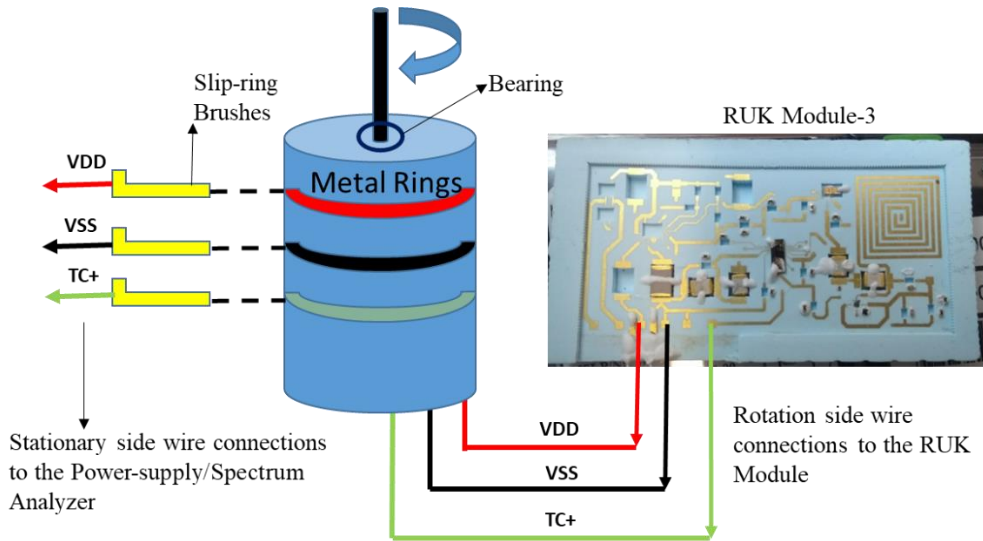


Fig. 73. Assembled RUK module-3 for the second spin-testing with block diagram of the slip-ring setup.

The module-3 is carefully placed on the CMC housing enclosure first, and then the CMC housing is taped over not to allow the module to move within the housing structure. Later, the CMC housing is gently placed on the mounting frame to be finally fitted on the spin disk, as shown in Fig. 74.

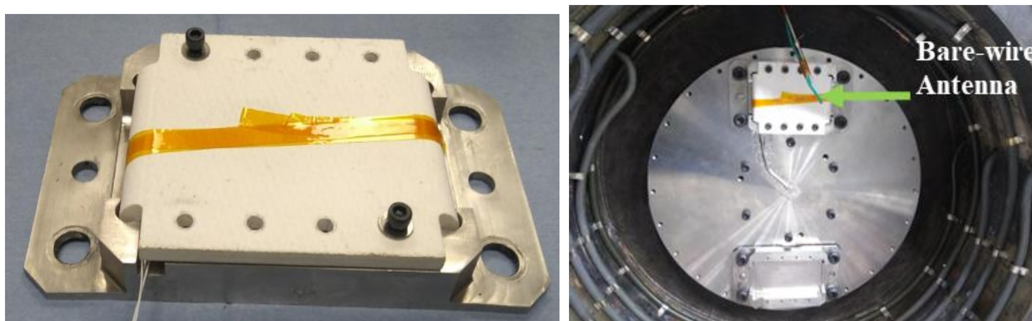


Fig. 74. (Left) Bracket mounting of the new RUK module within the CMC housing for second spin testing, (right) bracket with the CMC housing attached to the spin disk.

The bare wire antenna is connected to the spectrum analyzer (Fig. 74) to detect the receiving modulated signal. The supply wires from the slip ring are connected to the three-channel DC power supply.

The module-3 operated and transmitted the signal through the spin test at the maximum rotation speed of 10,920 rpm, around 16,000 G-force. Further speed has not been attempted due to the spin rig system reaching its critical vibration limit of 5 inch/s. The overall spin test lasted two and half hours. The spectrum analyzer output at 6 V supply is captured at the beginning of the spin test and at the 10,920 rpm speed. At 6 V supply voltage, only the Colpitts oscillator circuit will operate. The resulting waveforms are shown in Fig. 75. The peak signal strength remained the same at -45.2 dBm (at a noise floor of -90 dBm), with the peak signal frequency barely shifted by 0.29 MHz.

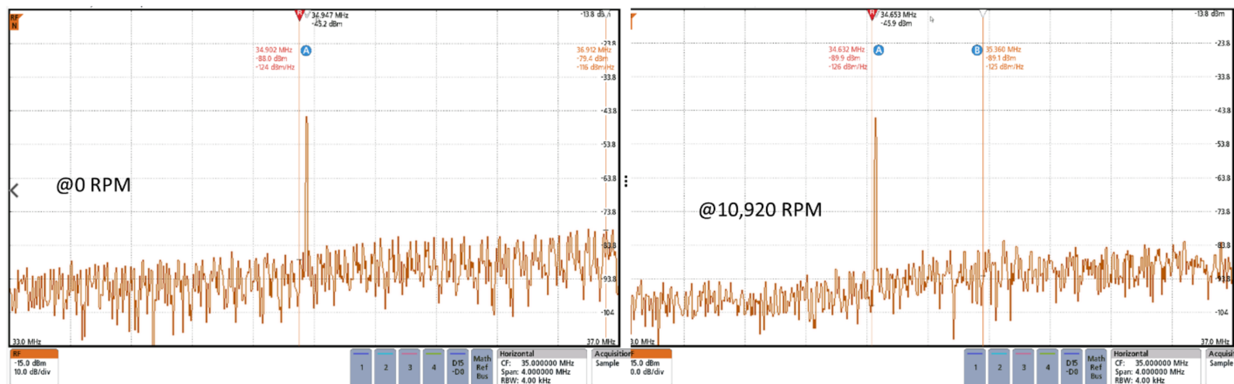


Fig. 75. Spectrum analyzer output detecting the Colpitts oscillator signal at – (left) 0 rpm, (right) 10,920 rpm.

As the supply voltage increased to 7 V, the WB oscillator and the AM modulator circuit started functioning. The resulting output waveforms from the spectrum analyzer at different rotational speeds, with supply voltage set at 7 V, are shown in Fig. 76. All the resulting waveforms show two peaks, indicating that the frequency modulation scheme is functioning on the module. The gap between the two peaks does not offer a significant change (varies between 0.38 MHz to 0.46 MHz).

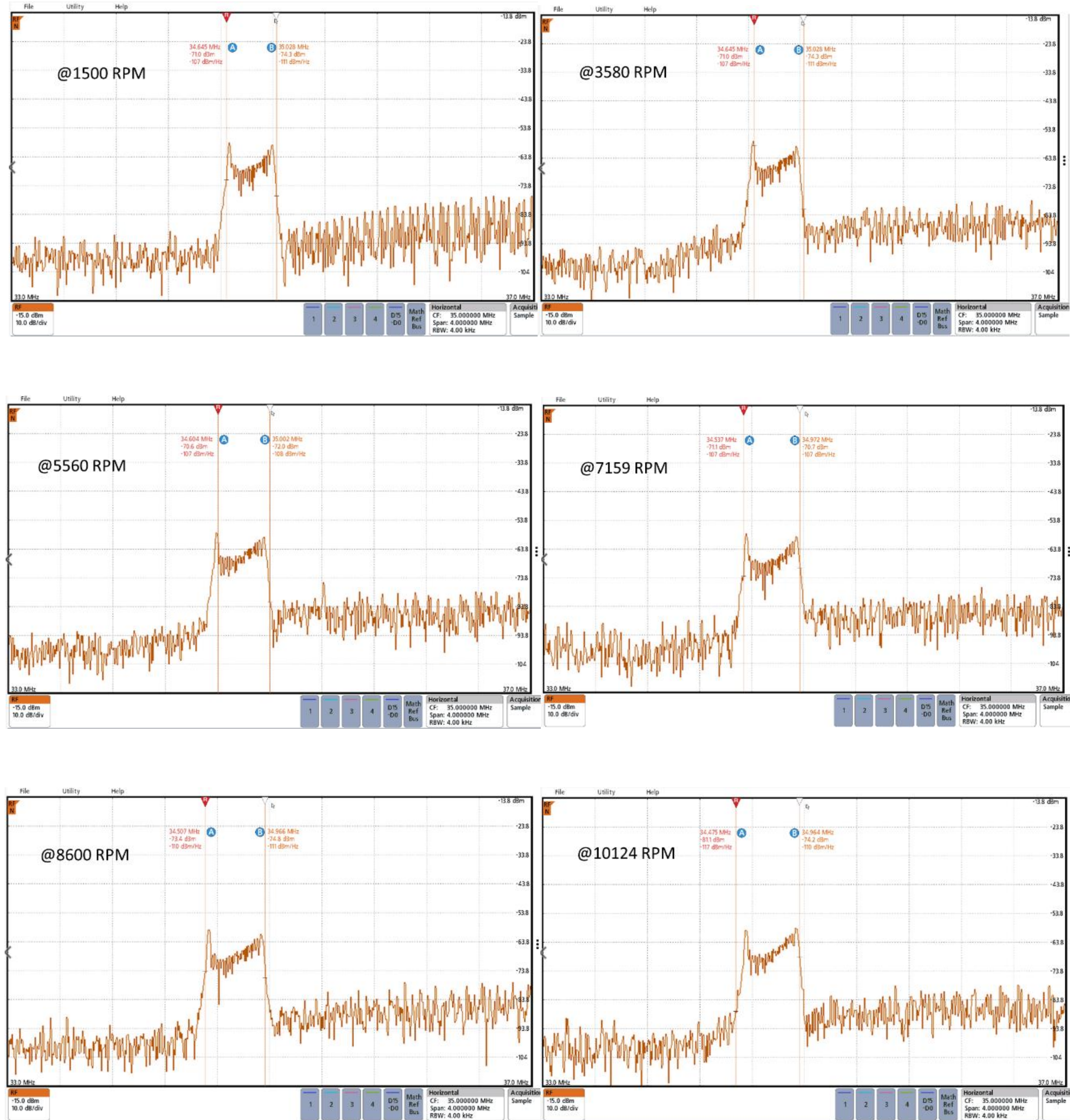


Fig. 76. Spectrum analyzer detection the FM signal from the RUK module at VDD = 7 V.

As the supply voltage increases to 9 V, the gap between the peaks would increase as the amplitude of the AM modulator output would also increase. This would eventually change the varactor capacitance (see section 5.2) and widen the gap between the two peaks. The spectrum analyzer waveforms for 0.72 V and 0.81 V swing for the amplitude modulator under the rotational speed of 10,920 rpm are shown in Fig. 77. The gap between the peaks increased to 0.673 MHz at 8 V and 0.955 MHz at 9 V.

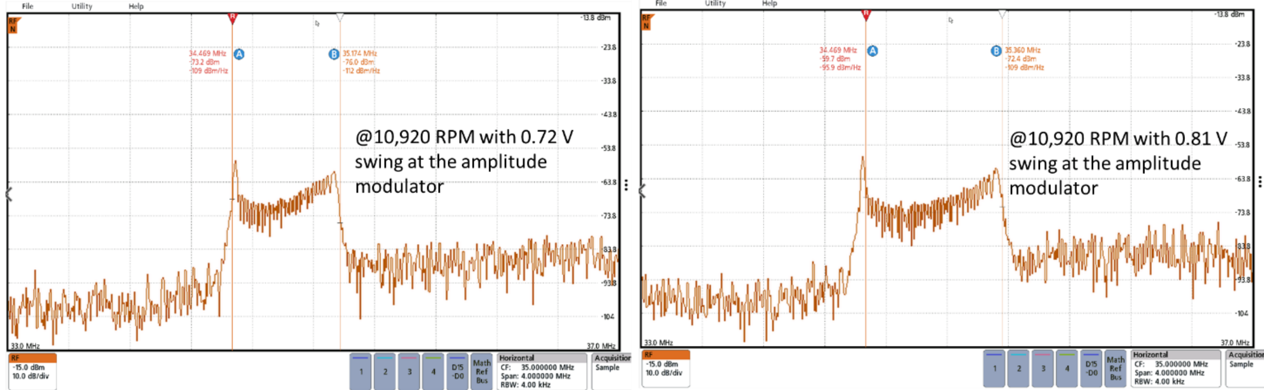
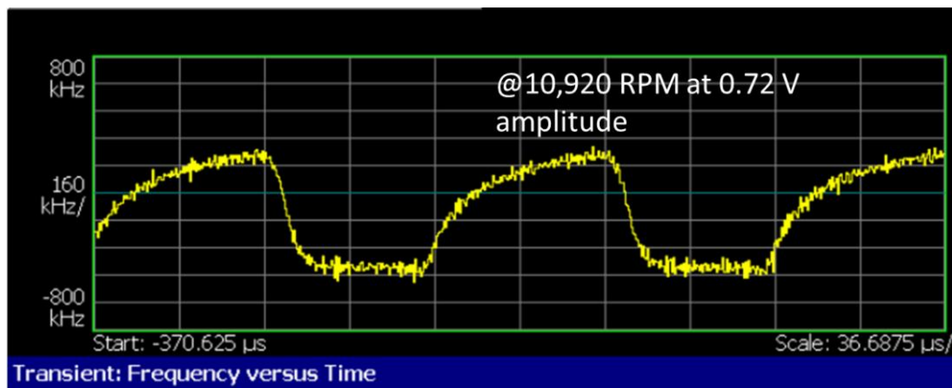


Fig. 77. Spectrum analyzer output showing a variation on the detecting FM signal due to the change in the swing of the amplitude modulator output.

This corresponding change can be clearly noticed through the use of a real-time spectrum analyzer (Appendix-4) where frequency vs. time waveform can be plotted. Fig. 78 shows the real-time SA frequency vs. time output waveforms for the 0.72 V and 0.81 V amplitude on the AM output at 10,920 rotational speed. The change in the amplitude of the AM output amplitude is represented in terms of the deviation in the frequency of the received signal. The peak frequency at 0.72 V and 0.81 V amplitude are 720 kHz and 880 kHz, respectively. Therefore (0.81- 0.72) 90 mV of change in amplitude corresponds to (880 – 720) 160 kHz of frequency deviation. Both the results from the standard-SA and the real-time SA confirm the WB and the Colpitts oscillator, along with the Raytheon op amp and transistor device, can sustain and transmit FM signal at 10,920 rpm.



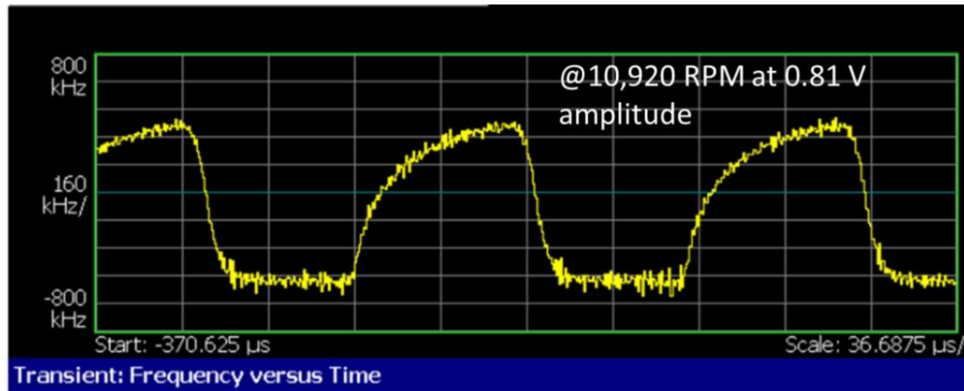


Fig. 78. Real-time spectrum analyzer detecting RUK module output during the spin test, showing the frequency vs. time plot for - 0.72 V amplitude and 0.81 amplitude from the AM circuit.

After the spin-test, the RUK module-3 was unmounted from the mounting bracket and inspected to observe any wirebond tear or noticeable crack. Fig. 79 shows the two sections on the module where a single wirebond detached from the passive parts' pads. The detached wirebond did not affect the system functionality as additional wirebond on the pads are still intact in both cases.

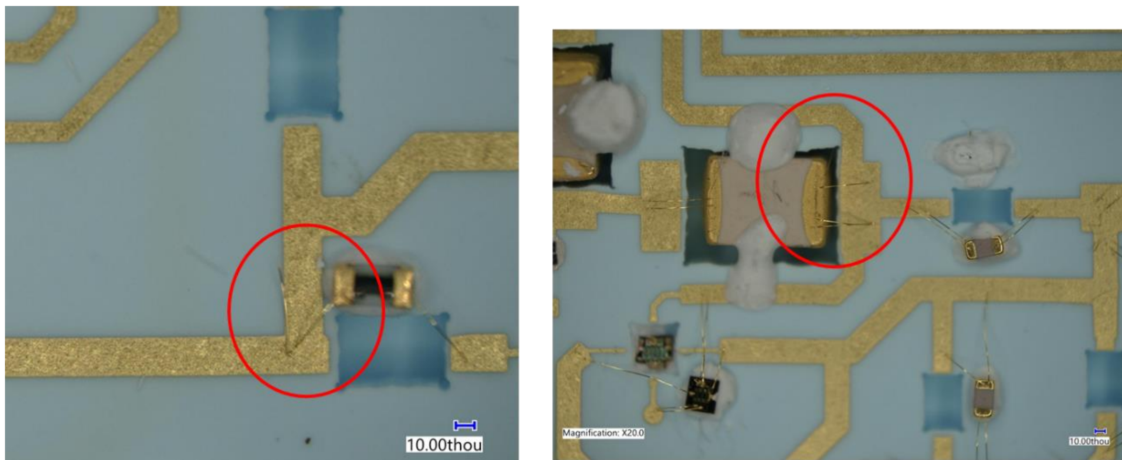


Fig. 79. Visible wirebond tear (non-critical) on the RUK module used for second spin testing.

The module-3, therefore, successfully operated at a speed of 10,920 rpm. However, it has to be noted that the actual application will include the ambient temperature to be 350°C and above with the high rotational speed. To account for the high temperature aspect and also to test the complete system at high temperature, the wire assembly on module-3 is modified, and the signal conditioning op amp has been wirebonded out. In regards to high temperature wire assembly,

instead of using tinned-copper wire, bare nickel-clad-copper (NCC) wires that are rated for 580°C are used to attach to the gold pads on the module. The bare NCC wires (with any insulation jacketing) cannot directly come out of the CMC housing; hence additional jacketed wiring is required to make the connection between the bare NCC wires and the slip-ring wiring. The wiring assembly for both temperature and spin-testing can be seen in Fig. 80. The bare wires on the module gold pads are NCC material, and the jacketed wires coming out of the CMC housing are K-type thermocouple wires. It is to be noted that the thermocouple wires have three times the resistance (for the same length) compare to the NCC wires; therefore, it is important to run the overall signal conditioning system at 9 V supply to reduce power consumption at higher temperatures.

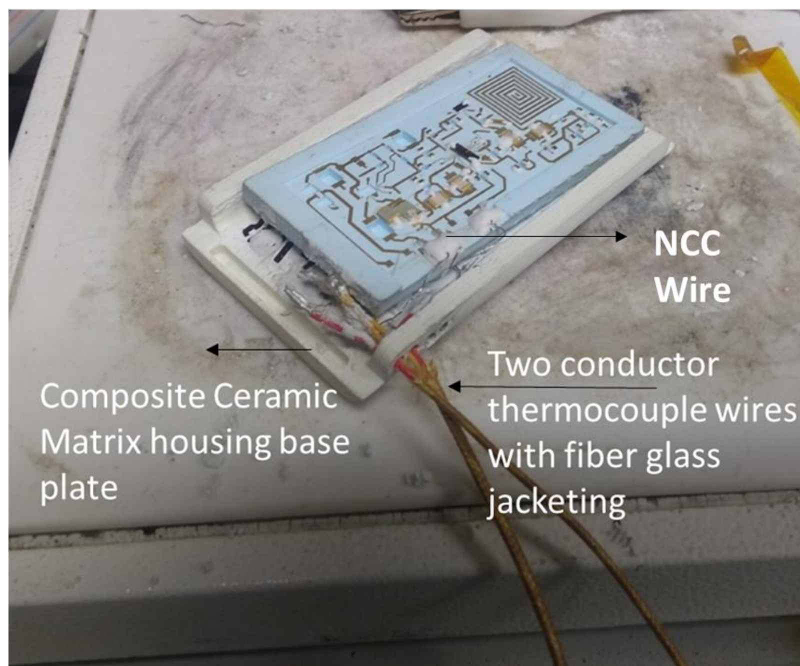


Fig. 80. Wire assembly on RUK module-3 for both temperature and spin-testing.

5.5. High-Testing of the RUK Module

The newly assembled RUK module-3 with high-temperature wiring, shown in Fig. 80, has been tested at 440°C on a thermal chuck of a probe-station. To accommodate temperature testing above 350°C, a new silver epoxy paste (Appendix-2), rated for 927°C, is used to attach a new InGaN varactor diode on the module. The applied supply voltage is 9 V, and the overall current consumption for the system equaled 6 mA. The transmitted signal is detected on a real-time spectrum analyzer using a probe-tip, terminated with BNC connector cable, as the receiver antenna. The input to the sensor amplifier (TC+) on the module is provided from the function generator. A 50 mV and 100 mV DC voltage are applied from the function generator with the output impedance set to 'High-Z'. The results from the high-temperature testing on module-3 are shown in Fig. 81 and Fig. 82.

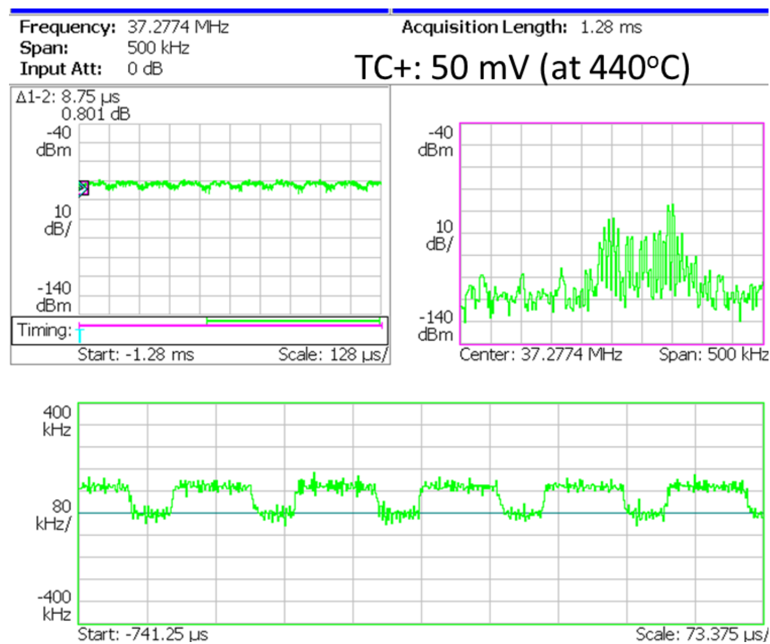


Fig. 81. RUK module-3 output at 440°C for 50 mV DC input to the sensor amplifier.

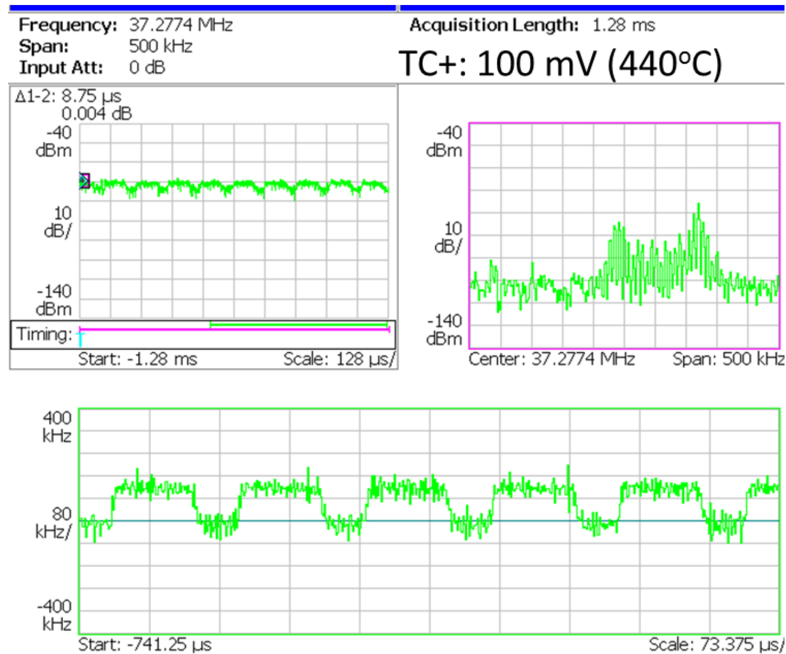


Fig. 82. RUK module-3 output at 440°C for 100 mV DC input to the sensor amplifier.

The frequency deviation on the transmitted signal from module-3 increases from 80 kHz to 140 kHz as the input to the sensor amplifier increases by 50 mV. This deviation indicates both the AM modulator, the frequency modulator, and the sensor op amp are working at 440°C.

5.6. Fraunhofer Module Testing

The assembled Fraunhofer module-1 shown in Fig. 54 is tested first to check individual circuit blocks' functionality. The schematic of the test setup configuration (for individual block testing on the Fraunhofer module) is shown in Fig. 83 (a). The op amp, amplitude modulator, WB oscillator, and the regulator output are measured through the oscilloscope. The voltage reference output is measured via a digital multi-meter. 10 nF of output load capacitance (with footprint sizing of 1209) for the regulator circuit is selected. Typically, the load capacitance on the regulator has to be > 0.1 μF; however, given the module area constraint, such output capacitance value will be difficult to implement. The use of lower output load capacitance would result in stability issues. The regulator circuit on the assembled Fraunhofer module-1 has been tested under probe station

at 350°C with a supply voltage of 20 V and 10 nF of load capacitance to showcase the stability problem. The resulting regulator output at 350°C is shown in Fig. 83 (b). At 25°C, the regulator output was 15.8 V. The regulator output has an output ripple of 6 V with 100 kHz frequency at 350°C. To minimize this output ripple to less than 0.5 V, load capacitance of more than 6/0.5 * 10 nF = 120 nF, is required which is equivalent to 12 capacitor components with 1209 footprint sizing. The reference circuit output voltage on module-1 drops down to 2.56 V at 350°C with 20 V supply (from 3.16 V @ 25°C with 20 V supply). As described in Chapter 3, this drop in the reference output would cause the regulator output voltage to drop. It also has to be noted that the resulting difference in this reference output from the results shown in Chapter 3 is due to the different die/reticle (from wafer #4) that is applied in the Fraunhofer module. The noted quiescent current from the reference and regulator circuit increased from 18 mA to 24 mA as temperature increased to 350°C for 20 V input supply. The reference circuit experienced visible damage due to overheating during testing at 350°C when the supply voltage increased to 30 V. Fig. 84 shows the damage (red circle) on the VDD trace of the reference circuits. The static current draw during the time of damage increased up to 35 mA. The regulator circuit also stopped functioning once tested at room temperature after the high-temperature testing (or one thermal cycle). The reference input node (the inverting node) on the regulator op amp can no longer control the regulator's output, although no visible damage can be observed while inspecting the regulator op amp.

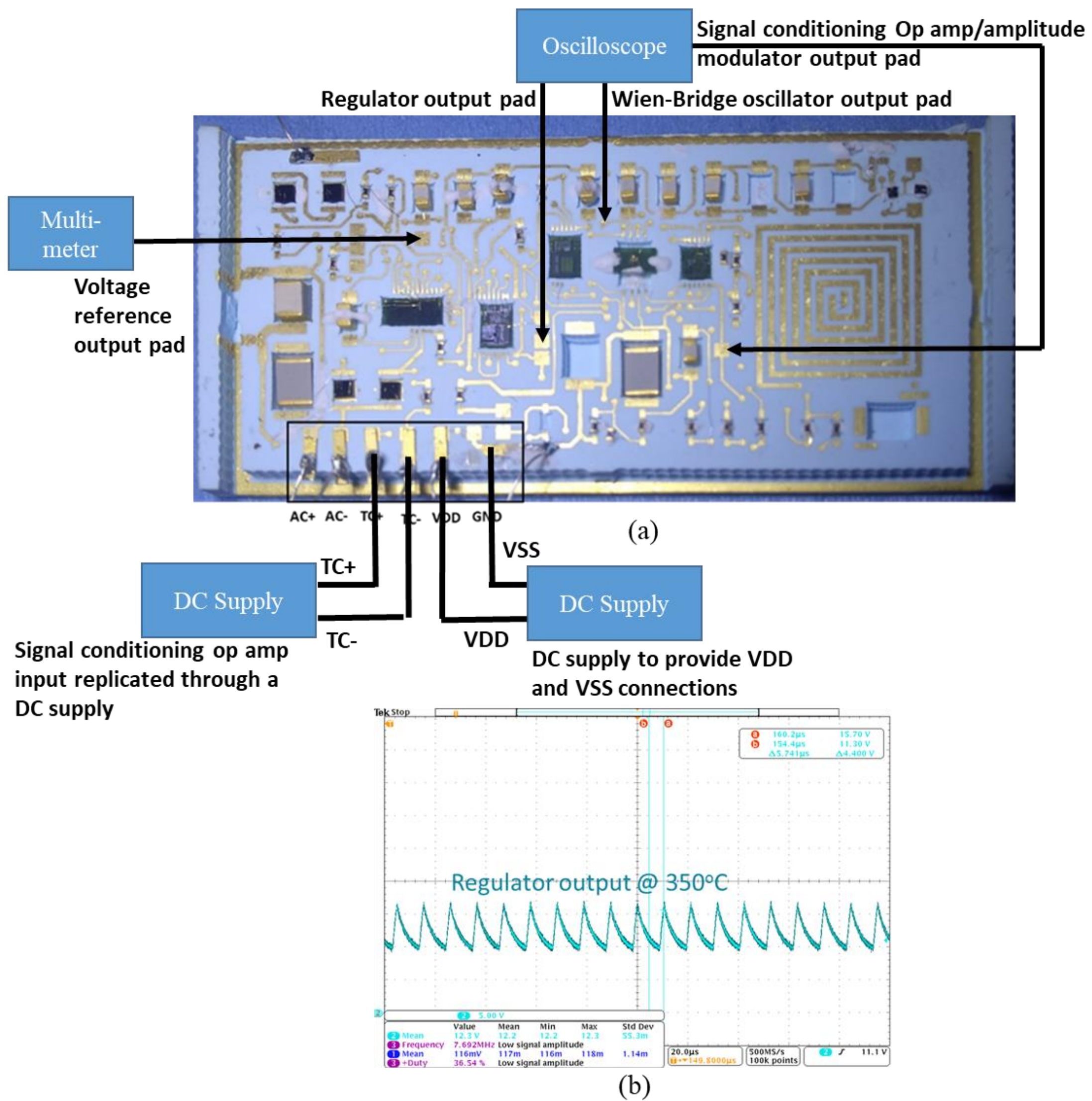


Fig. 83. (a) Test setup configuration for individual circuit testing on the Fraunhofer module, (b) Fraunhofer SiC Regulator output on the Fraunhofer module at 350°C.

Fig. 84. Visible damage (red-circled) on the reference circuit die due to VDD trace blowing up during 350°C testing with a static current draw of 35 mA at VDD = 30 V.

The Wein-Bridge oscillator (WB), amplitude modulator (AM), and the signal conditioning op amp circuits on the Fraunhofer module have also been tested. With a bridge RC network values of 100 kΩ, 100 pF, and closed-loop feedback gain resistors values of 10 kΩ and 100 kΩ, the resulting output frequency for the WB oscillator is observed at 6.28 kHz. The signal conditioning op amp showed an input-referred offset of 0.25 V when tested with a 300 mV, 1 kHz sinusoidal signal.

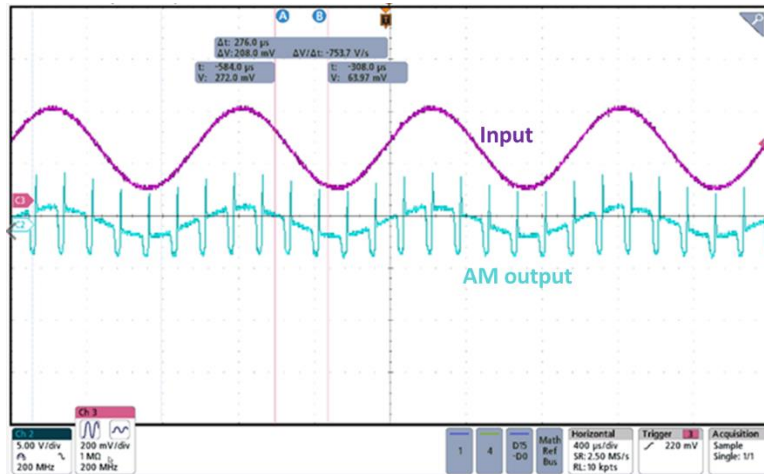


Fig. 85. Amplitude modulator output on the Fraunhofer module at 25°C.

The AM output at 25°C is shown in Fig. 85. The amplitude modulator in the Fraunhofer module has two NFETs in a common-source configuration. As a result, the modulated output is in the

opposite phase to the WB oscillator output. The observed spikes on the AM output occur at the falling edge of the WB oscillator output signal showing charge-injection effects due to the gate-drain capacitance of the NFET pass device. At 350°C, the op amp failed to operate, and the swing on the WB oscillator dropped. Post high-temperature testing, both the signal conditioning op amp and the WB oscillator failed to operate at room temperature, indicating that the system did not survive one thermal cycle.

The rectifier circuit section for the wireless power transfer mechanism on this module-1 has not been tested due to the damage sustained on the reference and regulator circuit. The rectifier circuit is tested in two steps, the first step included a half-wave rectifier circuit test on a dummy module, and the second step had the full-bridge rectifier test on the module-2 shown in Fig. 52 (bottom).

5.6.1 Rectifier Circuit Testing

Prior to the full-bridge rectifier circuit test, a half-wave rectifier circuit using a single SiC Schottky diode has been tested on a spare dummy module (the same module that has been used to test the Colpitts oscillator). The expected rectified output for the half-wave rectifier can be found by the equation below,

$$\boldsymbol{V_{RECTIFIER}} = \frac{\mathbf{0.5}\boldsymbol{V_{PK-PK}} - \boldsymbol{V_{(Diode-Drop)}}}{\boldsymbol{\pi}}$$

The inductor coil for this dummy module is created with another 0.4 mm diameter bare wire (similar to the one shown in Fig. 55). The inductance value for this coil, measured with an LCR meter, is 170 nH. The dummy module with the coil and Schottky diode is shown in Fig. 86 (left). The coil allowed to test the feasibility of wireless power transfer on the module. In Fig. 86 (right), the bench-top setup for the wireless power transfer test on the module is shown.

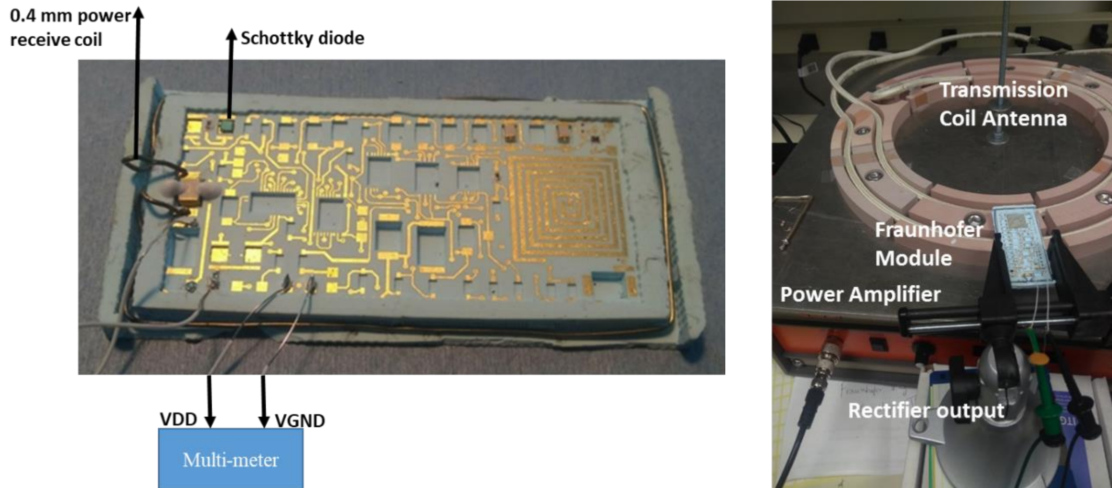


Fig. 86. (Left) Half-wave rectifier assembly on the dummy/spare Fraunhofer module, (right) bench-top setup for the half-wave-rectifier test with wireless power transfer.

Due to the unavailability of conductor trace on the cavity between the side-walls of this spare Fraunhofer module, the inductor coil has been looped across the stand-off region to be connected to the resonant capacitor of 1 nF value. The power transfer coil is connected to a 75 W power amplifier (Appendix-4) to provide sufficient transmitted signal strength for the module's coil to receive power. The gain of the power amplifier can be varied to generate the 20 V DC at the rectifier output. The input to the power amplifier is derived from a function generator capable of providing a maximum amplitude of 10 V. An external 10 nF output capacitor is connected in parallel with a 5 kΩ output resistor between the VDD and VGND pads. The rectified output is measured between the VDD and VGND pads with a multimeter. The wireless power transfer follows the resonant inductive coupling mechanism [35] and requires a capacitor in parallel to form the resonant circuit. With a 1 nF resonant capacitor, the expected resonant frequency of operation will be 12.2 MHz. The actual resonating frequency at which the transmission signal peak can be achieved is verified and selected at 11.5 MHz with the spectrum analyzer. A 3 $V_{PK\text{-}to\text{-}PK}$ at 11.5 MHz signal is provided to the power amplifier input through the function generator. The power coil is 0.75 cm in diameter and is placed on the ceramic base cavity. The wire coil material

is tin-plated copper. The module with the receiving coil is placed on top of the ceramic base, above the transmitting coil, with an air gap of few millimeters. A spectrum analyzer hooked to a coaxial coil antenna has been placed close to the module to monitor the receiving power as seen by the inductive coil on the module. The SA showed the receiving signal power peak at 9 dBm (or 1.782 $V_{PK\text{-}to\text{-}PK}$). For this peak value, the minimum rectified output, by applying the equation (page 110), will be 0.08 V. The actual rectified output is expected to be higher. The measured rectified output at the 5 kΩ load resistor from the multimeter shows 0.18 V.

The full-bridge rectifier circuit is tested for functionality on the second assembled Fraunhofer module-2, shown in Fig. 55. The configuration on the Fraunhofer module for the full-bridge rectifier test is shown in Fig. 87 (left). The module includes the regulator circuit whose input and output nodes were shorted for the full-bridge rectifier testing. In complete system testing this short will not be present. The module is tested prior to the inductor coil assembly and has been tested on the probe station. The image of the probe station setup is shown in Fig. 87 (right). This Fraunhofer module also has the Colpitts oscillator assembled on it with the tank capacitance set to 25 pF.

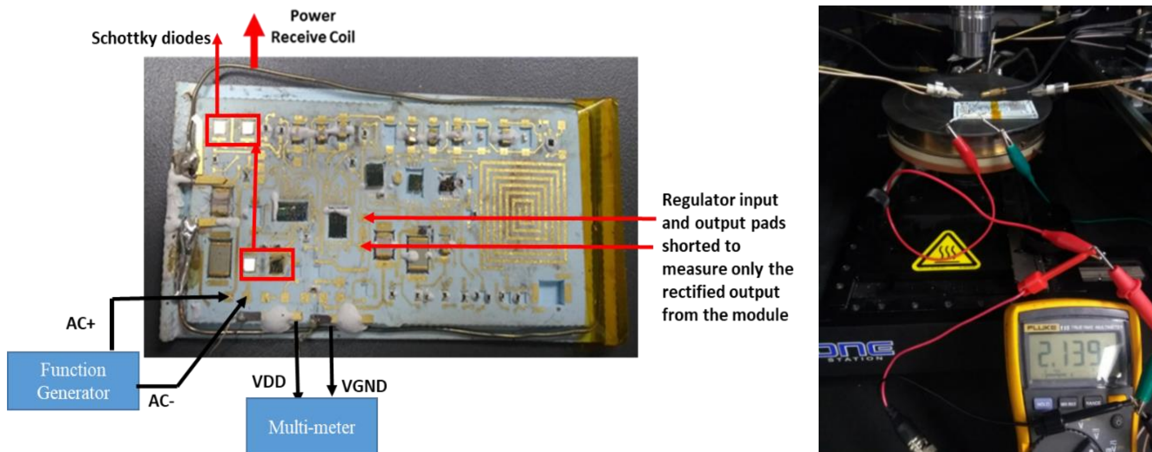


Fig. 87. (Left) Module configuration to test the full-bridge rectifier, (right) robe station setup to test the full-bridge rectifier circuit on the Fraunhofer module over temperature.

The probes shown in the image provide the AC signal on the AC+ and AC- pads on the module, coming from the function generator. The rectified output is measured across the 5 kΩ resistor via multimeter, similar to the half-wave rectifier test. A 5 MHz, 10 V_{PK-PK} sinusoidal signal is provided to the AC+ and AC- nodes on the module. The measured rectified output is 2.139 V. This is slightly lower than the theoretical full-bridge rectified output of 2.32 V, calculated using the equation below,

$$\boldsymbol{V_{RECTIFIER}} = \frac{\boldsymbol{2[0.5V_{PK-PK} - V_{(Diode-Drop)}]}}{\boldsymbol{\pi}}$$

The rectifier circuit on the Fraunhofer module is tested at high temperatures on the same probe station. The alligator wires connected to the VDD and GND pads are spaced apart from the probe station's thermal chuck to avoid melting of the cable exterior jacket. The rectifier circuit is tested at 350°C. The DC output voltage, measured through the multimeter, increased up to 2.412 V as expected. This is due to the forward voltage drop across the Schottky diode decreasing at high temperatures causing the rectified output voltage to increase.

The rectifier is intended to provide 20 V (or above) of rectified output in actual application across the regulator circuit. This can be done with the same power amplifier, as standard lab function generators cannot provide a signal with an amplitude of above 10 V.

The setup to validate the wireless power transfer mechanism on the Fraunhofer module-2, with full-bridge rectifier assembly, is the same as the half-wave rectifier testing on the dummy module. The rectified output is measured from the multimeter and the AC signal to the thick power-transmission coil if provided from the function generator through the same 75 W power amplifier. The power amplifier has 10 manual setting knob to increase amplification and vary the transmission signal strength. An 11.8 MHz, 15 V_{Pk-Pk} signal is provided on the power amplifier

input. The frequency is slightly higher for the full-bridge rectifier due to the receiving inductor coil having a somewhat lower (150 nH) inductance value. When the power amplifier setting knob is at its initial bar (which is the minimum gain of 18 dB), the rectified output on the multimeter showed 3.07 V. As the power amplifier setting knob is increased by 2 bars (each bar or step indicates 3 dB increase in gain), the rectified output rose to 8.71 V.

With the validation of the wireless power transfer and the full-bridge rectifier circuit, it is essential to check if the rectified DC output can supply the Colpitts oscillator for signal transmission on the second module. The Colpitts oscillator is one of the fundamental blocks in the signal conditioning system that allows the frequency modulation and transmission of the sensed signal. As mentioned earlier, the power transmission frequency is set to 11.8 MHz, the transmission frequency from the Colpitts oscillator is required to be set at a frequency outside the odd/even order harmonics of the power transmission signal. Therefore, a tank capacitance of 25 pF is used to provide a transmission signal centered at 55 MHz. It is to be noted that the actual center frequency of the oscillator would drop down to 30 to 40 MHz range once the decoupled capacitor and the varactor LED are added. Fig. 88 shows the Colpitts oscillator output at 5 V supply when tested separately.

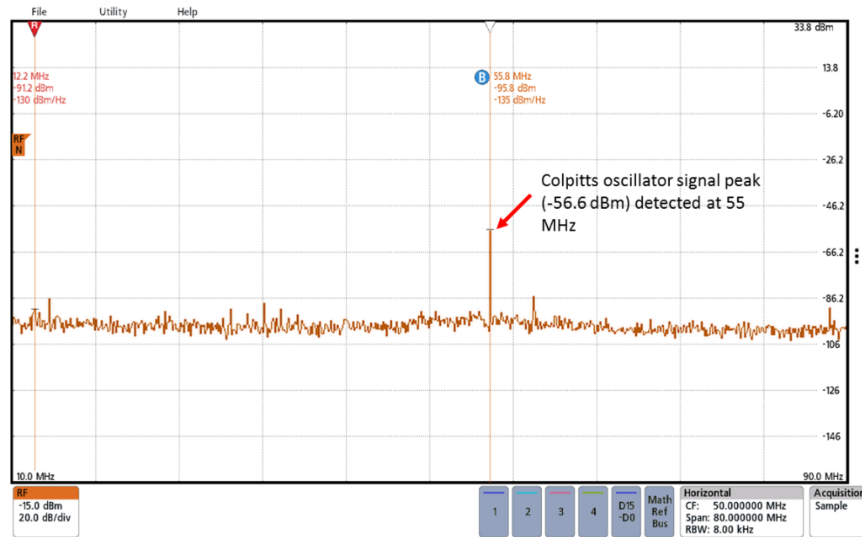


Fig. 88. Colpitts oscillator output on the Fraunhofer module at 5 V prior to the wireless power transfer/delivery test.

To detect this RF signal, a bare wire antenna is placed close to the module with the other end of the wire connected to the spectrum analyzer via a coaxial cable with a BNC termination port. The setup for testing the wireless power transfer, full-bridge rectifier powering the RF Colpitts oscillator circuits is shown in Fig. 89.

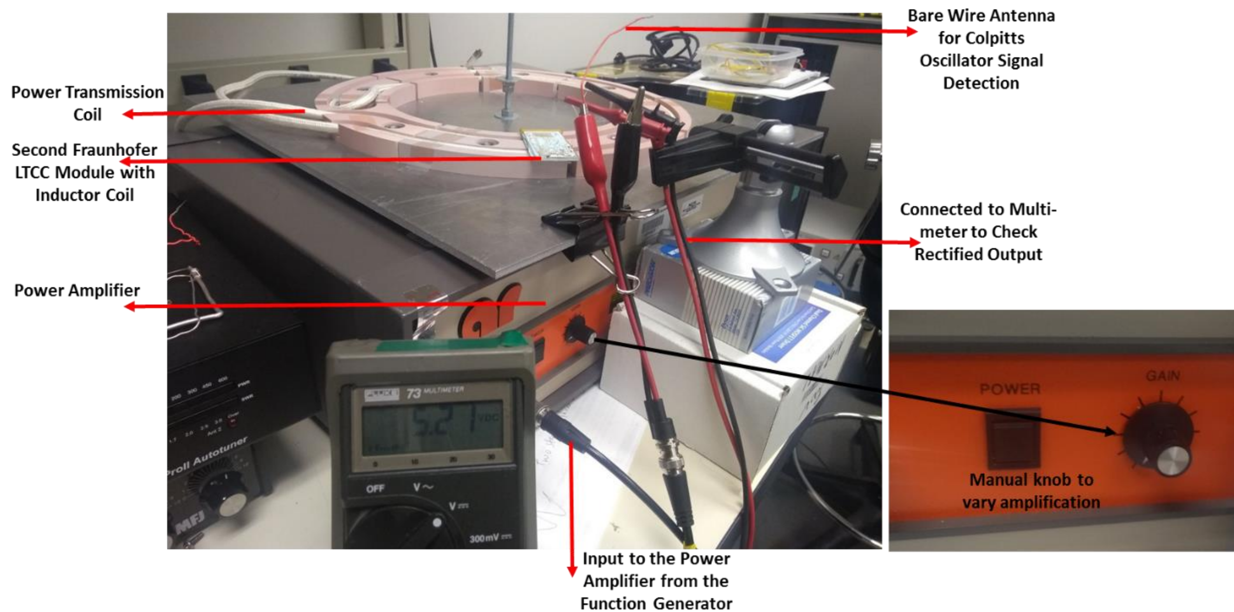


Fig. 89. Bench-top setup for testing the wireless power transfer with full-bridge rectifier powering the Colpitts oscillator.

The power amplifier knob is set to the second bar and 11.8 MHz, 10 V sinusoidal signal provided on the power amplifier input to generate between 5 V to 6 V of rectified output to power the oscillator circuit. The test setup image on Fig. 89 shows the measured output on the multimeter at 5.21 V. Fig. 90 shows the spectrum analyzer output (for a span 80 MHz – starting at 10 MHz and stopping at 90 MHz) with the detected Colpitts oscillator signal along with all the harmonics generated from the power transmission signal from the function generator. As the amplitude of the sinusoidal signal decreases to 5 V, the rectified output drops down to 3.07 V, resulting in the Colpitts oscillator circuit no longer functioning or transmitting. This can be seen in Fig. 91.

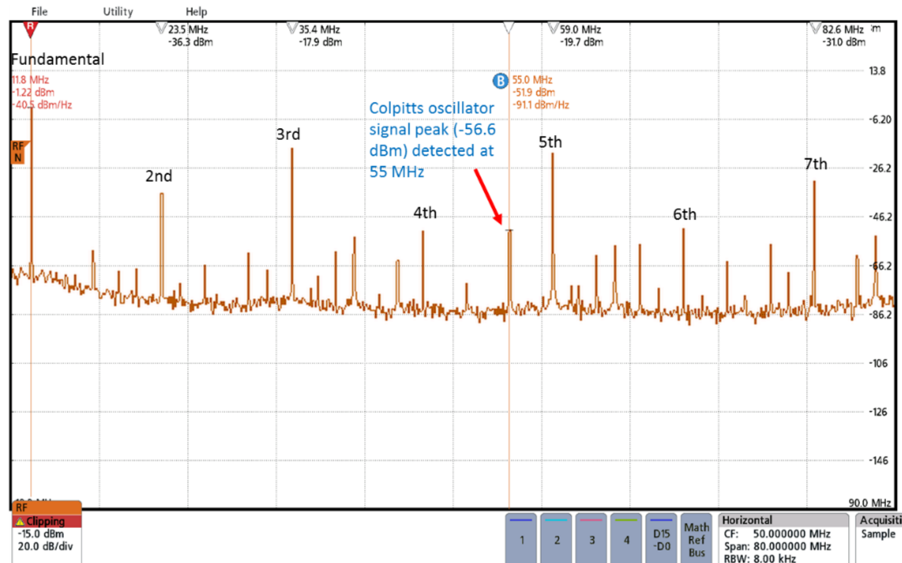


Fig. 90. Spectrum analyzer output detecting the wireless power transmission frequency, its harmonics, and the Colpitts oscillator output frequency.

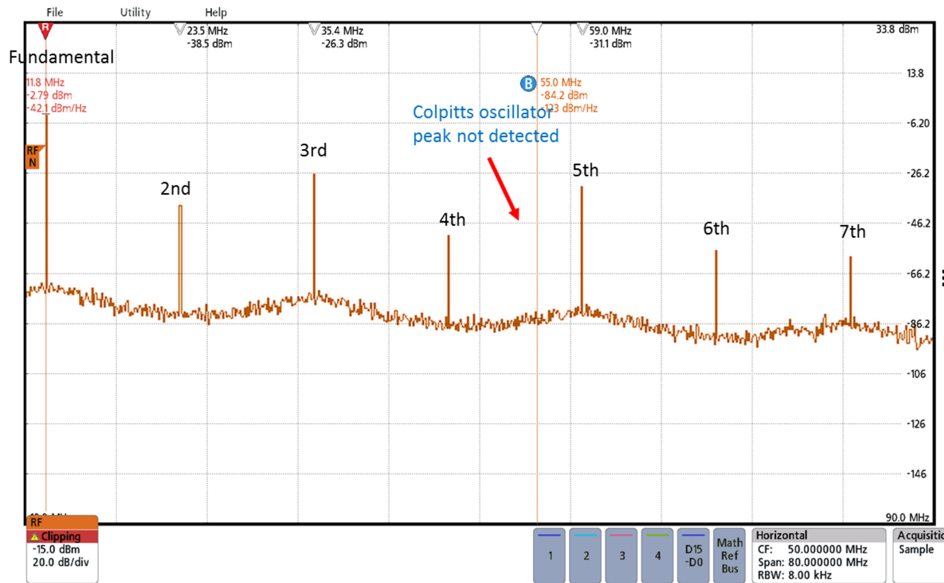


Fig. 91. Spectrum analyzer output detecting the wireless power transmission frequency and its harmonics but not the Colpitts oscillator output frequency.

It has to be noted that this verification test for the wireless power delivery system did not include any tuning devices or instruments. Hence, the power transfer efficiency is expected to be low. To improve the efficiency, tuning circuits are required to match the function generator to the power amplifier. Additionally, replacing the thin tin-plated copper wire coil with thick silver material-based coil would improve the overall power transfer efficiency.

5.6.2 Fraunhofer Module-2 High-Temperature Testing

After the testing and verification of the wireless power delivery section on the Fraunhofer module-2, the module is tested for signal conditioning system verification at temperature with the assembled reference and regulator circuit. The reference and the regulator are the final pieces of the complete wireless power transfer system, and therefore, the validation of the wireless power transfer system with these circuits is necessary. As seen on the test results from the Fraunhofer module-1, the regulator showed instability at higher temperatures. Increasing the output decoupling capacitors was not an option due to the module area constraint, so to minimize the ripple at the regulator output, a 1 nF capacitor was introduced at the output of the regulator's op

amp circuit. The NFET pass device regulator uses an internal two-stage op amp. The op amp was not internally compensated as the regulator's output capacitor was intended to provide the dominant low-frequency pole to provide enough phase margin for stabilizing the internal feedback loop of the regulator. Internally compensating the op-amp would likely have made a second relatively low-frequency pole and made stability challenging to achieve. However, in module-1, the output capacitance value is limited, and at higher temperatures, when the loop gain of the regulator increases (regulator loop gain comprises of the resistor divider, op amp, and the common-source level-shifter), the overall stability of the feedback system degrades. Hence, at higher temperatures, the regulator's op amp gain is compensated by adding the 1 nF capacitor at the op amp output.

The signal conditioning system testing with the regulator and the reference circuit on the Fraunhofer module-2 was performed under probe station at high-temperature by applying 20 V from an external supply to the node where the rectified output would be generated, which is also the regulator input pad (VREG). The wireless power delivery cannot be tested on the probe station due to space constraints associated with the large power transmission cable. The module-2 was tested at 300°C (due to the power receiving coil being assembled with 95/5 Pb-Sn solder, which is rated for 330°C) with the input (low voltage DC) to the signal conditioning op amp non-inverting node (TC+) provided from the function generator. The op amp initially had 1.8 V of offset at 25°C that dropped down to 0.8 V at 300°C. To compensate for the offset, the inverting node (TC-) of the signal conditioning op amp was provided with the offset value from a separate supply. Unlike the RUK modules, the Fraunhofer has the TC- node separated out to allow compensation for input offset. The transmitted frequency modulated signal from module-2 was detected by placing a probe-tip close to the spiral inductor of the LC-tank circuit. The probe tips have coaxial cables

with BNC termination that can be connected to the spectrum analyzer. The configuration for the full system test on the Fraunhofer module-2 is shown in .The frequency modulated output from the Fraunhofer module was detected through the spectrum analyzer. At 300°C, the spectrum analyzer outputs for 0 V, 50 mV, and 100 mV applied input to the signal conditioning op amp are shown in Fig. 93 (a), Fig. 93 (b), and Fig. 93 (c) respectively.

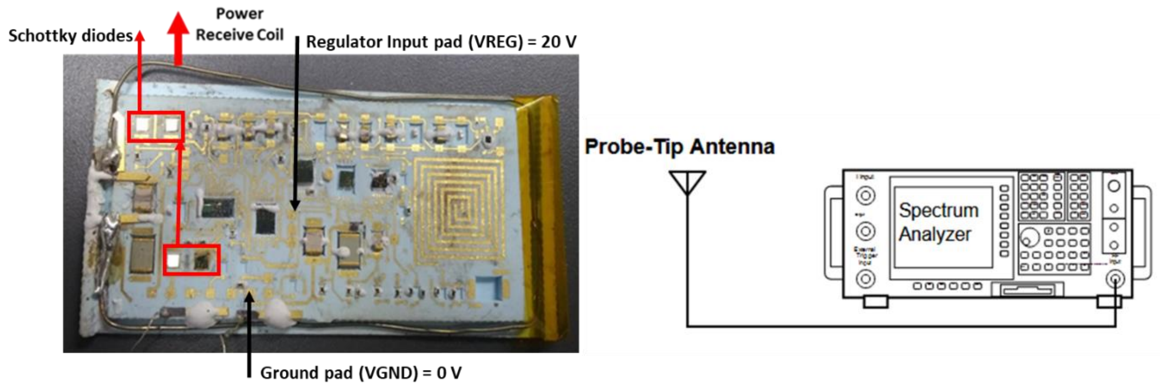
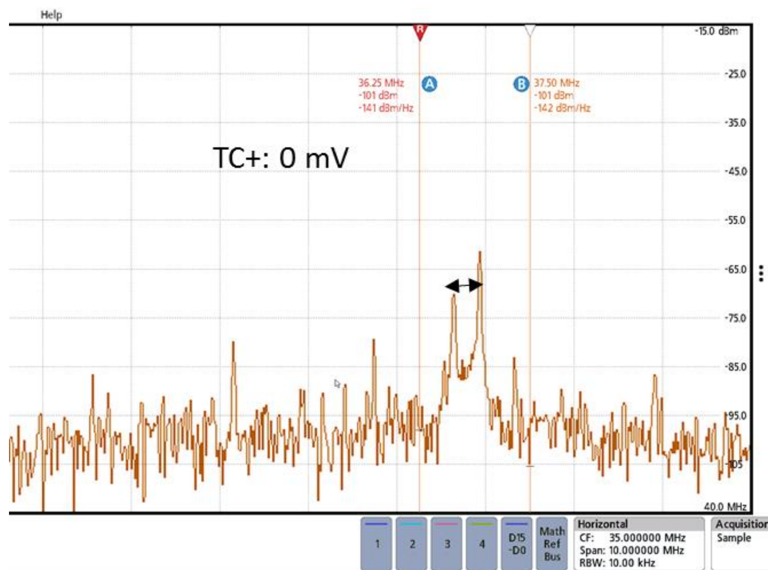
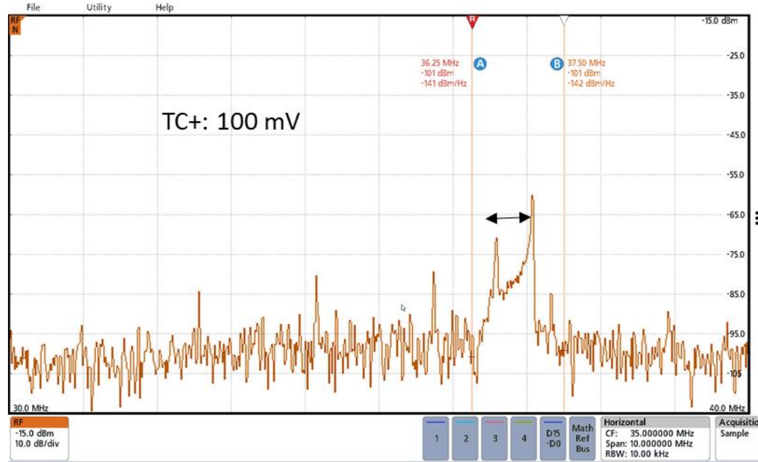


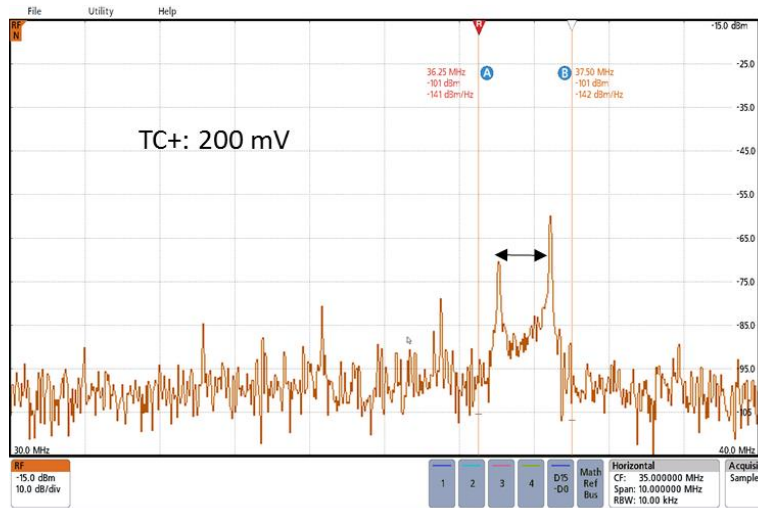
Fig. 92. Configuration of the Fraunhofer module for the full-system testing



(a)



(b)



(c)

Fig. 93. Spectrum analyzer output for the Fraunhofer module-2 signal conditioning system testing at 300°C.

5.6.3 Fraunhofer Module-3 Functional Testing

The assembled Fraunhofer-3 has been tested on the probe-station for SiC circuit functionality that constitutes the signal conditioning system. This includes the regulator, reference, WB oscillator, AM modulator, and the signal conditioning op amp circuits. The reference circuit output was measured with multimeter to avoid any capacitive loading on the reference circuit. The scaled

reference output voltage was 3.74 V at 20 V supply. Fig. 94, Fig. 95, Fig. 96, and Fig. 97 shows the individual circuit output from module-3. The regulator output for an externally provided 3.5 V reference and 20 V supply is equal to 16.2 V. The regulator output has feedback resistors of 210 kΩ and 55 kΩ (ratio of 3.81), resulting in an expected regulated output of (1+3.81)*3.5 = 16.83 V. The measured value is lower due to the low loop gain of the overall regulator circuit at room temperature. It has to be noted that the reference voltage applied to the regulator cannot exide 3.5 V as the regulator includes an NFET pass transistor which requires a minimum gate overdrive voltage of 3.1 V to operate. At reference voltage above 3.5 V (with supply voltage fixed at 20 V), the gate overdrive voltage on the NFET pass device of the regulator would drop, causing the regulator to not source sufficient current to the output. Thus the reference circuit output of 3.74 V is required to be further scaled down to properly operate the regulator circuit. The WB oscillator output is 8.27 kHz, lower than the expected frequency of 15 kHz, due to the loading effect on the bridge oscillator op amp output. The AM modulator output does not show any spiking at the falling edge of the bridge oscillator output, indicating negligible charge injection. The signal conditioning op amp shows 1 V peak-to-peak output for 100 mV sinusoidal input signal resulting in a closed-loop gain of 20 dB.

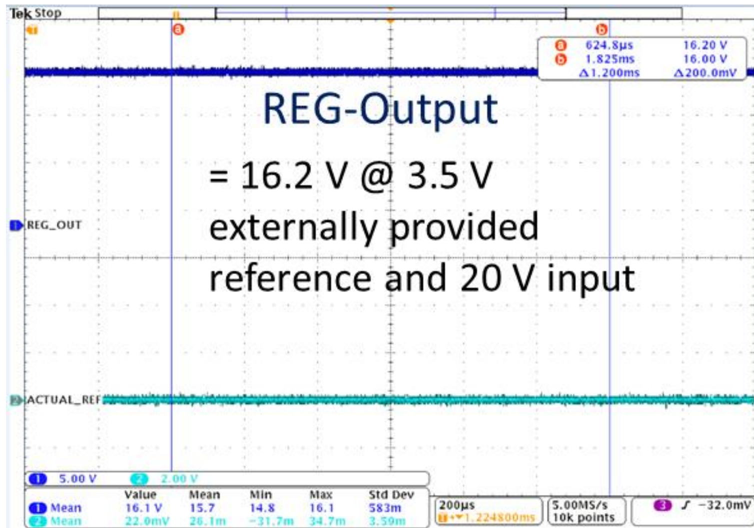


Fig. 94. Fraunhofer module-3 regulator output

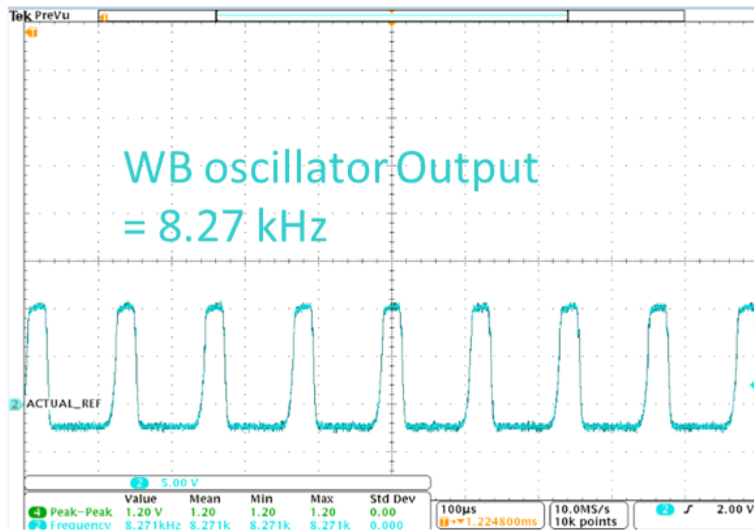


Fig. 95. Fraunhofer module-3 Wein-Bridge oscillator output

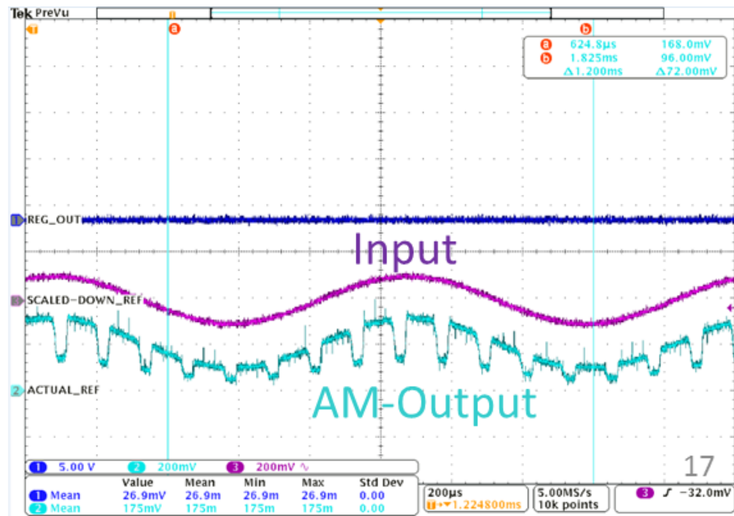


Fig. 96. Fraunhofer module-3 amplitude modulator output

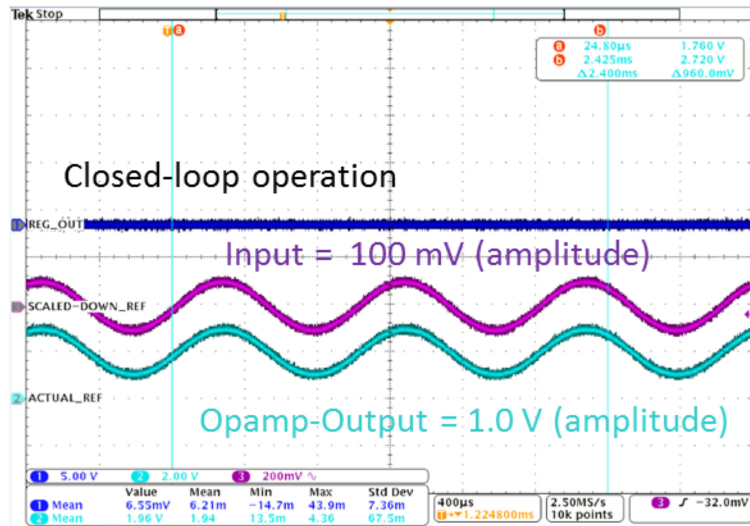


Fig. 97. Fraunhofer module-3 signal conditioning op amp output

Chapter 6. Conclusions and Future Work

6.1. Conclusion

The research work in this dissertation involved the design and assembly of extreme environment sustainable LTCC modules in supporting SiC signal conditioning circuits for sensors operating under harsh ambient. In lieu of that, a complete characterization of the new SiC CMOS process, from Fraunhofer, through two fabrication runs has been demonstrated in this dissertation. The transistor characterization over temperature from the first run to the necessary modifications on the fabrication steps to improve the transistor behavior (especially PFET) for the second run has been thoroughly discussed. The PFET to NFET drive strength improved by more than two times. The dissertation describes the design and testing of the circuits from the second fabrication run. The circuits on the second fabrication run were designed with increased P-to-N driver ratio to accommodate for the poor PFET behavior observed on the first fabrication run. The designed circuits includes the first op amp based voltage reference design in SiC CMOS that has been shown to operate at 350°C on bench-top level. The output variation on the voltage reference circuit was 1.97 mV/^{o}C. The op amp used in the voltage reference circuit has a two-stage architecture with NFET differential pair and indirect compensation technique that is the first in SiC CMOS process. Other designed circuits include two-stage op amp with PFET differential input pair that has been tested for at 500°C and provided open-loop gain of 48.9 dB. These circuits (including the PFET two-stage op amp) were used to design the signal conditioning module with modulation (frequency and amplitude) and signal transmission capability. The previous state of the art signal conditioning system did not include an op amp circuit for signal conditioning purpose, instead used a conventional differential amplifier. As part of the work, rather than just relying on the newly

fabricated SiC circuits from a new SiC CMOS process, circuits from the previously fabricated Raytheon UK (RUK) process (a well-developed process) were also used to design another signal conditioning module. SiC bipolar process was also investigated as a viable option to implement the high-temperature signal conditioning system. In relation to that, the first negative voltage charge pump and the first signal conditioning system was designed in the SiC bipolar process. The designs were tested and operated up to 450°C for the first fabrication run, however, all the designs on the second fabrication run failed to operate due to fabrication mishap related to improper on-chip resistor fabrication.

The dissertation details the design and assembly of the two LTCC modules (RUK and Fraunhofer), created on 20 layers of Dupont's 9k7 Green Tape™ material. The end modules were 68.5 mm × 34. 3 mm in dimensions with multi-depth cavities and stand-off rings to allow the modules to be fitted within an enclosure to protect the circuits, passive components, and bond wires. Both the RUK and Fraunhofer modules deploy the same modulation scheme to transmit the sensed signal using the Colpitts Oscillator. The assembly methods to attach electronic components were validated by testing the LTCC modules at high temperatures (up to 440°C) and high rotational speeds (10,920 rpm). The previous state of the art LTCC module has been tested under 10,124 RPM and temperatures at 425°C. The RUK module supports a wired medium to deliver power to the circuits, and the Fraunhofer module supports both the wired and wireless medium for power delivery. The wireless power transfer mechanism was validated on the Fraunhofer module by powering the transmitter circuit (Colpitts Oscillator). The previous state of the art LTCC module only provided provision for wired power supply.

6.2. Future Work

The circuits from the Fraunhofer SiC CMOS process were designed without the assistance of a complete process design kit and accurate device models. These limitations are expected on a process that is currently in its development phase as the fabrication steps are not ironed out, and device characterization is not fully understood, resulting in low circuit yield due to high process variation. These issues can be observed through the results for the reference and regulator circuit that showed diminishing behavior over temperatures. The process also suffers from poor P+ contacts, which is a damning factor in a CMOS process technology as it degrades the performance of PFETs and WELL diodes. However, the process does show an instance of progress in relation to providing functional circuits on aluminum metallization wafers. With the availability of proper models with corners and low-resistive P+ contacts, the design methods for the circuits can be improved with further fabrication runs in the future.

Improvements on the current circuits can also be made in case the process cannot further optimize the contacts. The op amp circuits especially can be designed with a dynamic offset cancellation technique that requires capacitors to store the op amp offset for one clock cycle. The trade-off in using such architecture is always the extra die area. The architecture requires additional differential pair in connection to the actual first stage differential pair of the op amp (Appendix-5). The module design area will also increase as the offset storage capacitors are high-valued (hundreds of pico-farads) and must be placed off-chip. The reference circuit can be improved by eliminating the PWELL-to-N+ on-chip diodes and use off-chip diodes. The trade-off again is going to be the additional module area to accommodate those off-chip diodes. Finally, the circuits in the Fraunhofer CMOS process are initially intended to operate at 400°C and above temperatures with repeatable functionality over multiple thermal cycles. This is difficult to achieve with aluminum

metallization. Thus, circuit structures with platinum metallization will be necessary to test and validate circuit design for temperatures above $400^{\circ}C$.

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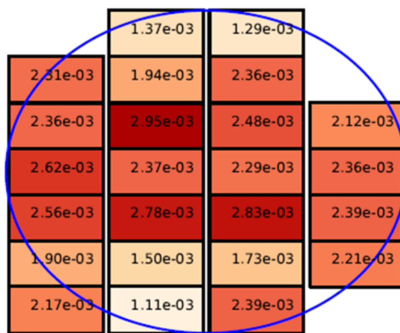
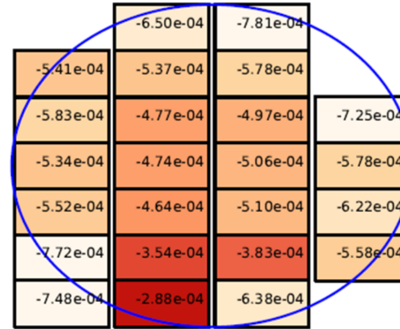
Appendix

Appendix-1

Drain current variation for RUK CMOS 20 µm by 1.2 µm NFETs and PFETs over a full wafer. The resulting drive current ratio for PFET-to-NFET in the RUK process is around 1:5. The threshold voltage over temperature for the RUK transistor (NFET) varies by 1.1 mV/°C. For the Fraunhofer transistor (NFET), the variation is 5.45 mV/ °C



20 µm by 1.2 µm NMOS maximum drain current variation over wafer



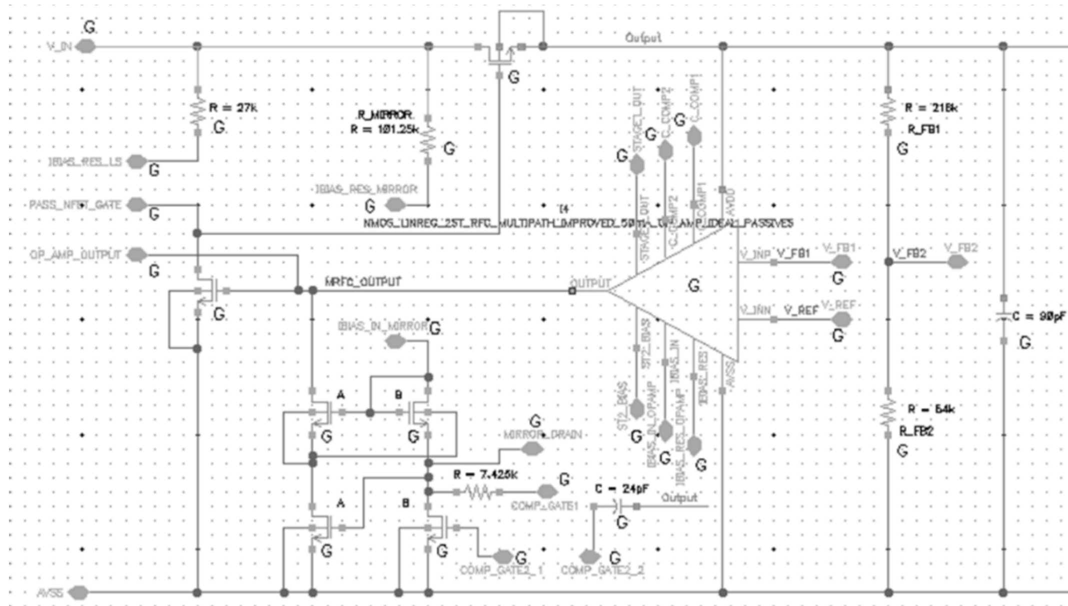
20 µm by 1.2 µm PMOS maximum drain current variation over wafer

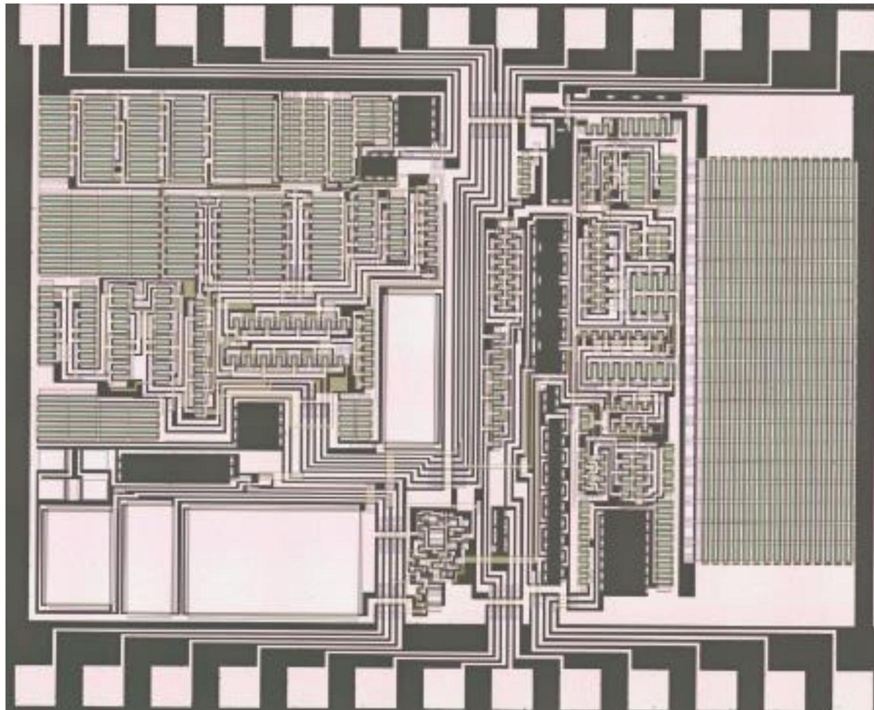
Comparison between RUK and Fraunhofer transistors' (PFET & NFET) parameters

Parameter name	RUK Parameter values		Fraunhofer Parameter values	
	NFET	PFET	NFET	PFET
Max. applied gate voltage (V)	15	-15	20	-20
Max. applied drain voltage (V)	15	-15	20	-20
Max. applied body voltage (V)	-15	15	-20	30
Typical threshold voltage (V) at 25°C	3	-5	-3.25 V	-6.5 V to -7 V
Gate leakage current (pA) @ 25°C and @ V_{GS} = 15 V	0.7	0.8	9.3	9.3
Gate oxide thickness (nm)	40	40	50	50
Minimum channel width (µm)	4	4	3	7
Minimum channel length (µm)	1.2	1.2	1	1
Test structure channel width (µm)	20	20	20	20
Test structure channel length (µm)	1.2	1.2	1.5	1.5
PWELL (NFET) /NWELL (PFET) doping concentration (cm^{-3})	6.7×10^{16}	4×10^{17}	$1x10^{17}$	$3x10^{15}$

Parameter name	RUK Parameter values		Fraunhofer Parameter values	
	NFET	PFET	NFET	PFET
Body leakage current (pA) @ 25^0C and @ $V_{DS} = 15$ V	55	20	143	4.4

Fraunhofer SiC CMOS linear regulator schematic, die micrograph, and load/Line regulation:





Load Regulation (initial 10 nF at 25°C, increased to 200 nF at 350°C for stability). I_{LOAD} was provided from a source meter.

<table>
<tr><th>Temp (°C)</th><th>V_{IN} (V)</th><th>I_{LOAD} (mA)</th><th>V_{REG} (V)</th><th>Load Regulation ($\Delta V_{REG}/\Delta I_{LOAD}$)</th></tr>
<tr><td>25</td><td>20</td><td>1</td><td>14.84</td><td rowspan="2">0.010</td></tr>
<tr><td>25</td><td>20</td><td>20</td><td>14.66</td></tr>
<tr><td>350</td><td>20</td><td>1</td><td>15.5</td><td rowspan="2">0.021</td></tr>
<tr><td>350</td><td>20</td><td>20</td><td>15.1</td></tr>
</table>

Line Regulation @ 25°C (initial 10 nF at 25°C, increased to 200 nF at 350°C for stability). I_{LOAD} was provided from a source meter.

Temp (°C)	V_{IN} (V)	I_{LOAD} (mA)	V_{REG} (V)	Line Regulation ($\Delta V_{REG}/\Delta V_{IN}$)
25	20	20	14.66	
25	21	20	15.16	0.49
25	22	20	15.55	0.39
25	23	20	15.77	0.22
25	24	20	15.87	0.10
25	25	20	15.71	-0.16

Line Regulation @ 25°C (initial 10 nF at 25°C, increased to 200 nF at 350°C for stability). I_{LOAD} was provided from a source meter.

Temp (°C)	V_{IN} (V)	I_{LOAD} (mA)	V_{REG} (V)	Line Regulation ($\Delta V_{REG}/\Delta V_{IN}$)
350	20	20	15.50	
350	21	20	15.30	0.2
350	22	20	15.30	
350	23	20	15.20	0.1
350	24	20	15.10	
350	25	20	15.10	

Appendix-2

Sintered silver epoxy, Duralco™ 124 rated for 343°C or 650°F. First phase of curing method involves mixing of equal quantity of silver resins and hardening material. Second phase involves curing the mixture at 200°F (93°C) on a vacuum oven for 4 hours. Prior to the curing on oven, the mixed epoxy should be applied to the module pads with carefulness as the silver epoxy is conductive and spreads easily.

Pelco high-performance silver paste that is rated for 927°C .The paste is highly viscous and requires addition of water to reduce viscosity for compoenent attachement on LTCC modules

High temperature ceramic epoxy, Resbond 940HT is rated for 2800°F (or 1537°C). The curing method involves mixing the ceramic power with hardening material in the 10:1 ratio or 100 grams of ceramic powder added to 10 grams of hardening material. The mixer takes less than 10 minutes to settle at room-temperature. At temperatures above 175°F (or 79°C) the mixture will solidify. Extra care has to be given when depositing the mixture to the cavities as the mixture can solidify quickly if left more than 30 minutes at room-temperature. While using the mixture to attach circuit die with smaller area and depth, apply caution as the mixture can easily spread over the die pads. To remove the mixture still is the liquid state, apply alcohol solution and micro-fiber fabric.

Nextel glass fiber fabric is prepped in the following steps:

i. Cut the Nextel fiber to the required area
ii. Put the fiber in a thermal over and heat the fiber up to 400°C for 10 minutes
iii. Remove the fiber from the over, cool down , and apply liquid super-glue all over the fiber
iv. Let the glue dry and put the fiber back again on the oven and heat the fiber up to 420°C for 30 minutes

v. Bring out the fiber from the oven

Appendix-3

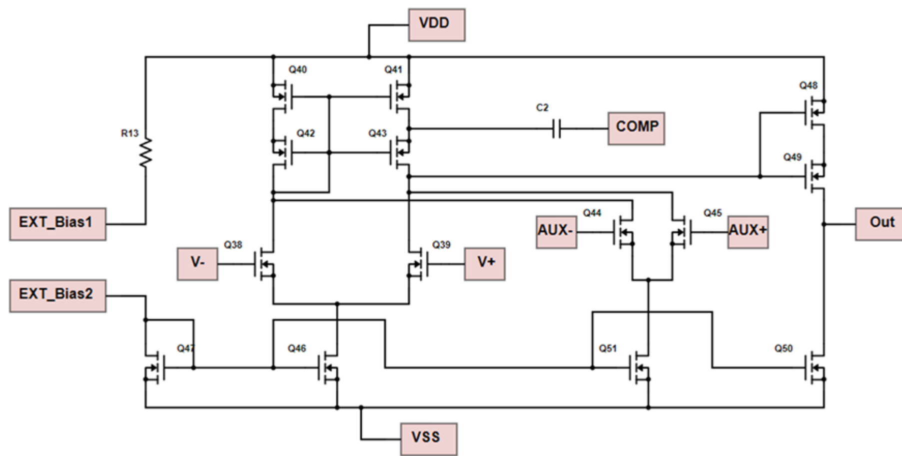
RUK Two-stage OP AMP Datasheet

Specification	Detail	Tested	Units	Comments
Supply Voltage		15	V	
Power Consumption		15	mW	
Bias Current		100	μA	
DC Gain (VCM=3V)	Temp = 25°C	60.6	dB	
	Temp = 400°C	60.6		
Unity Gain Bandwidth	Temp = 25°C	3.2	MHz	10 pF load
	Temp = 400°C	2.3		
Offset	Temp = 25°C	-13	mV	
	Temp = 400°C	-60		
Positive Slew Rate	Temp = 25°C	6.2	V/μs	10 pF load
	Temp = 400°C	5.2		
Negative Slew Rate	Temp = 25°C	30.3	V/μs	10 pF load
	Temp = 400°C	39.4		
Input Common Mode	Temp = 25°C	0-9.6	V	
	Temp = 400°C	0-11.2		
Output Range	Temp = 25°C	0.3-13	V	
	Temp = 400°C	0.3-13		

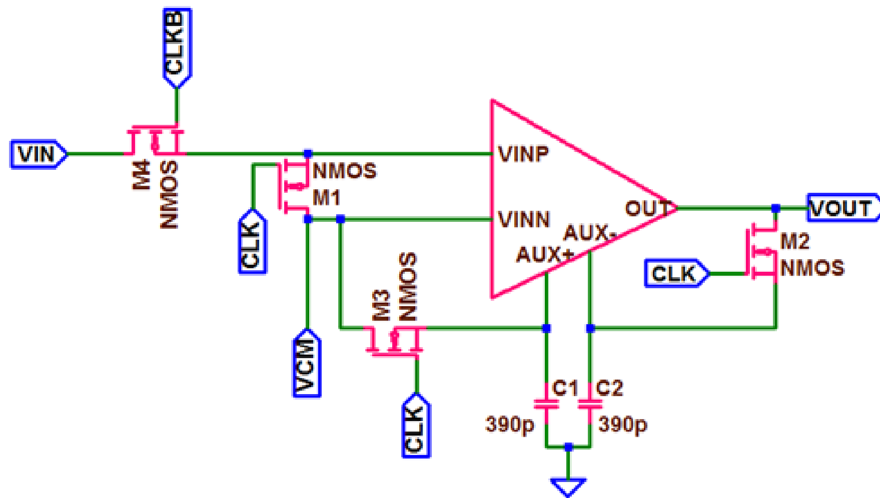
Appendix-4

1. Wireless Data Corp Telemertry Receiver or WDC receiver provided by Siemens
    a. The receiver can detect frequency between 63 MHz to 78 MHz with demodulation bandwidth of 150 kHz
2. Real-time Spectrum Analyzer or RSA provided by Wolfspeed (CREE)
    a. The RSA has the capacbility to provide frequency variation within a signal on the time-domain format
3. Amplifier Research (AR) 75 Watts power amplifier with frequency range of 10 kHz to 250 MHz provided by Wolfspeed (CREE)

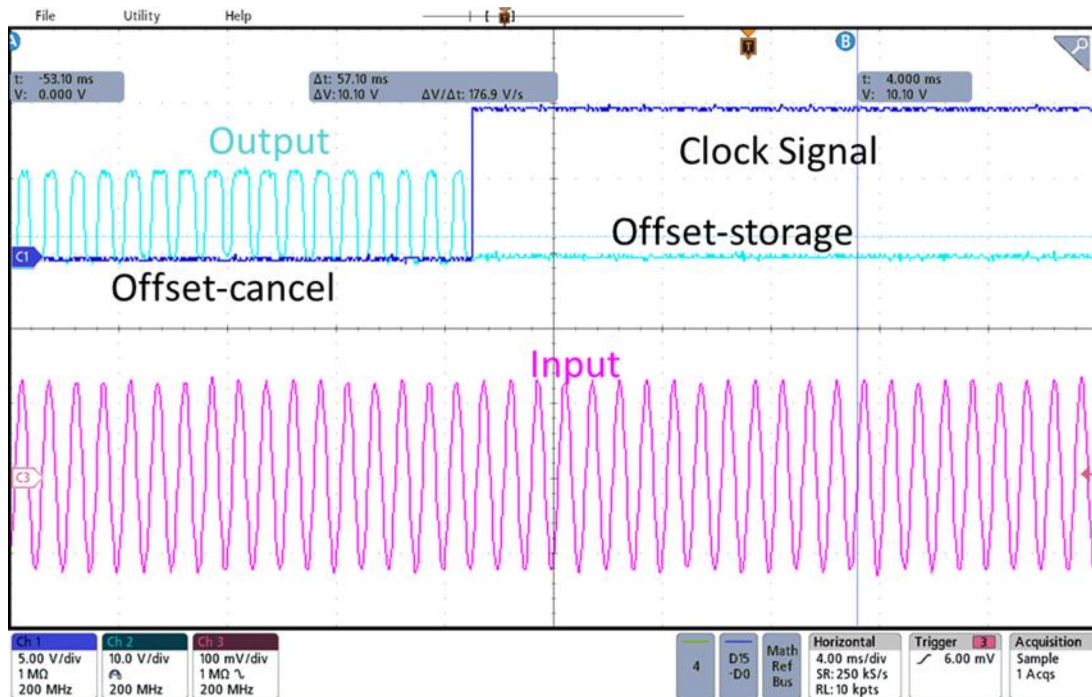
Appendix-5



Two-stage NFET op amp with auxiliary differential pair to implement dynamic offset cancellation



Top-level schematic of the dynamic offset cancellatio circuit wutg C1 and C2 being the offset storage capacitors.



Measured output for the op amp output with offset cancelled

- Biasing resistor (65 kΩ) provided externally
- Uses indirect compensation and requires two 390 pF offset storage external capacitors
- Testing performed on Rogers-4350 breakout board
- Testing involved supplying VDD = 15 V and VSS = 0 V. Non-inverting node (VINP) saw

  1 kHz, 250 mV sinusoidal signal on DC value of 4 V.

  - Inverting node (VINN) saw 4.89 V to observe amplification prior to apply the offset cancellation capacitors
  - With offset cancellation capacitors connected, applied VNN = 4 V
- Applied clock signal: 15 V, 20 Hz