HIGH-DENSITY MULTILEVEL POWER CONVERTERS FOR USE IN RENEWABLE AND TRANSPORTATION APPLICATIONS

BY

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DISSERTATION

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ABSTRACT

Electrification of transportation and the development of renewable resources promise to offer both environmental and economic benefits. In each instance, the size and weight of the power electronics play a role in the overall system efficiency and installation cost. This dissertation demonstrates opportunities for increasing the power density and efficiency of inverter systems through the use of high-density capacitive energy storage and flying capacitor multilevel (FCML) power converters.

While historically limited to energy-dense electrolytic or low-loss film-based capacitors, designers now have an increasing array of high-energy-density ceramic capacitors available to them. In addition to the small signal characteristics of these devices which are typically provided by the manufacturer, designers need to understand the characteristics of these devices under large voltage swing. This dissertation addresses this need by developing and demonstrating a method of characterizing capacitors under large voltage swing. The significance of a proper understanding of the large-signal characteristics of these devices has been demonstrated through the a wide survey of available devices and the development of a design process for maximizing the power density of active energy buffers based on capacitor technology.

Building on an understanding of the potential benefits of capacitor technology, this dissertation next explores the application of ceramic capacitors as the primary energy storage mechanism in DC-AC inverters. The flying capacitor multilevel topology (FCML) has been shown to exhibit high efficiency and high power density. This is especially true in applications requiring low harmonic distortion such as inverters driving low-inductance high-density electric machines. Much of the prior work on the FCML converter has focused on various aspects of converter control. However, the demonstration of the power density and efficiency benefits of the topology have often been masked by the use of general-purpose lab hardware and low switching frequency. This work seeks to demonstrate the applicability and advantages of the FCML architecture for a range of applications. Through the design and implementation of a 13-level flying capacitor converter, the passive balancing characteristics of the FCML converter previously demonstrated at level counts of four to seven can be ex-

tended to higher level counts and voltage using high-speed, wide bandgap gallium nitride (GaN) devices.

The FCML topology holds special potential in applications where high specific power density (kW/kg) has significant value such as three-phase motor drives for hybrid electric aircraft. These designs incorporate turbine-driven electric generation with distributed electric propulsion to achieve system-level aerodynamic benefits. While conventional Jet-A fuel may be used, low-temperature fuels such as liquefied natural gas (LNG) offer additional system-level benefits through the use of low-temperature fuel to cool the power electronics. This can not only improve the efficiency of the power conversion, but also reduce the energy expended to heat the fuel before combustion. This dissertation demonstrates that GaN-based FCML converters can be advantageous at low temperature through the design and detailed evaluation of a 3-level flying capacitor converter operating near cryogenic temperatures.

Having demonstrated the benefits of the FCML architecture on a single-phase basis, the dissertation commences with the design of a complete FCML-based motor drive tailored for high-density, low-inductance permanent magnet machines. The drive system incorporates a scalable architecture allowing a wide variety of applications to be met using an optimized single-phase FCML module. Even current sharing and vector control of a low-inductance permanent magnet machine were achieved.

To my amazing brothers and sisters, Anna, Benjamin, Daniel, Eric, Jonathan, Laura, Melissa, Rebekah, and Ryan.

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LIST OF ABBREVIATIONS

CCM	Continuous Conduction Mode
EMI	Electromagnetic Interference
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
FCML	Flying Capacitor Multilevel (Converter)
FPGA	Field Programmable Gate Array
GAN	Gallium Nitride
HIL	Hardware-In-The-Loop
ILM	Interleaved Module
LNG	Liquefied Natural Gas
MLCC	Multilayer Ceramic Capacitor
MMC	Modular Multilevel Converter
PMSM	Permanent Magnet Synchronous Machine
POF	Plastic Optical Fiber
PSPWM	Phase-Shifted PWM
RDC	Resolver to Digital Converter
THD	Total Harmonic Distortion
VTOL	Vertical Take-off and Landing (Aircraft)

CHAPTER 1

INTRODUCTION

Power electronics are an enabling technology for numerous applications ranging from energy efficient lighting to electrified transportation and renewable energy. The specific power density (power to weight ratio, $\frac{kW}{kg}$) of electric power conversion is a significant factor in the cost and performance of many system. In stationary applications, power converter weight and volume play a role in both capital and installation costs. This is especially true in PV systems as the rapid decline in panel costs has made the reduction of installation time and required equipment a key aspect of further progress in system affordability [1].

In mobile applications, especially aviation, overall vehicle weight will impact the vehicle's efficiency and range. Ongoing research is highlighting the advantages of electric hybridization in aircraft applications. When applied to single-aisle aircraft, estimates of efficiency indicate measureable reductions in fuel consumption in addition to reduced noise and pollution at take-off [2, 3]. In addition to single-aisle fixed wing aircraft, vertical take-off and landing aircraft (VTOL) could potentially be revolutionized through hybridization and the opportunity for a larger number of thrust producing fans. Hybridization also promises to revolutionize small short-range aircraft, opening new commercial opportunities in regional air transportation [4]. Recognition of these opportunities has fueled research into the development of high-power-density electric drive train systems. Given the dramatic gains in turbine engine efficiency and thrust to weight ratio over the last sixty years, electric motors and drives must meet formidable specific-power density specifications in order to justify their integration into hybrid aircraft designs.

The research in this dissertation has been undertaken with the goal of increasing the density of power conversion systems with a special focus on renewable and aviation applications. The primary means to achieve this objective has been through the efficient utilization of capacitor-based energy transfer. At the scale of energy conversion addressed by many power electronics applications, the energy storage of capacitive energy storage is found to be 1-2 orders of magnitude higher than inductive energy storage [5]. This trend is illustrated in Fig. 1.1 by the comparison of 118 mJ of capacitive energy storage in the form of ceramic multilayer capacitors with 4 mJ of inductive energy storage. While research continues on

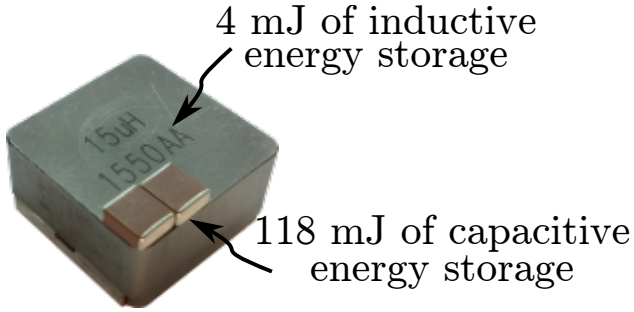


Figure 1.1: The energy storage density of capacitors far exceeds that of inductors in most power electronics applications.

the development of magnetic materials, at present this reality suggests that capacitive-based power conversion is a means to achieving higher power conversion density.

This research has sought to further the development of capacitor-based energy conversion through developing a greater understanding of the capacitor technology currently available to power electronics designers, integrating these devices into high-density, flying capacitor multilevel (FCML) converters, and finally coordinating these FCML converters into a modular motor drive system focused on aviation applications.

1.1 Organization of This Dissertation

The work in this dissertation is organized as follows:

1. Chapter 1: Evaluation of Capacitor Energy Density and Efficiency for Energy Buffering Applications

   Based on an understanding of the high potential energy conversion density of capacitors, it is worthwhile to invest time in understanding their performance as accurately as possible. Historically, most capacitor analysis and data have been based on small signal device modeling. Reviewing most manufacturer data sheets will reveal data for capacitor impedance and ESR which is measured using a perturbation amplitude on the order of 100 mV over a range of frequencies. This test condition is significantly different from the typical use case in power conversion. In addition to high-frequency applications, such as the flying capacitors, there is also an increasing need for efficient, dense, energy buffering in single-phase line-frequency applications. Conversion between a constant power dc source, such as PV systems and batteries, and alternating current ac sources requires the use of an energy storage device to balance the instantaneous power difference between the source and load that is present in all single-phase

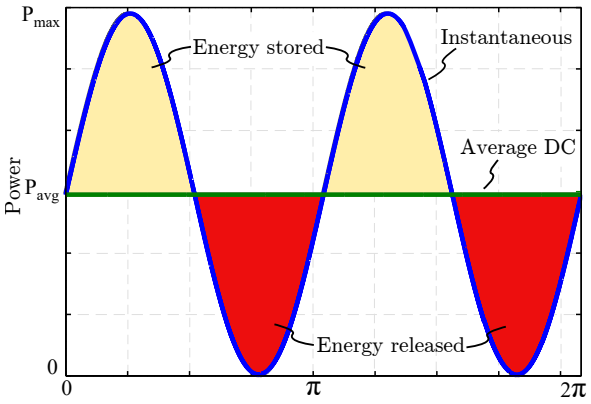


Figure 1.2: Instantaneous power mismatch between DC and single-phase AC.

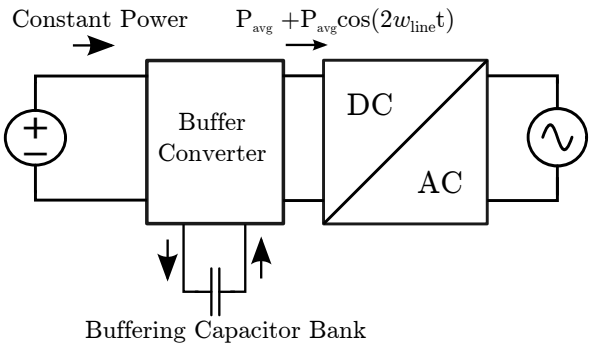


Figure 1.3: Energy buffering circuit of single-phase inverter.

systems. Fig. 1.2 depicts the power imbalance between the DC source and the AC load and the difference in energy which must be buffered over a full AC cycle.

This power buffering has often been accomplished using a large capacitance which was sized to minimize ripple; however, an alternative approach is shown conceptually in Fig. 1.3 in which an active power converter is used to decouple the energy storage in the capacitor from the voltage regulation on the dc link. While this minimizes the size of the capacitance required, it also necessitates a more complete understanding of the large-signal characteristics of the capacitor.

In Chapter 1 [6] an experimental configuration is developed for evaluating capacitor energy storage density and efficiency under a large sinusoidal voltage swing. Combined with a survey of the capacitor performance over a range of technologies, this chapter explains the process of designing using ceramic capacitors and provides a design example demonstrating the gains in energy density which can be obtained through taking the bias-dependent capacitance of Type II ceramic capacitors into consideration. This work was used to direct the selection of ceramic capacitors used in the series stacked energy buffer presented in [7], and also became the starting point for an investigation, supervised by the author, of ceramic capacitors in high-frequency switching applications with large voltage ripple [8].

2. Chapter 2: Design and Control of a GaN-based, 13-level, Flying Capacitor Multilevel Inverter

   As discussed, the replacement of inductors with high-energy-density capacitors can lead to significant gains in power conversion density. Building on the data and experience gained through the capacitor characterization in Chapter 2, this chapter investigates

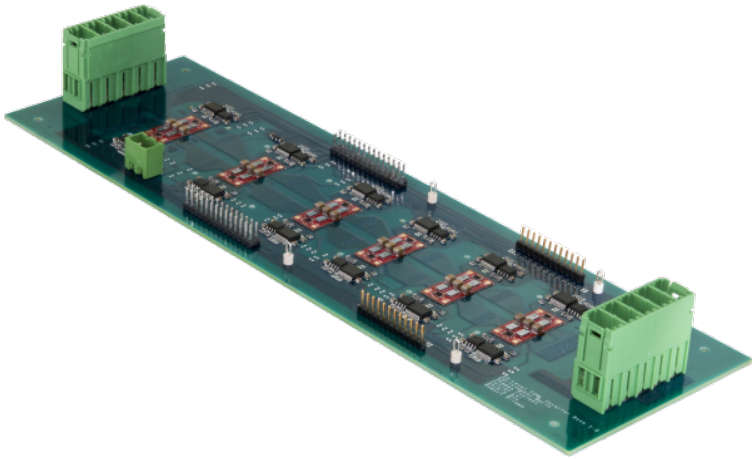


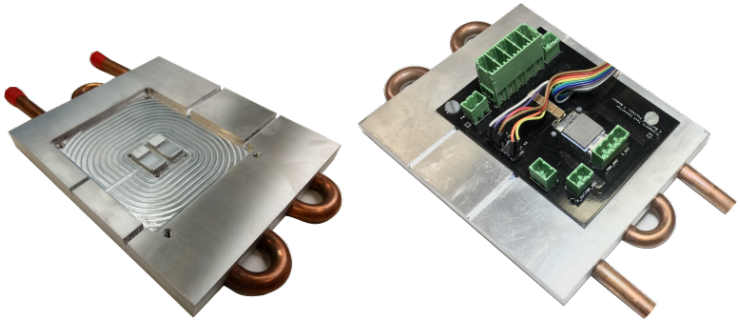
Figure 1.4: 13-level FCML converter used to demonstrate capacitor voltage balancing at high level count.

the design and performance of a single-phase, 13-level FCML inverter [9]. Taking the voltage bias dependent capacitance of ceramic capacitors into account, a design process for sizing ceramic capacitors to meet energy storage and current carrying requirements is outlined. The hardware developed in this chapter, and shown in Fig. 1.4, is reconfigurable and can be used to demonstrate a 3, 5, 7, 9, 11, or 13 level FCML inverter.

The demonstrated performance of this converter verified that passive balancing of capacitor voltages in the FCML converter could be extended to higher level counts than had been achieved as part of an intensive collaborative project with members of the author's research group over a nine-month period to develop a single-phase FCML inverter and energy buffer system [10]. In addition to passive balancing at steady-state, this chapter experimentally demonstrates capacitor voltage balancing under step load. This work provided the confidence to proceed with the 9-level FCML designs in [11,12].

3. Chapter 3: Analysis of GaN-based FCML Inverters Operating in Low-Temperature Environments

   Having demonstrated the robust balancing of precisely implemented FCML converters in Chapter 2, the question arose as to how GaN-based FCML converters could be applied in cryogenic or near cryogenic applications. Recent work had shown that the dc series resistance of certain GaN devices decreased by nearly an order of magnitude as the device was cooled from ambient to -120 °C [13], and there was interest in evaluating the impact of low-temperature operation on the performance of the complete converter. One of the primary drivers for this research was to investigate the potential



Cold plate Inverter mounted to cold plate

Figure 1.5: Three-level FCML inverter with cold plate for low temperature testing.

for the use of liquefied natural gas (LNG) as a combined fuel and heatsink in hybrid aircraft.

With an energy density 30 times that of batteries, and a per-unit energy cost of 50% that of jet A fuel, LNG offers the potential for enabling longer flight time and reduced environmental impact for vehicles like drones. Additionally, LNG is stored at a temperature of -160 °C and can serve as a heatsink for power electronics on the vehicle. In Chapter 4 a 3-level inverter is assembled and tested up to 1 kW. The converter was attached to a milled heatsink as shown in Fig. 1.5 to simulate the cooling configuration which could be used in an LNG-based system. This work [14] is one of the first demonstrations of a complete GaN-based power converter operating at near cryogenic temperatures and includes a detailed analysis of the impact of low temperature on each component based on a literature review, and on measurements taken personally and as part of the work supervised in [15]. It was found that operating at a temperature of -60 °C resulted in a 16% reduction in converter losses.

4. Chapter 4: Implementation of a Modular, Scalable, FCML-based Hierarchical Motor Drive

   The application of the FCML performance achieved in Chapter 2 and Chapter 3 into an aviation propulsion system requires the integration of single-phase converters into a 3-phase motor drive system. Chapter 4 of this dissertation presents the design and implementation of an FCML-based drive system which has been developed with a specific focus on electric and hybrid aircraft which are motivating the development of high-power-density electric propulsion systems. In particular, this work includes the development of high-density electric machines.

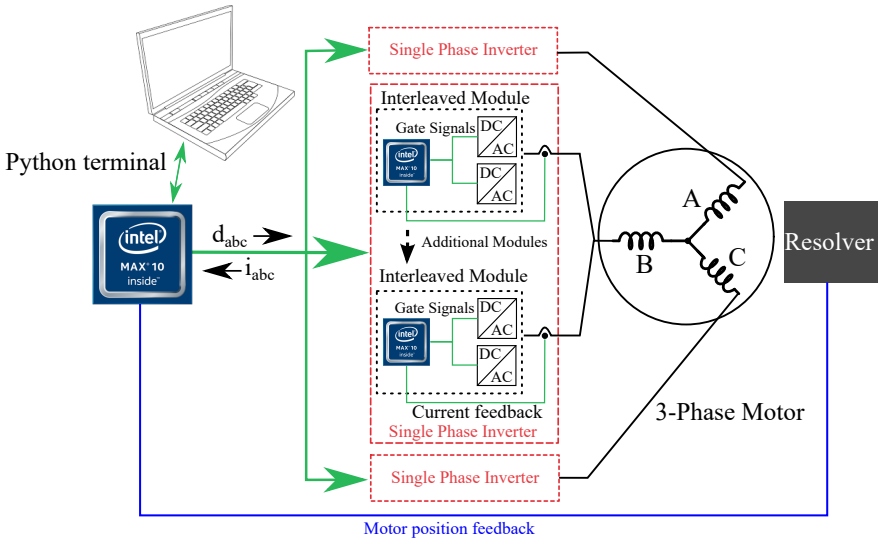


Figure 1.6: Structure of FCML-based motor drive system.

Recent work has shown that high-pole-count, permanent magnet synchronous machines offer some of the highest power densities available with known machine architectures [16]. As will be discussed in this chapter, the efficiency of a low inductance electric machine relies on the availability of a low-THD drive in order to maintain its efficiency. In a traditional 2-level drive design, low THD is accomplished through the use of of a large filter stage, but this approach reduces the power density of the drive and the overall propulsion system. FCML converters are well suited for use with high-density electric machines because they offer both high power density and low THD simultaneously. To address these needs, the drive in this work is tailored for use with permanent magnet synchronous machines.

In addition to power density, the modular drive system shown structurally in Fig. 1.6, also seeks to address the need for reliability required in aviation applications by providing the potential for redundancy in the event of a component failure. Furthermore, by addressing the issues associated with current sharing even in the presence of modest hardware mismatch, this drive architecture allows for a range of applications to be addressed by configuring multiple optimized, flight-certified modules in parallel to meet the application power requirements. This chapter includes results for up to 3 FCML modules operating in parallel, in addition to the operation of the drive running at a fundamental frequency of 1.6 kHz and driving a 32-pole permanent magnet machine up to 6,000 RPM at 2.8 Nm of torque.

CHAPTER 2

EVALUATION OF CAPACITOR ENERGY DENSITY AND EFFICIENCY FOR ENERGY BUFFERING APPLICATIONS

2.1 Motivation for Large Signal Capacitor Characterization

Conversion between DC and AC electric power using inverters or power factor correction (PFC) rectifiers, requires energy buffering to balance the instantaneous power difference between the two systems. Figure 2.1 depicts the power imbalance between DC and AC energy transfer and the difference in energy which must be buffered over a full AC cycle. This challenge is often referred to as power pulsation decoupling or twice-line-frequency energy buffering in the literature and is present in all single-phase DC/AC and AC/DC converters [17, 18].

The simplest capacitive energy buffering strategy is the placement of a large capacitor across the DC bus. The energy which must be stored in the DC bus capacitor (W_{buffer}) each line cycle is determined by the converter average power (P_{ave}) and the AC frequency (f_{line}), and can be expressed as

$$W_{buffer} = \frac{P_{ave}}{2\pi f_{line}}. \tag{2.1}$$

This energy will be stored in a capacitance (C) by rippling the voltage between some maximum (V_{max}) and minimum (V_{min}) value during each line cycle. For an ideal capacitor, the energy stored over this voltage range can be calculated as

$$W_{buffer} = \frac{1}{2}CV_{Cmax}^2 - \frac{1}{2}CV_{Cmin}^2. \tag{2.2}$$

Assuming a constant value of capacitance, and defining V_{avg} as the arithmetic average of V_{max} and V_{min}, this result can be equivalently stated as

$$W_{buffer} = C * V_{avg} * \Delta V. \tag{2.3}$$

Many practical applications impose very strict ripple requirement on the DC bus voltage, so the voltage ripple ΔV is typically limited [19]. To meet this ripple requirement and the

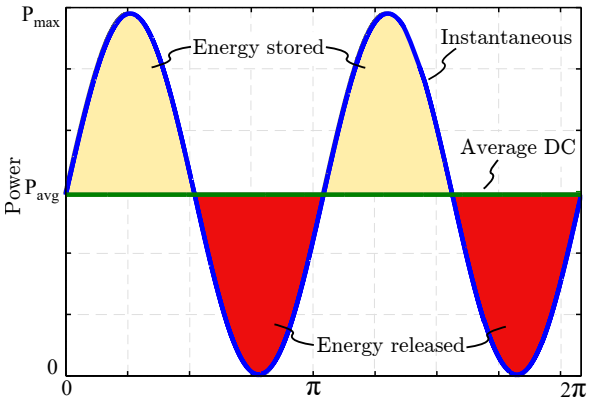


Figure 2.1: Comparison of instantaneous power presented by single-phase AC at twice the line frequency and the average DC power over one power line cycle.

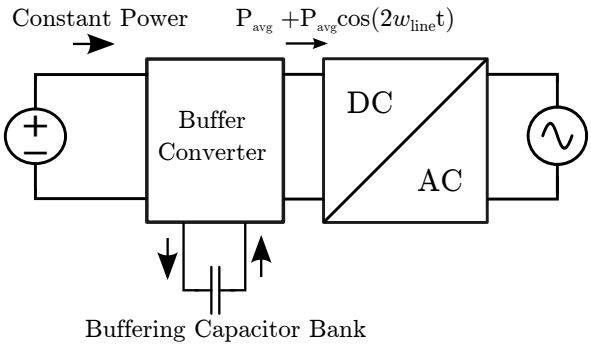


Figure 2.2: Energy buffering circuit of single-phase inverter.

accompanying energy storage requirement, a large capacitance is typically required on the DC bus. Additionally, certain applications, such as power supplies for telecommunication and computing, typically impose hold-up time requirements where sufficient energy storage must be maintained to continue uninterrupted power delivery in the event of a short-term (e.g., one or a few line cycles) voltage disturbance. The energy storage requirements for such applications are typically significantly higher than for twice-line-frequency buffering.

Historically, designers have used electrolytic capacitors for energy buffering because of their relatively high energy storage density and relatively low cost. Unfortunately, electrolytic capacitors pose concerns in long-life applications because of the use of a wet electrolyte which evaporates with age. Electrolytic capacitors are also lossy during charging and discharging compared to other technologies [20]. When long system life is important, designers have the option to use capacitors with dry dielectric which will not evaporate such as film or ceramic capacitors. Film capacitors exhibit lower energy density than electrolytics which results in a trade-off between density and the lifespan of the completed system.

In contrast to electrolytic and film capacitors, multilayer ceramic capacitors (MLCCs) have a dry dielectric and moderate energy density. A significant drawback of MLCCs is that they have historically been comparatively costly and they are limited in size due to the fragile nature of ceramics. Thus, although ceramic capacitors exhibit high energy storage density per unit of volume, the accumulation of sufficient capacitance for passive energy buffering in a single package has been challenging due to cost and mechanical constraints. Additionally, the capacitance of MLCCs suitable for energy buffering also changes with DC bias voltage, aging, temperature, large signal amplitude, and frequency [8, 21].

The effective energy density of capacitors can also be improved dramatically by decoupling the energy storage and voltage regulation requirements of buffering as is done in [7, 10, 17–19, 22–28]. These systems interface the buffering capacitance to the DC bus through a power converter, thereby allowing the capacitor voltage to vary over a wider range while maintaining a constant DC bus voltage. A basic schematic of an energy buffering architecture is shown in Fig. 2.2. Such power buffering techniques enable the use of thin film and MLCCs because smaller capacitance values are needed as compared to a passive buffer comprised of a capacitor connected directly to the DC bus. Moreover, as will be shown, MLCCs offer comparable or higher energy density than film or electrolytic capacitors when used in active energy buffering applications.

A great deal of research has been done to characterize the performance of capacitors under small signal operation [29–31]. A key contribution of this work is the analysis and experimental verification of the performance of commercially available capacitors operating with large voltage swings. Although the focus of this work is twice-line-frequency energy buffering, many other applications use capacitors in large voltage swing operation to store and transfer energy. The design of switched-capacitor converters [11, 32–34] (especially soft-charging converters [35,36]), requires a knowledge of the practical energy storage capability of MLCCs operating with wide voltage swing at high frequencies. In this work, we use experimental and analytical approaches to study the actual energy storage capability of various capacitors in detail, and have included test data from a range of capacitor technologies.

The remainder of this chapter is organized as follows: Section 2.2 discusses the proper method of evaluating the energy stored in a ceramic capacitor and how manufacturer provided data sheets can be used to obtain an estimate of energy storage. Section 2.3 discusses the experimental setup which has been used to test the energy storage and power loss of a wide variety of capacitors. Section 2.4 provides analysis of the measured data, highlighting energy density results across capacitor technologies. Section 2.5 includes an example of how the information in this chapter can be used in the design of an active power buffer. Section 2.6 summarizes the contributions of the chapter.

2.2 Large Voltage Swing Characteristics

2.2.1 Fundamentals of Ceramic Multilayer Capacitors

There are three classes of ceramic dielectrics defined per IEC/EN 60384-1. The three main classes of ceramic capacitors are tailored for a range of operating temperatures and des-

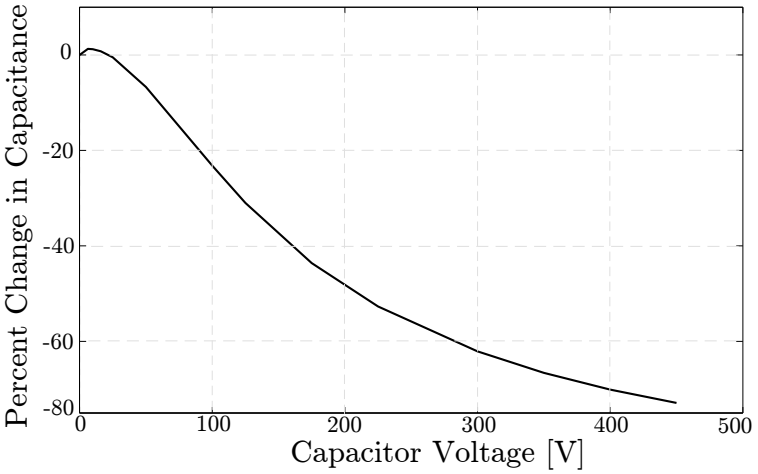


Figure 2.3: Plot of capacitance change vs. bias voltage for TDK CKG57NX7R2J474M500JH capacitor [39].

ignated by a three-character code which indicates the minimum operating temperature, maximum operating temperature, and the deviation in capacitance over the temperature range respectively [21].

Capacitors with the temperature class designations of NP0, CG, and C0G employ Class I dielectrics. Class I ceramics are paraelectrics which have dielectric constants that are stable with temperature, DC bias, and capacitor age. Hence these devices are unaffected by changes in DC operating point as well as temperature and capacitor age. Class I capacitors also have low loss and therefore high quality factor. These characteristics make Class I devices well suited for resonant and precision circuits. The main drawback of Class I ceramics, in energy buffering applications, is that they have a low relative permittivity (ϵ_r) of 15-100, and therefore have low energy storage density [21, 37, 38].

Barium titanate-based ($BaTiO_3$) Class II ceramic dielectrics are ferroelectric, with relative permittivities in the range of ϵ_r = 2000-4000, and are the focus of this work. One drawback of Class II ceramics is that their permittivity, and hence the capacitance of the device they are used in, decreases significantly with applied electric field [31]. This decrease in permittivity under electric field saturation is analogous to the decrease in relative magnetic permeability exhibited by magnetic materials under high magnetic fields.

Figure 2.3 shows the manufacturer's specified capacitance for a Class II device designed for 450 V operation. It can be seen that the capacitance can decrease by as much as 78% at the rated voltage compared to the value at a bias voltage of zero. Some examples of Class II temperature designations include X8R, X7R, X5R, and X6S. In practice, it is found that energy storage in MLCCs increases approximately linearly with voltage, instead of quadratically as one would expect if the dielectric permittivity were independent of voltage

[37].

Class III ceramic dielectrics have an even higher relative permittivity than Class II, with values of up to 50,000. However, along with this high initial permittivity, Class III devices also exhibit higher variation in capacitance values with temperature, voltage and age than Class II devices [31]. Hence, although Class III capacitors typically have exceptional initial capacitance density, they are not ideal for energy storage.

2.2.2 Calculation of Energy Storage Density

In order to account for the voltage dependence of a ceramic capacitor as the capacitor is charged from V_{min} to V_{max}, the energy stored in the capacitor (W_{stored}) can be defined as

$$W_{\text{stored}} = \int_{q_{\text{min}}}^{q_{\text{max}}} v \; dq, \tag{2.4}$$

where q is the charge in the capacitor. Using the substitution

$$dq = C(v) \; dv, \tag{2.5}$$

(2.4) can be rewritten as

$$W_{\text{stored}} = \int_{V_{\text{min}}}^{V_{\text{max}}} C(v) v \; dv. \tag{2.6}$$

It is important to note that C is now a function of voltage, and V_{min} and V_{max} are the limits of the voltage ripple imposed on the capacitor. It can be seen that, if C is independent of v, then the integration of (2.6) will yield (2.2).

Equation (2.6) is idealized in that it does not take into account the energy lost due to capacitor non-idealities during charging or discharging. The dominant capacitor losses are usually combined into an equivalent series resistance (ESR), so the energy required to charge the capacitor may be approximated in terms of losses and W_{stored} as

$$W_{\text{charge}} = W_{\text{stored}} + i_{\text{RMS}}^2 \; R_{\text{ESR}} \; T_{\text{cycle}}, \tag{2.7}$$

where i_{RMS}, R_{ESR}, and T_{cycle} are the RMS capacitor current, the equivalent series resistance, and the buffering period respectively. Equation (2.7) can be alternatively stated as

$$W_{\text{charge}} = W_{\text{stored}} + W_{\text{loss}}, \tag{2.8}$$

where W_{loss} is the loss incurred over the complete charge and discharge cycle. The ESR in

(2.7) represents device physical series resistance and parallel leakage as well as the hysteretic losses which result from a realignment of the electrostatic domains within the dielectric. The hysteretic losses are of special interest because they are dependent on frequency and potentially the voltage bias at which the capacitor is operated [8].

2.2.3 Characterization of Capacitor Performance

Round-trip efficiency is an important parameter in the evaluation of any energy storage system. The capacitor full-cycle energy storage efficiency is defined as the ratio of the energy extracted from the capacitor during discharge to the energy supplied to charge the capacitor, or equivalently

$$\eta = \frac{W_{\text{charge}} - W_{\text{loss}}}{W_{\text{charge}}} \times 100\%. \tag{2.9}$$

As discussed in the Section 2.1, energy density is also of primary importance in energy buffers and defined to be

$$C_{\text{Density}} = \frac{W_{\text{charge}} - W_{\text{loss}}}{\text{Capacitor volume}}. \tag{2.10}$$

Another capacitor characteristic used in some applications is the quality factor, or Q factor, of the capacitor. This characteristic normalizes the energy stored in the capacitor (or any resonant system) by the amount of energy lost per cycle [40]. The Q factor can be defined as

$$Q = \frac{2\pi \times (W_{\text{charge}} - W_{\text{loss}})}{W_{\text{loss}}}. \tag{2.11}$$

2.3 Experimental Measurement of Energy Storage

As the preceding discussion has shown, it is important to accurately calculate the energy storage of capacitors and MLCCs in particular. We have therefore performed detailed experimental characterization of a number of capacitors of different voltage ratings, dielectrics and packages under large signal, voltage swing. This testing strategy also enables an accurate assessment of losses in energy buffering applications with large signal conditions so that hysteretic and other second-order losses are properly represented [8]. In order to equitably select a group of test devices, the basic specifications for thousands of ceramic, electrolytic, metalized polyester, and metalized polypropylene capacitors were mined from supplier data. The energy storage density for each device was calculated based on the volume, capacitance at zero bias, and rated voltage of the devices using equation (2.2). It should be pointed out that this is a simplification required to narrow the scope of the project as one of the main

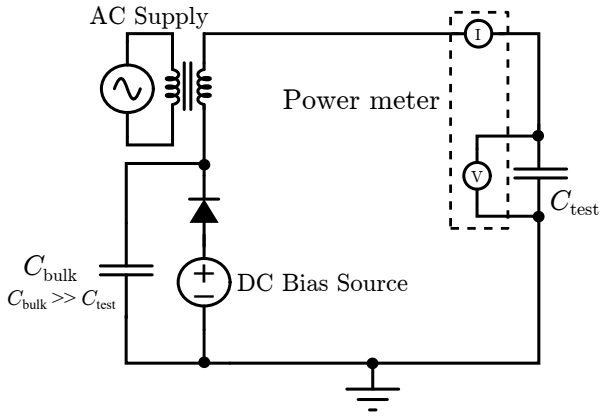


Figure 2.4: Capacitor test schematic.

Table 2.1: Equipment used in capacitor experimental test circuit.

Label	Instrument
DC Bias Source	Keysight N8937A
Power meter	Yokogawa WT3000E
Power Analyzer	Keysight PA2201A
AC Supply	Pacific Smart Source 112-AMX
Isolation Transformer	Schneider Electric Cat. No: 151F

points of this work is that (2.2) does not accurately capture energy storage. It is possible that the characteristics of different dielectrics may yield different energy storage densities at operating voltage. To address this issue, the highest density devices of each dielectric technology and voltage ratings of 50, 100, 250, 450, and 630 V were selected. In some instances the highest density capacitors were devices with individual capacitances which were too small for practical energy buffering applications. In these cases, a device with slightly lower energy density but a capacitance of 1 μF or greater was typically chosen.

A schematic for the experimental test circuit is shown in Fig. 2.4 along with a list of the hardware used for implementation in Table 2.1. This test configuration was capable of varying both the AC voltage ripple amplitude and DC voltage bias of the capacitors. To increase measurement accuracy and average tolerances between capacitors, the capacitors were typically tested in sets of 6 or more. A photo of the test equipment and capacitor test holder is shown in Fig. 2.5.

During the testing of the film and ceramic capacitors, the voltage was cycled from 0 to the rated voltage with an average value of one-half the rated voltage. Thus, the dc bias was 50% of the rated voltage and the ac peak amplitude was 50% of the rated voltage. This replicates the waveform imposed when the capacitor is used in an active twice-line-frequency unipolar buffer application. In the case of the electrolytic capacitors this full voltage range ripple far exceeded the current rating of the devices. The electrolytic capacitors were instead rippled between the rated voltage and the lowest voltage possible such that the manufacturer-defined RMS current rating was not exceeded. The integration function of the Yokogawa WT3000E meter was used to measure the energy flowing into and out of the capacitor. This work was specifically focused on determining the performance of the capacitors in twice-line-frequency applications, so the capacitors were cycled at 120 Hz. During testing, an integration of energy flowing into and out of the each device was performed over 5 separate 30 s intervals. The

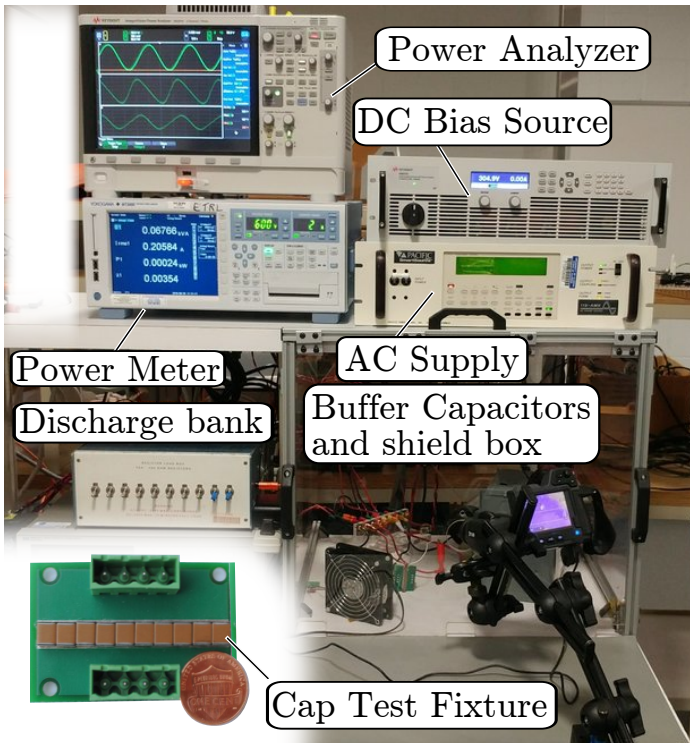


Figure 2.5: Experimental test setup and capacitor test fixture with 10 MLCCs.

standard error for each set of five measurements is included with the full data in Table A.1. This approach thus computed the average energy stored over 3600 cycles, and nullified any phase-induced measurement errors. With the integral of power given by the meter in watt-hours, and the integral of current given in amp-hours, a unit conversion then yields energy transferred into and out of the capacitor over a complete cycle.

This setup provides an accurate method of measuring the power flow into and out of the capacitors to determine the performance of the devices when operating over a large voltage swing as in energy buffering applications. Provided the appropriate transformer is used, the Pacific Smart Source AC supply is capable of cycling power through the capacitors at frequencies from 20 Hz to 5 kHz to test capacitors for applications such as switched capacitor converters and high-frequency motor drives.

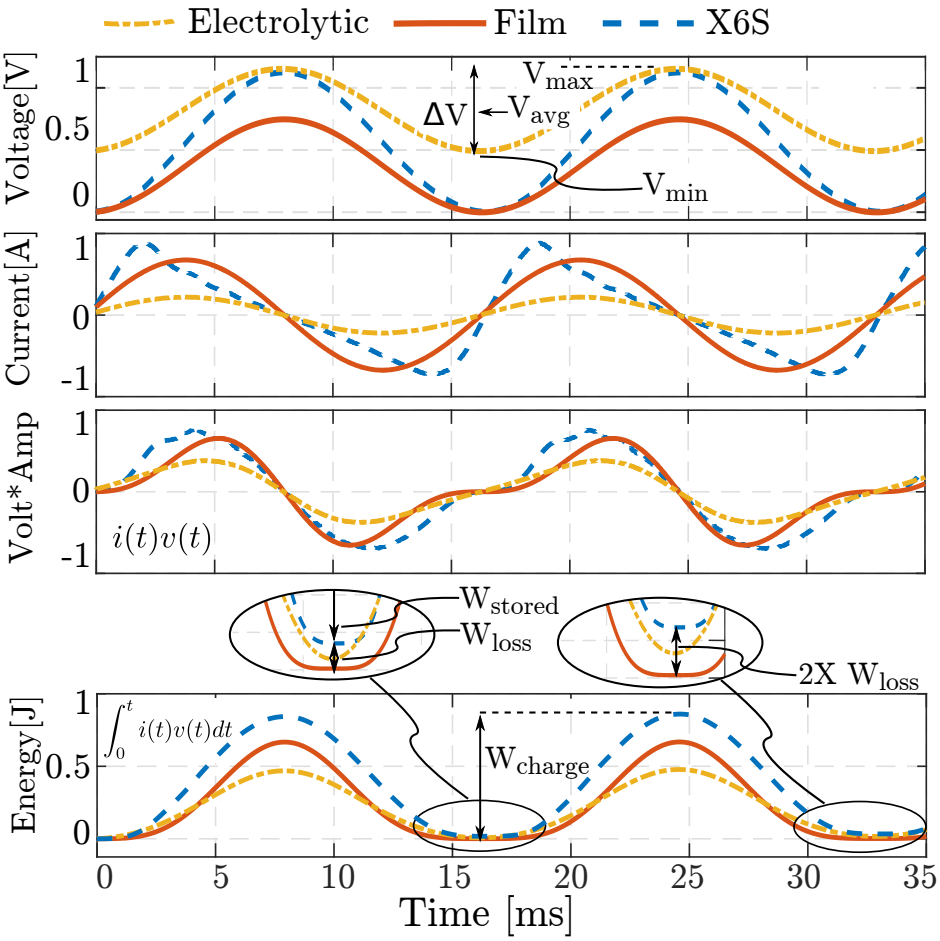


Figure 2.6: Experimental test waveforms for electrolytic, X6S ceramic and metallized polyester capacitors.

2.4 Capacitor Performance Evaluation

2.4.1 Behavior of Capacitor Energy Storage under Large Voltage Swings

Figure 2.6 compares the experimental charge and discharge waveforms for an X6S Type II ceramic capacitor a bias-independent film capacitor and an electrolytic capacitor. All three capacitors have sinusoidal AC voltage applied, but it can be seen that the bias-dependent capacitance of the X6S capacitor leads to a linearly increasing/decreasing current while the current drawn by the other two capacitors is sinusoidal. The quantities referenced in (2.4) through (2.8) are labeled as well. Of particular interest is the offset between the minimum energy after the first and second cycle and the numerical zero value. This measurement of W_{loss} shows the difference between the energy extracted from the capacitor and the energy which would theoretically be available if the capacitor was 100% efficient.

Table 2.2: Measured and calculated energy stored per cycle for Type II ceramic capacitors.

Approach	X6S 2.2 uF	X7R 0.47 uF	X5R 0.22 uF	X7T 2.2 uF	Avg. Error
Measured (mJ)	66.9	21.4	11.4	84.3	
Calculated using $C(0V)$ (mJ)	203.9	46.1	23.5	194.4	+80.58%
Calculated using $C(450V)$ (mJ)	36.1	7.6	3.9	52.6	-74.84%
Calculated using $C(v)$ (mJ)	58.9	20.6	10.6	81.3	-6.84%

For a first high-level design iteration, it is helpful to estimate energy storage based on manufacturer specified capacitance. Table 2.2 shows three different estimations of capacitor energy storage at rated voltage based on data sheet specifications. For each device, the manufacturer-provided capacitance vs. voltage data is scaled by the ratio of the measured to nominal capacitance of the test devices at zero bias voltage. This reduces the impact of tolerance and aging on the results of Table 2.2.

The first data row of Table 2.2 is the experimentally *measured* energy stored by the capacitor minus losses. This value is then compared to the energy storage *calculated* based on the nominal capacitance value and the manufacturer supplied capacitance at full voltage using (2.2), in rows 2 and 3 respectively. It can be seen that both of these methods are poor estimations of experimentally measured capacitor energy. The fourth row of Table 2.2 shows the energy storage calculated using a midpoint Riemann sum over $C(v)$ from the manufacturer data sheet. This approach applies (2.6) to accurately calculate the stored energy for a changing capacitance value while taking the losses of (2.7) into account. The last column on the right shows the error between a given method and the measured energy storage of the capacitor. This value is averaged over all capacitors.

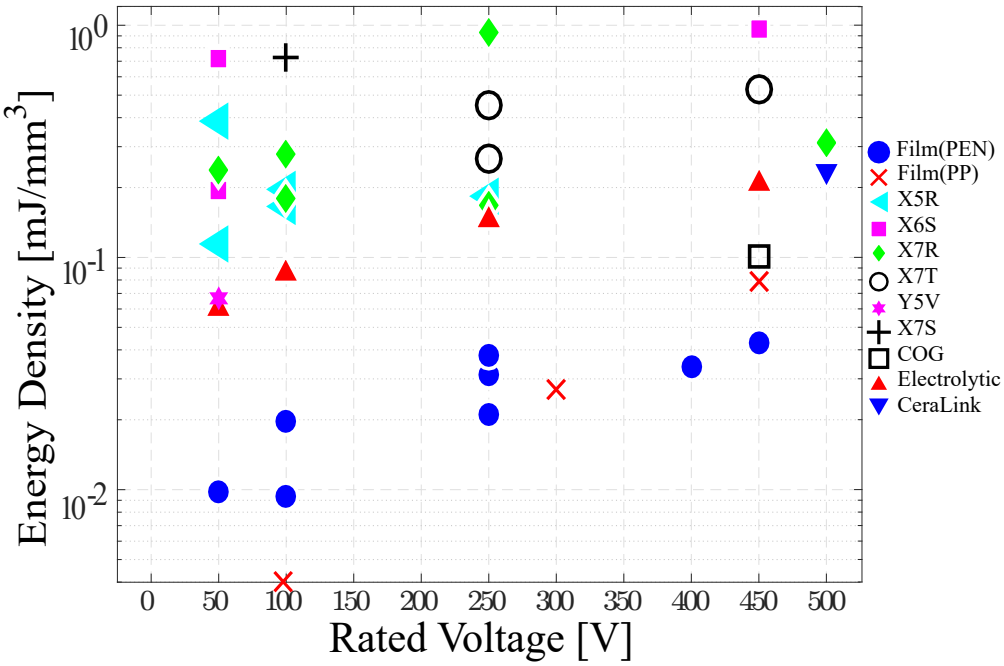


Figure 2.7: Measured capacitor energy density with film capacitors ranking among the lowest energy density and ceramics ranking among the highest.

It is evident that the use of a constant nominal capacitance over the full voltage range leads to very inaccurate energy storage estimation when device capacitance is bias dependent as it is in ceramic capacitors. However, by performing piece-wise integration using the manufacturer-provided capacitance data, the energy stored in the capacitor between two voltage levels can be estimated with relatively small (i.e., $< \pm$ 10%) error. This accuracy is contingent on the accuracy of the manufacturer-supplied capacitance derating with bias. It is worth noting that the energy storage capabilities of all ceramic capacitors are underestimated numerically. It is suspected that this is due to ESR losses being overestimated.

2.4.2 Full Comparison of Devices

It is also insightful to see how trends in energy density develop over a broader range of capacitor technologies. The complete list of capacitors tested along with detailed test data is provided in Appendix A. Shown in Fig. 2.7 is a plot of measured capacitor energy density versus rated voltage, for metal film, ceramic, and electrolytic capacitors, as indicated in the legend.

It is observed that MLCCs generally achieve the highest energy density under this test scenario. It should be re-emphasized that the electrolytic capacitors tested here were current

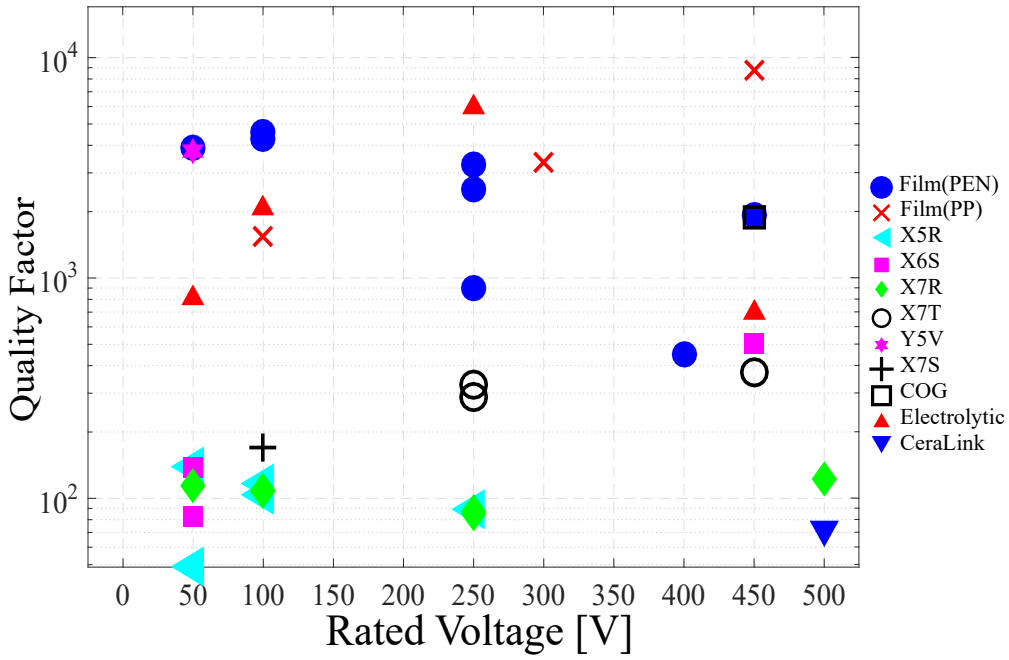


Figure 2.8: Measured capacitor quality factor showing that film capacitors rank among the highest in quality factor.

ripple limited, meaning that although they can fundamentally store more energy than what is shown here, not all of that energy can be effectively *transferred* at twice-line-frequency without causing excessive loss (and heating). While the metal film capacitors (metalized polyester and metalized polypropylene) evaluated in this study have relatively low energy density, their low loss is readily apparent in Fig. 2.8, which shows the capacitor Q factors versus voltage ratings. It should again be noted that the Q factor here is as defined in (2.11), and is derived from measured energy loss and storage capability.

Cost is another important consideration in system design. Figure 2.9 explores the relationship between the capacitor normalized energy storage cost and the device energy density over the range of capacitors tested. With X-axis of energy density inverted from the normal direction of increase, figure-of-merit components are plotted toward the lower left of the figure. It is of special interest to see that the cost of MLCCs is currently an order of magnitude higher than that of electrolytic capacitors. However under the constraints of full range voltage ripple, they are able to store an order of magnitude more energy on a per-cycle basis. Additionally, MLCCs generally come in smaller form factors and in lower capacitance values than metal film and electrolytic capacitors, therefore requiring a large number of individual capacitors to be paralleled. While this may lead to reliability and manufacturing challenges, it also enables flat and customizable form factor, which may be important in some applications.

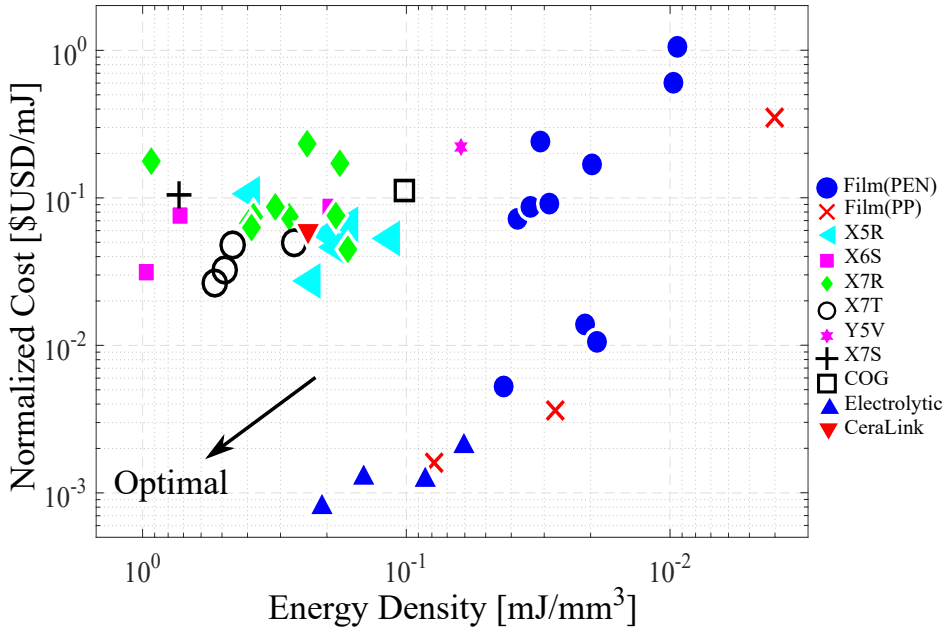


Figure 2.9: Normalized cost of energy storage vs. energy storage density. 10k quantity assumed. Under full amplitude voltage ripple, ceramic capacitors have up to an order of magnitude higher energy density than electrolytics. This is at the expense of over an order of magnitude higher cost [41, 42].

Figure 2.10 displays Q factor versus energy density for all capacitors evaluated in this study. For the twice-line-frequency buffering applications considered here, the MLCCs again stand out for their high energy density, and acceptable Q factor. It should be noted that at higher frequencies the trade-off between Q factor and energy density may be different, leading to other preferred capacitor technologies.

2.5 Energy Buffering Converter Design

The preceding sections have evaluated the large-signal performance of a range of capacitor technologies and have shown that MLCCs have some of the highest energy density among the non-electrolytic devices. As discussed, this trait comes with the complication that the capacitance of these devices changes with DC bias voltage. In order to utilize the results presented in Section 2.4 in the design of an active energy buffer, it is important that the design of the power converter in which the capacitors will be used be tailored to the capacitor characteristics. It will be shown that the power density of the system can also be improved by rippling the voltage of the buffer capacitors at a voltage lower than the capacitor's maximum specified voltage. In this design discussion, the focus will be on minimizing overall system

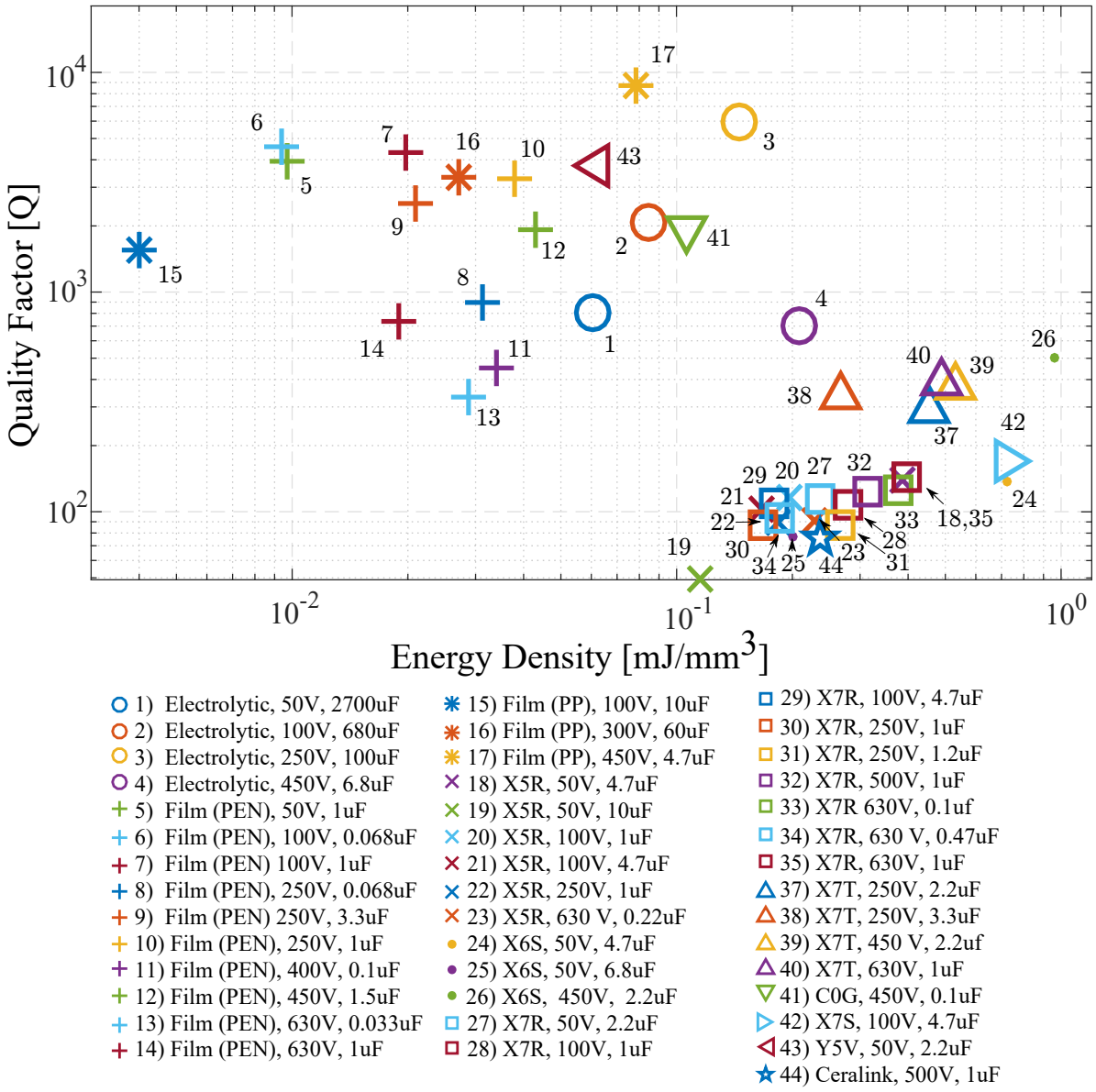


Figure 2.10: Capacitor Q vs. energy storage density.

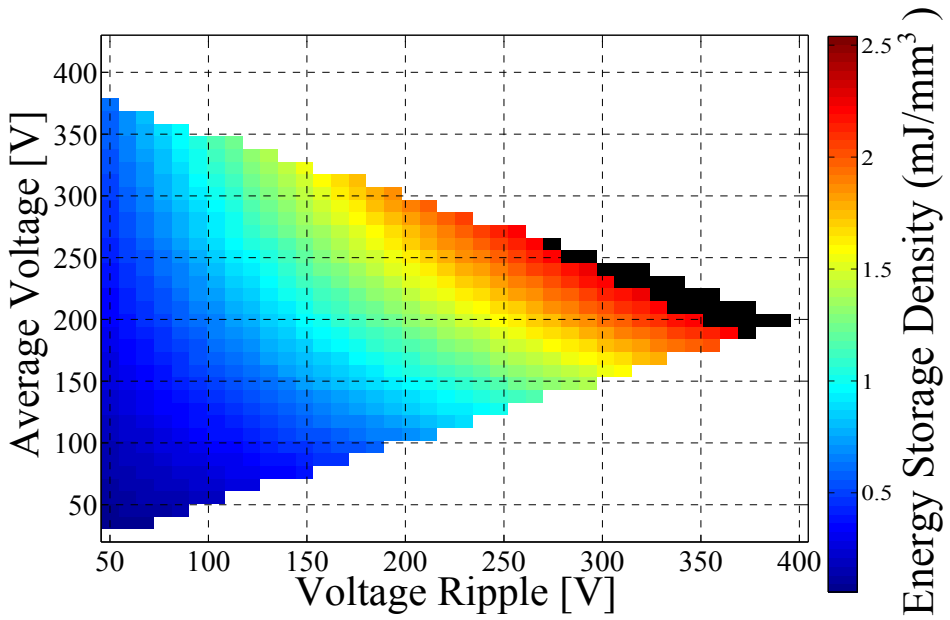


Figure 2.11: Energy buffering density for a bias-independent 2.2 μF capacitor with the same dimensions as #23. Black region indicates top 10% of energy density. It can be observed that, under the constraint of the capacitor and switch voltage ratings, the maximum energy density is obtained by maximizing the voltage ripple and maintaining the highest possible voltage.

volume, but this strategy can be incorporated into a more comprehensive optimization with specific cost and efficiency goals.

2.5.1 Impact of Voltage Ripple Range on Capacitor Energy Storage Density

In order to understand the implications of bias dependent capacitance on the energy buffering system, it is helpful to first compare the energy storage density of a bias-independent capacitor and an MLCC bias dependent ceramic capacitor. As is highlighted by (2.3), it is typically advantageous to operate energy buffering capacitors such that the ripple and DC average voltage are optimized with respect to the constraints imposed by the peak voltage limits of the system. Assuming unipolar voltage ripple, the ripple is constrained to,

$$\frac{\Delta V}{2} < V_{pk} - V_{avg}. \tag{2.12}$$

To maximize density, V_{pk}, should be the highest voltage within the system limits. For a system using bias-independent capacitors, the highest energy density for a given V_{avg} is

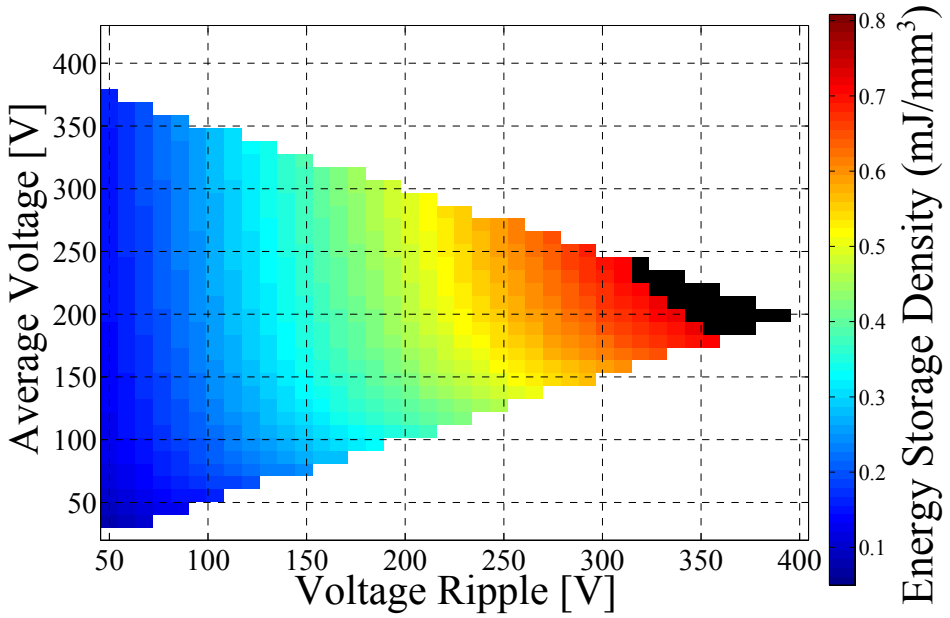


Figure 2.12: Energy buffering density for the 2.2 μF, 450V, X6S capacitor #26. Black region indicates top 10% of energy density. In the bias-dependent buffer configuration note that the maximum energy density still occurs at high voltage ripple, but the average voltage is shifted slightly down. Exploring the implications of this shift is the focus of this section.

calculated as,

$$W_{buff} = 2CV_{avg} * (V_{pk} - V_{avg}), \tag{2.13}$$

which implies that the maximum energy can be stored by operating with $V_{avg} = \frac{V_{pk}}{2}$. [1]

Figure 2.11 plots energy storage density, as a function of capacitor average voltage and ripple for a capacitor with a voltage independent dielectric. This "ideal capacitor" is assumed to have a value of 2.2 μF, and a 2220 SMT package. It can be seen that the highest energy density tends to be located at high ripple voltage and the highest average voltage which can be accommodated by the system. However, the optimal operating voltage range for systems based on real (bias-dependent) MLCCs is not as clear due to bias dependent capacitance.

Figure 2.12 plots the corresponding energy density for the bias dependent 2.2 μF X6S ceramic capacitor enumerated as 26 in Fig. 2.10 and the Table A.1. The X6S ceramic is used for reference because it has the highest energy density of the evaluated MLCCs. Although the trend in Fig. 2.12 is similar to that in Fig. 2.11, it will be noted that the contours of equal energy density are more vertically aligned as opposed to the diagonally aligned equidensity lines in Fig. 2.11. This shows that the energy density of ceramic capacitors is reduced at high bias voltage. The absolute difference in energy density between the two plots is not

[1]The author especially thanks a journal reviewer for sharing their thoughts in articulating this concept.

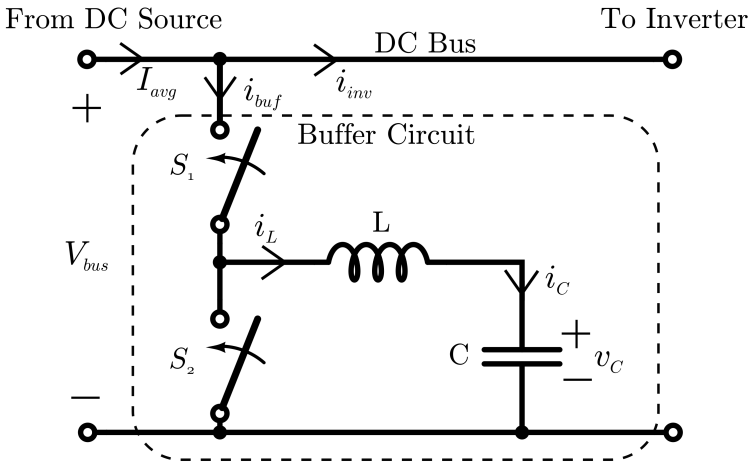


Figure 2.13: Bi-directional buffer converter schematic.

the focus of this comparison. Instead, the purpose is to compare the relative values of ripple voltage and average voltage that yield the maximum energy density in both cases.

In addition to identifying the average voltage and ripple at which the capacitor energy storage density is the highest, it is important to consider the capacitor operating voltage range which will minimize the volume of the entire buffer system. At least 50 different topologies have been proposed for energy buffering applications [17, 43]. These designs each represent tradeoffs between complexity, size, and performance, with different benefits and drawbacks. The full ripple port topology shown in Fig. 2.13 is a relatively simple and robust architecture which allows a large degree of flexibility in the capacitor DC bias and ripple voltage and has been utilized in a number of works [23, 24]. Because of its simplicity and broad design space, the full ripple port converter will be used in this work to illustrate the design of an energy buffering converter using ceramic capacitors.

It is clear that the minimum inductance requirement for continuous conduction mode, current rating, and losses for the full ripple port converter in Fig. 2.13 will change over the range of energy buffering average voltages and voltage ripple magnitudes shown in Fig. 2.11 and Fig. 2.12. These factors will each have an impact on the overall system density. The following design sequence outlines a general approach to minimizing the overall converter volume.

1. Determine maximum twice-line-frequency energy storage required for the application as specified by (2.1).

2. Model the voltage dependence of the capacitor technology to be used.

3. Develop a model for converter losses and volume as a function of the average voltage

and ripple of the buffering capacitors.

4. Iterate over the feasible range of average voltage and ripple voltage to determine system power density for each operating condition.

Section 2.5.2 through Section 2.5.4 will discuss this process in detail.

2.5.2 Calculation of Required Inductance and Current Stress

Because the inductor is one of the largest components in the converter, there is strong incentive to design the system in such a way that inductor volume is minimized. In order to simplify the optimization and comparison of buffering converter designs, it is helpful to have a defined relationship between converter input and output voltage so that input and output current flow and power can be defined. This constraint can be guaranteed by designing with a large enough inductance that the converter operates in continuous conduction mode (CCM) with non-zero current flow through the inductor at all times. Under this condition, the relationship between the bus voltage (V_{bus}) and the capacitor voltage (v_C) for the converter of Fig. 2.13 is

$$d_{S1}(v_C) = \frac{v_C(t)}{V_{bus}}, \tag{2.14}$$

where d_{S1} is the instantaneous duty ratio of switch S_1. This relationship holds throughout the line cycle as the capacitor is charged and discharged from the constant voltage DC bus. At any point in the line cycle, the required duty ratio of the converter is simply the ratio of instantaneous capacitor voltage to bus voltage.

Although the limits of the converter duty ratio are known based on the bus voltage and intended capacitor voltage ripple range, it is helpful to calculate the instantaneous converter duty ratio over the line cycle so that instantaneous capacitor and inductor current can be calculated. With the DC bus voltage fixed, it is only necessary to determine the instantaneous capacitor voltage over the line cycle and the duty ratio follows directly from (2.14). Because capacitor voltage is determined by the charge stored on the capacitor, one method of determining instantaneous capacitor voltage is to integrate the capacitor current which must be enforced to meet buffering requirements.

Referencing Fig. 2.1 and Fig. 2.13, it can be observed that the current feeding the inverter (i_{inv}) takes the form

$$i_{inv}(t) = I_{avg} + I_{avg}\ \cos(2\omega t). \tag{2.15}$$

Equation (2.15) is the sum of the current supplied by both the buffer and the DC source. Assuming constant current and voltage from the DC supply, the buffer must supply a current

(i_{buf}) of

$$i_{buf}(t) = -I_{avg}\ \cos(2\omega t). \tag{2.16}$$

However the instantaneous buffer current is not equal to the instantaneous capacitor current, but instead to the buffer current scaled by the converter duty ratio

$$i_C = i_L = \frac{i_{buf}}{d_{S1}}. \tag{2.17}$$

As seen from (2.17), the instantaneous duty ratio is required to determine the capacitor current; however, the instantaneous capacitor voltage and duty ratio are unknown without the capacitor current. Thus it is not possible to calculate the capacitor current directly from the buffer current alone and an iterative approach must be used to combine (2.15) through (2.17) to define the relationship between capacitor voltage and current.

The change in charge stored on the capacitor (Δq) is simply the integral of capacitor current (i_C) over time,

$$\Delta q = \int_0^{\Delta T} i_C dt. \tag{2.18}$$

The incremental change in voltage (Δv_C) is the change in charge divided by the buffer capacitance (C),

$$\Delta v_C = \frac{\Delta q}{C(v_C)}, \tag{2.19}$$

where the effective capacitance of $C(V_C)$ is a function of instantaneous capacitor voltage ($v_C(t)$). By extension, the capacitor voltage can be calculated at any point in the line cycle as

$$v_C(t) = \int_0^t \frac{i_C(\tau)}{C(v_C)} d\tau + v_C(0). \tag{2.20}$$

Equation (2.20) can then be rewritten in terms of converter current through substitution of (2.17) which yields the capacitor voltage over time as a function of i_{buf} and d_{S1},

$$v_C(t) = \int_0^t \frac{i_{buf}(\tau)}{C(v_C)\ d_{S1}(v_C)} d\tau + v_C(0). \tag{2.21}$$

Finally, (2.21) can be rewritten by substituting (2.14) to obtain

$$v_C(t) = \int_0^t \frac{i_{buf}(\tau)\ V_{bus}}{C(v_C)\ v_C(\tau)} d\tau + v_C(0). \tag{2.22}$$

Evaluating (2.22) in a piece-wise fashion will allow the computation of the capacitor voltage over a full line cycle, and hence the instantaneous converter duty ratio will be known. With

the duty ratio and buffer current waveform defined, (2.17) then allows for the capacitor current and inductor current to be calculated.

2.5.3 Inductor Volume

As mentioned, the previous relationships assume that the converter inductance is large enough to operate in CCM. For a given duty ratio d_{S1}, the minimum inductance required for CCM can be calculated as

$$L_{CCM} = \frac{V_{bus}(1 - d_{S1})d_{S1}}{\Delta I_L f_{sw}}, \tag{2.23}$$

where V_{bus} is the bus voltage, ΔI the peak-to-peak current ripple, and f_{sw} the converter switching frequency. It can be seen in (2.23) that L_{CCM} has a maximum value at a duty ratio of 50%. Thus, in order to determine the minimum inductor size for each average buffer capacitor voltage and ripple voltage shown over the axes in Figs. 2.11 and 2.12, it is necessary to determine the duty ratio closest to 50% which will be used during converter operation. Based on this duty ratio, the minimum inductance required to maintain continuous conduction can be determined.

In order to perform a minimization of the overall system volume, it is necessary to develop a model of inductor volume as a function of inductance and current rating. In practice, these two specifications are often combined into the energy storage (W_L) rating of the inductor as

$$W_L = \frac{1}{2} L I_L^2, \tag{2.24}$$

for use in preliminary design analysis [44]. When considering component volume, it is important to take into account both the thermal and magnetic saturation limit of the inductor. The inductor thermal limit will set the RMS inductor current rating, and the saturation limit will set the peak inductor current limit.

In a practical implementation, the inductor volume will be determined by component availability and will not be a continuous function, but will instead be a discretized function depending on available core sizes. As an example to illustrate the discrete nature of inductor volumes and ratings as well as overall trends, Fig. 2.14 plots the energy storage of the IHLP series of inductors from Vishay as a function of inductor volume. The linear fit of RMS energy stored (W_{RMS}) as a function of volume (V_L) is found to be

$$W_{\text{RMS}} \ [\text{mJ}] = 6 \cdot 10^{-4} \left[\frac{\text{mJ}}{\text{mm}^3} \right] \ * \ V_L \ \left[\text{mm}^3 \right]. \tag{2.25}$$

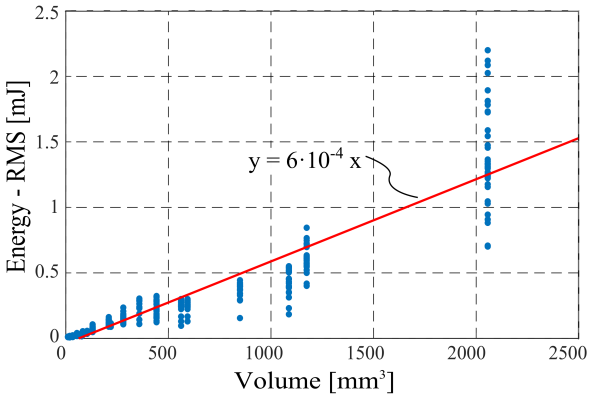


Figure 2.14: RMS energy storage as a function of inductor volume for the IHLP inductor series by Vishay [45].

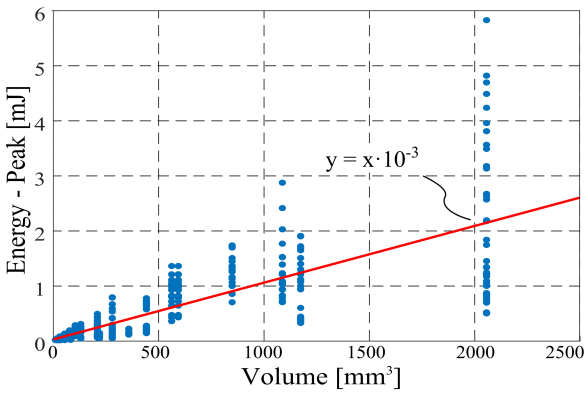


Figure 2.15: Peak energy storage as a function of inductor volume for the IHLP inductor series by Vishay [45].

While a linear fit is a rough estimation of energy storage, it provides an approximate estimate of the volume requirements of existing technology. In addition to following the RMS current ratings which set the thermal limits of the inductor, the peak current rating of the inductor must also be accounted for in order to avoid saturation. Figure 2.15 plots the inductor peak energy as a function of volume. The linear fit of peak energy storage as a function of volume is found to be,

$$W_{pk} \ [\text{mJ}] = 1 \cdot 10^{-3} \left[\frac{\text{mJ}}{\text{mm}^3}\right] \ * \ V_L \ \left[\text{mm}^3\right]. \tag{2.26}$$

It is evident that the peak energy storage for a given volume is higher than the RMS energy density. This is due to the smaller copper area and package needed to support short-term current peaks and maintain an acceptable temperature. What is not immediately evident is the ratio of RMS to peak current which the inductor will encounter for each design of voltage bias and ripple. Thus, in order to evaluate the energy density of a design, the volumes needed to meet the RMS and peak requirements are both calculated separately and the maximum volume is chosen for each operating condition.

2.5.4 Heatsink Volume

An important final step in developing a volumetric model of the converter is to consider the volume of the cooling hardware required to dissipate converter losses. Low converter efficiency results not only in higher energy loss, but in larger required volume for cooling the converter. In this analysis, dissipation of inductor losses were accounted for by heeding the RMS ratings of the inductors, as this rating generally does not assume any type of

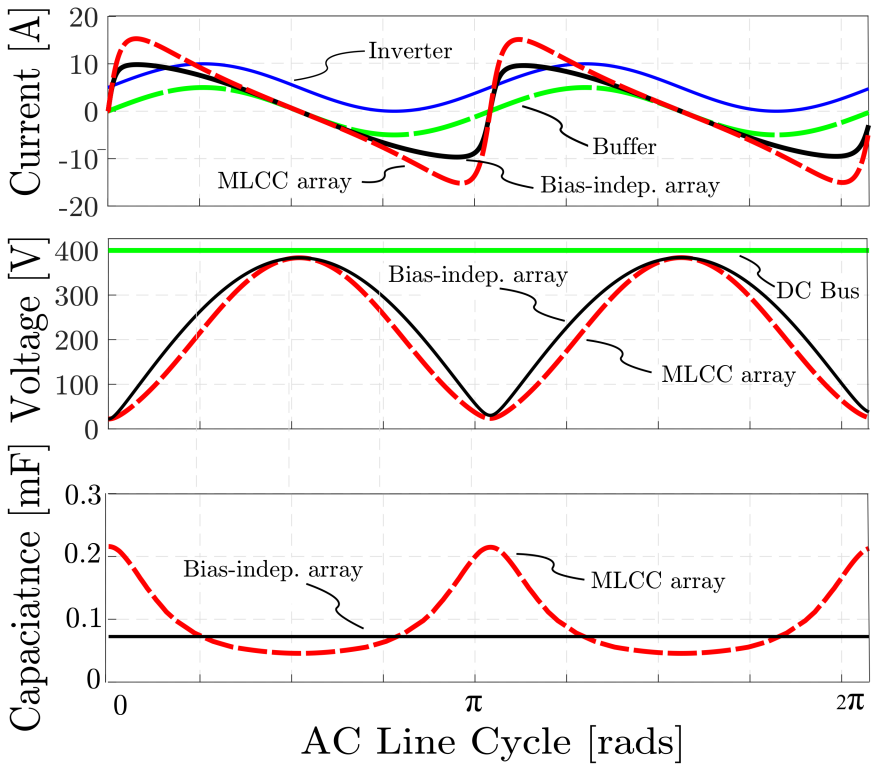


Figure 2.16: Operating waveforms for capacitor array, buffer and inverter. The peak currents of the MLCC array are significantly higher than the peak currents for an ideal capacitor array due to the large change in capacitance of the MLCC array over the line cycle.

heatsinking on the inductor. The other major source of losses occurs in the conduction and switching of the converter power switches. In this example the switch losses for a half-bridge built of GS66508P devices from GaN Systems switching at 120 kHz were calculated and averaged over a full line cycle using a standard loss model for conduction and switching losses [46, 47].

The heatsink volume needed to dissipate the energy lost in the switches will change depending on the cooling approach (i.e. whether natural convection, forced air, or liquid cooling are used). Air cooling provides a simple baseline on which to make comparisons between designs. A thermal admittance of $0.02 - 0.03$ W/(cm^{3}K) for highly optimized air cooled systems, and $0.005 - 0.01$ W/(cm^{3}K) for more standard extruded systems was identified in [44]. In this example a thermal admittance of 0.01 W/(cm^{3}K) was assumed as well as an ambient temperature of 30 °C and a maximum heatsink temperature of 100 °C, or 70 °C above ambient. Under these constraints, 1428 mm^3 of heatsink volume are required per watt of loss to provide adequate cooling. This estimate has also neglected the thermal impedance between the switching devices and the heatsink which would likely increase the

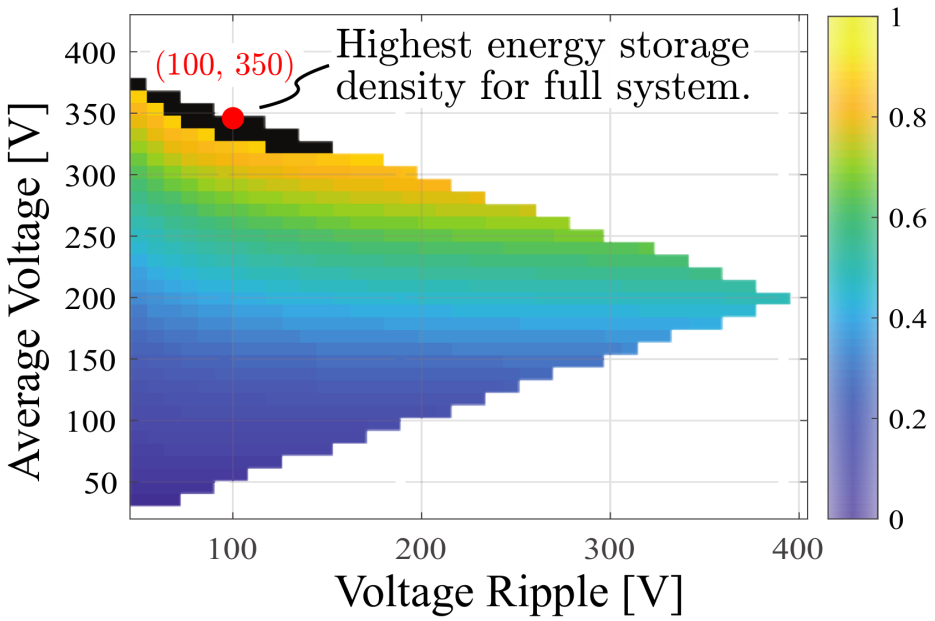


Figure 2.17: Normalized relative energy density over ripple and average voltage for a full system including bias-independent capacitors, inductor and heatsink. Black region indicates top 10% of density. It can be seen that the maximum energy density occurs at high average voltage.

required heatsink volume.

2.5.5 Impact of Voltage Ripple Range on Energy Storage Density of the Full Buffer Converter

In analyzing the impact of ceramic capacitors in energy buffering applications, it is first significant to note the differences between the operating waveforms of a buffer converter built using MLCCs and capacitors with voltage independent dielectrics. Figure 2.16 shows calculated values of the inverter current, buffer current, and capacitor current for one full cycle for both an ideal capacitor array and the MLCC capacitor array. In this example, both arrays are sized to ripple between equal voltage limits and store equal energy as required by (2.1) for a complete line cycle. Although the ripple limits of both capacitor banks are equal, the amounts of energy stored at each differential voltage are not equal. This is because at high voltage the MLCC array has a lower capacitance than the ideal capacitor and at low voltage the capacitance of the X6S capacitor is over 2x larger than the capacitance of the ideal capacitor.

The impact of this characteristic is clearly seen by comparing the three plots in Fig. 2.16. Considering the lower plot, it is seen that the capacitance of the MLCC array at the minimum

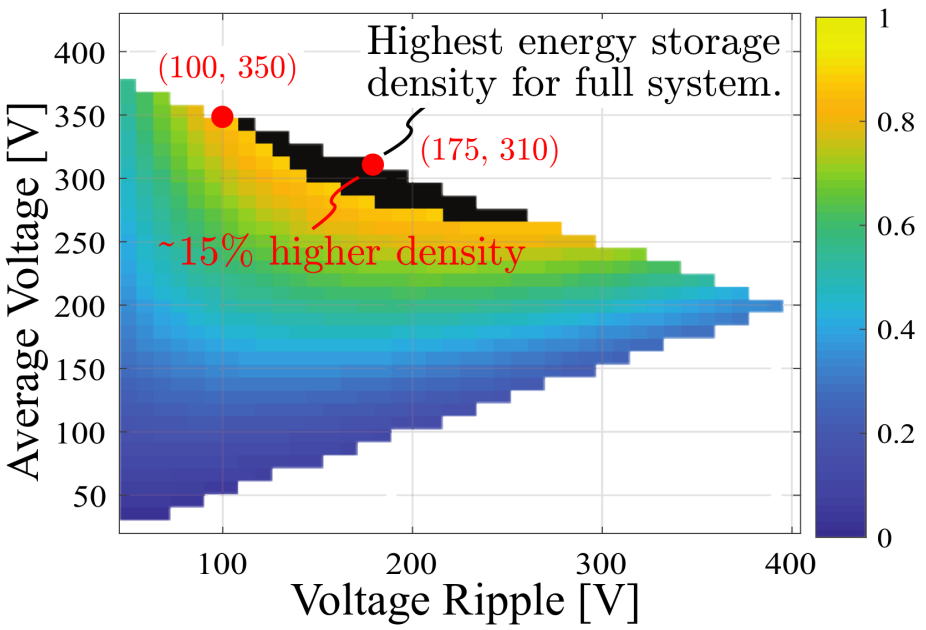


Figure 2.18: Normalized relative energy density over ripple and average voltage accounting for X6S MLCCs, inductor and heatsink. Black region indicates top 10% of density. It can be seen that the maximum energy density occurs at a lower average voltage of 310 V as opposed to the system using bias-independent capacitors which achieve optimal energy density at an optimal energy density of 350 V. Under the assumptions of this analysis, the system energy density can be increased ≈15% through operating at 310 V average as opposed to 350 V average.

capacitor voltage is over twice that of the ideal array. Thus, the dynamically changing capacitance of the X6S, MLCC capacitor array results in higher peak currents in the buffering capacitor and converter than occur for the bias-independent capacitor array. These higher peak currents translate into higher conduction and switching losses which must be taken into account in the overall optimization of the energy buffering system.

Combining the density impact of the MLCCs, the inductors, and the system cooling, it is possible to identify the buffering energy density which can be obtained for each value of buffering capacitor average voltage and voltage ripple. It should be emphasized that the purpose of this discussion is not to perform detailed loss or size calculations of power converters, but rather to inform readers of the assumptions made to determine the impact of MLCC capacitors on buffer converter power density. After totaling the volume contributions from Section 2.5.2 to Section 2.5.4 the overall power rating of the converter was divided by the volume to determine the effective system power density. The resulting density plots are shown in Fig. 2.17 and Fig. 2.18.

Figure 2.17 shows the plot of normalized system buffering energy densities which can

be achieved using the previously specified bias-independent capacitors and a unipolar, hard switched, ripple-port converter to implement a twice-line-frequency buffer. Similarly, Fig. 2.18 shows the relative energy density obtained for an active buffer developed using the X6S capacitors numbered 23 in Fig. 2.10.

It can be seen that the highest system-level energy density can be obtained by operating the bias-independent capacitors at 350 V average with a 100 V peak ripple, while the optimal average for the X6S capacitors is a 310 V average and a 180 V ripple voltage. Looking at the color gradient, it is evident that operating the X6S-based system at the same optimal ripple range as the bias independent system would result in an $\approx 15\%$ reduction in the power density of the system. This shows that there is a benefit to be obtained through taking the characteristics of the bias dependent capacitors into account in the design of energy buffering systems. Additionally, it can be seen that this benefit extends beyond the initial sizing of the capacitor bank. This general process can be repeated for any given ceramic capacitor in order to obtain the optimal operating range for overall system power density.

2.6 Conclusions

This chapter has explored the selection of ceramic capacitors for energy buffering applications. Suitable methods for computing the energy stored in ceramic capacitors are discussed and demonstrated through experimental measurements. Additionally the energy density and quality factor of ceramic capacitors are compared to those of polyester and polypropylene film capacitors as well as electrolytics. Finally the results discussed in the initial sections of the chapter are applied in the design process of a line frequency buffer. It is found that the optimal voltage ripple range is changed by the derating of Class II ceramic capacitors. This information is presented with the hope that the operational data, demonstrated test method, and system design suggestions will be useful tools for designers to select, size and design with the appropriate ceramic capacitors for line energy buffering and other applications.

CHAPTER 3

DESIGN AND CONTROL OF A GAN-BASED, 13-LEVEL, FLYING CAPACITOR MULTILEVEL INVERTER

3.1 Motivation

The specific power density (power to weight ratio, $\frac{kW}{kg}$) of inverters is a significant consideration in both mobile and stationary applications. In electrified transportation overall system weight will impact both efficiency and range. In many stationary applications, such as photovoltaic systems, power converter weight and volume play a role in determining installation costs.

As will be discussed further in Chapter 5, the density of an associated electric machine is also an important factor in the power density of mobile systems [48–50]. High-density electric machines, such as those being designed for electric aircraft, utilize reduced iron and fewer windings and consequently have a much smaller synchronous reactance than conventional designs [16]. H-bridge, 2-level inverter topologies typically rely on the large reactance of conventional machines to filter voltage pulses into sinusoidal winding currents. Since high-density machines do not have this reactance, large filter inductors must be added to 2-level inverters to achieve sinusoidal winding currents and avoid harmonic losses in the machine. This filtering requirement can significantly reduce the inverter power density.

In order to avoid the mass penalty of a large filter inductor, a multilevel inverter topology can be used to reduce harmonics in the load current. Due to fundamental physics and technology considerations, commercially available capacitors currently offer an energy storage density up to two orders of magnitude higher than that of inductors. Although research continues in the development of new magnetic materials, at present this reality suggests that power converters based on primarily capacitive energy transfer with reduced inductance have the potential to offer higher energy density than power converters which rely heavily on inductive filtering.

While neutral point and capacitor clamped multilevel topologies can be used to implement low level count multilevel inverters, these topologies become unwieldy at higher level counts. The modular multilevel converter (MMC) and flying capacitor multilevel converter (FCML)

are two capacitor-based multilevel topologies which are scalable to high level counts [51–53]. The MMC converter offers redundancy, modularity, and scalability which is especially appealing for applications such as high-voltage DC transmission. Each capacitor and switch in the MMC converter operates with equal voltage stress. However, the capacitive energy storage requirements in the MMC are inversely proportional to the slow inverter fundamental frequency and relatively independent of the converter switching frequency [54].

As will be discussed, the capacitor sizing for an FCML converter is inversely proportional to the converter switching frequency. This allows the total energy storage of the FCML converter to be reduced by increasing the switching frequency which is typically at least an order of magnitude and possibly two orders of magnitude higher than the fundamental frequency. As a result of this trait, FCML converters are able to achieve a higher power density than MMC converters for typical high-density motor drive applications [54]. In addition to being used as low-THD inverters or rectifiers, the general FCML structure can also be used for voltage multiplication and pulsed power applications where the inherent voltage stress distribution, allows conversion at high voltage ratios with low-voltage switches [55].

Since the original publication of the flying capacitor multilevel converter [53], there has been considerable theoretical work with respect to capacitor voltage balancing and its dynamics [56–65]. However, there have been relatively few complete prototypes that have functionally demonstrated the many power density, efficiency, and EMI advantages of this topology at the power and voltage levels required for applications such as electrified aviation or photo-voltaic solar inverters. Functional prototypes demonstrated in journal publication have primarily been focused on demonstration of control architecture and have not been optimized for power density [64, 66–68]. Many of the demonstrations of converter control have been accomplished using laboratory hardware-in-the-loop (HIL) type systems instead of more deployable single FPGAs or microcontrollers. Other exceptionally well engineered hybridized extensions of the FCML inverter are focused on high efficiency and therefore switch at frequencies 16 kHz and below [69]. In exchange for increased efficiency, a slower switching frequency requires larger flying capacitance and decreases the power density of the inverter system, which may be a preferred trade-off depending on the application.

Leveraging recent advances in wide-bandgap semiconductors and supporting level-shifting and gate driving ICs, this work demonstrates experimentally that the self-balancing characteristics of FCML inverters demonstrated at three to seven levels can be extended to higher level counts and bus voltages using low-voltage GaN devices. Due to the lower flying capacitor voltages required to implement the 400 V inverter in [10], the high-density ceramic capacitors exhibited less voltage derating resulting in a simpler implementation.

Necessitated by the high (800 V) input dc voltage, this work explores the minimum capacitance required to ensure that switch ratings are not exceeded for a given expected operating duty ratio when using ceramic capacitors, and demonstrates that the mismatch in capacitor impedance values resulting from the series connection of capacitors at higher voltage levels does not contribute significantly to capacitor voltage imbalance. Additionally, this work demonstrates that the stable operating characteristics achieved in [10] can be extended to a higher number of levels despite the potential for additional sources of switching mismatch arising from the greater number of switches and gate drivers being required.

The remainder of this chapter is organized as follows: Section 3.2 discusses the design of the FCML converter. Section 3.3 demonstrates the use of open and closed capacitor voltage balancing. In Section 3.4 the estimated loss breakdown for the converter and requirements for the effective management of switch losses in GaN devices are discussed. Section 3.5 outlines the experimental results obtained for the 13-level prototype. Finally, a review of key points is presented in Section 3.6.

3.2 FCML Inverter Design Process

3.2.1 Level Selection

The design tradeoff for the FCML level count will change significantly depending on the family of components available to the designer. Increasing the converter level count results in a decrease in the required switch blocking voltage which allows lower voltage switches with higher figures of merit to be used, essentially maintaining the conduction losses in comparison to a single switch rated for the full converter voltage. Moreover, as shown in [70] the required filtering inductance is reduced inversely proportionally to $(N-1)^2$ due to the decrease in the ripple amplitude and increase in ripple frequency with the number of levels. However, an increase in the number of levels also brings an increase in component count and complexity due to the increased number of switches as well as accompanying level shifters and gate drivers.

As mentioned in the introduction, one of the primary purposes of this design was to experimentally validate that the benefits of FCML inverters at three, four, five, and seven levels could be experimentally demonstrated at higher level counts. This is especially important because weight and THD sensitive applications such as electric aircraft are being envisioned at voltages of 1 kV and above [71]. In order to design for a voltage stand-off of 1 kV with high level count, a 13-level inverter with a nominal switch blocking voltage of 83 V was

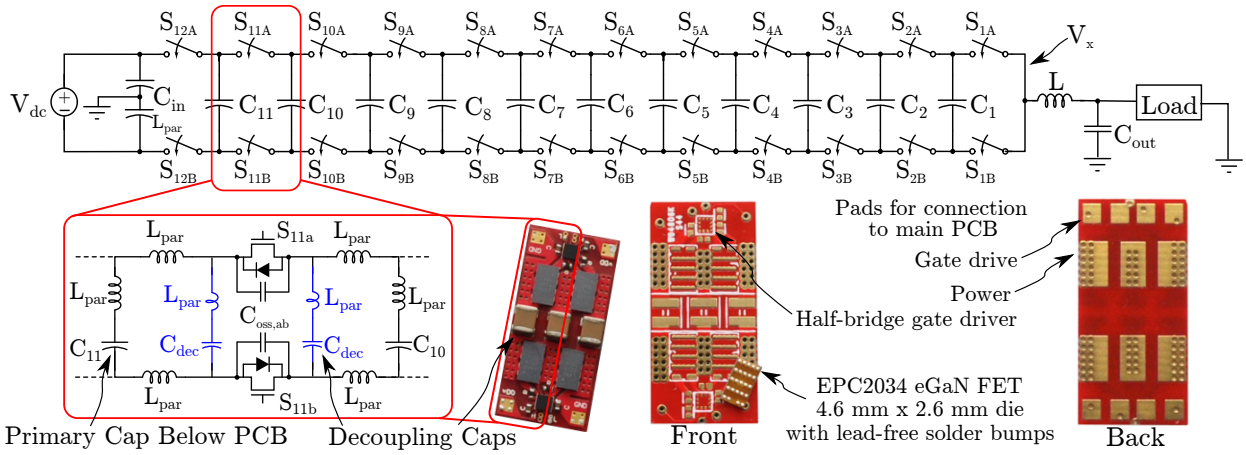


Figure 3.1: Full inverter schematic. Lower left inset highlights the use of small decoupling capacitors immediately adjacent to the GaN FETs to reduce the effective parasitic inductance at the switching nodes. Lower right inset gives closeup of switching cell fabricated on a 0.4 mm PCB with ENIG finish.

selected.

3.2.2 Capacitance Sizing

A schematic drawing of a 13-level FCML is shown in Fig. 3.1, along with a closeup schematic showing some of the implementation details of this work. An N-level FCML converter utilizes N-2 flying capacitors with operating voltages following a pattern of

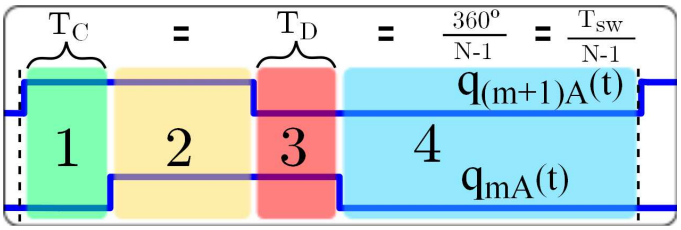
$$V_{\mathrm{C(m)}} = \frac{m \ \cdot V_{\mathrm{dc}}}{N-1}, \ m = 1, 2...(N-2). \tag{3.1}$$

Although the required voltage rating of the higher-level capacitors is high, the voltage rating of each switch is equal and is limited to the voltage difference between two capacitors, or

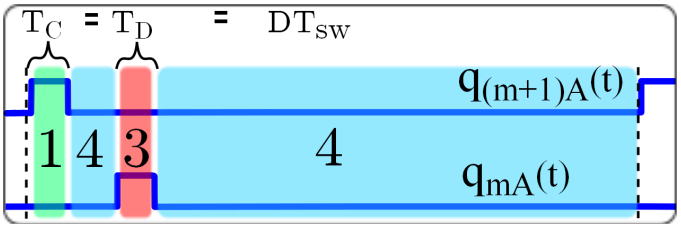
$$V_{\mathrm{SW,nom}} = \frac{V_{\mathrm{dc}}}{N-1}, \tag{3.2}$$

which allows for the use of low-voltage devices with improved figures of merits and higher switching frequencies.

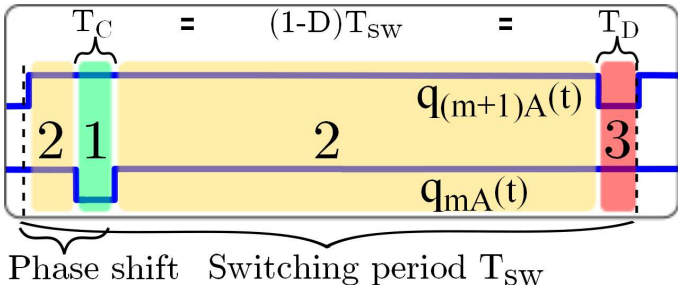
Phase-shifted pulse-width modulation (PSPWM) has been shown to be an effective method for controlling the FCML converter [53]. The PSPWM plots in Fig. 3.2 show the switching signals for the "A" switches in two adjacent switch pairs of the inverter. Each signal "$q_{\mathrm{kA}}(t)$" has an equal duty ratio (D) and is shifted $\frac{360^\circ}{N-1}$, or 30° in the 13-level case from the adjacent signals. Despite the phase shift, the voltage conversion ratio of an FCML operating in buck



(a) Within the range $\frac{1}{N-1} < D < 1 - \frac{1}{N-1}$, the charge and discharge interval is set by the phase shift.



(b) For $D < \frac{1}{N-1}$ the charge and discharge is proportional to D.



(c) For $D > 1 - \frac{1}{N-1}$ the charge and discharge is proportional to $1 - D$.

Figure 3.2: Control waveforms for switch pairs adjacent to capacitor C_{m}. The charge interval (T_{C}) is designated as interval 1, high bypass as interval 2, discharge (T_{D}) as interval 3, and low bypass as interval 4.

mode is equal to that of a standard, two-level buck converter, or

$$V_{out} = D \cdot V_{in}. \tag{3.3}$$

The change in charge on a flying capacitor will be determined by the load current (i_{load}) and the charge/discharge interval over which the capacitor is connected in the circuit. This is explored in the subcircuit shown in Fig. 3.3. The charge and discharge of capacitor C_{m} is dictated exclusively by the positions of the adjacent switch sets S_{m} and $S_{\mathrm{m+1}}$. In each switch set, switch A is the top device and the complementary switch, B is the lower device.

The possible paths current can take through the circuit segment are outlined with arrows #1 through #4 on the left side of the figure. Current path #1 charges the capacitor, path #2 bypasses the capacitor on the high side, path #3 discharges the capacitor, and #4

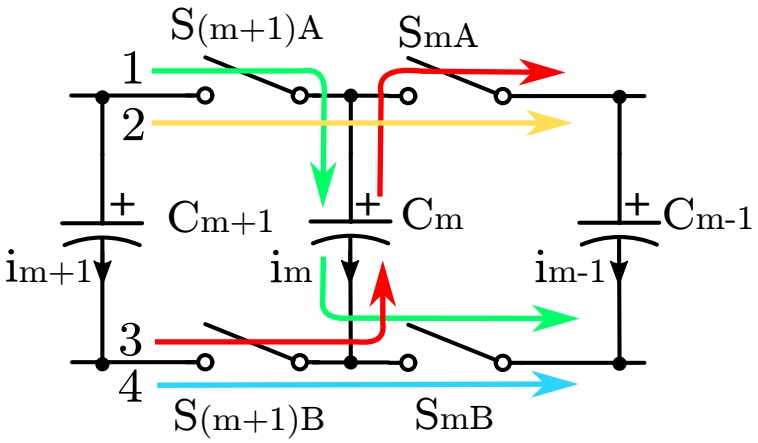


Figure 3.3: Subcircuit depicting the current flow in different switch configurations. The charge/discharge of capacitor C_{m} is entirely dictated by the positions of switch sets S_{m} and $S_{\mathrm{m+1}}$. Switches A and B are always complementary, in order to maintain a voltage difference between capacitors.

bypasses the capacitor on the low side. The switch states and current flow are dictated by the converter duty ratio.

The length of the charge (T_{C}) and discharge (T_{D}) interval is dependent on the converter operating conditions and, as shown in the colored regions of Fig. 3.2, is divided into three ranges depending on the relationship between the converter duty ratio (D) and the phase shift of the converter. When the converter duty ratio is in the range $\frac{1}{N-1} < D < 1 - \frac{1}{N-1}$, the charge and discharge interval of each capacitor is constant regardless of duty ratio and is dictated by the phase shift. Below and above this range the charge and discharge time is determined by D and $1 - D$ respectively. Figure 3.2 highlights the current flow through or around capacitor C_{m} under each condition over the full switching cycle.

Because the condition $\frac{1}{N-1} < D < 1 - \frac{1}{N-1}$ imposes the largest charge/discharge time on the capacitors of $\frac{1}{f_s \cdot (N-1)}$, the worst-case change in charge on the flying capacitors (ΔQ_{C}) can then be calculated to be

$$\Delta Q_{\mathrm{C}} = i_{\mathrm{load}} \Delta t = i_{\mathrm{load}} \frac{1}{f_{\mathrm{s}} \cdot (N-1)}. \tag{3.4}$$

The capacitors are then sized based on this charge ripple, as the ripple for other operating conditions will be smaller [54].

The peak voltage ripple on a given capacitor ($V_{\mathrm{ripple,pk}}$) may be defined as a fraction, (α_{cv}), of $V_{\mathrm{SW,nom}}$ [54]. The peak-to-peak flying capacitor voltage ripple (ΔV_{C}) on the capacitor can then be expressed as

$$\Delta V_{\mathrm{C}} = 2 \cdot \alpha_{\mathrm{cv}} \cdot \frac{V_{\mathrm{dc}}}{N-1}. \tag{3.5}$$

As the capacitor voltage ripple increases, the voltage blocking stress on adjacent switches is increased. Thus the maximum allowed voltage ripple is limited by the maximum blocking voltage of the switches. Over the interval of $\frac{1}{N-1} < D < 1 - \frac{1}{N-1}$, adjacent capacitors always charge and discharge sequentially, and as a result the voltage fluctuation across the switches will be $2\Delta V_{\mathrm{C}}$, but the voltage will oscillate ΔV_{C} above and below the nominal and therefore the maximum switch voltage stress will be approximately $V_{\mathrm{SW,nom}} + \Delta V_{\mathrm{C}}$.

Combining (3.4) and (3.5), the capacitance required at each node for a given load current, as a function of capacitor voltage ripple, is found to be

$$C = \frac{\Delta Q_{\mathrm{C}}}{\Delta V_{\mathrm{C}}} = \frac{i_{\mathrm{load}}}{2 \cdot \alpha_{\mathrm{cv}} \cdot V_{\mathrm{dc}} \cdot f_{\mathrm{SW}}}. \tag{3.6}$$

In the case of an inverter, the peak load current must be used in the expression of i_{load}.

Because the capacitance per cell does not depend on the number of levels in the converter [54], total converter capacitance increases linearly as levels are added. Thus there is a trade-off between the reduction in inductor volume achieved by increasing the number of levels and the accompanying increase in capacitor volume.

In addition to the capacitance required for energy storage in each flying capacitor node, the current carrying requirements for the capacitors must be taken into account. As previously discussed, the longest charge and discharge intervals occur in the range $\frac{1}{N-1} < D < 1 - \frac{1}{N-1}$. Under this condition, the capacitor is conducting the load current for $\frac{2 \cdot 360^{\circ}}{N-1}$ degrees each switching cycle. Thus for a dc i_{load}, the worst-case RMS value of a pulsed capacitor current with a duty ratio $\frac{2}{N-1}$ is known to be

$$i_{\mathrm{C,RMS}} \leq i_{\mathrm{load,dc}} \cdot \sqrt{\frac{2}{N-1}}. \tag{3.7}$$

Equation (3.7) also holds for the RMS capacitor current under inverter operation with an RMS load current, in which case $i_{\mathrm{load,RMS}}$ can be substituted for $i_{\mathrm{load,dc}}$.

3.2.3 Capacitor Selection

Based on the selected 13-level configuration and 100 V rated switching cells with a 1 kV dc bus, each of the switches operates with a nominal 83 V blocking voltage ignoring capacitor voltage ripple. Selecting a $\Delta V_{\mathrm{C}} = 5$ V per capacitor, and an $\alpha_{\mathrm{cv}} = 0.03$, the peak nominal voltage across a switch will be 88 V, allowing a 12 V margin for inductor ripple, overshoot, and small capacitor imbalances. Based on (3.6), a 3 kW load power at 1 kV input voltage

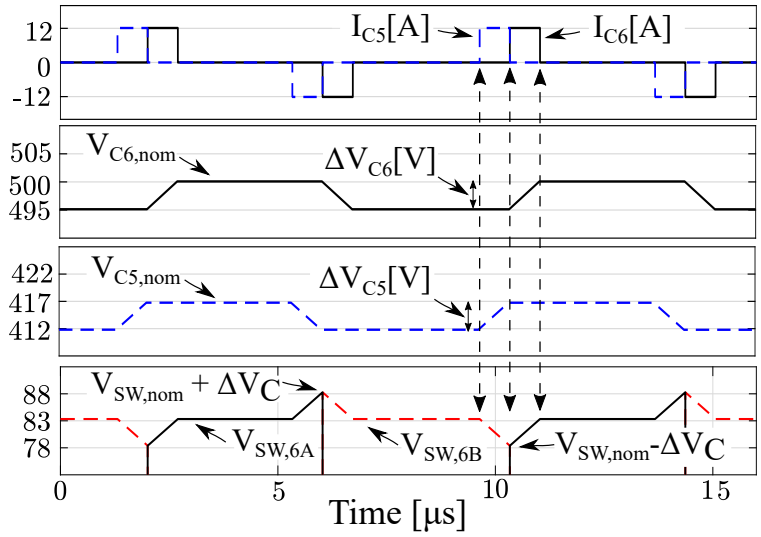


Figure 3.4: PLECS simulation showing charge and discharge of capacitors 5 and 6 in the 13-level inverter at 50% duty ratio. The voltage stress on switches 6A and 6B is increased during the intervals of voltage mismatch between the capacitors as C5 and C6 sequentially charge or discharge.

(350 V_{RMS} output), and a 120 kHz switching frequency, 1.7 μF of capacitance is required per flying node. Referencing (3.6), the required flying node capacitance increases rapidly as the voltage ripple is constrained. A practical implementation challenge in this work was the 100 V maximum voltage rating of the LM5113 half-bridge gate-driver, which constrained the maximum switch stress. In follow-on work, the half-bridge drivers used in this hardware were replaced by isolated low-side drivers which allowed for increased voltage ripple on the flying capacitors and a significantly decreased flying capacitance [11, 12].

Figure 3.4 shows an annotated PLECS simulation of the charging and discharging of 1.7 μF capacitors C5 and C6 when the converter is operating at 50% duty. For purposes of illustration, an ideal current source of 12 Adc (peak nominal operating current for this design) was used in place of an inductor to emphasize the timing and amplitude of the capacitor voltage deviations. Ignoring inductor ripple is a justified first approximation because the inductor current ripple, which is 2.5 App in this design, can be minimized in an FCML inverter due to the increased effective frequency and smaller voltage amplitude. A PLECS simulation of the full 13-level converter modeled with a 4.7 μF inductor, capacitor ESR, and a 40.8 Ω load is shown in Fig. 3.5. The oscillations in capacitor voltage are due to multiple inductor current ripple peaks as will be discussed in Section 3.2.4. It is evident, however, that the ripple is largest over the interval $\frac{1}{N-1} < D < 1 - \frac{1}{N-1}$, emphasizing that initial capacitor sizing should be made based on the PWM phase shift required for a given FCML level count ($\frac{360°}{N-1}$).

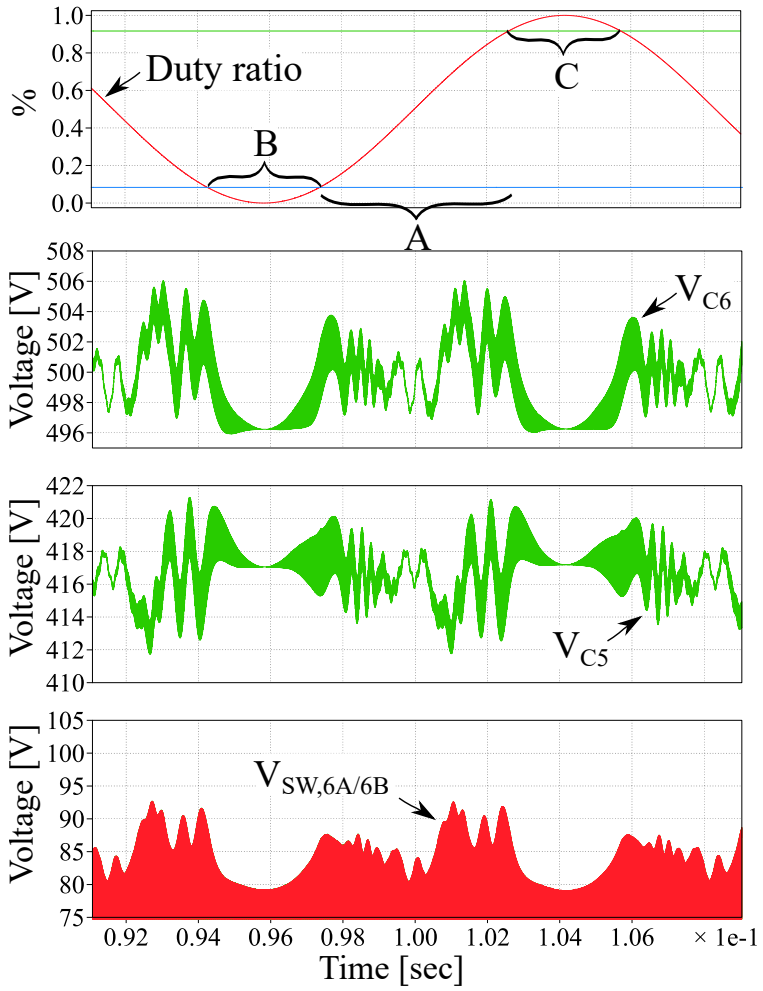


Figure 3.5: PLECS simulation showing switch blocking voltage for the 13-level converter operating at 350 V_{RMS}, 8.6 A_{RMS}. It can be seen that switch blocking voltage is maintained in a safe region and that the interval $\frac{1}{N-1} < D < 1 - \frac{1}{N-1}$ (Region A) is the region of highest capacitor voltage ripple as outlined in Fig. 3.2.

Table 3.1: Minimum capacitor configuration for 1.7 μF per flying node.

Node	V_{Node}(V)	# Caps	Cap reference	Configuration
C1	83	2	A	Parallel
C2	167	2	A	Parallel
C3	250	3	A	Parallel
C4	333	4	A	Parallel
C5	417	5	A	Parallel
C6	500	6	B	Parallel
C7	583	6	B	Parallel
C8	667	14	A	7 series sets
C9	750	16	A	8 series sets
C10	833	18	A	9 series sets
C11	917	18	A	9 series sets

As was discussed in Chapter 2, the energy storage density of Class II ceramic capacitors is currently significantly higher than other non-electrolytic dielectric technologies. This density comes with the drawback that the capacitance of these devices is reduced by the device dc bias. As a result, capacitors must be sized based on their derated capacitance value for the voltage they will be operating at. In this inverter, two different capacitors have been used to minimize overall volume. Based on an extensive evaluation [6], a 2.2 μF X6S dielectric capacitor has been shown to have good energy density for voltages below 450 V. At voltages between 450 V and 630 V, a 1 μF X7T dielectric capacitor is used to meet voltage requirements. The flying capacitor nodes at voltages above 630 V utilize series connected sets of the 450 V capacitor. Based on the capacitance of each device at the nominal flying node voltage, the minimum number of capacitors which may be used at each node to provide the minimum 1.7 μF is shown in Table 3.1. It should be noted that extra capacitance was added to the implemented hardware because of space availability.

In this design the worst-case RMS capacitor current is 3.5 A. Due to the manufacturer specified ESR rating for capacitor A of 5.4 mΩ at the converter switching frequency, a temperature rise above ambient of 20 °C, and a manufacturer specified package thermal impedance to ambient of 240 °C/W, the current carrying capability of capacitor A is approximately 3.9 A per capacitor [72]. Thus the number of devices required to meet the capacitance requirement supersedes the current requirement. When the current stress on the capacitors is high, the increased effective ESR of ceramic capacitors under bias should also be considered [8] to prevent excessive heating.

3.2.4 Inductor Sizing

One of the primary benefits of multilevel inverters is the reduction in required filtering inductance for a given ripple specification. The maximum voltage ripple seen by the inductor is the voltage across the smallest flying capacitor, $\frac{V_{bus}}{N-1}$. Additionally, under phase shifted PWM modulation, the effective switching frequency seen by the inductor is equal to $(N-1)f_{\mathrm{SW}}$ where f_{SW} is the switching frequency of a single switch in the inverter. When combined, these effects reduce the inductance required to meet a given peak ripple specification by $(N-1)^2$ as compared to a two-level inverter switching at f_{SW} [10, 70].

In a two-level buck converter, the inductor current ripple amplitude can be described as,

$$\Delta i_{\mathrm{pp}} = \frac{V_{\mathrm{in}} \cdot (D \cdot (1-D))}{L \cdot f_{\mathrm{sw}}} \tag{3.8}$$

with a maximum ripple amplitude at D = 0.5. Because the FCML converter has multiple voltage levels, the duty ratio seen by the inductor is not the simple duty ratio, but is instead given by

$$D_{eff} = D \cdot (N-1) - floor(D \cdot (N-1)). \tag{3.9}$$

The current ripple for the FCML then becomes,

$$\Delta i_{\mathrm{pp}} = \frac{V_{\mathrm{in}} \cdot (D_{\mathrm{eff}} \cdot (1-D_{\mathrm{eff}}))}{L \cdot f_{\mathrm{sw}} \cdot (N-1)^2}. \tag{3.10}$$

Figure 3.6 plots the normalized inductor current ripple for a 2-level buck and 13-level FCML with equal DC bus voltage, switching frequency, and inductance [73]. In addition to the dramatic difference in peak current ripple magnitude, it can be seen that there are duty values at which the inductor current ripple is zero, corresponding to conversion ratios equal to one of the 13 output voltages. Here, the FCML inductor is sized to limit the peak-to-peak inductor current to 2.5 A resulting in a 4.7 μH inductor. For reference the same ripple amplitude with a two-level buck inverter would require a 677 μH inductor assuming the same switching frequency and DC bus voltage.

3.2.5 Circuit Layout and Switch Configuration

As will be discussed in Section 3.3, the successful implementation of a high level count FCML inverter is greatly aided by passive balancing of the flying capacitors. Some of the biggest contributors to capacitor mismatch include voltage ripple at the converter input caused by inadequate input capacitance, and mismatch in the gate driving strength and

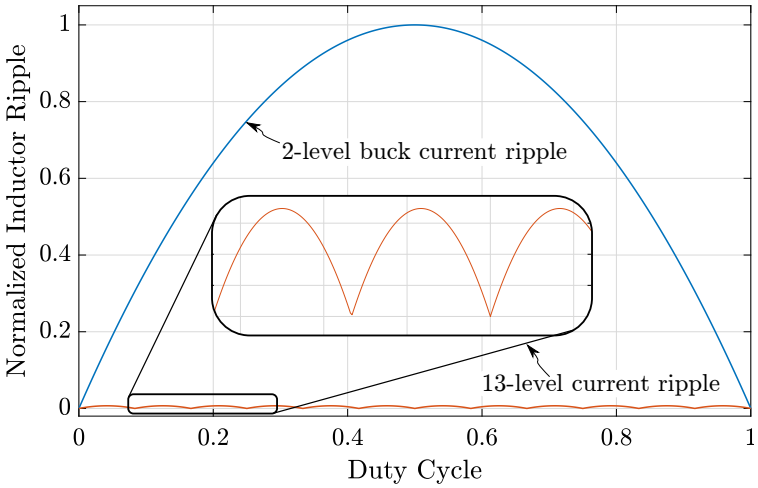


Figure 3.6: Normalized relative inductor current ripple amplitude for two-level and thirteen-level converter with equal DC bus voltage, switching frequency, and inductance.

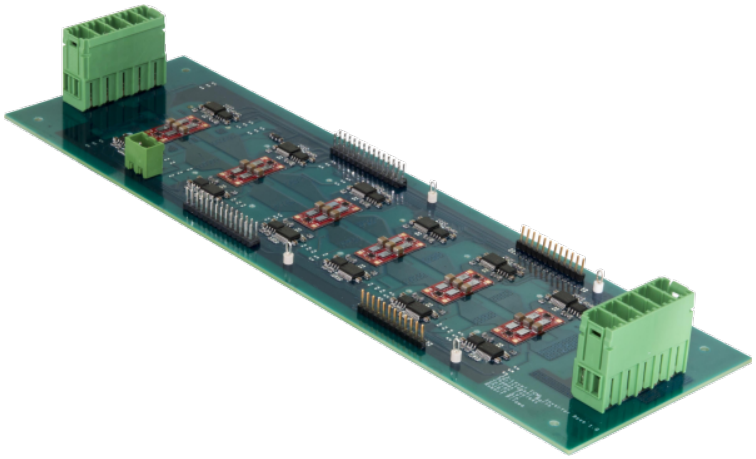


Figure 3.7: Complete 13-level FCML inverter.

switch transition speed of the individual switches [74]. In this design symmetric operation was ensured by matching the gate driving loop inductance among FETs and minimizing both the gate driving loop inductance and the power stage commutation loop inductance.

In order to optimize the gate drive layout and allow for modular assembly, the 13-level inverter is composed of six modular "switching cell" cells, as shown in the schematic drawing and photographs of Fig. 3.1. Each cell comprises two opposing half-bridges driven by TI LM5113 drivers with a floating power supply and logic isolating IC located adjacent to the cell. The low-inductance layout between the gate driver and switch enables symmetrical, high-speed operation of the FETs [10].

Excessive commutation loop inductance in the power stage results in overshoot at the switch transitions requiring the FET gate drive strength to be reduced. The resulting slower

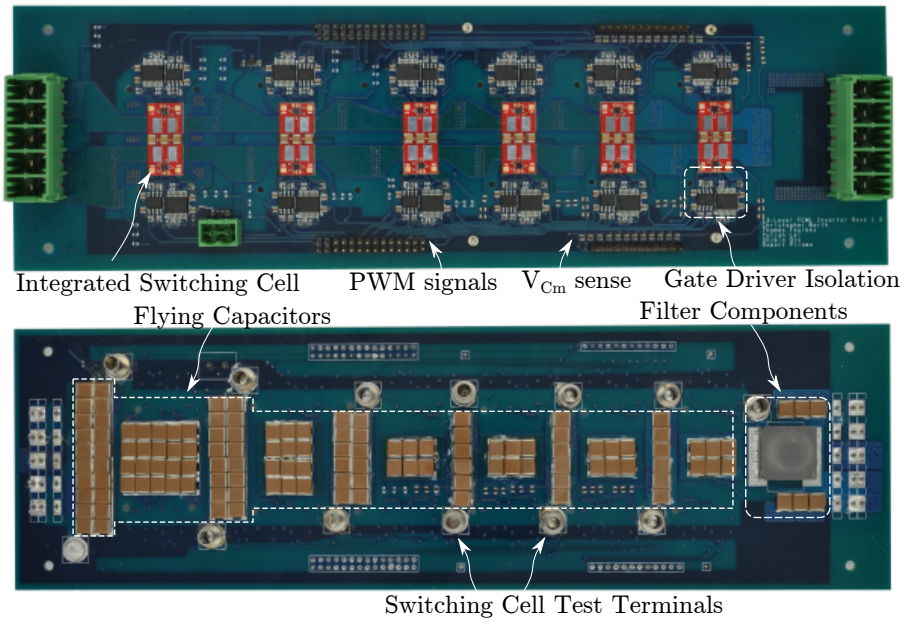


Figure 3.8: Annotated photographs of top and bottom of inverter.

switching rates and higher switching losses may contribute to mismatch in switch timing and flying capacitor imbalance. In order to minimize commutation loop inductance in this implementation, the PCB traces are routed with minimal loop area. Additionally, small "decoupling" capacitors are mounted immediately adjacent to each switch. As shown in the Fig. 3.1 subset, these smaller decoupling capacitors provide a low-impedance path for the commutation current to flow, irrespective of the ESL or parasitic trace inductance of the larger bulk flying capacitors located below the inverter. In this design, the small, local, decoupling flying capacitors are used to reduce ringing and overshoot during switch commutations, whereas the bulk flying capacitors provide energy transfer during the remainder of the switching period.

As the DC voltage bus of the converter is increased for higher power applications it becomes increasingly difficult to maintain small commutation loops due to the need for larger creepage and clearance to prevent arcing at high voltage (e.g., 800 V in this design). In this work 1 kV rated decoupling capacitors were successfully used on the switching cell; however, other approaches such as a double-sided design can also be used to enable low-inductance commutation paths while maintaining adequate clearance [11].

Assembly of the switching cells was accomplished using a Finetech SMT station which allowed for precise placement and a consistent reflow cycle as specified by EPC. Prior to mounting components, the switching cells were cleaned with rubbing alcohol and a small amount of Kester TSF-6522 tacky flux was applied. After soldering the completed switching

cells were cured at 150° for 30 min to deactivate the flux as specified by Kester. The switching cells are affixed to the main inverter board using hot air and low-temperature solder to avoid disturbing the gate drivers, and passives which are preassembled using standard prototyping Sn63/Pb37 solder.

Figure 3.7 provides an overview photo of the complete 13-level hardware prototype, and Fig. 3.8 provides annotated photographs of the top and bottom of the converter. The full converter parts list is provided in Table 3.2. A unique feature of this prototype is the ability to reconfigure the inverter to utilize 3, 5, 7, 9, 11, or 13 levels using various jumper configurations. This reconfigurability is designed to allow the converter to be used as a test platform for evaluation of various FCML level counts and was used to evaluate the accuracy of a real-time hardware in the loop simulation, and to develop metrics for the evaluation of the simulation accuracy [75]. The jumper connections also allow full power testing of the individual switching cells in the converter before the full system is assembled.

Table 3.2: 13-Level hardware prototype component listing.

Component	Part Number	Parameters
FPGA Controller	Altera - 10M08SAE144C8GES	
GaN switches	EPC - 2033	150 V, 7 mΩ
GaN gate driver	Texas Instruments - LM5113	100 V half-bridge
Flying caps - A (450 V)	TDK - C5750X6S2W225K250KA	2.2 μF
Flying caps - B (630 V)	TDK - CKG57Nx7T2J105M500JJ	1 μF
Decoupling caps (1 kV)	Kemet - C1210V563KDRACTU	0.056 μF
Inductor	Vishay - IHLP6767GZER4R7M5A	4.7 μH
Digital isolators	Silicon Labs - Si8423BB-D-IS	
Power isolators	Analog Devices - ADUM5210	
PWM signal filtering		229 Ω, 47 pF

3.3 Balancing of Flying Capacitor Voltages

The voltage balancing of FCML converters is one of the challenges faced in implementation. Although passive balancing is effective, there are times when it is beneficial to augment the balancing with auxiliary control. Active balancing can be achieved through linear [61–63] or non-linear [58,64,65] control techniques. Non-linear techniques can achieve a better transient response, but measurement timing and signal quality become challenging due to the need for precisely timed measurements of switching waveforms. In this work, the operation of the 13-level FCMl was demonstrated using passive balancing.

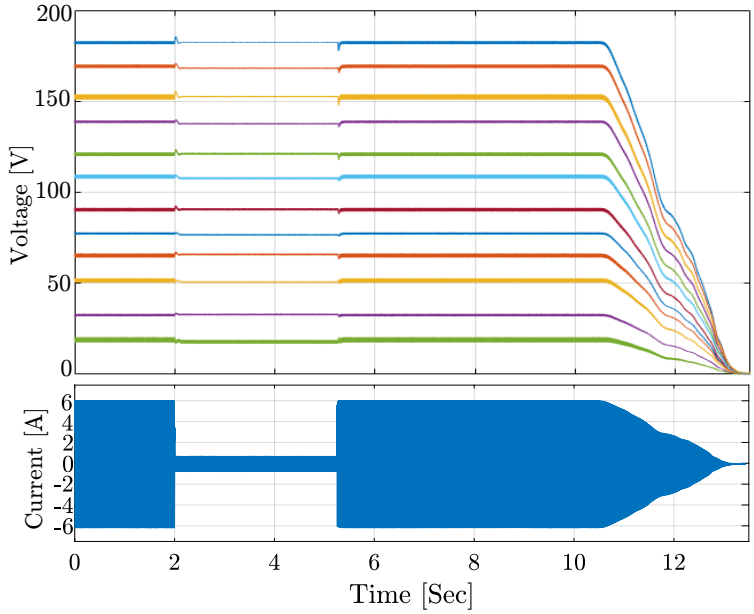


Figure 3.9: Experimental waveforms of capacitor voltage, showing that the 13-level FCML maintains excellent passive capacitor voltage balancing even in the presence of a step load from 1 A_{pk} to 5.5 A_{pk}. Upper plot shows 12 capacitor voltages for the converter operating off of a 200 V bus. Below the capacitor voltages the envelope of the load current can be seen.

3.3.1 Passive Balancing Explanation

The flying capacitors shown in Fig. 3.3, $C_{\text{m-1}}$, C_{m}, and $C_{\text{m+1}}$, along with switch sets S_{m} and $S_{\text{m+1}}$ form a modular control unit which can be explored to understand the voltage balancing of the FCML. The instantaneous current i_{m} through each capacitor C_{m} can be expressed as

$$i_{\text{m}} = (S_{\text{m+1}} - S_{\text{m}})i_{\text{load}}, \tag{3.11}$$

where S_m and S_{m+1} are represented by 1 for the ON state and 0 for the OFF state. The output inductor instantaneous current is represented by i_{load}. In order for capacitor voltages to remain stable, the amp-second balance of each capacitor must sum to zero over the switching interval. This can be articulated as

$$\overline{i_{\text{m}}} = \int_0^{T_{\text{sw}}} (S_{\text{m+1}} - S_{\text{m}})i_{\text{load}}dt = 0, \tag{3.12}$$

where T_{sw} is the switch period as shown in Fig. 3.2. Provided the integral of current through the capacitor is zero, the capacitor voltage will be constant.

While (3.12) is theoretically met by PSPWM, there are frequently practical higher order

disturbances which arise. For example, in designs using half-bridge boot-strap drivers, the high-side switch is frequently driven with marginally less voltage than the low-side switch due to the voltage drop associated with the bootstrap diode, which may distort the duty ratio of the switch. Additionally, it has been shown that voltage ripple at the converter input will result in non-ideal ripple in the inductor current and a resulting distortion in capacitor charging current [74]. The level count of an FCML also has an impact on converter balancing as it has been shown that even-level flying capacitor converters are more resistant to the imbalancing impact of input voltage ripple than odd-level count designs [74]. These challenges can be partially mitigated by reducing the impedance of the source feeding the converter and utilizing appropriate gate-driving strategies [76].

These practical sources of error in capacitor charging current result in bounded voltage drift between capacitors. Under the assumption that the inverter modulating frequency is significantly lower than the balancing time constants of the converter, the converter can be modeled as operating at steady state [56]. At steady state, any diversion of capacitor voltages from their nominal value results in switching frequency harmonics in the load current. These harmonics result in higher dissipation in the load, which limits capacitor drift from the nominal voltage value [57]. It should be noted that natural balancing only occurs in the presence of a real load current. Purely reactive loads will theoretically not allow the converter to balance properly [57, 59]. In practice, losses in the converter itself will typically draw sufficient current to correct small imbalances. This is especially true because the energy in the high-frequency harmonics resulting from capacitor imbalance is more easily dissipated in high-frequency loss mechanisms such as core loss, eddy current, or inductor skin effect [77].

3.3.2 Passive Balancing Results

To investigate the steady-state and dynamic voltage balancing, a high-voltage, multi-channel digital acquisition system (PXIE-4300) from National Instruments was used to simultaneously sample each capacitor voltage. Figure 3.9 shows measurements of the excellent passive load balancing capability of the 13-level converter in both steady state and in the presence of a current load step. In this demonstration, the 200 V bus is divided among the 12 flying capacitors with a voltage difference of 16.7 V between capacitors. It can be seen that the voltage on the capacitors remains stable and balanced both at steady-state and in the presence of a load current step from 1 A_{pk} to 5.5 A_{pk}.

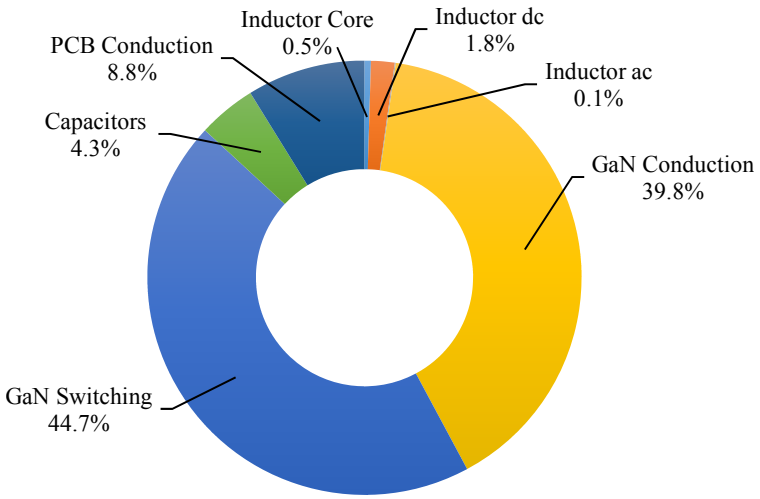


Figure 3.10: Estimated distribution of losses for 13-Level FCML inverter operating at 800 Vdc, 250 Vac, 3 kW.

3.4 Thermal Management Assessment

Because optimization frequently hinges on understanding the loss penalty of design trade-offs [44], a proper assessment of losses is critical in the design process. Additionally, an estimation of losses is important for proper sizing of converter cooling. In this design, transistor conduction losses, overlap and output capacitance switching losses, and estimates of capacitor and inductor losses were calculated based on standard practice [46,78] and averaged over the fundamental period.

An approximate loss breakdown for the FCML converter operating at 3 kW, between 800 Vdc and 250 Vac bus, is shown in Fig. 3.10. It can be noted that switching and conduction losses in the GaN devices are the dominant loss mechanisms. Thus, care must be taken to provide proper heatsinking of the devices while taking into account the small thermal mass and surface area of the EPC GaN FETs. Electrical isolation is important because of the close proximity of the heatsink to the uninsulated FET sides and exposed BGA pads. Finally, compliance is needed between the rigid heatsink and the individual GaN FETs to account for mechanical tolerances as the flip-chip silicon devices are easily damaged by excessive pressure.

Bergquist GP5000S35 Gap-Pad was used as the thermal interface material between the FETs and the heatsink. Based on the manufacturer suggested pressure of 30 PSI [79], the heatsink standoffs were milled to accommodate a compression ratio on the Gap-Pad of $\sim$15% [80]. Figure 3.11 shows the inverter with attached heatsink and Gap-Pad sample. The heatsink along with the rest of the converter are cooled using low-volume forced air.

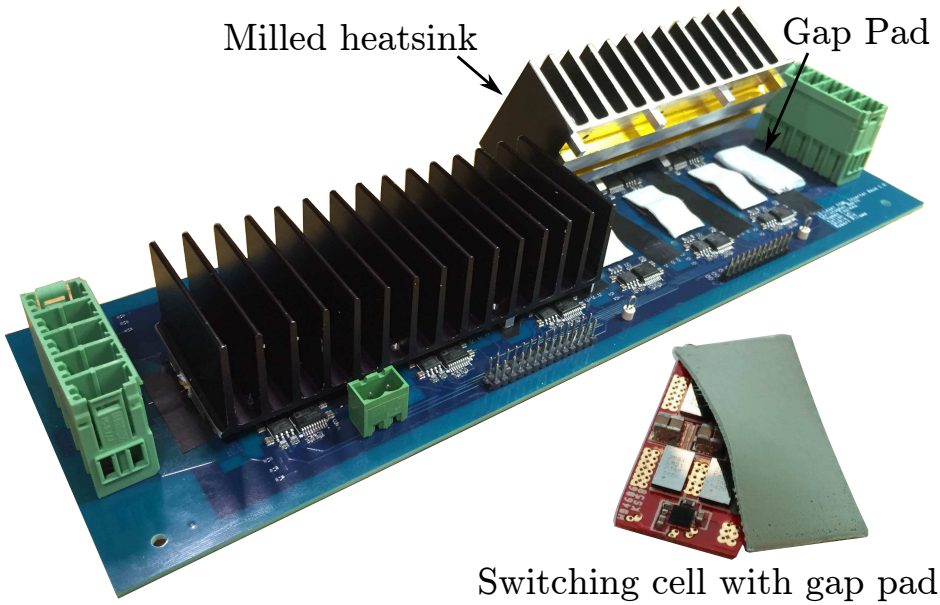


Figure 3.11: 13-level inverter with heatsink.

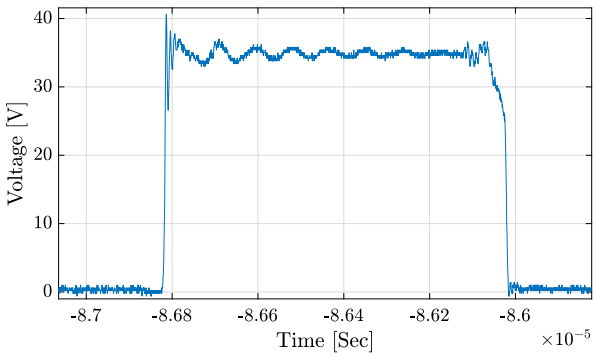


Figure 3.12: Minimal gate-source ringing at switch transition.

Table 3.3: Tested inverter specifications.

Specifications	Values
Number of Levels (N)	13
Input Voltage	800 V
Output Voltage	250 V_{RMS}
Output Power	3.1 kW
THD	0.7 %
Peak Efficiency	98.3 %
Density (w/o heatsink)	12.4 kW/kg

This air flow is also sufficient to cool the flying capacitors and output filter elements on the bottom of the inverter board. Since capacitors are the main energy transfer element in an FCML inverter, the small output inductor receives a fraction of the stress normally seen by output inductors, and thus has dramatically smaller magnetic core losses than those normally experienced in similar applications.

3.5 Demonstrated Inverter Performance

As mentioned in Section 3.2.5, one of the key elements in the successful implementation of the FCML converter is the minimization of parasitic inductance in a large number of commu-

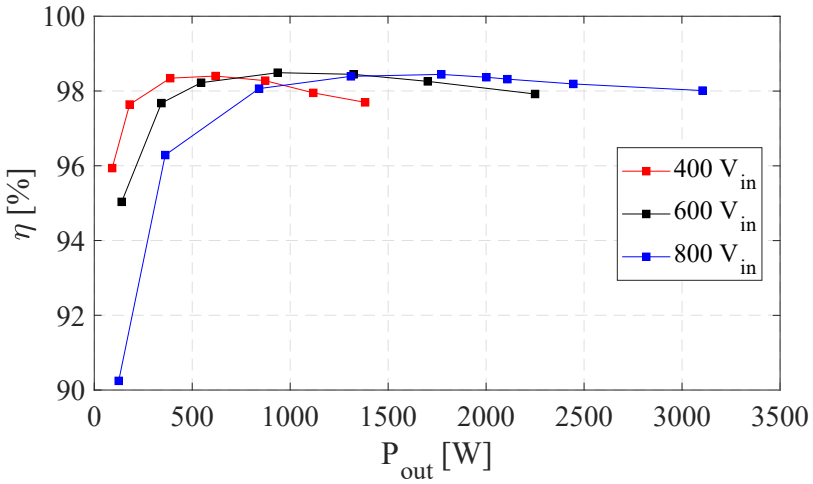


Figure 3.13: Inverter efficiency over load for dc bus voltages of 400 V, 600 V, and 800 V with a constant modulation depth.

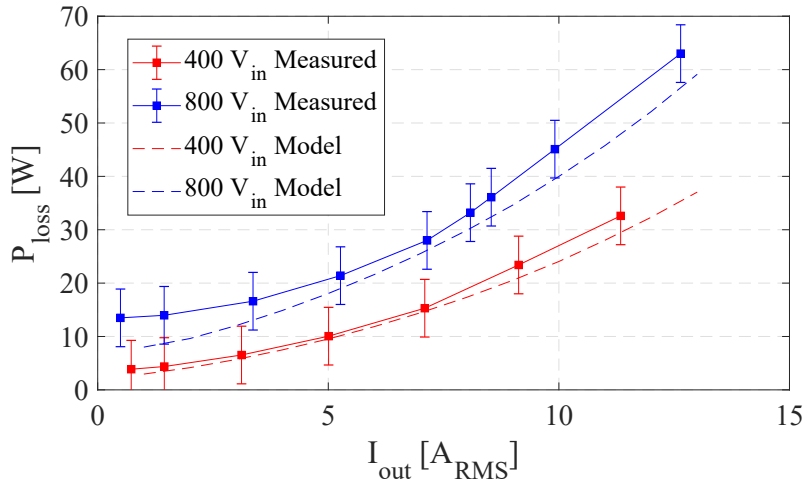


Figure 3.14: Total measured plotted along with model-based estimates of loss.

tation loops. Large parasitic inductance will result in significant ringing in the tank circuit formed by the drain-source capacitance of the FET and the parasitic inductance. In this design the parasitic loop inductance was minimized through careful component placement as well as the use of the decoupling capacitors as outlined in Fig. 3.1. The results of this approach can be seen in Fig. 3.12 which shows the measured drain-source ringing at switch turn-on and turn-off with minimal ringing despite maintaining a quick, 10 ns rise time. In this design the LM5113 gate driver with a 5 A peak driving strength was used in conjunction with a 22 Ω gate resistor.

The final demonstrated performance for the 13-level converter is shown in Table 3.3. The power density 12.4 kW/kg excludes the weight of the heatsink as the heatsink design focused

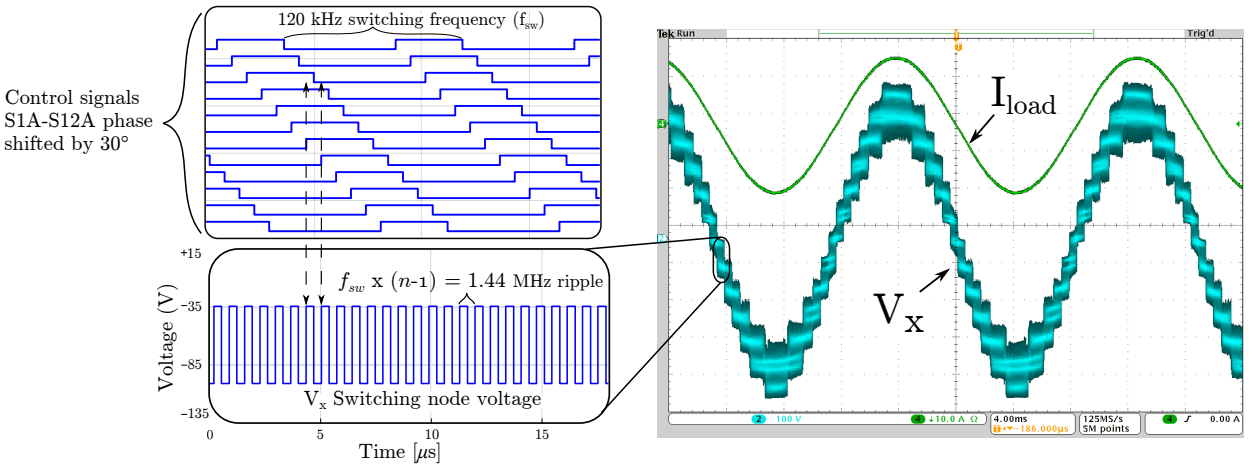


Figure 3.15: Simulation of phase-shifted switch PWM, switching node ripple frequency, and experimentally measured switching node voltage.

primarily on cooling and less on minimizing weight. Follow-on work building on this design focused extensively on the optimization of the combined heatsink and converter [12]. Load sweeps were performed for the 13-level FCML operating at a dc bus voltage of of 400 Vdc, 600 Vdc, and 800 Vdc with Yokogawa WT310 power meters being used to measure converter supply and load power in order to calculate converter efficiency.

The efficiency curves in Fig. 3.13 show a peak efficiency of 98.4% for multiple DC bus voltages. In each test the modulation depth was maintained at a constant value of 0.89, and therefore, the AC RMS voltage was 125 V_{RMS}, 188 V_{RMS}, and 250 V_{RMS} for the DC bus voltages respectively. The loss model used in Fig. 3.10 was validated by the reasonable agreement seen in overlaying measured and calculated losses at 400 Vdc and 800 Vdc in Fig. 3.14. The divergence at higher current is suspected to be related to second-order effects of device heating which are only partially accounted for in the model. In particular after the conclusion of this work it was realized that a more appropriate selection of filter capacitors in the LC output filter stage could have been utilized. In this design the output filters were constructed of the same 2.2 μF X6S capacitors used to build the flying capacitor banks. Measurements made using the capacitor testing configuration in Chapter 2 revealed a total loss in the filter capacitance of 2.6 W when the converter was running at 800 Vdc. This loss, combined with the losses of the filter inductor and adjacent GaN switches on the top side of the board, led to significantly elevated component and PCB temperatures near the output of the FCML. This elevated temperature, in turn, led to higher conduction losses as the power level of the converter was increased. Follow-on work, discussed in Chapter 5, utilized NPO capacitors with significantly lower impedance at low frequency. This approach significantly reduced losses in the filter stage and accompanying thermal challenges.

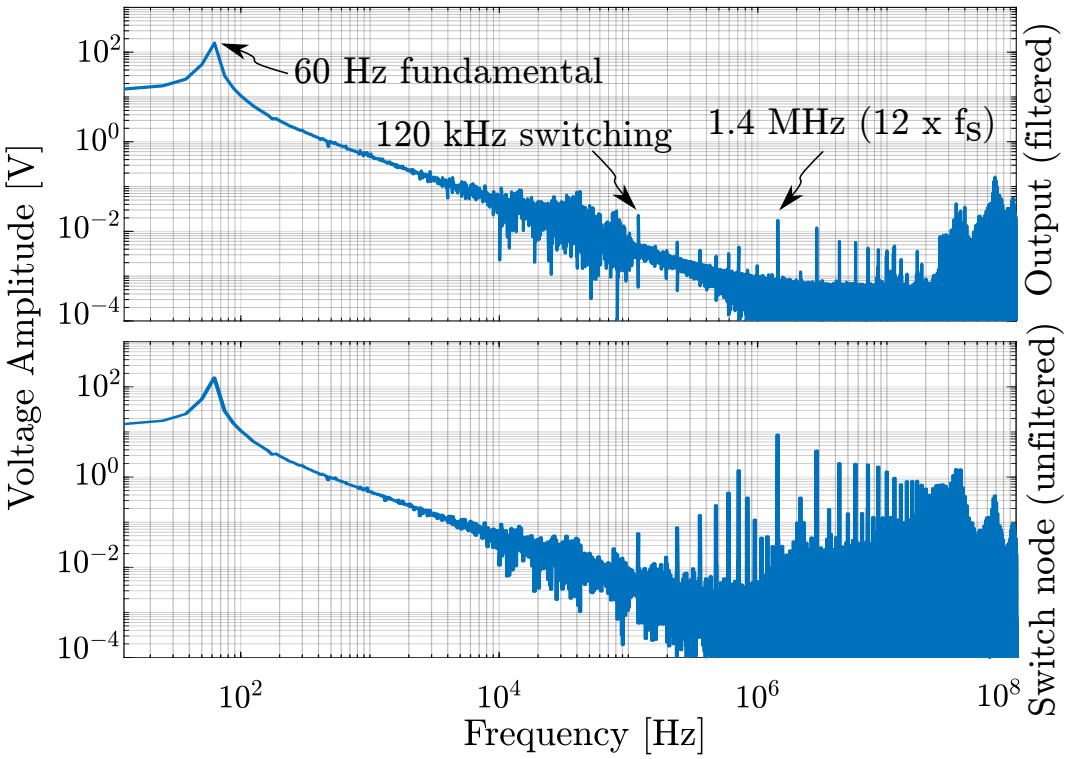


Figure 3.16: FFT of the measured filtered line voltage and the unfiltered switching node voltage.

Figure 3.15 shows output line current and switching node voltage for the 13-level FCML operating at 800 Vdc, 250 Vac, and highlights the frequency multiplication effect of PSPWM. The evenly spaced PWM steps in the Vx wavefrom of Fig. 3.15 highlight the good voltage balancing attained using the open loop, PSPWM approach. In the event of imbalanced capacitor voltage values, the 13 levels in the switch node voltage waveform will be blurred due to changes in voltage at each step in the PWM sequence. As shown in the left inset of Fig. 3.15, the 12 PWM signals are each shifted by 30°, and the overlapping effect of the phase shift results in an effective output frequency at the switching node of N-1 times the switching frequency of 120 kHz.

The frequency multiplication effect of the multilevel design is directly visible in the FFT of the inverter voltage plotted in Fig. 3.16. It can be seen that the multilevel architecture produces a very low THD fundamental sine wave at the modulation frequency of 60 Hz. The effective switching frequency is four orders of magnitude higher than the fundamental frequency at 1.44 MHz, minimizing filtering requirements. This high inductor pulse frequency enabled a low THD of 0.7% with only a 4.7 μH inductor.

3.6 Conclusion

This chapter has presented the design and hardware implementation of a 13-level flying capacitor inverter. By taking advantage of the low switching losses and high power density of GaN FETs it has been possible to build an efficient, power-dense 13-level FCML inverter which generates a nearly perfect sinusoidal output waveform. The voltage division of the FCML topology allows the use of 100 V switching modules to construct an 800 Vdc to 250 Vac inverter using low-voltage switches with a high figure of merit. The frequency multiplication of the FCML topology also enables the implementation of a 3.1 kW inverter operating with an effective switching frequency of 1.44 MHz which minimizes the output filtering requirements of the converter.

CHAPTER 4

ANALYSIS OF GAN-BASED FCML INVERTERS OPERATING IN LOW-TEMPERATURE ENVIRONMENTS

4.1 Motivation

Liquefied natural gas (LNG) has been proposed as a possible fuel for next-generation aircraft such as drones and quadcopters to reduce cost and minimize environmental impact [81–84]. Per unit of energy, natural gas has 23% lower CO_2 combustion emissions than conventional jet fuel in addition to reduced emissions of particulate matter and SO_2 [81]. LNG has the disadvantage of requiring more volume per unit of energy than jet fuel due to its lower mass density. However, at the moment of writing, LNG is less than 50% of the cost of jet A fuel per unit of energy and may offer aircraft operators a significant financial savings [85, 86]

Before combustion, LNG must be warmed from a storage temperature of -161 °C to operating temperature. This requirement opens the possibility for new system-level efficiency gains through using the thermal capacity of the LNG for system cooling including both the cooling of high-temperature superconductors and the power electronics required in hybrid fuel/electric systems. Capitalizing on these waste heat sources for fuel heating will reduce or eliminate the need to expend additional energy for fuel heating and potentially increase the feasibility of LNG-powered systems.

In addition to aviation applications, LNG is seeing increasing use in utility power generation systems. Recent advancements in gas extraction have lowered the cost of natural gas and made it very competitive for electricity generation. After overseas shipping in liquid form to minimize shipping cost, evaporation of LNG is often accomplished using thermal energy from seawater or ambient air before the fuel is burned. The cooling of the generation system and supporting power electronics is another option for utilizing this low-temperature potential energy [87].

To date, relatively little work has been done to evaluate WBG power transistors at ultra-low temperatures, and even less attention has been paid to the benefits for a complete converter incorporating WBG devices at ultra-low temperatures [88–91]. In this work the performance of a 1 kW, single-phase, 3-level inverter, using GaN power field effect transistors

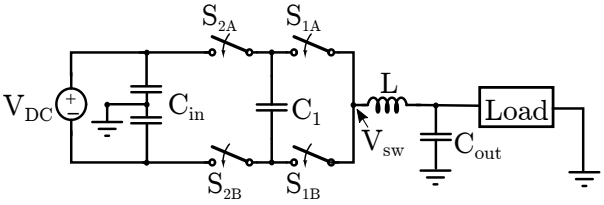


Figure 4.1: Schematic drawing of the 3-level GaN FCML inverter.

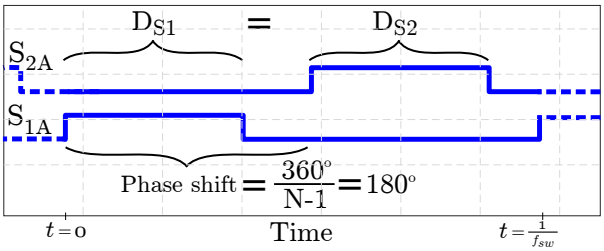


Figure 4.2: High-side gate signals for 3-level FCML driven with PSPWM.

(FETs) is evaluated at low temperature. The goal of the investigation is to verify system functionality, as well as quantify the efficiency and power density improvements possible through low-temperature operation. A 3-level flying capacitor multilevel (FCML) topology was chosen, as recent work has demonstrated its potential for very high power density and efficiency [10, 11, 54, 92].

The organization of this chapter is as follows. Section 4.2 discusses the consideration given to the effects of low-temperature operation on each component in the design. In addition to the GaN FETs, the impact of temperature on the capacitors and inductor required to build the FCML converter is also key to the overall converter efficiency at low temperature. In Section 4.3 the design of the converter hardware and thermal management as well as the construction of the test environment is discussed. The experimental results obtained for full converter operation are presented in Section 4.4 followed by a discussion of the elements of converter losses over the temperature range tested in Section 4.5. Finally, a review and summary are given in Section 4.7.

4.2 Impact of Low-Temperature Operation on Inverter Components

The benefits of the FCML topology have been discussed in Chapter 3. Building on that work, a 3-level FCML of a similar architecture was designed for evaluation under low-temperature conditions. The schematic diagram of the single-phase, 3-level FCML converter is shown in Fig. 4.1. Because the on-state resistance and capacitive parasitics of FETs are largely proportional to blocking voltage, the distributed switch voltage stress afforded by multilevel designs allows the FCML topology to maintain high efficiency despite the increased number of series switches and to distribute switching losses comparable to those of a 2-level design over a larger number of devices. This approach allows for better thermal management because of

the distributed heat load, and is especially helpful for achieving low-temperature operation of the GaN switches due to the increased cooling capability. As discussed, the power density of the FCML topology is also aided by the reduced amplitude of PWM voltage transitions and the accompanying reduction in required EMI filtering as compared to traditional 2-level designs.

As in Chapter 3, the 3-level FCML is driven using phase-shifted pulse width modulation (PSPWM) [53, 93] in which each gate signal is controlled at equal duty ratio and phase-shifted from adjacent signals by an angle of $\frac{360^\circ}{N-1}$ where N denotes the number of converter levels. In this 3-level converter, PSPWM control dictates that switch set S_1 in Fig. 4.1 is shifted 180° from switch set S_2, and switches A and B are complementary. Figure 4.2 shows the PSPWM gate signals for the high-side switches S_{1A} and S_{2A}.

The objective of this work is to extend the demonstrated benefits of the FCML topology to cryogenic applications. As cryogenic temperatures are well outside the range of performance specified in most component manufacturer data sheets, there is little information on the functionality of individual devices at low temperature. The remainder of Section 4.2 will discuss the impact of each component on the performance of the overall converter prototype.

4.2.1 FET Operation at Low Temperatures

Driven by the frigid hazards of space exploration [94, 95] and the opportunity to increase system-level efficiency through superconducting machines and power electronics [96–98], silicon FET performance at cryogenic temperatures has been studied extensively [99, 100]. Reductions in on-state resistance of 5-10 times have been demonstrated for some devices [101], as well as reduced diode reverse recovery and faster switching times yielding on the order of 25% reduction in total switching loss [102]. Additionally, silicon FET threshold voltages tend to rise slightly ensuring robust operation [101].

In the face of these benefits, there are also some challenges with the cryogenic operation of silicon devices. Although on-state resistance decreases as the temperature is lowered from ambient, below 77 K (-196 C) this trend reverses and conduction is limited by carrier freeze-out. The blocking voltage of Si devices has also been shown to decrease by 20%-30% at liquid nitrogen temperatures [100, 102].

Wide bandgap GaN and SiC devices have been gaining traction in research and some industrial applications with the majority of focus being placed on the high-temperature capabilities of the devices. However the improved figures of merit of wide-bandgap devices, minimal or no reverse recovery current (for SiC and GaN respectively), as well as high

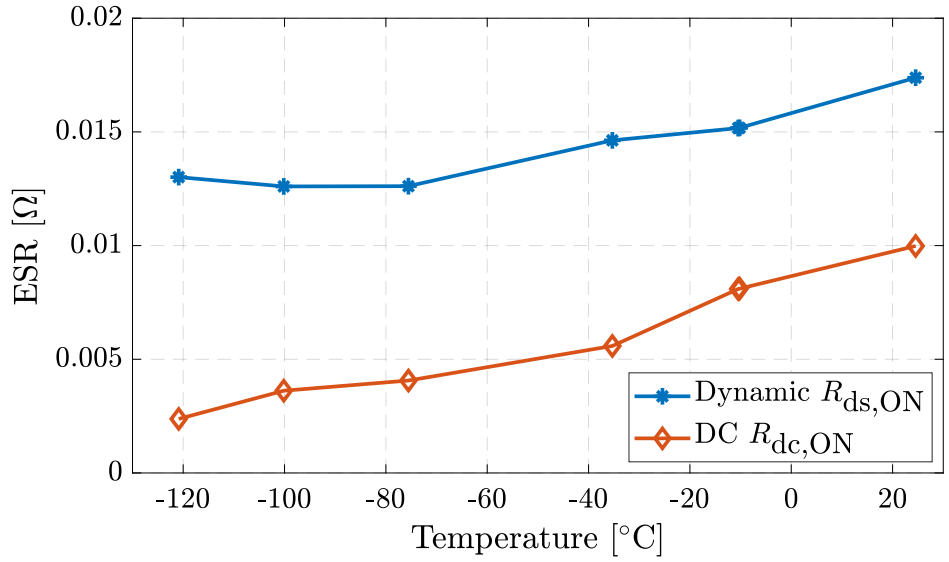


Figure 4.3: Measured dc and dynamic $R_{\mathrm{ds,ON}}$ of EPC2034 over temperature. While dc measurements suggest a $\approx 76\%$ reduction, the dynamic on-state resistance only decreases by ≈ 27 %, and shows a slight increase below -80 °C [13, 103].

conductivity have prompted investigation into the cryogenic operation of these devices. Additionally, the inherent radiation hardness of the wide-bandgap structure makes these devices potentially useful in space applications.

With their higher voltage ratings, SiC devices are appealing for many high-power applications such as cryogenic machines. It has been shown that the breakdown voltage of SiC devices holds roughly constant under cryogenic conditions as does the threshold voltage. Thus the devices are stable and functional at low temperature [104, 105]. However, although the devices are stable at cryogenic temperatures, their conduction and switching losses increase significantly. SiC on-state resistance increases much more quickly than Si due to carrier freeze-out and electron trapping, with a significant increase in resistance at temperatures below 200 K (-73 C) [26]. Additionally, SiC FET switching tends to slow down, which increases switching losses and the body diode exhibits a higher voltage drop [91, 106]. Thus while SiC devices are potentially functional at low temperatures, there appears to be no efficiency benefit to be gained.

Gallium nitride devices have also been tested for operation under cryogenic temperatures. GaN devices do not suffer from carrier freeze-out at low temperature and exhibit significant reduction in dc conduction resistance. Additionally, GaN switching losses have been shown to decrease as the temperature is lowered and the blocking voltage exhibits minimal change [91, 107, 108].

In [13] the authors documented the performance of the EPC2034, a high electron mobility

transistor (HEMT), from ambient down to -195 C. The dc on-state resistance for the device decreased to 20% of its nominal value without any sign of carrier freeze-out, as shown in Fig. 4.3. The device operation also remained stable as the threshold voltage was relatively unchanged over the range tested. It should be noted that recent evaluation of higher voltage (i.e., 650 V) GaN devices [108] has shown a significant reduction in threshold voltage at low temperature, suggesting threshold tolerance at low temperatures differs between various GaN devices and voltages.

Historically, one drawback of GaN has been the phenomenon of dynamic on-state resistance or dynamic $R_{\mathrm{ds,ON}}$ which is a decaying $R_{\mathrm{ds,ON}}$ exhibited when the device transitions from blocking voltage to conducting [109]. Dynamic $R_{\mathrm{ds,ON}}$ is the result of electron trapping during the off-state of the device and is accentuated by higher blocking voltage stress and device temperature. The elevated conduction resistance of dynamic $R_{\mathrm{ds,ON}}$, which decays on the order of milliseconds, dictates that the functional $R_{\mathrm{ds,ON}}$ of the device in a switching power converter may be as high as twice the dc value provided in manufacturer data sheets. A detailed method of characterizing device $R_{\mathrm{ds,ON}}$ as a function of blocking voltage and temperature is presented in [103]. Additional measurements have also been taken of the dynamic $R_{\mathrm{ds,ON}}$ of the EPC2034 device and are in the process of publication.[1]

The measurements in Fig. 4.3 show that although there is no carrier freeze-out exhibited in the dc $R_{\mathrm{ds,ON}}$ of the tested GaN transistor, the dynamic $R_{\mathrm{ds,ON}}$ of the EPC2034 exhibits functionally similar behavior as the effective on-state resistance decreases and then increases slightly as the device is cooled below -80 °C. This trend of increased impact from dynamic $R_{\mathrm{ds,ON}}$ at low temperature is alluded to in [110] where it was found that the drain-to-source current under pulsed transient analysis was significantly more distorted at 100 K than at 300 K. It is believed that extra time is required for the trapped carriers to gain kinetic energy at cryogenic temperatures. Additionally, the effect was only visible at the higher tested value of V_{ds}, again pointing to the impact of blocking voltage on dynamic $R_{\mathrm{ds,ON}}$. Recent generations of GaN devices exhibit dramatically reduced $R_{\mathrm{ds,ON}}$ and the performance of these devices will continue to improve.

4.2.2 Gate Driver and Isolator Characterization

In [13] the authors demonstrated that the LM5113 half-bridge gate driver functioned well down to -195 °C. The only change in behavior was a decrease in both the turn-on and turn-off time of the gate driver. The equal decrease in both functions is attributed to the higher

[1]The author thanks Thomas Foulkes for providing the measurements of dynamic $R_{\mathrm{ds,ON}}$ under cryogenic conditions referenced here.

electron mobility of silicon at low temperature and meant that the operation of the GaN switch would be unchanged and an equal duty ratio and dead-time can be used.

In addition to gate drive ICs, the FCML topology requires gate driver isolation due to the multiple flying switching nodes. The ADUM5210 and SI8423BB-D-IS devices were used for power and signal isolation respectively. During testing it was found that the ADUM5210 provided a stable isolated voltage over the temperature range of interest. As for the LM5113, the signal propagation rate of the SI8423BB-D-IS increased slightly due to the change in electron mobility of silicon. The change in signal propagation time was slightly less than the change in the LM5113 response rate due to the lower current required for signal driving as compared to the current required to charge the gate of EPC2034 FET.

4.2.3 Capacitor Characterization

Because capacitors play a critical role in the FCML converter operation it is important to understand their loss characteristics over temperature. As discussed in Chapter 2, multilayer ceramic capacitors (MLCCs) exhibit some of the highest energy storage density among dry electrolytic devices. MLC capacitors are grouped into three main classifications by IEC/EN 60384-1, of which two are most commonly used in power electronics applications. Class I capacitor dielectrics are paraelectrics with good capacitance stability over temperature and bias voltage but relatively low energy storage density. Class II capacitor dielectrics are ferroelectrics with higher energy density, but these devices also exhibit higher variability over temperature and a decrease in capacitance with applied voltage bias. Within these classifications, devices are tailored for a range of operating temperatures, each designated by a three character code.

In order to understand the impact of cryogenic operation on MLCCs, six different devices were tested using the large-signal, low-frequency technique outlined in Chapter 2 over the temperature range of interest. In this test, the capacitor voltage was cycled from zero to rated voltage at 60 Hz, and energy flowing into and out of the capacitor was measured using Yokogawa WT310 power meters. Based on the capacitor round-trip energy efficiency, the capacitor losses and equivalent ESR can be calculated. Figure 4.4 shows the relative change in ESR for each device over the temperature range tested.

It can be observed that the devices comprised of ferroelectric dielectric materials (X7T, X7R, X6S) exhibit a measurable increase in ESR as their temperature decreases. The same holds for the CeraLink capacitor which uses an antiferroelectric dielectric designed to exhibit maximum capacitance at rated bias [111]. The increase in ESR at low temperature

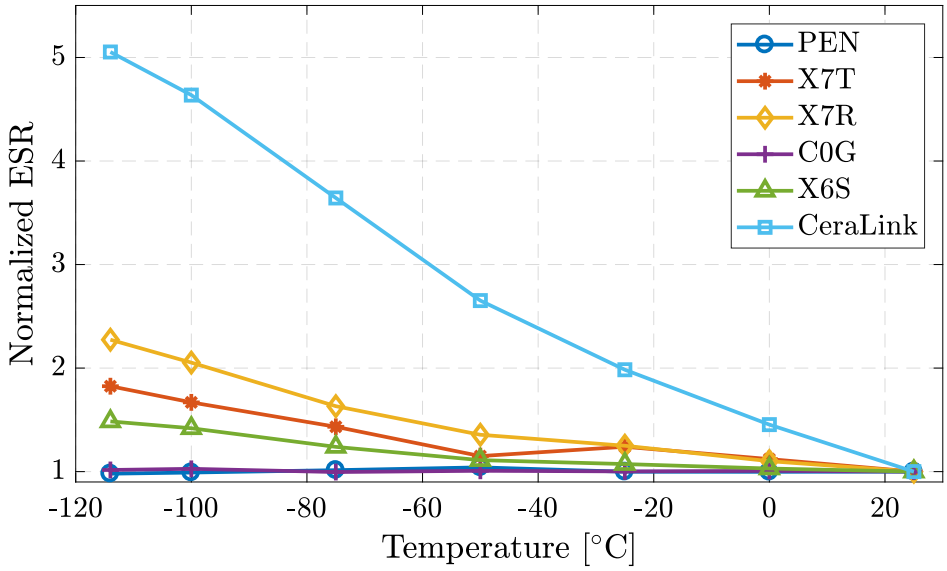


Figure 4.4: Measured large signal ESR over temperature normalized to ambient value for several different capacitor dielectrics. Measurements are taken using the large signal test outlined in [6].

is especially pronounced in the CeraLink device as a consequence of the fact that the device composition is tailored for high-efficiency operation at temperatures of up to 150 °C to facilitate high-temperature power conversion. These findings for Class II devices are substantiated by prior literature [112], and similar results have been shown for solid tantalum capacitors [113, 114]. It is suspected that the higher dielectric loss in ferroelectric dielectrics at low temperature is the result of an increase in ferroelectric coercive field at low temperature [112].

In contrast to the high permittivity Class II materials, the Class I ceramic and film-based PEN capacitors exhibit negligible change in ESR over temperature, corroborating the trend noted in [115]. This is because Class I capacitors such as COG are made of a paraelectric, low-permittivity material and are very stable over temperature and voltage bias. This suggests that Class I dielectrics and film-based capacitors may be preferable in cryogenic applications provided they are able to meet energy density requirements. A significant drawback of COG and film-based dielectrics is their lower permittivity as compared to Class 2 ceramics. For applications requiring higher permittivity and higher density energy storage, fully functional capacitors using dielectrics optimized for operation near 77 K have been tested and may play a role in the design of future LNG or otherwise cryogenically cooled systems [115, 116]. In addition to having optimal permittivity at low temperature, these dielectrics also exhibit higher dielectric breakdown strength and higher thermal conductivity at cryogenic temperatures.

The X6S device was selected for this work due to its high energy density [6] and acceptable temperature performance. In specific applications, designers may be more likely to select a lower energy density technology with potentially lower ESR at cryogenic temperatures.

4.2.4 Inductor Characterization

Inductors of the IHLP series from Vishay were used in this work as they offer a wide selection of devices with low form factor and integrate well with the cold plate-based cooling. Although inductor losses can be calculated using Steinmetz equation based on known material properties, material properties are not published for cryogenic temperatures. Thus if loss estimates are needed, it is necessary to experimentally measure inductor losses directly.[2]

The direct electrical measurement of inductor losses in a power converter is challenging due to the requirement for wide-range, high-accuracy, voltage measurements at high frequency. Inductor losses manifest as small voltage drops on the order of millivolts which must be measured accurately in the presence of high-frequency switching voltage waveforms on the order of several tens of volts. In this work the 3-level FCML generates an effective inductor ripple frequency at up to 240 kHz, which is twice the switching frequency, due to the frequency multiplication effect of FCML converters driven using phase-shifted PWM (PSPWM). In order to characterize relative inductor losses for this design over the temperature range of interest, a careful multi-step measurement process combining electrical and calorimetric methods was followed. The combined strategies were used for validation of electrical measurements and because calorimetric methods are challenging at cryogenic temperatures.

Calorimetric loss measurements rely on a thermal mass with a known volume, density and specific heat to capture losses generated from the DUT. The thermal mass is located in an isolated chamber with high thermal impedance to ambient, and any energy dissipated by the DUT into the thermal mass is exhibited as an increase in mass temperature. The thermal impedance from the mass to ambient, and indeed the exact specific heat of the thermal mass, can be calibrated based on a known power dissipation.

In this work the system was calibrated using the DUT inductor with a DC current of 10 A_{dc}. The exact dissipation in the inductor during the calibration run was known based on the DC current passing through the inductor and the voltage across the terminal. The rise in thermal mass temperature over time was measured using thermocouples and the Fluke Hydra

[2]The measurements of inductor loss discussed here were taken by Oscar Azofeifa and originally published in [15] with the author's oversight and direction. These measurements have been incorporated into the loss analysis in this work.

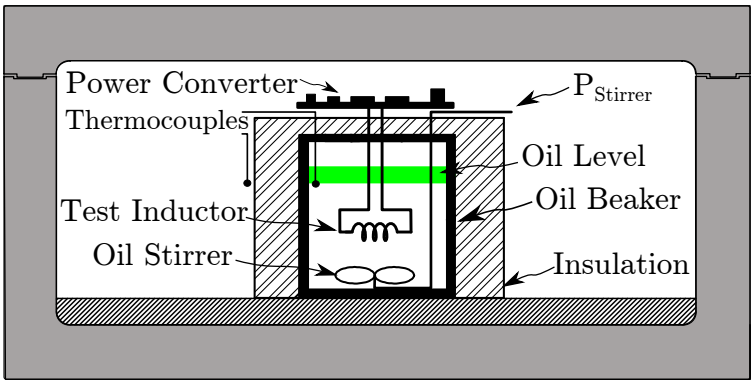


Figure 4.5: Cooler-housed calorimetric measurement system cutaway. Power converter replaced with DC source for calibration.

DAQ controlled by a LabView VI. In order to maintain a constant temperature throughout the oil, a stirring motor was submerged in the oil. Because the stirring mechanism was completely submerged, both the losses and stirring motion contributed to oil heating. The power applied to the stirrer (P_{stirrer}) was therefore added to the power dissipated in the inductor (P_{loss}) to determine overall dissipation in the oil (P_{cal}) such that

$$P_{\text{cal}} = P_{\text{loss}} + P_{\text{stirrer}}. \tag{4.1}$$

The relationship between the change in oil temperature over time and the power dissipated in the oil is then characterized as

$$P_{\text{cal}} = (m_{\text{oil}}\ C_{\text{oil}} + k)\left(\frac{\Delta Temp}{\Delta t}\right), \tag{4.2}$$

where the parameters m_{oil}, C_{oil}, and Δt are the total mass of oil, the heat capacity of the oil and the change in temperature of the oil respectively. The factor k is the calibration factor for the test system and was calculated based on the known power dissipation during the DC calibration test and the measured rise in the temperature of the oil. This factor accounts for the thermal mass of the glass beaker and the heat loss from the system. It was assumed that the thermal impedance to ambient remained constant over the 25 °C to 40 °C temperature swing used for testing. The overall layout of the test chamber is shown in Fig. 4.5.

With the calibration factor known, the calorimetric test system was used to measure the loss in the inductor of the FCML converter while operating in dc-dc mode at a constant duty ratio. In an effort to increase the proportion of core losses in the measurement, two inductors were used in parallel and a length of wire was added between the inverter and the IHLP-676GZ-01 inductors thus allowing them to be submerged in the beaker of oil while

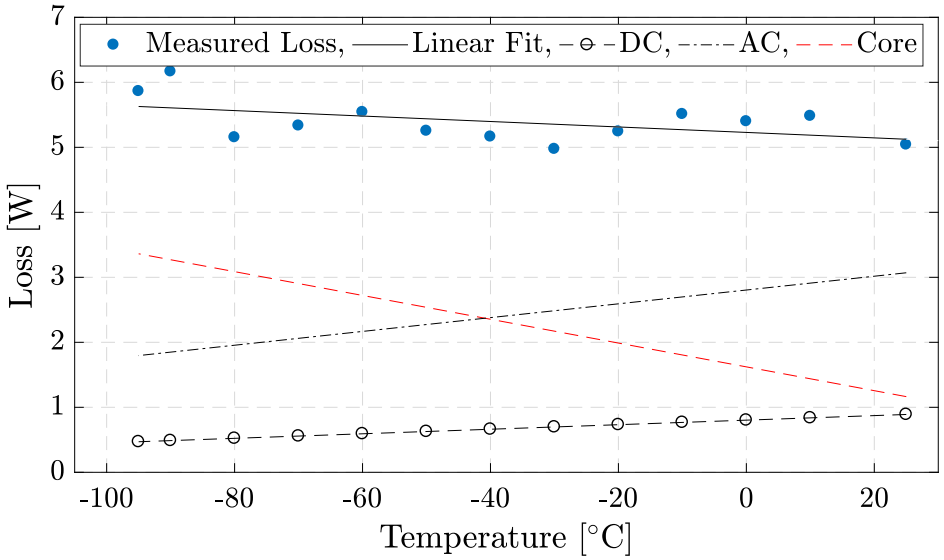


Figure 4.6: Electrically measured losses for two parallel inductors in dc-dc test. $V_{\text{in}} = 100$ V, $D = 0.75$, $I_{\text{load}} = 7.4$ A, $I_L = 8.3$ A_{RMS}, $F_{\text{sw}} = 70$ kHz, $F_{\text{effective}} = 140$ kHz. It is observed that the overall losses remain relatively stable indicating that core losses increase to account for the difference between the measured loss and the known decrease in conduction and AC losses based on the temperature coefficient of copper.

the converter was positioned above the beaker. The converter duty ratio was set at 75% in order to maximize the current ripple in the inductor and accentuate potential losses in the core material [73]. The converter was then run at a power level of 1.2 kW between source at 100 V, and a load at 75 V. Solving (4.1) and (4.2) for P_{loss}, the power dissipated in the inductor during converter operation was found to be 6.0 W. This value is also in reasonable agreement with manufacturer-supplied loss estimates for this operating condition [117].

After experimentation and multiple iterations, the DA1855A differential amplifier from Teledyne LeCroy with a DXC100A passive probe was selected for voltage measurements. This instrument has a signal conditioning preamplifier with a high common-mode rejection ratio of 94 dB at 100 kHz. A high common-mode rejection ratio proved essential for accurately measuring the average voltage across the inductor in the range of millivolts in the presence of an instantaneous voltage that fluctuated several tens of volts. In addition to the DA1855A/DXC100A combination used for measuring inductor voltage the CP030A current probe was used to measure current flowing through the inductor and data was sampled at 10 GS/s using the HDO6104A Oscilloscope. Average power lost in the inductor was calculated based on a running integral of the instantaneous power over 400 nsec or 24 effective switching cycles at the converter switching node. After proper configuration of the measurement equipment, the electrically measured loss fell within 5% of the calorimetric measurements,

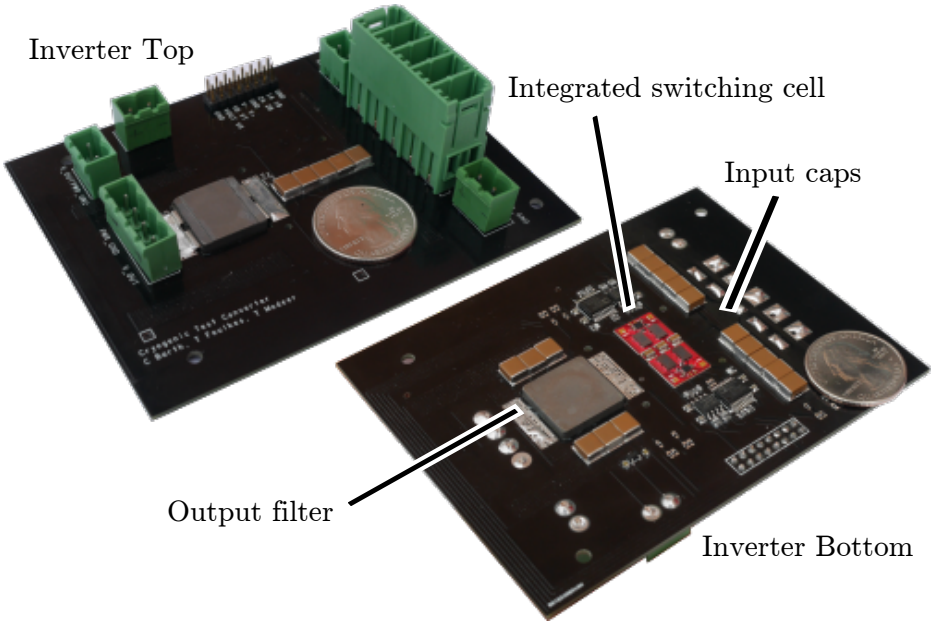


Figure 4.7: Top and bottom view of 3-level inverter.

validating that an effective system for electrically measuring loss, and, in particular, change in loss over temperature, had been achieved.

After validation of the electrical measurement configuration, measurements of inductor loss were then taken at inductor core temperatures from 25 °C down to -95 °C. Figure 4.6 plots electrically measured inductor losses over temperature for a single test condition. Due to the sensitivity of the measurement there is a notable variation between data points; however, the trend in the data is gives an understanding of trend in core material losses over temperature. It can be seen that the overall inductor loss remained relatively constant over the temperature range tested; however, this is understood to be due to the conflicting trends between the reduction in copper resistivity and the increasing losses in the ferrite core. Based on the inductor current ripple, the dc and ac losses can be estimated using the modified Steinmetz equation (MSE) incorporating the change in the resistivity of copper [117, 118]. The coefficient of resistivity for copper is 0.393% per °C, therefore inductor ohmic resistance decreased by 49% between 25 °C and -100 °C leading to a 49% reduction in both the ac and dc winding losses. The remaining losses after the removal of the ac and dc winding loss are understood to be core losses which increase by a factor of ≈ 3 in order to account for the measured trend in overall losses. This agrees with prior research documenting the increasing losses in ferrite material at cryogenic temperatures [119, 120].

Table 4.1: Inverter component list.

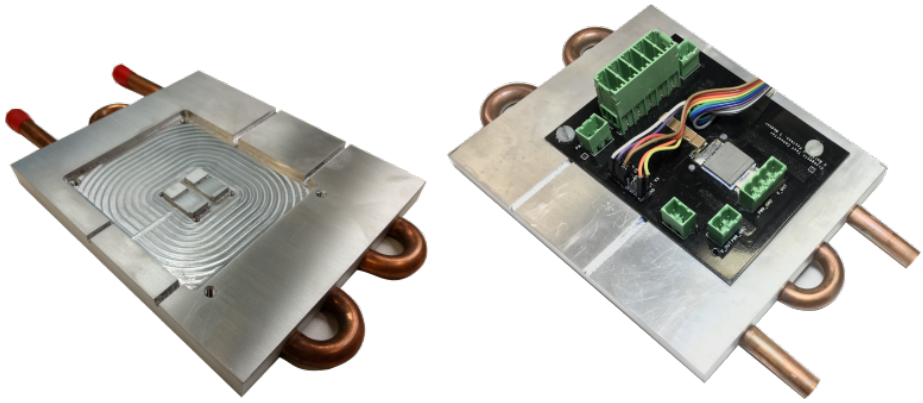
Component	**Part Number**	**Parameters**
GaN switches	EPC 2034	200 V, 7 mΩ
GaN gate driver	Texas Instrument LM5113	5 V, half bridge
$R_{\text{gate,on}}$		22.5 Ω
$R_{\text{gate,off}}$		0.5 Ω
Flying Cap., C_1	TDK C5750X6S2W225K250KA x5	2.2 μF, 4.3 mΩ
Filter Cap., C_{out}	TDK CGA9Q1C0G2J104J280KC x6	0.1 μF, 0.5 mΩ
Inductor, L	Vishay IHLP6767GZER220M11	22 μH, 25 mΩ
Signal isolators	Silicon Labs Si8423BB-D-IS	
Signal Filters	R = 229 Ω , C = 47 pF	
Isolated power	Analog Devices ADUM5210	
PWM Generator	TI TMS320F28069	

4.3 Development of Low-Temperature Inverter and Test Chamber

4.3.1 Final Converter with Thermal Management

An annotated photograph of the full 3-level FCML converter hardware prototype is shown in Fig. 4.7. In order to provide sufficient flying capacitance and minimize trace lengths and parasitic switching loop inductance, the flying capacitance is divided into two sections. The bulk of the capacitance is located below the PCB opposite the switches. The parasitic inductance of the commutation loop is further reduced through the use of local decoupling capacitors as discussed in Section 3.2.5. To ensure all devices are cooled to a similar temperature, the supporting electronics such as signal isolators, gate drivers, input bus capacitors, and the output filter capacitors are located with the GaN devices on the bottom of the inverter PCB. A complete component listing is given in Table 4.1.

The converter is cooled using a cold plate machined to the negative height of the primary converter components as depicted in Fig. 4.8. The clearance between the cold plate surface and the GaN devices was set at 0.02", and a uniform cavity was milled into the remainder of the cold-plate to provide 0.04" clearance for the inductor and filter capacitors. A hole for the output filter inductor was milled through the PCB so that the inductor is recessed through the PCB and located at the same height as the filter capacitors, thus minimizing the overall height of the PCB and cold plate. The entire cavity of the cold plate was covered with Bergquist gap filler 4000 in order to provide a good thermal interface and even cooling of the components on the lower side of the inverter.



Cold plate Inverter mounted to cold plate

Figure 4.8: Milled cold plate and cold plate with the FCML inverter.

4.3.2 Design of Cryogenic Test System

Cryogenic cooling in ambient moisture levels will lead to water vapor condensation and icing on the power converter. To prevent icing, the converter and cold plate were placed inside a Lesker vacuum chamber and purged with nitrogen gas. The chamber and cold plate test configuration is shown in Fig. 4.9 and Fig. 4.10. After purging the chamber of humidity, liquid nitrogen (LN2) was drawn through the cold plate using an Instec model LN2-P8AD10 8-stage pump. The flow rate of the LN2, and consequently the temperature of the cold plate, was determined by manually controlling the speed of the pump.

In order to minimize the heat absorbed by the LN2 as it was pumped up from the dewar into the cold plate, the LN2 feed line and cold plate were heavily insulated. Thermocouples were attached directly onto the integrated switching cell, the cold plate surface, the LN2 input line, the LN2 output line, and on the inductor. These temperatures were tracked and logged along with electrical measurements of voltage, current, and power at the input and output of the converter taken using Yokogawa WT310 digital power meters and a National Instruments LabVIEW automated data collection virtual instrument as shown in Fig 4.10.

4.4 Low-Temperature Performance of FCML Inverter

Figure 4.11 shows the 3-level switching node voltage and output current for normal operation of the 3-level converter, operated to produce a sinusoidal output voltage (i.e., as an inverter). Figure 4.12 shows the overall converter losses measured electrically with a Yokogawa WT310

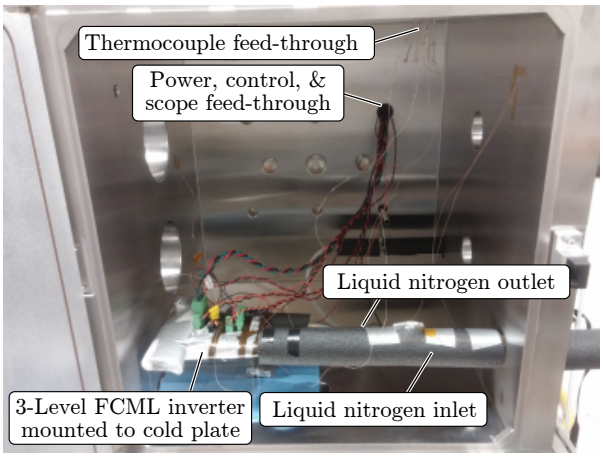


Figure 4.9: Vacuum chamber with converter configured for testing. Thermocouples, power and LN2 were passed through feedthroughs to the converter.

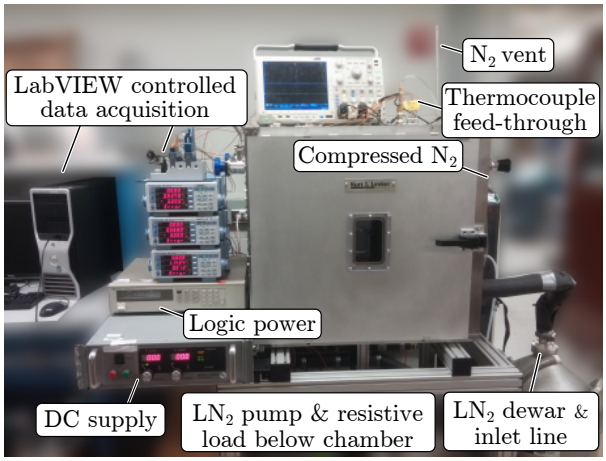


Figure 4.10: Complete cryogenic experimental setup with NI LabVIEW data acquisition.

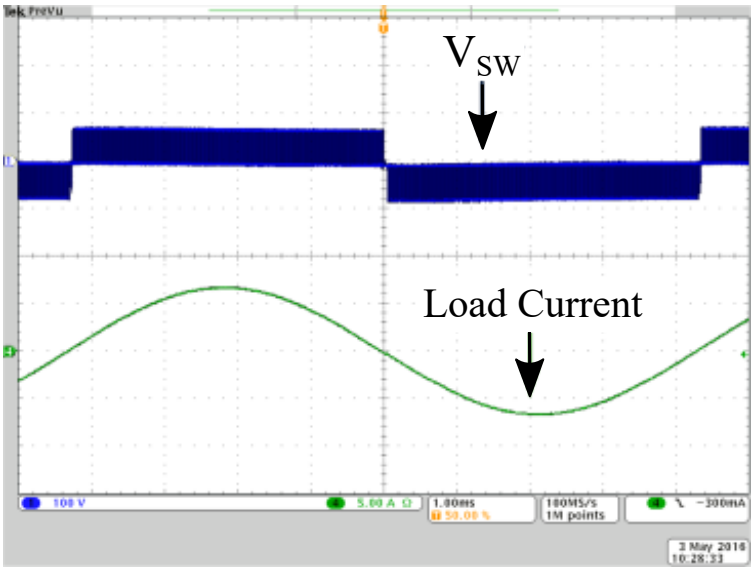


Figure 4.11: Waveforms showing the output current and the switching node voltage (V_{SW}) of the 3-level GaN converter.

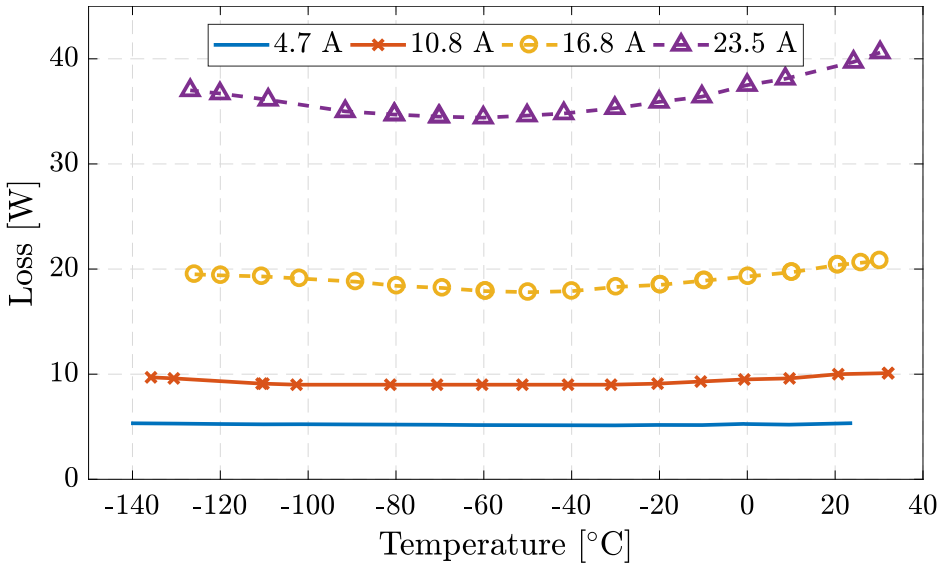


Figure 4.12: Converter losses at four different loads. At higher load conduction losses dominate and there is a measurable decrease in losses down to −60 °C.

and Fig. 4.13 displays the corresponding converter efficiency as a function of temperature for each load current tested. Operating between 150 V_{dc} and 45 V_{RMS} the converter was tested at four different load currents from light to rated load and operated successfully with a cold plate heatsink temperature between ambient and −140 °C. The finite cooling capability of the cold plate and Instec liquid nitrogen pump limited the lowest temperature achievable as the converter load and losses increased. For this reason the light-load temperature sweep with 5 W of loss is cooled ≈ 10 °C further than the full load case with 40 W of loss as shown in Fig. 4.12 and Fig. 4.13. The data in Fig. 4.12 and Fig. 4.13 was taken for a fixed load over a temperature sweep. This approach required significantly more time than would have been required to test four different power levels as the converter was cooled from ambient. Taking data over a temperature sweep ensured that the system was in thermal equilibrium throughout the test and minimized thermal stress which would be accentuated during a step in converter output power due to the FET temperature quickly increasing without coming to thermal equilibrium with the PCB. The EPC 2034 GaN FETs used in this work are fabricated on a passivated die with solder bumps. This configuration is important for minimizing commutation loop inductance and switching losses, but it also makes the device susceptible to mechanical stress [79] due to disparity between the FET and PCB coefficients of thermal expansion.

At the low power level of 4.7 A, the switching and core losses dominate over the conduction losses and therefore there is little reduction in overall losses over the temperature sweep. A similar trend holds at the 10.8 A load as the loss curve is still roughly constant over

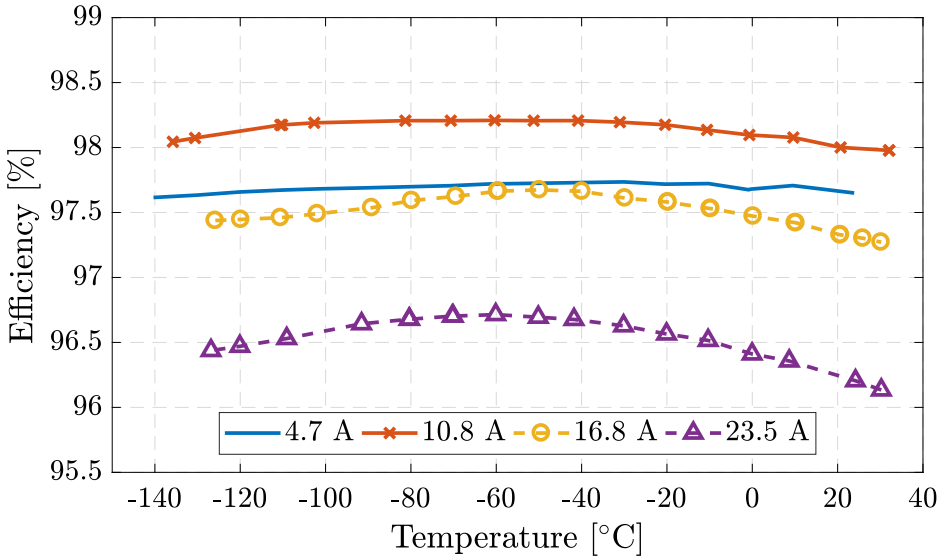


Figure 4.13: Measured efficiency versus temperature for four different load levels. At light load the converter losses are dominated by switching and therefore there is minimal change in efficiency with temperature.

temperature. As the current is increased to 16.8 A and 23.5 A, the ohmic losses in the converter are a higher percentage of overall losses so there is measurable decrease in losses over the first half of the temperature sweep until approximately −60 °C. At a cold plate temperature of −60 °C and rated 23 A load, a 16% reduction in losses was achieved compared to RT operation. This resulted in a 0.6% increase in efficiency from 96.1% to 96.7%. The highest efficiency of 98.2% was measured at −50 °C with an output load of 10.8 A or 500 W. As the converter is cooled below −60 °C losses begin to climb again.

4.5 Analysis of Inverter Losses Over Temperature

The decrease in converter losses from ambient to −60 °C followed by a slight increase in loss for lower temperatures can be understood at a qualitative level by considering the component analysis discussed in Sections 4.2.1-4.2.4. This trend was unexpected based on the results presented in [13], which suggested that the efficiency of the converter would continue to decrease with decreasing temperature. However, as shown in Fig. 4.3 and explained in Section 4.2.1, the functional dynamic $R_{\mathrm{ds,ON}}$ of the EPC2034 GaN FETs was shown to decrease to −80 °C and then taper off with potentially a slight increase. Combined with the increasing losses exhibited in both the ceramic capacitors as shown in Fig. 4.4, and the increasing core loss in Fig. 4.6, the trend in losses found experimentally in Fig. 4.12 is

reasonable. Indeed, only copper losses are reduced unequivocally by lowering temperature, and for moderate loads with low inductor current ripple (low ac losses), ohmic copper losses may not be dominant. In order to explore the trend in converter losses over temperature, a loss model was created taking component temperature dependencies into account.

Referring to Fig. 4.1 it is clear that switch pairs A and B are forced to be complementary; therefore, the converter conduction losses for an N-level converter are the result of the RMS inductor current ($I_{\mathrm{L,RMS}}$) flowing through the conduction resistance of N-1 switches, or one switch in each pair. The conduction losses ($P_{\mathrm{FET_{cond}}}$) for the transistors can be calculated as

$$P_{\mathrm{cond_{FET}}} = (N-1)\ R_{\mathrm{ds,ON}}(\mathrm{T_{FET}})\ I^2_{\mathrm{L,RMS}}, \tag{4.3}$$

where the conduction resistance ($R_{\mathrm{ds,ON}}$) is a function of the temperature of the GaN FET ($\mathrm{T_{FET}}$).

The energy lost in the FET parasitic capacitance ($P_{\mathrm{FET_C}}$) is proportional to the switching frequency (f_{sw}) and roughly proportional to the output capacitance of the FET (C_{oss}). In reality, the output capacitance is non-linear and the charge stored in the output capacitance (Q_{oss}) must be determined as a function of blocking voltage (V_{ds}) according to manufacturer specifications. The switches in an FCML converter are symmetrical with each blocking the voltage between adjacent capacitors when they are closed. For (N-1) complementary pairs of switches, the worst-case loss can be calculated as

$$P_{\mathrm{FET_C}} = 2\ (N-1)\ Q_{\mathrm{oss}}(V_{\mathrm{ds}})\ f_{\mathrm{sw}} \approx (N-1)\ C_{\mathrm{oss}} V^2_{\mathrm{ds}} f_{\mathrm{sw}}. \tag{4.4}$$

As mentioned, this is the worst-case condition. In operation the Q_{oss} is reduced through the discharge of the output capacitance during the dead-time between switch transitions and therefore partial soft-switching occurs. This partial soft switching is accounted for in the loss assessment. The overlap losses per switch pair ($P_{\mathrm{FET_{SW}}}$) can be calculated over time (t) as

$$P_{\mathrm{FET_{SW}}} = (N-1)\ f_{\mathrm{sw}}\ (E_{\mathrm{ON}} + E_{\mathrm{OFF}}), \tag{4.5}$$

where the turn-on and turn-off energy are calculated as

$$E_{ON/OFF} = \frac{t_{\mathrm{ON/OFF}}\ V_{\mathrm{ds}}\ I_L}{2}. \tag{4.6}$$

The notation $t_{\mathrm{ON/OFF}}$ designates the turn-on and turn-off transition periods of the switch.

These times were estimated using,

$$t_{\mathrm{ON/OFF}} = \frac{Q_{\mathrm{G}}}{I_{\mathrm{G_{ON/OFF}}}}, \tag{4.7}$$

where Q_{G} is the gate charge of the GaN power FET, and $I_{\mathrm{G_{ON/OFF}}}$ are the gate turn-on and turn-off currents respectively during the switching process, which are calculated from

$$I_{\mathrm{G_{ON}}} = \frac{V_{\mathrm{DR}} - V_{\mathrm{TH}}(\mathrm{T_{FET}})}{R_{\mathrm{ON}}}, \tag{4.8}$$

and

$$I_{\mathrm{G_{OFF}}} = \frac{V_{\mathrm{TH}}(\mathrm{T_{FET}})}{R_{\mathrm{OFF}}}. \tag{4.9}$$

The term V_{DR} is the gate drive voltage, and R_{ON} and R_{OFF} are the turn-on and turn-off resistances respectively. Finally, V_{TH} is the threshold voltage, which is temperature dependent. The temperature dependence of V_{TH} was measured in [13].

The device temperature was calculated based on the total power dissipated from the device ($P_{\mathrm{FET_{total}}}$), the temperature of the cold plate ($\mathrm{T_{plate}}$), and the thermal impedance of the gap filler (R_{TH}) between the FET and cold plate as

$$T_{\mathrm{FET}} = T_{\mathrm{plate}} + R_{TH}\ P_{\mathrm{FET_{total}}} \tag{4.10}$$

where $P_{\mathrm{FET_{total}}}$ is the summation of the losses discussed in (4.3) - (4.5) or

$$P_{\mathrm{FET_{total}}} = P_{\mathrm{FET_{cond}}} + P_{\mathrm{FET_{sw}}} + P_{\mathrm{FET_C}}. \tag{4.11}$$

In addition to the FET losses, losses in the capacitors, inductor, and PCB were also taken into account. Referring to Fig. 4.4 it is evident that the power dissipated in the effective ESR of the X6S flying capacitors (P_{C}) increases as the temperature is reduced. The nominal ESR of the devices at the switching frequency is on the order of 7 mΩ [8] and there are 5 devices configured in parallel. During converter operation, current flows through the flying capacitors when the adjacent complementary switch pairs are in opposing positions.

The length of the charge and discharge interval is dependent on the converter duty ratio (D) and the phase shift of the converter. Applying the relationships introduced in Section 3.2.2, in a 3-level FCML the charge and discharge times are both equal to $D \cdot \frac{1}{f_{sw}}$ for $D < \frac{1}{2}$ and $(1-D) \cdot \frac{1}{f_{sw}}$ for $D > \frac{1}{2}$. Based on the capacitor duty cycle, the capacitor losses

as a function of temperature can be calculated as

$$P_C = I_C^2 \; ESR_C(T), \tag{4.12}$$

where the total capacitor current (I_C) is calculated as

$$I_C = \begin{cases} I_L \; \sqrt{2D}, & \text{for } D < \frac{1}{2} \\ I_L \; \sqrt{2(1-D)}, & \text{for } \frac{1}{2} > D > 1 \end{cases} \tag{4.13}$$

As mentioned in Section 4.2.4, inductor losses can be divided into dc, core, and ac losses. Inductor dc loss ($P_{\mathrm{L_{dc}}}$) is determined as a function of temperature by scaling the nominal inductor resistance by the temperature coefficient of copper. The conduction loss is then calculated simply as

$$P_{\mathrm{L_{dc}}} = R_{\mathrm{L}}(T) \; I_{\mathrm{L,RMS}}^2, \tag{4.14}$$

where $I_{\mathrm{L,RMS}}^2$ considers both the fundamental and ripple components of the current output. Numerous solutions have been proposed for the modeling of core losses in magnetic material. Because if the complex nature of the loss generation under magnetic fields, the majority of models use curve fitting to express measured loss characteristics in a mathematical form. The Steinmetz equation which assumes sinusoidal magnetic excitation is the starting point for many of these methods. For core loss calculations in the this work a form of the modified Steinmetz equation (MSE) was used which accounts for nonsinusoidal switching waveforms [121]. In this approach, an effective frequency (f_{eq}) may be defined which accounts for the rate of change of flux in the core magnetic material. Defining the magnitude of the change in flux as

$$\Delta B = B_{\max} - B_{\min}, \tag{4.15}$$

the effective frequency can be defined based on period (T) as

$$f_{\mathrm{eq}} = \frac{2}{\Delta B^2 \pi^2} \int_0^T \left(\frac{dB}{dt} \right)^2 dt. \tag{4.16}$$

With the aid of the effective frequency, the power loss density can be calculated as

$$P_h = k_{\mathrm{eq}} \left(\frac{f_{\mathrm{eq}}}{f_b} \right)^{\alpha - 1} \left(\frac{\Delta B}{2 B_{\mathrm{b}}} \right)^{\beta} \frac{f}{f_{\mathrm{b}}} \tag{4.17}$$

where f_{b} and B_{b} are the base frequency and base flux density respectively. The exponents α and β are experimentally-determined material properties. The ac winding losses were

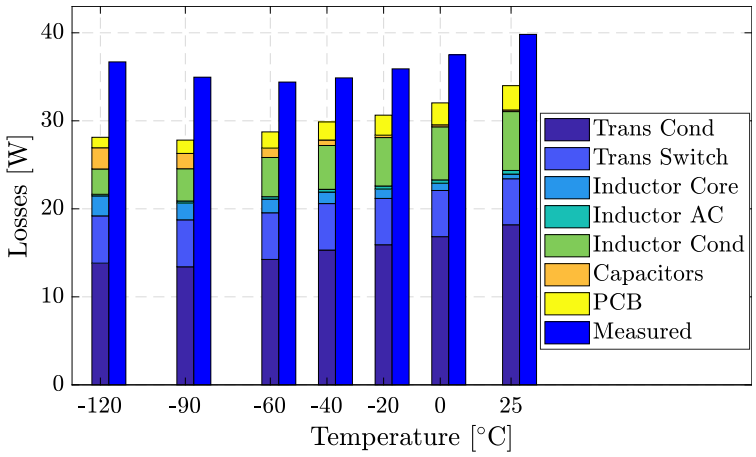


Figure 4.14: Measured power losses and estimated losses versus temperature at (23.5 A_{RMS} output). Although the losses are under estimated by the model, the trend is in agreement.

estimated based on scaling factors provided by the manufacturer [118].

Finally, the losses resulting from simple PCB conduction resistance (P_{PCB}) are estimated and scaled with temperature as,

$$P_{PCB} = R_{PCB}(T)\ I^2_{out,RMS}. \tag{4.18}$$

In this analysis, the total losses of the converter were calculated and averaged over a complete line cycle to determine the average loss. The bar graph in Fig. 4.14 shows a comparison between the measured loss at a load current of 23 A_{RMS} and 65 V_{RMS} and the calculated breakdown of loss. It can be seen that the overall losses initially decline with temperature and then stabilize. In particular, the conduction losses of the inductor and PCB decrease over the temperature range tested, and the inductor core loss as well as the capacitor losses increase. Additionally, the conduction losses of the GaN FETs fall and then stabilize. Cumulatively these trends lead to the hockey-stick trend in overall losses, although the exact replication of the trend would require additional knowledge of component properties and their internal operating temperature when the converter is operating.

Despite the smaller than expected gains in efficiency, the concept of combined cooling and fuel in LNG powered systems still has potential merit. Through proper design of the thermal management system, the operating temperature of the power electronics, and GaN devices in particular, can be optimized for maximum efficiency while still utilizing the waste heat from the power electronics to warm the LNG from storage temperature.

4.6 Increase in Power Conversion Density with LNG Cooling

Cryo-cooled power converters hold potential to operate at higher efficiency than standard, air-cooled designs. However, for the applications discussed in the introduction it is also critical that the complete system achieve high power density. The preliminary design in this work was constructed primarily to validate the operation of the flying capacitor converter at LNG temperatures, but values can be extrapolated to obtain an understanding of the power density benefits which may be obtained.

The converter specified power load is 22.2 A, at 45 V for a total power of 1 kW. The active overall volume of the converter has dimensions of approximately 65 mm X 85 mm X 10 mm for an overall power density of 18 W/cm^3. If the converter were designed to be air cooled, it would be operated at a significantly higher temperature than ambient. Assuming a modest 0.5% decrease in efficiency, a total of 43.7 W of loss would need to be removed from the system. Referencing the assumptions in Section 2.5.4, specifically a maximum device temperature of 100 °C, or 70°C above ambient and a heatsink admittance of 0.01 W/cm^{3}K, 1.428 mm^3 of heatsink volume are required per watt of loss. The converter would thus require a heatsink with a volume of around 62.4 cm^3. Combined with the converter itself this results in a power density of 8.5 W/cm^3.

Using cryogenic cooling, the converter efficiency is increased and only 32.9 W of waste heat must be removed from the system. The current, unoptimized cold plate can be redesigned to have the same footprint as the converter. Assuming a worst-case scenario in which the cold plate is milled using a similar strategy to the current version, the cold plate will add 45 cm^3 of volume to the converter allowing for a power density of 10 W/cm^3 or an increase of around 15% in power density over an air-cooled design. In larger systems an estimated increase of 50% to 75% in power conversion density has been estimated in [122]. Additionally this increase in power conversion density comes with the added benefit of an increase in the converter's efficiency.

It is important to note that the apparent power density benefits of LNG are complicated by system level considerations. Cryogenic cooling offers the opportunity to realize improvements in the efficiency and size of the power conversion electrical system, through the elimination of cooling radiators and other airflow channels which would otherwise be required. On the flip side, LNG has lower energy density than other hydrocarbon fuels and requires cryogenic storage with the accompanying fuel system insulation. Nevertheless, studies of hybrid urban air mobility aircraft have found that an LNG power diesel cycle competes favorably against advanced air-cooled diesel-powered hybrid vehicles, at the system level. By taking advantage of the low-temperature fuel to cool the power electronics and genset generator it was found

that maximum system range could be extended by 20% [123]. This improvement accounts for an estimated increase in the powertrain system volume of 10% which accompanied the required LNG support system, and comes with the added benefits of clean burning LNG fuel.

4.7 Conclusions

This work has demonstrated the feasibility of operating a GaN-based FCML inverter at the reduced temperatures accessible in an LNG powered hybrid system. Building on prior work characterizing EPC 2034 GaN FETS, the experimental evaluation of a 1 kW single-phase inverter was completed from ambient down to -140 °C and from light to rated load. A reduction in losses was demonstrated down to -60 °C, where a 16% reduction in losses compared to room temperature was observed. This trend reversed at lower temperature suggesting that the optimal performance for such hybrid systems will be achieved through the co-design of the electrical system and thermal impedances. Through proper design of the thermal management system, the optimal temperature for the power electronics can be obtained while maximizing the waste heat extracted for fuel vaporization. An estimated power loss breakdown was also performed to provide further understanding of the components of inverter loss and opportunities for improvement in future systems.

CHAPTER 5

DEVELOPMENT OF A MODULAR, SCALABLE, FCML-BASED HIERARCHICAL MOTOR DRIVE

5.1 Motivation and Background

Chapters 3 and 4 have demonstrated the design, operation, stability, and versatility of the FCML converter. This chapter will discuss the advantages of low-THD, FCML converters in high-power-density motor-drive systems, and demonstrate the implementation of an FCML-based motor drive tailored for aerospace applications. As will be explained, the efficiency and power density of many modern machine designs depend on the availability of a drive system which is not only high density, but capable of low THD as well. While 2-level inverters using a large filtering stage are capable of achieving both of these goals individually, low-THD requires that a 2-level design include a large filter stage which reduces the power density of the inverter. Due to the multilevel structure of the FCML inverter facilitated by high-density capacitor-based power transfer, the FCML inverter is capable of respectable performance in both metrics simultaneously.

As has been the case for single-phase FCML converters, much of the work in FCML-based drive systems has been focused on demonstrating fundamental operating principles of FCML operation rahter than the design's potential power density advantages. In [67], the authors experimentally demonstrate the use of a 3-level FCML with space vector modulation and voltage balancing as a wind turbine rectifier. The system control was implemented using a laboratory dSPACE module, and the authors note that delay in controller computation time had an impact on the capacitor voltage balancing of the system. This was corrected using a computational compensation. Additionally, the system was tailored for use at low fundamental line frequency between an induction machine and the grid. There has also been work focused on increasing the effective level count generated line-to-line by FCML converters in 3-phase applications. In [124], the authors experimentally demonstrate that two 3-level inverters operating off of two separate supply voltages in a 3:1 ratio can be used to produce 9 different voltage levels. The authors utilize space vector modulation (SVM) as an extension of the work done in [125]. Although the results are promising, the relatively

low switching frequency of 2 kHz reduces the power density benefits of the converter. Work has also been done to highlight the potential for improved performance through the use of FCML-based drive systems. In [126] the authors demonstrate that direct torque control (DTC) of an induction machine using an FCML results in more precise control of the motor field and speed, but the experimental results presented are limited.

Even in applications where power density is of reduced concern, FCML drive systems offer significant benefits in the operating efficiency of traditional induction machines. In [127] the authors experimentally demonstrate an 18% decrease in the total system losses (drive and motor) when transitioning from a 3-level FCML to 7-level FCML. Experimental losses are not presented for 2-level operation, but these would certainly further emphasize the benefits of the FCML topology in a wide range of motor drive applications.

Building on the concepts established in past work, this chapter seeks to more fully experimentally demonstrate the benefits of an FCML-based drive system using high-power-density, GaN-based FCML modules. In particular, this drive system is tailored for the needs of low inductance electric machines in aerospace applications. Recent work has shown that high-pole-count permanent magnet synchronous machines offer some of the highest power densities available with known machine architectures [16]. Additionally, as will be discussed, the high power density and efficiency of these machines are dependent on the availability of a low-THD drive. In addition to power density, this modular drive system also seeks to address the need for reliability required in aviation applications.

One of the challenges of aircraft design is the need for extensive certification on the reliability and manufacturing quality of all components. This process is costly and time consuming. One method of addressing this burden is through the development of an optimized, certified drive module that can be used in a parallelized, scalable drive architecture to address a wide range of application power levels. This is especially true in rising markets such as vertical take-off and landing aircraft for personal transport. In these instances, the availability of a certified module which can be used across a range of vehicle maximum takeoff weights will save development costs and offer consumers a broader vehicle selection with higher reliability and safety. To address this need, this drive system demonstrates a modular architecture in which the number of parallel FCML inverters can be scaled depending on the load requirements.

5.2 High-Density Electric Machines and Low-THD Motor Drives

In conjunction with high-density power converters, the density of the accompanying electric machine is crucial to the development of lightweight electric propulsion systems for electric and hybrid aircraft. One approach for increasing electric machine power density is to reduce magnetic flux projected per pole so that the flux density, and hence required magnetic material, is reduced in the rotor and stator [128]. With an understanding that the flux per pole (ϕ_p) is given according to the relationship

$$\phi_p = \frac{2}{P} L_{stack} D B_{peak,ag}, \tag{5.1}$$

where P, L_{stack}, D, and $B_{peak,ag}$ are the number of poles, stack length, air-gap diameter, and peak flux density in the air-gap [128, 129]. The decrease in flux per pole, and hence required flux carrying back iron, is directly proportional to the increase in pole count. Thus, increasing pole count decreases required magnetic material enabling lighter machine designs.

While reducing the flux per pole reduces required magnetic material, it also decreases the flux linkage per pole and hence the back-EMF generated by the machine (E_a). This can be seen in the relationship

$$E_a = K_\omega N_{ph} \omega_e \phi_p sin(\omega_e t) \tag{5.2}$$

where K_ω, N_{ph} and ω_e refer to the winding factor, number of turns per phase, and electrical frequency respectively [128, 129]. Thus, in order to maintain machine power while holding the winding factor and the number of turns constant, the electrical frequency of the machine must be raised to account for the increase in poles. However, provided the pole count and operating frequency can be raised, the path to higher power density is relatively direct.

One challenge arising from the increased pole count is the accompanying reduction in magnetizing inductance in the machine. This can be readily observed from first principles since the inductance (L) can be defined as

$$L = \frac{N\phi}{i} = \frac{N^2}{\mathcal{R}}, \tag{5.3}$$

where N is the number of times electric current i encircles the magnetic circuit with a reluctance $\mathcal{R}$. A machine with reduced back-iron will have a higher reluctance because of the reduced magnetic flux path through the machine, and as a consequence winding inductance will be proportionally reduced. This reduction in magnetizing inductance eliminates the filtering characteristics typical of more conventional machines. This is significant because this inductance is used in many drive systems to filter PWM drive voltage into sinusoidal

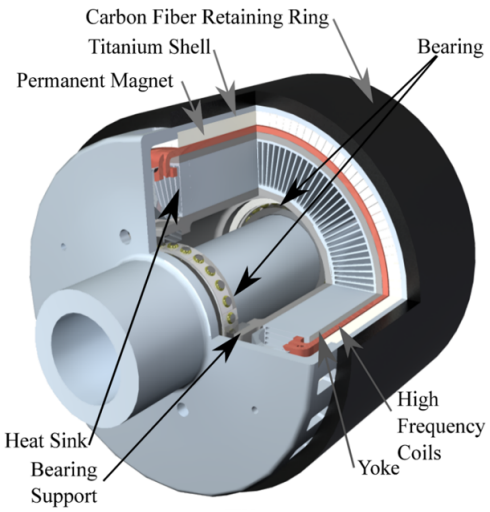


Figure 5.1: 1 MW permanent magnet, outer rotor motor developed at UIUC [128].

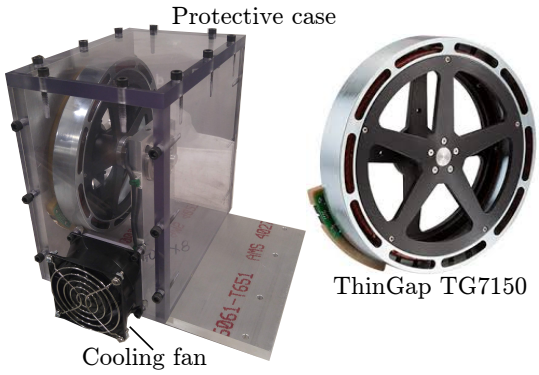


Figure 5.2: ThinGap 32-pole test machine mounted in enclosure [130].

current.

With the reduced filtering inductance available in high-density electric machines, the task of filtering the switched bus voltage into sinusoidal current falls on the inverter. This makes low drive THD combined with high drive power density a requirement for maintaining the power density and efficiency of the combined motor-drive system. For this reason, the FCML-based motor drive is a valuable tool in furthering the development of lightweight electric propulsion systems such as those needed for the realization of hybrid and electric aircraft.

One example of a high-density toothless motor design is shown in Fig. 5.1. This machine incorporates a permanent magnet and outer rotor architecture, and has a peak power rating of 1 MW at a fundamental frequency of 2.5 kHz [128, 131, 132]. Designed at the University of Illinois at Urbana-Champaign with funding from the NASA Advanced Air Transport Technology program, the machine has a target specific power density of 15 kW/kg and a low synchronous reactance of 0.06 per unit. In order to operate at designed efficiency, this machine requires the use of a low-THD sinusoidal drive making it an excellent candidate for an FCML-based drive system. This chapter discusses the design of a drive system which can be scaled to 200 kW for a system-level demonstration with the Illinois electric machine. In order to demonstrate the use of a scalable drive architecture the system is designed from 10-20 kW rated FCML modules which can be controlled to function as a single drive.

Due to the concurrent development of the 1 MW machine and this modular drive system at UIUC, the TG7150 slotless outer-rotor PM machine from ThinGap, shown in Fig. 5.2,

Table 5.1: Comparison of key specifications between ThinGap test machine and high-density research prototype.

Motor ID:	Illinois	TG7150
Pole Count	20	32
Rated Speed (RPM)	15,000	10,300
Rated Power (kW)	1,000	4
Fundamental Freq. (kHz)	2.5	2.7
Design specific power (kW/kg)	15	2.5
Sync. Reactance (pu)	0.06	0.06

was selected to serve as the initial low-power test platform for this drive. This outer rotor, 32 pole PM machine has a rated speed of 10,300 RPM yielding a peak fundamental frequency of 2.7 kHz making it an excellent representation of the 1 MW UIUC machine and of the trend in high-power-density machines toward minimal back iron, high pole count, and high fundamental frequency [16]. This wye-configured machine has a terminal inductance of 20.5 μH resulting in a per-unit reactance of 0.06 pu [130]. A comparison of the key specifications of the 1 MW UIUC machine and the ThinGap machine is shown in Table 5.1.

The following sections of this chapter will discuss the design and implementation of the modular drive system. Beginning in Section 5.3, motivation and design of the hierarchical structure of the drive system will be outlined along with the consensus-based control for even current sharing between the parallel modules in the drive system. With the system structure established, the implementation of field-oriented control based on direct rotor position measurement will be discussed in Section 5.4. This includes the scalable signaling distribution structure which allows the system to be reconfigured to meet required power demands. Section 5.5 discusses the hardware of the drive system beginning with the physical communication layer, followed by the development of the FCML-based interleaved inverter module (LIM) which forms the building block for the drive system, and then the three generations of drive hardware which have been used in development. Next, the drive operation results obtained are presented in Sections 5.6 and 5.7, followed by a review of accomplishments in Section 5.8 and a discussion of future work in Section 5.9.

5.3 Hierarchical Structure of Modular Drive System

The advantages of FCML power density and low THD are accompanied by some additional challenges in the area of control implementation. Because an N-level FCML requires N-1 switch pairs, the generation and distribution of a relatively large number of PWM signals

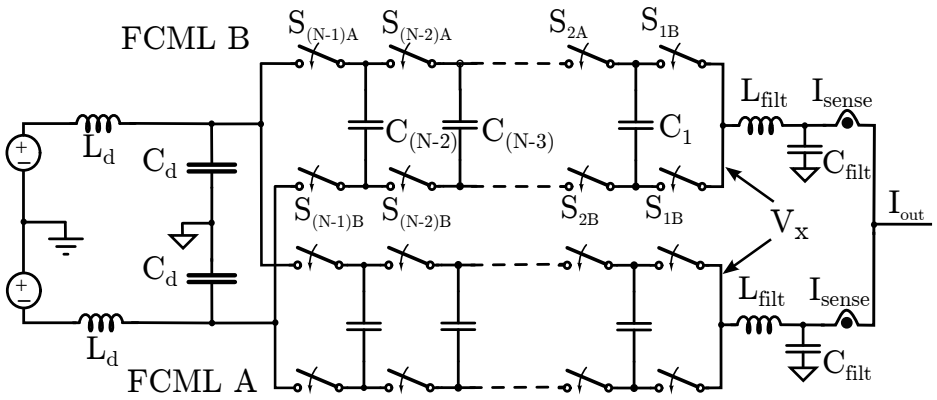


Figure 5.3: Schematic of power path for interleaved inverter module. Current sensing and PWM generation for each module are handled by slave FPGA controller located directly on the module.

must be addressed. As discussed in Section 3.3, the balancing of FCML flying capacitor voltage levels is highly dependent on precise PWM resolution. Mismatch in switch timing will result in capacitor voltage imbalance. Additionally, simply the number of PWM signals required raises challenges in routing and maintaining EMI immunity.

For these reasons, the single-phase FCML inverters discussed in this chapter as well as Chapters 3 and 4 have utilized a designated controller to generate the required PWM signals in close proximity to the inverter. While extending this strategy to a larger three-phase inverter system requires significantly more processing hardware than would be required for a single, centrally located controller, it improves scalability because the system is not constrained by the need to route $2 * (N - 1)$ individual PWM signals per FCML converter and is therefore capable of accommodating a larger number of parallel modules. Additionally, as will be shown, distributed control allows for the system to accommodate differences in inverter hardware while maintaining balanced current loading.

Figure 5.3 shows the power schematic for the single-phase modules used to implement this drive system [11, 12]. Each interleaved module (ILM) consists of two parallel FCMLs, which are phase shifted (at the switching frequency) to reduce filtering requirements at both the converter input and output. A slave controller located on each ILM generates $4(N - 1)$ PWM signals and coordinates the measurement of current from each FCML. Additionally, as will be discussed in Section 5.3.1, the slave controller is used to tune the duty ratio of each FCML inverter to ensure that the current loading on each FCML matches the reference from the master controller. Building on the ILM-level control, a master-level controller is then used to coordinate the operation of the individual inverters to form a complete motor drive. Figure 5.4 shows a high-level overview of the drive structure. The master controller,

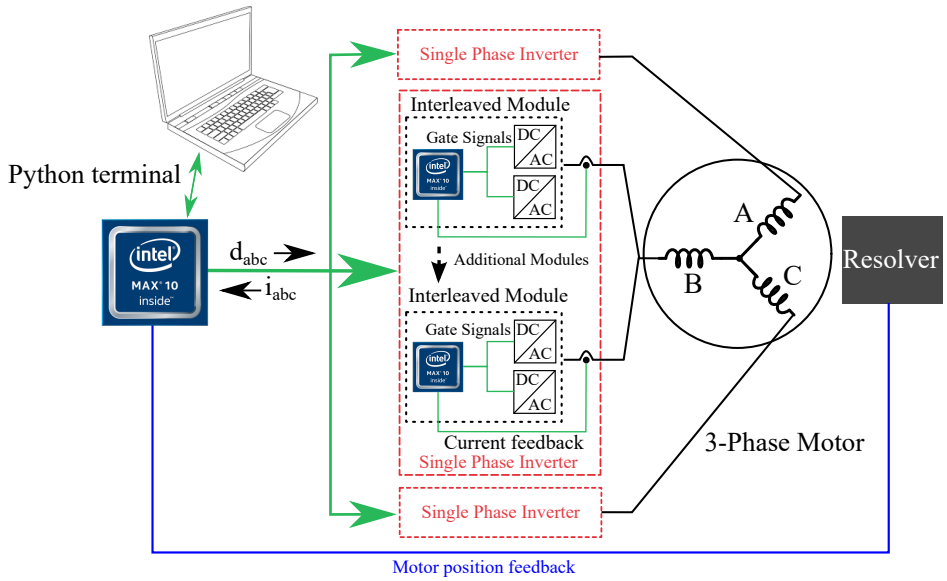


Figure 5.4: High-level hierarchical control structure for FCML-based motor drive system. Master controller sends reference duty ratio to slave controllers based on measured motor position and current feed-back from slaves.

implemented in an Intel MAX10 FPGA, communicates with a PC-based Python script to facilitate drive parameter tuning and the debug of drive data from the field-oriented control algorithm. As will be discussed in Section 5.4, the control of the drive system is coordinated based on a direct measurement of motor position fed into the master controller. The master controller also receives current feedback from each each FCML in the drive system and commands a common reference duty ratio to each of the three phases in the system.

This modular approach serves two purposes. First, it allows multiple applications with a range of power requirements to be addressed using a single inverter module, allowing the potential for economies of scale and simplified service. Second, the parallel interconnection of inverters provides for redundancy. In the event of a single module failure the remaining system can continue operation with a reduced peak power. This is of special importance in aviation applications.

5.3.1 Current Sharing Among Parallel FCML Inverters

The parallel connection of smaller modular inverters into a larger, scalable system requires the even distribution of current between modules. Ideally, equal duty ratio PWM would generate a matched load current through each of the converters. In practice, small differences in the signal path, switch devices, or passive components can result in uneven current

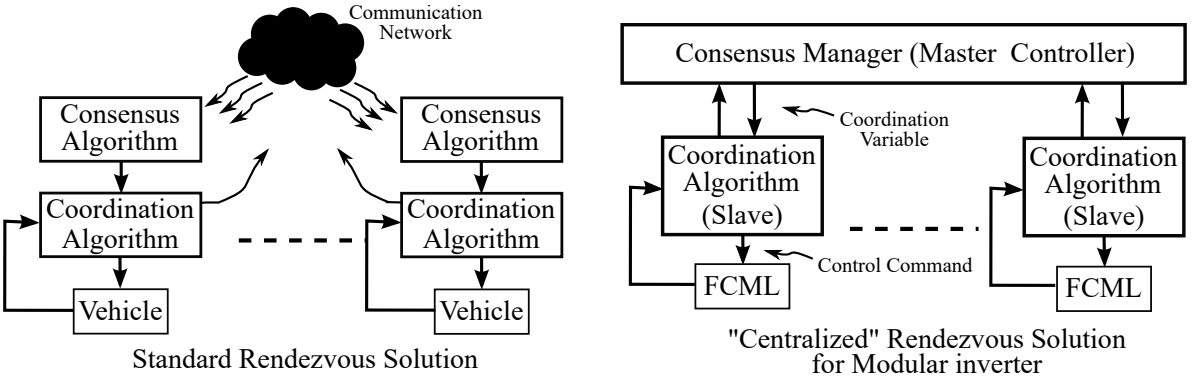


Figure 5.5: Master controller functions as the consensus manager in the rendezvous problem.

loading. Fundamentally, imbalance in current sharing typically stems from differences in the impedance of parallel converters [133]. In the case of the FCML converter, a low filter inductance and by extension low filter impedance makes impedance mismatch more likely.

In the case of inverters operating in parallel on a dc bus, a large impedance mismatch can lead to current flowing back into weaker inverters resulting in a circulating current. This is a well documented phenomena in literature, with the majority of the work addressing the parallel connection of 3-phase inverters tailored to low-frequency PFC or UPS type applications. In line-frequency systems, a derivative of droop control is often used to manage the real and reactive power as is done in utility applications [134]. Another approach is to sum the three-phase currents and use a PI control loop to adjust the PWM duty ratio in order to force the circulating currents to zero [135].

As discussed in [136] many of the strategies for ensuring even current sharing presented in literature center around the theme of using the overall average current in the system as a reference value. The duty ratio of each converter is then adjusted to match this average value. A direct application of this principle to the modular motor drive system would force each inverter to follow an instantaneously changing current reference, but this would eliminate the benefits of vector-based motor control in which the instantaneous drive voltage is directly determined by motor position without the use of any high-frequency feedback loops.

In this work, equal load current sharing between parallel ILMs is implemented based on a recognition that the impedance mismatches which lead to current sharing imbalances between FCML converters are relatively constant. Variations in flying capacitors, GaN switches, and inductors, as well as control tolerances and thermal imbalances from uneven cooling, are all steady-state with respect to the converter switching frequency and motor control bandwidth. As a result, current sharing compensation requires very low bandwidth.

The coordination of parallel ILMs to achieve even current sharing is a direct application of

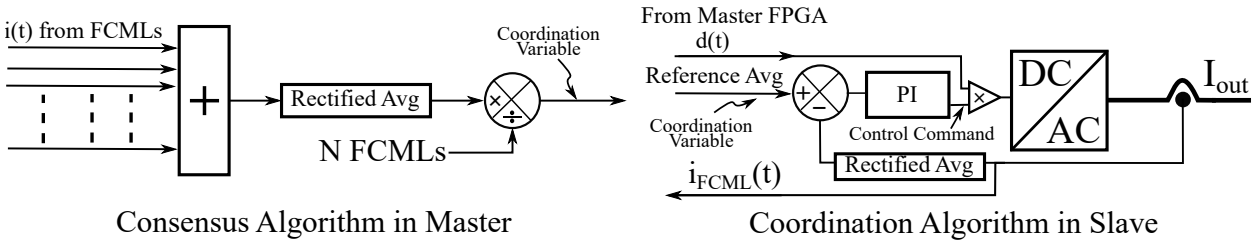


Figure 5.6: Consensus and coordination algorithm operating in master and slave.

the "rendezvous problem" from the field of consensus-based control. Consensus algorithms are a set of tools which can be used to enable a group of autonomous systems to settle on a common, mutually agreed upon, "coordination" variable even in the presence of non-uniform environmental disturbances [137]. In the case of the modular inverter system these disturbances may be imbalances in converter loading or cooling.

One form of solution to the rendezvous problem consists of a consensus algorithm in cascade with a coordination algorithm [138]. The consensus algorithm determines the "coordination variable" based on available communication with all autonomous systems. In most consensus-based control applications the consensus algorithm runs independently in each autonomous system using information obtained from independent communication received from as many other autonomous systems as possible to determine the coordination variable. After the consensus algorithm has established the current iteration of the coordination variable, the coordination algorithm operates to guide the autonomous system to meet the coordination variable. Figure 5.5 shows the standard rendezvous solution with a communication network supporting interaction between several separate autonomous systems.

In the case of the modular inverter, the hierarchical structure is dependent on a communication link between the slaves and a master controller. Unlike a group of autonomous systems, the position of the motor must be communicated to each inverter in order to enable its function. Although it is feasible to implement a completely distributed vector control algorithm using an observer to determine rotor position, such an undertaking was outside the scope of this work [139]. Therefore in this application the consensus algorithm is consolidated in the master controller as shown on the right side of Fig. 5.5.

Figure 5.6 shows the implementation of the consensus and coordination algorithm in the master controller and slave. The consensus algorithm performs the addition and averaging of the current readings from each FCML in a phase. This phase-wide average value is then divided by the number of FCMLs to calculate the average reference per FCML. This is the average value which all FCMLs should match when the system is balanced and is the

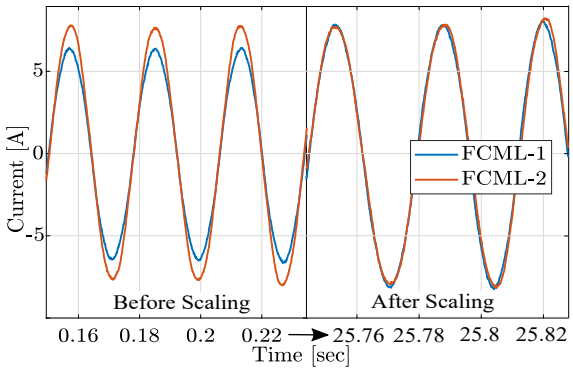


Figure 5.7: Measured FCML AC current before and after modulation depth scaling.

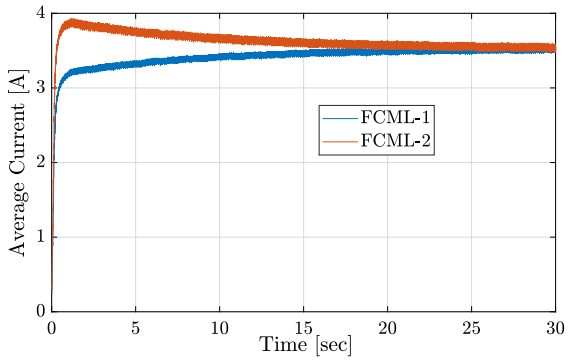


Figure 5.8: Measured 160 millisecond running average of rectified current measurement from FCML-1 and FCML-2.

coordination variable in control terminology.

After the coordination variable is sent to the slave controller, a PI controller is used to scale the $d(t)$ commanded by the vector control system to raise or lower the average FCML current as shown on the right side of Fig. 5.6. This scaling forces the rectified current measurement from each FCML to be equal to the phase-wide reference set by the master. Because the control is simply a scaling of the instantaneous commanded duty ratio, the only change in the dynamic control of the FCML is a small adjustment in response magnitude. Since the master controller operates all FCMLs in parallel as a unit this change does not impact performance.

Using this approach, impedance mismatches between parallel converters are compensated for without disturbing the stability and dynamic performance of the vector-based motor control algorithm. This technique is very similar to the approach used in [140] where the current flowing into parallel boost PFC rectifiers is averaged and used as a reference to match the instantaneous current load in each converter. The primary difference in the implementation in this work is that the current sharing is performed on a longer timescale than [140] and is less susceptible to distortion over the ac cycle.

Figure 5.7 shows the AC current waveforms of two FCMLs on an ILM at startup and after compensation. It can be seen that there is a measurable mismatch at startup. Although the system will operate under these conditions, unequal current sharing will result in some level of heating imbalance and a resulting reduction in peak system rating. It can be seen that after several seconds of applying current balancing, the amplitudes of the current waveforms leaving each FCML match closely. Figure 5.8 plots the average of the rectified current measurements from FCML-1 and FCML-2. The system initializes with a nearly 25% discrepancy in the individual rectified average current values. The current balancing controller can then

be seen to slowly bring the averages from both FCMLs into convergence. In order to prevent integrator windup, current sharing controllers running in the slave FPGA are only active when the average current in both ILMs is over 2 A.

5.4 Implementation of Field-Oriented Control

As mentioned, the drive system being developed in this work and the motor in Fig. 5.1 are intended for fixed-wing aviation propulsion applications. As such, the dynamic performance of the drive system is less important than the system scalability and redundancy. For this reason field-oriented control with smooth torque regulation was chosen as opposed to direct torque control (DTC) which could offer potentially higher control bandwidth.

In induction machines the rotor field always lags the stator field, and thus the motor can provide varying torque over a wide range of speeds using open loop control. This is not true of synchronous machines in which excess torque under open loop control will result in motor pullout and cogging. Some synchronous machines, such as the ThinGap machine in Fig. 5.2, achieve high specific power through high mechanical speed (10,000 RPM), as opposed to high torque, or more specifically high sheer stress through the air gap. In these cases the likelihood of pullout at startup is even higher than for other synchronous machines. In practice it was found difficult to start the ThinGap machine in an open-loop, volts per hertz configuration.

To address this issue, PM machines are most commonly driven using vector-oriented control in which the alignment between the stator and rotor field is enforced by direct measurement of the rotor position, or by means of a control observer. There is a wide body of literature on a range of position observer strategies for PM motors which avoid the need for a resolver or decoder measurement system. The focus of this work was on the coordination of a modular drive system, and therefore, spending extensive time on the position measurement strategy was undesirable. Thus a direct position measurement was made using a resolver.

5.4.1 Position Measurement

The resolver used for position measurement in this work is shown in Fig. 5.9. It was desired to use the same resolver for drive development as was required by the 1 MW UIUC machine in shown in Fig. 5.1. For this reason a resolver capable of operation up to 15 kRPM was needed for full speed demonstration. The RE-21-1-V02 brushless classical resolver which was selected has a rated speed of up to 20 kRPM, and is available from LTN Servotechnik

Figure 5.9: Magnetic resolver (RE-21-1-V02, LTN Servotechnik GmbH) used for position measurement in drive system.

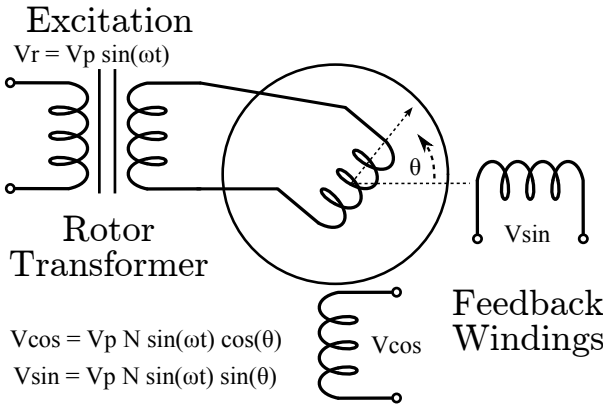


Figure 5.10: Functional schematic of brushless classical resolver.

GmbH.

A resolver is a rotating transformer used to modulate a sinusoidal excitation signal by the sine and cosine of the motor shaft angular position. The resolver excitation,

$$V_r = V_p \times sin(\omega t), \tag{5.4}$$

is sent to the resolver from the resolver to digital converter (RDC). The classical brushless design used in this work magnetically couples the excitation signal from the stator to the rotor. The field from the rotor is then picked up by sine and cosine feedback windings which are mechanically shifted by 90° with respect to each other as shown in Fig. 5.10. This process results in feedback signals,

$$V_{cos} = V_p N sin(\omega t) \times cos(\theta), \tag{5.5}$$

and

$$V_{sin} = V_p N sin(\omega t) \times sin(\theta), \tag{5.6}$$

where θ is the shaft angular position, N is the turns ratio between the excitation and pickup windings, and V_p is the amplitude of the excitation signal. Figure 5.11 shows the measured resolver signals as the motor is spinning. The envelope of the excitation signal is at the top of the image and the envelope of the modulated sine and cosine feedback signals at the bottom. The AD2S1205 resolver decoder (RDC) receives the modulated sine and cosine signals and then through subtraction and demodulation forms a reference signal which tracks the rotor position [141].

The initial alignment of the resolver rotor on the motor shaft is arbitrary and depends

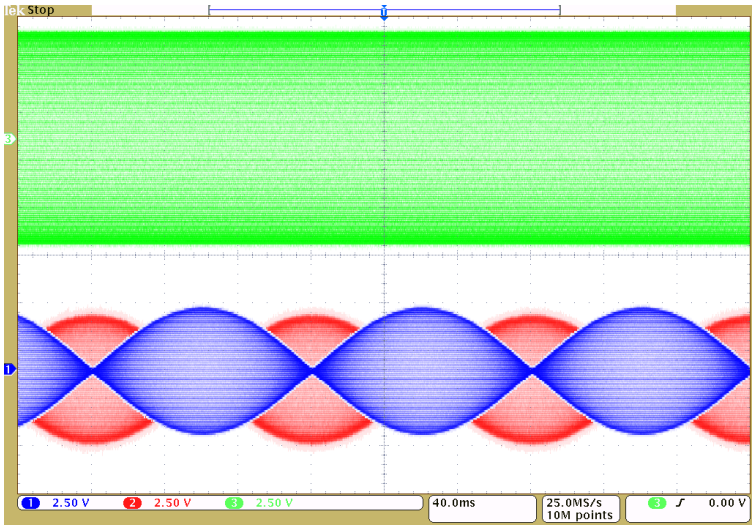


Figure 5.11: Resolver excitation signal (top), sine and cosine feedback signals as motor shaft rotates (bottom).

on the assembly of the resolver. After assembly of the motor and resolver and after any change to the resolver or resolver decoder, it is critical to check the alignment between the rotor d-axis and the resolver zero position as seen by the drive. Because both the ThinGap machine and the 1 MW machine in Fig. 5.1 are slotless designs with negligible reluctance torque, the maximum torque is obtained when the stator field peaks on the rotor q-axis and 90° from the rotor d-axis. The "zero" position of the rotor can be found by aligning the rotor magnetic axis with the phase A magnetic axis. Because the neutral connection in this machine is not accessible, this was accomplished by connecting phase B and C in parallel to ground and applying positive dc current to the A phase winding. Assuming balanced phase resistance for B and C windings, this will pull the rotor d-axis into alignment with the stator phase A winding thus positioning the stator in the "zero" position as required for proper function of the $dq0$ transformation in vector control. The position reading given by the resolver decoder at this location is then subtracted off to generate the rotor position used in vector control.

The measurement of rotor position with the zero offset subtracted becomes the reference angle θ_m used in the $dq0$ transformation between the dq and ABC winding quantities. The angles $\theta_m - \frac{2\pi}{3}$ and $\theta_m - \frac{4\pi}{3}$ are generated by subtracting $\frac{1}{3}$ of the full resolver reading of $2^{12}-1$ with rounding as required. The VHDL coding in the FPGA was checked by comparing the controller-calculated ABC winding voltages to the results of the same calculations in MATLAB as shown in Fig. 5.12. This was helpful to ensure that all bit manipulations were conducted correctly and that the controller-calculated values were not shifted by a power

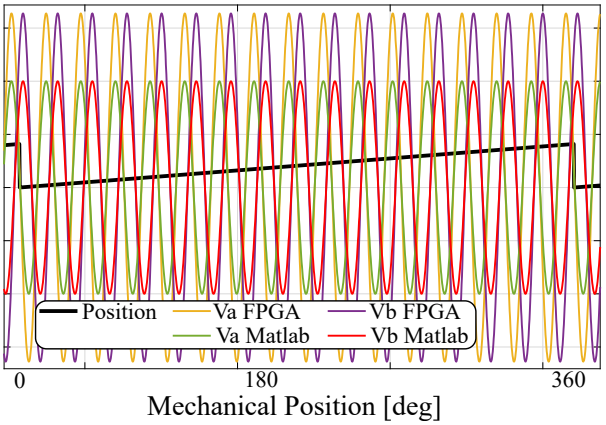


Figure 5.12: Numerical comparison of FPGA and MATLAB calculated dq to ABC transformation.

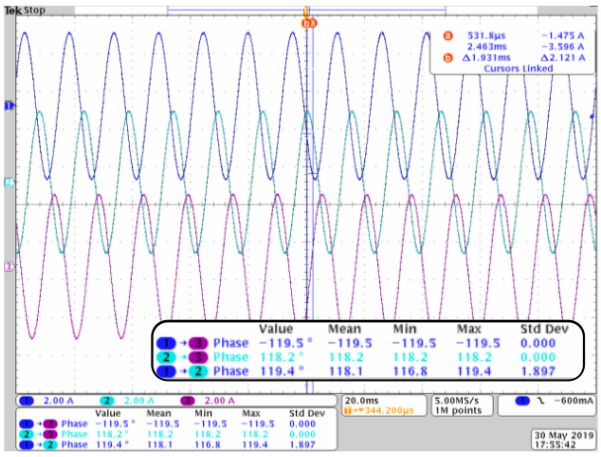


Figure 5.13: Check of phase shift between ABC winding voltages.

of two. After performing all required calibrations, the resulting measured phase shift is shown in Fig. 5.13. Additional details on the implementation of vector control, including the transformation from mechanical to electrical angle, are discussed in Section 5.4.2.

After the initial zero point of the machine, and required phase shifts are set, the alignment between the measured motor position and rotor can be checked by comparing the phase of the motor back-EMF to the applied voltage of the drive. Instead of connecting the motor terminals to the drive system, the motor and drive are both connected to separate, high-resistance, three-phase loads so that negligible current flows through the windings and the motor terminal voltage is in phase with the motor back-EMF. In addition to the minimal current flow, the phase shift due to winding inductance in this application will be small because the inductance of the ThinGap motor windings are small. The motor is then rotated by a prime mover and both the motor back-EMF voltage and the applied drive voltage plotted on the scope. Because the back-EMF of the motor is the derivative of flux linkage, when the rotor flux, or d-axis, aligns with the stator d-axis the motor back-EMF will appear on the stator q-axis. By applying a fixed q-axis voltage in the drive, and comparing the back-EMF of the motor as it is spun by a prime mover to the ac waveform generated by the drive, the alignment between the measured and actual rotor position can be verified. As mentioned, this process must be repeated any time there is disruption to the resolver or resolver decoder. The final check of alignment is shown in Fig. 5.14.

The accuracy of the rotor position measurement must be high enough to ensure efficient operation of the electric machine. The RE-21-1-V02 device has a stated accuracy of $\pm 3'$, or $\pm 0.05°$, while the decoder has an accuracy of $\pm 11'$ or $\pm 0.18°$. Assuming a worse-case

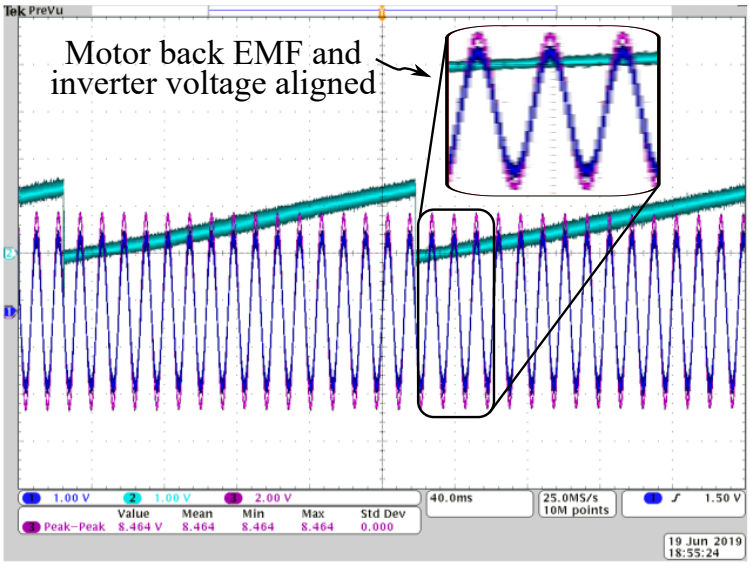


Figure 5.14: Validation of alignment between drive position reading and motor magnetic position.

combination of the position measurement, this results in an uncertainty of, $\pm 0.23°$ mechanical degrees. When this resolver is used in conjunction with the 32 pole ThinGap machine during drive development, this is equal to an electrical accuracy of

$$\pm 0.23° \times \frac{\text{poles}}{2} = \pm 0.23° \times 16 = 3.68°. \tag{5.7}$$

For a synchronous machine, a misalignment of the applied stator field from the q-axis will result in a reduction in torque from the nominal value, and hence a loss in mechanical power. The relative loss in motor efficiency can then be calculated as

$$1 - \cos(3.68°) = 0.2\%. \tag{5.8}$$

This loss calculated based on the published hardware resolution is marginal and was deemed acceptable. However in the process of system development it was discovered that the resolver position measurement can be easily distorted by non-idealities in the sine and cosine signals fed back from the resolver.

The AD2S1205 RDC calculates the resolver position based on the sine and cosine feedback signals received from the resolver. For this reason, the position accuracy is sensitive to a mismatch in the peak amplitudes of the sine and cosine signals. Differences in signal amplitude stemming from small differences in the resolver hardware or connection will result in an error in position measurement that oscillates at twice the rate of rotation. A similar

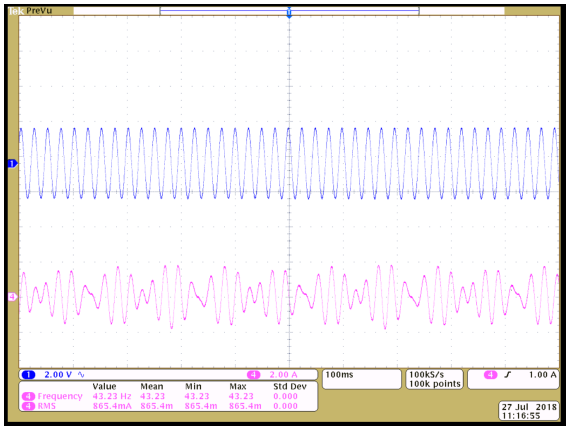


Figure 5.15: Motor current even sinusoidal voltage and oscillation in current amplitude resulting from oscillating phase shift.

error will be induced by differences in the DC bias of the sine and cosine signals [141, 142]. This oscillating error in rotor position measurement results in a cyclic shifting of the angle between the rotor and stator magnetic fields. The resulting fluctuation in motor back-EMF in turn causes oscillation in the amplitude of motor phase current and torque. Figure 5.15 shows an example of this current amplitude oscillation.

In order to understand the source of this error more accurately and evaluate potential solutions, the resolver measured position needed to be compared to the actual rotor position. This is accomplished by comparing the rotor back-EMF and inverter applied voltage using the same process as outlined previously for checking the alignment of the rotor measured and magnetic position. The motor back-EMF and drive applied voltage, which are independent due to the fact the motor is disconnected from the drive power, should remain perfectly synchronized. However, the measurements in Fig. 5.16 show that the inverter waveform period has a cyclic variation in phase twice per rotation. This variation in the phase of the two signals was quantified more precisely by comparing the period of the motor back-EMF and inverter voltage over a rotation of the machine.

To address these challenges, a reference circuit from [142] was modified with a loading potentiometer and a common mode bias reference as shown in Fig. 5.17. The 294 Ω resistance in series with the resolver terminals allowed the potentiometer loading to create a voltage drop at the decoder input without drawing significant current from the resolver windings. This was important to prevent saturation of the resolver or phase shift due to resolver impedance. Before adjustment the sine and cosine signals as shown in Fig. 5.11 exhibited differences in amplitude on the order of tens of millivolts. This mismatch was compensated for by adjustment of the potentiometers.

Based on the period of the motor back-EMF and inverter applied voltage, it is possible

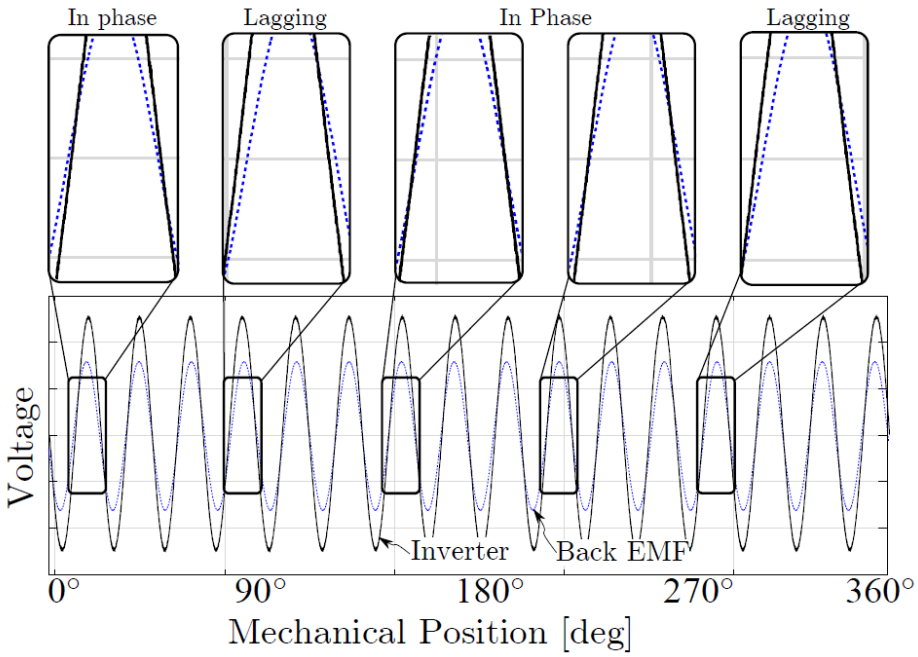


Figure 5.16: Single-phase comparison of inverter voltage and open winding motor back-EMF. Inverter applied voltage lags motor back-EMF twice per mechanical rotation.

to interpolate the error between the measured and actual rotor position in terms of counts in the 12-bit resolver reading. Figure 5.18 shows the position measurement error before and after the addition of the tuning load. It can be seen that adjusting the amplitude of the resolver feedback signals largely eliminates the resolver measurement error at low rotation speed.

In addition to the RDC's sensitivity to errors in signal amplitude, the circuit is also susceptible to measurement error during high-speed rotation. Due to impedance in the resolver windings, there is a slight phase shift between the resolver excitation signal and the sine and cosine signals fed back to the decoder. The voltage induced on the sine and cosine windings at higher rotation speed tends to accentuate this error. The cumulative error can be approximated as

$$Error = PhaseShift \times \frac{RotationRate}{ReferenceFrequency}. \tag{5.9}$$

The RE-21-1-V02 device has a synthetic reference generation circuit that is designed to minimize the impact of this error, and the reference frequency was set to the resolver maximum rated frequency of 10 kHz [141, 142].

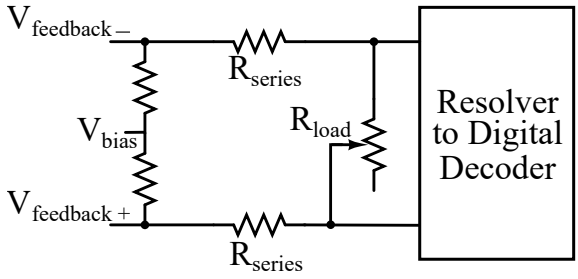


Figure 5.17: Resolver loading circuit used to match feedback amplitude. A separate circuit is used to adjust the amplitude of each resolver signal.

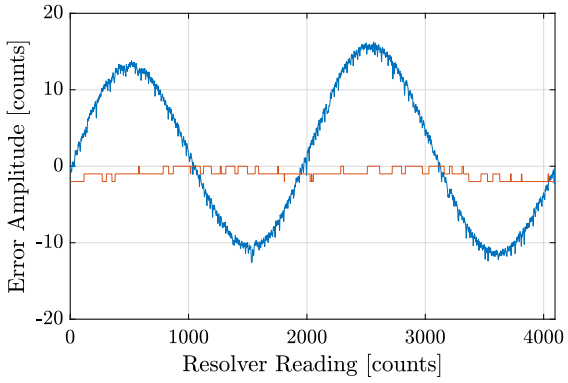


Figure 5.18: Error in position measurement before and after implementation the tuning circuit in Fig. 5.17.

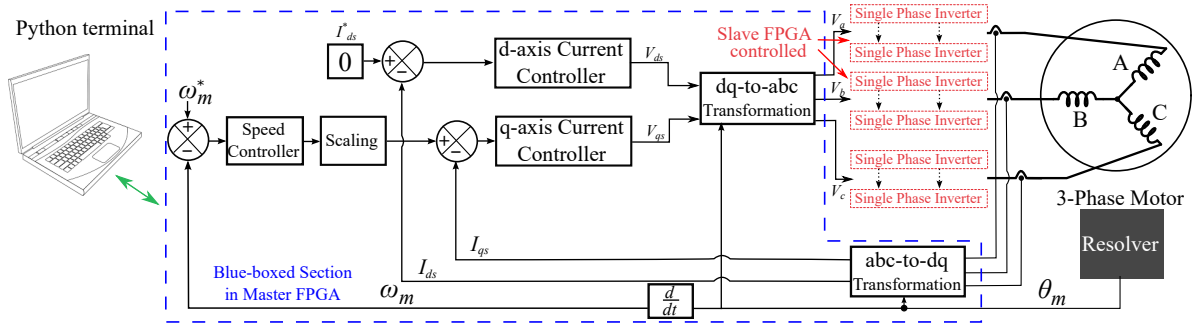


Figure 5.19: Control structure for FCML-based motor drive. Drive-level control is accomplished in the master controller while PWM generation and current balancing is handled in the slave controller.

5.4.2 FOC Implementation and Distribution

Based on the measured rotor position, vector-oriented control was implemented above the physical layer of modular hardware [143]. Figure 5.19 shows an overview of the relationship between the master controller and single-phase inverters used to drive the three-phase motor. Each phase of the modular inverter is composed of multiple ILMs operating in parallel to meet the per-phase power requirements. As explained, each ILM is composed of two FCMLs which are controlled by the local slave converter.

Figure 5.20 illustrates the signal distribution module coded in VHDL to receive and distribute data to and from each of the ILMs. The master controller and communication hardware, which will be discussed in Section 5.5.1, provide mapping for 15 channels. With each iteration of the control algorithm, data must be sent to and read from each of the active channels. If the number of parallel modules is changed, the data interface in the FPGA must

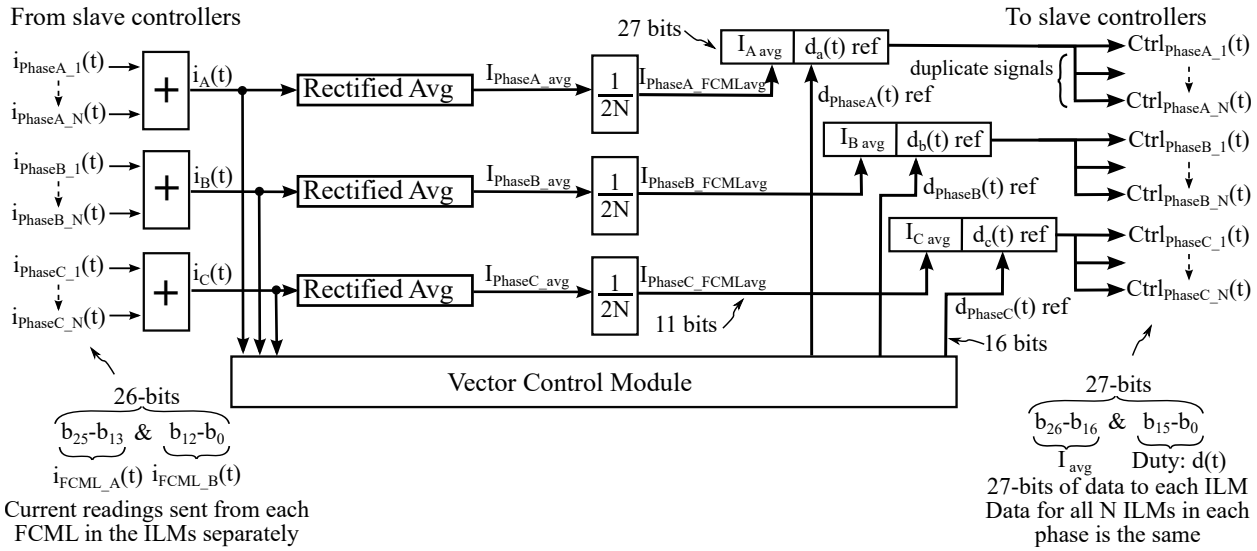


Figure 5.20: The signal distribution module used to facilitate communication and even current sharing between all ILMs.

be modified. The control mapping VHDL module accepts the number of parallel modules to be used per phase, as well as the starting position of each phase before compilation. Based on these inputs, the summation of currents from the ILMs as well as the transmission of the current reference signal and phase duty ratio are configured.

For intermediate debugging purposes, the current from each FCML in the ILM is returned to the master controller separately as a signed 13 bit value. The current readings from both FCMLs in the ILM are appended together to form a 26 bit value which is transmitted using asynchronous serial communication. The data enters the system on the left side of Fig. 5.20. Once the data arrives in the master controller, the current readings from each phase are added together to generate the 3-phase currents $(i_{\mathrm{A}}(t), i_{\mathrm{B}}(t), i_{\mathrm{C}}(t))$. The current in phase X (X incrementing from A to C) is the sum of the current coming from ILM 1 through N in the phase ($i_{\mathrm{PhaseX1}}(t)$ through $i_{\mathrm{PhaseXN}}(t)$). The current reading from each ILM is comprised of current readings from each FCML in the ILM ($i_{\mathrm{FCML\_A}}(t)$ and $i_{\mathrm{FCML\_B}}(t)$). The total phase currents $i_{\mathrm{A}}(t), i_{\mathrm{B}}(t), i_{\mathrm{C}}(t)$ are then passed into the vector control module. In return, the vector control module supplies the 16-bit reference duty ratios, $d_{\mathrm{PhaseA}}(t), d_{\mathrm{PhaseB}}(t)$ and $d_{\mathrm{PhaseC}}(t)$, which represent the ABC winding voltages required to drive the motor.

In order to ensure even current sharing between between all FCMLs, the compensation technique discussed in Section 5.3.1 is spread across the modular inverter system. As shown in Fig. 5.20, the total phase currents $i_{\mathrm{A}}(t), i_{\mathrm{B}}(t)$, and $i_{\mathrm{C}}(t)$ are used to calculate the rectified average for the complete inverter system. This value is then divided by the number of ILMs in the phase to determine the average ILM current for the phase, and later by two to set

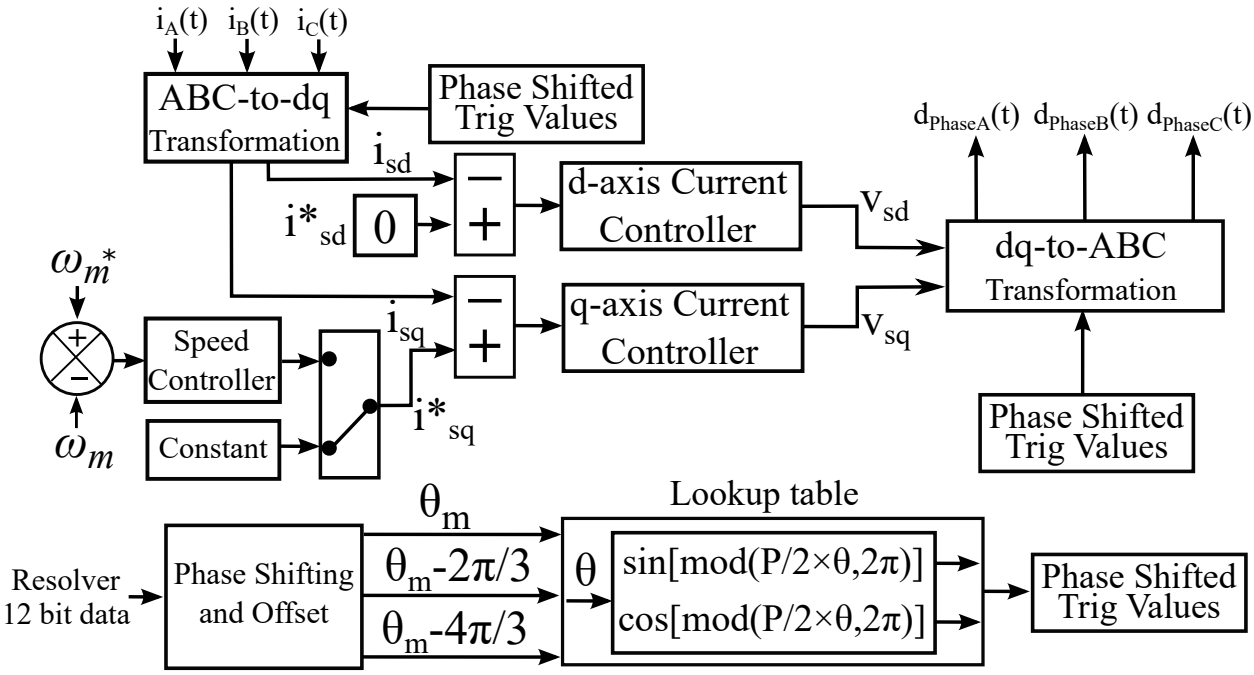


Figure 5.21: Vector control module used to generate phase voltages.

the reference current which each FCML will use as its average current setpoint as discussed in Section 5.3.1. Thus, even current sharing is ensured throughout the system. The final step in the control process is the appending of the ILM reference current with the duty ratio reference for transmission to the ILM. These 27 bits of data are then sent to the slave using asynchronous serial.

Figure 5.21 shows the vector control module which receives the 3-phase current readings from the signal distribution module and generates the required 3-phase reference duty ratios. The generation of sine and cosine values required for transformation from dq to ABC winding quantities is accomplished using the signal path shown in the lower half of Fig. 5.21. After the offset and phase shifts are subtracted from the resolver data, the sine and cosine of each values are calculated. Two approaches were tested to perform this functionality. The first was to directly multiply the resolver position by the number of pole pairs and then perform the trigonometric calculations using a CORDIC algorithm provided in the standard library of the FPGA development kit. The second was to use the resolver reading to reference the corresponding sine and cosine values in a precomputed table which accounted for the number of pole pairs. Both of these approaches were implemented, but the use of the CORDIC required additional bit manipulation in VHDL in order to perform both the multiplication by the number of pole pairs and trigonometric calculation while maintaining floating point accuracy. The lookup table approach off-loaded the needed floating point calculations and

facilitated a more direct implementation and was used in the results presented

Having calculated the required trigonometric quantities, the required vector multiplications are performed to convert the ABC winding currents into their dq representation. This allows the use of basic PI control to regulate the field current (i_{sd}), and the torque producing current (i_{sq}) of the machine [143]. In the case of a PM machine, the magnetic field is provided by permanent magnets and field current is generally not applied except in the instance of field weakening in order to reduce machine back-EMF and required DC bus voltage for high-speed operation at reduced torque. In this instance the field current was set to zero because rated torque at full speed operation was desired and adequate dc bus voltage was expected to be available.

In many motor drive applications such as electric vehicles, torque is the preferred control variable. In applications where speed control is appropriate, a torque-producing current reference (i^*_{sq}) is generated based on the error between the commanded motor speed (ω^*_{m}) and the measured motor mechanical speed (ω_{m}). In the results presented in Section 5.7 a constant i_{sq} current reference was applied. Both i_{sq} and i_{sd} are regulated by PI controllers which set the corresponding v_{sd} and v_{sq} to be generated by the drive. In order to produce the duty ratio reference for each phase of the drive, the v_{sd} and v_{sq} winding voltages are transformed into the ABC winding voltages or, more precisely, the ABC duty ratios based on motor electrical position.

The use of field-oriented control allows the control of motor torque and field to be accomplished using standard PI control as the three-phase currents are transformed into a dc dq representation. Thus the tuning and update rate of v_{sq} and v_{sd} is a function of the system requirements for torque response, and is independent of the motor rotation speed. In the results presented, the i_{sd} and i_{sq} controllers were updated at a rate of 3.1 kHz which is adjustable as needed.

5.4.3 Impact of System Sampling Frequency and Delay

Unlike the calculation of dq voltage, the dq to ABC transformation is updated in synchronization with the motor position in order to generate the sinusoidal voltages required to drive the motor. Thus, the instantaneous phase duty ratio of the inverter system is a function of the motor position. Distortion, or delay in the phase of the applied voltage, will degrade the performance of the motor because the field applied by the stator will be shifted from the rotor q-axis much as described by (5.8). At low motor rotation speed the impact of delay between the motor position measurement and the update in voltage applied to the motor is

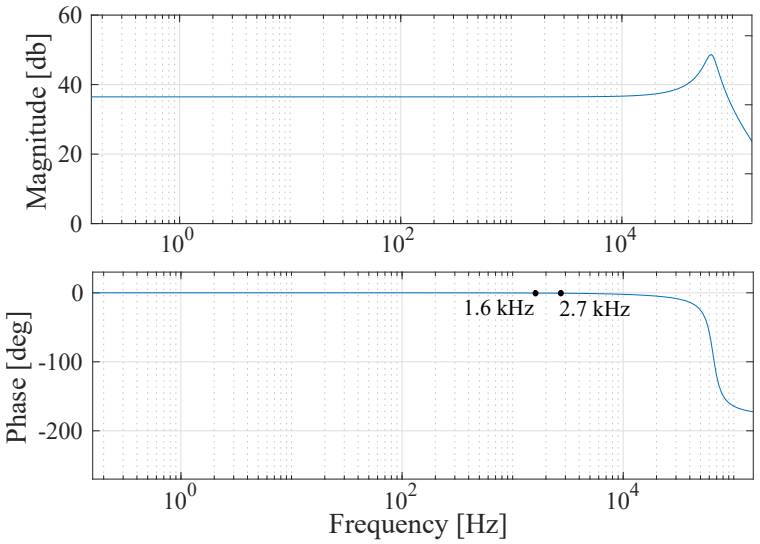


Figure 5.22: Amplitude and frequency response for buck converter/FCML with 10 μH, 0.6 μF filter stage.

negligible. This is because the delay incurred as a result of communication, duty ratio calculation, and inverter filtering, is an insignificant percentage of the slow fundamental period. As the motor rotation speed increases and fundamental period becomes shorter, the delay between the motor position measurement and update in the inverter applied voltage can become a significant percentage of the fundamental period resulting in phase delay between the motor position and applied voltage.

The FCML converter functions as a multilevel buck converter in a motor drive application. As has been discussed in Section 3.2.4, the multilevel structure allows for a significant reduction in the required filtering without increasing the THD of the load voltage. Because the FCMl is functioning as a multilevel buck, its small signal response is still dominated by the output LC filter. In addition to power density, an added benefit of the reduced filtering is the high control bandwidth of the FCML converter. Provided the FCML capacitor voltage ripple is small, the FCML frequency response can be approximated at that of a 2-level buck with equal filter sizing [144]. Neglecting parasitic components, the small-signal model of the control to output voltage frequency response, $G_{vd}(s)$, for the buck converter can be written as

$$G_{vd}(s) = D\frac{R_{\text{load}}}{R_{\text{load}} + sL + s^2LCR_{\text{load}}}. \tag{5.10}$$

The hardware used in the development of the modular motor drive (discussed in Section 5.5.2) incorporates 10 μH inductance and 0.6 μF of capacitance in the output filter. Because of these low filter values, the bandwidth of the ideal converter far exceeds the 2.7 kHz requirements as shown in the frequency response plot of Fig. 5.22. The details of PWM

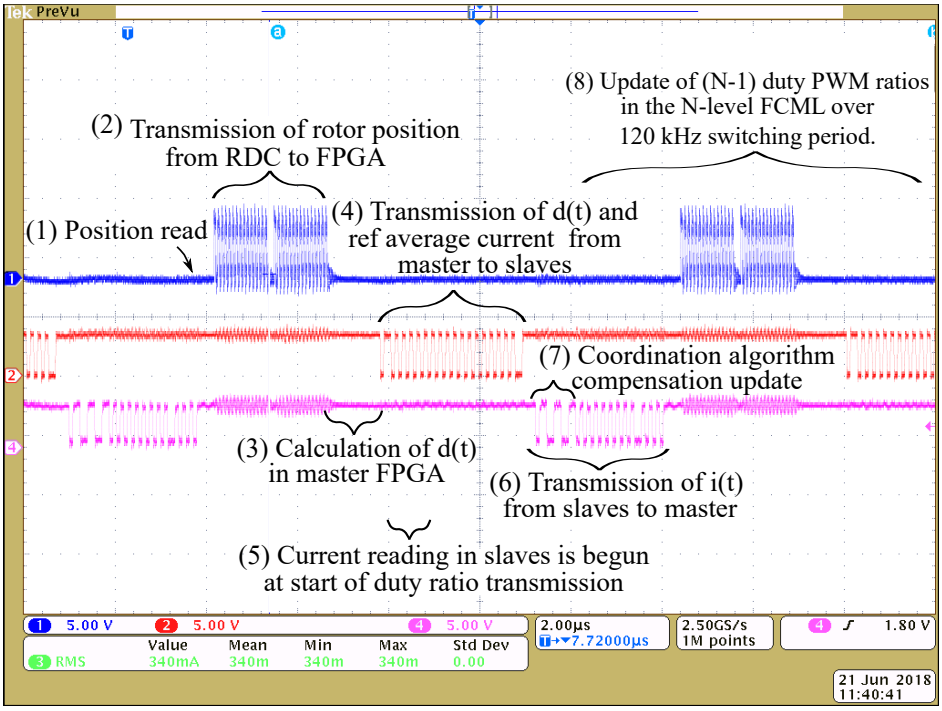


Figure 5.23: Duty ratio update sequence shown in the context of communication between the resolver decoder, master controller, and slave.

modulation reduce the high-frequency performance of the system [145], however the FCML converters used in this work are optimized for a switching frequency of 100-120 kHz which is sufficient for the fundamental frequency required. In contrast, the inverter duty ratio is a function of the rotor position, and delay between motor measurement and PWM adjustment plays a key role in determining the phase delay in the system.

For the results which will be presented in Section 5.7, the measurement of the rotor position and communication of updated duty ratios to the slave modules occurs at an update frequency of 100 kHz. Figure 5.23 shows a scope shot of the communication signals between the resolver decoder, master controller, and slave controller. The communication channel with each slave controller is managed by a separate serial module. Thus, the sequence in Fig. 5.23 occurs simultaneously as each slave exchanges communication with the master FPGA. The data lengths in this example are from an earlier version of the hardware and are shorter than those described in Fig. 5.20. When the required data lengths were extended in order to incorporate current sharing, the communication clock speed was increased to maintain the same 100 kHz update rate.

As designed, the duty ratio update cycle begins at point (1) with the reading of the motor position and speed by the resolver decoder. During interval (2), the motor position and speed are serially transmitted from the resolver decoder to the master controller. The 12

bits corresponding to both measurements are visible in Fig. 5.23 over the interval. Next, the vector control logic in Fig. 5.21 is executed over interval (3) with the phase shifted sine and cosine values being calculated every iteration along with the dq-to-ABC transformation. At the desired interval, the update of the i_{sd} and i_{sq} controllers is executed immediately following interval (3). The updated v_{sd} and v_{sq} values are available for the following communication cycle. This is done to minimize overall update time and because the steady-state dq winding quantities will not be impacted by a 10 μs delay.

After calculations are complete in the master controller, the updated $d(t)$ is sent to the slaves via asynchronous serial during interval (4). The start of this data transmission also triggers the reading of the phase current on each FCML during interval (5). This optimizes the overall update rate by allowing both the reading from the current sensor and the duty ratio to be clocked into the slave simultaneously. Shortly after completion of the duty ratio transmission, the transmission of the current reading back to be master is begun (6) as well as the calculation of the actual FCML duty ratio based on the $d(t)$ reference sent from the master controller and the control command for compensating the average current value as shown in (Fig. 5.6). After these computations are complete, the updated duty ratio is loaded into the PSPWM module which runs asynchronously from the communication interface. This allows the PWM frequency to be changed independently, depending on the hardware being operated, without impacting the communication. The duty ratio of each of the $N-1$ phase-shifted counters in the PWM module is updated individually at the counter reset and thus the PWM duty ratio is updated consecutively over an entire FCML switching cycle.

The communication sequence of Fig. 5.23, introduces a delay of $\approx$ 16 μs between the measurement of rotor position and the update in the final PWM modulator duty ratio in the FCML phase-shifted PWM module. This corresponds to a delay of 15° at the 2.7 kHz rated frequency of the ThinGap motor. Because this delay is known, it can be compensated for in control by extrapolating the measured motor position forward based on the time delay between the measurement and when the updated voltage will be applied to the stator [146]. During review of the data presented in Section 5.7 and VHDL code used in control it was discovered that an additional $\approx$ 7 μs was inadvertently added to the measurement delay bringing the overall delay to $\approx$ 23 μs. Instead of the position measurement being taken at time (1) as indicated, it was taken immediately after the transmission of the previous value during time interval (3) and transmitted during the following cycle. This was the result of a timing selection made inside the resolver decoder HDL driver early in the design process. This issue is easily remedied by a bit shift in the code, but the error was present during testing and its impact will be discussed in Section 5.7.

5.5 Development of Drive Hardware

5.5.1 Physical Communication Layer

Communication between the master controller and slave modules is a key aspect of the operation of this modular drive system. Digital logic transfer, whether PWM or data, is challenging in any power converter application due to the rapidly changing electric and magnetic fields created by high voltages and switching currents. This challenge is amplified by the use of fast-switching wide-bandgap devices for two reasons. First, rapidly changing current and magnetic flux due to fast switching induces higher voltage potential on adjacent signal lines than would occur for a lower switching speed. Second, due to the low parasitic capacitance and fast response of wide bandgap devices, instantaneous voltage spikes on the signal lines can result in a full switch transition whereas a slower switching device would filter the signal. In addition to following recommended practice for signal routing and maintaining a low-impedance ground return path, proper signaling hardware and filtering have proven essential to ensure robust data transfer.

The quest for energy efficiency has led to the development of many power conserving communication ICs which have high internal driving impedance. Pull-up and pull-down impedance of 5-9 kΩ are common in these devices. While this design may operate satisfactorily in a purely digital environment, the high driving impedance which enables low power consumption can allow the signal trace voltage to bounce in the presence of rapidly changing magnetic fields produced elsewhere in the converter. For this reason, it is important to select devices with adequate signal driving strength. The Intel MAX10 FPGA family offers an IO driving strength of 8 mA in the 3.3 V LVTTL protocol corresponding to a 412 Ω drive impedance [147]. This signal strength has proven to be a satisfactory building block in a robust converter control system.

In addition to robust signal driving strength, the use of low-pass filters on all logic inputs has proven essential to preventing erroneous logic fluctuations. These filters must be applied not only to PWM inputs, but also to any single-ended communication signals such as data lines from ADCs and current sensors. For 120 kHz PWM signals, a low-pass cut-off frequency in the neighborhood of 15 MHz has proven satisfactory (R = 229 Ω, C = 47 pF). For maximum reliability, signals should be filtered with as low a cutoff frequency as feasible while maintaining bandwidth required by the application. Figure 5.24 shows the filtered clock and chip-select signal entering one of the two current sensor ADCs on the ILM used in this work. The impact of filtering is clearly evident in the rounded edges of the signals, but all timing constraints are met with sufficient margin.

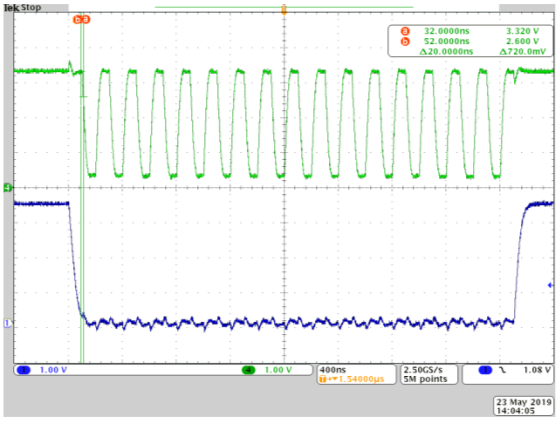


Figure 5.24: Filtered clock and chip-select single-ended signals and the input of the current sense ADC on the 10-level ILM.

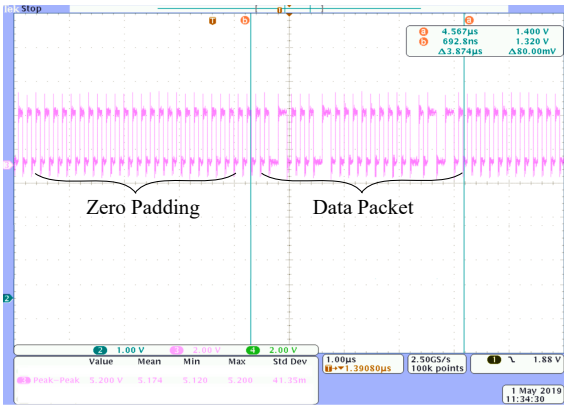


Figure 5.25: Manchester asynchronous serial with zero padding transmitted via optical link.

In addition to single-ended on-pcb communication, this drive system also requires extensive communication between the master controller and slave controllers on the ILMs. Instead of being connected through a solid signal trace, the ground is interconnected through the terminals of the ILM, and long trace lengths allow for EM coupling. In these instances, it is frequently helpful to use differential communication in which data is transmitted based on the difference between two signals instead of with respect to a ground reference. As with single-ended communication, differential driving signal strength must be sufficiently robust. Low-voltage differential signaling (LVDS) is one example of a high-speed differential communication protocol. The LVDS standard utilizes a 350 mV differential voltage swing around 1.25 V with an allowed common-mode voltage range of 0.05 V - 2.35 V to transfer data at speeds of 650 Mbps or even higher at reasonable power levels. The LVDS standard requires a termination resistance of 90-132 Ω and has a standard drive strength of 3.5 mA [148]. For signaling requirements typical of power converter applications, RS485/422 is slower but more robust with a specified common mode voltage range of -7 V, to +12 V, and a differential voltage of 1.5 V across a termination load as low as 54 Ω, correlating to a minimum driving strength of 28 mA [149].

As will be discussed further in Section 5.5.2, the final revision of inverter hardware incorporated the Broadcom AFBR-59F1Z optical transceiver for communication between ILM modules and the master control card. This device was selected due to its small physical size and cable locking mechanism which allowed for the use of bare plastic optical fiber (POF). The AFBR-59F1Z is an LVDS to optical transceiver and LVDS interface chips were used for the short connection between the FPGA and the optical transceiver. A POF razor cutting

tool from FiberFin was used to cut and finish the fiber in a single step. This approach facilitated quick assembly and an overall compact design.

Data communication between the master and slaves was accomplished using asynchronous Manchester protocol. For this work an open-source VHDL-based Manchester driver was modified to provide the needed functionality. This included a start and stop sequence in addition to zero padding to prevent the AFBR-59F1Z transceivers from transitioning into power-saving mode between data packets spaced at 10 μs. A single data packet being transmitted between the master and slave is shown in Fig. 5.25. Data transfer from the master FPGA to a PC for control tuning is accomplished using a PC-based Python terminal and an SPI to USB link from FTDI. This communication allows the data processed in the FPGA to be viewed and stored on a PC for troubleshooting and documentation purposes.

5.5.2 FCML Inverter Development

Applying the lessons learned in FCML implementation in [10], and Chapter 3, three follow-on generations of FCML-based inverters were designed in parallel with this drive system by research collaborators. These prototypes use 200 V rated EPC2034 GaN FETs each driven by an isolated power supply and gate driver. This design eliminates the need for half-bridge boot-strapped gate drivers which limited the usable blocking voltage of the switches in Chapter 3 to a maximum of 100 V. With the ability to allow higher switch stress utilization, the allowed capacitor voltage ripple range is increased and the required flying capacitance decreased.

A key innovation in each of these converters is the use of the FR-4 PCB material as the primary voltage blocking medium within the commutation loop. As discussed in Chapter 3 the reduction of parasitic switching inductance in the FCML converter is paramount to the efficient, reliable operation of the FCML converter. As the voltage of the converter is increased, the minimum commutation loop must be increased to maintain creepage and clearance distances and avoid electrical arcs. As demonstrated in Chapter 3 it is possible to use local decoupling capacitors to negate this switching loop inductance, but in spite of their adequate nominal voltage rating, these capacitors pose a potential arc location because of their small size.

In order to eliminate the need for separate decoupling capacitors and reduce the FCML commutation loop inductance using only the primary flying capacitors, a double-sided design was implemented. This approach utilizes the high dielectric constant of the FR-4 board material to separate electrical potentials instead of depending on the much lower dielectric

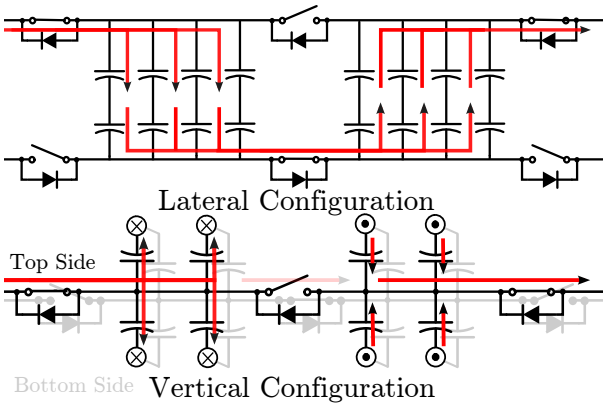


Figure 5.26: Comparison of the current path for lateral and vertical switching cell configuration.

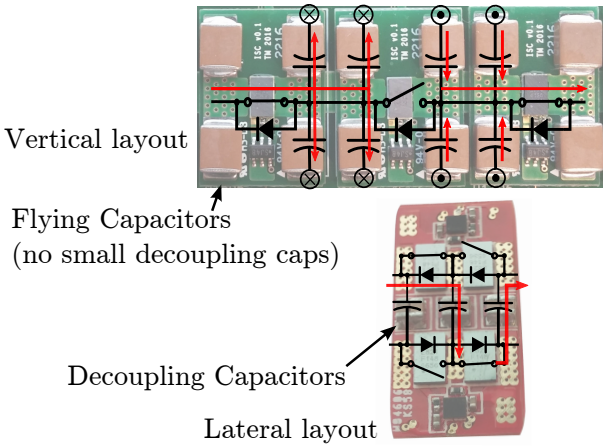


Figure 5.27: Comparison of the vertical and horizontal FCML switch layout. The small decoupling capacitors are replaced by larger flying capacitors in the vertical design.

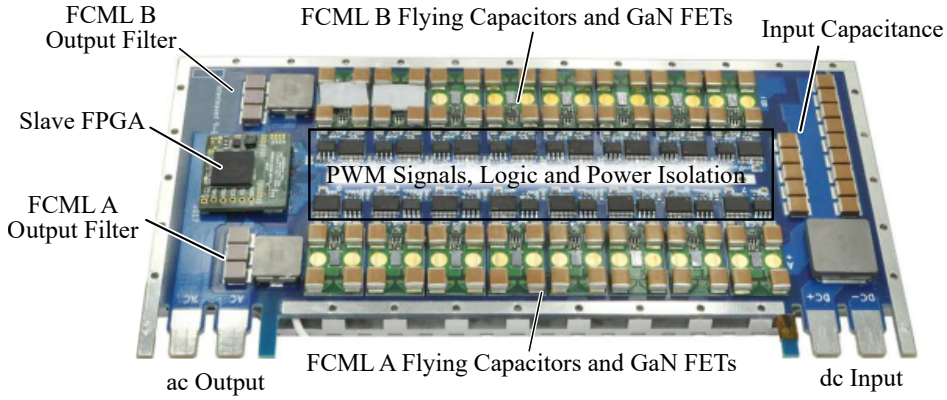


Figure 5.28: Generation 1 of Interleaved Inverter Modules (ILMs) incorporating dual, interleaved, 9-level FCMLs [12].

constant of air which would require a larger spacing distance between components and incur a higher parasitic inductance in the circuit. By separating high potential differences on either side of the PCB, the overall commutation loop area is reduced while maintaining adequate clearance. Figure 5.26 traces the current path for both the lateral switch configuration demonstrated in [10] and Chapter 3 and the vertical configuration demonstrated in [11, 12]. It can be seen that the lateral configuration results in significant loop area while current flow in the vertical configuration folds back on itself, reducing the impact of trace inductance. In Fig. 5.27 the current path is traced over the image of the switching cells to demonstrate the implementation strategy more clearly.

Following tentative plans for aircraft hybridization as outlined in Chapter 1, these inverters

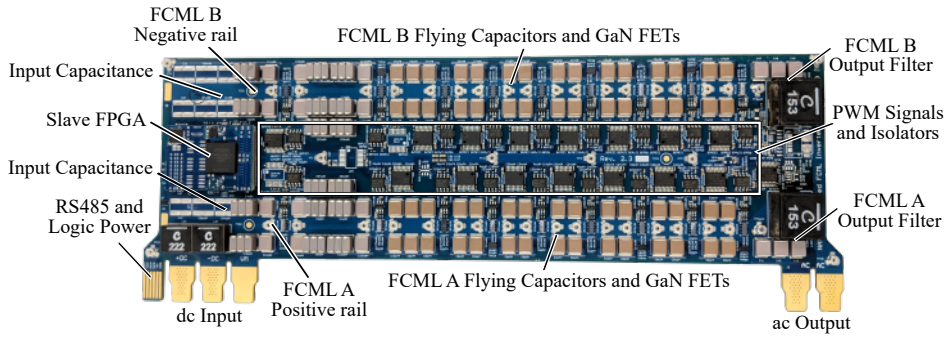


Figure 5.29: Generation 2 ILM. Dual, interleaved 10-level FCML design reduces impact of dynamic R_{dsON}. Separating signal and power traces forces opposite polarity dc supply rails on FCML A and B.

are rated for a 1 kV bus. The overall power density is optimized through the use of 9 or 10-level FCML inverters switching at 100-120 kHz. In order to further reduce the ripple at the input and output of the converter, each Interleaved Inverter Module (ILM) consists of two parallel FCML inverters which are interleaved as shown in Fig. 5.3. By shifting the relative phase of the two FCML inverters by 180° the effective ripple frequency at the converter input is doubled, reducing the amount of filtering capacitance required. Additionally, the interleaved inductor ripple at the output of the ILM nearly cancels due to the triangular shape of the current ripple, further minimizing the THD at the inverter terminals. Each fully populated FCML incorporates 5 μH of output inductance. These designs utilize ceramic capacitors for the flying capacitors (X7R and X6S) and input and output filter capacitors (NPO). The X7R and X6S flying capacitors were selected to optimize for dc energy storage density at the voltage required for each node, while the NPO filter capacitors were selected due to their low dielectric loss under large amplitude, ac excitation.

Each of these designs is based on a loss model analogous to that developed in Section 4.5. The model was validated using a 3-level FCML and then fed into a Monte-Carlo optimization which was used to generate a large number of designs (50,000). The variables used in the optimization included the type and number of flying capacitors and filter inductors, as well as the number of voltage levels, switching frequency, gate resistance, and the current loading of the inverters [11]. This optimization process led to the 9-level designs shown in Fig. 5.28. The Gen 1 ILM design was demonstrated at 9.7 kW output power with a specific power density of 17.3 kW/kg and a volumetric power density of 35.3 kW/L including the mass of a forced-air heatsink [12].[1]

A key component in the ILM 2 and 3 revisions shown in Fig. 5.29 and Fig. 5.30 was the

[1]The author thanks Dr. Tomas Modeer for leading the development of the Gen 1 ILM, and for the valuable insights he shared with the Pilawa research group during his time at UIUC.

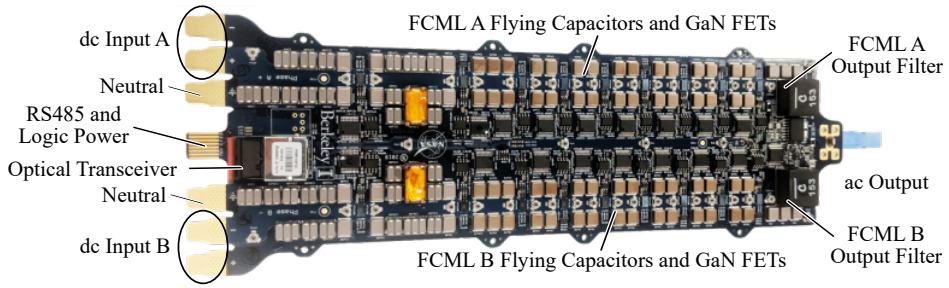


Figure 5.30: Generation 3 ILM. Dc link capacitance is moved to the backplane providing room for POF transceiver [150].

incorporation of accurate dynamic $R_{\text{ds,ON}}$ measurements into the design optimization [103].[2] As mentioned in Section 4.2.1, the impact of dynamic $R_{\text{ds,ON}}$ grows as the switch blocking voltage is increased. For this reason the conduction losses in the inverter do not directly scale with the number of levels. As a consequence, Gen 2 and Gen 3 revisions incorporate 10 levels instead of 9 to minimize overall losses. As mentioned in Section 3.2.2 the nominal voltage stress per switch in an N-level FCML is $\frac{V_{\text{bus}}}{N-1}$. As the number of levels increases, the switch voltage in each switch decreases. This results in lower dynamic $R_{\text{ds,ON}}$ being exhibited by the GaN devices and lower over-all losses in the converter despite the addition of an extra FCML stage.

As discussed in Section 5.3, each ILM includes a local slave controller which is used to generate PWM signals and control the current sensor located on each FCML. ILM Gen 1 utilized the 50 A TLI4970 current sensor from TI which asynchronously sampled the FCML current at 80 kHz and relayed the reading back to the slave controller via SPI when polled. In order to fully synchronize current measurements, the ACS733 analog current sensor from Allegro was paired with the AD7277 ADC from Analog Devices in ILM Gen 2 and 3. This allowed current sampling synchronized with the system-level update frequency.

5.5.3 Drive Assembly

In order to reduce assembly complexity during control prototyping, drive control development was conducted using partially populated versions of ILM Gen 1 and 2 populated to 3 or 4-levels. As discussed in Chapter 3, PSPWM control of FCML converters is highly adaptable to level count, requiring only a change in the phase shift to adjust between level counts. This allows the full system control to be developed at a lower level count without any loss of

[2]The author credits Nathan Pallo for the development of ILM Gen 2 and 3 with input from other members of the research group.

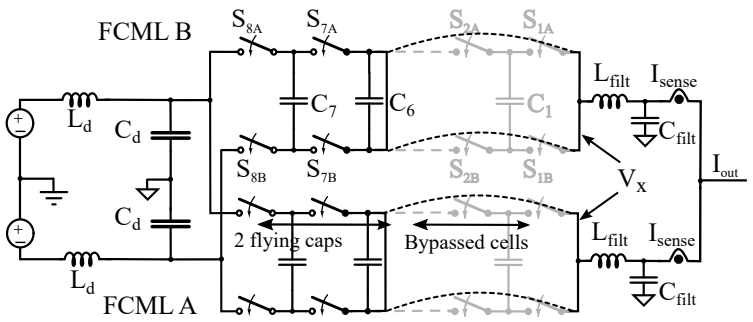


Figure 5.31: Schematic for 9-level interleaved module (ILM) module bypassed to 3 levels for drive development.

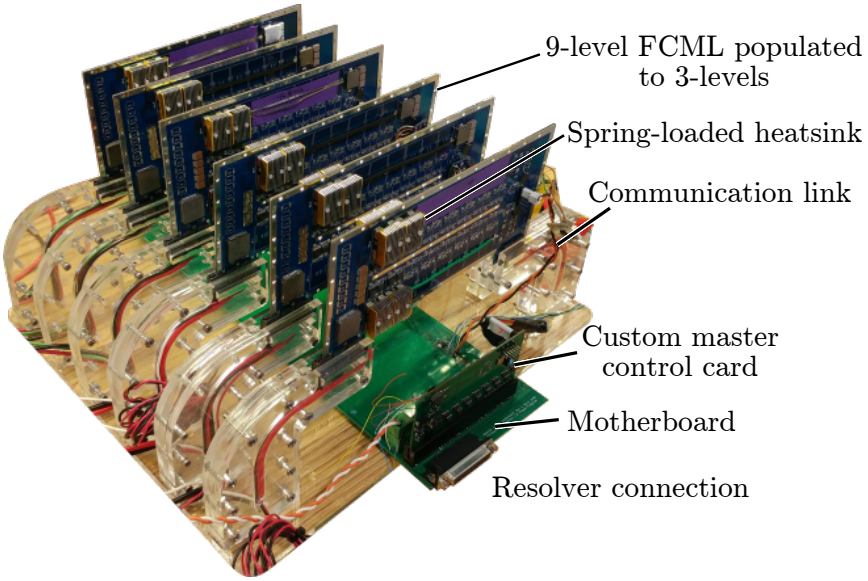


Figure 5.32: Version 1 of FCML-based drive system. Six, 3-level FCMLs assembled into a 3-phase inverter using an acrylic frame.

generality. An abbreviated schematic of the 9-level inverter along with an illustration of how six switch pairs can be bypassed to form a 3-level inverter is shown in Fig. 5.31. All control hardware and current sensing were the same for partially and fully populated hardware.

Generation 1 Modular Inverter Configuration

The architecture of the full modular inverter has progressed through three iterations. Figure 5.32 shows the first revision of the drive system using the Gen 1 ILM. After initial demonstration using evaluation modules for the master FPGA and resolver to digital converter, a signal backplane or motherboard was created to assist in routing data between

the slave controllers and a custom master FPGA control card designed by a collaborator.[3] Using an RS485 communication channel, this system was used to begin development of the control architecture discussed in Section 5.4.2. Because the ILM structure was not finalized at the time of assembly, a wired connection was used between the slave control card and motherboard with the LVTTL-RS485 transceiver wired in line.

Using this hardware, the challenges of position measurement for driving a high-pole-count machine were identified, and the circuit of Fig. 5.17 was adopted to give satisfactory operation at the speeds tested. Despite being a relatively simple control system, the need to maintain communication with 6 FPGAs in order to read measurements from 12 current sensors as well as maintain the operation of 48 sets of isolator, gate drive, and GaN FETs during testing is not trivial. Additionally, the fast switching behavior of GaN FETs makes them unforgiving, and mistakes during testing often necessitate manual rework. Additionally, the unshielded differential connections between the master controller and slaves were subject to electromagnetic interference.

Generation 2 Modular Inverter Configuration

Building on the functionality demonstrated using the first version of hardware in Fig. 5.32, a revision was created to accompany the Gen 2 ILM. In this second revision of the system hardware, the system DC link, as well as logic power and RS-485 signaling, were incorporated into a common backplane. The outputs of the inverter array are also tied into a second backplane with separate routing for each AC terminal.[4] The ac terminals of the individual ILMs in the system are then tied together off the backplane allowing for flexibility in the phase configuration of individual ILMs during testing. Both the dc input and ac output backplanes are mounted to an acrylic base for structural support.

The second revision of backplane also incorporated RS-485 communication between the slave controller on the ILM and the master control card. In order to test communication, the ILM was run with an open-loop sinusoidal PWM modulation programmed in the slave and independent of any communication with the master controller. This operation created the electromagnetic environment which would be observed with the modular drive operating. Under these conditions data was sent in a loop from the master controller through the RS-485 channel to the slave and then back to the master controller. By checking for bit errors between the data sent to and received from the master controller, it was possible to test the susceptibility of the RS-485 communication in the backplane to electromagnetic interference.

[3]The author thanks Pourya Assem for the use of his hardware.

[4]The author credits Samantha Coday for her design of the Gen 2 backplane.

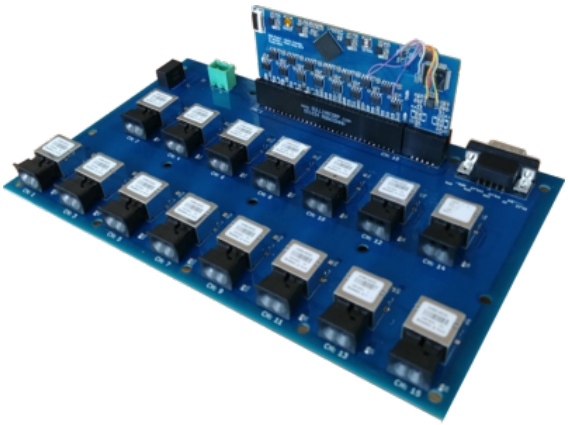


Figure 5.33: Optical adapter board built facilitate communication between master and slave controllers over POF.

Figure 5.34: Optical transceiver breakout attached to slave controller on Gen 2 ILM. This configuration was used to test the asynchronous serial communication which had been modified for use with optical transceivers.

In the process of preliminary testing, it was discovered that the RS-485 communication was unreliable at bus voltages above 600 Vdc. Due to time constraints, the decision was made with collaborators to add the option for POF communication into the final hardware revision in order to continue progress on the system with the highest potential for success. This approach had initially been avoided due to the relatively large size of optical transceivers available on the market, but it was determined to be the best option for ensuring a successful implementation.

Figure 5.33 shows the PCB designed to interface between the master control card and POF lines. This breakout board includes a DB-9 plug interfacing the motor resolver with

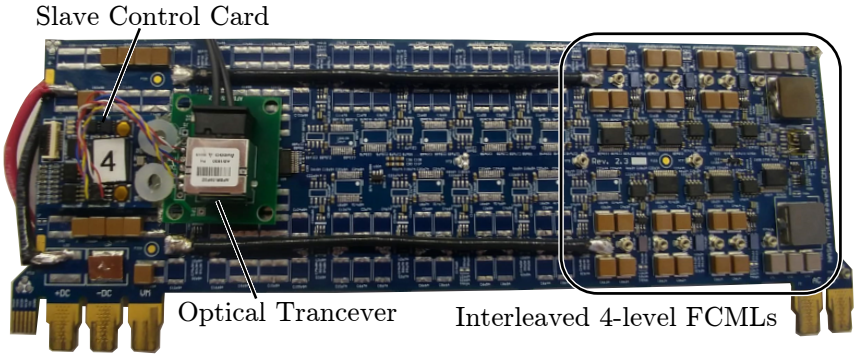


Figure 5.35: Gen 3, 10-level ILM bypassed to four levels for drive development. Optical transceiver added to slave control card.

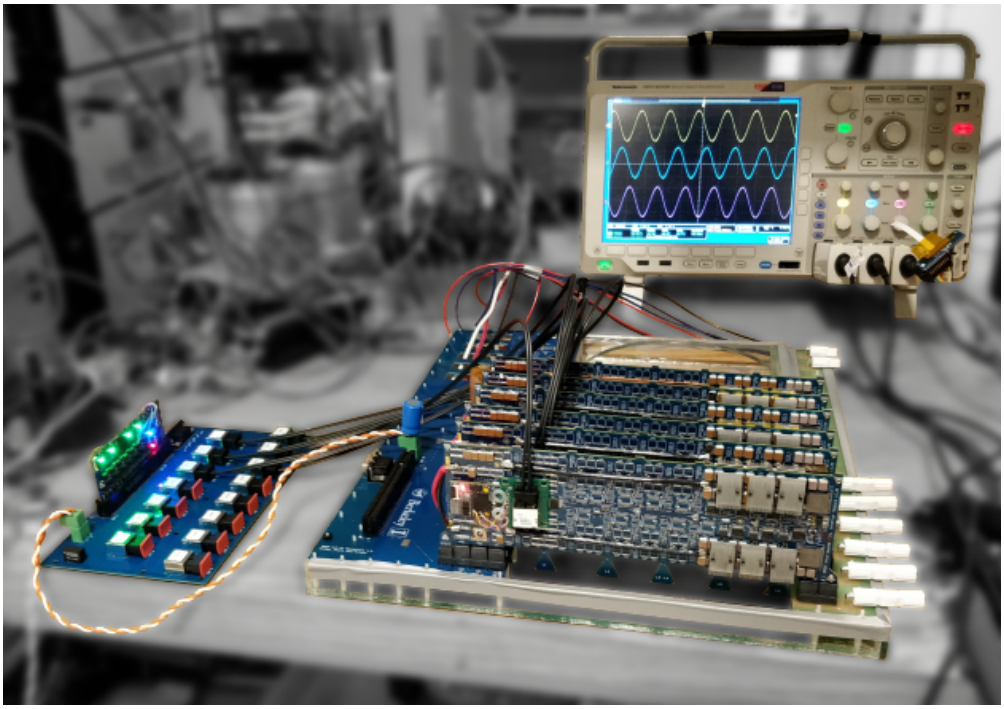


Figure 5.36: Version 2 the modular drive system. Six, 4-level FCMLs combined in a single backplane. Master-slave communication is built into the backplane using RS-485 protocol and the system was adapted to optical communication for final testing.

the master control card as well as POF connections for 15 ILM cards. The number of communication channels was selected to facilitate 5 sets of 3-phase motor windings. The 5 inverters in each phase can be tied together to feed a high-current load or connected to 5 individual winding sets as would be done for the 1 MW machine in Section 5.2. Communication between the master control card and POF transceivers was accomplished using LVDS signaling as required by the POF transceivers.

To facilitate development of the communication code required for the optical transceivers being designed into Gen 3 hardware, an optical adapter board was configured to map the differential signal pairs from the slave control card of the Gen 2 ILMs to the optical transceiver.[5] Figure 5.34 shows the modified slave control card with optical communication which was used for testing. A set of six Gen 2 ILMs were configured for control development with the FCML converters bypassed to 4 levels as shown in Fig. 5.35. The full Gen 2 hardware configured with 6 parallel ILMs is shown in Fig. 5.36. This hardware revision was used to generate the current sharing and 4-level drive results presented in Sections 5.6 and 5.7.

[5]The author credits Pourya Assem for his design of the Gen 2 slave control cards.

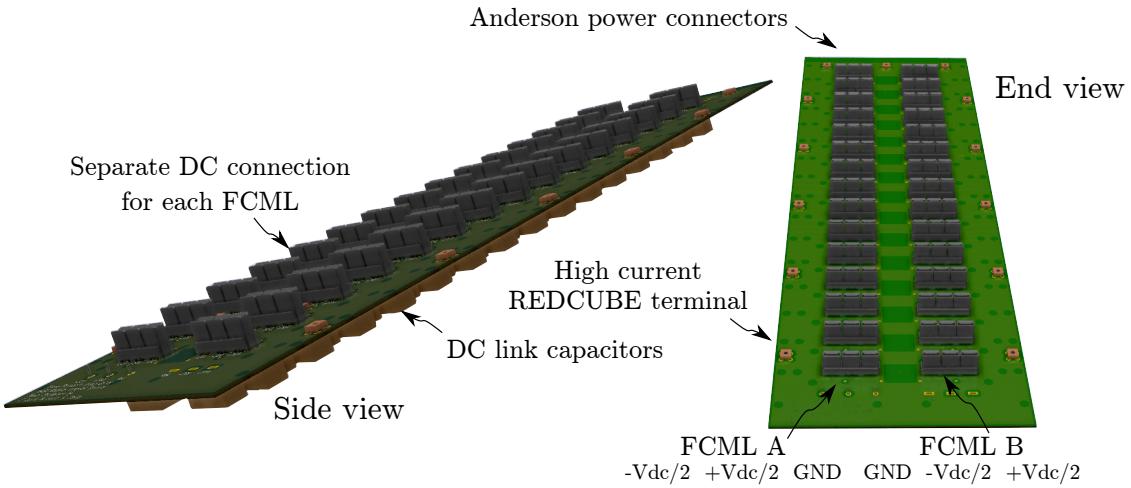


Figure 5.37: Third-generation dc backplane incorporating decoupling capacitors, and DC polarity inversion for FCML A and B.

Generation 3 Modular Inverter Configuration

As articulated in [74], source impedance of the FCML converter is a significant contributor to steady-state imbalances in the flying capacitor voltages. For this reason, adding adequate decoupling capacitance at the input of the converter is an important part of the design of the inverter system. The Gen 1 and Gen 2 ILMs utilized decoupling capacitance located directly on the module. Surface-mount ceramic devices were selected in order to minimize the PCB profile. Because the decoupling capacitors must withstand the full dc-link voltage they are larger and have lower capacitance than the lower-voltage flying capacitors. This limits the amount of dc link capacitance which can be added to the ILM.

Another challenge in the design of the Gen 2 ILM was the mapping of the power path for the two FCMLs from a common dc bus. As depicted in Fig. 5.29, in order to maintain separation between the PWM control signal lines and the power path, all signals are routed through the middle of the ILM. This allows the gate terminals on the GaN FETs, and accompanying isolators and gate drivers to face the middle of the inverter. A drawback of this design is that it forces the polarities of the two FCMLs to be opposite each other, meaning that the positive rail of FCML A is on the same side of the board as the negative rail of FCML B. At the ac terminal this arrangement is of no consequence as the output voltages of the two inverters are equal. However, opposite polarity dc rails are needed at the FCML input on each side of the FCML. In ILM Gen 1 this polarity reversal was accomplished on the PCB occupying board space and an extensive number of vias. In ILM Gen 2, this polarity reversal was accomplished using an external connection which incurred lower conduction losses, but increased assembly complexity.

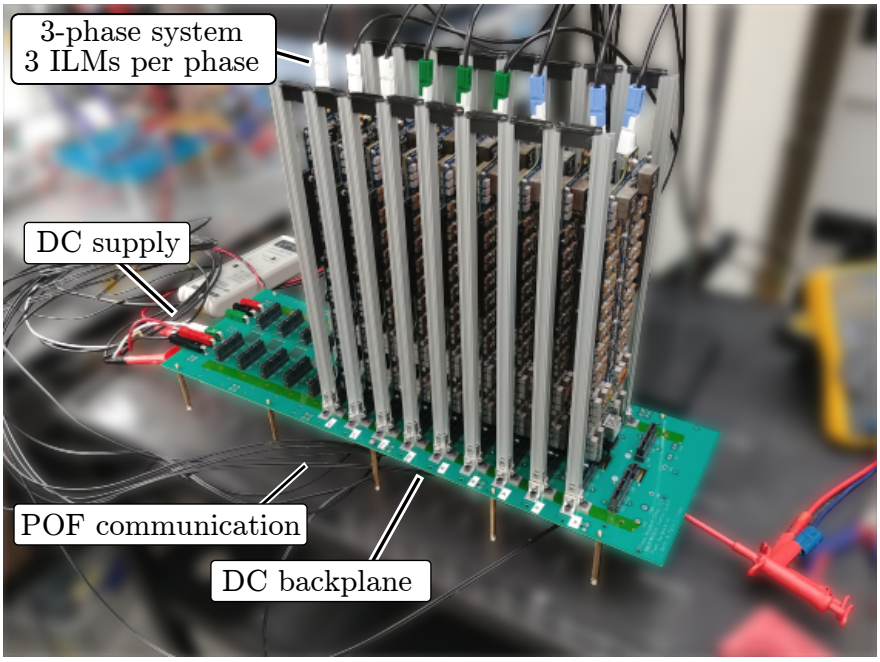


Figure 5.38: Third-generation inverter system assembly with 3 inverters per phase for a total of 9 inverters.

In order to incorporate additional decoupling capacitance on the DC link, as well as to eliminate the need for dc link polarity reversal on the ILM, a third generation of backplane and cooling structure was developed. This design shifted the dc-link connections from the side to the end of the FCML with separate dc link terminals for each FCML in the ILM. The removal of much of the dc link capacitance from the ILM created room for the addition of the optical transceiver which was added to ensure robust communication.

A rendering of the backplane designed for the Gen 3 ILM is shown in Fig. 5.37. The inverter system was tested in a split-bus configuration with the positive and negative dc rails centered around ground. Four 2.2 μF film dc link capacitors were included for each ILM with two capacitors placed between each rail and ground at the input of each FCML. In order to minimize parasitic inductance and resistance, a complete layer of the PCB was designated for each voltage rail ($+V_{dc}$, $-V_{dc}$, and ground) with a fourth layer used to provide additional interconnection. In addition to Anderson power connectors at the end of the board, Redcube terminals from Wurth were added to facilitate high-current operation.

The preliminary assembly and testing of the Gen 3 drive system was completed shortly before the writing of this dissertation. In addition to the backplane redesign, the revision required significant mechanical design by other members of the Pilawa research group.[6]

[6]The author credits Nathan Pallo and Joseph Schaadt for their extensive work on the design and fabrication of the Gen 3 modular inverter support structure.

Table 5.2: Key control system components.

Component	Part Number
Master FPGA	Intel - 10M40SAE144
Slave FPGA	Intel - 10M16SCU169C86
Resolver decoder	Analog Devices - AD2S1205
Resolver	LTN - RE-21-1-V02
USB to SPI converter	FTDI - C232HM-DDHSL-0
ILM Gen 1 I sense	Infineon - TLI4970D050T5XUMA1
ILM Gen 2 and 3 I sense	Allegro - ACS733 and Analog Devices - AD7277
Optical Transceiver	Broadcom AFBR-59F1Z

Figure 5.38 shows the Gen 3 drive system assembled in a low-power testing configuration with 3 inverters operating in parallel per phase. Additional baffling and enclosures are needed to direct cooling air for full-power operation. System control is accomplished using the control board shown in Fig. 5.33. Table 5.2 gives a list of the key control hardware used in the implementation of this system.

5.6 Modular Drive Operation with Resistive Load

The demonstration of the drive system was first performed using a resistive load before demonstration as a motor drive. Throughout the development of the modular inverter drive control and hardware, the SPI link with USB interface depicted in Fig. 5.19 enabled data debugging and tuning. This step was critical for control implementation in the FPGA, and several plots in this section utilize readings taken directly from the master controller in addition to data collected using a lab oscilloscope.

5.6.1 High-Frequency Operation and Capacitor Voltage Balancing

As discussed in Section 3.3, successful utilization of capacitor self-balancing depends on the inverter modulation frequency being significantly slower than the converter self-balancing dynamics. Thus there is a limit in the highest fundamental frequency that can be achieved for a particular FCML implementation. Figures 5.39 and 5.40 show the 4-level FCML balancing when the inverter is running at a 2.7 kHz fundamental frequency at light and moderate load. This is the rated frequency of the ThinGap machine. It can be seen that the converter self-balancing is more than adequate for the required drive frequency as in both figures the four levels of operation are cleanly defined without distortion. The switch-node

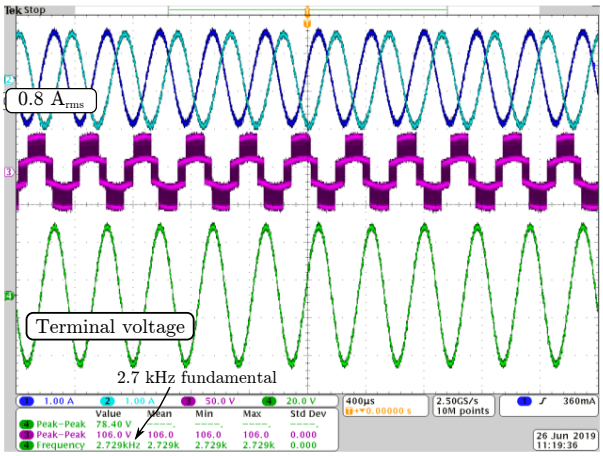


Figure 5.39: Capacitor voltage balancing at 2.7 kHz fundamental with 0.8 A_{RMS} load current. High fundamental frequency has negligible impact on voltage balancing.

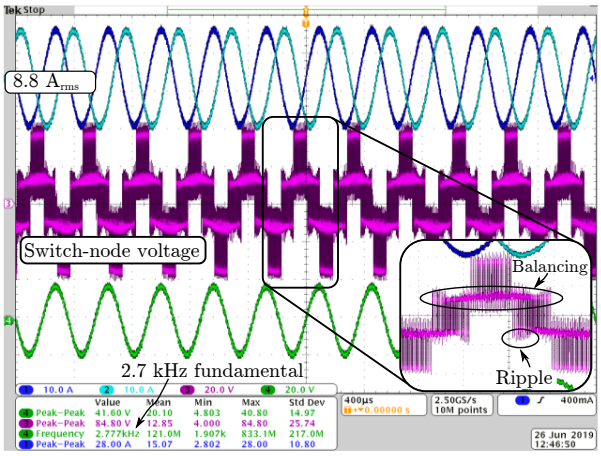


Figure 5.40: Capacitor voltage balancing at 2.7 kHz fundamental with 8.8 A_{RMS} load current. Voltage balancing is maintained.

waveform in Fig. 5.40 shows capacitor voltage ripple at the edges of the level transitions, but the average capacitor voltages, indicated by the definition of the four output voltage levels, are still balanced.

During testing, electrical power measurements were taken at the dc bus, and between the inverter and wye-connected resistive load. The ac power leaving the drive was measured using the 2-wattmeter method in which the line currents for phase A and C are measured as well as the voltages from A to B and C to B. The power measurement taken by each wattmeter are

$$P_1 = V_{\mathrm{AB}} I_{\mathrm{A}} \cos(\theta_{\mathrm{VAB}} - \theta_{\mathrm{IA}}) \tag{5.11}$$

and

$$P_2 = V_{\mathrm{CB}} I_{\mathrm{C}} \cos(\theta_{\mathrm{VCB}} - \theta_{\mathrm{IC}}). \tag{5.12}$$

With the aid of the trigonometric product identities, it can be shown that

$$P_2 + P_1 = 3 V_{\mathrm{ln}} I_{\mathrm{l}} \cos(\theta_{\mathrm{V}} - \theta_{\mathrm{I}}) = P_{3\phi} \tag{5.13}$$

and

$$\sqrt{3}(P_2 - P_1) = 3 V_{\mathrm{ln}} I_{\mathrm{l}} \sin(\theta_{\mathrm{V}} - \theta_{\mathrm{I}}) = Q_{3\phi}. \tag{5.14}$$

Therefore, provided care is taken to identify the meters, both the real and reactive power can be calculated. Reversing the meters will reverse the sign of $Q_{3\phi}$.

Table 5.3 provides the power measurements for the power from the resistive load test

Table 5.3: Test data from drive system feeding wye-connected, 3-phase load

Test #	Frequency Hz	Load Ω	Vdc V	P_{dc} W	$P_{3\phi}$ W	$Q_{3\phi}$ VAR	Measured P.F. $\frac{P_{3\phi}}{S_{3\phi}}$	η
1	65	30.6	98.6	70.9	66.2	-0.9	1.00	93.4%
2	647	30.6	99.8	72.7	67.9	-0.7	1.00	93.4%
3	1285	30.6	98.9	71.6	66.8	-0.4	1.00	93.3%
4	2729	30.6	98.6	71.5	66.6	0.4	1.00	93.0%
5	2729	1.5	78.4	364.5	349.1	23.4	1.00	95.8%

		W meter 1			W meter 2		
Test #	V_{AB} V_{RMS}	I_A I_{RMS}	P_1 W	V_{CB} V_{RMS}	I_C I_{RMS}	P_2 W	
1	45.209	0.851	33.391	44.910	0.847	32.893	
2	45.761	0.862	34.184	45.460	0.858	33.767	
3	45.335	0.855	33.531	45.072	0.852	33.303	
4	45.230	0.852	33.193	45.048	0.851	33.402	
5	22.732	8.973	167.790	22.708	8.841	181.320	

shown in Fig. 5.39 and Fig. 5.40. This test demonstrated the high-frequency operation driving of the modular drive and capacitor balancing. The low efficiency in the first four rows of data in Table 5.3 is due to the light-load operation of the inverters running at 45 V_{ll} into a 30 Ω load. It can be observed that the measured reactive power is slightly negative and then increases as the frequency is increased. This is in accordance with the increase in reactive power which would be expected as the frequency increases due to the inductance of the wire-wound resistors. At the tested frequency of 2.7 kHz, the 23.4 VAR measured corresponds to a per-phase inductance of 5.7 μH. This is reasonable given the 1-2 m of wire used to connect the wire-wound resistors.

5.6.2 Check of $dq0$ Transformation

The full functionality of the transformation between ABC and dq domains in Fig. 5.21 can be demonstrated by the use of a counter in place of motor position feedback and a resistive load. This approach avoids oscillations which may be induced by inaccurate motor position measurement and allows the consistency of the sinusoidal voltage commands to be validated. Figure 5.41 shows the inverter q-axis current ramping from zero to a set point. The inset shows a closeup on the applied q-axis voltage and the resulting q-axis current. It is observed that there are oscillations which occur in the inverse $dq0$ transformation as a result of ripples in inductor current and PWM generation as well as rounding in the fixed-point calculations,

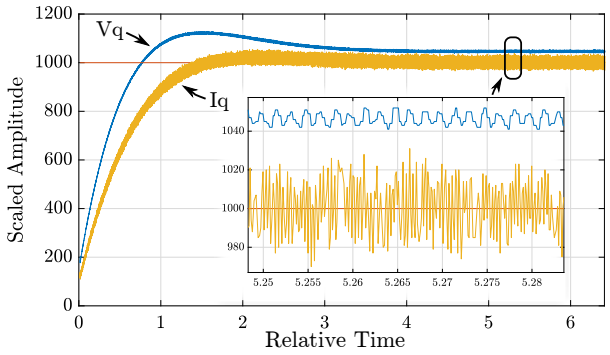


Figure 5.41: Ramp of q-axis voltage and current into a resistive load for demonstration. Time stamp from master controller is approximate.

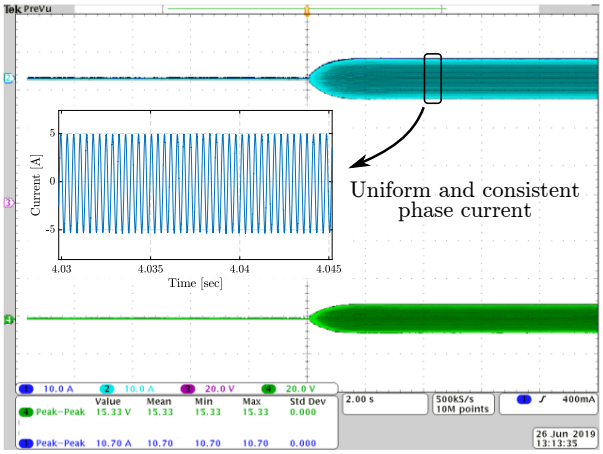


Figure 5.42: Current on phase A during i_{sq} ramp. Data captured concurrently with Fig. 5.41.

but the waveforms are periodic and consistent. Figure 5.42 shows the envelope and a closeup of the A phase current captured on the oscilloscope concurrently with Fig. 5.41. The inset replots the oscilloscope data and shows that the drive currents are uniform and sinusoidal.

5.6.3 Demonstration of Current Sharing

Figure 5.43 shows the measurement of $i_{\mathrm{A}}(t)$ as defined in Fig. 5.20 being supplied by 2 parallel ILMs. This data is the instantaneous current measurements from four FCMLs sent back through the slave controllers on each ILM and added together in the master controller. The master controller then calculates the rectified average and divides it by the number of ILMs operating in parallel to calculate the $I_{\mathrm{PhaseA\_ILMavg}}$ and then $I_{\mathrm{PhaseA\_FCMLavg}}$ as shown in Fig. 5.20. Because there are two FCML converters operating in each ILM, $I_{\mathrm{PhaseA\_ILMavg}}$ is twice the $I_{\mathrm{PhaseA\_FCMLavg}}$. The same process of addition and averaging is executed when the drive system is equipped with a higher number of parallel ILMs for larger loads. As discussed, the control distribution of Fig. 5.20 is used to distribute the coordination variable, which is the reference average current, to the array of N ILMs in each phase. The coordination PI controller on each FCML in the system then adjusts the duty ratio scaling as outlined in Section 5.3.1 and illustrated in Fig. 5.6 to match this reference value. Because this compensation is designed to account for hardware tolerances and mismatched thermal loading, low gains are used to match the individual FCML currents over several seconds.

The system-wide current sharing was demonstrated by separating the ac terminals of

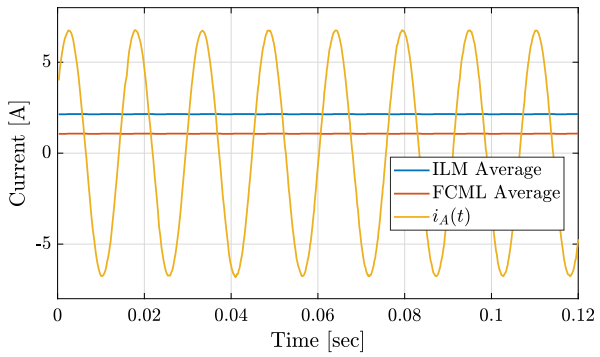


Figure 5.43: Motor phase current as well as ILM and FCML average values read from master controller over SPI.

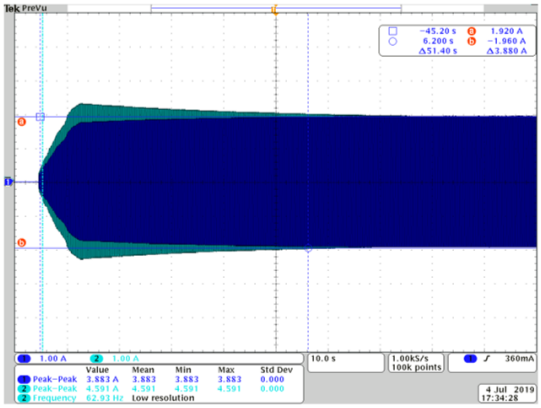


Figure 5.44: Duty ratio compensation used to evenly distribute load current.

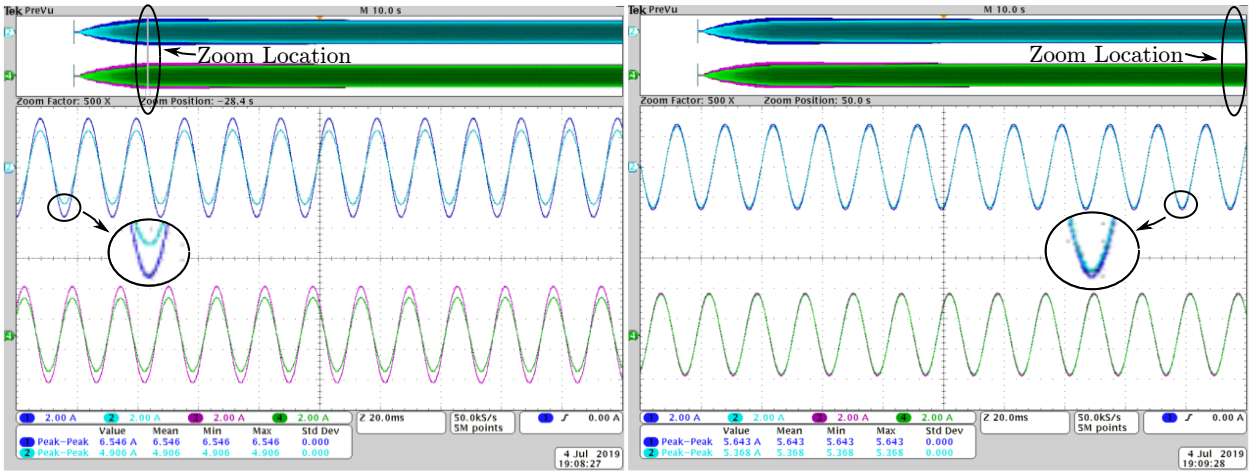


Figure 5.45: Converging current amplitude for 2 phases in a 3-phase system. Slow proportional control is used to compensate for a 30% load mismatch in roughly 90 sec.

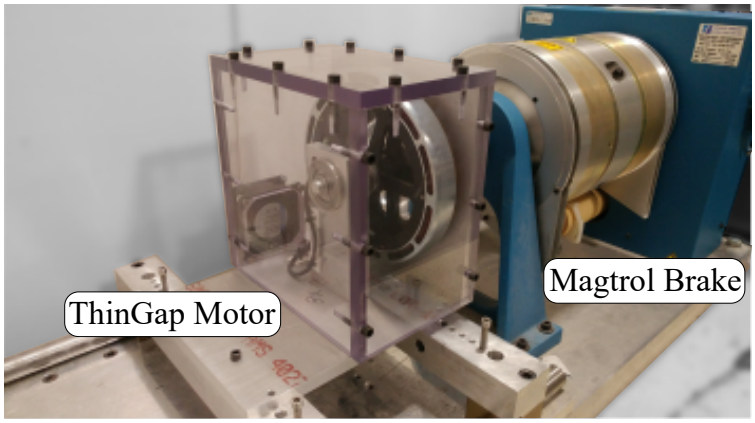


Figure 5.46: Magtrol hysteresis dynamometer with mounted ThinGap motor.

the 6-ILM system (2 ILMs in parallel per phase) to allow the system to be connected to separate 3-phase loads. Two separate wye-connected 3-phase loads were configured with a 30% mismatch (8 Ω and 11 Ω) and the six ILMs were connected to the loads. This configuration represents the impact of imbalances in parallel loads as well as steady-state differences in the current sourcing capabilities of individual ILMs. The large 30% imbalance is for illustrative purposes and likely highly exceeds any imbalance which would be observed in practice. Figure 5.44 shows the envelope of the current leaving two parallel ILMs. Initially there is a mismatch due to the imbalance in load, but the balancing control gradually brings the converter load currents to the average value.

Figure 5.45 expands the converging current envelopes to show the difference in the amplitude of the sinusoidal phase currents at the beginning and end of the duty ratio scaling. The initial figure on the left shows a mismatch in current amplitude between the two ILMs in phase A. Over a period of about 90 sec, a slow integral control is used to scale the reference duty ratio sent to each FCML and force the current amplitudes to converge.

5.7 Modular Drive Operation with PMSM Machine

As discussed, the drive system operation has been demonstrated using the ThinGap motor. During testing the motor was mounted to a Magtrol hysteresis dynamometer (model HD-815-8N-4488) as shown in Fig. 5.46. The Magtrol DSP6001 brake controller was then used to set the operating speed or load torque applied to the machine. In addition to the electrical power measurements described in Section 5.6 the mechanical power applied to the dynamometer was also recorded.

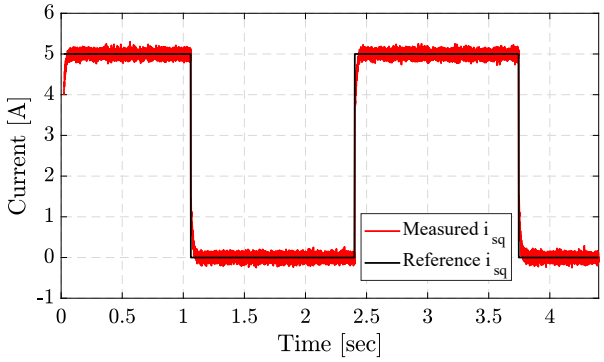


Figure 5.47: Critically damped i_{sq} step response during tuning of the i_{sq} and i_{sd} controllers. Both reference and measured values read from the master controller.

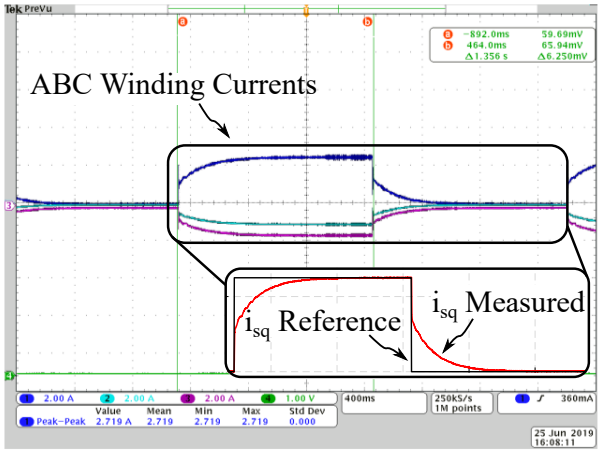


Figure 5.48: Overdamped i_{sq} step response in ABC and dq winding currents with rotor stationary. ABC winding currents are measured using oscilloscope and q-axis current read from master controller.

5.7.1 Controller Tuning

Vector-based control allows the opportunity for precise control of motor field and torque. As the focus for this work was the demonstration of the coordinated control of a modular motor drive system, the motor dynamic response was not considered a priority. Therefore, the controller gains were selected to allow the motor to start safely and operate at steady state. To meet this objective, the controllers were experimentally tuned based on their step response. The stator d-axis and q-axis winding voltages, v_{sd} and v_{sq}, can be formulated as

$$v_{sd} = R_s i_{sd} + \frac{d}{dt}\lambda_{sd} - \omega_m L_s i_{sq} \tag{5.15}$$

and

$$v_{sq} = R_s i_{sq} + \frac{d}{dt}\lambda_{sq} + \omega_m (L_s i_{sd} + \lambda_{fd}), \tag{5.16}$$

where R_s is the stator phase resistance and L_s is the sum of the stator leakage (L_{ls}) and magnetizing inductance (L_m). The terms λ_{sd} and λ_{sq} are the d-axis and q-axis flux linkages and λ_{fd} is the flux linkage of the stator d-axis winding with the rotor magnet flux.

It can be seen that the quadrature axis current shows up in the calculation of direct axis voltage and the reverse for $\omega_m > 0$. Therefore, the precise control of i_{sq} and i_{sd} currents when the motor is running requires the use of a decoupling term proportional to the motor speed [143]. However, provided the motor is stationary, the i_{sd} and i_{sq} step response may be tuned independently.

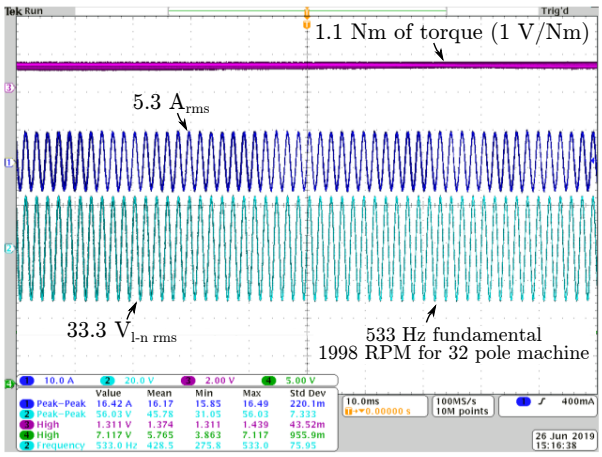


Figure 5.49: Line current and voltage when driving the 32 pole ThinGap motor at 2 kRPM. This equates to 15,990 RPM for a 4-pole machine

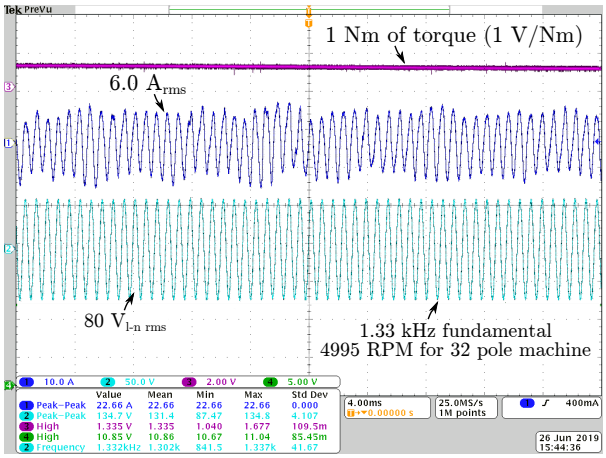


Figure 5.50: Waveforms from driving the ThinGap motor at 5 kRPM.

In order to fix the stator q-axis in position, the resolver position feedback was disconnected. The master controller was then used to command a step current separately on the d and q axes. This allowed both controllers to be tuned for a damped or overdamped response. Figure 5.47 shows the reference and measured q-axis current during tuning as read from the master controller. Figure 5.48 shows an overdamped controller step response in both the ABC and dq domain. The 3-phase currents captured on the oscilloscope are transformed into the q-axis current shown in the subset by the master controller. For a salient machine it would be important to align the d-axis of the stator and rotor before tuning, but the ThinGap machine is non-salient, and there is no change in the inductance with position.

5.7.2 Demonstration with 4-level ILMs

The operation of the ThinGap motor was conducted using both single and parallel 4-level ILMs per phase. Beginning with a single ILM per phase, the ThinGap motor was driven at 1 Nm of torque up to 5 kRPM. For demonstration of steady-state performance, the drive d-axis current was set to zero, and the q-axis current was set to achieve the desired torque. The Magtrol brake controller was then used in conjunction with a Magtrol hysteresis dynamometer to set the operating speed. As the motor speed was increased, the dc link voltage was also raised to prevent the saturation of the d-axis and q-axis controllers.

Figure 5.49 shows the phase current and voltage when driving the ThinGap machine at 2 kRPM and 1.1 Nm of torque using a single ILM. It can be seen that the line current is

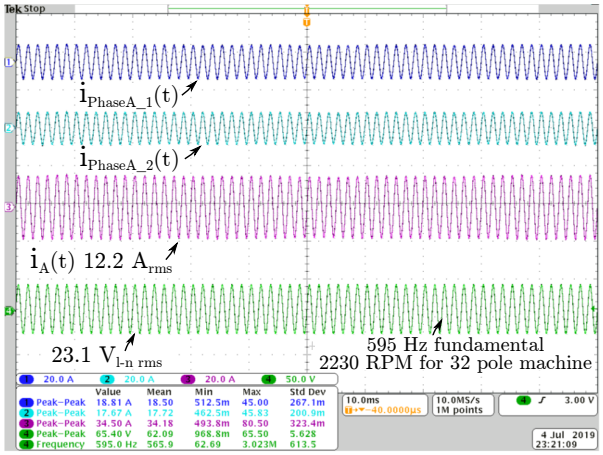


Figure 5.51: Two ILMs driving the ThinGap machine at 2.95 Nm of torque, 2200 RPM.

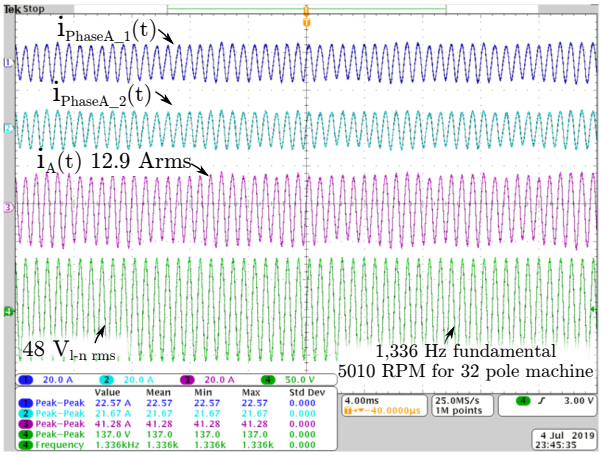


Figure 5.52: Two ILMs driving the ThinGap machine at 2.85 Nm of torque, 5010 RPM.

smooth and without any of the oscillations discussed in Section 5.4.1. The flat line at the top of the plot is an analog representation of the motor torque which is also displayed on the DSP6001 controller. Figure 5.50 shows the inverter performance at 5 kRPM. It is observed that although there are no ripples visible in the inverter voltage, the interaction between the drive and the high-pole-count machine is creating irregularities in the phase current.

The operation of parallel ILMs for driving the ThinGap machine is shown in Fig. 5.51 through Fig. 5.53. The manufacturer-specified peak continuous torque for the machine ranges from 2 to approximately 4 Nm depending on rotation speed, with a higher rotation speed facilitating higher continuous torque [130]. Starting at 2200 RPM and 3 Nm, Fig. 5.51 shows the sinusoidal current and voltage of the two ILMs working together to source 12.2 A_{RMS} phase current. At this speed there are no ripples in the envelope of the phase currents. In Fig. 5.52 the motor has been accelerated to 5 kRPM with the same q-axis current set point. Figure 5.53 shows the operation of the drive at 6 kRPM. At this speed the amplitude oscillations have again begun to surface although the drive operation is stable.

Analysis of 4-level Drive Results

Figure 5.54 plots the demonstrated drive power tested vs. fundamental frequency. For perspective, the maximum demonstrated frequency of 1600 Hz equates to a 4-pole machine spinning at 49,800 RPM. Figure 5.55 plots the efficiency of the 4-level drive system operating with 2 parallel ILMs per phase. The drive efficiency is 97% over the range tested except for the lowest power level. This efficiency is acceptable based on the results of the 13-level

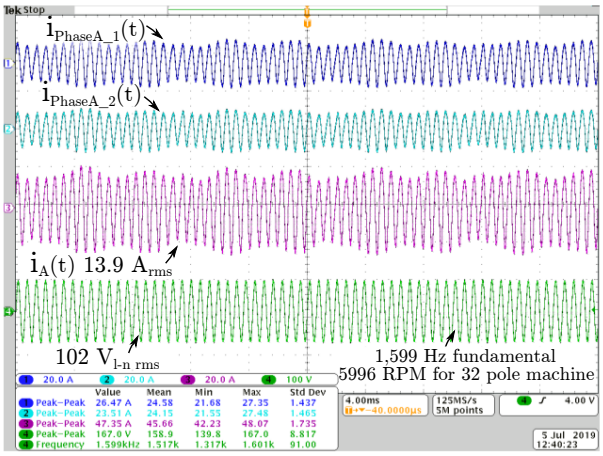


Figure 5.53: Two ILMs jointly driving the ThinGap machine at 2.85 Nm of torque, 5996 RPM. Some oscillations are present in the phase current.

design in Section 3.5 and the 3-level in Section 4.4 at room temperature. It is worth noting that these are light-load results with 13 A_{RMS} of line current distributed between 4 FCML converters due to the 2 ILMs operating in parallel. The efficiency of the inverter system will be higher at full power. The measured data for the ThinGap machine driven by two parallel ILMs per phase is provided in Table B.1 for the reader's reference.

Comparing the efficiency of the ThinGap motor plotted in Fig. 5.55 and listed in Table B.1 to the manufacturer's data sheet values reveals a roughly 6% discrepancy from the 90% peak efficiency published. Reviewing the reactive power drawn by the motor, it is evident that the reactive power drawn by the machine is increasing significantly as the motor speed increases. This dramatic increase in reactive power is not expected for a PM machine under vector control. Unlike a wound rotor synchronous machine, the torque angle between rotor and stator of a vector-controlled PM machine does not increase with increasing load because the angle between the rotor field and the applied field is held constant by the drive system. The analysis of this data was performed after lab measurements were taken. In the process, it was realized that the calculation of reactive power as $\sqrt{3}(P_2 - P_1)$ indicated a leading, capacitive, behavior. This is inconsistent with the understanding of the control-induced phase lag described in Section 5.4.3. Therefore this explanation proceeds with the understanding that the arrangement of wattmeters P_1 and P_2 was reversed during testing with respect to the ABC phase sequence. This discussion is an effort to highlight the challenges in driving a high-pole-count, low-inductance machine as it relates to the phase delay discussed in Section 5.4.3.

Given the high pole count of the ThinGap machine, an increasing reactive power can be understood based on the discussion in Section 5.4.3 regarding the delay between the motor

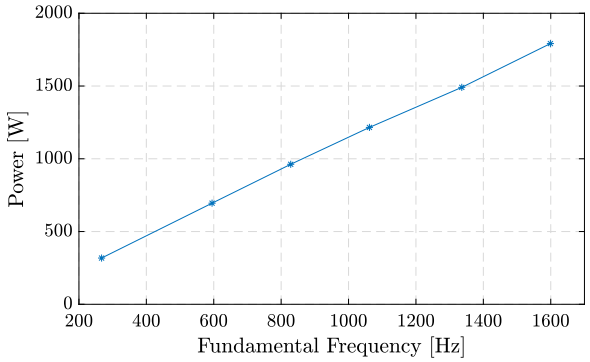


Figure 5.54: Demonstrated motor power vs speed for 4-level modular inverter (2 ILMs per phase) system.

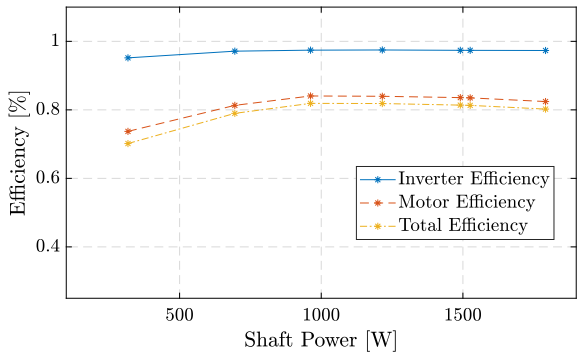


Figure 5.55: Demonstrated efficiency vs power of the combined 4-level modular inverter (2 ILMs per phase) and motor.

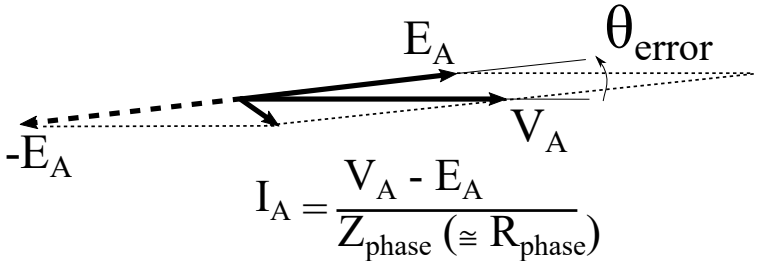


Figure 5.56: Delay in inverter applied voltage (V_A) results in increased lagging line current and inductive reactive power flow.

position reading and the application of the updated PWM and voltage on the ABC windings. As the motor frequency increases, this set value of delay correlates to an increasing phase shift between the PM rotor and the stator applied field. The delay, from the moment of shaft position reading to the application of updated stator voltage, will result in the back-EMF of the rotor leading the field applied by the stator instead of being in-phase as shown in Fig. 5.14. This phase shift will, in turn, result in higher reactive power flow as illustrated by the vector diagram in Fig. 5.56. For illustration, the reactance of the motor is ignored, and the figure accounts for only the winding series resistance. The motor series inductance will cause further lag in the winding current. The calculations which follow include both series inductance and resistance.

The impact of this control delay can be evaluated based on the steady-state machine model shown in Fig. 5.57. Based on data-sheet parameters, the nominal terminal power characteristics can be estimated for the operating conditions tested [130]. Calculations which follow are conducted at the lab measured torque (T_{lab}) and mechanical rotation speed (ω_{lab}) values in order to understand the real and reactive power requirements which would be expected. Selecting the current vector as the zero reference, the nominal RMS line current

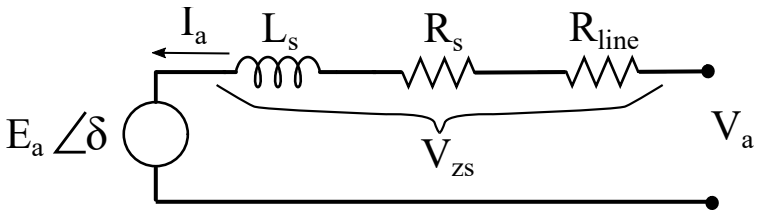


Figure 5.57: Single-phase equivalent circuit for PM machine.

$\hat{\mathbf{I}}_{\text{line}}$ for the machine can be calculated based on the machine torque constant as

$$\hat{\mathbf{I}}_{\text{line}} = T_{\text{lab}}(\text{Nm})\frac{1}{\text{K}_\text{t}}\left(\frac{\text{A}_{\text{RMS}}}{\text{Nm}}\right). \tag{5.17}$$

Using the magnitude of line current, the phasor of the voltage across the series machine impedance ($L\text{s}, R\text{s}$) and motor lead resistance (R_{line}) can be calculated as

$$\hat{\mathbf{V}}_{\text{zs}} = \hat{\mathbf{I}}_{\text{line}}(R_s + R_{\text{line}} + j\omega_{\text{lab}}L\text{s}). \tag{5.18}$$

The magnitude of the motor back-EMF ($\text{Re}(\hat{\mathbf{E}}_\text{a})$) can also be calculated based on the manufacturer-supplied data in line-to-neutral RMS form

$$\text{Re}(\hat{\mathbf{E}}_\text{a}) = \omega_{\text{lab}}0.21\left(\frac{\text{V}_{\text{pkll s}}}{\text{rad}}\right)\frac{1}{\sqrt{2}\sqrt{3}}. \tag{5.19}$$

As discussed in Section 5.4.3 the control implemented during testing included a 23 μs delay between the motor position reading and PWM update. This delay (τ_{control}) will result in $\hat{\mathbf{E}}_\text{a}$ leading the voltage applied by the drive. The phase shift (δ) caused by this delay can be calculated over frequency as

$$\delta = \omega_{\text{lab}}\frac{\text{p}}{2}\tau_{\text{control}}. \tag{5.20}$$

Next the motor terminal voltage ($\hat{\mathbf{V}}_\text{a}$) can be calculated as the sum of the back-EMF and the voltage across the motor series impedance

$$\hat{\mathbf{V}}_\text{a} = \hat{\mathbf{E}}_\text{a} + \hat{\mathbf{V}}_{\text{zs}}. \tag{5.21}$$

Finally, motor apparent power is calculated,

$$\hat{\mathbf{S}}_{\text{total}} = 3\hat{\mathbf{V}}_\text{a}\hat{\mathbf{I}}^*_{\text{line}}. \tag{5.22}$$

The ThinGap machine has a series inductance and resistance of 10.25 μH and 0.118 Ω

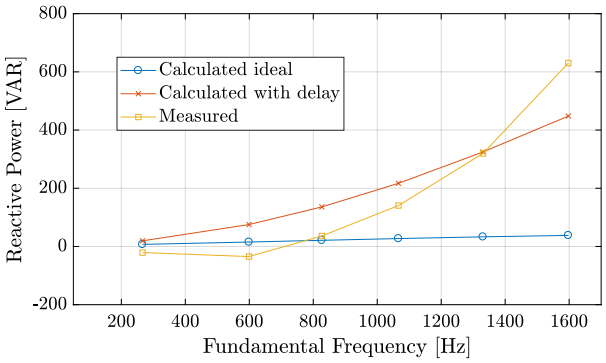


Figure 5.58: Comparison of reactive power drawn by ThinGap motor in lab measurements against reactive power based on motor parameters with in-phase and delayed excitation.

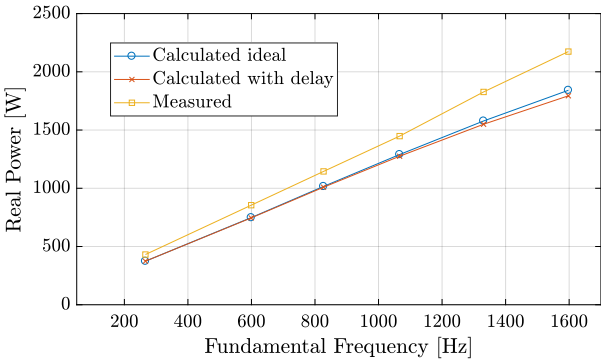


Figure 5.59: Comparison of real power drawn by ThinGap motor in lab measurements against real power based on motor parameters with in-phase and delayed excitation.

respectively [130]. Based on manufacturer-provided data, the theoretical reactive and real power for the ThinGap machine at the torques and speeds tested is plotted in Fig. 5.58 and Fig. 5.59. The low inductance of the ThinGap motor allows it to run at near-unity power factor under optimal conditions. This is beneficial in reducing overall system losses. However, when a phase-shift is introduced between the rotor back EMF and the applied voltage the reactive power drawn by the motor increases quickly. This increased reactive power creates additional losses in the motor and cabling and decreases efficiency. Additionally, the phase shift between the rotor and stator fields decreases machine torque, as discussed in (5.8), further degrading efficiency. The real motor power is plotted in Fig. 5.59 and shows a much reduced deviation from ideal as compared to the reactive power, but power drawn in testing is higher.

One trait which is not considered in these plots is the oscillation in line current shown in Fig. 5.53. This is understood to be caused by the control delay and the resulting distortion in conversion between dq and ABC quantities. These oscillations likely involve fluctuations in the d-axis and q-axis controllers which are not accounted for in stead-state approximations. Based on this analysis, the low efficiency and high reactive power in the motor operation and oscillations at higher speed are considered to be at least partially caused by the need for phase compensation in the drive to account for communication delay when operating at high fundamental frequency. The addition of this feature in future work will be aided by significant prior work in the field including [146].

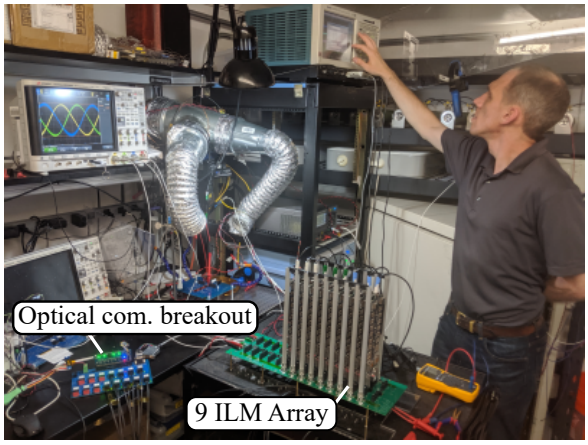


Figure 5.60: Third-generation drive system preliminary test configuration.

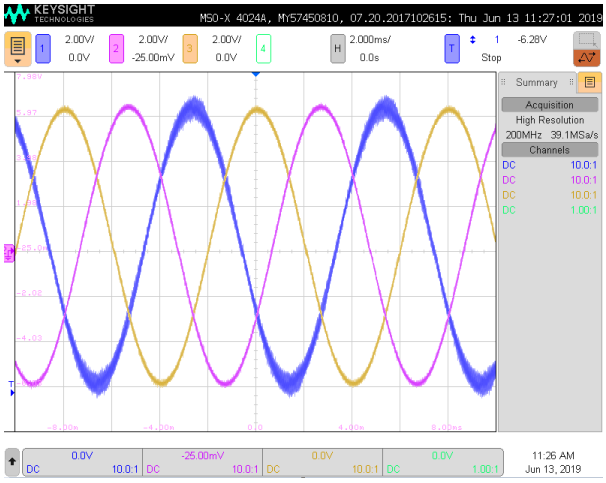


Figure 5.61: Three-phase voltage from set of 10-level ILMs operating in parallel.

5.7.3 Demonstration of Drive Scaling Using 10-level ILMs

The 4-level ILM implementation facilitated the development of the system communication, and of the control required by the FCML drive system. From a controls standpoint, the transition from 4-level hardware to 10-level hardware only requires the adjustment of the PSPWM phase shift from $\frac{360}{4-1} = 120°$ to $\frac{360}{10-1} = 40°$ as discussed in Section 3.2.2. In implementation, the extension to 1 kV introduced additional challenges in ensuring robust communication as the dc link voltage was increased. The addition of fiber optic communication was used to address this issue. The assembled drive system is shown in Fig. 5.60.

The assembly and testing of the third-generation, 10-level system was conducted at the conclusion of this research, and therefore the results obtained are preliminary. Figure 5.61 shows the three-phase voltage from the ILMs coordinated together to form a combined three-phase source. As with the 4-level system, each of the three ILMs share part of the load current. Figure 5.62 shows the phase current from the three ILMs in phase A combined to drive the ThinGap motor off of a 200 Vdc bus. Due to the lack of a motor dynamometer at the test location, a fan was affixed to the ThinGap motor and the machine was mounted in an enclosure for safety as shown in Fig. 5.63. This allowed the demonstration of the basic motor drive functionality. A drawback of the use of a fan instead of the dynamometer was that the negligible load applied to the motor did not allow it to be driven with a meaningful level of torque. As a result the motor torque angle has higher fluctuation and the motor current waveform in turn exhibits amplitude oscillations which are much the same as those shown in Fig. 5.15. At reasonable torque the motor current will respond as described in Section 5.7.2.

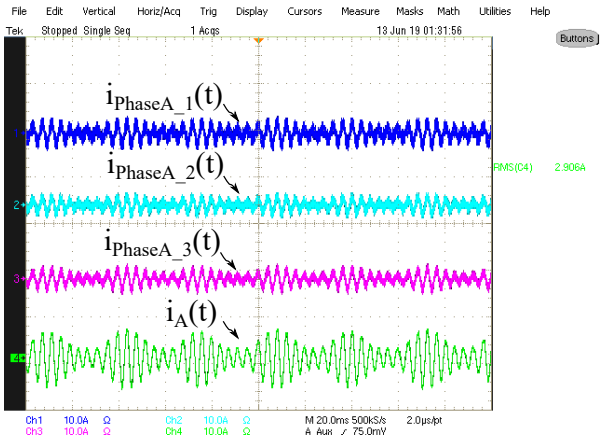


Figure 5.62: Combined phase A current from three ILMs operating in parallel. Ripples in current amplitude are the result of driving the ThinGap motor at light load.

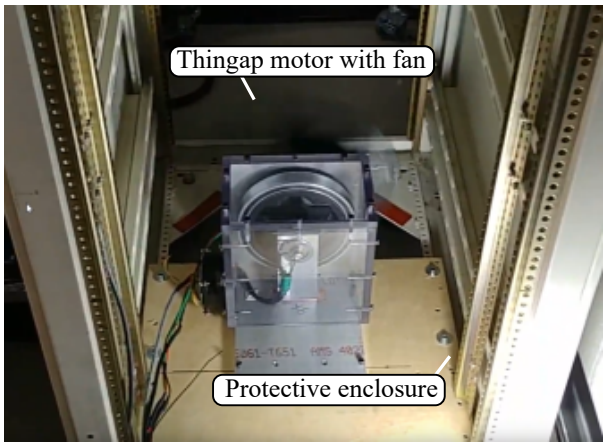


Figure 5.63: ThinGap motor with fan mounted in protective enclosure.

5.8 Conclusions

This chapter has discussed the implementation of FCML-based FOC motor drive specifically tailored for low-inductance, high frequency, electric machines. The FCML topology allows for high power density while maintaining the low-THD required by high-density electric machines. In order to address the reliability needs of aviation applications as well as to provide for system scalability, a modular system approach was followed which allows the system capacity to be adjusted in order to fulfill a range of power requirements. In addition to the sensing and communication requirements for field-oriented control, a modular method for even current sharing among parallel inverter modules was devised and implemented.

Control development was accomplished on a series of two different scaled systems in parallel with the development of the FCML modules. Low-power test results have been completed using scaled 4-level hardware to demonstrate the function of current sharing between inverters. Additionally, the drive system has been demonstrated using a slotless motor with identical per-unit reactance to the intended final target machine. Operation at a speed of 6000 RPM, 1.6 kHz and a torque of 2.8 Nm was achieved. Finally, a system of 9 individual, 10-level, FCML inverters was operated at low power as a preliminary step towards the demonstration of the full 200 kW system.

5.9 Future Work

It is the author's desire that this dissertation provides a valuable reference point for future researchers in the development of FCML-based drive systems. There are a few primary considerations which should be addressed to aid the follow-on work to this dissertation.

5.9.1 Need for a Floating Point Computation Platform

In this work, the use of an FPGA was dictated by the need for high IO count, and the demand for a large number of flexible communication channels. The use of an HDL-coded FPGA enables the precise manipulation of counters for generating a large number of PWM signals or the handling of a large amount of parallel data at the input and output of the master controller. For these purposes, VHDL and Verilog are outstanding tools which offer unparalleled flexibility. The drawback of a purely HDL design is the challenge of working with exclusively fixed-point notation, especially considering the nuances of a strongly-typed language such as VHDL.

Research and industrial development in machine control and drives is typically conducted using relatively high-level languages such as C or more frequently an embedded code generation toolchain such as Simulink Coder. This approach allows the use of floating point notation and the accompanying use of engineering units in control coding. Should the application demand the use of an FPGA, products such as Mathworks HDL coder facilitate the process of converting from high-level languages into HDL. This type of toolchain has saved significant time and expense in industry, allowing control engineers to implement firmware instead of coordinating with an intermediate software engineer [151]. For the modular inverter application, the use of the NIOS II soft processor inside the MAX 10 FPGA may provide a good trade-off allowing the use of single precision (32 bit) floating point computation for tasks which are not time critical while the remainder of the FPGA can still be coded in HDL to implement PWM generation and communication interfaces.

With the aid of floating point calculations, the challenge of motor position measurement could also be addressed using an observer-based approach instead of the resolver-based measurement used in this work. This would be an important aspect of any high-speed commercial drive system.

5.9.2 Increased Phase Shift Precision Capability

As explained in Section 5.4.2, the phase shift of $\pm\frac{2\pi}{3}$ is calculated based on the measured shaft position. As implemented, the resolver generates a 12 bit position value from which is calculated both the d-axis position for the rotor, θ_m, but also phase shifted values of $\theta_m - \frac{2\pi}{3}$ and $\theta_m - \frac{4\pi}{3}$. The 12-bit accuracy of the resolver allows for a resolution of $360°/2^{12} = 0.087°$ "mechanical degrees" which would appear to be more than sufficient. This holds true when driving a 4-pole machine ($360° \times 2/2^{12} = 0.17°$). In contrast, the 32 pole configuration of the ThinGap machine dramatically increases the accuracy requirements of the application as in this arrangement 12 bits of mechanical resolution only results in $360° \times 16/2^{12} = 1.4°$ of electrical resolution.

Because the full resolution of the resolver is not divisible by 3, $2^{12}/3 = 1365.33$, there is an error in the phase shift which can be applied to the 12-bit position counter without the utilization of fractional bits in the calculation. By shifting the resolver reading left, and appending zeros in a fractional representation, the required phase shift accuracy can be obtained. If a 16 bit position representation is implemented (resolver reading with zero appended in the four lowest positions), resolution of $360° \times 16/2^{16} = 0.088°$ is obtained. This phase shift will not impact the resolution of readings from the resolver, as those will still have the equivalent of 12-bit resolution and generate increments of 1.4°. This increase in resolution will allow for precise phase shifting under the challenging requirements of high machine pole count.

The strongly-typed characteristics of VHDL increase the difficulty of recoding the phase shift process in the master FPGA. Additionally, such a change would require the transition from the trigonometric look-up table back to the CORDIC (used in the initial stages of the modular drive implementation), or a rework of the lookup table to avoid a 16X growth in the size of the lookup table. Both changes are entirely feasible but this undertaking was not considered to be a priority in the time available.

5.9.3 Compensation for Signal Processing Time Delay

The analysis of Section 5.7.2 has highlighted the importance of compensating for the delay between motor position measurement and the update in voltage applied to the stator, and it is known that phase delay in high-speed motor control can lead to control instability [152]. This challenge is common for all high-speed drive systems and has been addressed in previous literature [146, 153]. The integration of floating point capability and increased phase resolution into the master controller as discussed in Sections 5.9.1 and 5.9.2 will be a

tremendous help in the efficient implementation of delay compensation.

5.9.4 Demonstration of Redundant Operation

One of the advantages of the modular implementation is the availability of fault redundancy in the event of a failure of one of the ILMs in the system. To facilitate this work a current limit IC has already been added to the ILMs so that a short circuit in control power (frequently arising from the failure of an ILM) in one unit will not disrupt the availability of control power to the remaining ILMs. Failure analysis may indicate that additional disconnects at the inverter input and output may be helpful in isolating faults, but in experience inverter faults most frequently lead to open conditions so this may not be needed. From a drive operation standpoint there are no significant changes needed to continue operation with the loss of an ILM. The failure of an ILM will reduce phase current momentarily, and this change in current will be sensed by the vector control algorithm. The duty ratio for the remaining ILMs in the phase will then be raised to account for the decrease in current in that phase.

5.9.5 Derivation of Current Sharing Between FCML Converters

From a theoretical perspective, there is still significant work to be done to characterize the behavior of parallel FCML converters. The results presented in Section 5.3.1 show relatively minimal current sharing imbalance, but in experimentation it was inadvertently discovered that mismatch in the sizing of flying capacitors resulted in higher sharing imbalance. Under extreme (2X) capacitor mismatch the PWM scaling approach demonstrated here failed to bring the currents into alignment. In simulation it was observed that a 5% mismatch in capacitance led to a significant mismatch in current sharing even in the case of fixed duty ratio operation. However the operation and capacitor voltage balancing of FCML converters is impacted by second-order effects such as inductor core loss which were not included in simulation. Additional work in this space is needed.

CHAPTER 6

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APPENDIX A

SURVEY OF CAPACITOR TWICE-LINE-FREQUENCY BUFFERING PERFORMANCE

Table A.1: Measured 120 Hz capacitor performance data plotted in Fig. 2.10.

#	Description	Manufacturer PN	Efficiency		Q		Density mJ/mm^3	
			Mean	SE	Mean	SE	Mean	SE
1	Electrolytic, 50V, 2700uF	EPCOS(TDK) - B41858C6278M	99.20%	0.14%	809	153	6.03E-2	9.39E-4
2	Electrolytic, 100V, 680uF	EPCOS(TDK) - B41858C9687M	99.45%	0.37%	2074	1550	8.49E-2	2.14E-4
3	Electrolytic, 250V, 100uF	EPCOS (TDK) - B43888F2107M	99.30%	0.34%	5968	10280	1.45E-1	8.92E-4
4	Electrolytic, 450V, 6.8uF	EPCOS (TDK) - B43890A5685M	98.92%	0.40%	698	329	2.08E-1	3.82E-4
5	Film (PEN), 50V, 1uF	Kemet - LDECD4100KA0N00	99.51%	0.35%	3921	3793	9.74E-3	1.96E-5
6	Film (PEN), 100V, 0.068uF	Panasonic - ECW-U1683KC9	99.49%	0.52%	4582	4281	9.40E-3	2.55E-5
7	Film (PEN) 100V, 1uF	Kemet - LDEEE4100KA0N00	99.69%	0.16%	4306	5010	1.97E-2	3.92E-6
8	Film (PEN), 250V, 0.068uF	Kemet - LDEID2680JA5N00	99.03%	0.35%	898	690	3.11E-2	2.12E-3
9	Film (PEN) 250V, 3.3uF	Nichicon - QAK2E335KTP	99.62%	0.29%	2528	1249	2.10E-2	4.90E-5
10	Film (PEN), 250V, 1uF	Panasonic - ECW-U2105KCZ	99.56%	0.35%	3277	2675	3.80E-2	7.06E-5
11	Film (PEN), 400V, 0.1uF	Kemet - LDEME3100JA5N00	98.45%	0.43%	448	173	3.39E-2	7.45E-5
12	Film (PEN), 450V, 1.5uF	Panasonic - ECQ-E2W155KH	99.64%	0.11%	1934	666	4.29E-2	2.55E-5
13	Film (PEN), 630V, 0.033uF	Panasonic - ECW-UC2J333JV	98.05%	0.40%	331	69	2.88E-2	2.18E-4
14	Film (PEN), 630V, 1uF	Nichicon - QAK2J105KTP	99.13%	0.13%	732	128	1.89E-2	2.55E-5
15	Film (PP), 100V, 10uF	Cornell Dubilier - 935C1W10K-F	99.54%	0.14%	1545	668	3.99E-3	9.80E-6
16	Film (PP), 300V, 60uF	EPCOS (TDK) - B32678G3606K	99.67%	0.22%	3332	1482	2.71E-2	5.88E-5
17	Film (PP), 450V, 4.7uF	Panasonic - ECW-FD2W475J	99.85%	0.15%	6753	4364	1.10E-1	2.16E-4
18	X5R, 50V, 4.7uF	TDK - C2012X5R1H475K125AB	95.65%	0.45%	140	15	3.88E-1	1.90E-2
19	X5R, 50V, 10uF	Kemet - C1210C106K5PACTU	88.57%	0.23%	49	1	1.15E-1	2.80E-4
20	X5R, 100V, 1uF	TDK - C3216X5R2A105K160AA	94.84%	0.35%	116	9	1.96E-1	1.11E-3
21	X5R, 100V, 4.7 uF	TDK - C3216Y5V1H225Z/1.15	94.25%	0.35%	103	7	1.66E-1	1.63E-3
22	X5R, 250V, 1uF	TDK - C5750X5R2E105K230KA	93.44%	0.21%	90	3	1.83E-1	5.92E-4
23	X5R, 630 V, 0.22 uF	TDK - C5750X5R2J224M230KA	93.54%	0.46%	91	7	2.29E-1	7.55E-4
24	X6S, 50V, 4.7uF	TDK - C2012X6S1H475K125AC	95.58%	0.39%	137	13	7.21E-1	1.64E-3
25	X6S, 50V, 6.8uF	TDK - C3225X6S1H685M250AC	92.98%	0.40%	83	5	1.95E-1	1.11E-3
26	X6S, 450V, 2.2uF	TDK - C5750X6S2W225M250KA	98.73%	0.21%	503	98	9.65E-1	8.58E-4
27	X7R, 50V, 2.2uF	TDK - C2012X7R1H225K125AC	94.78%	0.34%	115	8	2.37E-1	8.11E-4
28	X7R, 100V, 1uF	TDK - C3216X7R2A105K160AA	94.44%	0.36%	107	8	2.79E-1	3.78E-3
29	X7R, 100V, 4.7uF	TDK - CKG45NX7R2A475M500JJ	94.52%	0.45%	109	9	1.79E-1	8.53E-4
30	X7R, 250V, 1uF	TDK - C5750X7R2E105K230KA	93.27%	0.30%	87	4	1.67E-1	3.16E-4
31	X7R, 250V, 1.2UF	Kemet - C2225C125KARACTU	93.09%	0.32%	85	4	2.56E-1	3.00E-3
32	X7R, 500V, 1uF	Knowles - 2220Y5000105KXTWS2	95.12%	0.14%	123	4	3.14E-1	6.92E-4
33	X7R 630V, 0.1 uF	AVX - 2220CC105KAZ2A	95.16%	0.46%	125	13	3.78E-1	1.69E-3
34	X7R, 630 V, 0.47 uF	TDK - CKG57NX7R2J474M500JH	93.72%	0.11%	94	2	1.85E-1	5.76E-4
35	X7R, 630V, 1uF	Knowles - 2220Y6300105KXTWS2	95.75%	0.34%	143	12	3.96E-1	1.25E-3
36	X7R, 1000V, 0.47uF	Knowles - 2220Y1K00474KXTWS2	95.14%	0.39%	124	11	3.86E-1	9.74E-4
37	X7T, 250V, 2.2uF	TDK - CGA9P3X7T2E225M250KE	97.80%	0.37%	288	54	4.55E-1	1.35E-3

APPENDIX B

MOTOR DRIVE OPERATION DATA

Table B.1: Test data from ThinGap motor using two parallel 4-level ILMs per phase.

Speed RPM	Frequency Hz	Torque Nm	Mech Power W	Vdc V	P_{dc} W	P_{ac} W	Q_{ac} VAR	$\Theta_{comdelay}$ deg
998.5	267.2	3.037	317.8	96.8	452.9	431.1	-20.92	2.21
2247	595	2.951	694.9	96.2	879.9	854.7	-34.64	4.93
3101	828.4	2.961	962.2	124.0	1174.9	1144.7	36.20	6.86
3999	1062	2.95	1215.6	148.7	1485.2	1447.8	140.64	8.79
4993	1336	2.849	1490.9	170.8	1831.9	1783.9	262.23	11.06
4990	1334	2.917	1525.7	176.5	1876.4	1827.1	319.56	11.05
5991	1599	2.853	1791.7	197.1	2233.3	2173.7	630.29	13.24

		W meter 1			W meter 2				
Speed RPM	V_{ll1} V_{RMS}	I_{l1} I_{RMS}	P_1 W	V_{ll2} V_{RMS}	I_{l2} I_{RMS}	P_2 W	Inverter η	Motor η	Total η
998.5	20.0	12.1	209.5	20.0	12.4	221.6	95.2%	73.7%	70.2%
2247	39.7	12.1	417.3	39.6	12.4	437.3	97.1%	81.3%	79.0%
3101	53.2	12.3	582.8	52.9	12.1	561.9	97.4%	84.1%	81.9%
3999	67.2	12.7	764.5	66.7	12.1	683.3	97.5%	84.0%	81.8%
4993	82.3	12.9	967.7	81.8	12.5	816.3	97.4%	83.6%	81.4%
4990	82.7	13.3	1005.8	82.2	12.8	821.3	97.4%	83.5%	81.3%
5991	97.8	13.9	1268.8	97.1	13.4	904.9	97.3%	82.4%	80.2%