MINIATURIZATION OF ON-CHIP PASSIVE ELECTRONIC DEVICES BY SILICON NITRIDE SELF-ROLLED-UP MEMBRANE MICROTUBE NANOTECHNOLOGY

BY

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DISSERTATION

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ABSTRACT

Miniaturization of the commonly used on-chip lumped elements is highly desirable to enhance the density, performance and functionality of integrated circuits (ICs) working from DC to millimeter wave frequency band. Numerous improvement methods have been demonstrated but all fail to fundamentally solve the intrinsic drawbacks of currently used planar spiral platforms for passive lumped elements. A new design platform based on self-rolled-up membrane (S-RuM) nanotechnology that "processes like 2-D and functions like 3-D" is proposed for constructing on-chip three-dimensional (3-D) rolled-up microtube structures. By taking lumped inductors and transformers, this thesis demonstrates a global solution to obtain on-chip lumped elements with an extremely small on-chip footprint and almost complete immunity to substrate issues.

The fabrication process of S-RuM lumped elements is designed to be CMOS compatible with a clear trend to achieving 100% fabrication yield. A quasi-dynamic finite element method (FEM) is established to precisely calculate the dimensions of rolled-up structures, which allows an accurate simulation of the electrical performance of S-RuM lumped passive devices by physical modeling. The design of the S-RuM inductor from FEM structural simulation to physical model electrical simulation is demonstrated, and its physical model is further integrated into the commercial Advanced Design System (ADS) software as a design kit for circuit-level simulation. Full wave FEM 3-D modeling of ICs including S-RuM inductors in the layouts is enabled by EMPro and ADS FEM co-simulation. A simple high pass filter is used as an example to show the S-RuM IC design process. A clear trend to save 38% ~ 50% chip size is also shown in active IC examples by replacing planar spiral inductors with S-RuM inductors. As a unit device, the S-RuM inductor can be used to build other passive elements like transformers. So, the S-RuM transformer is also investigated in this thesis. The thermal and mechanical reliability of the S-RuM platform

are tested by using rapid thermal annealing (RTA) and nano-indention, which provide data for further packaging S-RuM lumped passive devices and applications in a power electronics.

All samples are fabricated on a 1 to 10 Ω·cm p-type silicon substrate. Cu based S-RuM inductor samples show a 119 nH/mm^2 inductance density, Q factor of 3 @ 8 GHz, a 0.3 nH to 2.4 nH inductance range, a self-resonant-frequency (SRF) of ~20 GHz, 250 °C thermal stability, and 48.6 N/m stiffness. Au based S-RuM transformer samples shows a 1.52:1 turn ratio (n), 0.99 mutual magnetic coupling coefficient (k_m), and 0.392 maximum available gain at 8.6 GHz with a footprint (S) of only ~0.0085 mm^2. The corresponding index of transformer performance ($(n \cdot k_m)/S$) is 177, which is ~2× than that of the best on-chip planar transformer reported so far with a similar turn ratio. The performance of the S-RuM transformers is stable at temperatures up to 250 ºC, and the hardness of the rolled-up structures is as high as 270.2 N/m.

To my parents, my wife, my son
~ your love always supports me

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CHAPTER 1: INTRODUCTION

1.1 Overview

On-chip lumped elements are widely used in radio-frequency (RF), microwave, and millimeter-wave (mm-wave) integrated circuits (ICs). The size across any dimension of lump elements is much smaller than the working wavelength ($<\lambda/20$, λ is the working wavelength) to avoid appreciable phase shift between the input and output terminals. The most frequently used lumped elements include inductors, capacitors, resistors, and building devices such as filters, transformers, and baluns.

On-chip lumped elements became an integral part in microwave integrated circuits (MICs) started from 1976 due to the development of monolithic fabrication [1-4]. The primary purpose of using lumped elements to replace distributed circuit parts on-chip (e.g., microstrip line) is to obtain compact, wider bandwidth, and lower-cost active and passive RF to mm-wave ICs. However, because of smaller element dimensions and the multilevel fabrication process, lumped elements based ICs usually exhibit a lower quality factor (Q factor). For most on-chip applications, small size is of primary importance when the Q factor is acceptable. Currently monolithic IC fabrication is based on two-dimensional (2-D) processing, so commercialized lumped elements are all designed in a planar frame. Even at a frequency up to 30 GHz, those planar lumped elements are still suitable for low-cost circuit solutions. At frequencies below the C-band, the reduction of chip size could be an order of magnitude by using lumped elements instead of microstrips or coplanar waveguides (CPWs). At RF and the low end of the microwave band, the chip size reduction could be significant, and the electrical performance remains the same. Smaller chip size means an increase of the number of chips per wafer, and leads to improved visual and RF yields, and eventually lowers the chip costs drastically.

From an electrical performance point of view, using on-chip lumped elements is the best solution in many cases. One example is the use of lumped inductors as RF chokes. Compared to $\lambda/4$ line transformers, lumped inductors can provide a much wider frequency bands and compact size. Another example is in broadband applications, where lumped elements usually associate with smaller amounts of parasitic capacitance than distributed circuit components, which will result in wider bandwidth circuits. At lower RF frequencies, using microstrip, coaxial, or waveguide transmission lines for certain circuit configurations is not practical, where lumped elements can be successfully applied. The circuit configurations include direct-coupled amplifiers; true lowpass and highpass filters; differential, push-pull, and feedback amplifiers; series and shunt gain peaked broadband amplifiers; bridged T-coil amplifiers; high-voltage and phase-splitting amplifiers; Gilbert-cell mixers; and Colpitts, Pierce, Hartley, Clapp, and multivibrator-type oscillators [5].

Among on-chip lumped elements, inductors are the most important basic unit due to their much more complicated working mechanism and fabrication processing compared to that of capacitors and resistors. Inductors are also the dominant part for electrical performance in many passive devices like filters, transformers, and impedance matching networks. In order to be compatible with planar ICs fabrication processing, such as CMOS and GaAs integrated circuits, planar spiral inductors made by copper (Cu) or aluminum (Al) are the most commonly used on-chip lumped inductors in RF, microwave, and mm-wave ICs.

The electrical performance of lumped inductor is described by its inductance, Q factor, and self-resonant frequency. The definition of inductance is the ratio of the voltage to the rate of the change of current with a unit of henries (H). Inductance represents the ability of an inductor to store magnetic field energy temporarily. To consider energy loss, the Q factor is defined and can be calculated by the following equation (1.1):

$$Q = 2\pi \cdot \frac{\text{energy stored}}{\text{energy loss in one oscillation cycle}} = 2\pi \cdot \frac{\text{peak magnetic energy} - \text{peak electric energy}}{\text{energy loss in one oscillation cycle}} \quad (1.1)$$

The net magnetic energy stored in the inductor can be calculated by the difference between the peak magnetic energy and the peak electric energy, which is proportional to the value of the Q factor. Crosstalk of EM fields between nearby metal parts of the inductor causes electric energy storage in the parasitic capacitors. The Q factor is dependent on frequency and vanishes at a certain frequency, which is called the self-resonant frequency f_0. Above the self-resonant frequency f_0, it is impossible for an inductor to output net magnetic energy to the external circuit.

A typical planar rectangular spiral inductor fabricated on a silicon substrate with ten turns is shown in Figure 1.1 [6]. Inductance is achieved by utilizing self- and mutual induction of long metal wires. However, because the mutual magnetic coupling between turns is weak, to obtain greater nH inductance, more than 10,000 μm^2 area is usually required, which is a huge size compared to the footprints of other on-chip components, such as transistors, capacitors, and resistors. When a lossy (low-resistivity) substrate is used, a significant interaction between the radiated electromagnetic (EM) field and substrate introduces parasitic capacitance and eddy current to reduce the Q factor and the maximum working frequency. It can be seen from Figure 1.1 that one input or output terminal connects the inner coil by a metal line underneath the coils and through a via hole, which additionally add parasitic capacitance to further reduce electrical performance. Considering flexible substrates working at the RF band, the deformation of the

substrate will cause tuning of every aspect of inductor performance, which will be a large deviation from the designed values and becomes unacceptable at high-frequency applications.

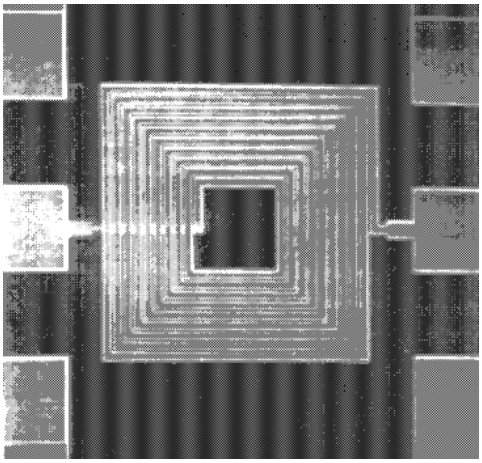


Figure 1.1 Top view of a rectangular spiral inductor fabricated on a silicon substrate with ten turns [6].

It is clear that design limitations on 2-D processing platforms is the intrinsic reason for all the above issues associated with every planar spiral inductor on chips. Over the decades, more advanced technologies and new fabrication platforms have been demonstrated to effectively reduce the parasitic effects from the substrate and, at the same time, to try to scale down the size of lumped inductors.

Based on the 2-D processing technology, many improvements have been demonstrated on planar spiral inductors to reduce the parasitic effects from the substrates and to scale down the size. All of the proposed solutions are classified into two categories: (1) suspending the spiral coils or (2) stacking coils vertically and connecting them by vias through the dielectric substrate. Major fabrication technologies used include multilayer fabrication [7], bulk micromachining [8], and surface micromachining [8-10].

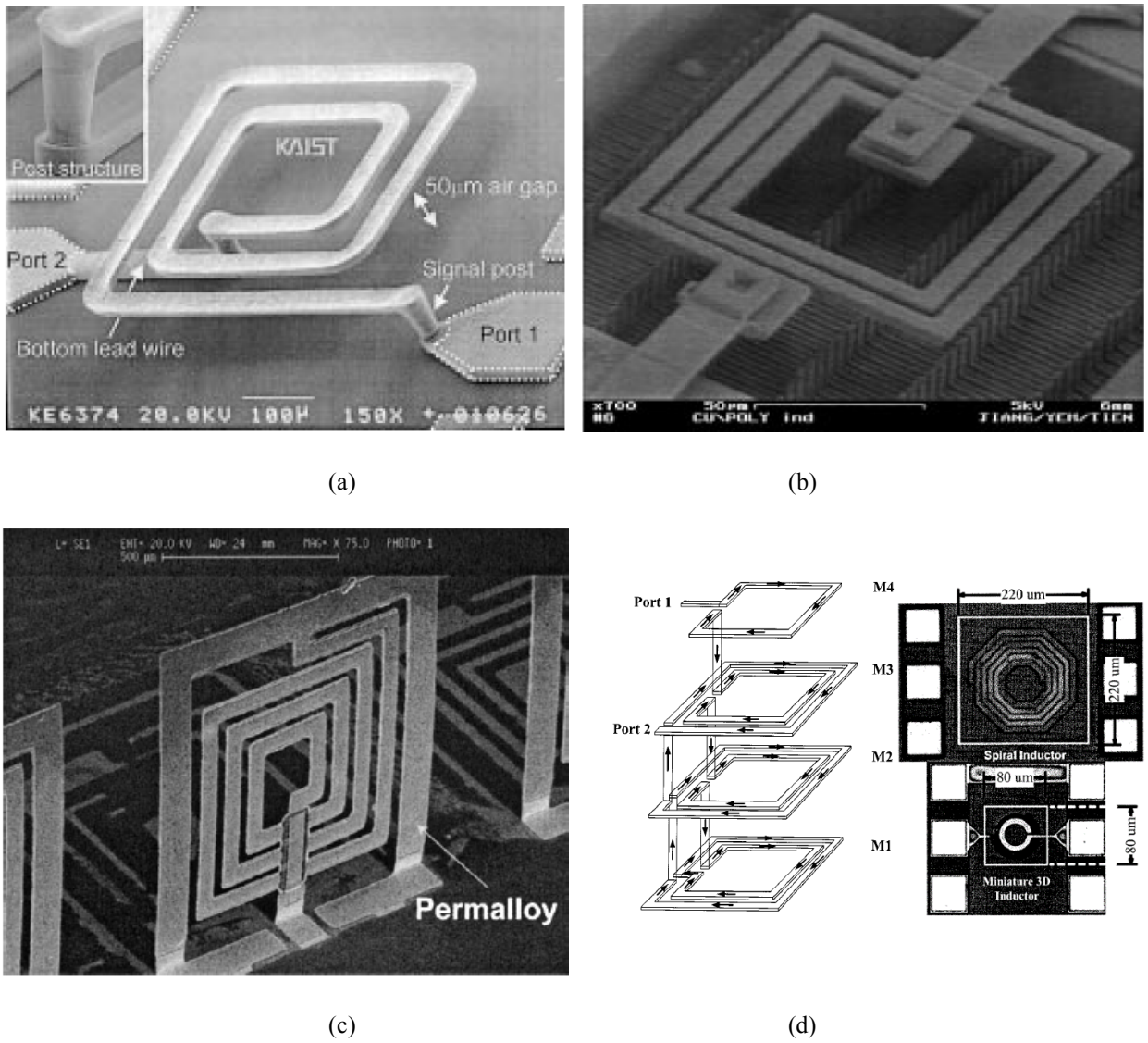


Figure 1.2 Improved planar spiral inductors. (a) Spiral wires are lifted above the substrate by surface micromachining [9]. (b) Spiral wires are lifted above the substrate, and the substrate underneath the spiral wires is etched away and Cu-lined by integration of surface and bulk micromachining [8]. (c) Spiral wires are lifted up perpendicular to the substrate by surface micromachining and external magnetic field force control [10]. (d) Miniaturized spiral inductor created by multiple layer 2-D processing, and its comparison to the size of a traditional monolayer spiral inductor [7].

Figure 1.2 shows several typical improved planar spiral inductors using technologies mentioned above. Figure 1.2 (a) shows a highly suspended spiral inductor on a standard silicon substrate (1~30 Ω·cm in resistivity) created by surface micromachining. The fabrication process is CMOS compatible. It achieved a high peak Q factor of 70 at 6 GHz with inductance of 1.38 nH

(at 1 GHz) and a self-resonant frequency of over 20 GHz. Figure 1.2 (b) shows a spiral structure of an inductor formed with polysilicon and electroless Cu plating. The inductor was suspended over a Cu-lined 30-μm-deep cavity. The fabrication process is not CMOS compatible. Figure 1.2 (c) is a vertical spiral inductor made by surface micromachining and a 3-D assembly process called plastic deformation magnetic (PDM) assembly. It is not CMOS compatible processing and complicated, but it completely eliminates the substrate effect. Figure 1.2 (d) is a miniaturized 3-D inductor fabricated by a standard digital 0.35-μm one-poly-four-metal (1P4M) CMOS process. It successfully reduces the size and cost but still suffers from substrate issues. It is clear that all these improvements are able to address certain problems of the traditional planar spiral inductors. However, they are still in the 2-D design framework, which means the trade-off between the size and overall inductor electrical performance always exists due to essential problems of the 2-D structures. The design of lumped inductor, or lumped elements, must to go 3-D coils in a more effective and CMOS compatible way.

1.2 Self-rolled-up Membrane (S-RuM) Nanotechnology

Self-rolled-up membrane (S-RuM) nanotechnology is a nanoscale fabrication method to make micro- and nanotubes by the strain-induced effect. It forms 3-D structures from the 2-D planar thin film growth and the structural design. The S-RuM system contains two functional parts – the strained membrane and the sacrificial layer. As an example, the strained membrane normally consisting of an oppositely strained bilayer is deposited on top of a sacrificial layer. Upon releasing the sacrificial layer, a rolling torque force from each of the bilayers is generated to drive the bilayer membrane to scroll up and continue to roll into a tubular spiral structure.

The first strain-induced self-rolled-up membrane microtubes were demonstrated by Prinz et al. in 2000 [11]. Because self-rolled-up nanotechnology can realize 3-D tubular structures at nano

to microscale, it quickly attracted great attention in many academic laboratories. The very first microtube contained a strained InAs/GaAs epitaxial thin film bilayer as the rolling vehicle by using molecular beam epitaxy (MBE). Since then, a variety of microtubes were obtained from different kinds of material, like semiconductors [11, 12], dielectrics [13-15], polymers [16], and metals [17]. Theoretically, if a rolling force can be established, any type of thin film material can be rolled up, as demonstrated in the above literature. General speaking, the material system for the strained layer includes amorphous films, epitaxial single-crystal films, strained polymer bilayers, or hybrid material systems. The rolling force can be formed between multilayers with different stresses or from just a single layer with a stress gradient inside the film. The thin film deposition technology is therefore versatile, depending on which type of material is needed. Practical methods include plasma enhanced chemical vapor deposition (PECVD), metal-organic chemical vapor deposition (MOCVD), and molecular beam epitaxy (MBE). So far, microtubes have been successfully implemented in many practical applications, like electromagnetic fields (metamaterials) [18], super capacitors [19], optical resonators [20], biological sensors [15], III-V quantum dot microtube lasers [21], and others.

Other than as microtube super capacitors, the self-rolled-up membrane (S-RuM) microtube platform is also very useful for the design and fabrication of other lumped elements. This thesis systematically studied every aspect of the implementation of the S-RuM platform for on-chip lumped elements: rolled-up structure design and fabrication (Chapter 2); the most important S-RuM lumped passive devices, inductor design, and fabrication (Chapter 3); S-RuM device design and fabrication, using a transformer as an example (Chapter 4); S-RuM platform reliability (Chapter 5); and the back-to-front S-RuM integrated circuit simulation platforms (Chapter 6).

CHAPTER 2: CMOS COMPATIBLE SELF-ROLLED-UP MEMBRANE MICROTUBE PLATFORM

2.1 S-RuM Platform Design and Fabrication Process

To be practically used in RF to mm-wave ICs, the proposed S-RuM platform must meet industrial standard requirements, including COMS technology compatibility, high fabrication yield, and good performance tolerance. As the performance of lumped elements totally depends on its physical structure, the design of the rolling vehicle is the key to success.

The proposed S-RuM platform is based on the SiN_x bilayer system. the SiN_x thin film is a CMOS technology compatible material, and it is often used as a passivation layer for transistors. The fabrication of SiN_x thin films is inexpensive and can be conveniently done by a dual-frequency plasma enhance chemical vapor deposition (PECVD) system in an ammonia (NH_3)/silane (SiH_4)/nitrogen (N_2) environment. When the SiN_x thin film is deposited under high frequency (HF) (13.56 MHz), a tensile residual stress is built inside the film. However, if the deposition frequency changes to low frequency (LF) (380 kHz), films deposited are naturally compressively strained. Other than deposition frequency, input power, gas flow rate, and other factors can be tuned to adjust the in-film residual stress of both HF SiN_x and LF SiN_x thin films. In the SiN_x thin films, there exist N-H, Si-H, and Si-N bonds at the same time. The type and the value of residual stress is determined by the content of the bonded hydrogen (combination of NH_x and SiH) [22]. The more the content of the bonded hydrogen the larger the tensile stress and the smaller the compressive stress. For the SiN_x platforms for on-chip lumped elements, it is expected to have a maximum rolling force, so the stress mismatch between the LF SiN_x and the HF SiN_x is optimized to reach a maximum value in our PECVD system. The residual stress in the films was measured using a FSM 500TC metrology tool to be −1168 and 406.95 MPa for the LF and HF SiN_x film,

respectively. Different from bulk silicon nitride, PECVD SiN_x thin film contains a high amount of amine fragments, which results in a Young's modulus of ~180 GPa and ~170 GPa for LF SiN_x and HF SiN_x thin films, respectively [23].

Pinholes in the SiN_x thin films are formed during PECVD growth. It is an intrinsic problem and associated with the residual stress after growth. The S-RuM platform for lumped elements application requires a rolling pattern with edge length from hundreds of micrometers to millimeters, which inevitably includes many pinholes in the rolling pattern. Pinholes introduce unwanted etching of the sacrificial layer and therefore put the rolling process out of control, which drastically reduces the fabrication yield.

On-chip lumped elements are made by conductive materials such as copper (Cu) or aluminum (Al), which are easily to be oxidized in a redox agent. For the S-RuM platform proposed in this thesis, germanium (Ge) is used as the sacrificial layer, so hydrogen peroxide (H_2O_2) is the solution to use for wet etching of the Ge thin film. Since H_2O_2 is a strong redox agent, when using Cu or Al as the conductive material, special consideration must be taken in the design.

The optimized structure design is shown in Figure 2.1. In all the experiments in this thesis, high resistivity p-type silicon (p-Si, 10 to 20 Ω·cm) is used as the substrate. SiO_2 with 1 μm thickness is grown as the electrical isolation layer. A rectangular mesa is defined by optical lithography and reactive ion etching (RIE) after the sacrificial layer (20 nm Ge) and bilayer SiN_x (20 nm LF SiN_x/20 nm HF SiN_x) are all deposited. The conductive strip is a bilayer structure: 5 nm Ni/Cu or Al with desired thickness. For specific applications, the conductive strip could be patterned to have different shapes. Ni thin film is used as the adhesion layer as well as protection layer for Cu oxidation. Atomic layer deposition (ALD) Al_2O_3 thin film covers the entire mesa, which functions as the cover layer to assure directionally rolling, to solve the pinhole issue, and to

protect Cu or Al from oxidation. By opening a window on one side of the mesa, the Ge sacrificial layer is continuously etched by H_2O_2 to trigger the self-rolling process.

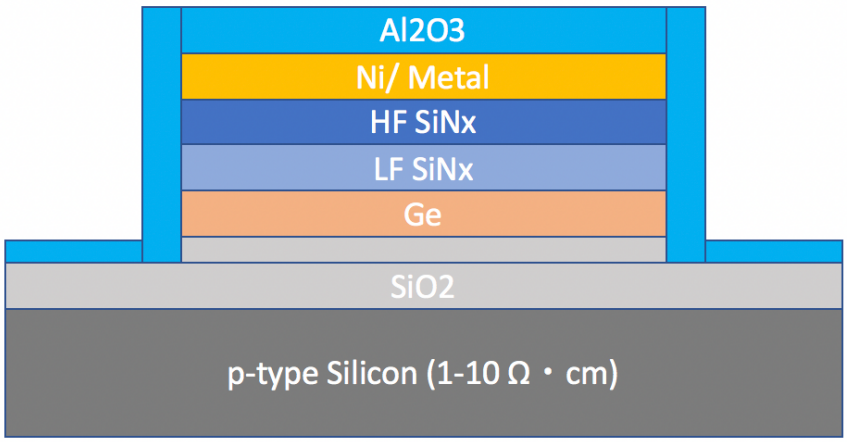


Figure 2.1 Structure design of the S-RuM platform for on-chip lumped elements.

2.2 Precision Structural Engineering by FEM Modeling

The key geometrical parameter determining the final dimension is the diameter of the innermost tube. For high frequency electronics and optics, it is crucial to precisely control the inner diameter because the electrical performance of those devices is very sensitive to geometric shapes. Several analytical and numerical methods have been developed to quantitatively predict the inner diameter of rolled-up microtubes from the macroscopic level down to the nanoscale level. The first analytical model was proposed in 1925 to estimate the curvature of a bimetallic thermostat deflection [24]. It is useful for the calculation of the bending curvature of strained bilayer nanoscale thin films [25, 26]. For the numerical method, the deformation of a bilayer structure is able to be estimated by the finite element method (FEM) under static conditions [27]. However, all those methods are only suitable for the simple geometries normally found with bilayer structures with uniform cross sections. For structures containing more than two sublayers and with the top strained layer patterned for certain functions, it is impossible to use traditional methods to determine the

inner diameter of the rolled-up structure (especially analytical methods). In this case, the numerical method is preferred with its ability to understand the kinetics involved in the rolling process dynamic simulations.

Figure 2.2 shows a transient quasi-static FEM modeling method for the rolling process of multilayer membrane structures. For convenient illustration, the bilayer S-RuM platform is used as an example here. In practice, the Ge sacrificial layer is used to hold the top strained bilayer steady before being released. Therefore, a fixed boundary condition is applied to all nodes at the bottom of the LF SiN_x thin film to model this effect. Because the proposed FEM method is in an elastic region but modeled with geometric nonlinearities due to large deformation, so all the materials are assumed to be isotropic and linear elastic. According to Mindlin-Reissner shell theory, shell elements can be used to model a multiple-layer structure with governed accuracy. According to the structure's design, different layer thickness and material properties can be assigned to corresponding layers. For the S-RuM lumped element platform, the Young's modulus *E* for both PECVD LF SiN_x and HF SiN_x thin films is set to be 210 GPa according to the literature [28-30]. The Poisson coefficient is set to be 0.28 for the bilayers. For both LF SiN_x and HF SiN_x thin films, their residual stresses are modeled by thermal expansion coefficients in FEM. For temperature increment, all the nodes in the simulation have the same setup value. To model the compressive and tensile stresses, different coefficients of thermal expansion are assigned to different layers. The values of compressive and tensile stresses are measured by a FSM 500TC metrology tool. The exact value of stresses can be determined by applying a proper temperature increment. The thermal coefficient of LF SiN_x is taken from the literature; therefore its temperature increment of LF SiN_x is then determined to be 1450 °C to achieve the measured value. When the temperature increment is fixed at 1450 °C, the thermal coefficients of other materials can be then determined to reach

their respective measured residual stress. For HF SiN_x thin film, its determined thermal coefficient value is approximately -9.61×10^{-7}, and for commonly used metal thin films in the proposed S-RuM platform, nickel (Ni) has the thermal coefficient value of approximately -1.9×10^{-6} and gold (Au) has the thermal coefficient value of approximately -1.85×10^{-6}.

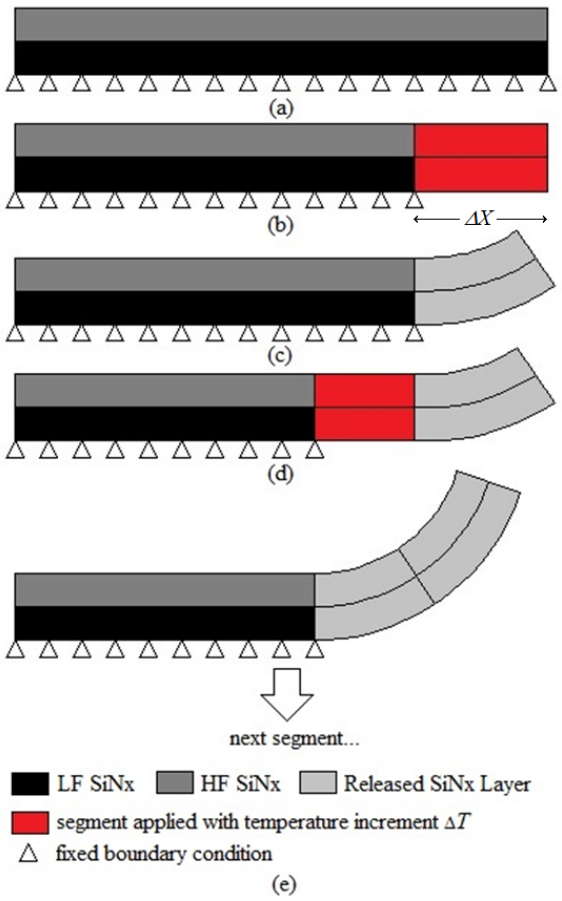


Figure 2.2 Transient quasi-static FEM modeling of the rolling process of bilayer membranes. (a) Applied fixed boundary condition to all element nodes for initial stage. (b) Unfix the first segment and apply a temperature increment ΔT to it. (c) Update the structure after static simulation. (d) Unfix the next segment and apply a temperature increment ΔT. (e) After static simulation, update the structure, and return to the first step to continue the simulation until the last segment is simulated. Reprinted (adapted) with permission from (W. Huang, S. Koric, X. Yu, K. J. Hsia, and X. Li, "Precision structural engineering of self-rolled-up 3D nanomembranes guided by transient quasi-static FEM modeling," *Nano Letters*, vol. 14, no. 11, pp. 6293 - 6297, 2014). Copyright (2014) American Chemical Society.

To model the dynamic etching progress of the sacrificial layer, a moving boundary condition is used. The rolling process is a nonlinear large deformation transient quasi-dynamic process, and it is modeled by a series of FEM simulations of static deformation by releasing the constraints on the bottom segments in sequence. In simulations, the length of each segment is set to be less than 1/200 of the estimated circumference of the first turn. A simulation loop as shown in Figure 2.2 is implemented as the moving boundary condition. The simulation loop starts by applying a fixed boundary condition at the bottom of the bilayer as shown in Figure 2.2(a). In Figure 2.2(b), the constraint on the first segment ΔX is released, and all the nodes in the released part are given a temperature increment ΔT = 1450 °C. Then, an updated geometry is obtained as shown in Figure 2.2(c) after static simulation is performed. By repeating the first three steps, the next segment is released and the same temperature increment is applied to obtain the next updated geometry as shown in Figure 2.2 (d). The simulation ends once the last segment is released.

The FEM modeling allows a precisely controlled the number of turns of the S-RuM devices. When the inner diameter is determined, the number of turns can be tuned by predetermining the length of the layered structures. Figure 2.3 shows the scanning electron microscopy (SEM) images of the computationally designed SiN_x bilayer that is rolled-up with $\frac{1}{4}$, $\frac{1}{2}$, $\frac{3}{4}$, or a full-turn with a 101 μm inner diameter. The high accuracy of the proposed FEM method can be found by looking at the seamless full-turn tube structure.

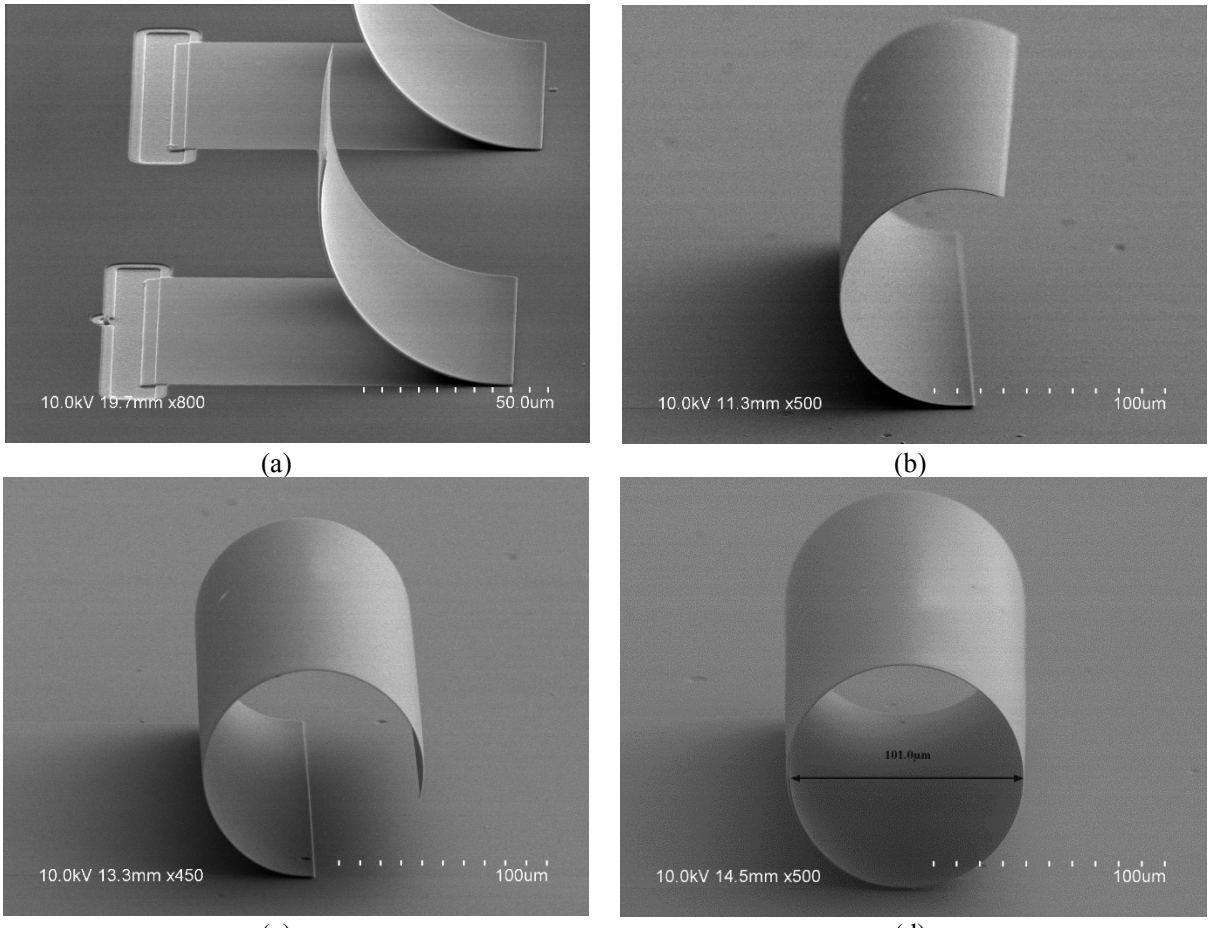


Figure 2.3 SEM pictures of precisely fabricated 101 μm inner diameter self-rolled-up SiN_x bilayer structures with designed fraction of turns. (a) A quarter turn. (b) A half turn. (c) Three-quarters turn. (d) Full turn with inner diameter measured and labeled. Reprinted (adapted) with permission from (W. Huang, S. Koric, X. Yu, K. J. Hsia, and X. Li, "Precision structural engineering of self-rolled-up 3D nanomembranes guided by transient quasi-static FEM modeling," *Nano Letters*, vol. 14, no. 11, pp. 6293 - 6297, 2014). Copyright (2014) American Chemical Society.

CHAPTER 3: S-RuM INDUCTORS

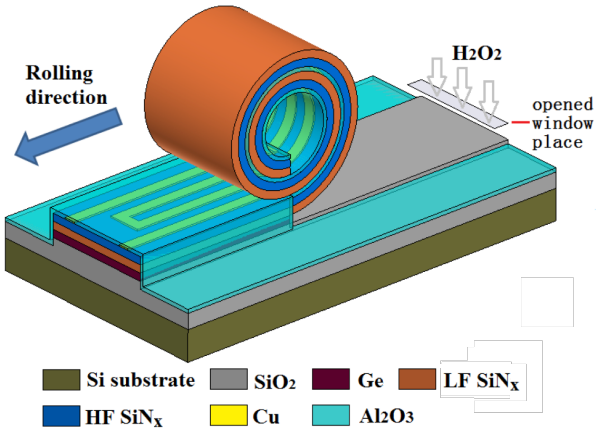
3.1 Design of S-RuM Inductor Structure

On the S-RuM platform, 3-D coils can be easily formed as shown in Figure 3.1. The structural design of the S-RuM platform ensures the 3-D coil is a tightly rolled-up 3-D spiral structure. Figure 3.1(a) is a schematic view of the S-RuM inductor in the rolling process, and the metal layer is patterned to be several strips connected in series with connection lines; afterwards, it can be rolled up with the other strained layers to form 3-D metal spiral coils. To ensure directional rolling towards the contact pads, a window is opened at one edge of the mesa indicated in the figure. Figure 3.1(b) shows an SEM image of a 6-cell S-RuM inductor with RF contact pads in the rolling process.

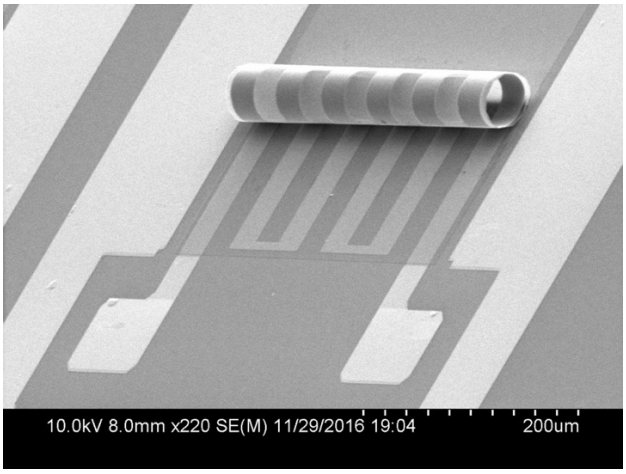
The inner diameter of the 3-D coils is determined by the material's mechanical property and the side-wall thickness of each layer, and it can be precisely determined by FEM modeling. Considering the packaging requirements, the height (outer diameter) is controlled according to different application requirements. The typical value of the inner diameter is 3 ~ 100 μm, and the wall thickness of a single turn is usually 30 ~ 700 nm. Because the wall thickness of each single turn is negligible compared to the inner diameter, all the metal spirals are strongly coupled to each other when an RF signal is applied. The induction of the electromotive force can be expected to be much more efficient in the microtube structure compared to the 2-D spiral structure. Furthermore, there is a little overlap between the metal spirals and the substrate, so the capacitive coupling and eddy current due to magnetic coupling are very small on any kind of substrate.

For the demonstration of CMOS compatibility, a thermally evaporated Cu thin film with thickness ~100 nm is chosen as the conductive material on top of the 5 nm Ni adhesion and oxidation protection layer. The tested resistivity of Cu thin film is only ~1.63× larger than that of

bulk Cu. Subsequently, an Al_2O_3 thin film was deposited over the entire mesa by atomic layer deposition (ALD), which multi-functions as a cover layer to assure directional rolling, to solve the pinhole issue, and to protect Cu from oxidation.



(a)



(b)

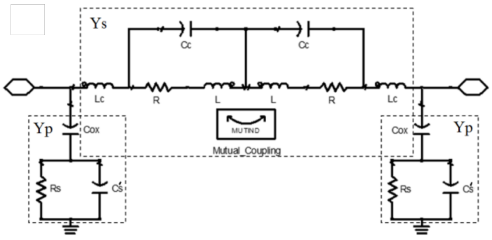
Figure 3.1 Design of the S-RuM inductor. (a) Schematic illustration of the Cu-based S-RuM inductor design with the 2-D planar pattern and 3-D rolled-up air core structure shown with all materials and rolling direction labeled. (b) SEM image of the Cu S-RuM inductor sample in the rolling process with RF contact pads.

3.2 Physical Equivalent Circuit Model

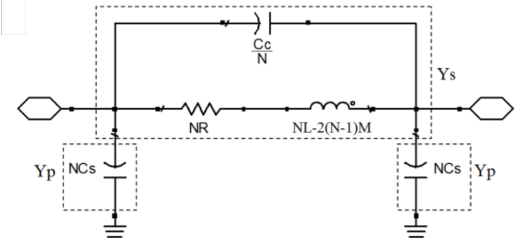
A compact, accurate physical model is desired for on-chip inductor design insights and optimization. The difficulty of modeling is to identify the relevant parasitic effects. The most

successful approach is to use a lumped circuit elements network to represent the complexity of high-frequency phenomena such as substrate effects and crosstalk between interconnects. Figure 3.2(a) shows the lumped circuit physical model for two adjacent spirals. The model considers the cancellation mutual inductance M between them due to their opposite current flow directions. Lumped capacitor C_c models the strong EM interference between turns, and lumped element L models the self-inductance of a spiral. The metal layer in the microtube inductor is just ~100 nm thick, which is much smaller than the skin depth at working frequency even up to 40 GHz. Therefore, the eddy current effect can be ignored and the resistance R of one spiral becomes frequency independent. Lumped elements R_c and L_c model the resistance and inductance effects of a single connection line.

Propagation of the EM waves in substrate could be a skin effect mode, surface wave mode, or quasi-TEM mode depending on the doping level of the substrate from high to low. The EM wave propagation can be modeled by a network constructed by lumped elements C_s' and R_s, as shown in the dotted box in Figure 3.2(a).



(a)



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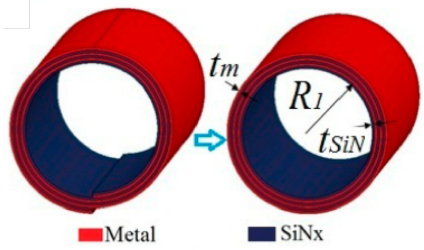

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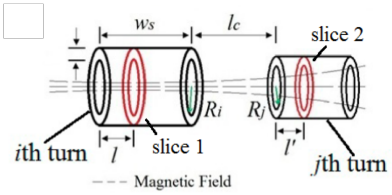


(d)

Figure 3.2 Lumped circuit physical model for microtube inductor. (a) Model for two adjacent cells. (b) Model for entire microtube inductor by ignoring the connection line inductance effect and substrate loss. (c) Concentric cylinders approximation structure. (d) Mutual induction between two cylinders separated by distance l_c. Reprinted (adapted) with permission from (W. Huang, X. Yu, P. Froeter, R. Xu, P. Ferreira and X. Li, "On-chip inductors with self-rolled-up SiN_x Nanomembrane tubes: A novel design platform for extreme miniaturization," *Nano Letters*, vol. 12, no. 12, pp. 6283 - 6288, 2012). Copyright (2012) American Chemical Society.

R_s models the substrate loss and can be calculated by the equation $R_s = 2/sG_{sub}$. C_{ox} models the capacitive effect between the bottoms of the outmost metal spiral and the doped substrate. C_s' and C_{ox} are calculated by $C_s' = sC_{sub}/2$ and $C_{ox} = s \cdot \varepsilon_{ox}/(2t_{ox})$, where s is the effective overlapping area of the outmost spiral with the substrate, G_{sub} and C_{sub} are the conductance and capacitance per unit area for the doped substrate. G_{sub} and C_{sub} are functions of the substrate dielectric constant and the doping level. In the fabricated microtube inductor, all the cells are the same, so the physical model for the entire structure can be built as shown in Figure 3.2(b) by ignoring the connection line inductance L_c and substrate loss R_s.

As shown in Figure 3.2(c), concentric cylinders are used to approximately model the electrical behavior of spirals because the radius change of each turn is negligible. If the mutual inductance M_{ij} of two cylinders separated with distance l_c as shown in Figure 3.2(d) is known, the self-inductance of a cell can then be calculated by $L = \sum_{i=1}^{N_t} \sum_{j=1}^{N_t} M_{ij,l_c=w_s}$ and the cancellation mutual inductance of adjacent cells can then be calculated by $M = \sum_{i=1}^{N_t} \sum_{j=1}^{N_t} M_{ij,l_c>0}$, where N_t is the number of turns. The magnetic flux density B is assumed to be uniform in slice 2 and its value equals to that at its center point O. The magnetic flux density B' generated by slice 1, if considering its thickness t, can be calculated by equation (3.1).

$$B'(l, l') = \int_R^{R+t} \frac{\mu_0 \rho^2 I}{2w_s t[\rho^2 + (l_c + w_s + l' - l)^2]^{3/2}} d\rho \tag{3.1}$$

The total magnetic flux density B generated by cylinder i passing through slice 2 can then be calculated by the following integral.

$$B(l') = \int_0^{w_s} B'(l, l')dl \tag{3.2}$$

Considering the length of cylinder *j*, the mutual inductance M_{ij} can be calculated by the equation

$$M_{ij} = \int_0^{w_s} \frac{B'(l, l')\pi R^2}{w_s I} dl' = \frac{\pi \mu_0 R_i^2}{4t{w_s}^2} \cdot D_{ej} \tag{3.3}$$

where

$$\begin{aligned} D_{ej} = {} & (l_c + 2w_s)^2 ln\left(\frac{R_j + t + \sqrt{\left(R_j + t\right)^2 + (l_c + 2w_s)^2}}{R_j + \sqrt{R_j^2 + (l_c + 2w_s)^2}}\right) \\ & - 2(l_c + w_s)^2 ln\left(\frac{R_j + t + \sqrt{\left(R_j + t\right)^2 + (l_c + w_s)^2}}{R_j + \sqrt{R_j^2 + (l_c + w_s)^2}}\right) \\ & + l_c^2 ln\left(\frac{R_j + t + \sqrt{\left(R_j + t\right)^2 + l_c^2}}{R_j + \sqrt{R_j^2 + l_c^2}}\right) \\ & + \left(R_j + t\right)\sqrt{\left(R_j + t\right)^2 + (l_c + 2w_s)^2} - R_j\sqrt{R_j^2 + (l_c + 2w_s)^2} \\ & - 2\left(R_j + t\right)\sqrt{\left(R_j + t\right)^2 + (l_c + w_s)^2} + 2R_j\sqrt{R_j^2 + (l_c + 2w_s)^2} \end{aligned} \tag{3.4}$$

with $R_i = R_1 + (i-1)\,\Delta R$, $i = 1,2,3\ldots$, $R_j = R_1 + (j-1)\,\Delta R$, $j = 1,2,3\ldots$.

Figure 3.2(a) shows the lumped equivalent circuit of any two adjacent spiral cells in the microtube inductor. Assuming all the cells are the same, the lumped equivalent circuit of the

microtube inductor is shown in Figure 3.3(b), which is a two-port π-type admittance network as shown within the dotted boxes. By ignoring the inductance L_c (when $l_s >> l_c$), the admittance matrix of the network is derived as

$$Y = \begin{bmatrix} Y_P + Y_S & -Y_S \\ -Y_S & Y_P + Y_S \end{bmatrix} \tag{3.5}$$

where

$$Y_P = j\omega N\left(C_c + C_p\right) \tag{3.6}$$

$$Y_S = \frac{1}{N} \cdot \frac{R}{R^2 + \omega^2 (L')^2} + \frac{1}{N} \cdot j\omega \left[C - \frac{L'}{R^2 + \omega^2 (L')^2} \right] \tag{3.7}$$

N is the number of spiral cells, $L' = L - 2(1 - N^{-1})M$. Matrix Y can be obtained from the de-embedded S parameters of the feed lines. The total effective inductance L_{etotal}, Q factor Q_{total} and the resonant frequency can then be derived from the matrix Y as shown in (3.8), (3.9), and (3.10).

$$L_{etotal} = \frac{Im\left(-\frac{1}{Y_{12}}\right)}{\omega} = \frac{Im\left(\frac{1}{Y_S}\right)}{\omega} = \frac{N\{L' - C[R^2 + \omega^2 (L')^2]\}}{1 + \omega^2 C^2 [R^2 + \omega^2 (L')^2] - 2\omega^2 C L'} \tag{3.8}$$

$$Q_{total} = \left|\frac{Im(Y_{11})}{Re(Y_{11})}\right| = \left|\frac{Im(Y_P + Y_S)}{Re(Y_P + Y_S)}\right| = \frac{\omega\left|L' - \left[C + N^2\left(C_c + C_p\right)\right]\left[R^2 + \omega^2(L')^2\right]\right|}{R} \tag{3.9}$$

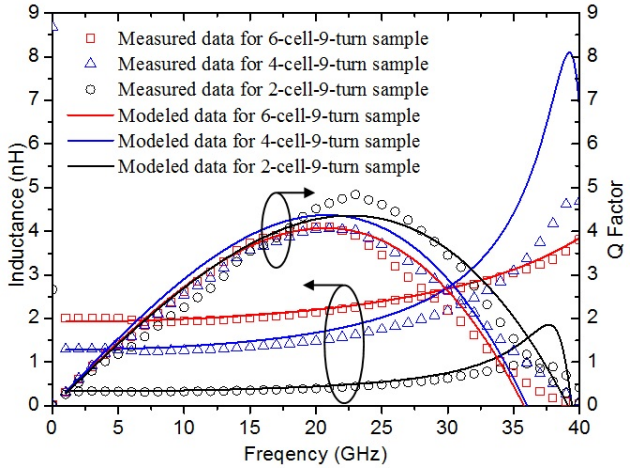
$$f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{(C_c + N_c^2 C_s)L'} - \frac{R^2}{(L')^2}} \tag{3.10}$$

Because the spacing between each turn is very small (t_{SiN} < 60 nm), the adjacent turns are not equipotential when the inductor is under high frequency operation. Therefore, the crosstalk capacitance *C* cannot be ignored. The value of *C* is similar to that of a coaxial capacitor whose capacitance can be calculated by equation (3.11).

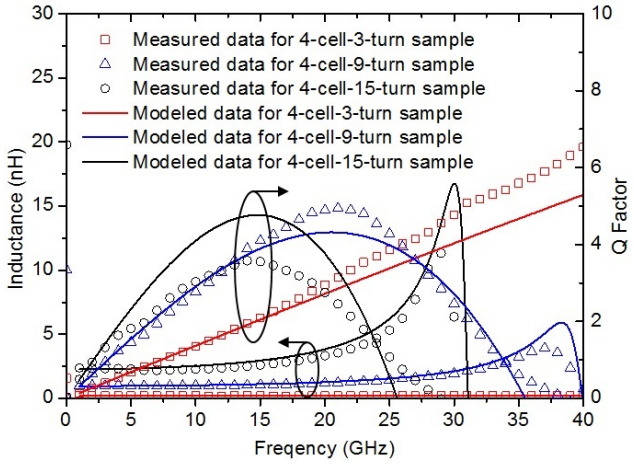
$$C = \left\{\sum_{i=2}^{N_t} \frac{ln\left[1 + \frac{\Delta R(i-1)}{R_1}\right]}{2\pi\varepsilon_{SiN} w_s}\right\}^{-1} \approx \frac{2\pi\varepsilon_{SiN} w_s}{ln\left[1 + \frac{\Delta R(N_t - 1)}{R_1}\right]} \tag{3.11}$$

To demonstrate the accuracy of the model, in Figure 3.3(a) and 3.3(b), the measured effective inductances and Q factors versus frequency from 0.01 GHz to 40 GHz are plotted and compared to modeled data. Au S-RuM inductors with 9 turns but with different numbers of cells, or 4 cells but different number of turns, are fabricated on a 40 ~ 60 Ω·cm p-type silicon substrate. Good agreement between the measured and modeled data can be found, which indicates the high accuracy and reliability of the physical model. Even with large resistance due to the narrow cross section of metal layers, the maximum values of the Q factor of all samples are acceptable in a practical RFIC design. A 100 nm thick gold thin film can make the surface of the metal strip very

smooth so as to obtain a resistivity just 2× times larger than its bulk value. Both skin effect and proximity effect can be negligible because the thickness of the gold layer is less than its skin depth, even at 40 GHz. So, the resistance of the tube inductor can be then considered as a constant value in the whole working frequency range, and the Q factor is therefore totally determined by the resistivity of the conduction layer.



(a)



(b)

Figure 3.3 Comparison between the experimental and modeled data for various geometries. (a) 9-turn Au S-RuM inductors with different numbers of cells. (b) 4-cell Au S-RuM inductors with different numbers of turns. The metal thickness is 100 nm for Au/5 nm Ni with 30 μm strip width.

3.3 Fabrication Results of Cu S-RuM Inductor Samples

Several types of Cu-based S-RuM inductor samples with different numbers of turns and cells were successfully fabricated. All samples have 2 or 3 turns but different numbers of cells: 2, 4, or 6 cells with 20 μm cell separation distance. The width of the conduction strip of all samples is designed to be 20 μm, 30 μm, and 40 μm. The SEM images of the 2-turns rolled-up S-RuM inductors with a 30 μm wide strip are shown in Figures 3.4(a) to 3.4(d). The optical photos of the 3-turns rolled-up S-RuM inductors with different width strips are shown in Figures 3.4(e) to 3.4(g). The 3-turn-2-cell S-RuM inductor has supporting bars. The inner diameter of all samples is ~60.8 μm, as shown in Figure 3.4(h). By defining the on-wafer footprint as the projection area on the substrate after being rolled-up, the 2-cell-3-turn Cu S-RuM inductor only occupies 80 × 60 μm^2. It can be noticed that the side wall thickness compared to the tube inner diameter (ID) of ~60.8 μm is negligible and the rolling is tight from turn to turn. Even rolling more and more all the way to 50 turns, which superlinearly increases the inductance, the total sidewall thickness will still be less than 15% of ID, and so has little increment on the footprint.

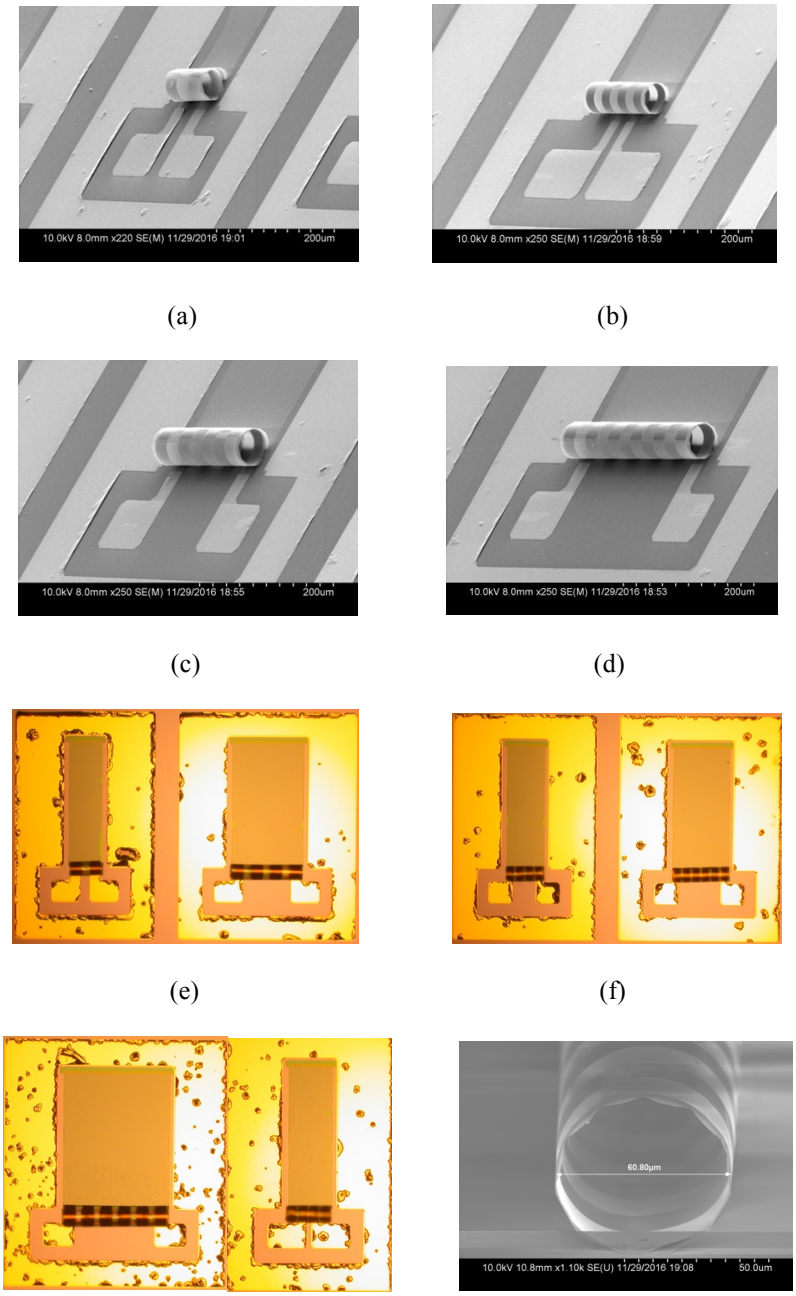
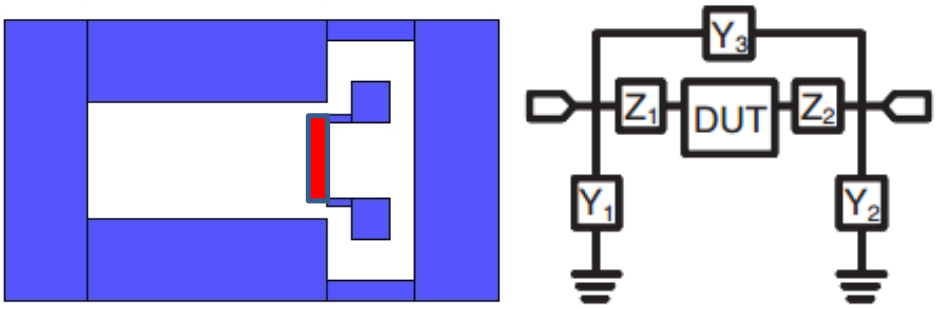


Figure 3.4 SEM and optical photos of Cu S-RuM inductor samples. (a) A 2-cell-2-turn sample without supporting bars. (b) A 2-cell-2-turn sample with supporting bars. (c) A 4-cell-2-turn sample. (d) A 6-cell-2-turn sample. (e) 2-cell-3-turn sample and 4-cell-3-turn sample with 40 µm wide strip. (f) 4-cell-3-turn sample and 6-cell-3-turn sample with 20 µm wide strip. (g) 2-cell-3-turn sample with supporting bars and 6-cell-3-turn sample with 30 µm wide strip. (h) Cross-section with measured inner diameter labeled.

3.4 Measurement and Characterization Method

Two port S-parameters are measured by using the Agilent PNA8363C purpose network analyzer with Cascade Microtech air coplanar ground-signal-ground probes in the frequency range from 10 MHz to 40 GHz. To do the RF measurement of the tube inductor, a test fixture is designed as shown in Figure 3.5. Parasitic effects introduced by feedlines need to be removed to obtain the real performance of the device under test (DUT). An open-through de-embedding technique is used here to calibrate the feedline effects. The lumped equivalent circuit model is constructed to represent the physics of parasitic effects. As the RF measurement goes up to 40 GHz, feedlines are designed as short as possible to minimize the distribution effect. Open-through de-embedding patterns are shown in Figure 3.5. As shown in Figure 3.5(a), an admittance Π-network is used to model the capacitive effects between the contact pads and the surrounding environment including the substrate and RF ground. A series connected impedance network is used to model the resistance and inductance of the feedlines. Figure 3.5(a) to 3.5(c) show schematic views of patterns with the DUT, without the DUT (open case) and with being grounded. Corresponding lumped equivalent circuits are constructed to model the RF performance of each pattern. The narrow branches of feedlines are bent 90° to avoid using additional lines to connect the two feedlines.



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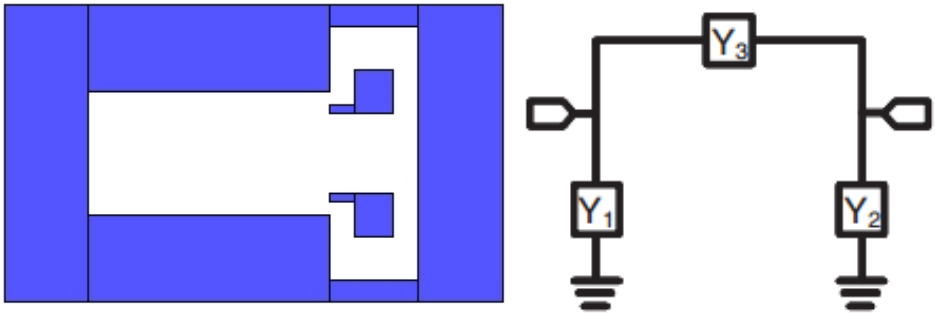

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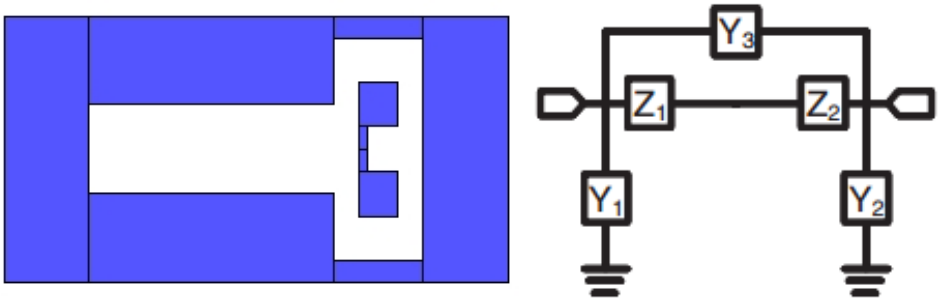


(c)

Figure 3.5 Open-through de-embedding patterns and their corresponding lumped equivalent circuits. (a) Test pattern with DUT. (b) Open pattern. (c) Grounded pattern.

The mathematical procedure to do the open-through de-embedding is shown in Figure 3.6. Figure 3.6 shows the first step which abstracts the admittance Π-network (open pattern) from the original data. The result still contains the parasitic resistances and inductances (Z1 and Z2) whose

total effect can be calculated by doing step 2 shown in Figure 3.6. Finally, the real performance of the DUT can be obtained by doing step 3.

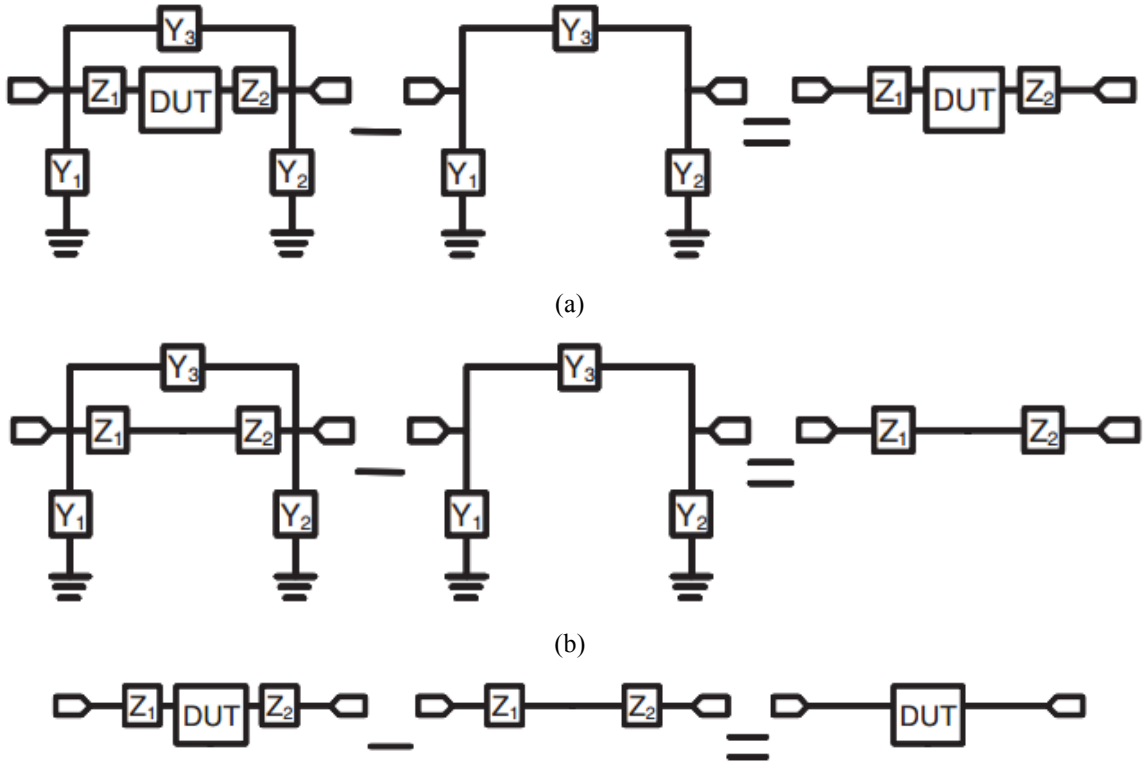


Figure 3.6 Mathematical procedure to do the open-through de-embedding. (a). Subtract measured data of the open pattern from raw data with DUT. (b). Subtract measured data of the open pattern from data of through pattern. (c). Subtract data obtained from step 2 from data of from step 1.

3.5 Tested RF Performance of Cu S-RuM Inductor Samples

RF performances are extracted based on a lumped single-π equivalent circuit model for the S-RuM inductor [31]. In Figure 3.7(a), for samples with 30 μm strip width and the same number of turns, the inductance shows linear increase with increase of the number of cells. For just a 2-turn coil, every 2-cell unit adds ~0.3 nH inductance. Adding cells means connecting more coils along the tube axis in series, which doesn't affect the self-resonant-frequency (SRF). Compared to

the Au based S-RuM inductor, the ID increases ~6× [32]. A larger ID, because of additional cover layer to prevent Cu oxidation, leads to lower SRF due to larger crosstalk capacitance and substrate parasitic capacitance, but allows better magnetic flux passage, and subsequently makes a bigger volume for integrating a larger magnetic core. The SRF of 2-turn samples is 18 GHz ~ 20 GHz due to fabrication variations. At 5 GHz, the 6-cell-2-turn sample has inductance of ~1nH with Q factor of ~1.8. Compared to a 6-cell-9-turn Au S-RuM inductor with inductance of ~1.6nH and Q factor of ~1.9, the Cu S-RuM inductor has almost half the inductance but a similar Q factor, implying a significant Q factor enhancement. The resistivity of the thermally evaporated Cu thin film is ~2.74e^{-8} Ω·cm, which is ~1.63× of its bulk value and an ~44% reduction compared to the Au thin film in the first Au S-RuM inductor. Although the Cu S-RuM inductor just has 2 turns, the inductance density has reached as high as 61 nH/mm^2.

Figure 3.7(b) shows the inductance and Q factor variation by tuning the conduction strip width of the 6-cell-2-turn sample. It shows that inductance slightly increases at low frequency when strip width goes narrower as expected, while the Q factor is increased with increasing Cu strip width below 7.5 GHz, because of the decrease of resistance with the wider strip. However, a significant drop of self-resonance frequency (SRF) is observed with wider strip width, presumably due to the significant increase of inter-turn crosstalk and the substrate parasitic capacitances. The maximum Q factor is achieved at ~2.4 @ 10 GHz for the sample with 30 μm strip width design. The highest SRF of 1 nH samples is ~23GHz with 20 μm strip width design. Therefore, the width cannot be too narrow or too wide; it must be optimized to balance the SRF and ohmic loss.

Figure 3.7(c) shows when the number of turns of the 2-cell sample increase to 3 turns, the inductance increases from 0.3 nH to 0.8 nH, which again demonstrates the superlinear relationship between the number of turns and the inductance. The SRF only drops a little from 16 GHz to 13.8

GHz even if the inductance increases ~2.67×. This is because the cross capacitance between turns decreases when there are more turns per cell. The inductance density therefore reaches as high as 162.7 nH/mm^2. It can be expected that the inductance could be the highest ever achieved on-chip due to the superlinear characteristic.

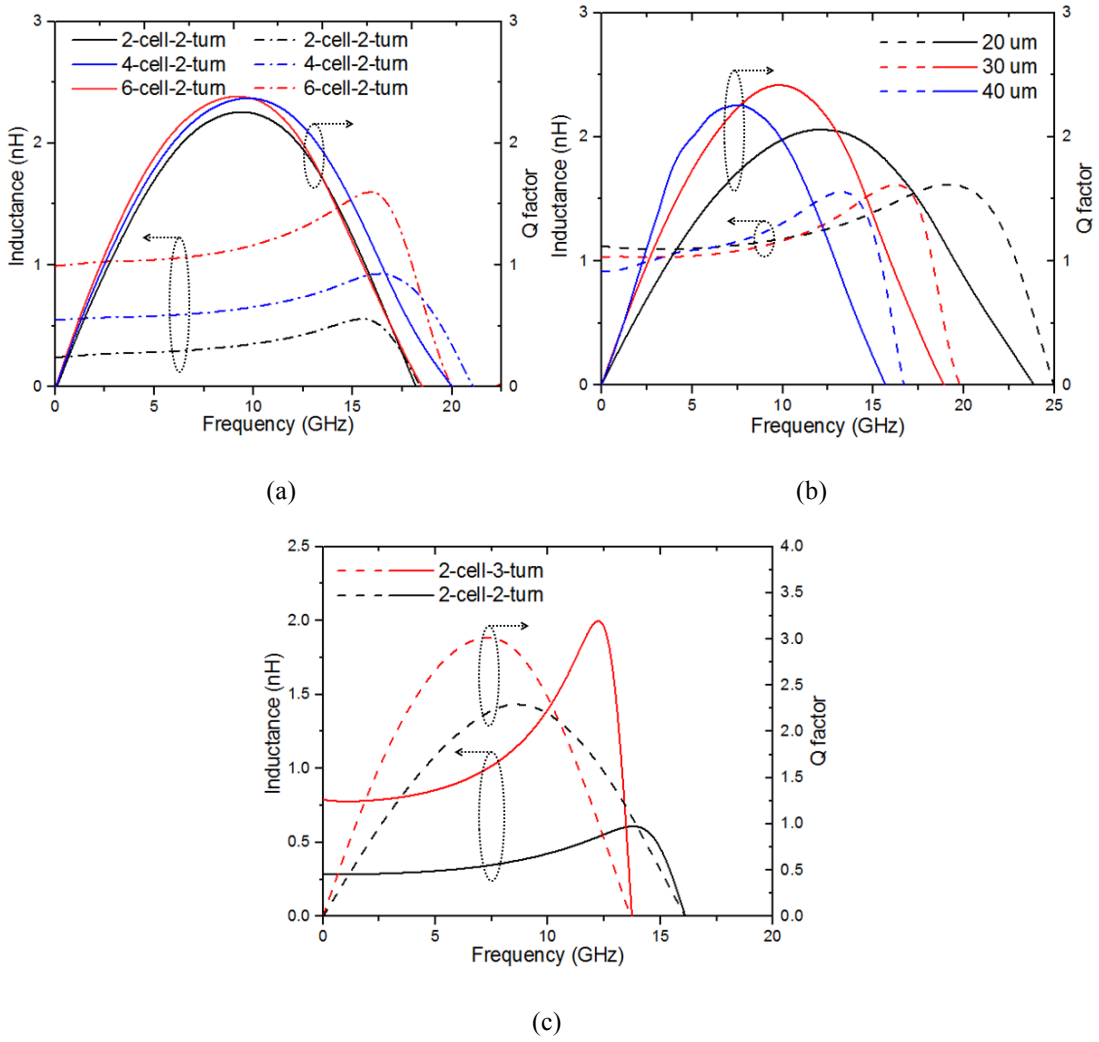


Figure 3.7 Tested RF performance of 2-turn Cu S-RuM inductors. (a) Extracted inductances (solid lines) and Q factors (dot-dash lines) vs. frequency for 30 μm strip width 2-turn samples with 2 cells, 4 cells, and 6 cells. (b) Extracted inductance and Q factor of 6-cell-2-turn Cu S-RuM inductors with different conduction strip widths.

3.6 Performance Reliability of Cu S-RuM Inductor Samples

Unlike traditional on-chip lumped elements, S-RuM lumped elements are designed and fabricated on a 3-D hollow spiral structure. Considering the electrical performance of passive electronics is determined by structural shape and dimension, study of the thermal and mechanical stability of SiN_x S-RuM microtube structures is critical to know the performance reliability of S-RuM lumped elements.

3.6.1 Thermal Stability of S-RuM Microtube Structure

As mentioned in Charter 2, PECVD SiN_x thin film could have different densities from 2 to 2.5 g/cm^3 and refractive indices from 1.8 to 2.35, depending on the deposition parameters such as pressure, gas flow ratio and rate, substrate temperature, and RF power and frequency. The stress built inside the film is directly related to the density and refractive index [33]. The deposition temperature on the platen is at 300 °C and on the shower head is 240 °C. And, according to the overall reaction for SiN_x films deposited using an $NH_3/SiH_4/N_2$ plasma shown below [23],

$$SiH_4 + 4NH_3(g) \xrightarrow{\text{Plasma}} Si(NH_2)_4(s) + 4H_2\,(g), \text{ at 80-300 °C} \tag{3.12}$$

$$3Si(NH_2)_4(s) \xrightarrow{\text{Anneal}} Si_3N_4(s) + 8NH_3(g) \text{ at } T \geq \text{deposition } T \tag{3.13}$$

it is possible that the film thickness, geometry, and diameter could be drastically altered at temperatures >300 °C, or have noticeable change at temperatures >240 °C. This thermal effect could happen when S-RuM lumped elements are in harsh environments or S-RuM lumped elements are developed for power applications. Rapid thermal annealing (RTA) is used to test the microtube thermal stability. The Cu S-RuM inductor is used as an example and is annealed at the

temperatures 250 °C and 350 °C for 5 mins in an N_2 environment, and then is used to test the RF performance of the samples.

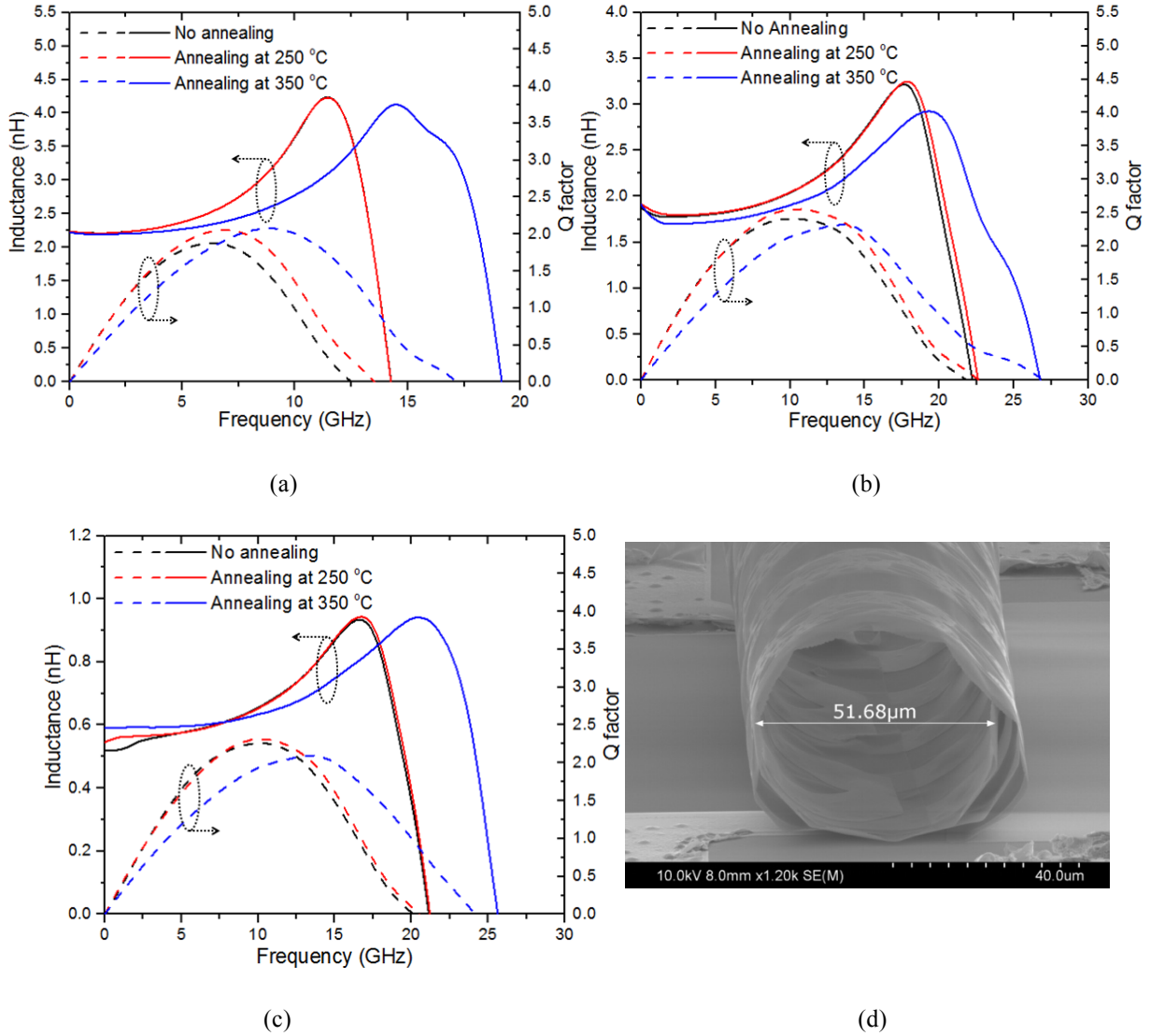


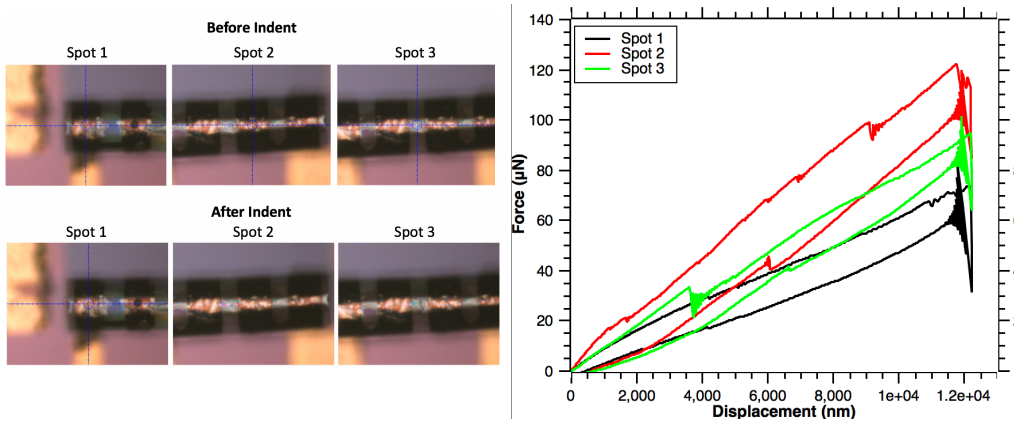
Figure 3.8 Thermal stability of the Cu S-RuM inductor at different RTA conditions. (a) Comparison of inductance and Q factor vs. frequency of 6-cell-3-turn with strip width 40 μm before annealing, after annealing at 250 °C and 350 °C. (b) Comparison of inductance and Q factor vs. frequency of 4-cell-3-turn with strip width 20 μm before annealing, after annealing at 250 °C and 350 °C. (c) Comparison of inductance and Q factor vs. frequency of 4-cell-2-turn with strip width 40 μm before annealing, after annealing at 250 °C and 350 °C. (d) SEM picture of a 6-cell-3-turn Cu S-RuM inductor after 350 °C annealing with inner diameter measured and labeled.

Figures 3.8(a) to 3.8(c) compare the inductance and Q factor of Cu S-RuM inductors with different numbers of cells and turns before and after RTA at 250 °C and 350 °C. It can be found that, independent of number of cells and turns, the electrical performance of Cu S-RuM inductors has almost no change after RTA at 250 °C, but has a significant change after RTA at 350 °C. Figure 3.8(d) is an SEM image of a 6-cell-3-turn Cu S-RuM inductor sample after 350 °C annealing with its inner diameter measured and labeled. The SiN_x membrane had a drastic stress change at 350 °C, and its inner diameter therefore becomes smaller. Compared to the original inner diameter of ~60.8 μm before RTA at 350 °C, it shrinks to 51.68 μm, which is 15% smaller. The turns are no longer rolled up tightly, and there is an air gap of several micrometers between turns. The cross-coupling capacitance is then reduced to increase the SRF even if there is almost no change of inductance. The case for the Q factor is a little complicated. By comparing the SRF of samples before RTA at 250 °C and after RTA, the SRF increases a little bit and leads to a small increment of the Q factor. However, if RTA is at 350 °C, the Q factor drops significantly before reaches its maximum value even with a higher SRF. It must be noticed that the RF test is done at room temperature after RTA, which means there is an irreversible decrease of Cu conductivity during the annealing process at 350 °C. For traditional passive electronics, the metal conductivity decreases at high temperatures because the molecular vibrations increase to obstruct the flow of electrons. The drop of the metal's conductivity is reversible if the metal's morphology is not permanently damaged. For the S-RuM inductor samples, the conductive material is made by Cu thin films. The surface morphology and deposition uniformity of Cu thin film determines its conductivity. During RTA at 350 °C, the stress change induced membrane deformation applies a strong mechanical impact on the Cu thin film, and therefore damages its surface morphology

(becomes rougher) and uniformity (introduces fracture, stretch, etc.). The change is irreversible, so the conductivity is permanently decrease to lower the Q factor.

3.6.2 Mechanical Stability of S-RuM Microtube Structure

By investigating the Cu S-RuM inductor's stiffness at various points along the device, a better understanding of critical failure points can be achieved and potential alleviation can be planned. The tests were performed using a Hysitron TI 950 TriboIndenter with a 65.3° Berkovich tip under load-partial unload conditions. A triangular pulse waveform with peak force of 150 μN and loading rate of 75 μN/s was used over 2 seconds to almost deform the microtube. Under examination, a 4-cell-2-turn Cu S-RuM inductor with strip width 30 μm after RTA at 350 °C was subjected to a maximum indentation of 12 μm and 150 μN at several spots along the microtube axis as shown in Figure 3.9(a).



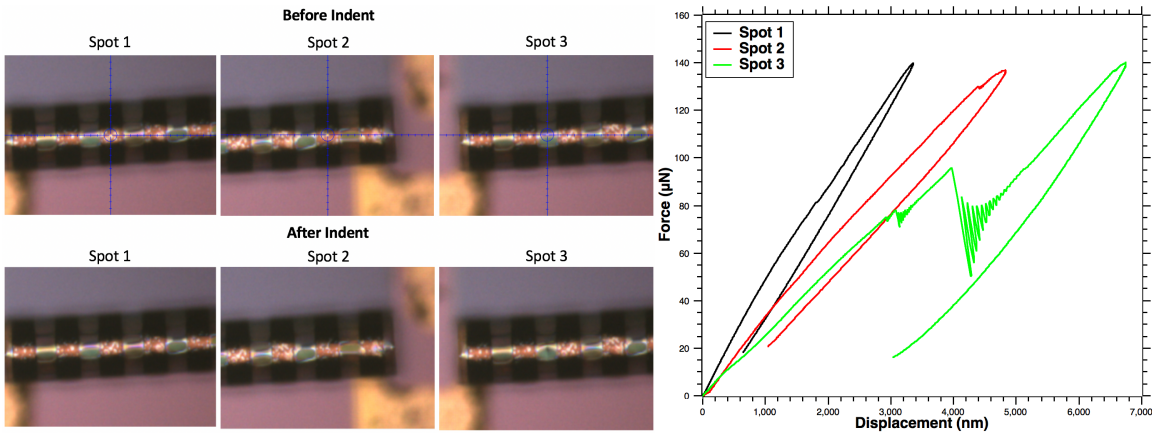
(a) (b)

Figure 3.9 Mechanical stability test of the 4-cell-2-turn Cu S-RuM inductor with strip width 30 μm. (a) Optical photos for the top views at different spots along the axis of the 4-cell-2-turn Cu S-RuM inductor before and after nano-indention. Spot 1 is on top of the edge coil. Spot 2 is on top of the middle coil. Spot 3 is on top of the SiN_x membrane. (b) Displacement vs. force curves at different spots.

The load vs. the displacement characteristics are compared for the spot on top of the edge coil, the spot on top of the middle coil, and the spot on top of the SiN_x membrane. It can be seen from Figure 3.9(b) that the structure at different spots under testing experienced continuous fracturing during the indention. Before the first fracture point, the structure at different spots was in the elastic deformation region. Stiffness at different spots can then be calculated in the elastic region, which are 8.71 N/m, 14.9 N/m, and 9.2 N/m, respectively. The mass of the 4-cell-2-turn Cu S-RuM inductor is ~4.89136×10^{-11} kg; therefore the force that could cause the top surface of the 4-cell-2-turn Cu S-RuM inductor to crack are 35, 881.7 g, 65, 087.7 g, and 69, 260 g, where g is the gravitation acceleration, or 9.8 m/s^2. Compared to a suspended MEMS high Q factor spiral inductor with X-beams, which has maximum stiffness of ~0.56 N/m at its inner turn and is claimed to have an enhancement of maximum mechanical strength more than 4500 times better than its counterparts [34], the maximum stiffness of the 4-cell-2-turn Cu S-RuM inductor is 26.6 times larger.

Another test is on a 6-cell-3-turn Cu S-RuM inductor sample. A triangular pulse waveform with peak force of 150 μN and loading rate of 75 μN/s was used over 2 seconds to almost deform the microtube. Under examination, the 6-cell-3-turn Cu S-RuM inductor with 20 μm after RTA at 350 °C was subjected to a maximum indentation of 7 μm and 150 μN at several spots along the microtube axis as shown in Figure 3.10(a). The load vs. the displacement characteristics of the 6-cell-3-turn Cu S-RuM inductor sample are compared for the spot on top of the middle coil, the spot on top of coil close to the edge, and the spot on top of the SiN_x membrane. It can be seen from Figure 3.10(b) that the structure at different spots under testing experienced several continuous fractures during the indention. Before the first fracture point, the structure at different spots was in elastic deformation region. Stiffness at different spots can be then calculated in the elastic region,

which are 48.6 N/m, 33.3 N/m, and 25.2 N/m, respectively. The mass of 4-cell-2-turn Cu S-RuM inductor is ~7.21202×10^{-11} kg, therefore the forces that could cause the top surface of the 6-cell-3-turn Cu S-RuM inductor to fracture are 116, 727 g, 183, 933 g, and 106, 115 g, where g is the gravitation acceleration, or 9.8 m/s^2. Compared to the maximum stiffness of the 4-cell-2-turn Cu S-RuM inductor, the maximum stiffness of the 6-cell-3-turn Cu S-RuM inductor is 3.26 times larger. It is clear that the mechanical strength of the Cu S-RuM inductor depends on its structural parameters, and will become larger when there are more turns. This test was done on samples after RTA at 350 °C, at which temperature the microtube structure already became loose. Structures with tightly rolled-up turns will have much larger mechanical strength (stiffness).



(a) (b)

Figure 3.10 Mechanical stability test of the 6-cell-3-turn Cu S-RuM inductor. (a) Optical photos for the top views at different spots along the axis of the 6-cell-3-turn Cu S-RuM inductor before and after nano-indention. Spot 1 is on top of the middle coil. Spot 2 is on top of the coil close to the edge. Spot 3 is on top of the SiN_x membrane. (b) Displacement vs. force curves at different spots.

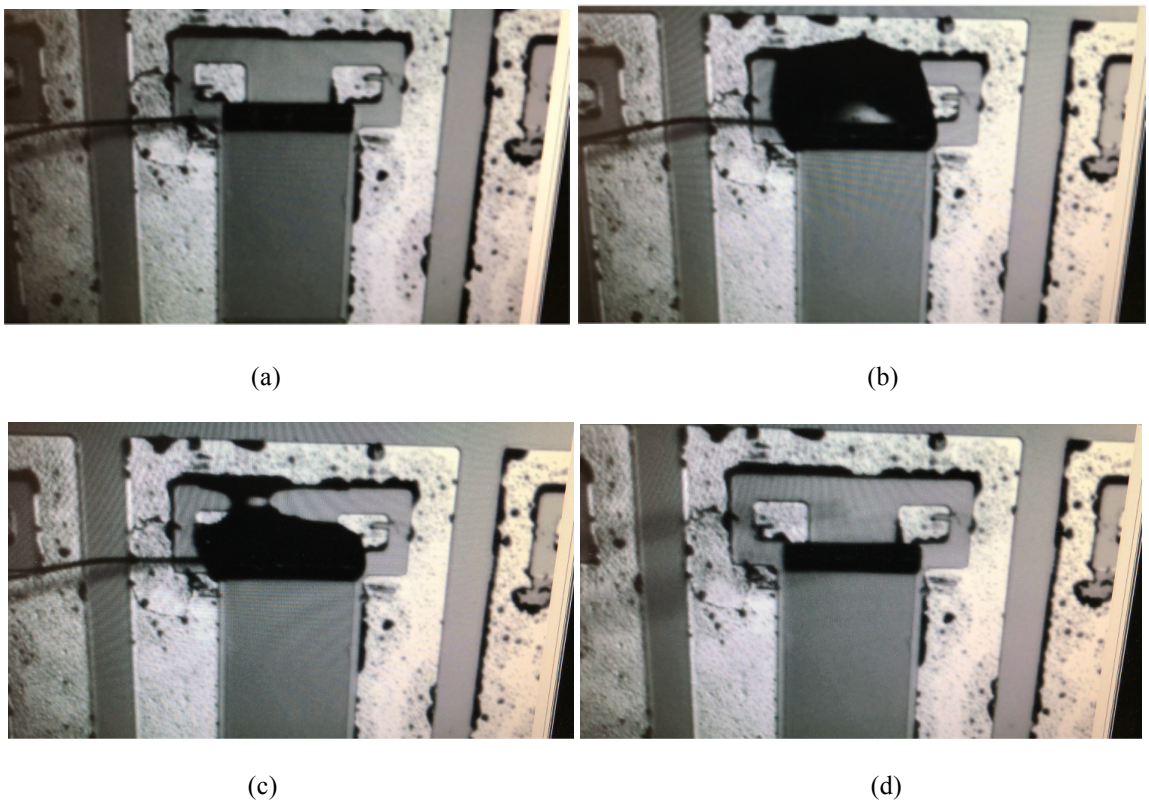
3.7 Magnetic Core Filling Technology for S-RuM Inductor

All Cu S-RuM inductor samples are air-core structures for the RF/microwave applications. The demonstrated samples so far are adequate for ultra-compact and low power circuits and

systems. Compared to the state-of-art planar spiral inductors with a few micrometers of Cu, it is impossible for the S-RuM platform to integrate Cu with the same thickness. Unless integration with higher conductivity 2-D material is completely achieved on the S-RuM platform, filling the air-core with magnetic material is the practical way to cross the Q factor bar and make S-RuM lumped elements suitable for all applications. Because the side wall thickness of the S-RuM platform is very small compared to the inner diameter, so the air-core volume ratio could be as high as 59.2% to 97.6% of the total device volume when it has 2 to 100 turns with 180 nm thick single turn side walls. Filling the core with high permeability magnetic material with sufficient switching frequency and low core loss could have significant enhancement of the electrical performance of the S-RuM inductors.

A practical method to deliver magnetic material into the air-core at nanoscale is the key for success. A preliminary demonstration is to utilize the capillary force of deionized (DI) water and do nano-manipulated injection by using a nano-needle. For high frequency operation, iron oxide (Fe_3O_4) nano-powder is mixed into DI water with a mass ratio of powder to DI water of ~1:2. The ferrite composite is then further mixed using a vortex mixer and quickly draw into the nano-needle, so that it contains a considerable ratio of ferrite while maintaining a reasonable DI water surface tension that can generate a large enough capillary force. Figure 3.11 show the process where the ferrite composite is automatically sucked into the air-core driven by the capillary force. In Figure 3.11(a), the nano-needle is placed towards one end of the Cu S-RuM 4-cell-3-turn sample and ready to inject ferrite composite. Figures 3.11(b) and 3.11(c) show how the ferrite composite is splashed around the sample and in the process of being sucked into the air-core by capillary force. Figure 3.11(d) shows the final state where ferrite composite is totally filled into the air-core. The

same process is repeated for several times to make sure as much ferrite composite as possible is packed into the air-core.



(a) (b)

(c) (d)

Figure 3.11 Ferrite composite filled into the air-core of a 4-cell-3-turn Cu S-RuM inductor by nano-manipulated injection by using a nano-needle. (a) Nano-needle is placed towards one end of the Cu S-RuM 4-cell-3-turn sample and ready to inject ferrite composite. (b) Ferrite composite is splashed around the sample. (c) Ferrite composite is in the process of being sucked into the air-core by capillary force. (d) The final state where ferrite composite is totally filled into the air-core.

After ferrite composite is filled into the air-core, the sample is dried in air for 48 hours. By observation with the naked eye, there is no shape change. An RF test is then taken on the sample from 10 MHz to 1 GHz, and the comparison of inductance test results before core filling and after core filling is shown in Figure 3.12. The inductance after core filling is significantly improved by ~14.2% from 1.55 nH to 1.77 nH. The resistance is unchanged, so the Q factor is linearly increased.

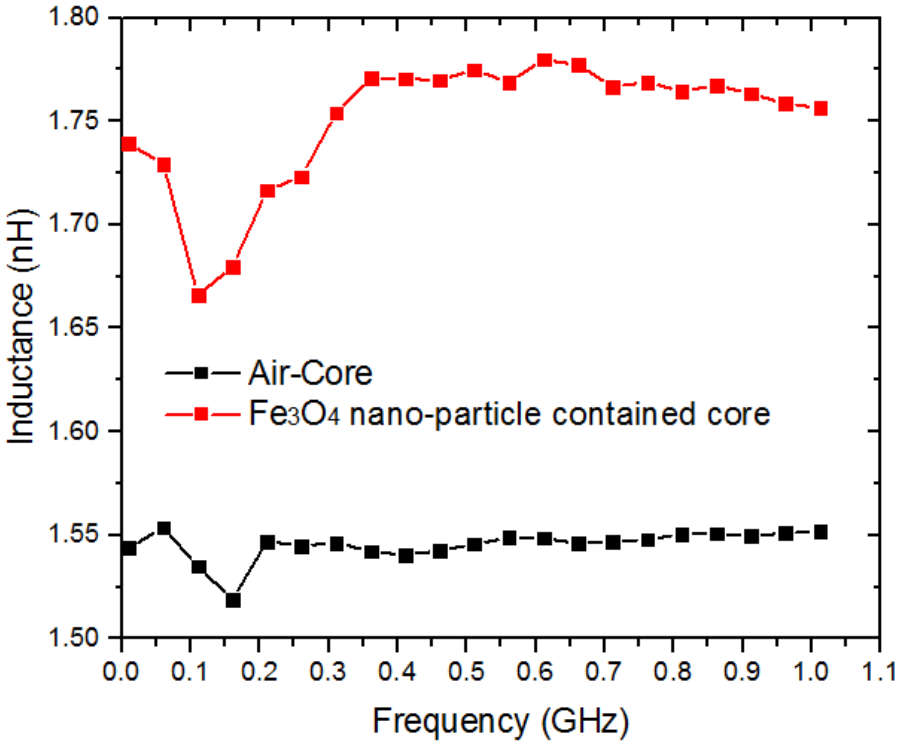


Figure 3.12 Comparison of inductance test results before core filling and after core filling.

CHAPTER 4: S-RuM TRANSFORMER

The explosive growth in the commercial Internet of Things (IoT) and the next generation (5G) wireless communication markets has generated tremendous interest in compact and inexpensive radio-frequency integrated circuits (RFICs). All major components in a narrowband front-end RFIC system need transformers to perform numerous functions, including voltage transformation, signal coupling, and impedance matching [35-38]. Current RFICs are implemented in the standard CMOS technologies to achieve low cost solutions. So, on-chip transformers are realized based on planar spiral coils which have weak mutual magnetic coupling and serious substrate parasitic effects. Therefore, current on-chip planar spiral transformers usually have a large footprint (high cost), narrow frequency range, and difficulty in achieving large turn ratios without serious magnetic coupling coefficient degrading. To solve the problem, many technologies are proposed to construct three-dimensional (3-D) high density coils to replace traditional planar spiral coils, such as implementing multiple layers for the primary and secondary coils or using an automatic wire bonding fabrication technology in conjunction with traditional MEMS processing [36, 39-41]. These approaches did improve the electrical performance by realizing relatively high coil density, but still suffered from the drawbacks of 2-D design frameworks or complicated fabrication.

4.1 Design of S-RuM Transformer and Fabrication Process

Strain-induced self-rolled-up membrane (S-RuM) nanotechnology is well developed recently and provides a new platform for the design of on-chip passive components. A tubular structure can be self-assembled from strained 2-D bilayer nanomembranes. By pre-patterning conductive layers deposited on top of the bilayer nanomembrane, complex, three-dimensional (3-D) architectures can be obtained. A well-designed architecture could have perfect electrical performance like the microtube inductor, which successfully solves the high density coil issue at the micro-scale. This

is extremely important for the design of on-chip transformers since the construction of a transformer is the combination of two or more on-chip inductors. The microtube platform liberates the CMOS compatible design of the on-chip inductor from a 2-D structure to a 3-D tubular structure. In addition to the convenience of obtaining high density coils, the elevated microtube platform naturally offers the advantage that the electromagnetic field that the microtube coil radiated has little interaction with the substrate below.

The fabrication process flow of the S-RuM transformer is shown in Figure 4.1. A 1 μm thick SiO_2 layer is formed by thermal oxidation for electrical isolation on a p-Si substrate with resistivity of 1 ~ 10 Ω·cm. A 20 nm germanium (Ge) sacrificial layer, a 20 nm low frequency (LF) SiN_x layer, and a 20 nm high frequency (HF) SiN_x layer are deposited in sequence, and then by dry etching to form a mesa. The primary and secondary coils are patterned at the same time on top of the HF SiN_x layer. To ensure directional rolling, a 25 nm ALD Al_2O_3 thin film layer is used as the cover layer to protect the sacrificial layer from unwanted wet etching due to pinhole issues of the SiN_x bilayer. Upon release of the Ge sacrificial layer, the red planar strips roll up to form the primary coil while the yellow planar strips become the secondary coil.

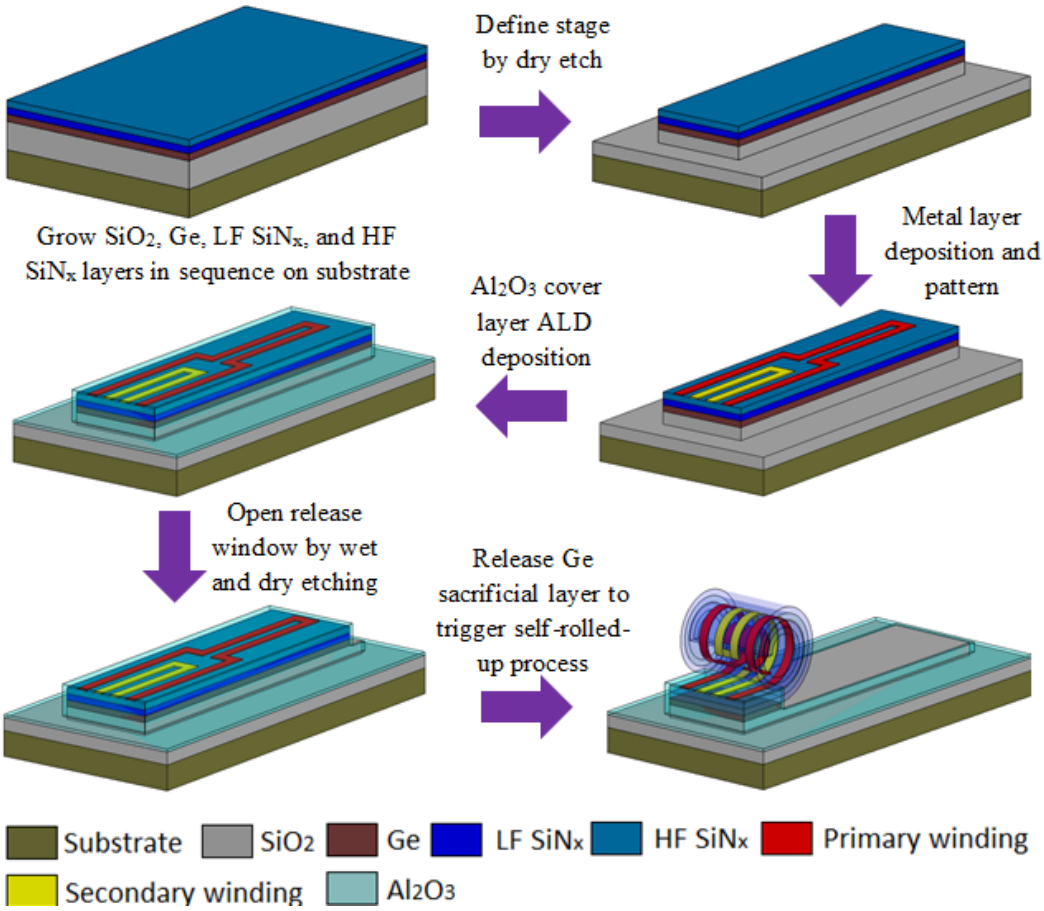


Figure 4.1 Schematic illustration of the 3-D S-RuM transformer fabrication process flow.

To better understand the working mechanism of the S-RuM transformer, an exaggerated structural view with the important parasitic parameters labeled is shown in Figure 4.2. The primary coil contains two side coils and at least two center coils, and the inductance of the primary coil is the sum of the self-inductance of the side coils and center coils and the mutual inductance between them. All the side coils and center primary coils are magnetically coupled to the secondary coil, but have different inter-turn cross-coupling capacitances (C_{cs}) and (C_{cp}). The inter-coil cross-coupling capacitance (C_{cps}) is determined by the overlap area and distance between the center primary coil and the secondary coil. The rolled-up coils interacting with the doped substrate forms parasitic capacitance across the oxide layer (C_{oxp} and C_{oxs}). The electromagnetic field penetrating

into the substrate introduces substrate parasitic capacitance (C_s) and eddy current loss modeled by resistance Rs. In fact, the S-RuM transformer is almost immune to substrate effects because it is elevated above the substrate.

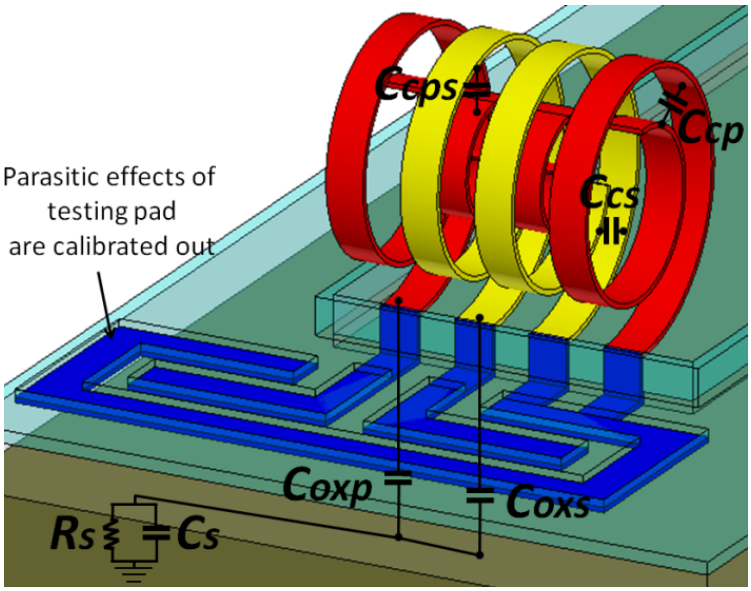
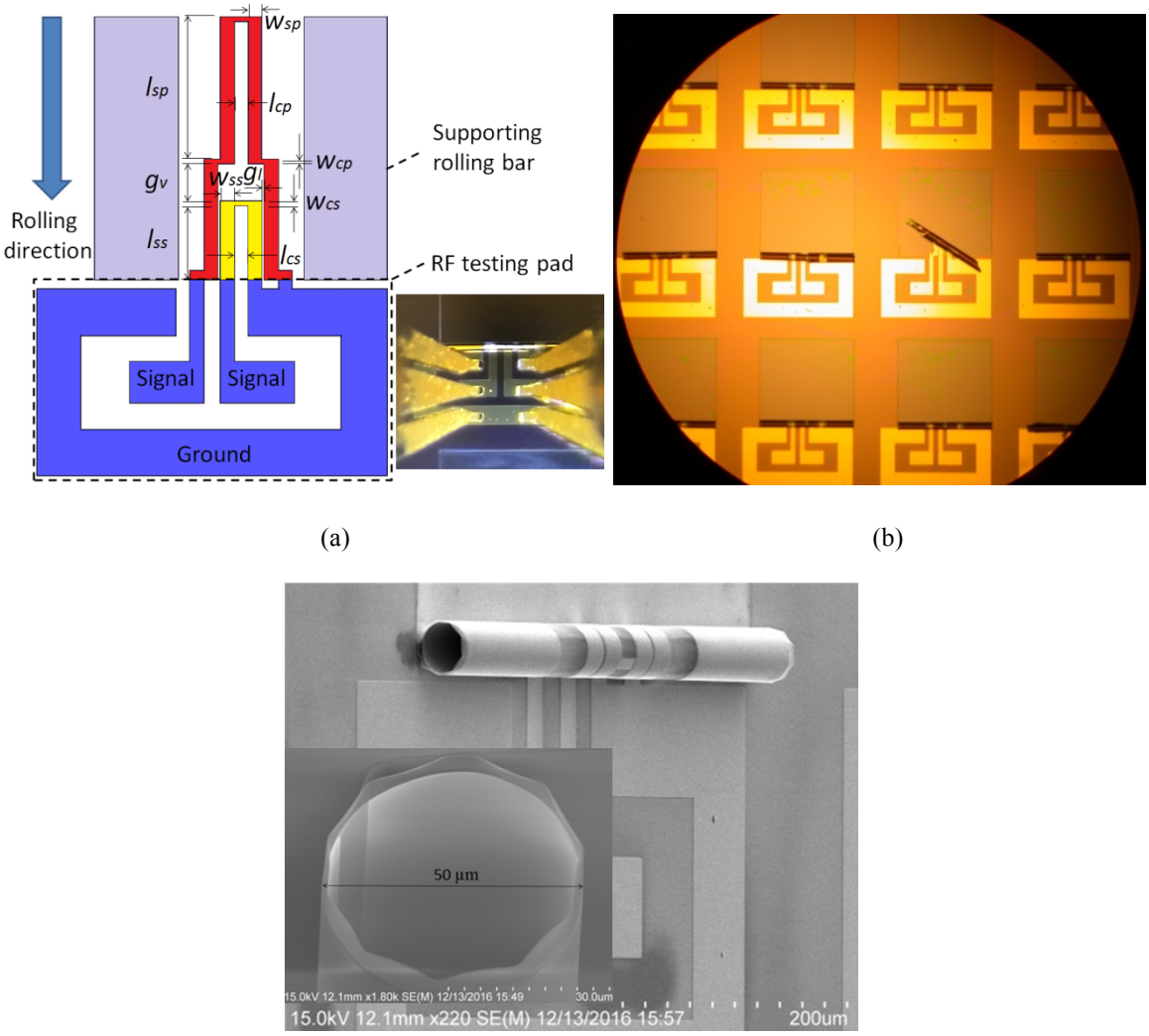


Figure 4.2 Exaggerated inner structural view with parasitic parameters labeled.

4.2 Fabrication Results of S-RuM Transformer Samples

Four different layout designs are fabricated to obtain a wide range of performance. Figure 4.3(a) shows the layout design with dimension parameters labeled. The RF testing pad is designed with a ground-signal-ground (GSG) configuration with 150 μm pitch for two 40 GHz probes shown in the optical photo. Table 4.1 summaries the top view dimension of the four structures. Expect for the center coil strip length l_{sp} and the secondary coil length l_{ss}, all the other parameters are the same. In all the designs, metal strips are made by 100 nm Au on top of a 5 nm Ni adhesion layer with 30 μm width and a 30 μm strip gap. Figure 4.3(b), a top view of twelve samples with eleven of them successfully fabricated, shows a clear trend of S-RuM transformers to obtain high a fabrication yields by using ALD Al_2O_3 to avoid the SiN_x bilayer pinhole defect. SEM images of

a rolled up sample with inner diameter measured is shown in Figure 4.3(c). The S-RuM transformer sample is rolled up tightly, and its inner diameter is 50 μm.



(a) (b)

(c)

Figure 4.3 S-RuM transformer design layout with fabrication results. (a) S-RuM transformer layout design with dimensional parameter and RF testing pads labeled. RF testing pads are designed for GSG probes. Inset figure shows a device under RF test. (b) Optical photo shows fabrication results of a 12-element S-RuM transformer array with 11 of them successfully fabricated. (C) SEM image of a S-RuM transformer sample with inner diameter measured.

TABLE 4.1
DIMENSION PARAMETERS OF FOUR TYPES OF S-RUM TRANSFORMERS

Parameter	Structure 1	Structure 2	Structure 3	Structure 4
w_{sp} (μm)	30	30	30	30
w_{cp} (μm)	10	10	10	10
w_{ss} (μm)	30	30	30	30
w_{cs} (μm)	10	10	10	10
l_{cp} (μm)	30	30	30	30
l_{cs} (μm)	30	30	30	30
g_l (μm)	5	5	5	5
l_{sp} (μm)	186	226	266	306
g_v (μm)	80	80	80	80
l_{ss} (μm)	280	240	200	160

4.3 Tested RF Performance of Au S-RuM Transformer Samples

RF performance was measured by Keysight E8363B PNA from 10 MHz to 40 GHz, and two port scattering (*S*) parameters were obtained. The "open-through" de-embedding procedures were used to calibrate out the RF testing pad effects. Electrical performance is then extracted based on the impedance (*Z*) parameter converted from the measured *S*-parameter. By using a high frequency T-network to model transformer performance, the frequency dependent effective self-inductances of the primary (L_p) and the secondary coils (L_s) and the mutual inductance (M) are given by $L_p = Im(Z_{11})/2\pi f$, $L_s = Im(Z_{22})/2\pi f$, and $M = Im(Z_{21})/2\pi f$, respectively. The Q factors of the primary coil (Q_p) and secondary coil (Q_s) are calculated by $Q_p = Im(Z_{11})/Re(Z_{11})$ and $Q_s = Im(Z_{22})/Re(Z_{22})$.

For all four designed structures, Figures 4.4(a) and 4.4(c) show the inductances of the primary coil and the secondary coil. Compared to traditional transformer performance, the inductances of the S-RuM transformer coils show different patterns: (1) The inductance is not a constant value at low frequency. Instead, inductance goes down before approaching to the resonant frequency. (2) Beyond the resonant frequency, inductance could still be a positive value. Physically, the reduction

of inductance means more loss of magnetic energy stored in the coils. As the skin effect should be small, cross-coupling capacitances storing electrical energy is the main reason for the phenomenon (1). The higher the frequency, the more RF signals could pass through the cross-coupling capacitances from the primary coil to the secondary coil, being stored as electrical energy in one time period. That is why the degrading of inductance becomes noticeable when the frequency goes up. The reason for phenomenon (2) is that the value of the resonant frequency of the primary coil is more than one. The side coils have a different resonant frequency than that of the primary coil. Therefore, when the center coils lose the magnetic energy storage ability, the side coils are not resonant yet, and that makes the inductance still have a positive value beyond the first resonant frequency. However, if the frequency goes higher, the inductance will eventually become a negative value.

For the inductance of the primary coil shown in Figure 4.4(a), at low frequency where the parasitic capacitance effect is not significant, the inductances of all four structures are slightly different. This is because, although the length of the center coil length l_{sp} and the side coil length l_{ss} are changing relatively to each other, their total number of turns is the same but with a different mutual coupling status between them. Among the four types of structures, when the center coil length l_{sp} becomes longer, the overall parasitic capacitance effect becomes more serious to introduce stronger distortion of both inductance and Q factor curves. As the resistance of the primary coil is unchanged, the Q factors of the primary coil of all four structures show different levels of distortion corresponding to the inductance distortion shown in Figure 4.4(b).

The secondary coils do not have side parts, so the distortion of inductance and Q factor is relatively smaller than that of the primary coil, except when the parasitic capacitance becomes serious in structure 4, as shown in Figure 4.4(d). Inductances decrease when the secondary coil

length l_{ss} becomes shorter. However, when the number of turns of the secondary coils is not too many, the superlinear relationship between inductance and number of turn is not significant, so the resistance of the secondary coil drops almost linearly with the inductance to make the Q factor nearly unchanged for all four structures before the parasitic capacitances become dominant.

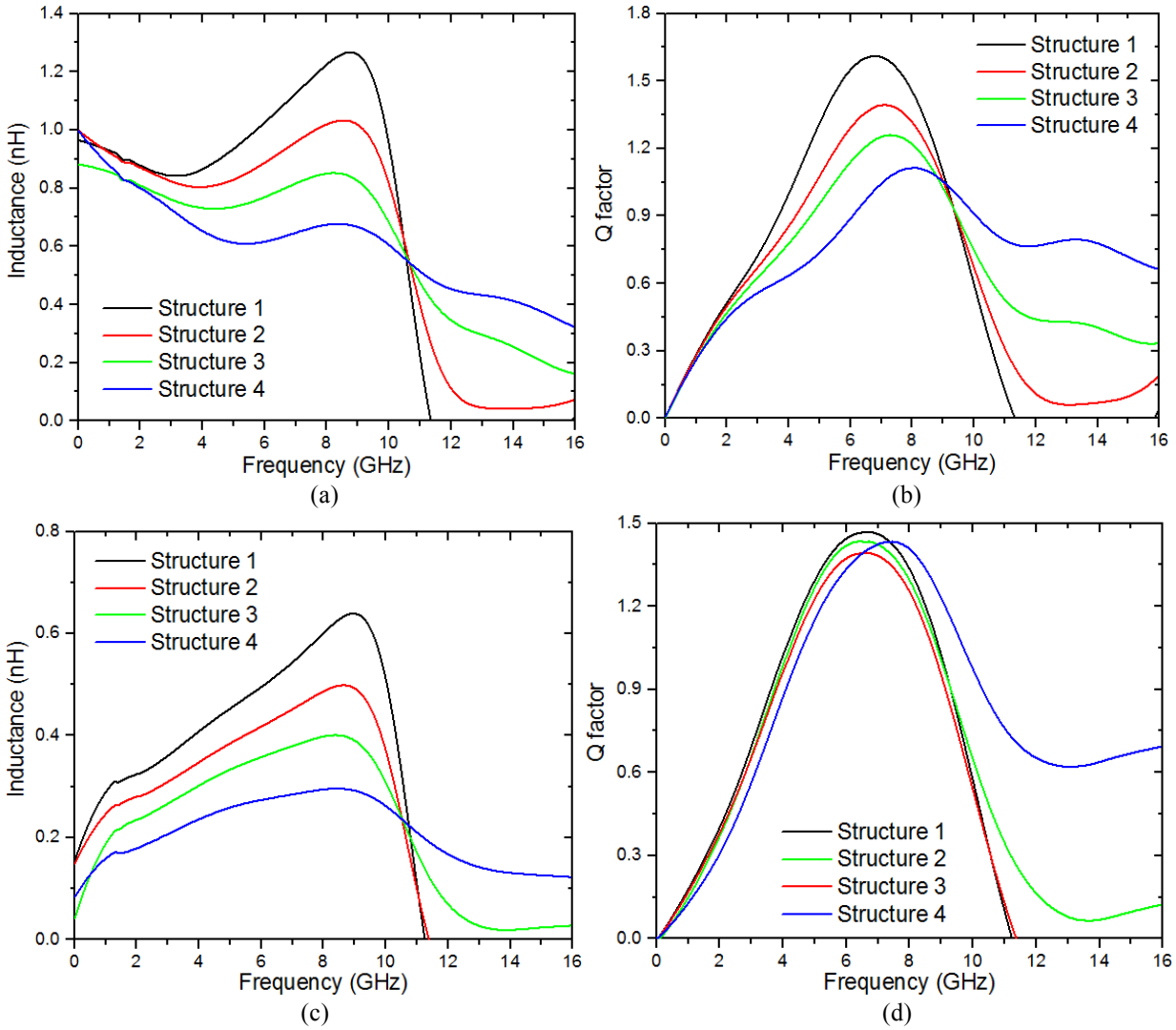
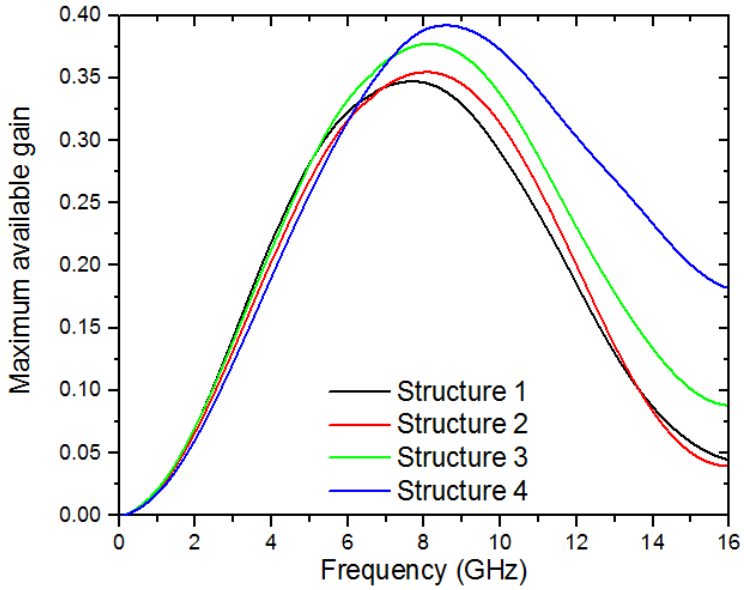


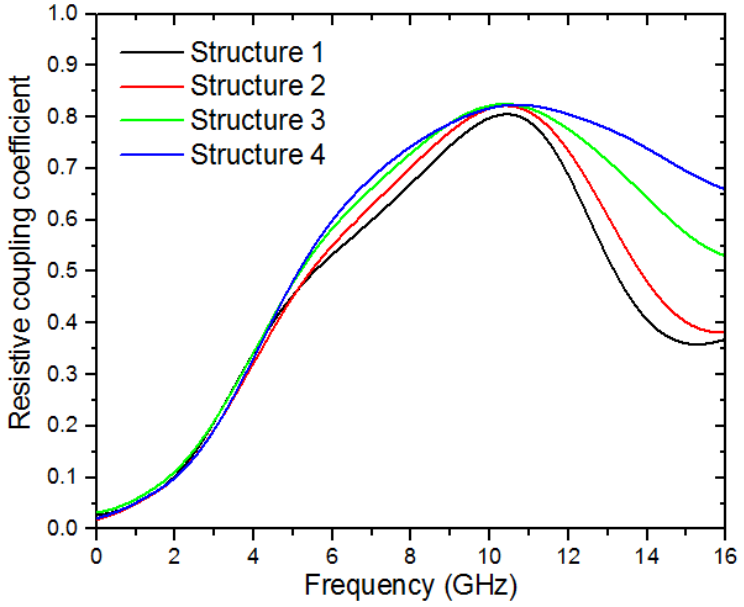
Figure 4.4 Extracted electrical performance of S-RuM transformer samples. (a) Frequency dependent inductance of primary coil. (b) Frequency dependent Q factor of primary coil. (c) Frequency dependent inductance of secondary coil. (d) Frequency dependent Q factor of secondary coil.

A maximum available gain (G_{max}) is used to elucidate the energy loss in the primary and the secondary coils. For the on-chip transformers, equation $G_{max} = \left[1 + 2\left(x + \sqrt{x^2 + x}\right)\right]^{-1}$ is defined to calculate the maximum available gain, where $x = \left(k^2 Q_p Q_s\right)^{-1}$. By observing the equation of G_{max}, large values of Q_s, Q_p, and k are needed to obtain a high maximum gain. Figure 4.5(a) shows the G_{max} of all four structures. The peak value of G_{max} of each structure occurs at the frequency where Q factors of both primary and secondary coils reach the maximum value. With the increasing of center coil length l_{sp}, the peak G_{max} occurs at a higher frequency. The maximum G_{max} reaches 39.2% at 8.6 GHz with structure four's design. It implies that structure four has the largest mutual magnetic coupling coefficient when G_{max} reaches its peak value, because its maximum Q factors of the primary and secondary coils have the smallest value compared to other structures.

Mutual resistive coupling coefficient k_r is calculated by $k_r = Re(Z_{12}) \cdot [Re(Z_{11}) \cdot Re(Z_{22})]^{-1/2}$, which mainly accounts for the hybrid effects of parasitic capacitances and eddy currents in the silicon substrate. The lower the k_r, the less substrate parasitic effects the transformer has. It is a convenient indicator for the improvement of the substrate issue of the S-RuM platform. Figure 4.5(b) shows the extracted k_r as a function of frequency for all four S-RuM transformer structures. It can be seen clearly that the frequencies of the peak value of G_{max} and k_r are different. Even if all S-RuM transformers are fabricated with only 0.8 μm thick SiO_2 insulation layers (the standard CMOS SiO_2 layer is >5 μm) on a standard doping range silicon substrate, the peak value of k_r of ~0.8 is still smaller than that of most reported on-chip planar transformers, which is usually larger than 0.9. Because majority portion of the EM field is confined away from the substrate is the reason for the substrate issue improvement, and it is consistent with what we found in S-RuM inductors.



(a)



(b)

Figure 4.5 Extracted electrical performance of the S-RuM transformer samples. (a) Frequency dependent maximum available gain. (b) Frequency dependent resistive coupling coefficient.

4.4 Performance Reliability of Au S-RuM Transformer Samples

Reliability is another important factor for the application of S-RuM transformers. As a passive device, the electrical performance of the S-RuM transformers mainly depends on the physical and chemical stability of its mechanical support, which is the rolled-up bilayer SiN_x film with Al_2O_3 covering on one side.

4.4.1 Thermal Stability of Au S-RuM Transformer Structure

The bilayer SiN_x film is deposited using a $NH_3/SiH_4/N_2$ gas mixture with processing temperature at 240 ºC at the shower head and at 300 ºC at the platen. The diameter can be drastically shrunk after rolling via a high temperature RTA due to outdiffusion of embedded hydrogen and ammonia within the SiN_x film. Annealing tests at temperatures close to the SiN_x film deposition temperature (250 ºC) and beyond (350 ºC) for 5 minutes are carried out to test the S-RuM transformer thermal stability. Figure 4.6(a) and 4.6(b) compare the inductances and Q factors of the primary and secondary coils with the Structure 1 design at different annealing conditions. For inductances, there is a little change at 250 ºC, and a noticeable decrease at 350 ºC especially at frequencies lower than 4 GHz. The Q factors change accordingly but with more substantial drop of Q_{max} due to the increase of Au resistivity, which is proved by measuring DC resistances at different annealing conditions, as shown in the inset of Figure 4.6(b). The DC resistances of both primary and secondary coils remain the same until being annealed at 350 ºC, and this is attributed to the Au film straining during the diameter altering process. Figure 4.6(c) summaries the change of the overall performance G_{max} and the corresponding mutual magnetic coupling coefficient k_m. When the diameter becomes smaller, the number of turns for both primary and secondary coils increases. With the unchanged separation distance between coils, more turns per coil means stronger mutual magnetic coupling. Therefore, for designs of all four structures, k_m

slightly increases, but G_{max} still drops especially at 350 ºC annealing, since inductance and Q factor degenerated more seriously. The shrunk inner diameter is shown in Figure 4.6(d) with a measured value of ~46.8 μm. Compared to original the SEM picture in Figure 4.3(c), there is about 6.4% alteration of the inner diameter, but the coils are still very tightly rolled up with no noticeable film damage.

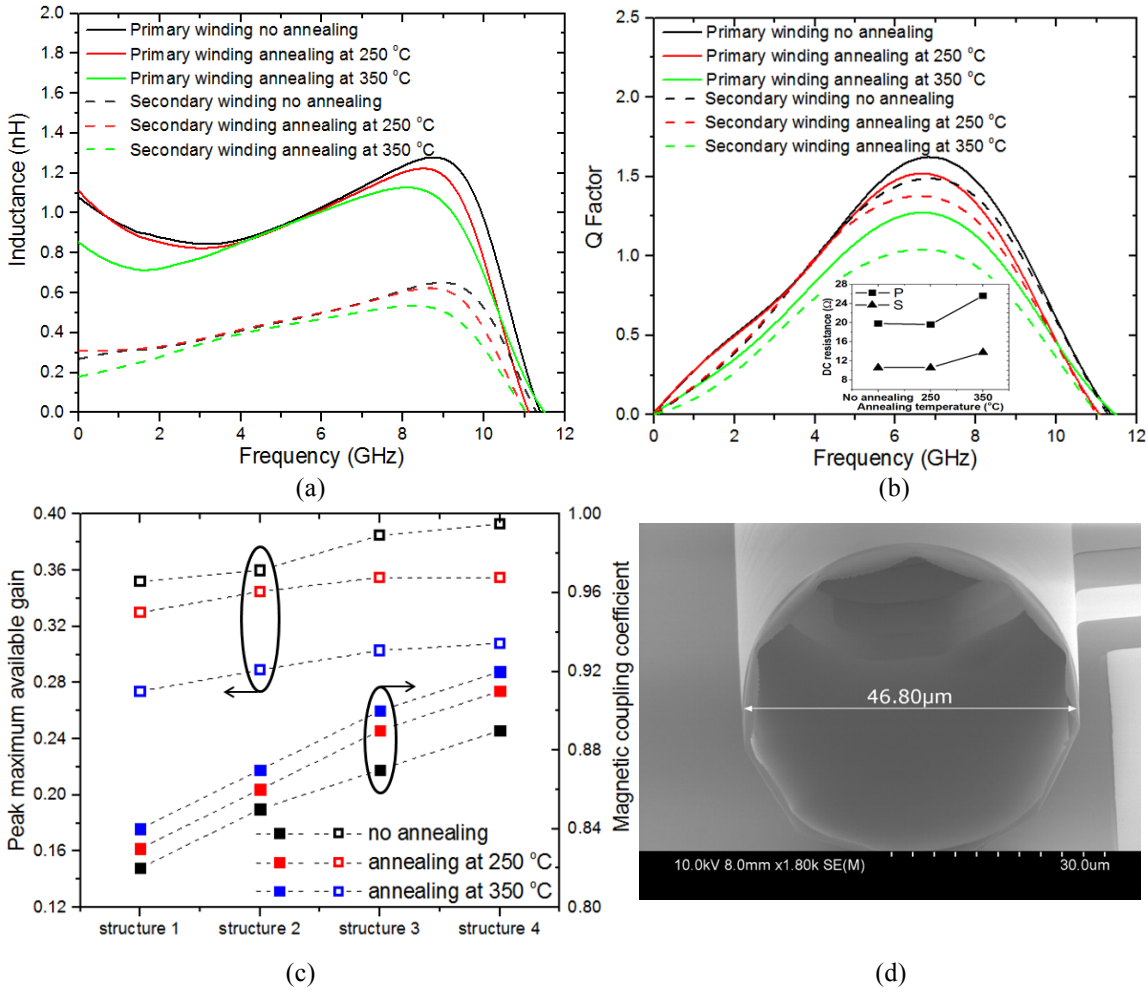
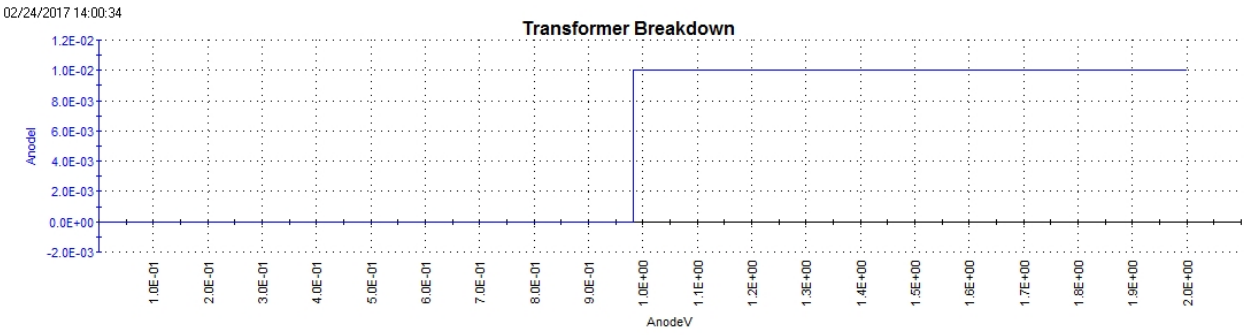


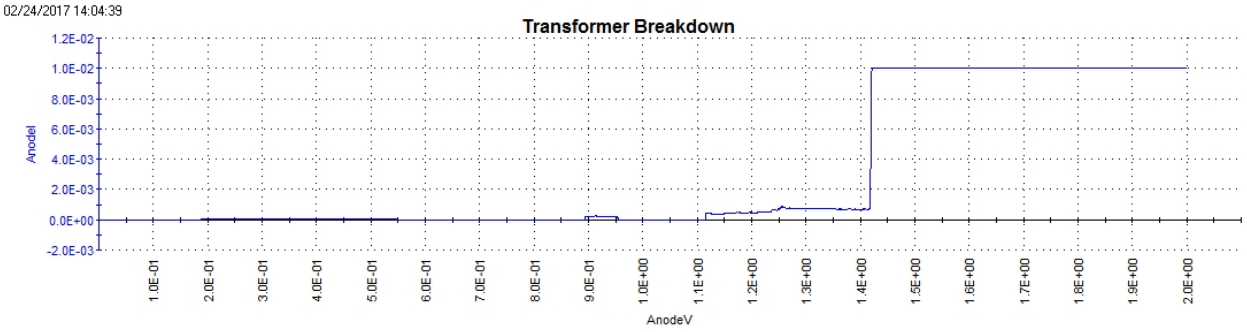
Figure 4.6 Thermal and mechanical reliability tests of S-RuM transformer devices. (a) Annealing tests on the inductances of the primary and the secondary coils of the S-RuM transformers with the Structure 1 design. (b) Annealing tests on the Q factors of the primary and the secondary coils of the S-RuM transformers with Structure 1 design. (c) Annealing tests on the peak maximum available gain and mutual magnetic coupling coefficient of all S-RuM transformer devices. (d) SEM picture shows the measured inner diameter after annealing at 350 ºC for 5 mins of the S-RuM transformer with the Structure 1 design.

4.4.2 Breakdown Voltage of Au S-RuM Transformer Structure

The S-RuM transformers could suffer long term failure after applying a high voltage between the primary and the secondary coils. High voltage will generate a large electric stress on the dielectric layers in between the closest face-to-face areas on the primary and secondary coils. The dielectric layers for the Au S-RuM transformer devices are constructed by 25 nm ALD Al_2O_3 on top of the 40 nm PECVD SiN_x bilayer. The ALD Al_2O_3 thin film is expected to be dense with high quality. However, the PECVD SiN_x bilayer has relatively low film quality due to pinholes and voids embedded inside the film. One problem is that the top ALD Al_2O_3 thin film layer will not be smooth as expected; it could be conformal with pinholes and surface voids so the surface quality will unknown. The other important problem is that, for normal bulky dielectric materials, irreversible mechanical and chemical deterioration of the insulating material is caused by the cumulative effect of partial discharging (PD), but as voids and pinholes come originally in the S-RuM transformer dielectric layer, the cumulative progress to the formation of numerous and branching partially conducting discharge channels (treeing) could be shorted out in less than one picosecond when the electric stress is high enough. Those two issues together become the breakdown mechanism for the S-RuM transformer. Figure 4.7 shows a breakdown voltage test on the Structure 2 Au S-RuM transformer by sweeping DC voltage from 0 V to 2 V with 0.001 V step size. The breakdown voltage of Structure 1 is about 0.983 V, and the breakdown voltage of Structure 2 is about 1.417 V. The variation of breakdown voltage of the same structural device reveals the fact that the randomness of the microstructure of dielectric layers determines the variation of electric stress breakdown. To increase the breakdown voltage, the spacing between the primary and the secondary coils needs to be enlarged (increase the value of g_v in Figure 4.3(a)) and the film quality needs to be improved too.



(a)



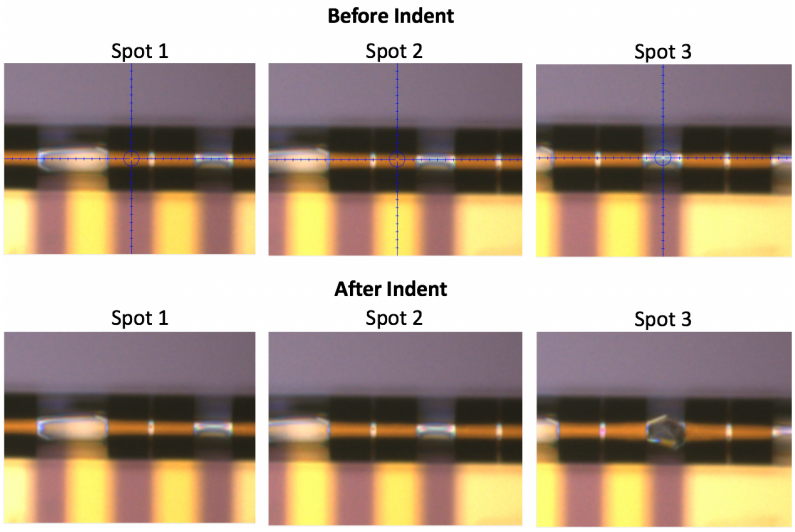
(b)

Figure 4.7 Breakdown voltage test on Structure 2 Au S-RuM transformer by sweeping DC voltage from 0 V to 2 V with 0.001 V step size. (a) Tested result of Structure 1. (b) Tested result of Structure 2.

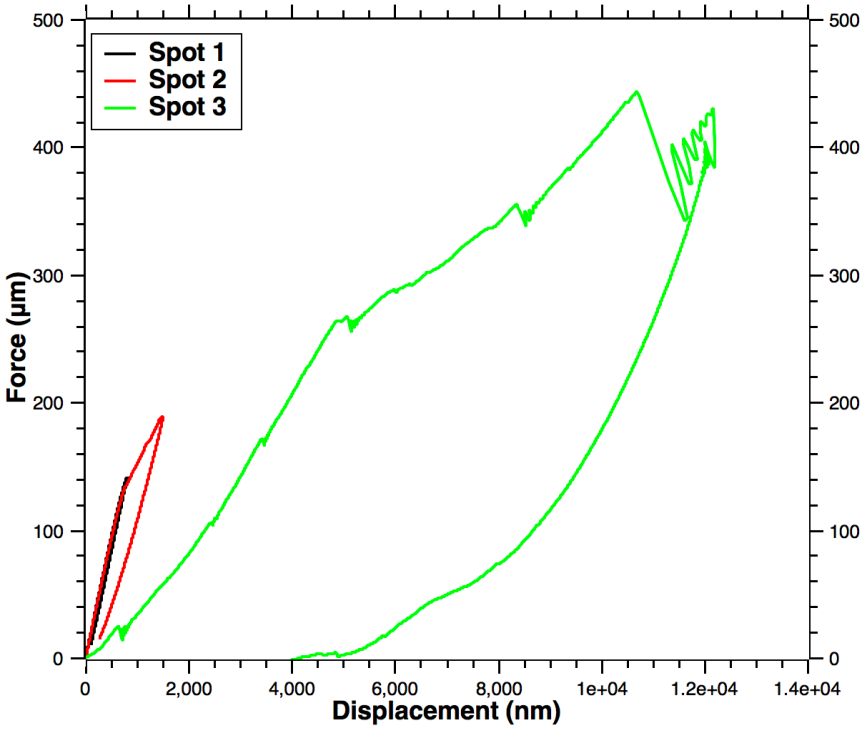
4.4.3 Mechanical Stability of Au S-RuM Transformer Structure

By investigating the Au S-RuM transformer's stiffness at various spots along the device, a better understanding of critical failure points can be achieved and potential alleviation can be planned. The tests were performed using a Hysitron TI 950 TriboIndenter with a 65.3° Berkovich tip under load-partial unload conditions. A triangular pulse waveform with different peak forces and loading rates was used over 2 seconds to almost deform the microtube.

Under examination, Structure 1 design of the Au S-RuM transformer structures after RTA at 350 °C were subjected to different maximum indentation and force at several spots along the microtube axis as shown in Figure 4.8(a).



(a)

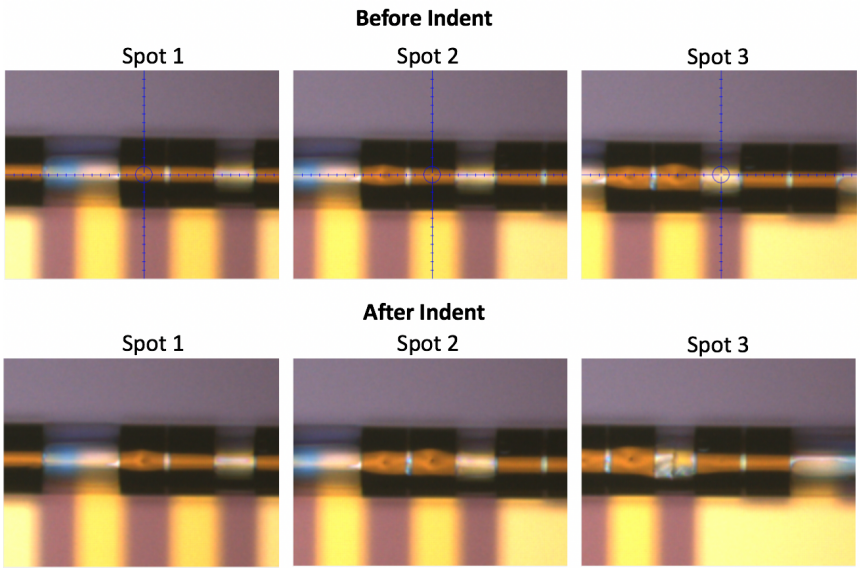


(b)

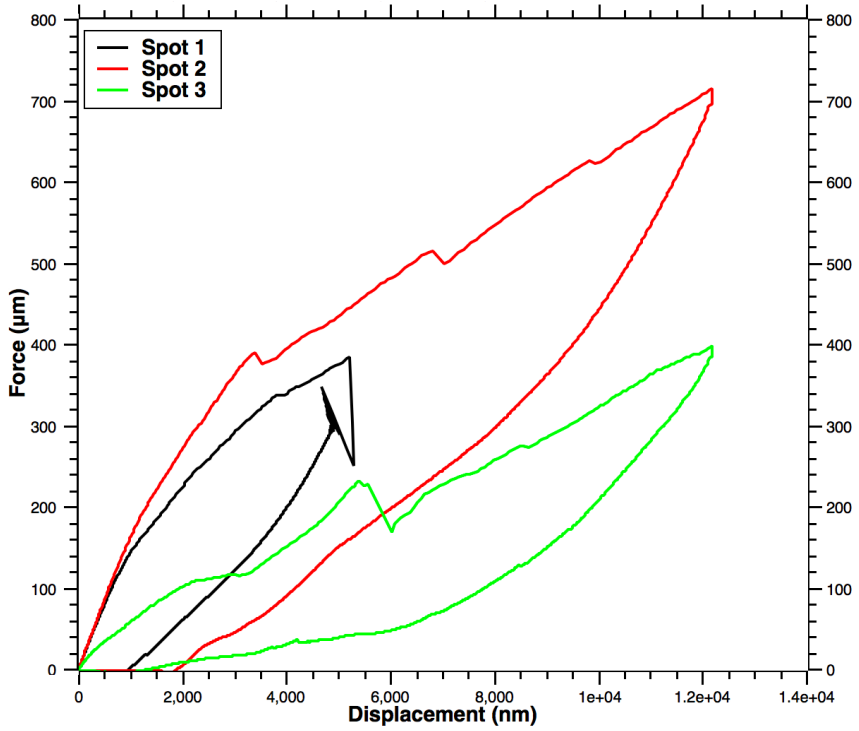
Figure 4.8 Mechanical stability test of Structure 1 design of the Au S-RuM transformer. (a) Optical photos for the top views at different spots along the axis of Structure 1 design of the Au S-RuM transformer before and after nano-indention. Spot 1 is on top of one center coil. Spot 2 is on top of the other center coil. Spot 3 is on top of the SiN_x membrane. (b) Displacement vs. force curves at different spots.

The load vs. the displacement characteristics are compared for the spot on top of the edge coil, the spot on top of the middle coil, and the spot on top of the SiN_x membrane. It can be seen from Figure 4.8(b) that the structure at different spots under testing experienced continuous fracturing during the indention. Before the first fracture point, the structure at different spots was in the elastic deformation region. Stiffnesses at different spots can then be calculated in the elastic region, which are 191.7 N/m, 188.4 N/m, and 37.6 N/m, respectively. The mass of the Structure 1 design of the Au S-RuM transformer is $\sim 8.36738 \times 10^{-11}$ kg; therefore the forces that could cause the top surface of the Structure 1 Au S-RuM transformer to crack are 207, 316 g at spot 2 and 28, 048.7 g at spot 3, where g is the gravitation acceleration, or 9.8 m/s^2. Compared to a suspended MEMS high Q factor spiral inductor with X-beams which has maximum stiffness ~0.56 N/m at its inner turn and is claimed to have an enhancement of maximum mechanical strength more than 4500 times better than its counterparts [34], the maximum stiffness of the Structure 1 design of the Au S-RuM transformer is 342.3 times larger.

Under examination, the Structure 2 design of the Au S-RuM transformers after RTA at 350 °C were subjected to different maximum indentations and forces at several spots along the microtube axis as shown in Figure 4.9(a).



(a)

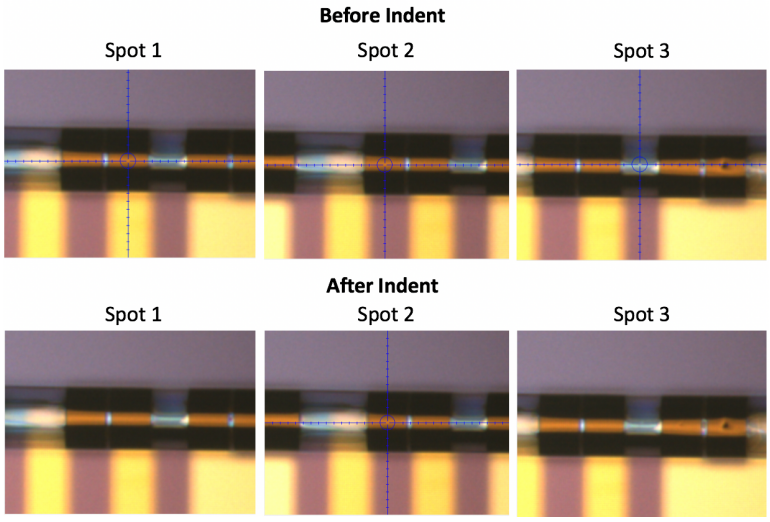


(b)

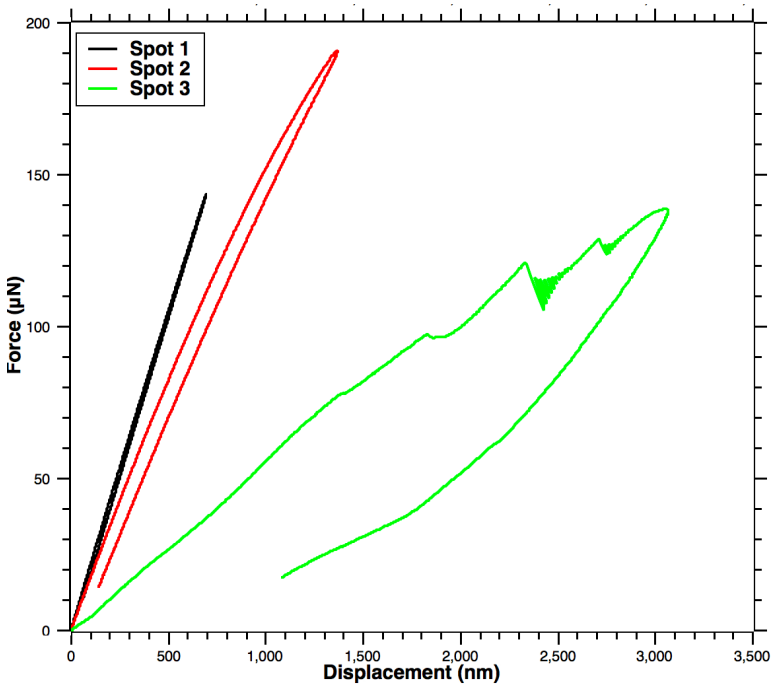
Figure 4.9 Mechanical stability test of the Structure 2 design of the Au S-RuM transformer. (a) Optical photos for the top views at different spots along the axis of the Structure 2 design of the Au S-RuM transformer before and after nano-indention. Spot 1 is on top of one center coil. Spot 2 is on top of the other center coil. Spot 3 is on top of the SiN_x membrane. (b) Displacement vs. force curves at different spots.

The load vs. the displacement characteristics are compared for the spot on top of the edge coil, the spot on top of the middle coil, and the spot on top of the SiN_x membrane. It can be seen from Figure 4.9(b) that the structure at different spots under testing experienced continuous fracturing during the indention. Before the first fracture point, the structure at different spots was in the elastic deformation region. Stiffnesses at different spots can be then calculated in the elastic region, which are 175.5 N/m, 181.6 N/m, and 90.3 N/m, respectively. The mass of the Structure 2 design of the Au S-RuM transformer is ~8.13242×10^{-11} kg, therefore the force that could cause the top surface of the Structure 2 design of the Au S-RuM transformer to crack are 426, 612 g at spot 1, 489, 349 g at spot 2, 138, 022 g at spot 3, where g is the gravitation acceleration, or 9.8 m/s^2. Compared to a suspended MEMS high Q factor spiral inductor with X-beams which has maximum stiffness of ~0.56 N/m at its inner turn and is claimed to have an enhancement of maximum mechanical strength more than 4500 times better than its counterparts [34], the maximum stiffness of the Structure 2 design of the Au S-RuM transformer is 324.3 times larger.

Under examination, the Structure 3 design of the Au S-RuM transformers after RTA at 350 °C were subjected to different maximum indentations and forces at several spots along the microtube axis as shown in Figure 4.10(a).



(a)

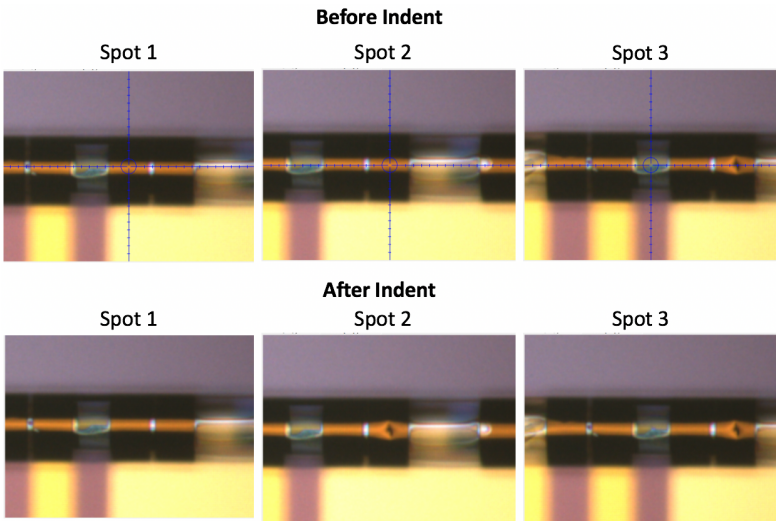


(b)

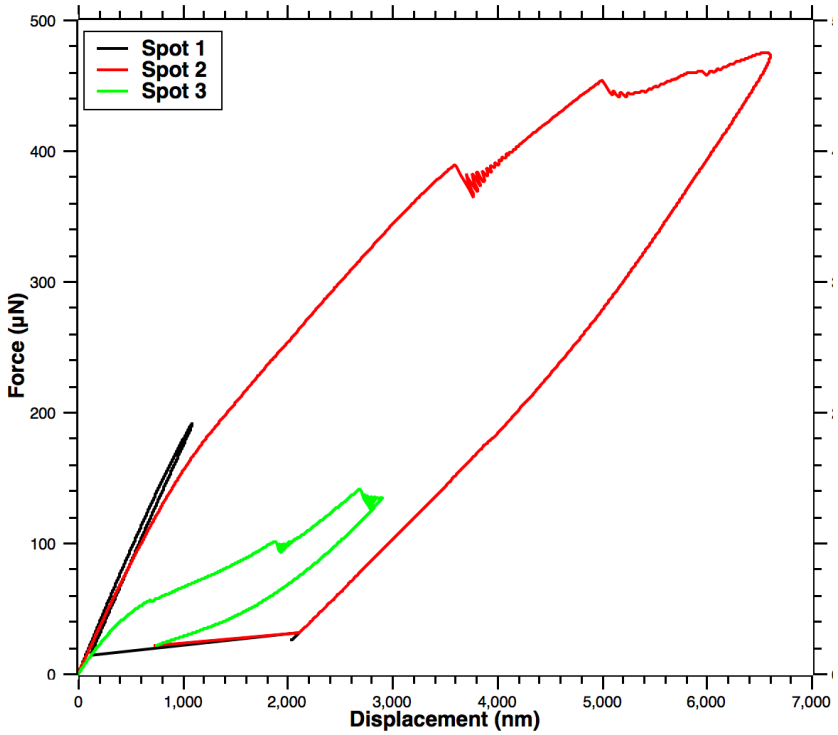
Figure 4.10 Mechanical stability test of the Structure 3 design of the Au S-RuM transformer. (a) Optical photos for the top views at different spots along the axis of the Structure 3 design of the Au S-RuM transformer before and after nano-indention. Spot 1 is on top of one center coil. Spot 2 is on top of the other center coil. Spot 3 is on top of the SiN_x membrane. (b) Displacement vs. force curves at different spots.

The load vs. the displacement characteristics are compared for the spot on top of the edge coil, the spot on top of the middle coil, and the spot on top of the SiN_x membrane. It can be seen from Figure 4.10(b) that the structure at different spots under testing experienced continuous fracturing during the indention. Before the first fracturing point, the structure at different spots was in the elastic deformation region. Stiffnesses at different spots can be then calculated in the elastic region, which are 210.2 N/m, 164.8 N/m, and 53.2 N/m, respectively. Compared to a suspended MEMS high Q factor spiral inductor with X-beams which has maximum stiffness of ~ 0.56 N/m at its inner turn and is claimed to have an enhancement of maximum mechanical strength more than 4500 times greater than its counterparts [34], the maximum stiffness of the Structure 3 design of the Au S-RuM transformer is 375.4 times larger.

Under examination, the Structure 4 design of the Au S-RuM transformers after RTA at 350 °C were subjected to different maximum indentation and force at several spots along the microtube axis as shown in Figure 4.11(a).



(a)



(b)

Figure 4.11 Mechanical stability test of the Structure 4 design of the Au S-RuM transformer. (a) Optical photos for the top views at different spots along the axis of the Structure 4 design of the Au S-RuM transformer before and after nano-indention. Spot 1 is on top of one side coil. Spot 2 is on top of the other side coil. Spot 3 is on top of the SiN_x membrane. (b) Displacement vs. force curves at different spots.

The load vs. the displacement characteristics are compared for the spot on top of the edge coil, the spot on top of the middle coil, and the spot on top of the SiN_x membrane. It can be seen from Figure 4.11(b) that the structure at different spots under testing experienced continuous fracturing during the indention. Before the first fracture point, the structure at different spots was in the elastic deformation region. Stiffnesses at different spots can be then calculated in the elastic region, which are 196.4 N/m, 180.7 N/m, and 93.2 N/m, respectively. Compared to a suspended MEMS high Q factor spiral inductor with X-beams which has maximum stiffness of ~0.56N/m at its inner turn and is claimed to have an enhancement of maximum mechanical strength more than 4500 times better than its counterparts [34], the maximum stiffness of the Structure 4 design of the Au S-RuM transformer is 350.7 times larger.

CHAPTER 5: S-RuM INTEGRATED CIRCUITS

5.1 Front-to-Back Design Flow for S-RuM ICs

Streamlining the design methodology and software environment of S-RuM lumped passive devices and ICs with the fastest turn-around time and at the lowest cost is important for practical use. Accurate and fast product design depends on a systematic and high efficiency simulation platform. Just like traditional IC design, the design of S-RuM discrete and IC devices also requires front-to-back design flow, which is able to consider every detail from design stage to packaging stage. Inner diameter prediction of rolled-up SiN_x structures by quasi-dynamic simulation was developed for this thesis based on a finite element method (FEM) method, and a physical model for calculating the performance of S-RuM inductor was also developed. Although the developed models are able to predict device geometry and performance, a multiphysics scenario is not possible. To build a multiphysics simulation platform for S-RuM devices and circuits, which allows designers to predict the eventual electrical performance of the final product from the initial 2-D layout design is critical.

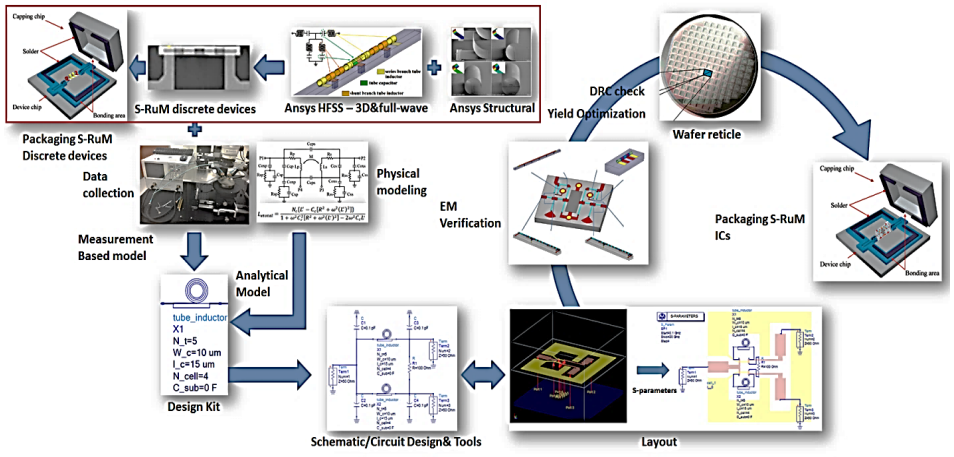


Figure 5.1 Front-to-back design flow for S-RuM IC chips using streamlined multiphysics simulation platforms, to enable visualizing the final 3-D rolled-up IC chip performance from initial 2-D layouts of discrete devices. The proposed discrete design platform is shown in the upper left box.

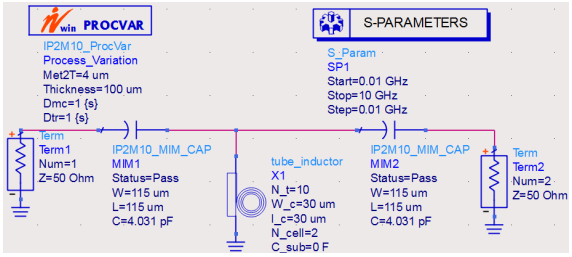
Figure 5.1 illustrates the front-to-back design flow for the S-RuM platform, in an effort to make it similar to traditional IC design flows. The design flow for S-RuM discrete devices is in the red box (upper left in Figure 5.1) and relatively straightforward. The Matlab platform can be used as a hub to interface the Ansys structural simulator and the Ansys high frequency structure simulator (HFSS) to do mechanical-electrical multiphysics co-simulation. Packaging details will be included in the HFSS simulation. S-RuM IC development will be integrated into the most widely used IC design software – Advance Design System (ADS) by Keysight. Similar to the traditional IC design in ADS, the following proposed design flow will help designers create robust S-RuM IC designs with first-pass success and high yield, while minimizing development and production costs. Both the measurement-based model and the physical model will be ready to be integrated into ADS as a user defined model. The rest of the design flow covers schematic/circuit design, layout design, EM verification, yield optimization, DRC check, wafer reticle, and packaging. As an advanced feature recently developed by Keysight, EMPro will be used for creating S-RuM devices together with 2-D circuit layouts and schematics within ADS to perform EM-circuit co-simulation, which is an important improvement for fast and efficient RF and microwave circuit design.

5.2 S-RuM IC Design Flow Example

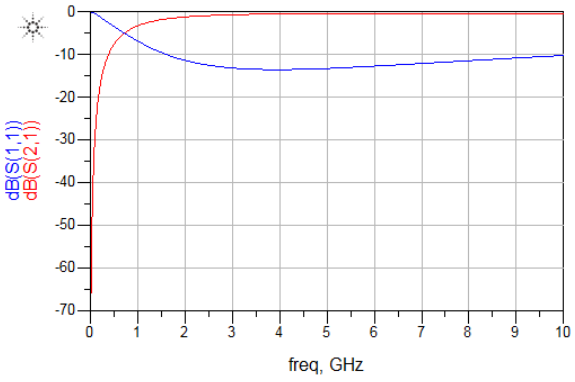
In this section, a high pass RF filter will be used as an example to go through the design flow of the S-RuM IC designs. A Win semiconductor IP2M_10_integrated_passive 2 metal interlayer processing design kit and a Cu S-RuM inductor design kit are used in the design.

The first step is to do schematic simulation. As shown in Figure 5.2(a), a simple T-network high pass filter is constructed by two (metal-insulator-metal) MIM capacitors connected in series and one S-RuM inductor connected in parallel. The model for the S-RuM inductor is based on a

physical equivalent circuit model with each circuit parameter calculated by an analytical equation. Dimension parameters, such as inner diameter, metal conductivity, strip width, and metal thickness, are determined in the previous model. Other parameters, such as number of turns, number of cells, connection line width and length, and substrate conductivity, can be changed. To design a high pass filter with cutoff frequency at 0.7 GHz, the calculated capacitance value is 4 pF and the inductance value is 8 nH. From the design kit, the dimensions of the MIM capacitor are 115 μm × 115 μm, and the S-RuM inductor is a 2-cell-10-turn inductor with a 30 μm long and a 30 μm wide connection line. Figure 5.2(b) shows the simulation result from 10 MHz to 10 GHz. The return loss S_{11} in the simulation result is just –5 dB at 0.7 GHz because the Q factor of the S-RuM inductor at 0.7 GHz is not high enough.



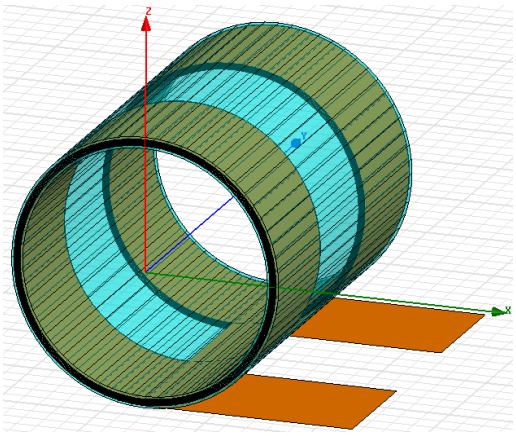
(a)



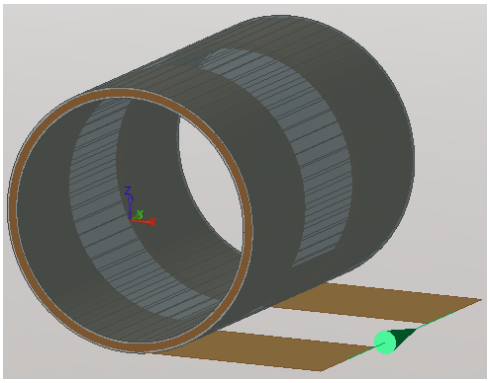
(b)

Figure 5.2 Schematic circuit layout and simulation result of a high pass filter with cutoff frequency at 0.7 GHz. (a) Schematic circuit layout with dimension parameter labeled in model symbols. (b) Simulation result from 10 MHz to 10 GHz.

The next step is to do layout simulation. To construct a 3-D model of the S-RuM inductor in the ADS FEM simulator, a 2-cell-10-turn S-RuM inductor with the same dimensions as the one used in schematic simulation is first built in the high frequency structure simulator (HFSS) as shown in Figure 5.3(a). The spiral coil and dielectric layers are approximately modeled by a polygon hollow cylinder with a zero thickness wall in order to reduce the computation load. The built 3-D model is then imported into EMPro as shown in Figure 5.3(b). Material properties and port definition are done in EMPro to generate a library which can be used in the ADS FEM simulator.



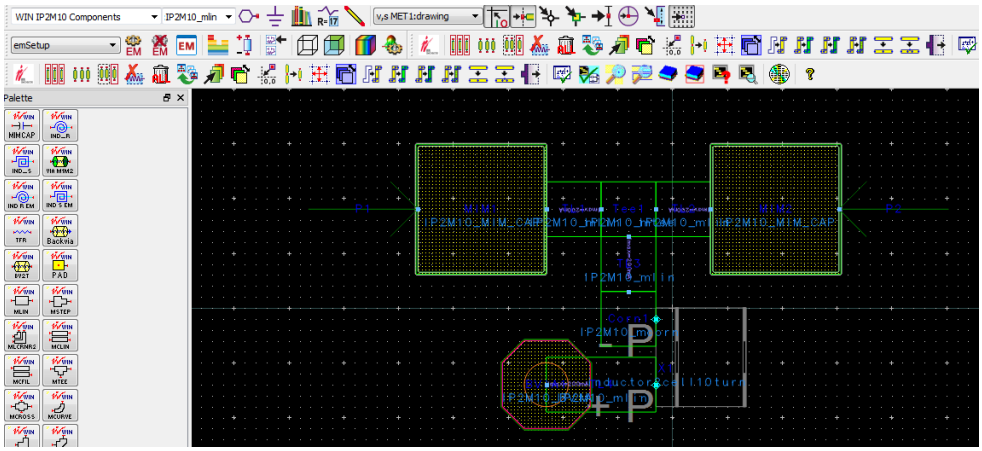
(a)



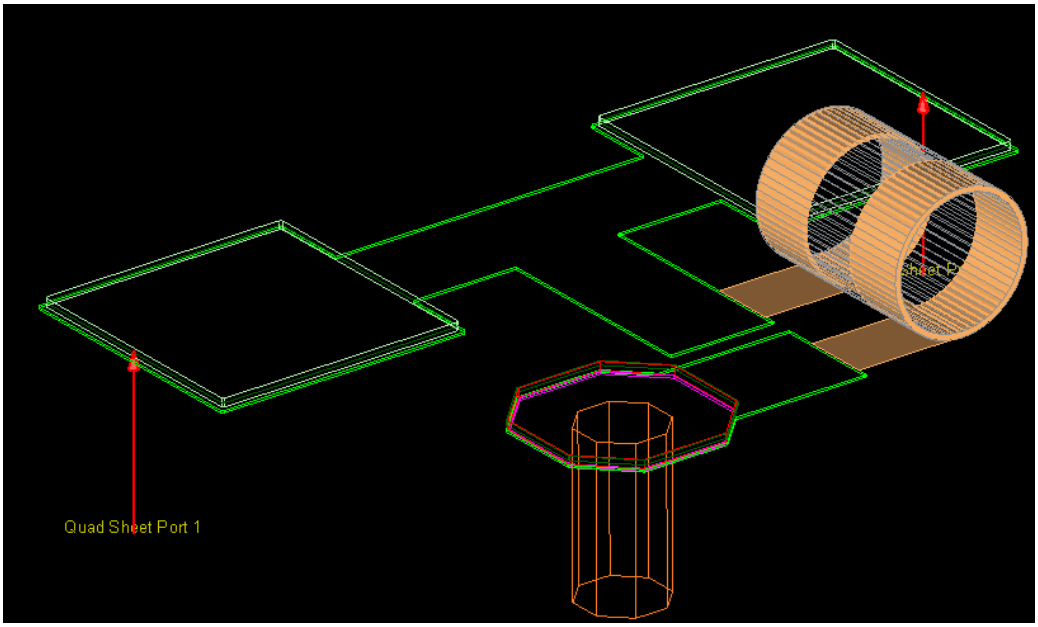
(b)

Figure 5.3 3-D model generation for FEM simulation in ADS. (a) 3-D structure built in HFSS. (b) 3-D model generated in EMPro.

The next step is to generate a 3-D layout in ADS to do the FEM simulation. It is the same as designing any other RF integrated circuits (RFICs) or mm-wave monolithic integrated circuits (MMICs). Figure 5.4(a) shows the 2-D view of the layout. Capacitors and inductors are connected by microstrip lines, and the inductor is connected to the ground by connecting to the backside via. Figure 5.4(b) shows the 3-D view of the designed structure.



(a)



(b)

Figure 5.4 FEM modeling in ADS. (a) 2-D view in layout. (b) 3-D view of designed highpass filter.

5.3 Chip Size Miniaturization by Using S-RuM Inductors in Active ICs

By simply replacing the planar spiral inductors on RFIC chips with our S-RuM inductor, the die size can already be reduced significantly. Figures 5.5(a) and 5.5(b) compare a low noise amplifier (LNA) layout designed on the conventional planar platform and on the S-RuM platform, for a Ku band MMIC LNA operating at 11.5 GHz to 12.5 GHz, using the ADS design kit (KeySight Technologies). When all three planar spiral inductors are replaced by S-RuM inductors of the same performance metrics, the die size is reduced from 1210 μm × 810 μm to 550 μm × 1000 μm, which is about half of the original size.

Figures 5.5(c) and 5.5(d) present an example showing how much area can be saved (~38% of the original size) when the S-RuM platform is used for a Wilkinson power splitter working at 24 GHz.

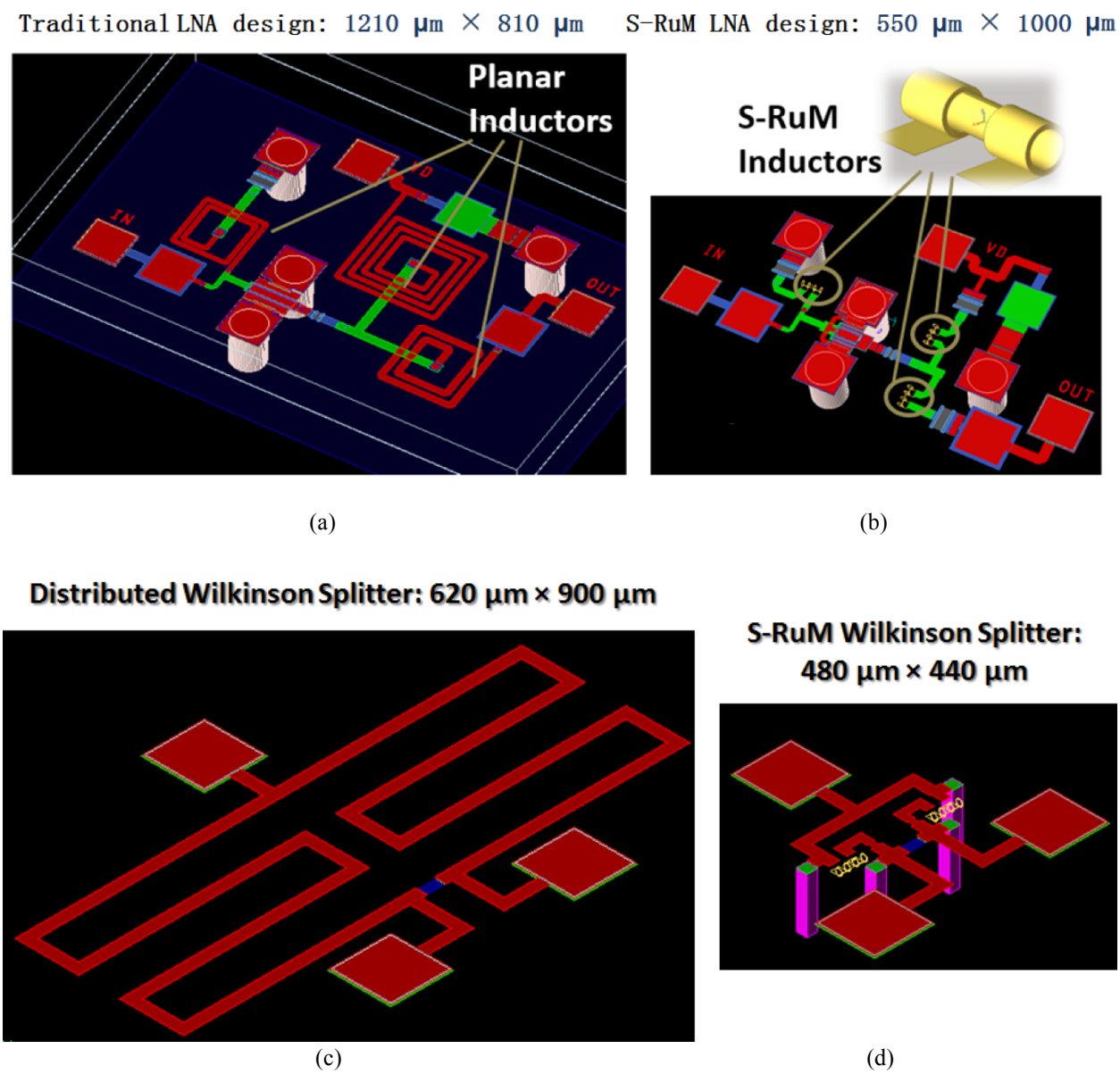


Figure 5.5 Die size comparison of the S-RuM IC vs. traditional IC. (a) LNA designed on traditional IC platform with a die size of ~1210 µm × 810 µm. (b) LNA designed on the S-RuM IC platform with a die size of ~550 µm × 1000 µm. The traditional LNA layout is taken from ADS (KeySight) and the S-RuM inductors were designed and embedded into ADS using EMPro 3-D EM Simulation Software. (c) A 24 GHz Wilkinson power splitter designed on a conventional distributed IC platform with a die size of ~620 × 900 μm^2. (d) A 24 GHz Wilkinson power splitter designed on S-RuM IC platform with a die size ~ 480 × 440 μm^2.

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APPENDIX A: CU S-RUM INDUCTOR FABRICATION PROCESS

(1) Silicon wafer preparation.

Standard RCA clean, $NH_4OH : H_2O_2 : H_2O = 1 : 1 : 5$, at 80 °C, 10 min, $HF : H_2O = 1 : 100$, at room temperature, 1 min, $HCl : H_2O_2 : H_2O = 1 : 1 : 5$, at 80 °C for 10 min, DI water raise, N_2 drying.

(2) Wet thermal oxidation.

1 μm SiO_2, at 1150 °C for 2 hours.

(3) Sacrificial layer deposition.

20 nm Ge is deposited by electron beam evaporation, with 0.5 Å/sec rate.

(4) SiN_x bilayer growth.

Dual-frequency STS-PECVD (Surface Technology Systems) deposition;

300 °C platen, 240 °C showerhead;

20 nm LF SiN_x deposition, 380 KHz RF power, 20 W, $SiH_4 : NH_3 = 1 : 1$, 300 mT;

20 nm HF SiN_x deposition, 13.56 MHz RF power, 20 W, $SiH_4 : NH_3 = 4 : 5.5$, 900 mT.

(5) Define the rectangle tube patterns.

Spin on positive photoresist (AZ5214E);

Soft bake 1min at 110 °C;

Exposed by 320 nm UV lithography (297W) with optical photo mask for 1min;

Develop in MIF 917 developer;

O_2 descum 2min 500 W for PR residual removal;

Reactive ion etching by CF_4 – Etching through Ge and 50 nm down to SiO_2 for 4 mins;

Acetone, Methanol, Isopropanol strip PR;

O_2 descum 2 min 500 W for PR residual removal.

(6) Cu/Ni(or Cr) strips deposition.

Spin on image reversal photoresist (AZ5214E-IR);

Soft bake 1min at 110 °C;

Exposed by 320 nm UV lithography with optical photo mask for 10 s;

Reversal bake 1 min at 115 °C;

Flood exposure for 2 mins;

Develop in MIF 917 developer for 40 s;

O_2 descum for 2 mins at 500 W for PR residual removal;

HCL for 2 min;

5 nm Ni or Cr, followed by 100 nm Cu deposition by electron beam evaporation, with 0.2 Å/sec and 0.5 Å/sec rate, respectively, pressure $<1e^{-7}$;

Metal lift-off in AZ 400T stripper at 80 °C for 10 min.

(7) ALD cover layer deposition

ALD 25 nm Al_2O_3.

(8) Open window for contacting.

Spin on negative photoresist (AZ5214E),

Soft bake 1min at 110 °C;

Exposed by 320 nm UV lithography with optical photo mask for 10 s;

Reversal bake 115°C for 1 min;

Flood exposure for 2 mins;

Develop in MIF 917 developer for 40 s;

O_2 descum 2 min 500W for PR residual removal.

BOE etching for 2 mins.

(9) Ni and Au protection strips deposition.

Spin on image reversal photoresist (AZ5214E-IR);

Soft bake 1min at 110 °C;

Exposed by 320 nm UV lithography with optical photo mask for 10 s;

Reversal bake 1min at 115 °C;

Flood exposure for 2mins;

Develop in MIF 917 developer for 40 s;

O_2 descum for 6 mins at 500 W for PR residual removal;

5nm Ni, followed by 50 nm Au deposition by electron beam evaporation, with 0.2 Å/sec and 0.5 Å/sec rate, respectively, pressure $<1e^{-7}$;

Metal lift-off in AZ 400T stripper at 80 °C for 10 min.

(10) Open releasing window.

Spin on negative photoresist (AZ5214E);

Soft bake 1min at 110 °C;

Exposed by 320 nm UV lithography with optical photo mask for 10 s;

Reversal bake 115°C for 1 min;

Flood exposure for 2 mins;

Develop in MIF 917 developer for 40 s;

O_2 descum 2 mins at 500 W for PR residual removal;

BOE etching for 2 mins.

RIE processing for 3 mins;

Acetone, Methanol, Isopropanol strip PR;

O_2 descum 3 mins at 500 W for PR residual removal.

(11) Lateral etching for tube inductor unidirectional scrolling,

Etchant, H_2O_2 : citric acid = 25 : 1, at 71 °C.

Citric acid is citric acid monohydrate: H_2O = 100 g : 200 mL, stirred 12 hours.

APPENDIX B: AU S-RUM TRANSFORMER FABRICATION PROCESS

(1) Silicon wafer preparation.

Standard RCA clean, $NH_4OH : H_2O_2 : H_2O = 1 : 1 : 5$, at 80 °C, 10 min, $HF : H_2O = 1 : 100$, at room temperature, 1min, $HCl : H_2O_2 : H_2O = 1 : 1 : 5$, at 80 °C for 10 min, DI water raise, N_2 drying.

(2) Wet thermal oxidation.

1μm SiO_2, at 1150 °C for 2 hours.

(3) Sacrificial layer deposition.

20 nm Ge is deposited by electron beam evaporation, with 0.5Å/sec rate.

(4) SiN_x bilayer growth.

Dual-frequency STS-PECVD (Surface Technology Systems plc.) deposition;

300 °C platen, 240 °C showerhead;

20 nm LF SiN_x deposition, 380 KHz RF power, 20 W, $SiH_4 : NH_3 = 1 : 1$, 300 mT;

20 nm HF SiN_x deposition, 13.56 MHz RF power, 20 W, $SiH_4 : NH_3 = 4 : 5.5$, 900 mT.

(5) Define the rectangle tube patterns.

Spin on positive photoresist (AZ5214E);

Soft bake 1 min at 110°C;

Exposed by 320 nm UV lithography (297 W) with optical photo mask for 1 min;

Develop in MIF 917 developer;

O_2 descum 2 min 500 W for PR residual removal;

Reactive ion etching by CF4 – Etching through Ge and 50 nm down to SiO_2 for 4 mins;

Acetone, Methanol, Isopropanol strip PR;

O_2 descum 2 min 500W for PR residual removal.

(6) Au strips deposition.

Spin on image reversal photoresist (AZ5214E-IR);

Soft bake 1 min at 110 °C;

Exposed by 320 nm UV lithography with optical photo mask for 10 s;

Reversal bake 1min at 115 °C;

Flood exposure for 2 mins;

Develop in MIF 917 developer for 40 s;

O_2 descum for 2 mins at 500W for PR residual removal;

HCL for 2 min;

5 nm Ni, followed by 100nm Au deposition by electron beam evaporation, with 0.2 Å/sec and 0.5 Å/sec rate, respectively, pressure $<1e^{-7}$;

Metal lift-off in AZ 400T stripper at 80 °C for 10min.

(7) ALD cover layer deposition

ALD 25 nm Al_2O_3.

(8) Open window for contacting.

Spin on negative photoresist (AZ5214E),

Soft bake 1min at 110 °C;

Exposed by 320 nm UV lithography with optical photo mask for 10 s;

Reversal bake 115°C for 1 min;

Flood exposure for 2 mins;

Develop in MIF 917 developer for 40 s;

O_2 descum 2 min 500 W for PR residual removal.

BOE etching for 2 mins.

(9) Open releasing window.

Spin on negative photoresist (AZ5214E);

Soft bake 1min at 110 °C;

Exposed by 320 nm UV lithography with optical photo mask for 10 s;

Reversal bake 115 °C for 1min;

Flood exposure for 2 mins;

Develop in MIF 917 developer for 40 s;

O_2 descum 2 mins at 500 W for PR residual removal;

BOE etching for 2 mins.

RIE processing for 3 mins;

Acetone, Methanol, Isopropanol strip PR;

O_2 descum 3mins at 500 W for PR residual removal.

(10) Lateral etching for tube inductor unidirectional scrolling,

Etchant, H_2O_2 : citric acid = 25 : 1, at 71°C.

Citric acid is citric acid monohydrate: H_2O = 100 g : 200 mL, stirred 12 hours.

APPENDIX C: CODE FOR S-RUM INDUCTOR SIMULATION

```
clc;

clear;

turns=10; % number of turns

ws=30e-6; % width of strip

wc=30e-6; %width of connection line

lc=30e-6; %seperation distance between adjacent cells

dR=40e-9; % LF SiN thickness + HF SiN thickness

p=1.63*1.7e-8; %Resistivity

m0=4*pi*1e-7;

t=100e-9; % metal strip thickness

D=60e-6; % inner diameter

R1=D/2;

Lself=0;

epsin=7*8.85419*1e-12;

epsi=11.9*8.85419*1e-12;

tsi=500e-6; % substrate thickness

Csub=0*1e-15/(1e-6)^2;

N=2; % number of cells

f=40; % maximum freq.

sf=0.01; % freq. step


Length=0;
```

```
for i=1:turns
   Ri=R1+(i-1)*(dR+t)
   Length=2*pi*Ri+Length;
   De=log((Ri+t+sqrt(ws^2+Ri^2+2*Ri*t+t^2))/(Ri+sqrt(ws^2+Ri^2)))+(Ri+t)*sqrt((Ri+t)^2+w
s^2)/ws^2-Ri*sqrt(Ri^2+ws^2)/ws^2-t*(2*Ri+t)/ws^2;
   Lself=m0*pi*Ri^2/(2*t)*De+Lself;
end
Length
Lmutual=0;
for i=1:turns-1
   for j=i+1:turns
      Ri=R1+(j-1)*(dR+t);
      De=log((Ri+t+sqrt(ws^2+Ri^2+2*Ri*t+t^2))/(Ri+sqrt(ws^2+Ri^2)))+(Ri+t)*sqrt((Ri+t)^2
+ws^2)/ws^2-Ri*sqrt(Ri^2+ws^2)/ws^2-t*(2*Ri+t)/ws^2;
   Lmutual=2*pi*m0/2*(R1+(i-1)*(dR+t))^2/t*De+Lmutual;
   end
end
L=Lself+Lmutual

C=2*pi*epsin*ws/log(1+dR*(turns-1)/R1)/6;
Cp=ws*(R1+turns*t+(turns-1)*dR)*Csub/2;
Cc=wc*lc*Csub/2;
Cox=ws*(R1+turns*t+(turns-1)*dR)*epsi/1e-6;
```

```
M=0;
for i=1:turns
   Ri=R1+(i-1)*(dR+t);
   for j=1:turns
      Rj=R1+(j-1)*(dR+t);
      Dej=(lc+2*ws)^2*log((Rj+t+sqrt((Rj+t)^2+(lc+2*ws)^2))/(Rj+sqrt(Rj^2+(lc+2*ws)^2)))-...
         2*(lc+ws)^2*log((Rj+t+sqrt((Rj+t)^2+(lc+ws)^2))/(Rj+sqrt(Rj^2+(lc+ws)^2)))+...
         lc^2*log((Rj+t+sqrt((Rj+t)^2+lc^2))/(Rj+sqrt(Rj^2+lc^2)))+...
         (Rj+t)*sqrt((Rj+t)^2+(lc+2*ws)^2)-Rj*sqrt(Rj^2+(lc+2*ws)^2)-
2*(Rj+t)*sqrt((Rj+t)^2+(lc+ws)^2)+...
         2*Rj*sqrt(Rj^2+(lc+ws)^2)+(Rj+t)*sqrt(lc^2+(Rj+t)^2)-Rj*sqrt(lc^2+Rj^2);
      M=pi*m0*Ri^2/(4*t*ws^2)*Dej+M;
   end
end
Ld=0;
theta=(turns+1)*2*pi;
a=(R1+t+dR)/2/pi;
R=p/(ws*t)*(2*pi*turns*R1+pi*turns*(turns+1)*(t+dR));
Rtotal=R*N

ii=1;
for i=0.1:sf:f
   w=2*pi*1e9*i;
```

```
    Lp=L+Ld-2*(1-1/N)*M;
    Letotal(ii)=N*(R^2+w^2*Lp^2)*(Lp-C*(R^2+w^2*Lp^2))/(R^2+w^2*(Lp-
C*(R^2+w^2*Lp^2))^2)/1e-9;
    ii=ii+1;
end
i=0.1:sf:f;
plot(i,Letotal);
xlabel('Frequency (GHz)');
ylabel('Inductance (nH)');
Letotal=Letotal';
hold on
ii=1;
for i=0.1:sf:f
    w=2*pi*1e9*i;
    Lp=L+Ld-2*(1-1/N)*M;
    Q(ii)=w*(Lp-(C+N^2*(Cc+Cp))*(R^2+w^2*Lp^2))/R;
    ii=ii+1;
end
Q=Q';
figure
i=0.1:sf:f;
plot(i,Q);
xlabel('Frequency (GHz)');
```

```
ylabel('Q factor');

hold on

i=i';
```

APPENDIX D: CODE FOR S-RUM INDUCTOR RF TEST DE-EMBEDDING

```
clear

clc


SDUT_file = '2cellmiddlenarrow.s2p'; % change this to the name of the desired file

S_Z0 = 50; % system impedance


SDUT_data = read(rfdata.data,SDUT_file);

S_freq = SDUT_data.Freq; % measurement frequency vector

S_DUT = extract(SDUT_data,'S_PARAMETERS',S_Z0); % can also extract Z and Y

parameters

Y_DUT = s2y(S_DUT,S_Z0);

Z_DUT = s2z(S_DUT,S_Z0);


Sopen_file = 'opennarrow.s2p'; % change this to the name of the desired file

Open_Z0 = 50; % system impedance


Open_data = read(rfdata.data,Sopen_file);

Open_freq = Open_data.Freq; % measurement frequency vector

SS_Open = extract(Open_data,'S_PARAMETERS',Open_Z0); % can also extract Z and Y

parameters

Y_Open = s2y(SS_Open,Open_Z0);
```

```
Sthru_file = 'thru.s2p'; % change this to the name of the desired file
Thru_Z0 = 50; % system impedance

Thru_data = read(rfdata.data,Sthru_file);
Thru_freq = Thru_data.Freq; % measurement frequency vector
S_Thru = extract(Thru_data,'S_PARAMETERS',Thru_Z0); % can also extract Z and Y
parameters
Y_Thru = s2y(S_Thru,Thru_Z0);

Y_DUTOpen = Y_DUT-Y_Open;
Z_DUTOpen = y2z(Y_DUTOpen);
Y_ThruOpen = Y_Thru-Y_Open;
Z_ThruOpen = y2z(Y_ThruOpen);

% pre-initialization, saves memory, runs faster
Zadj_DUT = zeros(size(Z_DUTOpen));
Yadj_DUT = zeros(size(Z_DUTOpen));
Sadj_DUT = zeros(size(Z_DUTOpen));
L = zeros(length(S_freq),1);
R = zeros(length(S_freq),1);
Q = zeros(length(S_freq),1);
Yp = zeros(length(S_freq),1);
```

```
Zp = zeros(length(S_freq),1);

Cs = zeros(length(S_freq),1);

Rs = zeros(length(S_freq),1);


%calculation loop

for i = 1:length(S_freq)

   Zdet = Z_ThruOpen(1,1,i)+Z_ThruOpen(2,2,i)-Z_ThruOpen(2,1,i)-Z_ThruOpen(1,2,i);

   Zadj_DUT(:,:,i) = Z_DUTOpen(:,:,i) - Zdet/2.*eye(2);

   Yadj_DUT(:,:,i) = z2y(Zadj_DUT(:,:,i));

   Sadj_DUT(:,:,i) = y2s(Yadj_DUT(:,:,i));

   L(i) = imag(-1/Yadj_DUT(2,1,i)/(2*pi*S_freq(i)));

   R(i) = real(-1/Yadj_DUT(2,1,i));

   Q(i) = -imag(Yadj_DUT(1,1,i))/real(Yadj_DUT(1,1,i));

   ImYadj(i)= -imag(Yadj_DUT(1,1,i));

   ReYadj(i)=real(Yadj_DUT(1,1,i));

   Yp(i)=Yadj_DUT(1,1,i)+Yadj_DUT(1,2,i);

   Zp(i)=y2z(Yp(i));

   Cs(i)=imag(Yp(i))/2/pi/S_freq(i);

   Rs(i)=real(Zp(i));

end

adjs2p=zeros(length(S_freq),9);

adjs2p(:,1)=S_freq;

for i=1:length(S_freq)
```

```
    adjs2p(i,2)=real(Sadj_DUT(1,1,i));
    adjs2p(i,3)=imag(Sadj_DUT(1,1,i));
    adjs2p(i,4)=real(Sadj_DUT(1,2,i));
    adjs2p(i,5)=imag(Sadj_DUT(1,2,i));
    adjs2p(i,6)=real(Sadj_DUT(2,1,i));
    adjs2p(i,7)=imag(Sadj_DUT(2,1,i));
    adjs2p(i,8)=real(Sadj_DUT(2,2,i));
    adjs2p(i,9)=imag(Sadj_DUT(2,2,i));
end
% ImYadj=ImYadj';
% ReYadj=ReYadj';
% plot(S_freq/1e9,ImYadj);
% figure
% plot(S_freq/1e9,ReYadj);
% % plots each on its own figure
plot(S_freq/1e9,L/1e-9)
xlabel('Frequency (GHz)');
ylabel('Inductance (nH)');
figure
plot(S_freq/1e9,R)
xlabel('Frequency (GHz)');
ylabel('Resistance (ohms)');
figure
```

```
plot(S_freq/1e9,Q)
xlabel('Frequency (GHz)');
ylabel('Q');
figure
plot(S_freq/1e9,Cs/1e-15);
xlabel('Frequency (GHz)');
ylabel('Cs(fF)');
figure
plot(S_freq/1e9,Rs);
xlabel('Frequency (GHz)');
ylabel('Rs (Ohm)');
s11=S_DUT(1,1,:);
fig=figure;
smithchart(s11(:));
title('Before de-embed');
s11adj=Sadj_DUT(1,1,:);
fig=figure;
smithchart(s11adj(:));
```

APPENDIX E: CODE FOR S-RUM TRANSFORMER RF TEST DE-EMBEDDING

```
clear
clc

SDUT_file = 'sample36.s2p'; % change this to the name of the desired file
S_Z0 = 50; % system impedance

SDUT_data = read(rfdata.data,SDUT_file);
S_freq = SDUT_data.Freq; % measurement frequency vector
S_DUT = extract(SDUT_data,'S_PARAMETERS',S_Z0); % can also extract Z and Y
parameters
Z_DUT = s2z(S_DUT);
Y_DUT = s2y(S_DUT);

Sopen_file = 'open1.s2p'; % change this to the name of the desired file
Open_Z0 = 50; % system impedance

Open_data = read(rfdata.data,Sopen_file);
Open_freq = Open_data.Freq; % measurement frequency vector
SS_Open = extract(Open_data,'S_PARAMETERS',Open_Z0); % can also extract Z and Y
parameters
Y_Open = s2y(SS_Open,Open_Z0);
```

```
Sthru_file = 'thru_transformer1.s2p'; % change this to the name of the desired file
Thru_Z0 = 50; % system impedance

Thru_data = read(rfdata.data,Sthru_file);
Thru_freq = Thru_data.Freq; % measurement frequency vector
S_Thru = extract(Thru_data,'S_PARAMETERS',Thru_Z0); % can also extract Z and Y
parameters
Y_Thru = s2y(S_Thru,Thru_Z0);

Y_DUTOpen = Y_DUT-Y_Open;
Z_DUTOpen = y2z(Y_DUTOpen);
Y_ThruOpen = Y_Thru-Y_Open;
Z_ThruOpen = y2z(Y_ThruOpen);

% pre-initialization, saves memory, runs faster
Zadj_DUT = zeros(size(Z_DUTOpen));
Lp = zeros(length(S_freq),1);
Ls = zeros(length(S_freq),1);
M = zeros(length(S_freq),1);
k = zeros(length(S_freq),1);
Rs = zeros(length(S_freq),1);
```

```
%calculation loop
for i = 1:length(S_freq)
    Zdet = Z_ThruOpen(1,1,i)+Z_ThruOpen(2,2,i)-Z_ThruOpen(2,1,i)-Z_ThruOpen(1,2,i);
    Zadj_DUT(:,:,i) = Z_DUTOpen(:,:,i) - Zdet/2.*eye(2);
    Yadj_DUT(:,:,i) = z2y(Zadj_DUT(:,:,i));
    Sadj_DUT(:,:,i) = y2s(Yadj_DUT(:,:,i));
    L(i) = imag(-1/Yadj_DUT(2,1,i)/(2*pi*S_freq(i)));
    R(i) = real(-1/Yadj_DUT(2,1,i));
    Q(i) = -imag(Yadj_DUT(1,1,i))/real(Yadj_DUT(1,1,i));
    Lp(i) = imag(Zadj_DUT(1,1,i))/(2*pi*S_freq(i));
    Ls(i) = imag(Zadj_DUT(2,2,i))/(2*pi*S_freq(i));
    M(i)=sqrt(imag(Zadj_DUT(2,1,i))*imag(Zadj_DUT(1,2,i)))/(2*pi*S_freq(i));
    Rp(i)=real(Zadj_DUT(1,1,i)-Zadj_DUT(2,1,i));
    Rs(i)=real(Zadj_DUT(2,2,i)-Zadj_DUT(1,2,i));
    k(i)=M(i)/sqrt(Lp(i)*Ls(i));
    Qp(i)=imag(Zadj_DUT(1,1,i))/real(Zadj_DUT(1,1,i));
    Qs(i)=imag(Zadj_DUT(2,2,i))/real(Zadj_DUT(2,2,i));
    kim(i)=sqrt(imag(Zadj_DUT(1,2,i))*imag(Zadj_DUT(2,1,i))/(imag(Zadj_DUT(1,1,i))*imag(Z
adj_DUT(2,2,i))));
    kre(i)=sqrt(real(Zadj_DUT(1,2,i))*real(Zadj_DUT(2,1,i))/(real(Zadj_DUT(1,1,i))*real(Zadj_
DUT(2,2,i))));
    x(i)=(1-kre(i)^2)/(kim(i)^2*Qp(i)*Qs(i)+kre(i)^2);
    eta(i)=1+2*(x(i)-sqrt(x(i)^2+x(i)));
```

```
    eta2(i)=1/(1+2*sqrt((1+1/(Qp(i)*Qs(i)*k(i)^2))*(1/(Qp(i)*Qs(i)*k(i)^2)))+2/(Qp(i)*Qs(i)*k(i)
^2))
end
    eta=eta';
% adjs2p=zeros(length(S_freq),9);
% adjs2p(:,1)=S_freq;
% for i=1:length(S_freq)
%     adjs2p(i,2)=real(Sadj_DUT(1,1,i));
%     adjs2p(i,3)=imag(Sadj_DUT(1,1,i));
%     adjs2p(i,4)=real(Sadj_DUT(1,2,i));
%     adjs2p(i,5)=imag(Sadj_DUT(1,2,i));
%     adjs2p(i,6)=real(Sadj_DUT(2,1,i));
%     adjs2p(i,7)=imag(Sadj_DUT(2,1,i));
%     adjs2p(i,8)=real(Sadj_DUT(2,2,i));
%     adjs2p(i,9)=imag(Sadj_DUT(2,2,i));
% end

figure
plot(S_freq/1e9,Lp/1e-9)
xlabel('Frequency (GHz)');
ylabel('Primary Inductance (nH)');
figure
plot(S_freq/1e9,Rp)
```

```
xlabel('Frequency (GHz)');
ylabel('Rp');
figure
plot(S_freq/1e9,Rs)
xlabel('Frequency (GHz)');
ylabel('Rs');
figure
plot(S_freq/1e9,Ls/1e-9)
xlabel('Frequency (GHz)');
ylabel('Secondary Inductance (nH)');
figure
plot(S_freq/1e9,M/1e-9)
xlabel('Frequency (GHz)');
ylabel('Mutual Inductance (nH)');
figure
plot(S_freq/1e9,k)
xlabel('Frequency (GHz)');
ylabel('Coupling coefficient');
fig=figure;
plot(S_freq/1e9,eta2)
xlabel('Frequency (GHz)');
ylabel('Efficiency');
```

```
for i=1:length(S_freq)
    s21(i)=20*log10(abs(S_DUT(2,1,i)));
end
fig=figure;
plot(S_freq/1e9,s21)
xlabel('Frequency (GHz)');
ylabel('S21(dB)');

s11=S_DUT(1,1,:);
fig=figure;
smithchart(s11(:));
title('Before de-embed');
% s11adj=Sadj_DUT(1,1,:);
% fig=figure;
% smithchart(s11adj(:));
% hold on
% s12adj=Sadj_DUT(1,2,1:1000);
% smithchart(s12adj(:));
```