# SPARKING AN INCREASE IN VOLUMETRIC AND SPECIFIC DENSITY FOR POWER CONVERTERS WITH AVANT-GARDE THERMAL MANAGEMENT STRATEGIES, TOPOLOGIES, AND PACKAGING SCHEMES

BY

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DISSERTATION

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# ABSTRACT

*To accept phase-change or not, that is the question.*
*Whether 'tis nobler in mind to suffer the aches and pains*
*of single-phase cooling or by latent heat end them.*
*Ay, there's the rub!*
– Translation of Shakespeare's *Hamlet, II, i* by Thomas Foulkes

Increasing electrification of mechanically controlled or driven systems has created a demand for the development of compact, lightweight electronics. Removing waste heat from these high volumetric and gravimetric power dense assemblies, especially in mobile applications, requires a thorough understanding of the loss mechanisms for each component and non-traditional thermal management strategies with high heat flux potential. After summarizing the current achievements for both power component loss characterization and the direct cooling of electronics with liquid vapor phase-change, this dissertation highlights the development and validation of an electro-thermal testbed for demonstrating the enhanced, directed cooling of the densely packaged power electronics.

*It is not the critic who counts; not the man who points out how the strong man stumbles, or where the doer of deeds could have done them better. The credit belongs to the man who is actually in the arena, whose face is marred by dust and sweat and blood; who strives valiantly; who errs, who comes short again and again, because there is no effort without error and shortcoming; but who does actually strive to do the deeds; who knows great enthusiasms, the great devotions; who spends himself in a worthy cause; who at the best knows in the end the triumph of high achievement, and who at the worst, if he fails, at least fails while daring greatly...*

– Theodore Roosevelt, 1858-1919

*To my parents, Jim and Beth Foulkes, for their unconditional love, sage advice, and inspiration to be persistent and to ask questions. I have benefited from both a Liberal Arts and Scientific education. My thesis reflects this unique and diversified background as I have had a similarly unique and diversified experience at the University of Illinois at Urbana-Champaign. I have had the opportunity to delve into two specialty areas of electrical and mechanical engineering. I was fortunate to contribute to many projects in both of these areas. As a result, my thesis reflects and highlights, through prose, my journey over the past five years.*

*To Zelma and Herbert Bailey, for starting me down this path.*

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Delphi Electronics and Safety in Kokomo, Indiana, had a profoundly positive impact on my desire to pursue a career in research and design. The kindness and friendly atmosphere at Delphi were truly special and enabled me to learn from a wide variety of challenging and meaningful projects. Specifically, sage advice from Ralph Taylor, Brian Denta, Kwan Shim, and Yansong Chen was instrumental in my decision to pursue graduate study in the cross-disciplinary field of power electronics. Moreover, I am appreciative of the career advice and technical development opportunities made available to me during an internship at NASA Glenn Research Center by Ralph Jansen, Cheryl Bowman, Randy Bowman, and David Avanesian. This propelled me into my second year of graduate studies.

Similarly, I received a fantastic foundation in technical communication and critical thinking during my high school education. I would like to thank Julia Thistle and Katherine Utley for developing a world-class language arts and honors writing program. Throughout my Science Fair career, I received advice, guidance, and inspiration from many wonderful educators including: Glenn Cook, Annie Bauer, Nancy Mottel, and Howard McLean. From developing engaging class activities such as taste-and-texture labs to volunteering their time with my research projects, these educators went above and beyond to help me succeed, and inspired me to pursue a career in engineering. I am also fortunate to have received superlative advice at a young age about the importance of solving the "big problems" facing our society from my neighbor and friend, Dr. Herbert Bailey, who bartered his insights about mathematics for help with his lawn care.

In addition to offering courses with some of the most innovative engineering educators in the world, Rose-Hulman also fostered a unique culture where faculty had the time and interest to work on independent research projects. In truth, many of the most valuable lessons from my undergraduate education as an engineer came from these independent research experiences. I am eternally grateful to Dr. Maarij Syed for allowing me to join his research lab during the start of my freshman year at Rose-Hulman. I learned a great deal about the best practices of research, design, and communication during our four years of research. Most importantly, Dr. Syed worked tirelessly behind the scenes by, for example, traveling to campus over breaks so that I could

work in the lab and facilitating many unique opportunities for me such as presenting at several international conferences. This foundation has been instrumental to my success throughout my graduate studies. Moreover, I am very appreciative that Dr. Diane Evans took time to discuss probability and statistics when I wandered into her office seven years ago. Her boundless enthusiasm for both research and teaching has been a constant source of inspiration toward pursuing a graduate degree. Furthermore, Dr. Daniel Moore, Dr. Marc Herniter, Dr. Niusha Rostamkolai, Dr. Ed Doering, and Dr. Robert Throne in the Electrical and Computer Engineering Department and Dr. Roger Lautzenheiser and Dr. Elton Graves from the Mathematics Department always went the extra mile to help me expand my horizons and to challenge me with rigorous end-of-quarter projects during my four years at Rose-Hulman. Moreover, I want to thank Alicia Cross-Engelhardt and Dana Engelhardt for welcoming me to the Urbana-Champaign community. All in all, many people in addition to those listed here, such as the staff at Rose-Hulman or my friends from the community, have also had a significant impact on my pursuit of graduate studies.

My graduate education benefited immensely from participating in entrepreneurial accelerators both locally such as the UIUC Technology Entrepreneurship Center and nationally including the VentureWell E-Team and NSF I-Corps programs. When I was a student and later an instructor for TE461 (Technology Entrepreneurship) and TE566 (Finance for Engineering Startups), Dr. Lilly empowered me to learn how to translate my ideas into impact via customer discovery and business development. I also was inspired by his engaging teaching style. I learned a great deal from working with Karl Reinhard and Edmond Rogers through the national NSF I-Corps summer 2019 cohort as we successfully explored the commercialization of technology to modernize the US power grid. I am also grateful to the advice from David D'Angelo, my VentureWell program manager, as I have examined the commercialization of heat transfer solutions for large electrical loads like data centers.

I would not have been able to finish my thesis if my dear friend Peter Sokalski had not acted quickly when my appendix burst on a return flight from a conference only seven weeks before my defense. I am eternally grateful

to Peter as well as the surgeons and nurses at Resurrection Hospital in Chicago who returned me to the land of the living.

# TABLE OF CONTENTS

# CHAPTER 1

# THESIS ROADMAP

> *If you're doing an experiment, you should report everything that you think might make it invalid, not only what you think is right about it; other causes that could possibly explain your results; and things you thought of that you've eliminated by some other experiment, and how they worked to make sure the other fellow can tell they've been eliminated. Details that could throw doubt on your interpretation must be given, if you have them. You must do the best you can if you know anything at all wrong, or possibly wrong, to explain it...In summary, the idea is give all of the information to help others judge the value of your theory, not just the information that leads to judgment in one particular director or another.*
>
> – Richard Feynman, 1918-1988 (Nobel Prize 1965)

A reading from the second letter[1] of Thomas to the Urbanans and Champaignites

Brothers and Sisters: Rejoice and be glad. I say it again, rejoice! For it is written, "Man shall not graduate on experimental evidence and theoretical analysis alone, but on every word that comes forth in his doctoral thesis." As an outline, this chapter serves as a lamp for your feet, a light on your path as we retrace my journey through graduate school. Let us embark on this quest together with the logic of Cicero, but the style of Plautus,

Something familiar, something peculiar;
Something for everyone, a thesis tonight!

Like many classical texts composed by our friends Homer and Virgil, Chapter 2 catalogs the origins of power electronics by examining what begot what and who begot or inspired whom. This historical examination reveals the importance of power factor correction and electric machines for the intriguing evolution of power converters.

Nothing with kings, nothing with crowns;
If you approve the thesis, Tom gets a gown!

[1]For the first letter, the interested reader should refer to [1].

The operational principles of different topologies and key loss mechanisms for power converters summarized in Chapter 3 are the chief cornerstone of this discussion. If compact converters herald an electrified Xanadu, then heat is the great salesman of what Milton warns could be a paradise lost.

High heat flux appealing, system implications appalling;
Something for everyone, a thesis tonight!

Chapter 4 surveys the state-of-the-art for high heat flux methods of mitigating heat and articulates why these techniques are insufficient for ensuring that heat blazing from the midst of densely packed electronics does not consume the power converter.

Old situations, new complications;
Something for everyone, a thesis tonight!

Channeling Shakespeare, Chapter 5 explores why power density is the thing wherein we'll catch the conscious of more than just the king. A parable about more-electric aircraft elucidates the paramount importance of power density for both systems and society.

Losses with disguises, stunning surprises!
Something for everyone, a thesis tonight!

Building on this foundation, the examination of loss mechanisms for wide-bandgap, gallium-nitride (GaN) transistors during high voltage switching and extreme cold environments are topics of Chapters 6 and 7 respectively.

Ambient measurements erratic, heat flux limits dramatic!
Something for everyone, a thesis tonight!

The benefits of and obstacles to removing this heat with liquid-vapor, phase-change are first introduced in Chapter 8 with a derivation and discussion of the theoretical limits for the maximum heat flux of jumping droplet condensation.

Nothing with gods, nothing with fate;
Jumping droplet cooling will just have to wait!

Insights shared in Chapter 9 from experiments regarding the directed cooling of GaN transistors with jumping droplets in vacuum conditions support the observations from the theoretical analysis about the physical obstacles limiting the experimental performance of jumping droplet condensation.

The PCB aesthetic, the boiling frenetic;
Something for everyone, a thesis tonight!

Just as Henley and Huxley speak of the unconquerable soul of man, Chapter

10 highlights how, as master of my fate with head unbowed, I forged a path into a brave new world of directed, electronics cooling with liquid-vapor phase-change. Realizing the origins of the limitations for jumping droplet condensation, I demonstrate a new thermal management technique combining confined boiling with self-assembled liquid bridges.

This time it all turns out alright;

Something for everyone, a thesis tonight!

After examining the fundamental physics governing this phenomenon and demonstrating ultra-high heat flux cooling of GaN devices, Chapter 11 underscores how these lessons from directed single- and two-phase cooling can realize improvements in power density and specific power via integration with a larger scale electronics system. A fair benchmark of performance against a state-of-the-art cold plate and a side-by-side comparison and contrast of this avant garde thermal management scheme against the traditional cooling technologies are made.

No royal curse, no Trojan Horse;

And there's a happy ending of course!

Chapter 12 closes this discussion in the example of the youngest apostle, John, by "reminding you of everything I have said to you." All in all, this first chapter as the late Justice Antonin Scalia once quipped, "...is kind of like the first pancake. If it's not perfect, that's OK. There are a lot more coming along."

Open up the curtain, a thesis, TONIGHT!

# CHAPTER 2

# HISTORICAL ORIGINS OF POWER ELECTRONICS

***William Gladstone, British Chancellor of the Exchequer****, "What is the practical value of electricity?"*
***Michael Faraday****, "Why, sir, there is every probability that you will soon be able to tax it."*
– Conversation from "Democracy and Liberty" by W. Lecky (1899)

## 2.1 Introduction

Seventy-five years ago, Alexanderson and Phillip from General Electric published the first paper [2] cataloging the historical evolution and provide a definition of what they referred to as the "Electronic Power Converter." Figure 2.1 highlights the four types of power converters created for driving motor drives, transmitting power in both ac and dc grids, and changing the waveform frequency for loads and generators connected together while operating at different frequencies [2–5]. This chapter underscores the co-evolution of power electronics with two major industrial applications: motor drives and power factor correction (PFC).

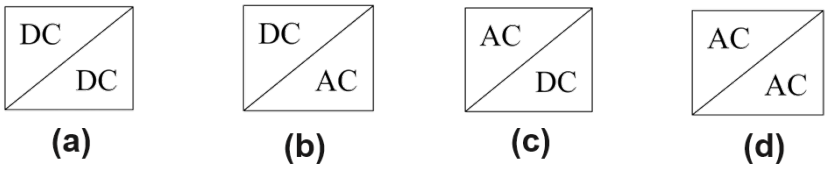


Figure 2.1: Four types of power electronics include (a) dc-dc conversion for the increase or decrease in the magnitude of direct voltage and current, (b) inversion for the transformation of direct to alternating voltage and current, (c) rectification for the conversion of alternating to direct voltage and current, and (d) cycloconversion for the shifting of frequency for alternating waveform.

## 2.2 Co-Evolution of Electric Machines & Power Electronics

Examining the intertwined development of electric machines and power electronics first requires an understanding of the explosive innovation in the field of power and energy that existed during the nineteenth century.

### 2.2.1 Brief History of Electric Machines

During the Industrial Revolution, the pace of fundamental and applied scientific discovery around the globe was truly unbridled. This rapid progress was in part due to expansion of global trade between Europe and colonies around the world, which sparked massive growth of mass manufacturing in industries ranging from textiles to pottery. Similarly, communication about technical and scientific progress also started to spread more rapidly around the world. In addition to providing lectures at royal scientific societies across Europe and the colonies, professional, hobbyist, and gentleman scientists of this era met locally to collaborate and to share ideas in forums such as the famed Lunar Society of Birmingham. These gatherings for technical exchange sparked many famous discoveries from this era like James Watt's steam engine, and interestingly enough, also the American Thomas Davenport's development of the first practical and patented electric machine in 1834.

The exciting path from theory to practice for electric machines actually started fourteen years earlier in Denmark [6]. In 1820, Hans Orsted observed that current passing through a wire influenced the direction of the needle on a magnetic compass. He observed that reversing the direction of current would also cause the direction of the needle to change. This discovery by Orsted, that magnetic field existed around moving charge, catalyzed intense interest around the world in this new field of electromagnetic theory. A few months later, Andre Ampere in France repeated Orsted's experiments with great interest. Ampere then contributed to the field by implementing an experiment where he could control the direction of current in two parallel wires independently and measure the force between them [6]. During this experiment, Ampere realized that, depending on the direction of current in these parallel wires, the wires would either repel or attract.

In 1821, the great British experimentalist Michael Faraday combined the observations of Orsted and Ampere to create the first demonstration of

motion due to electromagnetics [6, 7]. Although Faraday was able to get a wire carrying current to rotate around a bar magnet, this was not the first electric machine because it did not convert electrical energy into mechanical energy for a useful purpose. Nevertheless, this was a very important discovery in the history of electric machines. Joseph Henry from the United States was also working on developing experimental demonstrations to better understand electromagnetics. In 1827, Henry realized that he could increase the strength of his electromagnets by adding additional turns. In order to layer the windings, Henry was the first to add insulation for the wire [6, 8]. This early insulation involving cotton or silk might seem strange today, but, for the voltage and power levels being considered, this insulation was sufficient for Henry and was a major contribution to the future practical fabrication of electric machines. Henry's first 2" (5.08 cm) square horse-shoe electromagnet was composed of 960 feet (292.6 m) of copper bell wire and stood 9.5" (24.13 cm) tall.

Interestingly enough, Thomas Davenport, a blacksmith with limited formal education, attended a public scientific demonstration in 1833 where Henry's electromagnetics lifted a 760 pound piece of iron and was immediately mesmerized by the potential of electromagnetics for practical applications [6, 8]. Like Jack of "Jack and the Beanstalk", Davenport persuaded his brother to sell their metalworking assets in order to purchase a working electromagnet and the materials to create additional electromagnets. After implementing numerous experiments, Davenport succeeded in creating the first practical DC electric machine in 1834 due to his invention of a mechanical commutator that could change the direction of current in the rotor electromagnets so that they would experience force from the fixed polarity stator magnets and the rotor would spin. Yet, during his lifetime, Davenport was never able to benefit financially from his patented electric machine because he was unable to get the torque and power levels high enough to compete with steam powered systems due to the quality and energy density of batteries available at this time [6].

Independently around the globe in Russia, Moritz-Hermann De Jacobi received money in from the Czar in late 1834 to construct a motor that could propel a boat [6]. De Jacobi also developed a mechanical commutator for his electric machine and was able to propel the boat successfully. Although De Jacobi's motor could spin significantly faster and produce much more torque

than Davenport's machine, De Jacobi's demonstration of the motor driving a boat was hampered by the weight of the batteries required to power the machine, which caused the boat to only travel approximately 3 miles per hour [6, 9]. Thus, in the case of Davenport and De Jacobi, the concept of creating useful mechanical work from electromagnetics was visionary and the technology was very ahead of its time. Interestingly enough, this historical survey has highlighted that system-level integration issues were a significant obstacle to the early acceptance of electric machines. Just like Davenport and De Jacobi, modern machine designers have to consider not only the size, weight, and efficiency of the electric machine, but also the complete system such as the drive, control, and energy source (e.g. batteries) in order for electrification of traditionally mechanical systems to be successful.

### 2.2.2 Intertwined Progress of Motors and Drives

Regarding the development of electric drives over the last century, a clear decreasing trend exists in total volume of the power electronics drive as shown in Figure 2.2 [10–17]. Between the 1930s and 1970s [10, 12–14] as well as between the 1970s and 1990s [11, 15, 16], orders of magnitude reduction in the combined machine and power electronics drive volume were observed due to significant changes in the electric machine, the power electronics, and control approaches. Without a doubt, a significant contributing factor to the slope of this trend involves the co-evolution of power electronic switching devices. Transitioning from mechanical commutation to electrical commutation starting in the 1930s [12, 13] offered drive designers the opportunity for enhanced control of industrial drives comprising networks of ignitrons and thyratrons in a current source inverter (CSI) topology. Thyratrons had the high efficiency common for mercury cathode one-way vacuum tubes combined with the convenience and controllability of three-electrode vacuum tubes [18]. The bulky nature of the thyratrons (i.e. 18" (45.7 cm) in length and 5" (12.7 cm) in maximum diameter for the bulb) clearly limited the power density of the early drives. Interestingly, the utility of rectification and inversion was quickly realized in the marketplace for example with locomotive inverters operating with a 9 kV dc bus and 20 MW power levels by the mid-1930s [2]. Eventually silicon controlled rectifiers

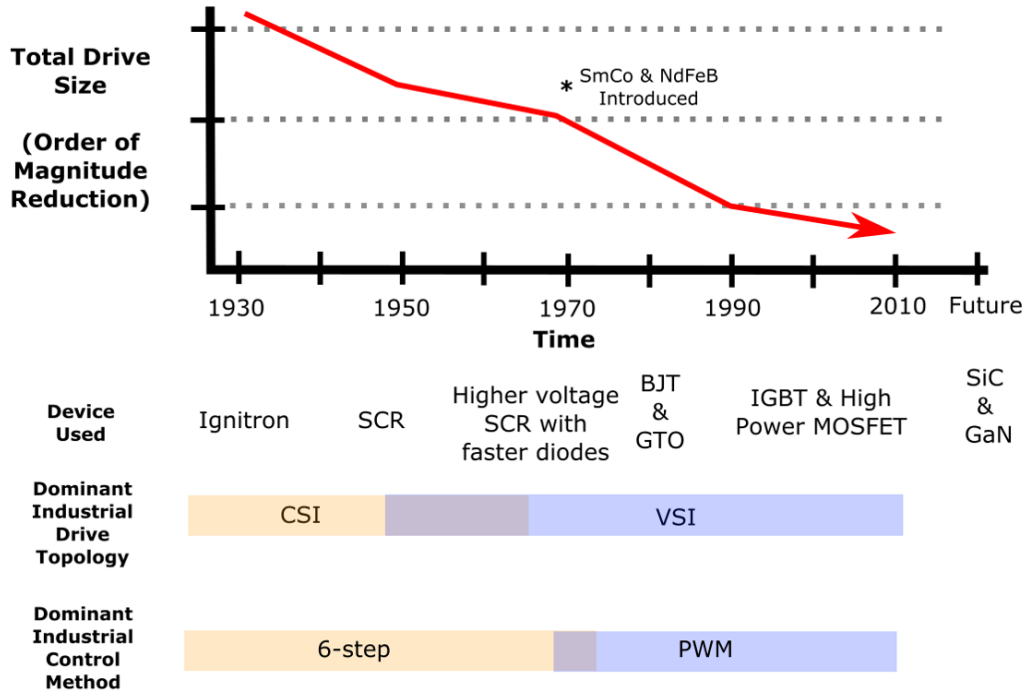


Figure 2.2: Technological advancement in power switching devices has had a profound impact on the development of electric machines, drives, and control techniques over the last century. Data synthesized from [11, 13, 14].

(SCR) and thyristor in 1957 [10, 12, 13, 19, 20] enabled the development and deployment of higher power and more compact inverters. As SCRs and thyristors improved, a new type of drive topology involving voltage source inverters (VSI) was developed. While CSIs keep the bus current constant and allow the voltage to vary with the winding impedance, VSIs maintain a fixed bus voltage and allow the winding current to change with winding impedance. VSIs became the dominant drive topology once fast enough freewheeling diodes were developed to prevent current flow from being interrupted during the deadtime of the switching transition between switches in the same leg of the inverter [11–13]. While CSIs are naturally short-circuit protected, VSIs need this deadtime to prevent large shoot-through currents from destroying the drive if both switches in a leg of the inverter are conducting at the same time.

Moreover, as power electronics switching devices were able to turn on and off faster with the introduction of the power bi-polar junction transistor (BJT), insulated gate bi-polar transistor (IGBT), and power metal–oxide semiconductor field-effect transistor (MOSFET), the switching losses in VSIs

dramatically improved [11–13, 19] and enabled the development of modern[1] hybrid-electric and all-electric powertrains for mobile vehicles[2] [30–33]. This contributed significantly to the improvement in power density for the entire drive. Interestingly, the transition from traditional 6-switch control schemes to more advanced pulse-width modulation (PWM) was also underscored as an important contributor to power density improvements by enabling the reduction in the size of filtering elements in the drive and improvements in the control of synchronous machines [11–15]. This survey can be expanded in the future to also capture the impact of the co-evolution of materials used to fabricate electric machines. For example, the introduction of samarium–cobalt (SmCo) and neodymium iron noron (NdFeB) magnets in the 1970s enabled the flux density of permanent magnetic machines to improve significantly [17]. This has enabled the synchronous permanent magnetic machine steadily to increase its prevalence and replace the wound dc machines in most high-performance applications. Moving forward, some suggest that wide-bandgap semiconductors might enable a renaissance for the current source inverter [34] or the increased industry acceptance of modern control techniques to further reduce losses for both the motor and drive compared to the classic PWM control scheme.

[1]While the EV1 released in 1996 was the first mass-produced all-electric vehicle, the first all-electric vehicles existed back at the end of the nineteenth century. Werner von Siemens' electric streetcar in 1879 is identified as one of the first examples of electrification [21–24]. One of the first feasible fully electric carriages with an energy density of 27 Wh/kg drove onto the scene in 1881 based on the design of French engineers Charles Jeantaud and Camille Faure [21,23]. President Woodrow Wilson is famous for having enjoyed rides down Pennsylvania Avenue in either the Milburn Light Electric or the Baker Queen Victoria Electric cars both housed at the White House [21, 23, 25]. A vast majority of electric cars were driven by women like First Lady Edith Wilson, who piloted the presidential automobile, since they did not require a hand crank to start. Unfortunately, broad market acceptance of electric automobiles was hindered by the limited range due to the low energy density of batteries, Charles Kettering's invention of the electric starter in 1912, and poor rural electrification at this time in the United States [23,25,26]. With regard to the curious history of electric vehicles, Gijs Mom [23] quips that, "the reputation of the electric vehicle lived off the imperfections of the gasoline engine and survived for niche applications where the battery's low energy density, high mass, and low range on one charge were not critical."

[2]Even the NASA Apollo Mission Lunar Roving Vehicle had PWM controlled, oversized silicon power transistors to drive the brushless dc motors in each wheel from its own battery pack [27–29]. This series, fully-electric powertrain architecture was the foundation for the all of the Apollo lunar vehicles (i.e. Apollo 15, 16, and 17) [27–29].

## 2.3 Importance of Power Factor Correction

As in electric machines, power quality and the need to regulate power factor have been key drivers in the growth and development of power electronics.[3] Figure 2.3 highlights, from a survey of published United States patents, how the number of new PFC methods has continued to grow over the past century. At the turn of the twentieth century, Westinghouse engineers worked diligently to tackle the control of induction machines and polyphaser power systems. Poor power factor from both reluctance and harmonics plagued the nascent ac power system by limiting transmission distances (e.g. in some cases less than 10 miles) and over-heating electric machines due to extra losses. Insights from long hours in the lab spurred Charles Legeyt Fortescue, the father of phasor analysis, to file a landmark patent, US1284293A, about single-phase PFC in 1916 [36] and refine his analysis for the general

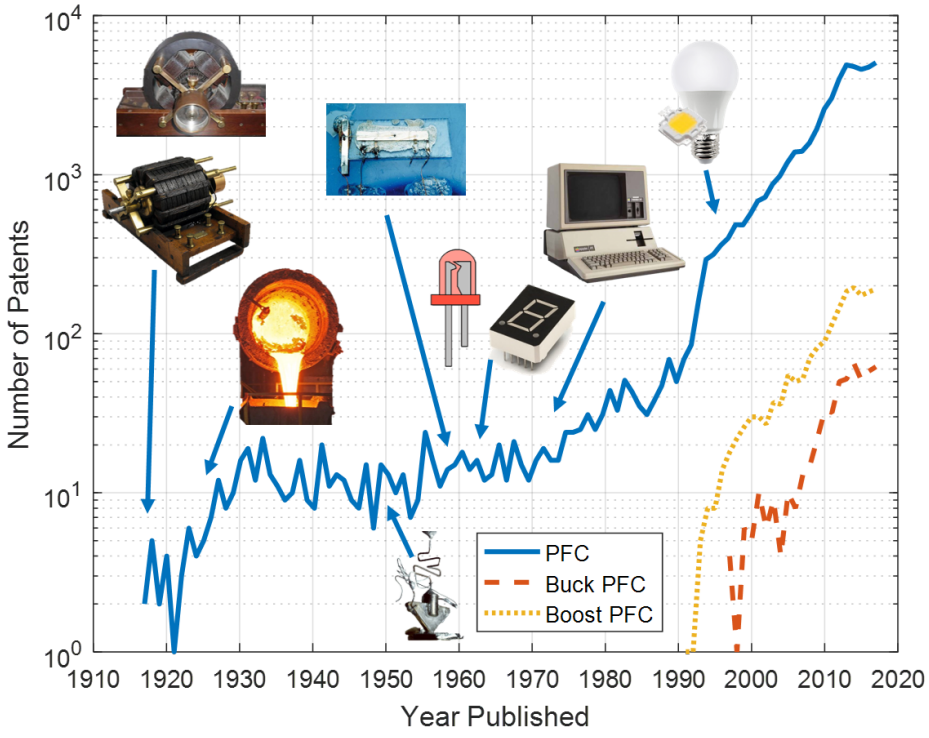


Figure 2.3: Progress related to the control of power factor has catalyzed innovation in power electronics.

[3] Legislative regulation regarding ac mains power quality started in 1889 due to flickering of lights in the early power grid [35].

theory of phasors [37]. With this foundation, early inverters [38, 39] and rectifiers [40, 41] in the 1920s composed of mercury-vapor vacuum tubes were deployed commercially to resolve power factor problems in the field. After addressing the needs of power generation and large-scale manufacturing plants like steel mills, the next major advancement for power factor correction would not occur until the invention of the three-electrode, point-contact transistor by Bardeen and Brattain[4] in 1947 [44] and the development of the integrated circuit by Jack Kilby in 1959 [45]. At both low and high power scales, the integration of transistors enabled a massive increase of systems connected in large networks, and therefore, power quality issues.[5] The commercial success of consumer electronics like computers[6] along with the adoption of more advanced lighting technology like CFL[7] and LED[8] were two additional sources of power quality issues on a large scale that required the development of compact, efficient PFC circuits. Both boost and buck PFC were developed to resolve these customer needs and satisfy grid-level power quality regulations.

## 2.4 Conclusion

The growth of the power electronics discipline has clearly been a case of "market-pull" as practitioners work to address the needs of their customers. Unlike in many areas of electrical engineering, industrial research and development in the field of power electronics historically has been ahead of academic work with some notable exceptions such as [51–68]. Taking into account the generalized method for predicting power converter topologies

[4]It is well established that Shockley was not involved in the experiments resulting in the discovery of the transistor [42, 43].

[5]IEC 555-2 established in 1978 required PFC circuits for all consumer products. EN61000-3-2 became a leading standard in 2001 requiring all mains connected devices operating $\leq$ 16 A to have PFC. EN61000-3-2 Class C addresses lighting products and Class D concerns consumer products between 75 W and 600 W such as computers or televisions [35].

[6]IBM launched the first portable business computer in 1975 with the 55 pound, 64 KB RAM IBM5100. The first personal computer, introduced in 1975, was the MITS Altair 8800. The Apple I was released in 1976, followed by the popular Apple II in 1977 [46, 47].

[7]Manufacturers released the first commercial CFL light bulb in 1973 [48].

[8]The LED was invented by Nick Holonyak Jr. in 1962 [49, 50] while he was working at General Electric. Holonyak was John Bardeen's first graduate student at the University of Illinois.

documented in [64], academic work should focus on addressing industrial challenges and avoid what power electronics pioneer Rudy Severns [69] referred to as "circuit reinvention." Given this application-oriented evolution of power electronics, Chapter 3 describes the general working principles and loss mechanisms of switching power converters.

# CHAPTER 3

# REVIEW OF FUNDAMENTAL POWER ELECTRONICS CONCEPTS

*How harmful overspecialization is. It cuts knowledge at a million points and leaves it bleeding.*

– Isaac Asimov, 1920-1992

## 3.1 Introduction

Understanding the operation of power converters[1] warrants a review of periodic steady state analysis, source and load replacement techniques, and the process for calculating key loss mechanisms for a power transistor.

## 3.2 Periodic Steady-State

Just as sinusoidal steady-state facilitates impedance analysis for a vast majority of electrical engineering analysis, periodic steady-state (PSS) is vitally important to the field of power electronics [70–72]. Switched-mode power converters operate cyclically, which means the system repeats the exact same behavior in each cycle. PSS can easily be determined by examining state variables such as current, $i$, or voltage, $v$, at the end of each cycle. The value of this state variable must be identical to both the ending and starting values of the previous cycles. For example in Figure 3.1a, the state variables clearly are in PSS because the beginning and ending values of each cycle are the same. In contrast, the waveforms of Figure 3.1b are not PSS because the beginning and ending values for each cycle are not the same, but instead shifting in time. Simply, PSS is the normal operational mode of a power electronics circuit (i.e. not startup, transients, or shutdown), and thus can reduce the complexity of the circuit analysis during normal operating conditions.

[1]The discussion in this chapter is based in part on power and energy coursework completed at the University of Illinois at Urbana-Champaign as part of the doctoral degree and insights from key references [70–72].

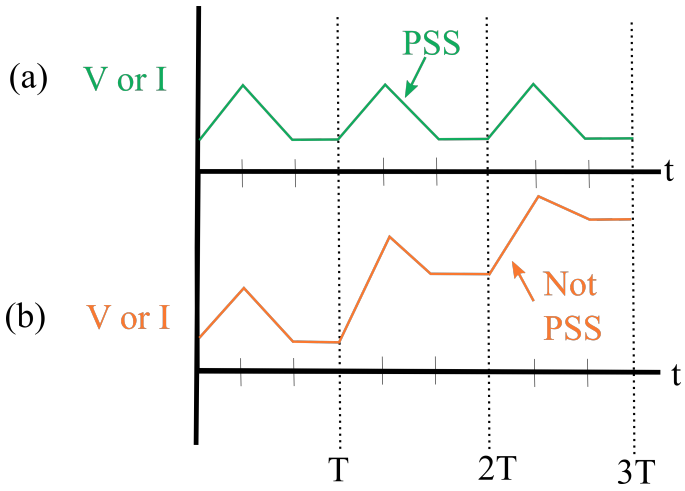


Figure 3.1: Waveform (a) with PSS and (b) without PSS.

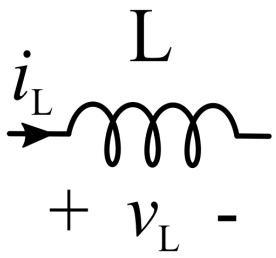


Figure 3.2: Passive sign convention for inductor.

To understand how PSS simplifies circuit analysis, we will examine how inductors and capacitors behave under PSS. Figure 3.2 highlights how an inductor should be modeled with passive sign convention in PSS. Recall that the governing equation for an inductor is:

$$v_L = L\,\frac{di_L(t)}{dt}. \tag{3.1}$$

If we apply an average operator to determine the average voltage across the inductor,

$$\left\langle v_L \right\rangle = \left\langle L\,\frac{di_L(t)}{dt} \right\rangle. \tag{3.2}$$

Since the inductance, $L$, is constant, it can pass out of the operator.

$$\left\langle v_L \right\rangle = L\left\langle \frac{di_L(t)}{dt} \right\rangle. \tag{3.3}$$

Now, if the circuit is in PSS, then the current will always be returning to the same point between cycles, which makes the derivative:

$$\left\langle \frac{di_L(t)}{dt} \right\rangle = 0. \tag{3.4}$$

Thus, the average value of the voltage across an inductor in PSS is:

$$\left\langle v_L \right\rangle = 0. \tag{3.5}$$

Inside a cycle, $\left\langle \frac{di_L(t)}{dt} \right\rangle \neq 0$, but, on average for the entire cycle of a waveform in PSS, the $\left\langle \frac{di_L(t)}{dt} \right\rangle = 0$. If the circuit is not in PSS, then the $\left\langle \frac{di_L(t)}{dt} \right\rangle \neq 0$.

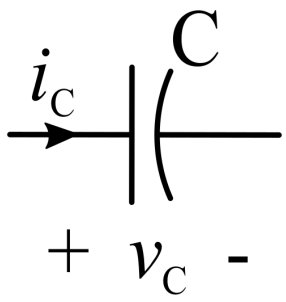


Figure 3.3: Passive sign convention for capacitor.

Similarly, a capacitor should be modeled with passive sign convention in PSS as shown in Figure 3.3. Recall that the governing equation for a capacitor is:

$$i_c = C\,\frac{dv_c(t)}{dt}. \tag{3.6}$$

If we apply an average operator to determine the current through the capacitor,

$$\left\langle i_c \right\rangle = \left\langle C\,\frac{dv_c(t)}{dt} \right\rangle, \tag{3.7}$$

the average value of the current through a capacitor in PSS is:

$$\left\langle i_c \right\rangle = 0, \tag{3.8}$$

due to the same observations as the analysis for the inductor. Inside a cycle, $\left\langle \frac{dv_c(t)}{dt} \right\rangle \neq 0$, but, on average for the entire cycle of a waveform in PSS, the

$\left\langle \frac{dv_c(t)}{dt} \right\rangle = 0$. If the circuit is not in PSS, then the $\left\langle \frac{dv_c(t)}{dt} \right\rangle \neq 0$.

Applying these same rules to Kirchhoff's voltage and current laws as well as the average input and output power in the circuit (assuming ideal conditions without losses) yields the remaining three commandments of PSS summarized in Figure 3.4, which dramatically simplify power electronics analysis.

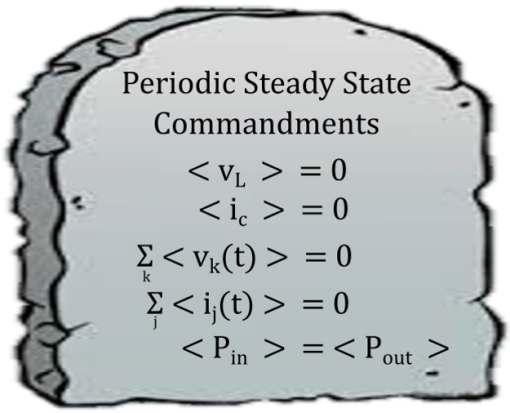


Figure 3.4: Summary of the five laws of PSS for power converter analysis (on a tablet potentially from Mount Sinai).

## 3.3 Load and Source Replacement for Converter Analysis

As a first step toward analyzing a power converter, consider the rectifier circuit in Figure 3.5. For a "large" inductance, $L$, the current through the inductor can be approximated as roughly constant (i.e. dc current) because $\frac{L}{R} \gg \frac{2\pi}{\omega}$ where $\omega$ is the frequency of operation. If this is true, then the output voltage, $v_o$, is constant, $V_o$. Thus, what is the average value of $v_x$, $< v_x >$? By PSS, $< v_L >= 0$, so $< v_x >=< v_o >$. Thus, source or load replacement can be applied to simplify the analysis.

If a load replacement is employed, the series L-R load can be replaced by a current source as shown in Figure 3.6. The validity of this assumption is clear in Figure 3.7 because the load has the same terminal characteristics at the $v_x$ node. Repeating this process with a source replacement instead of a load replacement provides additional insight into circuit behavior. Instead of

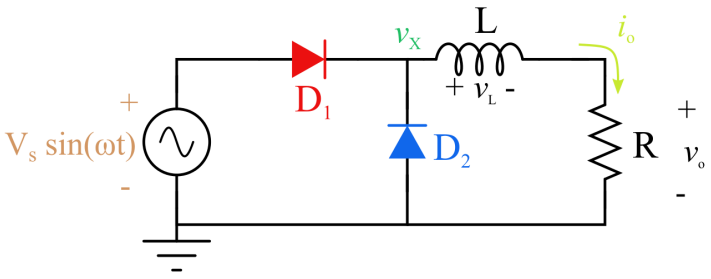


Figure 3.5: Example ac-dc converter to motivate load & source replacement.

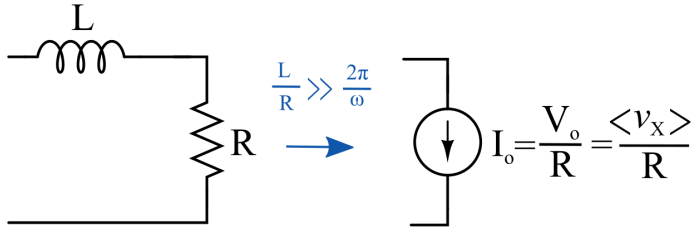


Figure 3.6: Example of load replacement.

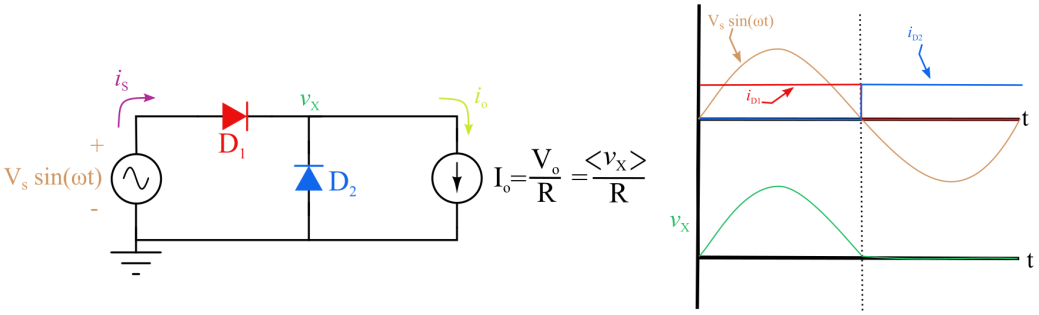


Figure 3.7: Example of ac-dc converter with load replacement.

a half-wave sinusoid, PSS underscores how the average value of the $v_x$ node is constant. Recall that the average value of the voltage across the inductor is zero by PSS, which means by KVL for the source replacement in Figure 3.8, the $< v_x >= V_o$.

During the time when the inductor voltage is non-zero, the current in the inductor ramps up. Once the inductor voltage is zero, the energy stored in the magnetic field of the inductor is released as the current ramps down. Thus, rearranging (3.1) slightly and recalling that a derivative looks at rate

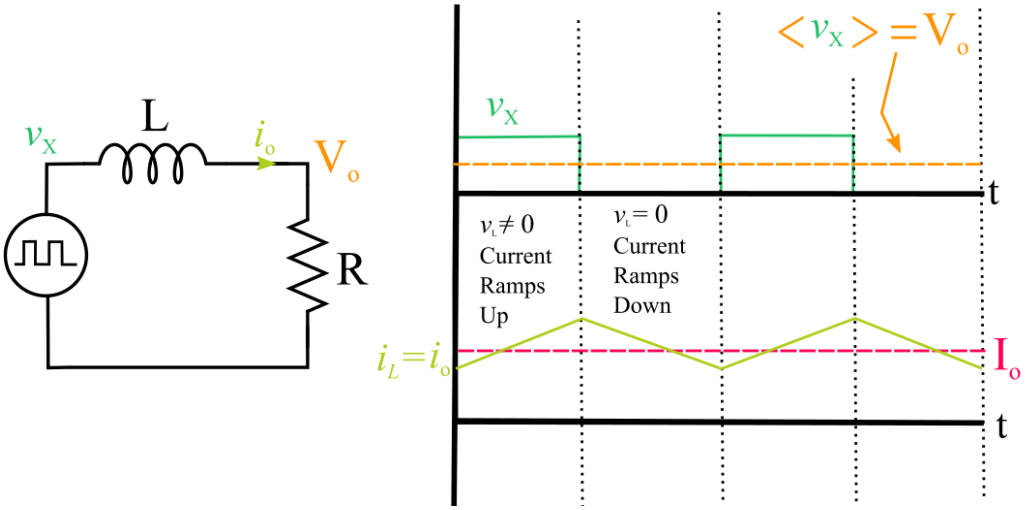


Figure 3.8: Example of ac-dc converter with source replacement.

of change enable the magnitude of the current ripple to be controlled via:

$$\frac{di_L(t)}{dt} = \frac{v_L}{L}$$
$$\Delta i = \frac{v_L\ \Delta T}{L}. \tag{3.9}$$

By making $\frac{\Delta T}{L}$ very small, the current ripple, $\Delta i$, can be made very small. Here, $\Delta T = \frac{T}{2}$ (i.e. the amount of time in this example during which the current ramps either up or down). Combining lessons learned from both the source replacement and the load replacement, the operation of the rectifier depicted in Figure 3.5 can be explained. The final operational waveforms of the important state-variables are recorded in Figure 3.9.

## 3.4 Overview of Key Loss Mechanisms for Power Transistors

All switching transistors are subject to joule heating due to loss mechanisms during operation including conduction ($P_{cond}$), the overlapping current and voltage for each switching transition ($P_{sw}$), and the loss from charging and discharging the parasitic capacitances of the device. By applying the techniques from Sec. 3.2 and Sec. 3.3 to a buck converter in Figure 3.10, the

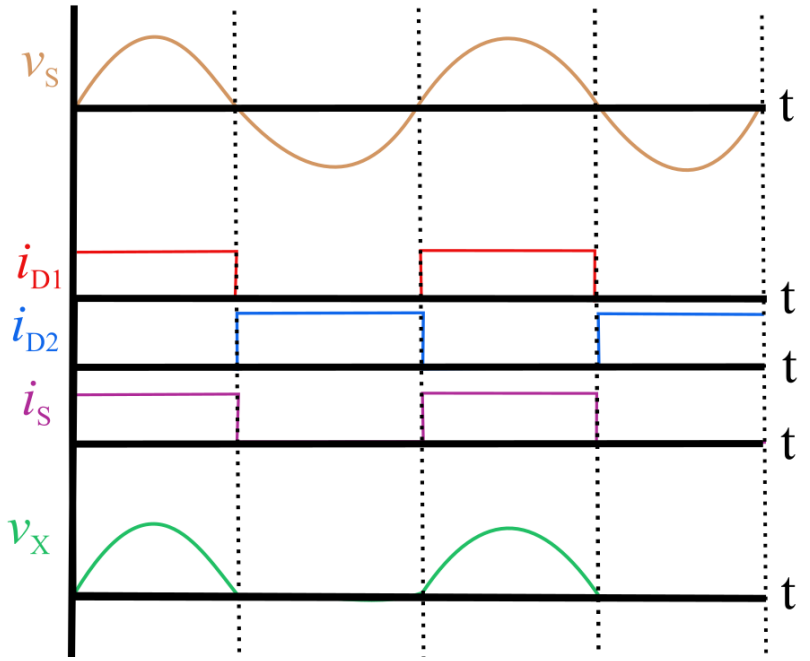


Figure 3.9: Example of ac-dc converter with state variable waveforms.

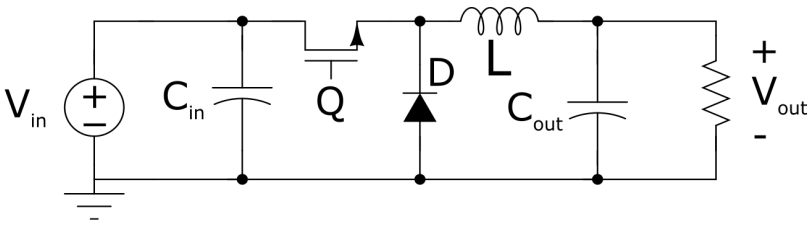


Figure 3.10: Example of dc-dc buck converter.

equations describing these loss mechanisms [70–72] simplify to:

$$P_{cond} = R \cdot (i_{sw,rms})^2 = R \cdot D \cdot I_L^2, \tag{3.10}$$

and

$$P_{sw} = f_{sw} \cdot \Big(0.5 \cdot t_{rise} \cdot Vin \cdot I_L + 0.5 \cdot t_{fall} \cdot Vin \cdot I_L\Big), \tag{3.11}$$

where $R$ is the device-specific on-state resistance, $t_{rise}$ and $t_{rise}$ are the rise and fall time of the switching transition respectively, $D$ is the duty ratio applied to the switching transistors, and $f_{sw}$ corresponds to the power converter switching frequency. $P_{sw}$ accounts for the instantaneous power loss from the overlap of current and voltage as the transistor turns on and off. Considering the buck converter example, as a switch turns off, current

will continue to flow through the device until the gate-to-drain parasitic capacitance has been charged and the voltage across the device reaches the blocking voltage, $V_{in}$. At this point, the current through the transistor decays since the diode begins to conduct and the gate-to-source capacitance is discharged. The energy lost during this transition where high voltage and current exist simultaneously occurs during every switching transition. Chapter 7 discusses how to measure switching loss using an industry standard double-pulse technique that enables identical current and voltage stress conditions during both the turn-on and turn-off transitions. Insights from probing switching loss guide design decisions about the operational switching frequency, component selection, topology, and adoption of control techniques to eliminate the crossover of current and voltage such as zero-voltage and zero-current switching [70–72]. Next, analyzing the loss for the drain-to-source capacitance ($C_{ds}$) will be examined as an example of how to account for the energy dissipated via the capacitive parasitics. When the switch is off, the diode is conducting so the voltage across this capacitance, $V_{ds}$, is equal to $V_{in}$ and energy is stored on $C_{ds}$ according to:

$$W_{Cds} = 0.5 \cdot C_{ds} \cdot V_{ds}^2. \tag{3.12}$$

During the switching transition, this capacitance is discharged and the energy is dissipated. Thus, the power loss for this mechanism simplifies to:

$$P_{Cds} = W_{Cds} \cdot f_{sw}. \tag{3.13}$$

Interestingly, increasing the die area or paralleling packaged components to reduce $R$ and $P_{cond}$ increases $C_{ds}$ and $P_{Cds}$. Thus, minimizing the overall loss of a converter requires careful consideration for the selection of components due to their parasitics. Accurately accounting for all loss mechanisms is key for selecting components and designing a converter to satisfy all electro-thermal requirements.

# CHAPTER 4

# REVIEW OF THE STATE-OF-THE-ART FOR ELECTRONICS COOLING

*Law school teaches you to think about ordinary things in a formal way. After two weeks of contracts, I saw a sign that said,"Apples Ten Cents," so I gave the store owner a dime and took two apples. He immediately said,"No, no, no!" Yet, I showed him where it said, "Apple**s**," and, realizing I was a law student, the store owner asked me to leave.*

– Retired Supreme Court Justice Anthony Kennedy, 1936-Present

## 4.1 Introduction

Addressing the thermal management problems facing power electronics first requires an appreciation[1] of the difficulty of the problem and the benefits and drawbacks of different cooling strategies.

## 4.2 Visualizing the Difficulty of Cooling Power Transistors

The heat transfer rate [W] is related to material properties and environmental conditions via

$$\dot{q} = h \cdot A \cdot \Delta T, \tag{4.1}$$

where $h$ is the heat transfer coefficient [W/m·K], $A$ is the surface area through which heat is flowing [$m^2$], and $\Delta T$ is the temperature difference driving the heat transfer [K]. Dividing by the bounding surface area, heat flux [$W/cm^2$] is simply

$$q'' = h \cdot \Delta T. \tag{4.2}$$

[1]The discussion in this chapter is based in part on heat transfer coursework completed at the University of Illinois at Urbana-Champaign as part of the doctoral degree and insights from key references [70, 73, 74].

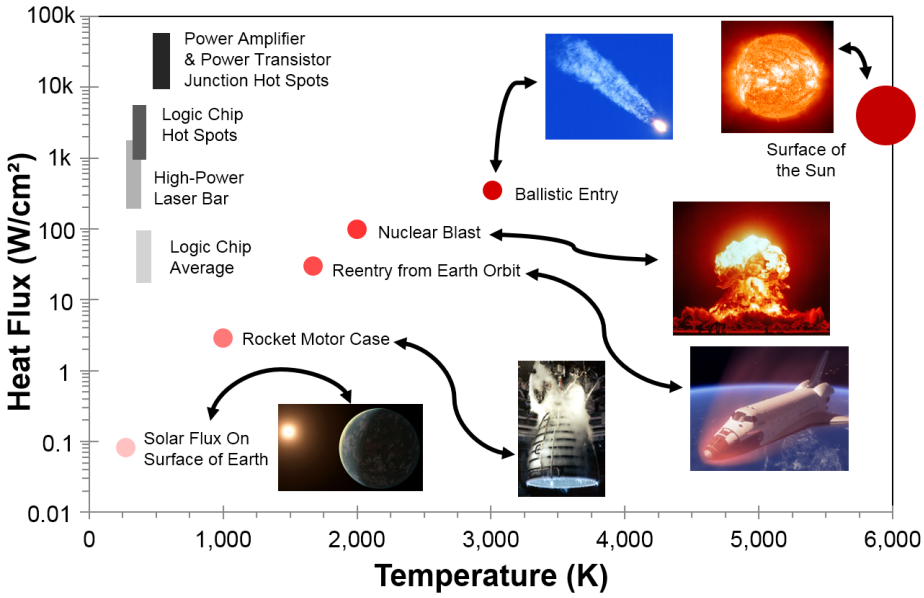


Figure 4.1: Power transistor heat fluxes for hot spots approach and in some cases exceed the heat flux on the surface of the Sun for $\Delta T$ of only a few hundred degrees. Adapted from [73].

Figure 4.1 provides a frame of reference from the immense challenge of cooling electronics since $q''$ for the hotspot at the junction of the power transistor can exceed the heat flux on the surface of the Sun [73]. Yet, the junction gallium-nitride (GaN) power transistor does not have the luxury of a several thousand degree $\Delta T$ that exists between the Sun and the cold vacuum of outer space. Since only a small $\Delta T$ of a few hundred degrees exists between the hot spot and the heat sink (e.g. air, liquid, metal surface), clearly the only way to dissipate heat fluxes exceeding 50 kW/cm$^2$ involves selecting a thermal management scheme to achieve an extremely large $h$.

## 4.3 Survey of Thermal Management Schemes

A survey of the order-of-magnitude of heat transfer coefficients for different thermal management strategies relevant to electronics cooling have been captured in Table 4.1 [75–77]. Cooling with natural and forced air convection has strict theoretical limits on heat flux ($<$ 30 W/cm$^2$) due to the poor thermophysical properties of air and the capacity to extract heat via laminar and turbulent parallel flow. Improving the heat rejection capability requires either increasing the surface area for heat spreading and fluid

Table 4.1: Survey of Heat Transfer Performance for Thermal Management

| Cooling Method | Heat Transfer Coefficient ($W/m^2K$) |
|---|---|
| Natural Convection, Air | 3 - 25 |
| Natural Convection, Dielectric | 10 - 60 |
| Natural Convection, Water | 30 - 300 |
| Forced Convection, Air | 15 - 200 |
| Forced Convection, Dielectric | 400 - 5,000 |
| Forced Convection, Water | 700 - 10,000 |
| Boiling, Dielectric | 1,000 - 20,000 |
| Boiling, Water | 4,500 - 100,000 |
| Condensation, Water | 6,000 - 140,000 |

interaction (i.e. adding a heat sink) or engineering ways to improve the turbulence dramatically such as tripping the boundary layer or employing jet impingement to enable dramatic thinning of the boundary layer and achieve a larger $h$. Transitioning to different fluids such as water or dielectric fluid for forced single-phase convection leverages improvements in the thermophysical properties for enhanced heat transfer. Beyond this, two-phase cooling facilitates several orders of magnitude higher heat transfer coefficients and leverages latent heat to transfer large amounts of heat during phase-change such as immersion, two-phase microchannel cooling, heat pipes vapor chambers, and spray cooling. A survey of publicly available state-of-the-art heat flux for these two-phase approaches [76–83] highlighted heat fluxes approaching $\sim 10^4$-$10^5$ $W/cm^2$ can be achieved with high flow rates, pressure drops, and surface enhancements. While boiling involves the phase transition from liquid to gas, Table 4.1 highlights that large $h$ also exists for condensation as hot vapor spreads heat to a colder surface through liquid droplet nucleation or film growth [84]. For boiling, heat transfer is enhanced by increasing the rate vapor bubbles leave the surface in order to facilitate fresh, cold liquid to quench the hot surface. Analogously, the effectiveness of dropwise condensation is maximized by increasing the rate of droplet shedding from the surface so fresh vapor can enable new nucleation. Both two-phase transitions are essential for the effective operation of heat pipes and vapor chambers, which are investigated through experiments in Chapters 8 - 10. All in all, this thesis examines how two-phase and directed cooling can enable improvements in power density for compact, lightweight electronics.

# CHAPTER 5

# UNDERSTANDING HOW POWER DENSITY AND SPECIFIC POWER IMPACT BOTH SYSTEMS AND SOCIETY

*It takes you a while to 'unthink' things you thought you knew...that's what it's all about: unmasking the prejudices of a discipline.*

– John B. Goodenough, 1922 - Present (Nobel Prize 2019)

## 5.1 Introduction

Before discussing power density, a common definition from a classical power electronics perspective must be established for both volumetric,[1]

$$\rho_c = \frac{P_c}{V_c}, \tag{5.1}$$

and specific,

$$\zeta_c = \frac{P_c}{m_c}, \tag{5.2}$$

density[2] where $P$ is the processed power [W], $V$ is the packaged volume [dm$^3$ or L], $m$ is the mass of the system [kg], and $c$ subscript stands for converter. Yet, when considering system-level volumetric and specific power, the system volume, $V_s$, and mass, $m_s$, must account for the volume and mass required for the entire supply-chain and processing of the materials for fabrication and energy source for propulsion. Also, the processed power, $P_s$, will be higher than that seen by an single subsystem since efficiency penalties of series and parallel networks of components must be considered. Thus, a system-level volumetric,

$$\rho_s = \frac{P_s}{V_s}, \tag{5.3}$$

and specific,

[1]For reference, 1 kW/L = 1 kW/dm$^3$ = 1 W/cm$^3$ = 16 W/in$^3$.

[2]For pulsed loads, often the peak output power is utilized for $P$. Also, published values for $\rho_c$ and $\zeta_c$ rarely account for heat exchanger or cooling system as part of the total volume, which is critical to consider for system-level analysis. Also, published values for $m_c$ rarely account for the heat sink mass.

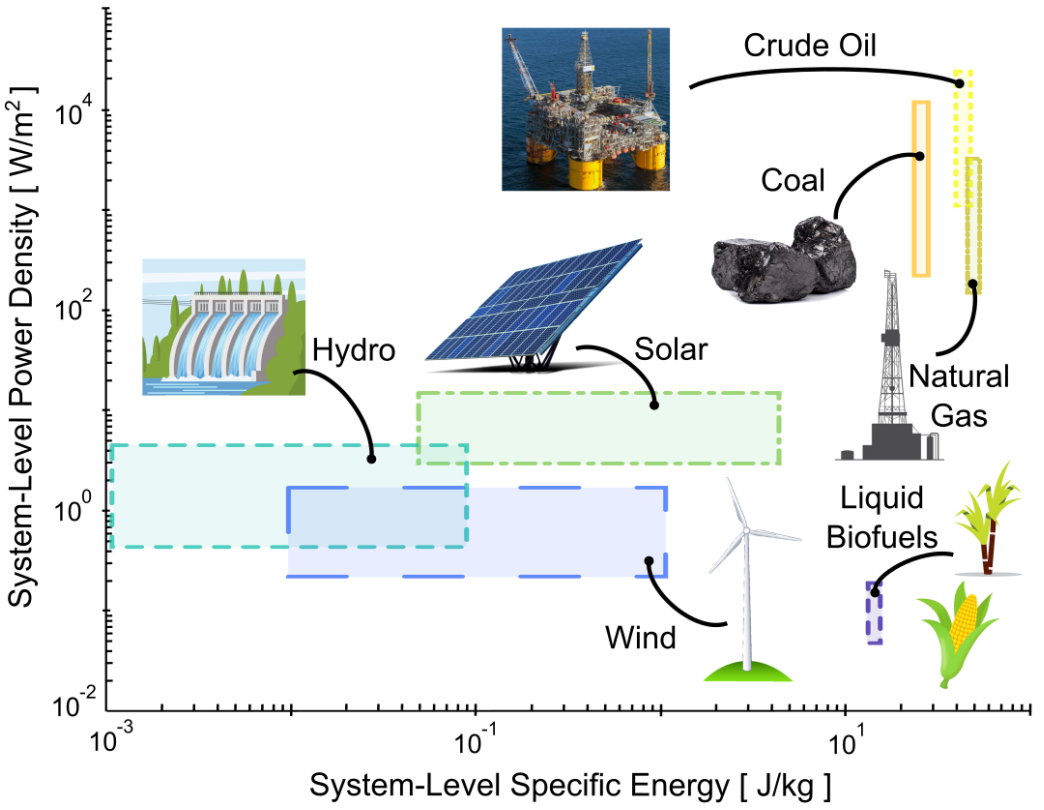


Figure 5.1: Examining how the primary energy sources compare in terms of system-level power density and specific energy. Data synthesized from [85, 86].

$$\zeta_s = \frac{P_s}{m_s}, \tag{5.4}$$

density[3] can also be obtained. Many considerations for $\rho_s$ including estimates for the complete energy supply-chain result in a flux per unit area [W/m$^2$] since the land area consumed by the right-of-way for obtaining, refining, and transporting these resources (e.g. mines, wells, land area consumed by reservoirs and dams for hydro resources, PV workable area, wind turbine farm factors such as turbine spacing requirements, pad area, and access road) must also be considered [85]. A survey of propulsion fuel sources in Figure 5.1 for example highlights the importance of considering the total supply-chain and life-cycle of an energy source when making design choices or considering the implications of policy decisions since fossil fuels vastly outperform all renewable energy resources by several orders-of-magnitude. As a

[3]For system analysis, comparing different technologies based on relative volume (L/kW) and relative weight (kg/kW) can also provide useful insights.

result, transitioning national or global economies to be supplied by renewable energy would be a reversal of centuries of human behavior as the first time in history that fuels with lower $\rho_s$ and $\zeta_s$ are selected preferentially [86]. For example, the extremely poor power density of biofuels from sugar cane and corn underscores that biofuels alone are not a viable alternative for totally replacing petroleum since, for the energy need of the United States alone, transition entirely to biofuels would require harvesting corn from three times the amount of suitable cropland that exists in the country [85, 86]. In contrast, fossil fuels utilize less than 0.5% of the land in the United States accounting for all rights-of-way and infrastructure for processing, which is much less than the land used for housing (1.5%), farming (18%), and the combination of forests and grasslands (60%) [85]. Similarly, even the best-case scenario for solar is still at best one order-of-magnitude lower for both power density and specific energy than all of the lowest performing fossil fuel energy sources. Thus, these observations underscore that electrification of mobile and stationary systems will require hybrid fossil fuel and alternative energy solutions to satisfy engineering feasibility, cost, and sustainability goals simultaneously.

## 5.2 Packaged Density Directly Impacts Energy Utilization & Carbon Footprint

To appreciate the importance of volumetric and specific power density first requires an understanding of how energy flows through the United States economy [87–89] as shown in the Sankey diagram of Figure 5.2. The primary energy sources and ultimate translation into either useful work or rejection as waste heat are all measured in quads (i.e. $1.055{\cdot}10^{18}$ J or 1.055 EJ). Interestingly, even after more than two decades of government subsidies to support the deployment of solar and wind power resources, the primary sources of energy in the United States have not shifted significantly away from fossil fuels (i.e. the energy landscape of the United States is still dominated by petroleum ($\approx$2% increase from 2017), coal ($\approx$5% decrease from 2017), and natural gas ($\approx$10.7% increase from 2017)) [88, 89]. Roughly 67.7% of this energy is ultimately rejected to the environment as waste heat through heat exchangers at temperatures less than $< 230$ °C, which includes the cooling

of electronics for stationary and mobile systems [87, 88]. Since the heat is primarily transferred to air, the external temperature of the air at the input of the heat exchanger dramatically impacts the efficiency of these systems (i.e. power plants in Maine are more efficient at rejecting heat than those in Texas due to the vast differences in average temperature annually) [87]. Given the small temperature differences that exist for this large fraction of low-grade waste heat, phase-change heat transfer methods such as the liquid-vapor techniques discussed in Chapters 8 through 11 have broader technological and societal significance beyond the localized, high heat flux cooling of densely packed electronics hotspots introduced in Chapter 4.

Figure 5.3 underscores how the primary energy sources utilized for electricity generation in the United States have changed in the last seven decades [86]. Just as fossil fuel consumption has not decreased below the 1950 levels for electricity production in the United States, the global fossil fuel consumption for all primary energy use has only decreased from 91% in 1992 to 89% in 2018 [86, 91, 92]. Of note, the modernization of China is an important factor curtailing the decrease in global fossil fuel consumption

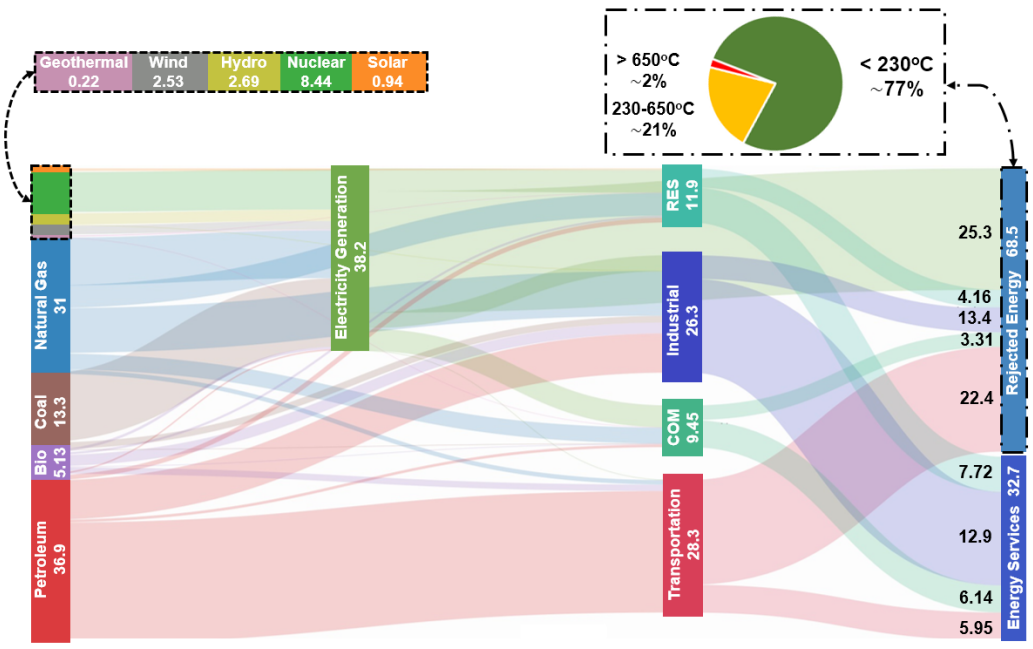


Figure 5.2: Visualizing how energy flows from sources through the United States network to loads (units are in quads) and understanding the fraction of waste heat associated with low-grade heat ($< 230$ °C). Data synthesized from [87–89].

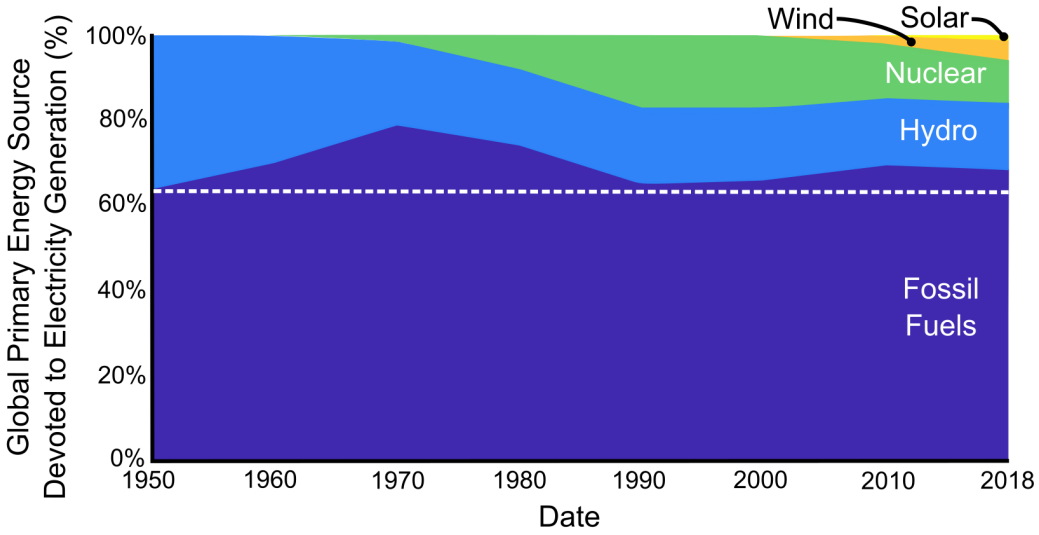


Figure 5.3: The global share of fossil fuels as a primary energy sources utilized for electricity has increased over the past seventy years (63.7% in 1950 to 68.1% in 2018). In 2018, the other sources of primary energy employed to produce electricity were hydro (16.2%), nuclear (10/5%), wind (3.9%), and solar (1.3%). Data synthesized from [86].

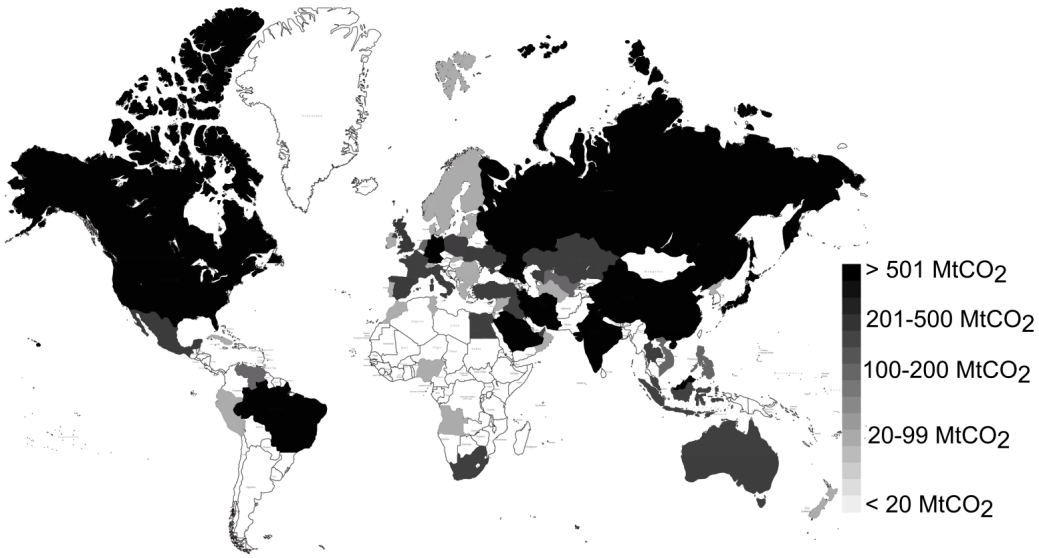


Figure 5.4: Total $CO_2$ emissions for each country in 2017 measured in mega-tons (Mt). Data synthesized from [90].

as China consumes massive quantities of energy not just for transportation and electricity, but also for raw material processing, manufacturing, and construction. For example, between 2011 and 2014, the Chinese poured more concrete into their roads and buildings than the United States consumed in the last century [85]. Realizing that a large fraction of primary energy

use globally and nationally is sourced from fossil fuels, an estimate of the carbon footprint for a system can be calculated using conversions from TWh of energy consumption to mega-tons of $CO_2$ (Mt $CO_2$) [93] and compared against the measured $CO_2$ emissions for each country [90] as shown in Figure 5.4. Since system-level volumetric and specific density can be mapped to carbon emissions, the impact of $\rho_c$ and $\zeta_c$ performance metrics for subsystem components like power converters can have significant impact on improving or limiting the carbon footprint of current and future systems.

## 5.3 Discussion and Concluding Thoughts

In summary, $\rho_c$ and $\zeta_c$ for converters inside of energy conversion systems are vital metrics to realizing a transition toward a more sustainable energy future. For mobile systems like aircraft and automobiles, $\zeta_c$ for each subsystem in the energy conversion path directly impacts the overall achievable range. Increasing $\zeta_c$, therefore, creates expanded opportunities for more sustainable fuel sources and hybrid configurations to be viable from a cost perspective. Since the transportation sector alone accounts for more than a third of all fossil fuel consumption in the United States alone, any effort to hybridize and electrify these systems will result in significant reduction in carbon emissions from fossil fuels. For electricity generation from renewable energy, increasing $\rho_c$ and $\zeta_c$ for converters ultimately enables broader deployment by reducing the overall installation cost, which is required to bridge the gap between fossil fuels and these renewable energy resources. All in all, higher $\rho_c$ and $\zeta_c$ are key enablers for accelerating the transition to a practical, lower carbon energy future, which realistically will involve a blend of high (i.e. fossil fuels) and low (i.e. renewable) $\rho_s$ energy resources.

# CHAPTER 6

# QUANTIFYING DYNAMIC ON-STATE RESISTANCE OF GAN HEMTS

*To find the secrets of the universe, think in terms of energy, frequency and vibration.*

– Nikola Tesla, 1856-1943

## 6.1 Introduction

Dynamic on-state resistance ($r_{\text{dson}}$) plagued the early acceptance of gallium-nitride (GaN) high-electron-mobility transistors (HEMTs) by producing significant additional device power loss. This time-changing $r_{\text{dson}}$ exists during the transition from the high blocking voltage stress of the device's off-state to the low voltage of the device's on-state. Thus, power converters exhibited more loss than expected based on the dc (low frequency) resistance measurement, which is the conventional test condition for the datasheet value of $R_{\text{dson}}$. The significant additional loss from dynamic $r_{\text{dson}}$ presented serious design challenges for RF and power electronics designers for applications with high switching frequency and high device voltage stress (i.e. high drain-to-source voltage) because these devices are not in the on-state long enough for the dynamic $r_{\text{dson}}$ to decay back to the $R_{\text{dson}}$ measured for dc operation.

Although GaN device manufacturers have previously claimed victory over this device defect [94–97], recent experimental observations for both hard-switched [98–101] and soft-switched [102–105], high-efficiency converters have suggested that this celebration might be premature because losses exist which cannot be explained from high-fidelity models for conduction, switching, and parasitic capacitance based losses. For converters employing soft-switching with GaN as well as SiC and Si superjunction switches, some of the anomalous loss has been attributed to additional loss from charge transfer in the non-linear device parasitic capacitances during ZVS transitions based on careful experimental observations [105, 106]. In other cases, the anomalous loss has exhibited a strong dependence on the drain-to-source voltage and

junction temperature of the GaN transistors [101]. This strong voltage and temperature dependence for the unexplained additional loss pathway warrants a detailed analysis of the dynamic $r_{\text{dson}}$ behavior for the current generation of GaN devices.

Both device and converter designers need a method for quantifying the impact of dynamic $r_{\text{dson}}$ either to modify the device design in order to mitigate this behavior or to predict the losses caused by this mechanism for new power electronics circuits. Yet, existing methods for analyzing dynamic $r_{\text{dson}}$ have been developed primarily for power device designers. Thus, these measurements require some additional translation to aid the design of a power converter. This study[1] introduces a method for analyzing and quantifying the impact of dynamic $r_{\text{dson}}$ in a meaningful way for power electronics designers agnostic of the clamping circuit, testbed, and experimental conditions employed. Readers familiar with the physical origins of dynamic $r_{\text{dson}}$ and methods for measuring this phenomenon with high fidelity, outlined in Sec. 6.2 and 6.3, can focus on the experimental evidence and two proposed metrics highlighted in Sec. 6.4 and Sec. 6.5 for benchmarking and incorporating dynamic $r_{\text{dson}}$ performance into converter design. Finally, Sec. 6.6 summarizes the main observations of this investigation and plans for future work.

## 6.2 Physical Origins of Dynamic $r_{\text{dson}}$ & Survey of Prior Measurement Methods

The increase in $r_{\text{dson}}$ due to higher GaN device voltage stress is attributed to a combination of electron trapping when the device is off and to hot-electron trapping and de-trapping when the device is turning on [108–115]. Figure 6.1 demonstrates how these electron trapping mechanisms manifest themselves during the off-state, transition state, and on-state of the GaN device. When the GaN device is off and blocking a large voltage, electrons are believed to be trapped in the AlGaN/GaN interface between the gate and the drain as depicted in Figure 6.1b. These trapped electrons form a "virtual gate" phenomenon as illustrated in Figure 6.1c that limits how quickly the channel can ramp up and carry the full drain current, which is referred to as current

[1]This chapter includes work published in part in [107].

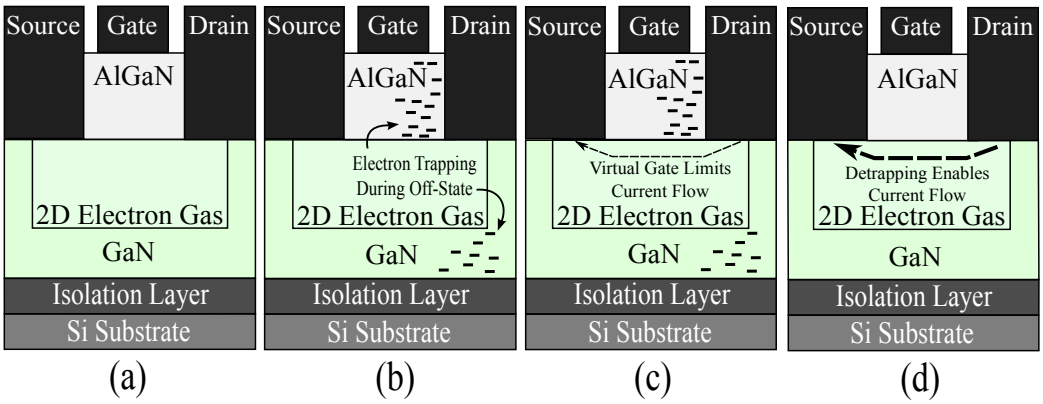


Figure 6.1: Understanding the origin of dynamic $r_{\text{dson}}$ (a) with a simplified cartoon of the GaN HEMT structure (not drawn to scale) in the (b) off-state, (c) initial on-state exhibiting electron trapping (black dashes) causing virtual gate and current collapse behavior, and (d) on-state after the decay to $R_{\text{dc}}$ measured for dc (low frequency) operation occurs.

collapse [108, 110, 112, 116]. Along with hot-electron trapping in the GaN layer, this limits the effectiveness of the 2D electron gas, which contributes to higher on-state resistance and other degraded switching performance such as gate lag [116]. Eventually, the de-trapping of these electrons allows the $r_{\text{dson}}$ to settle back to the value measured under dc operation [108, 112, 117] as in Figure 6.1d. Evidence of suppression of this unwanted dynamic device behavior, such as dielectric passivation, buffer doping distributions, and shaping the electric field with multiple-field plates between the gate and drain [114, 118–120], offers strong support of the electron trapping theory as the physical mechanism behind dynamic $r_{\text{dson}}$.

The current-transient method of [111, 112] revealed how the de-trapping phenomenon within the GaN devices has both fast (between 200 ns and 1 ms) and slow transients (1 ms to 100 s) when the device voltage stress is increased. Thus, for power electronics applications, a practical measurement circuit must have an ultra-fast reaction time (i.e. very small time constants in the measurement circuit) in order to capture an accurate measurement of the dynamic $r_{\text{dson}}$ during and right after the switch transitions from the off-state to the on-state. Unfortunately, the expensive, custom test equipment employed by [111,112] is not readily available to the average power electronics practitioner in either industry or academia. Thus, lower cost measurement methods utilizing readily available components that do not compromise the integrity of the measurement fidelity are required. Additionally, as these test

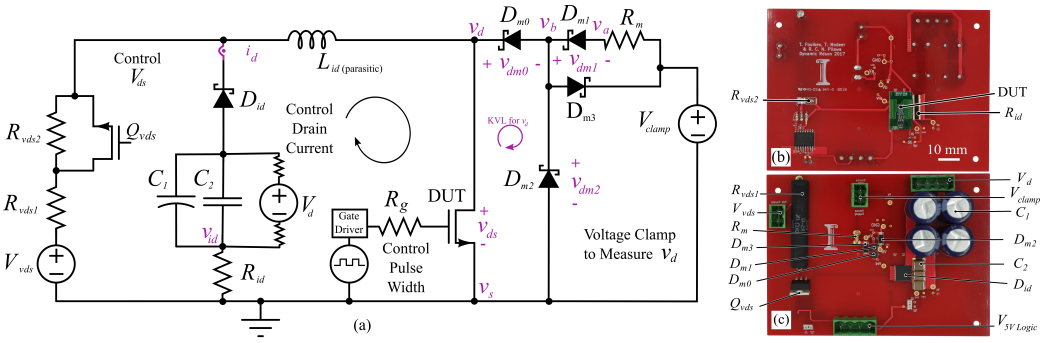


Figure 6.2: (a) Annotated schematic along with photos of the (b) front and (c) back of the experimental testbed for the survey of dynamic $r_{\text{dson}}$ for commercial GaN devices. The labels $v_{\text{a}}$, $v_{\text{b}}$, $v_{\text{id}}$ & $v_{\text{s}}$ correspond to the location of measurement probes in the circuit. While the drain current was measured via a precision sense resistor in this experiment, current probes could also be employed to measure at location $i_{\text{d}}$ as shown. $L_{\text{id}}$ is a parasitic inductance in the loop controlling the magnitude of drain current. Adapter boards attached to the testbed enable a broad survey of commercial GaN devices.

circuits and methods are evaluated, emphasis should be placed on developing a method that accurately reflects the usage scenarios for power converters.

Prior work has focused on approaches for accurate voltage sensing of fast transients via external clamping circuits. This approach overcomes any analog-to-digital converter (ADC) overdrive measurement errors and facilitates high-resolution sampling on an oscilloscope with full utilization of the ADC for the quantization of the small voltage across the device during the on-state after the device-under-test (DUT) had previously been blocking a high-voltage during the off-state [121–124]. Different realizations of clamping circuits involving combinations of transistors, diodes, and resistors have been proposed [29, 121, 123–127]. All of these clamps enable the basic measurement, but have varying impacts on the offset and delay of the measured drain voltage due to their parasitic capacitances. These types of distortions could have a dramatic impact on the fidelity of the dynamic $r_{\text{dson}}$ measurement.

Furthermore, prior work has primarily focused on methods for sensitive measurements of voltage and built on testbeds designed for Si MOSFET characterization and reliability testing such as hard-switching double pulse, soft-switching, or thermal evaluation [128–133], which largely ignore the simultaneous independent control of voltage stress, drain current, on/off

time, and device steady-state temperature for the DUT. In past experimental setups, measurements were often implemented for only a few test cases of voltage, current, package temperature, and pulse-width for the device stress. Thus, this work focuses on developing a precise, yet low-cost technique for characterizing the dynamic $r_{\text{dson}}$ of a wide range of commercial GaN transistors under conditions for voltage, current, pulse shape, and package temperature similar to the intended usage scenarios for power converters.

## 6.3 Probing $r_{\text{dson}}$ with Varying Voltage, Current, Pulse Shape & Device Temperature

### 6.3.1 Experimental Setup

This work seeks to leverage lessons learned from prior voltage clamping circuits and methods for high-accuracy measurement in order to develop a new testing method that allows the voltage stress, drain current, on/off time, and steady-state temperature to be varied independently. Figure 6.2a depicts a schematic drawing of the proposed method for probing dynamic $r_{\text{dson}}$ that allows independent control over all of these variables. The measurement circuit was carefully designed so that only four single-ended voltage measurements were required, which enables this method to be employed with any four-channel oscilloscope. Here, drain current can be varied through the path with Schottky diode, $D_{\text{id}}$, current sense resistor, $R_{\text{id}}$, bank of capacitance, $C_1$ and $C_2$, and a battery, $V_{\text{id}}$, in order to ensure a stiff dc voltage and a sufficient current supply when the device is conducting. A complete component listing for the experimental testbed can be found in Table 6.1. The drain current can be measured either with a current sensor (i.e. clamp-on Rogowski coil or high bandwidth current shunt) or with a single-ended voltage measurement across a high-precision, temperature-stable $R_{\text{id}}$. The voltage measurement with $R_{\text{id}}$ was employed in this work to determine the drain current, $i_{\text{d}} = v_{\text{id}}/R_{\text{id}}$, because a high-bandwidth measurement could be obtained while limiting the impact on both commutation loop inductance and variations due to probe calibration.

Oscillations in the drain current and clamped voltage source

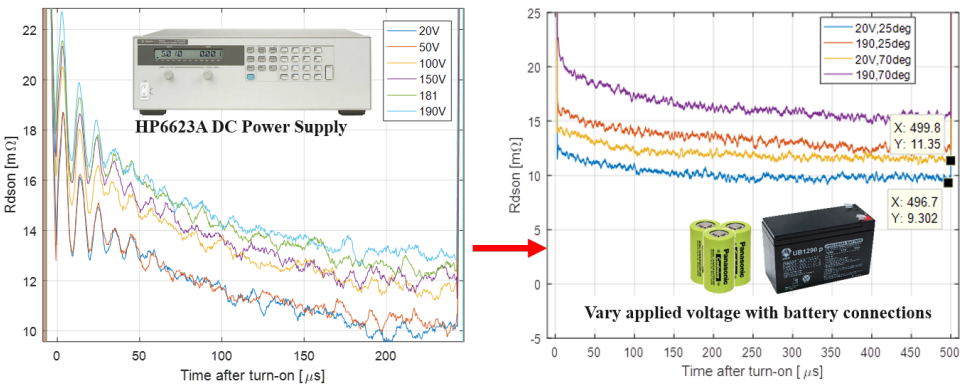


Figure 6.3: Supplying the drain current with batteries isolated the circuit from parasitic current paths associated with a floating power supply.

measurements, due to parasitic inductances and capacitive paths for noise currents to flow, can dramatically reduce the fidelity of the measured response. The drain current commutation loop inductance, $L_{\mathrm{id}}$, was isolated via simulations and lab measurements as the main source of ringing in early generations of this measurement setup. Great care was taken to ensure $L_{\mathrm{id}}$ was minimized during subsequent designs both by keeping this path as short as possible and by intentionally selecting low inductance, surface-mount components for the drain current loop as shown in Figure 6.2b and 6.2c. Interestingly, experimental observation highlighted that another major source of high-frequency noise in the measurement involved the type of voltage source used to charge the local capacitor bank and to provide drain current during conduction (Figure 6.3). When a power supply serves as the floating power supply for $V_{\mathrm{id}}$, the fidelity of the dynamic $r_{\mathrm{dson}}$ is compromised by high-frequency ringing due to the high capacitive coupling to ground via this floating power supply. This parasitic current path was identified experimentally using a clamp-on Rogowski coil (PEM Ultra-Mini CWT015). By employing various combinations of batteries in series and parallel to vary the floating voltage, this current path was eliminated and independent control of drain current supplied to the DUT was still possible.

The voltage clamping network comprising the four Schottky diodes—$D_{\mathrm{m0}}$, $D_{\mathrm{m1}}$, $D_{\mathrm{m2}}$ and $D_{\mathrm{m3}}$—provides a high resolution measurement of the drain voltage. The voltage bias of this clamping circuit, $V_{\mathrm{clamp}}$, is fixed at 5 V in order to enable full utilization of the ADC. When the DUT is on, $D_{\mathrm{m0}}$ and $D_{\mathrm{m1}}$ conduct, and the accuracy of the clamping circuit relies

Table 6.1: Components for the $r_{\text{dson}}$ Experimental Testbed

| Component | Part Number | Parameters |
|---|---|---|
| GaN FETs | EPC2016C | 100 V, 16 mΩ |
| | GS61004B | 100 V, 15 mΩ |
| | EPC2045 | 100 V, 7 mΩ |
| | EPC2033 | 150 V, 7 mΩ |
| | EPC2034 | 200 V, 10 mΩ |
| | EPC2047 | 200 V, 10 mΩ |
| | PGA26E07BA | 600 V, 63 mΩ |
| | GS66508B | 650 V, 50 mΩ |
| | TPH3208PS | 650 V, 130 mΩ |
| Si MOSFETs | Infineon IRFP4668 | 200 V, 8 mΩ |
| | IXYS IXFX230N20T | 200 V, 10 mΩ |
| | Infineon IPP65R125C7 | 650 V, 125 mΩ |
| $R_{\text{id}}$ | Vishay Y08562R00000F9W | 2 Ω, 1%, × 2 in // |
| $D_{\text{m0}}$, $D_{\text{m1}}$ | Cree C3D1P7060Q | 600 V, 1.7 A |
| $D_{\text{m2}}$, $D_{\text{m3}}$ | Comchip CDBA240-HF | 40 V, 2 A |
| $D_{\text{id}}$ | Infineon IDL06G65C5 | 650 V, 29 A |
| $C_1$ | Panasonic ECA-1HM222 | 2.2 mF, 4 in // |
| $C_2$ | TDK C5750X6S | 2.2 μF, 6 in // |
| $Q_{\text{vds}}$ | Infineon IPP65R125C7 | 650 V, 18 A |
| $R_{\text{m}}$ | | 120 Ω, 5% |
| Battery | EnerSys 0850-0004 | 2 V, 8 AH |
| Battery | Panasonic LC-R067R2P | 6 V, 7.2 AH |
| Battery | Panasonic LC-R127R2P | 12 V, 7.2 AH |

on the assumption that these two diodes have identical forward voltage drops. Therefore, these two diodes are chosen to be of the same type (Cree C3D1P7060Q), and taken from the same production batch to ensure that the diodes themselves are well-matched. For the assumption of equal forward voltages to hold, the two diodes must also have the same, or at least very similar, temperatures. Placing the diodes close to each other on the PCB minimizes the dissimilar temperature effects from external sources. When the DUT is turned on, the current through the diodes is the same, and therefore the self-heating and temperature are also very similar. However, slightly more losses in $D_{\text{m0}}$ exist as the DUT turns on and off. In the off-state, the leakage current through $D_{\text{m0}}$ will be approximately 55 μA at 600 V, leading to 33 mW of losses in $D_{\text{m0}}$. The extra losses in $D_{\text{m0}}$, as compared to $D_{\text{m1}}$, lead to an expected increase in junction temperature. Yet, even a conservative thermal resistance network for natural convection (∼15 K/W) would result

in a temperature difference between $D_{\mathrm{m0}}$ and $D_{\mathrm{m1}}$ of only $\sim$0.5 K, which corresponds to less than 1 mV for this diode [134]. Another source of loss that could result in temperature difference involves the charging and discharging of the parasitic capacitance of $D_{\mathrm{m0}}$ during the switching of the DUT. Since this energy is very small ($\sim$1 $\mu$J), heating of $D_{\mathrm{m0}}$ associated with this loss mechanism will also be negligible.

When the DUT is on, $D_{\mathrm{m0}}$ and $D_{\mathrm{m1}}$ conduct and are assumed to have identical voltage drops since they are well-matched and at a similar package temperature. $D_{\mathrm{m0}}$ must be rated to block higher voltages when the DUT is off, so the parasitic capacitance can only be reduced so much by careful part selection. $D_{\mathrm{m2}}$ and $D_{\mathrm{m3}}$ provide clamping of the measured voltage $v_{\mathrm{b}}$ to ensure that negative or positive ringing does not damage the probes or degrade the measurement fidelity. Therefore, $D_{\mathrm{m2}}$ and $D_{\mathrm{m3}}$ do not have the strict large voltage blocking requirement enabling the use of low-voltage, low-parasitic capacitance Schottky diodes. Figure 6.2a demonstrates how the drain-to-source voltage measurement is obtained by subtracting the single-ended voltage measurement of the DUT's source terminal from the voltage drop across the Schottky diodes, $D_{\mathrm{m0}}$ and $D_{\mathrm{m2}}$, as in:

$$v_{\mathrm{ds}} = v_{\mathrm{d}} - v_{\mathrm{s}} = \Big[v_{\mathrm{dm2}} + v_{\mathrm{dm0}}\Big] - v_{\mathrm{s}}. \tag{6.1}$$

The voltage $v_{\mathrm{dm0}}$ is obtained from the mirrored voltage drop across $D_{\mathrm{m1}}$,

$$v_{\mathrm{dm0}} = v_{\mathrm{dm1}} = v_{\mathrm{b}} - v_{\mathrm{a}}, \tag{6.2}$$

where $v_{\mathrm{a}}$ can be measured with high fidelity at a lower potential established by $V_{\mathrm{clamp}}$, which prevents oscilloscope overdrive with the low clamping potential. The $v_{\mathrm{dm2}}$ voltage drop is directly measured with a single-ended probe,

$$v_{\mathrm{dm2}} = v_{\mathrm{b}}. \tag{6.3}$$

The drain-to-source measurement for the DUT thus simplifies to

$$v_{\mathrm{ds}} = 2 \cdot v_{\mathrm{b}} - v_{\mathrm{a}} - v_{\mathrm{s}}. \tag{6.4}$$

While dividing (6.4) by $i_{\mathrm{d}}$ describes the $r_{\mathrm{dson}}$ behavior to first order, the impact of $L_{\mathrm{id}}$ (i.e. $v_{\mathrm{L}} = L_{\mathrm{id}} \frac{di_d}{dt}$) during the initial transition

when the measured $\frac{di_d}{dt} \neq 0$ is important to consider especially for measurements with short pulse-widths and considering that de-trapping occurs on various time-scales. With the benefit of only requiring four single-ended voltage measurements, the resulting calculation to obtain dynamic on-state resistance is

$$r_{\text{dson}} = \frac{v_{\text{ds}} - v_{\text{L}}}{i_{\text{d}}}. \tag{6.5}$$

Enhancing the precision and accuracy of the measured voltages for the clamping and drain current sub-circuits requires careful consideration regarding the best practices of using single-ended oscilloscope probes. First, the ground return connections for all probes should be as short as possible in order to minimize any ringing caused by oscillations with this parasitic inductance. This requires a ground plane connection to be placed intentionally close to the measurement node during layout. Realizing that any offsets between the calibration of the $v_{\text{a}}$ and $v_{\text{b}}$ voltage probes could result either in an offset or a reduced fidelity measurement, active 10x probes (1 GHz Tektronix P6243 with 1 pF & 1 MΩ) with ultra-short ground connections were utilized for these sensitive clamped voltage measurements. Active probes significantly reduced both ringing and capacitive loading in the measurement due to the low probe tip capacitive parasitics. While the response for the $v_s$ and $v_{\text{id}}$ measurements is important, experimental testing highlighted that these voltages could be obtained with well-calibrated and matched standard 10x probes (500 MHz Tektronix P6139A with 8 pF & 10 MΩ) without compromising the integrity of the analysis (Figure 6.4).

The drain voltage can be changed independently via $V_{\text{vds}}$ so that careful sweeps of stress voltage can be conducted. Figure 6.5 highlights how a line filter (Schaffner FN2200B-25-33) was inserted between the external power supply (Magna-Power SL600-2.5/UI) and the testbed in order to isolate the circuit from noise currents generated by the power supply. The power transistor, $Q_{\text{vds}}$, helps control how long the DUT is stressed by high voltages before turning on since this is hypothesized to contribute to the degree of initially trapped electrons (i.e. larger initial dynamic $r_{\text{dson}}$). $R_{vds1}$ is sized (e.g. 10 kΩ) to ensure that the power supply will not source significant drain current during the conduction time. $R_{vds2}$ simply reduces the impact of ringing from the $Q_{\text{vds}}$ transition and can be several orders of magnitude larger than $R_{vds1}$. Just like $Q_{\text{vds}}$, the pulse-width and frequency of the DUT turn-

on are controlled using an arbitrary waveform function generator (Keysight 33500B) and a gate driver for the DUT. None of the enhancement-mode commercial GaN MOSFETs currently surveyed included integrated gate drivers. The LM5114 gate driver was employed for all GaN switches in order to eliminate variations in switching performance caused by different gate drivers for this comparison. The manufacturer datasheet recommendation for the gate voltage of each device was employed for this analysis in order to operate each device with the same operational characteristics intended by the manufacturer.

Finally, the steady-state temperature of the device was varied using a hot air gun with calibrated flow rate and temperature settings based on measurements with thermocouples for the device package temperature. A manifold was constructed to duct air directly to the DUT and also helped thermally shield other components such as the current sense resistors from any degraded performance due to convective heating from the hot air supply. Similarly, all probe connections were made from the side of the circuit board opposite to the DUT and heat source so that these measurement devices were also shielded from the hot air. During the experiments, measurements at elevated temperature were not obtained until the DUT had achieved thermal steady-state, which calibration indicated required approximately 5 minutes. Thermocouples were attached to the outside of the GaN device and both the front and back of the PCB. This enabled the junction temperature

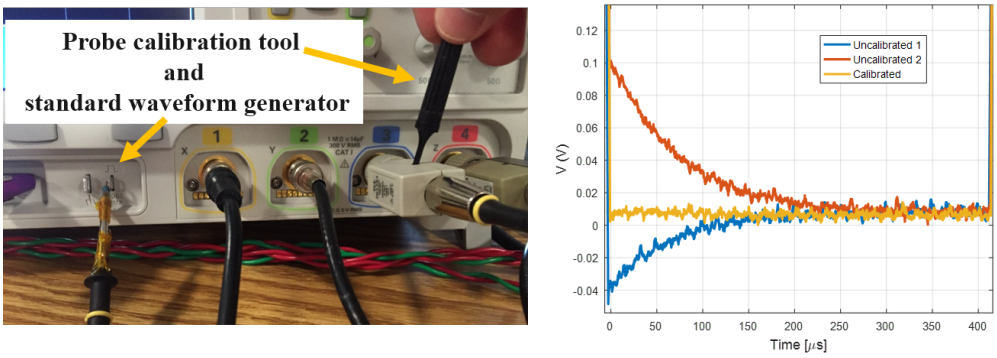


Figure 6.4: While active probes are designed to ensure low-inductance measurements and compensate for the highest fidelity measurement (i.e. $v_{\mathrm{a}}$ and $v_{\mathrm{b}}$), the traditional single-ended probes were carefully calibrated to ensure well-matched performance (i.e. $v_{\mathrm{s}}$ and $v_{\mathrm{id}}$).

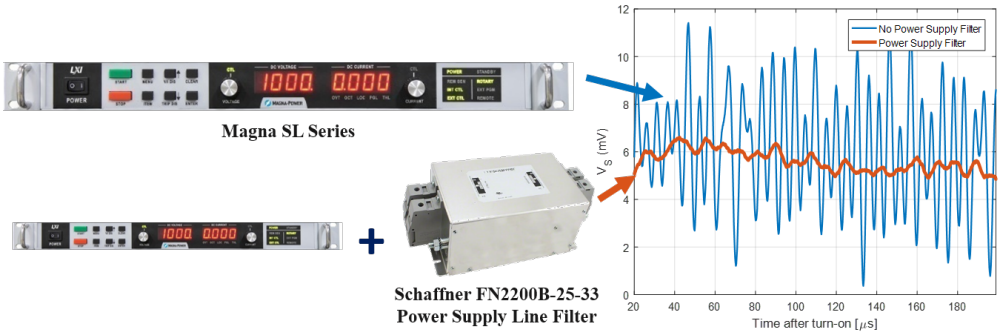


Figure 6.5: Incorporating a line filter isolates the testbed from noise currents emitted by the power supply.

to be determined from a thermal resistance network. The dc resistance calibration enabled verification of the heater settings sufficient to achieve specific junction temperatures in agreement with the trends provided by device manufacturers.

### 6.3.2 Standardized Testing Method

The experimental testbed shown in Figures 6.2b, 6.2c, and 6.6 was designed and assembled to evaluate the dynamic performance of commercial GaN transistors. To facilitate a large survey of low- and high-voltage GaN HEMTs described in Table 6.1, a custom adapter board for each DUT was developed as in Figure 6.7, which could be attached with low-temperature solder to the larger measurement circuit testbed. All devices evaluated as part of this study were purchased from distributors and none were engineering samples. In prior work, only high-voltage GaN HEMTS (i.e. maximum rated $V_{ds}$ = 650 V) have been investigated. Probing the dynamic $r_{\text{dson}}$ behavior of the 100 V and 200 V rated GaN devices from Table 6.1 serves two important purposes. While large voltage stress for a high-voltage GaN transistor clearly can induce electron trapping if not addressed at the device level, the severity of this second-order mechanism for lower voltage devices needs to be examined and quantified. Since the dynamic response could potentially be lower for this class of GaN transistors than for high-voltage components, testing this family of devices will also serve to illustrate the sensitivity of this dynamic $r_{\text{dson}}$ measurement method. The initial survey shared in [107] was expanded as part of this work to include additional low- and high-voltage

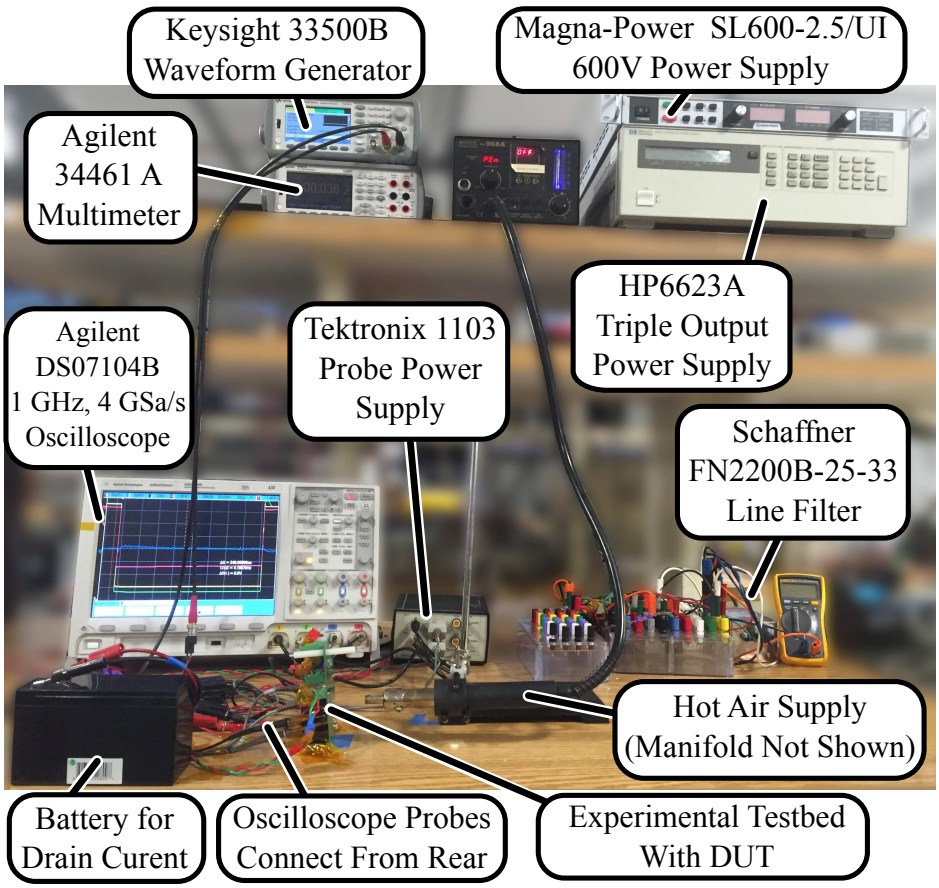


Figure 6.6: Experimental setup to probe $r_{\text{dson}}$ for varying voltage stress, temperature, drain current, and pulse shape.


Figure 6.7: Examples of custom adapter boards for: (a) EPC2016C, (b) GS61004B, (c) EPC2045, (d) EPC2033, (e) EPC2034, (f) EPC2047, (g) PGA26E07BA, (h) GS66508B, (i) TPH3208PS, and (j) IXFX230N20T.

devices enumerated in Table 6.1.

The full dynamic $r_{\text{dson}}$ characterization of a GaN HEMT begins with a standard dc on-state resistance measurement, $R_{\text{dson}}$, in order to establish a benchmark for the minimum $r_{\text{dson}}$ including all additional resistance contributions of the printed circuit boards. This initial measurement also ensures that a reliable contact exists between daughterboard and

motherboard. A dc power supply is used to provide a drain current of 1 A since this is a longer dc measurement and any oscillations from noise currents or transients will have decayed before the measurement is obtained. After adjusting the pulse-width for the conduction time to be 5 seconds, the four single-ended voltage measurements discussed earlier ($v_{\mathrm{a}}$, $v_{\mathrm{b}}$, $v_{\mathrm{id}}$, & $v_{\mathrm{s}}$) are obtained with an Agilent 34461A multimeter as depicted in Figure 6.8, which offers much better precision than the oscilloscope. These measurements were implemented for both low- and high-temperature operational cases (i.e. 25 °C and 75 °C). The resistance of the precision sense resistor was also gathered via a four-wire resistance measurement.

For a subset of the devices considered in this survey, a full factorial design-of-experiment involving 19 measurements was employed to investigate the impact of drain current, voltage stress magnitude, voltage stress time, and junction temperature. These 19 measurements include 16 corner-case measurement combinations and three intermediate measurement combinations to expose any curvature in the trends. The corner-cases for each DUT included: approximately 15% and 50% of the rated drain current, 12.5% and 95% voltage stress magnitude, 1 second and 2 minutes of voltage stress duration, and junction temperatures of 25 °C and 75 °C. In a typical application, a balance between trapping and de-trapping will exist during the off and on intervals respectively. A single soak time less than 1 second is therefore not an adequate representation of real applications conditions. Accurately capturing the dynamic $r_{\mathrm{dson}}$ response in an application requires the application-specific voltage switching stress over a longer time horizon than the typical trapping and de-trapping time constants. Thus, results from these application-specific experiments do not provide generalized insights about dynamic $r_{\mathrm{dson}}$ behavior. However, a single dynamic $r_{\mathrm{dson}}$ measurement with long soaking time will provide valuable information on the both the magnitude and time dependence of the de-trapping. These experimental results can serve as input both for estimating dynamic $r_{\mathrm{dson}}$ impact for a real converter application as well as for designing application-specific test setups for measuring dynamic $r_{\mathrm{dson}}$. While this experimental setup can be controlled for any soak time of interest, soak times greater than 1 second were employed for this study since they are common for investigations probing the fundamental physics of the trapping behavior for a GaN device [135]. Soak times of 1 second and 2 minutes were probed to ensure that only negligible

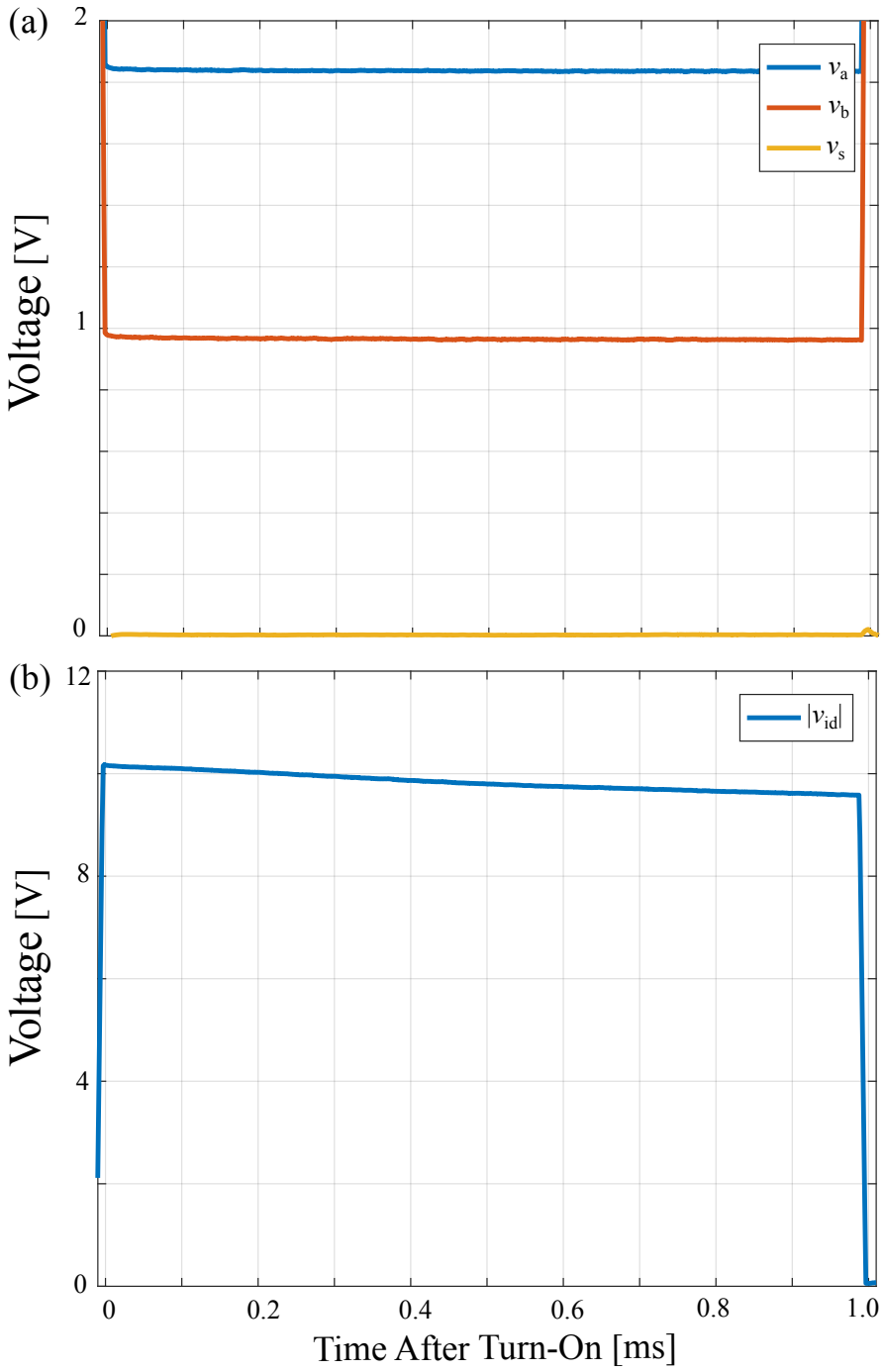


Figure 6.8: Measurements for Si MOSFET IXFX230N20T (24 V, 10 A) as an example of the measured switching waveforms made with the voltage clamping and drain current portions of the experimental setup.

differences existed between these two soak times. Experimental evidence highlighted that for these devices a 1 second soak time was sufficiently long to provide meaningful insight about de-trapping and dynamic $r_{\text{dson}}$

behavior. The intermediate measurement case involved 50% voltage stress for 1 minute with approximately 25-30% of the rated drain current and a junction temperature of 50 °C. To capture the longer decay mechanism for dynamic $r_{\text{dson}}$, these measurements were repeated for pulse-widths of 500 $\mu$s and either 10 ms for lower current or 1 ms for higher current due to the energy rating of the precision sense resistor.

This full factorial measurement method provides significant advantages over traditional approaches of changing one variable at a time and keeping the remaining variables fixed. In addition to reducing the number of measurements required, the results from this approach also clearly underscore the variables with the largest individual and potentially coupled impact on the dynamic $r_{\text{dson}}$ performance. Moreover, with the full factorial method, the measurements are taken in a random order each time to ensure that measurements are not impacted by latent variables not being considered or measurement artifacts from obtaining the measurements in a specific order. Thus, three intermediate measurement conditions, which are also randomly spaced throughout the experimental procedure, also serve as a reality check since no shift should exist between these measurements. Before each measurement, a background measurement with less than 12.5% applied voltage (only due to the voltage contribution of the batteries in the measurement circuit) was obtained. This additional procedural step served to further reduce the impact of prior measurements such that all measurements experienced the same experimental conditions. For all DUT, these background data points also agreed well with the $r_{\text{dson}}$ results obtained in the dc on-state resistance test and established the reference against which to compare the full factorial runs in order to establish the normalized change in $r_{\text{dson}}$. Initially, a gate resistance of 30 Ω was employed for all of the devices surveyed. These results strongly agree with measurements obtained with the recommended gate resistance from the manufacturer data sheet indicating that slew-rate did not have a significant impact for this hard-switching measurement condition. For the final survey, gate resistances were: 30 Ω for the EPC and Transphorm devices, 10 Ω for the GaN Systems devices, and recommended network of resistors and capacitors for the Panasonic device [136].

Since the magnitude of applied voltage stress was shown to have the most significant impact on the dynamic $r_{\text{dson}}$ performance based on the full

factorial preliminary experiments, a third experiment was conducted for each DUT in the survey where the other variables were fixed (e.g. 25% rated drain current, 2 minute voltage stress time, and 25 °C junction temperature) and the voltage stress was varied in a random order between 12.5% and 95% such that measurements for at least two additional intermediate voltages were obtained. Similar to the full factorial run, background measurements were also implemented. This standardized experiment helped validate the rate of change in dynamic $r_{\text{dson}}$ based on this important contributing variable. Depending on the results from the full factorial measurement analysis for the new generation of GaN switches, this third type of experiment where one variable is changed at a time can be repeated with other variables of interest if they are found to be significant contributing factors and the rate of change needs to be quantified in more detail.

## 6.4 Validating Experimental Setup

After obtaining the $v_{\text{ds}}$ voltage from the subtraction described in (6.1) and depicted in Figure 6.9, the dynamic $r_{\text{dson}}$ for all three testing procedures was found by dividing this voltage by the measured drain current for the DUT as shown in (6.5). In addition to the background runs obtained before each measurement for the DUT under stress, Si MOSFETs were also probed using the testbed to serve as a calibration tool. Figure 6.9 highlights that for a Si MOSFET no measurable dynamic $r_{\text{dson}}$ exists between the low and high voltage measurements. Since Si MOSFETs are known not to exhibit dynamic $r_{\text{dson}}$, these measurements for two different Si transistors underscore the background noise in the measurement and the impact of any latent sources of offset or delay during the different experimental conditions and from the measurement circuit. To provide more insight into the uncertainty of experimental measurements, the different error contributions were analyzed. Using standard techniques for error propagation [137, 138], the unique contributors of uncertainty were examined. For the Agilent DS07104B oscilloscope with an 8 bit ADC [139, 140], error due to the utilization of the vertical scale and the dc vertical offset accuracy were considered for all four voltage measurements. Also, the horizontal time resolution of 2.5 ps and a time-base accuracy of 15 ppm were incorporated into this analysis. Since

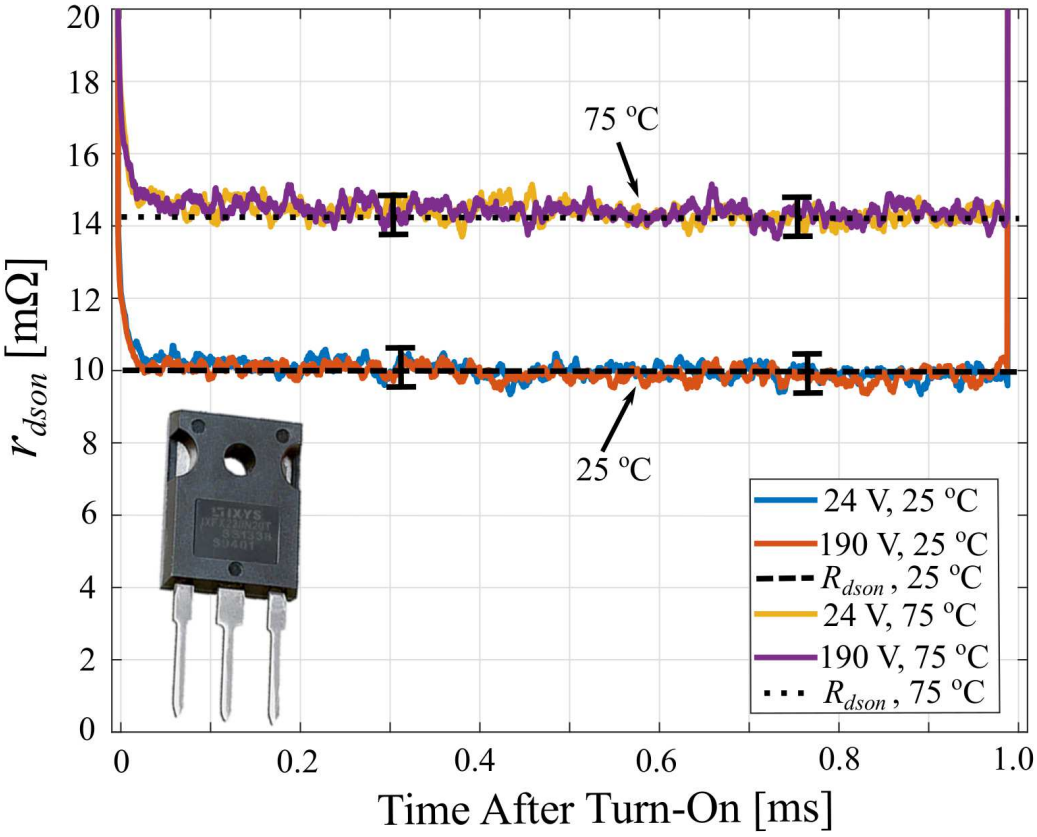


Figure 6.9: Measurements for Si MOSFETs (IXFX230N20T shown here and both the IRFP4668 and IPP65R125C7) revealed no dynamic $r_{\text{dson}}$ behavior between the reference (24 V, 24 A) and stressed conditions (190 V, 24 A) for both ambient and elevated temperatures. Strong significance exists between the dc $R_{\text{dson}}$ and the transient $r_{\text{dson}}$ measurements.

the resistance for $R_{id}$ was captured with a four-probe measurement using the Agilent 34461A multimeter, both range and read error were utilized [141].

Propagating the uncertainty for the measurement outlined in Sec. 6.3 involves rules for the subtraction of measurements in (6.4) and the division of measurements in (6.5). Realizing in this case that all sources of error are independent and random, the uncertainty for the addition or subtraction of measured values always is the sum in quadrature [137, 138]. Applying this observation to (6.4) yields

$$\delta v_{\text{ds}} = \sqrt{\left(|2| \cdot \delta v_{\text{b}}\right)^2 + \left(\delta v_{\text{a}}\right)^2 + \left(\delta v_{\text{s}}\right)^2}, \tag{6.6}$$

where $\delta$ signifies the uncertainty or margin of error for a specific instrument or measurement technique. If this assumption regarding the randomness and

independence of the margins of error did not hold for a different measurement method, (6.6) can be generalized where the resultant uncertainty is always less than or equal to the sum of these sources of error [138] as in

$$\delta v_{\mathrm{ds}} \leq |2| \cdot \delta v_{\mathrm{b}} + \delta v_{\mathrm{a}} + \delta v_{\mathrm{s}}. \tag{6.7}$$

In both cases, since the constant 2 has no uncertainty, the resulting uncertainty is the product of the margin of error for the measured value and the absolute value for the constant. The term $\delta v_a$ will be derived as an example of the information required for a detailed treatment of error, which can be applied to all of the other sources of error outlined in Sec. 6.4. For the Agilent DS07104B oscilloscope with a 30-minute warm-up period [139, 140], $\delta v_a$ is the sum of the dc vertical gain accuracy (i.e. 2% of the full scale considering 500 mV per division and 8 divisions is ±80 mV) and the vertical offset error (i.e. the sum of ±0.1 div, ±2 mV, and ±1.5% of the 3.12 V offset value is ±48.8 mV), which in this case is ±128.8 mV. For (6.5), margin of error is still based on addition in quadrature; however, the terms are the quotient of the error and the measurement [123, 137, 138] as in

$$\delta r_{\mathrm{dson}} = |r_{\mathrm{dson}}| \sqrt{\left(\frac{\delta v_{\mathrm{ds}}}{v_{\mathrm{ds}}}\right)^2 + \left(\frac{\delta v_{\mathrm{L}}}{v_{\mathrm{L}}}\right)^2 + \left(\frac{\delta i_{\mathrm{d}}}{i_{\mathrm{d}}}\right)^2}. \tag{6.8}$$

Combining the contributions of these sources of error underscored that the propagated experimental uncertainty for this dynamic $r_{\mathrm{dson}}$ measurement method is less than +/- 2.2% of the final resistance value [137, 138].

An example of the dynamic $r_{\mathrm{dson}}$ response for an EPC2034 GaN device for a specific set of experimental conditions (12 A drain current, a 10 ms pulse-width) is depicted in Figure 6.10 for two different voltage stress levels (0.12 and the maximum 0.95 of the rated voltage respectively, as well as two different junction temperatures, 25 °C and 75 °C). Depending on the device design and ratings as well as the intended switching frequency, this degree of increase due to dynamic $r_{\mathrm{dson}}$ varies. In contrast, the Si MOSFET evaluated with the same measurement setup did not display any dynamic $r_{\mathrm{dson}}$, which supports the hypothesis that the measured results for the GaN switches correspond to dynamic $r_{\mathrm{dson}}$ and not a measurement artifact.

Figure 6.10 also underscores how for a fast timescale, the dynamic $r_{\mathrm{dson}}$ has not decayed back to the dc $R_{\mathrm{dson}}$. Yet, the full decay of the $r_{\mathrm{dson}}$ back to

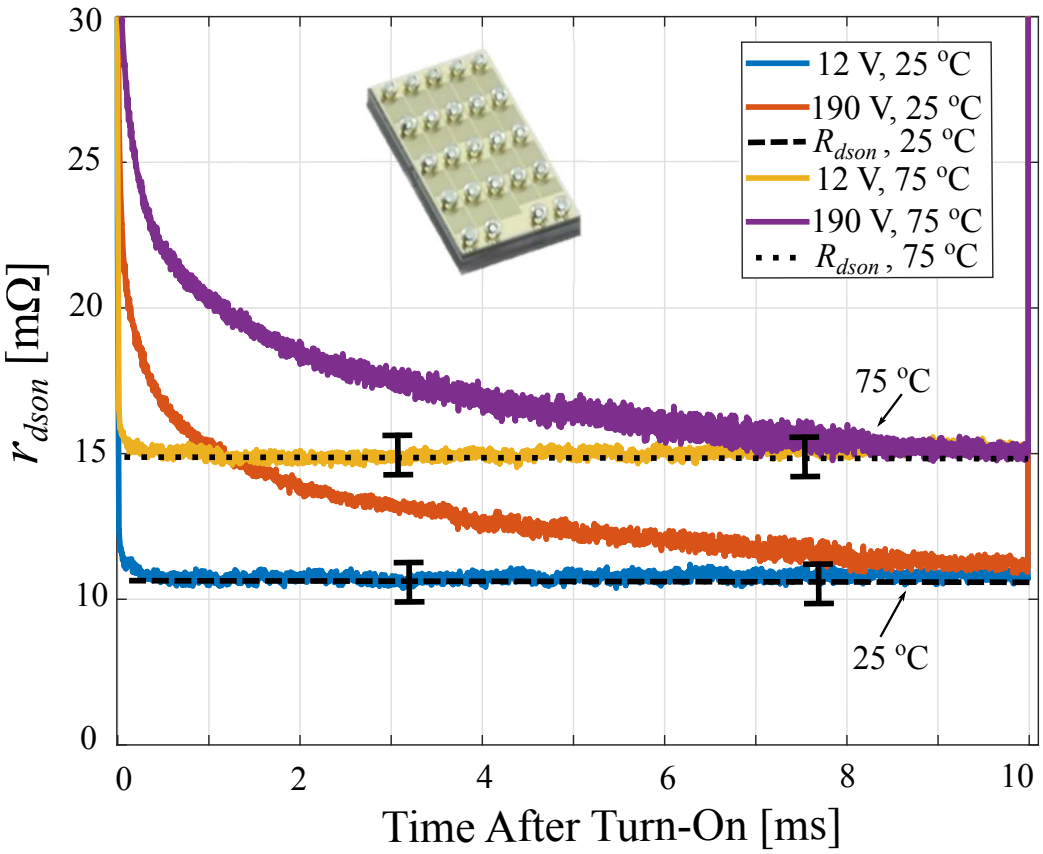


Figure 6.10: In contrast to Si MOSFETs, measurements for the EPC2034 GaN device underscore significant dynamic $r_{\text{dson}}$ between the reference case (12 V, 12 A) and stressed condition (190 V, 12 A) with varying package temperature. The 10 ms pulse length demonstrates the full decay of $r_{\text{dson}}$ during stressed conditions back to the reference $R_{\text{dson}}$.

the $R_{\text{dson}}$ value for approximately 20% of the rated drain current and varying junction temperatures was achieved in approximately 10 milliseconds. This dynamic behavior also exists for higher drain currents, but the energy rating of the precision sense resistor must be considered in order to set the measurement pulse length. Large differences in the amount of time required for each DUT to achieve full decay of this dynamic $r_{\text{dson}}$ for large voltage stress have been observed. While some devices decayed back in a few hundred microseconds, other technologies required more than 10 milliseconds, which agrees with the slow timescale behavior described in the literature.

Since the major market for GaN transistors involves switching frequencies ranging from 100 kHz to 10 MHz, the devices will never be conducting long enough for full de-trapping to occur. Consequently, the $R_{\text{dson}}$ obtained either

from the manufacturer datasheet or a dc lab measurement will not accurately describe the higher $r_{\text{dson}}$ exhibited during the switch transition. Thus, a new method to incorporate dynamic $r_{\text{dson}}$ into the modeling, optimization, and design of power converters is required.

## 6.5 Quantifying $r_{\text{dson}}$ for Converter Design

### 6.5.1 Summary of Analysis Method

Regardless of the clamping circuit or experimental testbed employed (e.g. double pulse, Figure 6.2, etc.), quantifying dynamic $r_{\text{dson}}$ behavior on a manufacturer datasheet with plots and metrics, which capture the impact of de-trapping time, varying voltage, and junction temperature, would provide valuable insight for power converter development. Plotting dynamic $r_{\text{dson}}$ measurements with a logarithmic timescale as in Figure 6.11 simplifies the visualization of the decaying $r_{\text{dson}}$ for pulse-widths, $td$, of interest to power electronics designers which are significantly shorter than the length of the original measurement. A second aspect of translating this measurement involves normalizing the response for each voltage condition by either the dc $R_{\text{dson}}$ or background low-voltage (e.g $v_{ref}$ = 12 V or 24 V) dynamic $r_{\text{dson}}$ measurement as in

$$N(v_{ds}, t) = \frac{r_{\text{dson}}(v_{ds}, t)}{r_{\text{dson}}(v_{ref}, t)} \approx \frac{r_{\text{dson}}(v_{ds}, t)}{R_{\text{dson}}}, \tag{6.9}$$

Normalizing the applied $V_{ds}$ enables a fair comparison of GaN devices with different maximum device ratings such as 100 V and 200 V. Moreover, normalizing measurements has also been shown to reduce the impact of bias or fixed uncertainty on sensitive experimental measurements [142]. Utilizing the low-voltage reference measurement to determine normalized change helps capture the impact of the effective bandwidth for very small pulse-widths based on the combination of clamping circuit, probes, and oscilloscope. For a specific $td$, a maximum normalized change in the dynamic $r_{\text{dson}}$,

$$N_{m,td} = N(v_{ds}, t)|_{(v_{ds},t)=(0.95v_{rated},td)}, \tag{6.10}$$

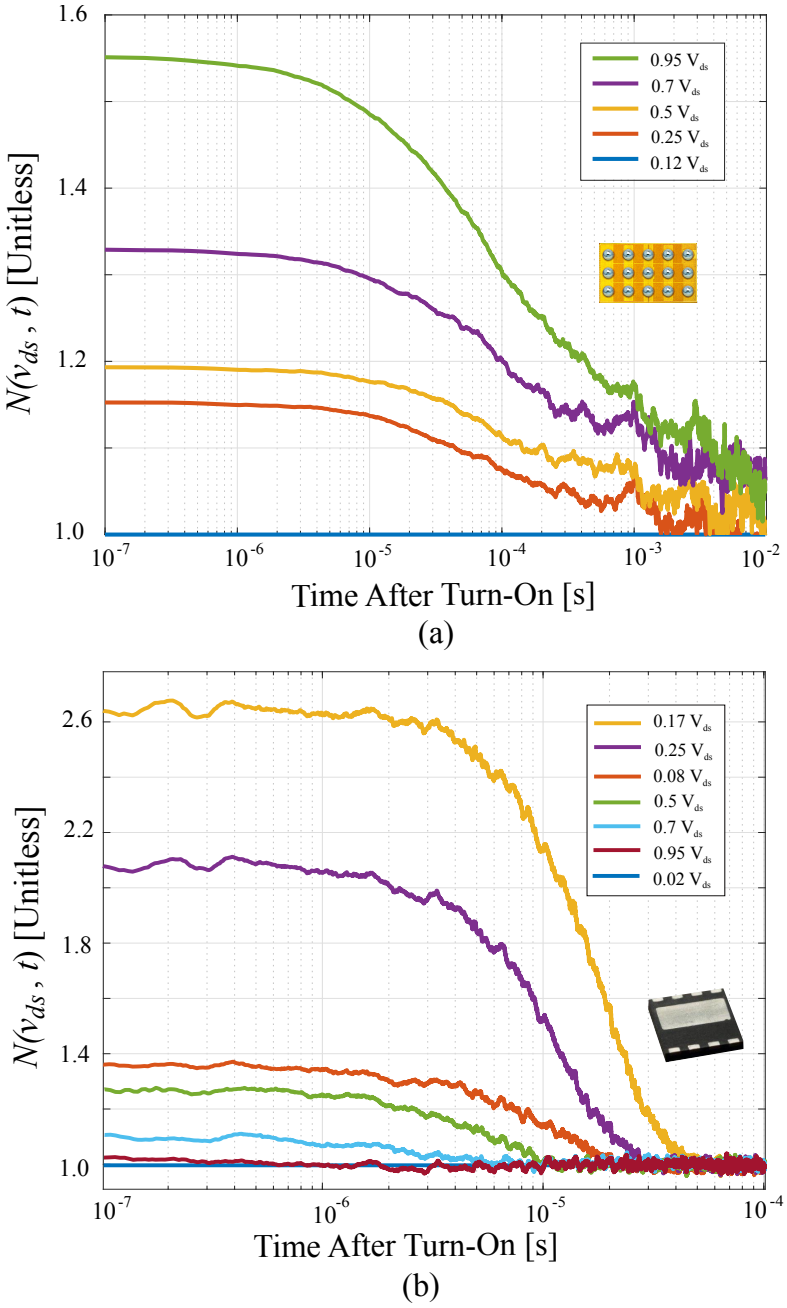


Figure 6.11: Examining the normalized change in $r_{\text{dson}}$, $N(v_{ds}, t)$, enables the worst-case change, $N_{m,td}$, corresponding to 95% voltage and 50% current stress to be scaled for the pulse-width, $td$, and voltage stress of interest by obtaining the slope, $\Delta N/\Delta V_{\text{ds}}$, through measurements for several voltage stress conditions. Interestingly, the trend with increasing voltage has a positive slope for low-voltage technologies like the EPC2045 device (a) and a negative behavior for several of the high-voltage technologies such as the Panasonic PGA26E07BA device (b).

for the worst-case stress conditions can be identified. Stressing the device with 95% of the rated voltage and 50% of the rated current was selected intentionally in this analysis. In practical designs, GaN transistors are operated with some voltage margin to account for transients, overshoots, and drain-source voltage ringing. Thus, 95% of the rated voltage stress is a reasonable condition for this worst-case metric when this voltage margin is considered. Similarly, since these wide bandgap devices are often thermally limited, testing with 50% of the rated current is representative of specifications for many intended applications while still being much below the dc current rating.

Yet, the single worst-case metric alone is not sufficient to describe the unique behavior of every device over the usable voltage range. For any given $td$, the slope, $\Delta N/\Delta V_{\mathrm{ds}}$, is also required to understand how the normalized change in $r_{\mathrm{dson}}$ scales for different voltage stress. Given the point (0.95, $N_{m,td}$) and the $\Delta N/\Delta V_{\mathrm{ds}}$, a designer can determine the normalized change in $r_{\mathrm{dson}}$ for different potential operating frequencies, duty cycles, and voltages in their design. Thus, if plots like Figure 6.11 are not provided, then $N_{v,td}$ can be found from

$$N_{v,td} = \frac{\Delta N}{\Delta V_{\mathrm{ds}}}\left(\frac{V_{ds}}{V_{rated}} - 0.95\right) + N_{m,td}. \tag{6.11}$$

Just like all other parameters provided on a data sheet, the $\mathrm{N}_{m,td}$ and $\Delta N/\Delta V_{\mathrm{ds}}$ metrics proposed here are being quoted for ambient conditions. Therefore, the final analysis step for designing with dynamic $r_{\mathrm{dson}}$ in mind requires accounting for the elevated junction temperature during converter operation. The temperature and dynamic $r_{\mathrm{dson}}$ effects are mainly due to different factors that are temperature dependent (i.e. increased buffering trapping [114, 135, 143], reduced electron saturation velocity [144, 145], and reduced channel width [115]). Therefore, although a compound model separating temperature and dynamic voltage dependency factors is suitable to first-order, the trapping and de-trapping behavior can be expected also to show some second-order temperature dependency. Elevated temperature testing of the devices has highlighted that composite on-state resistance behavior including higher temperature can be modeled by

$$r_{\mathrm{c}} = N_{\mathrm{v,td}}\Delta_{\mathrm{Tj}}R_{\mathrm{dson}}, \tag{6.12}$$

where $\Delta_{\mathrm{Tj}}$ is the normalized increase in the $R_{\mathrm{dson}}$ due to junction temperature from the data sheet. Experimental evidence highlights that this composite model accurately captures the dynamic $r_{\mathrm{dson}}$ behavior for all of the devices incorporated in this study and the trend of increasing dynamic $r_{\mathrm{dson}}$ with increasing temperature agrees with observations in the literature [114, 135, 143]. This $r_{\mathrm{c}}$ is the resistance that should be used for conduction loss modeling and comparison with other devices during design.

To demonstrate how the proposed metrics can be incorporated into the design process, consider the following operational constraints: 80 V maximum drain voltage, 100 kHz switching frequency, duty ratio of 50%, RMS current of 16 A, and sufficient cooling to maintain a junction temperature of 100 °C. Thus, the 100 V EPC2045 device is a suitable candidate for additional analysis. Examining the $0.95v_{ds}$ measurement from Figure 6.11a at $td = 5$ $\mu$s enables a designer to apply (6.10) and determine $N_{m,td} = 1.51$. The slope $\Delta N/\Delta V_{\mathrm{ds}} = 0.536$ can be found by repeating this process for the other voltage stress measurements in Figure 6.11a. For $v_{ds}/v_{rated} = 0.8$, (6.11) yields $N_{v,td} = 1.42$. Next, $R_{\mathrm{dson}}$ and $\Delta_{\mathrm{Tj}}$ are determined either from laboratory measurements or an examination of the manufacturer datasheet [146] to be 7 m$\Omega$ and 1.45 respectively. While a traditional estimate for $R_{\mathrm{dson}}$ at the elevated junction temperature would be 10.2 m$\Omega$, (6.12) highlights that the composite resistance incorporating dynamic $r_{\mathrm{dson}}$ is $r_c = 14.5$ m$\Omega$. Therefore, the estimates of conduction loss for this switch with the traditional and composite method are 2.6 W and 3.7 W respectively. This enhanced understanding of losses is important for the design of ultra-high-efficiency converters where every watt of loss matters, or multilevel converters where this conduction loss would be further magnified by a network of switches.

### 6.5.2 Observations from Applying Proposed Analysis Approach

Figures 6.12 and 6.13 underscore how visualizing $N_{m,td}$ and $\Delta N/\Delta V_{\mathrm{ds}}$ with a plot facilitates both insightful comparison of different device technologies and design. First, these plots help reinforce the value of Si MOSFETs as calibration tools since they exhibit $N_{m,td} = 1$ and $\Delta N/\Delta V_{\mathrm{ds}} = 0$. Moreover,

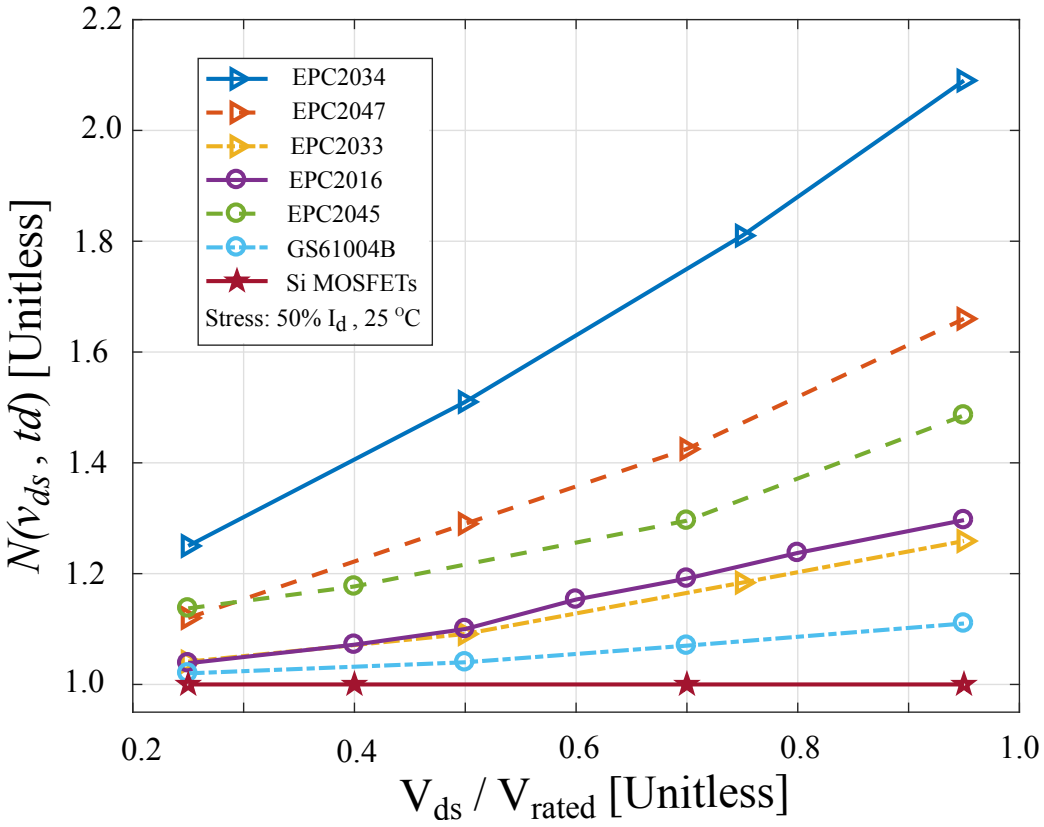


Figure 6.12: A survey of commercial low-voltage GaN devices highlights that dynamic $r_{\text{dson}}$ is still an important consideration for designing with GaN transistors and low-voltage technologies exhibit a positive slope for $\Delta N/\Delta V_{\text{ds}}$. The analysis for this plot was implemented for 5 $\mu$s after the device had turned on. The maximum normalized change in $r_{\text{dson}}$, $N_{m,td}$, is dependent on the amount of allowed de-trapping time after the device turns on. Thus, these curves should be generated for pulse-widths of interest for the application.

viewing the measurements in this way enables rapid interpolation of $N_{v,td}$ for any drain voltage stress. Figure 6.12 underscores how the normalized change in dynamic $r_{\text{dson}}$ for the low-voltage commercial GaN devices was found to increase linearly with normalized voltage stress across the device. Thus, reducing the applied $V_{ds}$ for these devices enables a reduction in both switching and conduction losses. Two of the high-voltage devices surveyed exhibited dramatically different responses to increasing $V_{ds}$ as shown in Figure 6.13. The change in dynamic $r_{\text{dson}}$ increased rapidly and peaked for low $V_{ds}$ ($V_{ds} \leq 0.3$), decayed for median $V_{ds}$ ($0.3 < V_{ds} \leq 0.7$), and plateaued for higher applied $V_{ds}$ ($0.7 < V_{ds} \leq 0.9$). Overall, the impact of

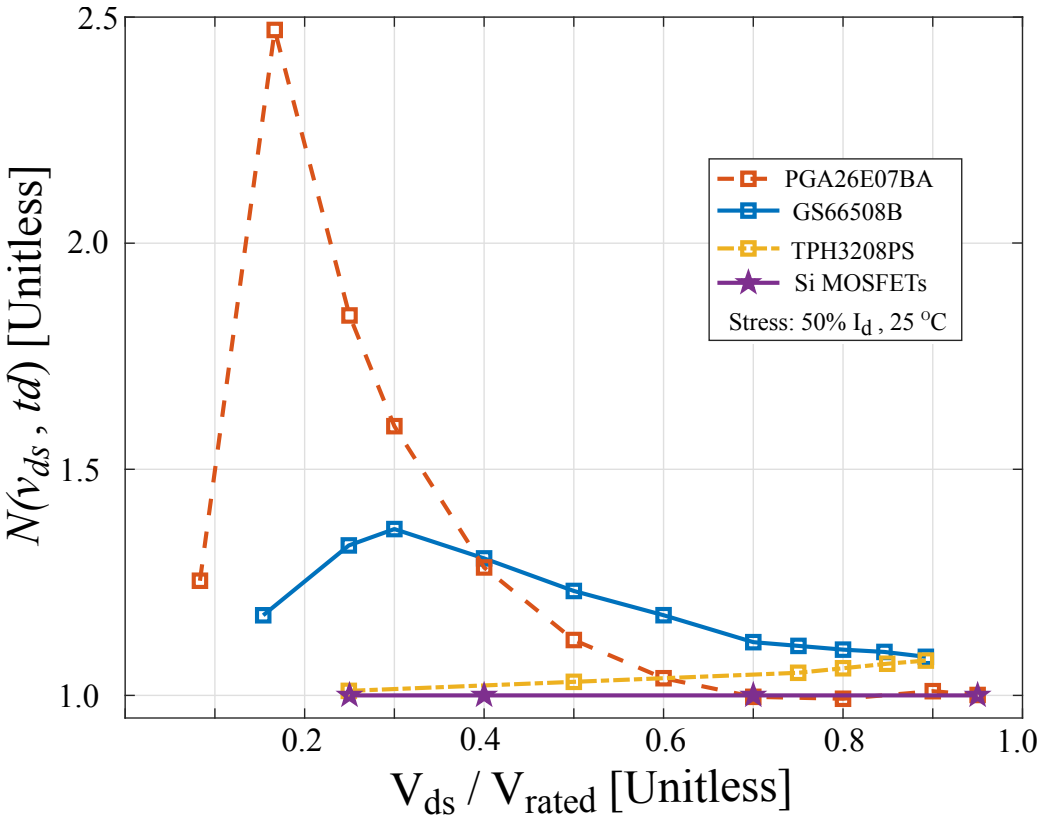


Figure 6.13: A survey of commercial high-voltage GaN devices highlights that dynamic $r_{\text{dson}}$ underscores that some manufacturers are tackling dynamic $r_{\text{dson}}$ such that negative slopes for $\Delta N/\Delta V_{\text{ds}}$ exist. Scaling $N_{m,td}$ for the voltage stress employed in a converter, $N_{v,td}$, with a 5 $\mu$s pulse-width can be obtained from this plot.

dynamic $r_{\text{dson}}$ decreased with higher $V_{ds}$ stress. From a design perspective, these trends highlight that care should be taken when utilizing these switches in applications with $V_{ds} < 0.7$ because an attempt to reduce switching losses with lower $V_{ds}$ would result in an increase in conduction losses with the higher composite $r_{\text{c}}$. Overall, these trends also suggest that different tools are being employed by device manufacturers to mitigate dynamic $r_{\text{dson}}$ for the low- and high-voltage device regimes.

Additionally, for a power device designer, $\Delta N/\Delta V_{\text{ds}}$ and $N_{m,td}$ provide another tool for tracking the generational improvement of their manufacturing and design techniques for reducing dynamic $r_{\text{dson}}$ behavior. For example, the generational improvements in performance between some of the low-voltage devices is evident both from a lower $\text{N}_{m,td}$ and a smaller $\Delta N/\Delta V_{\text{ds}}$ (i.e. between EPC2034 and EPC2047 the $N_{m,td}$ and $\Delta N/\Delta V_{\text{ds}}$

improved). Also, since device manufacturers cannot predict all of the innovative ways converter designers might utilize their GaN transistors, providing detailed slope information for the high-voltage devices will enable converter designers to make informed design and control decisions when operating these devices anywhere within the voltage ratings.

Using the proposed analysis approach, the impact of dynamic $r_{\text{dson}}$ for GaN-based converters switching over 100 kHz was found to be in strong agreement with predicted and measured losses for a multi-level converter utilizing low-voltage GaN transistors [101, 147]. While the measurement setup was found to be robust and repeatable, some variation in $N_{m,td}$, $\Delta N/\Delta V_{\text{ds}}$, and the estimated final de-trapping time was observed for some of the devices of the same type from different supply lots purchased from distributors. The observed variation between lots was significantly larger than the variation within each lot, which supports how this analysis approach could aid part acceptance sampling for power supply manufacturing. This experimental observation also underscores that a study with a larger sample size of lots for each device is required to develop a plot like Figure 6.11 for each technology at different junction temperatures so that a converter designer can apply this proposed analysis method themselves and to document $N_{m,td}$ and $\Delta N/\Delta V_{\text{ds}}$ for quick device comparison. If GaN device manufacturers are hesitant to share raw data like Figure 6.11, then providing metrics like $N_{m,td}$ and $\Delta N/\Delta V_{\text{ds}}$ or plots like Figures 6.12 and 6.13 for a few representative pulse-widths (e.g. 10 $\mu$s, 1 $\mu$s, and 0.1 $\mu$s) and junction temperatures would also enable converter designers to account for dynamic $r_{\text{dson}}$ during power supply development.

## 6.6 Conclusions & Future Work

After reviewing physical explanations for dynamic on-state resistance in GaN transistors and providing historical context for this issue, the merits and drawbacks of prior published approaches for measuring this phenomenon were discussed. Prior work has focused on low delay and offset measurements of drain voltage, but has not outlined the best-practices for the overall dynamic $r_{\text{dson}}$ measurement or enabled the probing of various independent variables such as device voltage stress, drain current, junction temperature, and device

on/off time (along with the duty ratio of these pulses). The proposed measurement circuit and testing method facilitates independent control of these four variables. The full factorial measurement protocol described not only examines the corner-cases for the device performance, but also facilitates a quantitative investigation of the interaction for these variables. Experimental evidence of dynamic $r_{\text{dson}}$ for a survey of commercial, low-voltage and high-voltage GaN transistors underscored a substantial increase in dynamic $r_{\text{dson}}$ depending on the device and operating conditions. While continued academic and industrial research investment is required to retire the risks of dynamic $r_{\text{dson}}$ completely, measurable improvements in both of the proposed dynamic $r_{\text{dson}}$ metrics were observed for the newer generation of GaN transistors considered in this study. The two metrics for quantifying dynamic $r_{\text{dson}}$ in a useful way for power supply design were outlined in order to aid in modeling of dynamic on-state resistance induced losses by converter designers. Through an applied example, the utility of incorporating these measurements into the design of an ultra-high-efficiency or conduction loss limited converter design was demonstrated. Future work with higher bandwidth clamping circuits can build on this method by examining how the soft- and hard-switching responses behave for even shorter time-scales, which will capture both fast and slow de-trapping effects.

All in all, providing these types of plots or tables for these metrics in GaN device data sheets is vital to realizing the full potential of GaN devices in the next generation of power electronics. This work contributes meaningfully to the discussion among GaN manufacturers, academics, power suppliers, and the JEDEC JC-70.1 committee about standard techniques for GaN characterization, reliability analysis, and converter design by providing some metrics and simple steps for analysis. Even as lateral GaN device designs and manufacturing methods improve in time [148] and vertical GaN devices with inherently lower trapping behavior [149, 150] are adopted, the proposed metrics can benchmark these advancements and catch defects as part of quality assurance for power supply manufacturing. Quantifying the performance of GaN devices with standardized metrics facilitates a fair comparison between different GaN device technologies during converter development, enables manufacturing qualification for GaN switches, and provides a benchmark to catalyze improvement for the next generation of GaN and ultra-wide-bandgap device development.

# CHAPTER 7

# PROBING LOSS MECHANISMS IN CRYOGENIC ENVIRONMENTS

*Science is a field which grows continuously with ever expanding frontiers. Further, science is a collaborative effort and the combined results of several people working together is always much more effective than could be that of an individual scientist working alone.*

– John Bardeen, 1908-1991 (Nobel Prize 1956, 1972)

## 7.1 Introduction

Both traditional and emerging applications for power electronics demand lightweight, compact, ultra-low-loss, and extreme-temperature-capable solutions. To enable improvements for these figures of merit, power electronics designers have pursued higher operating switching frequencies, advanced circuit topologies, and cutting-edge materials for heat transfer, active devices, and passive components. For example, new wide-bandgap semiconductor materials, such as silicon carbide (SiC) and gallium-nitride (GaN), have catalyzed significant progress toward these goals [68, 151, 152]. In contrast to silicon, GaN offers several advantages when high power density and high efficiency are needed such as lower on-state resistance and parasitic capacitances [153]. Combining wide-bandgap power devices with low-temperature operation is one potential avenue for catalyzing additional increases in these figures of merit since the conduction losses of components will decrease with operating temperature [154–156].

Low-temperature-compatible power electronics have a broad array of applications. For deep space probes and satellites, power electronics are a critical interface between the energy source and subsystems such as sensors or communication electronics. Yet, these converters are often packaged next to sources of heat such as auxiliary heating units or radioisotope thermoelectric generators due to uncertainty about their cryogenic performance [157, 158]. Insight about converter performance and improvements in power density at

cryogenic temperatures also has the potential to benefit many hybrid and more-electric transportation systems. Power density is especially important for the electrification of aircraft [159, 160]. Ultra-light, compact, cryo-cooled superconducting electric machines hold great promise for catalyzing the electrification of aircraft [161–164], and in this scenario, the power electronics could be cooled by the existing cryo-cooling hardware. Converters compatible with cryogenic temperatures could also be packaged much closer to these superconducting machines, which would further increase the power density and viability of the final powertrain.

Collaborative measurements of dc $R_{dson}$ and threshold voltage of GaN transistors at cryogenic temperatures ($< -140$ °C) highlighted a 5X reduction in dc $R_{dson}$ with no deleterious change in threshold voltage, which suggested that operating a converter limited by conduction losses at cryogenic temperatures could offer benefits for efficiency [165]. Yet, after testing a flying capacitor multilevel converter under these extremely cold conditions, the measured losses for the complete converter did not decrease as expected [166]. Thus, the dynamic $r_{dson}$ testbed from Chapter 6 was modified to understand how the transient loss mechanisms, which had not been previously examined, changed for cryogenic conditions.

## 7.2 Probing GaN Transistor Losses at Cryogenic Temperatures

One of the challenges of low-temperature power electronics is the condensation and icing which can form. In order to prevent this, the loss measurement testbeds were placed inside of a Kurt Lesker vacuum chamber, which was purged with nitrogen gas in order to displace any humid air in the chamber with dry nitrogen. Depicted in Figure 7.1, each loss evaluation circuit was attached to a cold plate and cooled by drawing liquid nitrogen (LN2) through the setup using a pump. Thermocouples were attached directly to the circuit board near the device under test and on the cold plate in order to track the temperature of the setup, which varied between $-140$ °C and 25 °C depending on the flow rate of the LN2 pump. First, the change in $R_{dson}$ was tracked with decreasing temperature and the results agreed, with strong significance, with measurements gathered previously with

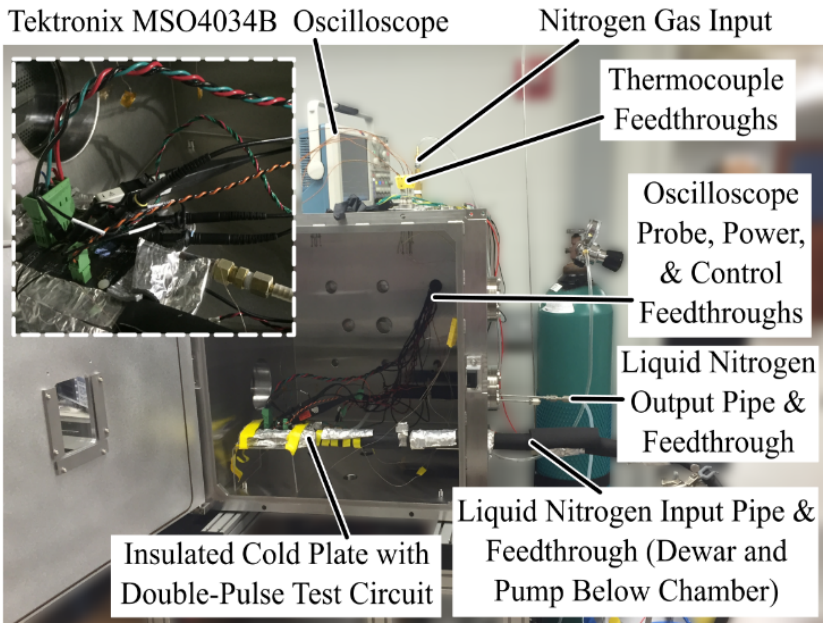


Figure 7.1: Chamber employed to enable evaluation of GaN device loss mechanisms at cryogenic temperatures.

a Lake Shore vacuum probe station [165]. This validated that the custom experimental setup constructed to investigate the switching and dynamic $r_{dson}$ losses had the same environmental conditions as the probe station for the $-140$ °C and 25 °C temperature range.

Next, a double-pulse test circuit was utilized to track the change in switching energy based on junction temperature. This traditional experiment enables turn-on and turn-off switching energy measurements for a device under test with the same current and voltage stress conditions. This is accomplished by ramping up the inductor current of a half-bridge module during the first pulse and capturing the turn-off measurement at the end of this pulse. When the device under test is off, the complementary device in the half-bridge, which is connected directly across the inductor, conducts and maintains a path for inductor current to flow. The turn-on transition is measured at the beginning of the second pulse. By integrating the overlap of drain current and drain-to-source voltage during each switch transition, an estimate of the energy dissipated can be obtained [167]. Unlike the dc $R_{dson}$, Figure 7.2 shows the normalized energy for both turn-on and turn-off did not change significantly with decreasing junction temperature. While switching losses were clearly not the source of the unexplained losses observed for the converter at cryogenic temperatures, this loss profile also underscored that

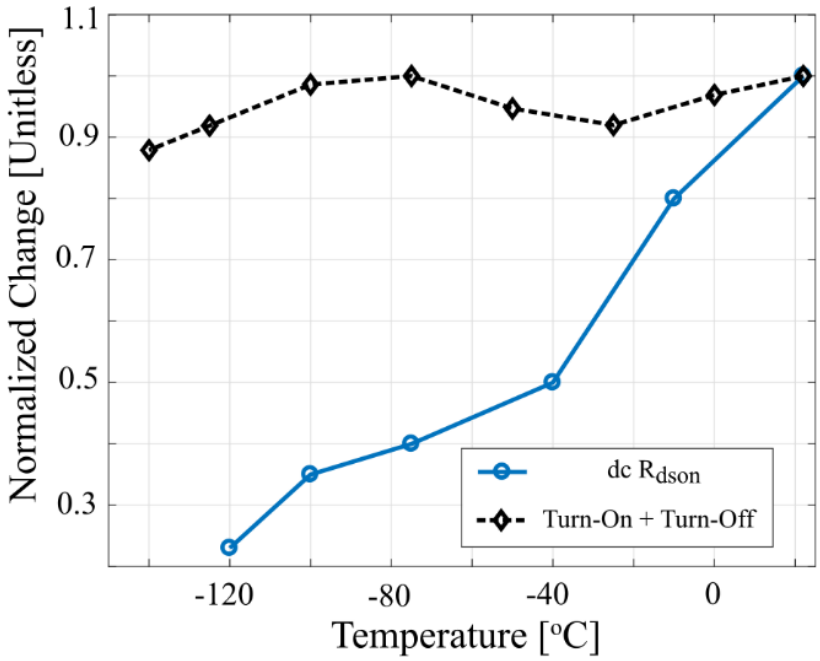


Figure 7.2: Switching losses did not decrease significantly with lower junction temperature.

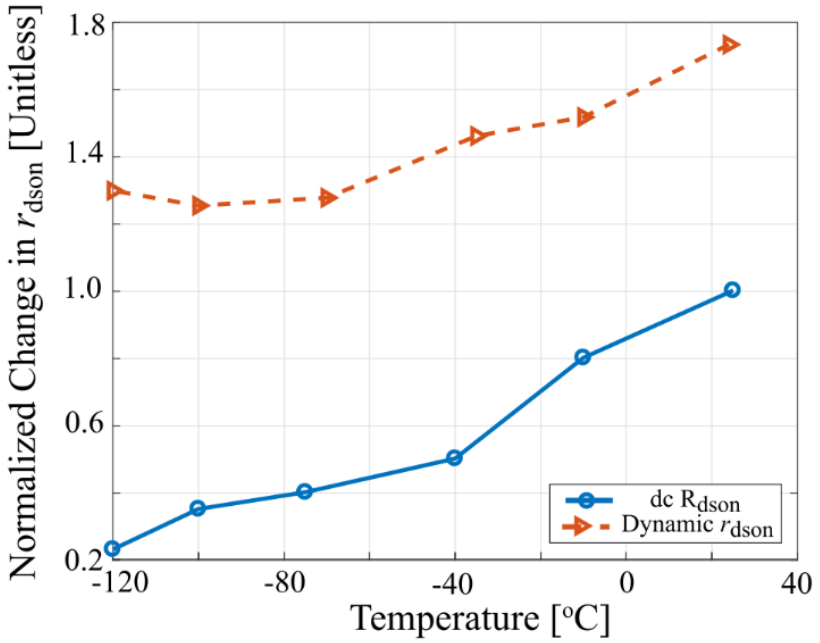


Figure 7.3: The decrease in dynamic $r_{dson}$ with temperature was not as pronounced as the 5X reduction in dc $R_{dson}$.

the device was able to switch without degradation in switching performance for the entire temperature range of interest.

Subsequently, the behavior of dynamic $r_{dson}$ with decreasing junction temperature was probed. Measurements for different voltage stress conditions were obtained at each junction temperature in order to apply the analysis method proposed in Chapter 6. While the overall normalized change in dynamic $r_{dson}$ did decrease at cryogenic temperatures, the composite result for large voltage stress highlighted in Figure 7.3 underscores that the change for the dynamic $r_{dson}$ is not the 5X reduction anticipated by the dc $R_{dson}$ measurements obtained from prior work. Although the higher conduction losses predicted from these measurements do not fully account for the anomalous losses observed for the complete converter, these observations do highlight that loss behavior of GaN transistors is more complex than initially anticipated by the first-order characterization results and warrants future examination once newer generation of GaN devices are commercially available.

## 7.3 Conclusion

After constructing and calibrating a custom cryogenic power device characterization testbed, the switching loss and dynamic $r_{dson}$ loss profiles for decreasing temperature from ambient (25 °C) to cryogenic (−140 °C) conditions were obtained. Neither the changes in switching loss nor those in conduction loss on account of dynamic $r_{dson}$ were enough to account for the anomalous losses measured for the complete power converter [166], which suggests that future work should examine second-order loss effects for other components in the converter in more detail. All in all, the experimental methods and measurement best-practices for characterizing power devices at cryogenic temperatures are general and can serve as a foundation for future studies evaluating next-generation wide-bandgap and ultra-wide-bandgap devices currently under development by industrial, government, and academic labs [74].

# CHAPTER 8

# FUNDAMENTAL LIMITS OF JUMPING DROPLET HEAT TRANSFER

*I don't know anything, but I do know that everything is interesting if you go into it deeply enough.*

– Richard Feynman, 1918-1988 (Nobel Prize 1965)

## 8.1 Introduction

Heat generation is the key obstacle to electrification of mobile and stationary systems classically controlled or propelled by mechanical and pneumatic processes [98–101, 159, 160, 168, 169]. As the surface area for cooling these electronic systems reduces due to packaging and integration constraints, traditional cooling pathways, such as conduction through a thermal interface material (TIM) and convection either to air or liquid inside of a cold plate, are unable to remove the required amount of heat while keeping the package within safe temperature operating limits [79, 98–101, 168–172]. In contrast, thermal management approaches such as phase-change cooling have found growing industrial application due to the potential for extracting heat as well as providing several unique system-level design benefits like buffering energy from temporally and spatially changing hotspots via the deployment of thermal energy storage [170–175]. Liquid-vapor phase-change cooling has significant potential to facilitate the development of

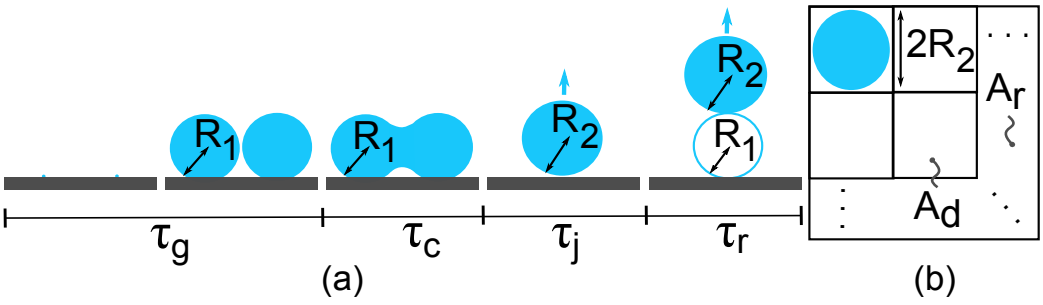


Figure 8.1: (a) Schematic of droplets undergoing droplet growth ($\tau_g$), coalescence ($\tau_c$), initial jump ($\tau_j$), and release ($\tau_r$) within (b) unit cells of a larger reference area as viewed form the top.

highly dense electronics by leveraging the large latent heat ($h_{fg}$) of working fluids during phase transition [1, 173–182]. As shown in Figure 8.1a, a promising form of liquid-vapor phase-change is jumping droplet condensation [1, 176–181, 183–188]. Droplet jumping initiates with isolated droplet nucleation and growth during condensation on a cooled, suitably-designed superhydrophobic surface. When neighboring droplets begin to coalesce, the merged droplet converts excess surface energy into kinetic energy, and ejects from the cold surface independent of gravity due to capillary-inertial energy conversion [1, 174–179]. Once coalesced, cold droplets reach the hotspot, heat is extracted from the electronic components via evaporation and is subsequently returned and spread to the original cold surface via condensation [1, 174–180, 182–184, 186, 189–193].

Liquid-vapor phase-change cooling is especially appealing for buffering the low-grade heat dissipated by electronics since the high heat transfer coefficients characteristic of evaporation and condensation ($\approx$100 kW/(m$^2$·K)) can transfer the largest amount of heat for the lowest temperature difference. While the upper bound of boiling heat flux has been identified as the sonic limit [194–196], defined by the maximum speed with which the vapor could depart from the surface allowing fresh, cold liquid to quench the hot surface and to form new bubbles, the fundamental limits of jumping droplet condensation have not been explored. In this work, we demonstrate that a delicate combination of droplet growth, coalescence dynamics, and fluid thermophysical properties governs jumping droplet heat transfer performance. A majority of recent works [1, 174–180, 182–184, 186, 189–193] have focused exclusively on water as the working fluid. Here, in addition to water, we analyze and identify a wide range of available working fluids, such as liquid metals, and demonstrate how these materials perform in directed cooling applications.

## 8.2 Analyzing the Important Timescales Impacting Jumping & Heat Flux

In order to elucidate the heat transfer physics governing jumping droplet condensation, we first consider that the maximum amount of heat extracted

This chapter includes work published in part in [197].

via evaporation from hot transistors is determined primarily by the number of cold droplets that strike the surface per unit time. As a vapor chamber is a closed system, the control volume can be drawn at the perimeter of the cold surface and the number of droplets leaving the surface per unit time can be examined without loss of generality. Figure 8.1a depicts the four key steps and their associated timescales governing droplet jumping: individual droplet growth ($\tau_g$), coalescence ($\tau_c$), initial jumping ($\tau_j$), and the time required for the ejected droplet to reach a distance of one radius from the cold surface, or release ($\tau_r$). After initial nucleation, $\tau_g$ captures the amount of time required for a droplet to grow large enough for coalescence with a neighboring droplet of equivalent size [198,199]. Once the neighboring droplets have bridged and combined, $\tau_c$, additional time is required for the resulting droplet to eject from the surface, $\tau_j$ [200, 201]. The release time portion of this process seeks to avoid the intersection of a droplet leaving the surface with a droplet growing rapidly underneath it due to the presence of residual liquid within structures remaining after departure and hence re-nucleation and growth at the same spot [178–180, 182–184, 184, 185]. The release time consideration accounts for the case of immediate recoalescence and infinitely fast droplet growth. This is an important modeling assumption required to bound the complexity of the jumping dynamics considered in this work. When combined, these four timescales comprise the complete jumping timescale,

$$\tau_t = \tau_g + \tau_c + \tau_c + \tau_j + \tau_r. \tag{8.1}$$

While complex expressions are employed in past literature to capture the behavior of each portion of this process [84, 198–201], scaling analysis (see Appendix A) shows that

$$\tau_t \approx \tau_g + 3.2\tau_c + \tau_r. \tag{8.2}$$

Considering fluid is a function of condensate thermophysical properties (liquid-vapor surface tension, $\gamma$, liquid density, $\rho$, and the critical nucleation droplet radius, $R_m$) and geometric properties at the solid-liquid interface (droplet growth-rate, $\left(\frac{\partial R}{\partial t}\right)$ and droplet radius, $R$), the complete jumping

timescale can be expressed as:

$$\tau_t \approx R\left(\frac{\partial R}{\partial t}\right)^{-1} + 3.2\left(\frac{\rho R^3}{\gamma}\right)^{\frac{1}{2}} + 4.35R_m\left(\frac{\rho R}{\gamma}\right)^{\frac{1}{2}}. \tag{8.3}$$

Now that the timescale has been defined, the rate of droplet heat transfer, $\dot{q}$, in one time interval is based on the mass flux, $\dot{m}$, and the latent heat of the working fluid, $h_{fg}$,

$$\dot{q} = \dot{m}h_{fg}. \tag{8.4}$$

Figure 8.1b highlights the method used to translate the rate of droplet heat transfer ($\dot{q}$) into overall surface heat flux ($q''$) by defining a large reference area composed of many unit cells where condensate droplets grow and coalesce with neighboring cells. Thus, the heat flux for jumping condensation can be shown to scale as (for derivation, see Appendix A):

$$q''_\tau \sim \left(\frac{\rho h_{fg}}{\tau_t}\right). \tag{8.5}$$

Given our understanding of the material-dependent timescales governing droplet jumping, we explored the fundamental heat transfer limits of droplet jumping condensation. To characterize the limits, we determined when timescales associated with jumping begin to approach one another. During droplet jumping, the growth of individual droplets prior to coalescence governs the growth timescale ($\tau_g$). If the growth timescale approaches or is smaller than either the coalescence ($\tau_c$) or jumping ($\tau_j$) timescales (i.e. $\tau_g < \tau_c$ or $\tau_g < \tau_j$), the jumping process cannot be analyzed as an isolated process with discrete phases independent on one another. In fact, to the best of our knowledge, all previous studies have assumed the opposite (i.e. $\tau_g \gg \tau_c$ or $\tau_g \gg \tau_j$). If $\tau_g$ approaches $\tau_c$, the growth of condensate liquid on the coalescing droplets during merging will interrupt the hydrodynamic processes governing jumping, and may impede departure. Similarly, if droplet re-nucleation and growth is so rapid as to not allow a coalesced droplet to depart prior to merging with the newly formed droplet beneath it ($\tau_g < \tau_j$), jumping will be impeded. Interestingly, the latter is a common observation in pool boiling studies, where $\tau_g \ll \tau_j$, resulting in multiple vapor bubble coalescence events with vertically departing bubbles from the surface, and formation of vapor columns [202].

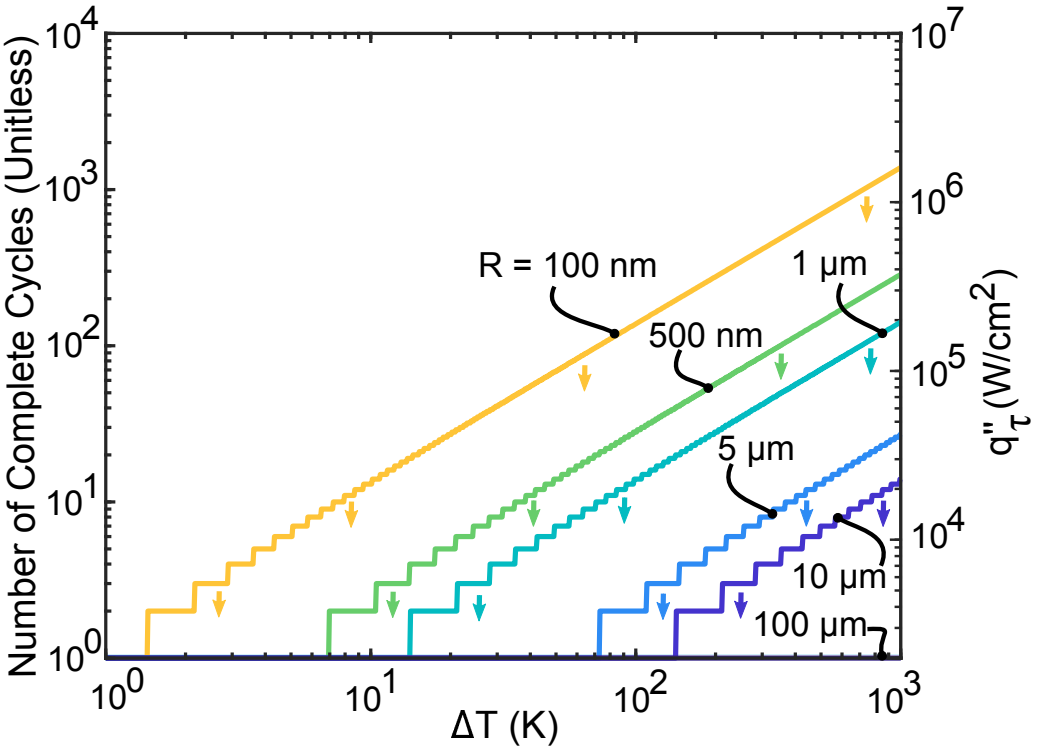


Figure 8.2: The total number of complete cycles per second for two-droplet coalescence and jumping (left axis) and the estimated overall surface heat flux (right axis) for water jumping droplet condensation as a function of vapor-to-surface temperature difference ($\Delta T$) and average droplet departure radius ($R$). Fluid properties assumed: $\rho = 998.2$ kg/m$^3$, $\gamma = 0.072$ N/m, $k_c = 0.2$ W/m$^2$·K, $k_f = 0.6$ W/m$^2$·K) and $R_m = 1$ nm.

The key parameter governing $\tau_g$ is the vapor-to-surface temperature difference, $\Delta T$. As $\Delta T$ increases, $\tau_g$ reduces and approaches $\tau_c$ or $\tau_j$. Figure 8.2 highlights the number of complete cycles per second per unit cell as a function of $\Delta T$ and average droplet jumping radius ($R$) for room temperature water working fluid. For example, approximately 10 droplets per unit cell will be ejected per second for an average droplet radius of $R = 100$ nm at a temperature difference of $\Delta T = 10$ K. A lower $\Delta T$ for the same $R$ yields fewer complete cycles, while higher $\Delta T$ results in more droplets departing per second. Yet, as $R$ increases, the number of complete cycles quickly decreases. For example, a 10X increase in $R$ requires a 10X increase in $\Delta T$ to maintain the same rate of droplets departing the condensing surface. Figure 8.2 also underscores how the maximum possible attainable heat flux during droplet jumping can be achieved by either increasing $\Delta T$ or decreasing $R$

in order to increase the number of droplet jumping events per second. The step-wise nature of this plot is a result of rounding down to ensure only whole droplets completing the entire jumping process were counted during a complete cycle. Interestingly, the $q''_\tau$ limits are quite high, exceeding ~20 kW/cm$^2$ for reasonable operating temperature ranges, departure radii, and assumptions for the dominant growth timescale (see Appendix A).

## 8.3 Considering Impact of Vapor-Side Hydrodynamics on Heat Flux

In order to verify the critical heat flux limitations from the vapor side perspective, we also considered vapor-side hydrodynamics on the jumping and departure process. As was previously reported [180,203], the presence of high heat flux at the condensing surface results in a rapid vapor flow normal to the surface and drag of droplets back to the wall. Scaling the maximum droplet jumping acceleration as:

$$|a| \sim \frac{v_j}{\tau_j} \tag{8.6}$$

where $v_j$ is the jumping departure velocity, and the Stokes drag force [204] as

$$F_D \sim \mu_v R\Big(v_v + v_j\Big), \tag{8.7}$$

where $\mu_v$ is the vapor viscosity and $v_v$ is the vapor velocity), one obtains a closed form solution for the critical heat flux not to be exceeded in order to allow droplet departure away from the surface as

$$m|a| \sim \frac{R^3 \rho v_j}{\tau_c} \sim \mu_v R\Big(v_v + v_j\Big). \tag{8.8}$$

Relating the vapor velocity to the heat flux, we obtain:

$$v_v \sim \frac{q''}{\rho h_{fg}}, \tag{8.9}$$

where the $v$ subscript corresponds to a material parameter for the vapor phase. Finally, equating the limits, a simplified closed form solution for the orientation-independent, hydrodynamic critical heat flux is (for derivation,

see Appendix A):

$$q''_h \sim \frac{\gamma \rho_v h_{fg}}{\mu_v}. \tag{8.10}$$

For room-temperature water ($\mu_v \approx 0.01$, $\gamma \approx 72.8$ mN/m, $h_{fg} \approx 2.5$ MJ/kg, and $\rho_v \approx 0.022$ kg/m$^3$), $q''_{crit} \sim 35$ kW/cm$^2$. Assuming that the velocity of vapor cannot exceed the speed of sound ($v_v < v_{sonic} < 300$ m/s), $q''_{crit}$ reduces to $q''_{sonic} \approx v_{sonic} \rho_v h_{fg} \approx 1.5$ kW/cm$^2$, much lower than the aforementioned timescale-based limitations (Figure 8.2).

The determination of the hydrodynamic and thermodynamic limits is important since it is well-established from experimental observations that $R$ during jumping droplet condensation increases over time as the superhydrophobic structured surface degrades and the condensation mode transitions into a flooding regime [179, 187, 188, 190, 191, 199, 205–207]. Progressive flooding characterizes surfaces where an increasing number of droplets become too large to jump and cover the cold surface, which prevents the nucleation of new droplets. Experimental observations highlight that flooding occurs mainly due to three mechanisms. The long-term robustness of the low surface energy functional conformal coating is limited and can degrade due to imperfections in the coatings [198,199,201,207]. Furthermore, localized pinning due to imperfections on the surface (i.e. regions of high contact angle hysteresis) promotes continued droplet growth without jumping, which ultimately leads to surface flooding and prevents droplet re-nucleation and growth [179, 187, 188, 190, 191, 199, 205, 206]. In addition to surface imperfections, progressive flooding can occur due to vapor-side hydrodynamics since droplets that jump can immediately return to the surface due to vapor shear. Based on conservation of mass, all condensate that forms on the surface comes from vapor generated at the hotspot. Yet, the ability of vapor to reach the cold surface and promote nucleation decreases as progressive flooding of the surface increases [178, 179, 187, 188, 190, 191, 207]. These flooding limitations explain the relatively low heat fluxes measured for electronics hotspot cooling ($< 10$ W/cm$^2$) using jumping droplets with water [1, 176, 177]. Namely, fundamental hydrodynamic and thermodynamic limits have yet to be reached, indicating that significant work is needed on the fabrication of the superhydrophobic surfaces to promote ever smaller $R$ via the rational engineering of well-defined and fixed nucleation sites to avoid nucleation-mediated and progressive flooding.

## 8.4 Survey of Working Fluids for Enhanced Jumping Droplet Cooling

Switching of the working fluid is another avenue for increasing the maximum jumping droplet condensation heat flux. Based on an examination of all of the elements in the periodic table, Figure 8.3 provides a regime map of the material survey. Since scaling analysis shows that the overall surface heat flux scales with the product of the latent heat and density of the working fluid (i.e. $q'' \sim \rho h_{fg}$), the performances of different elements were normalized against the baseline behavior of water. Moreover, a significant number of elements have melting temperatures greater than the useful range for many cooling applications, so only the elements with melting temperatures less than 873.15 K (600 °C) were preserved for further analysis. Figure 8.3 categorizes the elements based on their supply chain and cradle-to-grave sustainability [208,209]. Ignoring sustainability of the working fluid selection, Figure 8.3 suggests that gallium (Ga) or a Ga alloy would be the best possible choice since it has an order of magnitude better performance than water for a similar working temperature range. Yet, based on the current rate of global consumption, a serious supply chain risk exists for Ga in the next century [208, 209]. Interestingly, other materials with greater than 2X improvement in a reasonable working temperature range for electronics cooling such as indium (In), tin (Sn), and lithium (Li) are all either serious or potential supply chain risks. However, metals like mercury (Hg) and sodium (Na) offer nearly 2X improvement in performance with either limited or no supply chain risk respectively.

Melting temperature does not capture all of the necessary thermophysical property requirements of a working fluid to undergo droplet jumping. By further sorting the subset of fluids with melting temperatures less than 473.15 K (200 °C) and normalized material performance similar or greater than that of water based on vapor pressure [205, 210–216], the capacity of the working fluid to condense with a reasonable saturation pressure (diffusion transport) and temperature can be identified. Figure 8.4 underscores that a vast majority of the superior working fluids highlighted in Figure 8.3 (i.e. Ga, In, Li, Na) require temperatures several hundred degrees higher than water to achieve similar vapor pressures and avoid pressure-based limitations. While these working temperatures are vastly greater than the

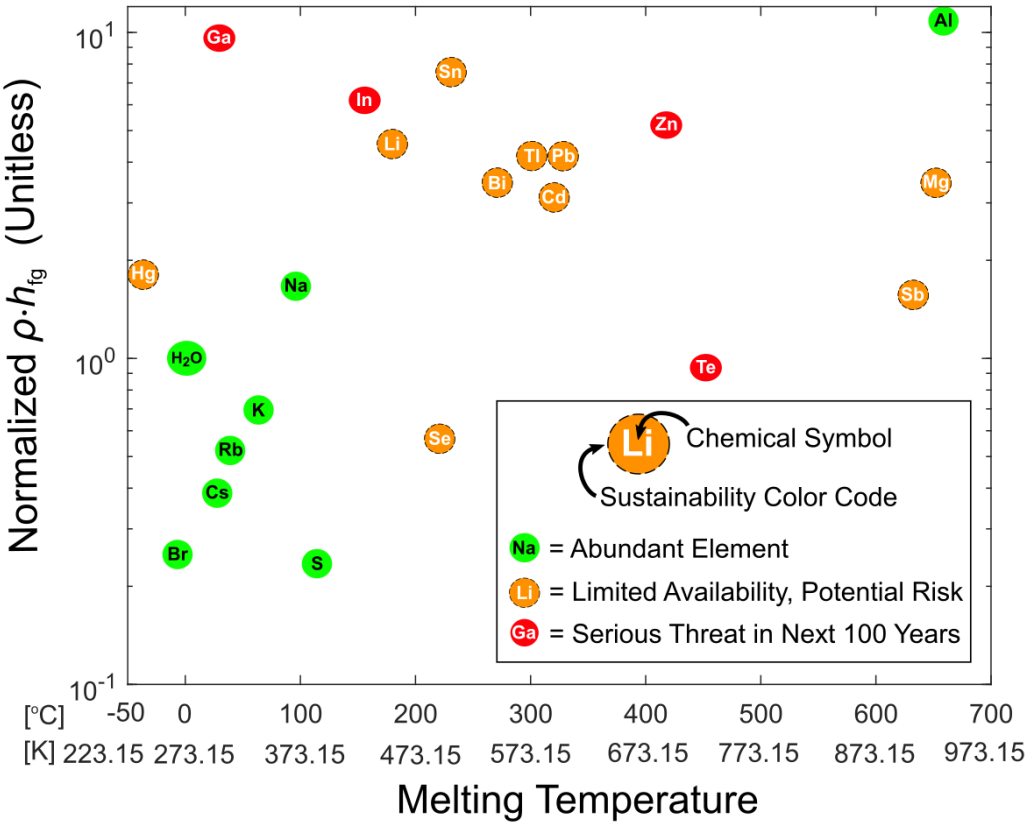


Figure 8.3: Comparison of performance of different potential working fluids for jumping droplet condensation based on considerations for supply chain sustainability. All energy density results are normalized against the energy density of water, $\rho h_{fg} = 2260$ MJ/m$^3$.

safe operating temperature of modern-day electronics, they still can be operated at reasonable temperatures to serve as cooling mechanisms for other high-heat-flux, extreme-environment systems [170, 173, 205]. Even Hg requires temperatures of ≈423 K (≈150°C) to achieve a modest vapor pressure on the order of 1 kPa, which is reasonable for the operation junction temperature of wide bandgap power transistors like gallium-nitride (GaN) and silicon carbine (SiC), but is significantly hotter than the standard operating temperature of silicon transistors, <393 K (<120 °C). The use of liquid metals as working fluids presents a promising approach from the perspective of high-temperature electronics. Furthermore, the high surface tension of liquid metals makes them ideal candidates for droplet jumping owing to their efficient capillary-to-inertial energy conversion and ability to be removed from unstructured smooth surfaces [217], and hence to eliminate

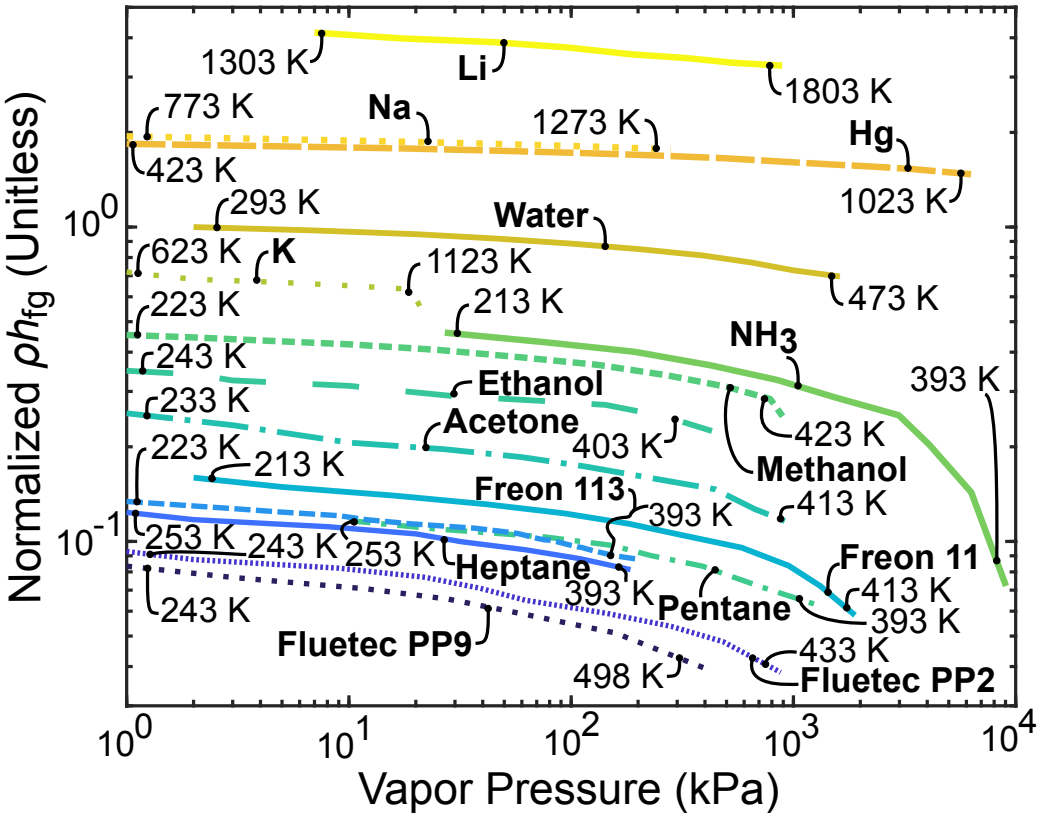


Figure 8.4: Regime map comparing the normalized energy density of a variety of potential working fluids as a function of vapor pressure relevant for saturation conditions required for condensation. All results are normalized with respect to water, $\rho h_{fg} = 2260$ MJ/m$^3$. Lines are labeled at their extremes with the corresponding saturation temperatures.

structure-based nucleation mediated flooding.

Given the limitation of liquid metals to high temperatures, we expanded our material survey to include other common working fluids for heat transfer applications. Acetone, ethanol, ammonia ($NH_3$), and methanol all exhibited inferior performance to water, but would have sufficient vapor pressure to be useful for the temperature ranges relevant for electronics cooling. Refrigerants and hydrocarbons all exhibited heat transfer performance at least 10X lower than water, and therefore are not promising to investigate further as jumping droplet cooling fluids. Furthermore, the ultra-low surface tension (<10 mN/m) of the majority of refrigerants makes them inappropriate for jumping droplet applications as currently no surface structuring approaches exist that enable the formation of refrigerant droplets residing in the non-wetting state (i.e. spherical high apparent contact angle

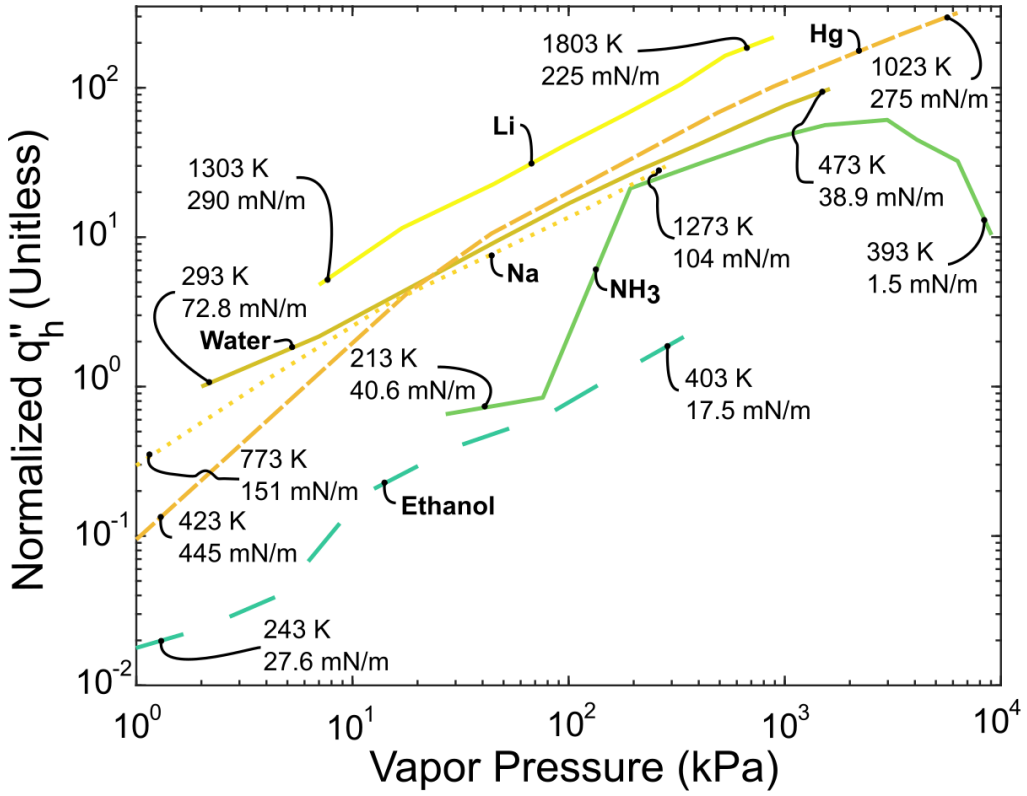


Figure 8.5: Regime map comparing the normalized hydrodynamic heat flux, $q''_h$, of a variety of potential working fluids as a function of vapor pressure relevant for saturation conditions required for condensation. All results are normalized with respect to water, $q''_h = 35.6$ kW/cm$^2$. Lines are labeled at their extremes with the corresponding saturation temperatures and surface tensions. All values were normalized by the performance of water at 293 K.

droplets) required to achieve efficient capillary-to-inertial energy conversion and droplet jumping [218]. Interestingly, past studies have been able to demonstrate droplet jumping using ethanol and ethylene glycol [218]. As a guideline, to ensure droplet jumping for common working fluids, we assumed a requirement of surface tension, $\gamma > 22$ mN/m, indicating that fluids such as methanol, ethanol, and ammonia are promising candidates for droplet jumping. Although demonstrated for deposited droplets, the development of omniphobic coatings capable of sustaining droplet jumping with fluids such as ethanol is assumed to be reasonable here from a theoretical standpoint.

Reexamining this survey of potential working fluids with respect to $q''_h$, Figure 8.5 highlights that only Hg and Li performed better than water for vapor pressures greater than ~100 kPa (i.e. temperature ranges >523

K (>250 °C)). Even though Na had a high $\rho$ and $h_{fg}$, the $q''_{crit}$ of water dominated Na in contrast to the behavior exhibited in Figure 8.5 since the $\rho_v$ of Na was an order of magnitude smaller than water for a majority of the vapor pressure range. While the $\rho_v$ of ammonia increases by four orders of magnitude over this vapor pressure range, the performance of ammonia was limited by the large decrease of both $h_{fg}$ and $\gamma$ with increasing vapor pressure. It is worth noting that many of these alternative working fluids would require engineering considerations for factors such as health risks, corrosion, and material compatibility with the vapor chamber casing. Overall, Figure 8.5 highlights that water has very competitive performance as a working fluid for jumping droplet condensation for temperatures relevant in many thermal management applications such as electronics cooling.

To put the material survey in context with the fundamental limitations for achieving maximum heat flux (i.e. $q''_{crit}$=min($q''_{\tau}$,$q''_{h}$,$q''_{s}$)), we computed the timescale-based as well as the sonic limitations for the most promising fluids, including $NH_3$, ethanol, Ga, Hg, and Li (for individual material plots, see Appendix A). Figure 8.6 underscores the importance of incorporating all three limits in the jumping droplet heat flux analysis since unique shapes exist for the $q''_{crit}$ behavior of all fluids surveyed. For example, our calculations demonstrate that ethanol offers enhanced $q''_{crit}$ for pressures between ∼7 and ∼30 kPa for a similar temperature range while Hg, Na, and Li outperform water for pressures above ∼100 kPa for higher temperature ranges. The inset table of Figure 8.6 summarizes the limitations, showing analogous results to water, namely that plenty of room exists to increase the jumping droplet heat flux prior to reaching fundamental limitations developed here.

## 8.5 Conclusion and Future Work

In summary, we developed the fundamental theory for the performance bounds of jumping droplet condensation. Similar to the theoretical critical heat flux limit for pool boiling, the heat flux for jumping droplet condensation increases with mass flux of droplets and the latent heat of the working fluid. Exploring the physics behind the jumping process highlights the process limitations due to individual droplet growth rate as well as structured surface design for anti-flooding. While this model assumes a uniform

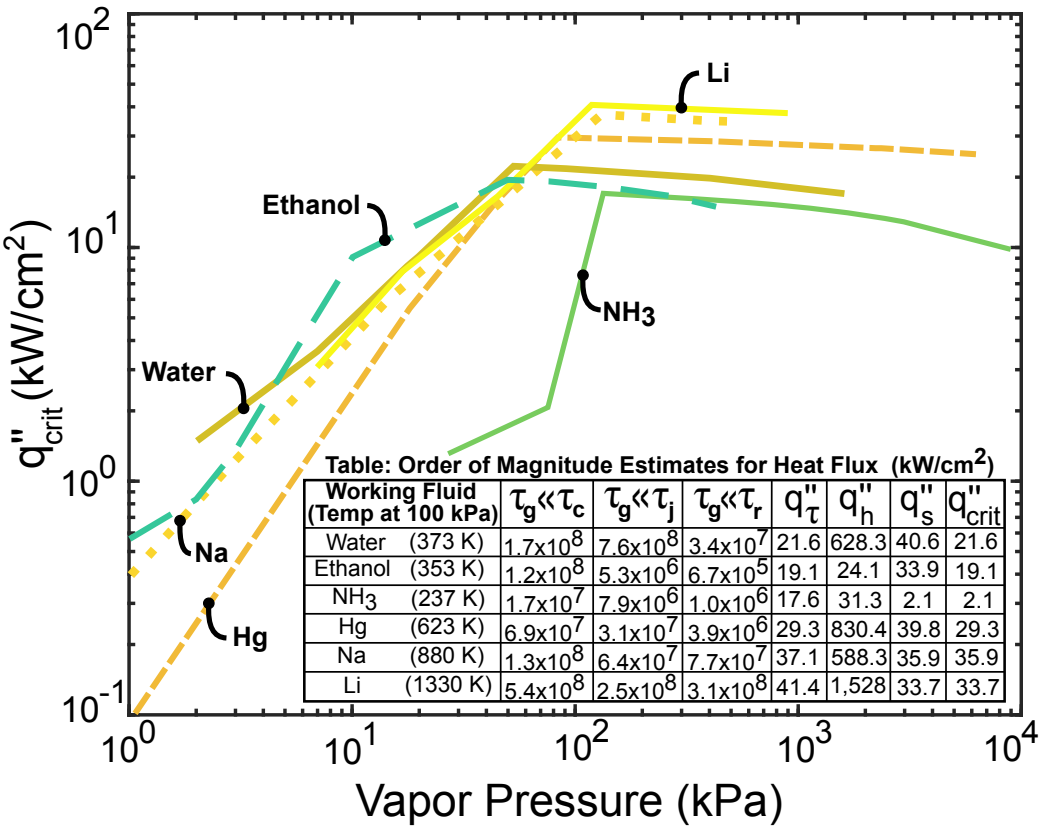


Figure 8.6: Theoretical critical heat flux, $q''_{crit}$, as a function of fluid vapor pressure for a variety of working fluids assuming $R = 10$ $\mu$m. The $q''_{crit}$ was determined from minimizing the calculated hydrodynamic, sonic, and thermodynamic timescale limitation heat fluxes tabulated (see inset table). All values were normalized by the performance of water at 293 K.

droplet distribution, which acts as an idealized distribution for estimating the upper bound for jumping droplet heat flux, the trends highlighted from exploring the limits provide important physical insight and serve as an idealized target. On realistic surfaces, droplets grow and coalesce following various size distributions. Improvements in surface engineering are still needed to translate monodisperse droplet nucleation site density [207] into the idealized monodisperse distributions for coalescence and jumping events assumed in this analysis. Future work can extend our framework for the theoretical bounds of maximum heat flux to incorporate different droplet size distributions and obtain more conservative estimates given additional constraints of specific structured-surface designs. Timescale analyses reveal that fundamental limitations have yet to be achieved, pointing to the need for surface-structure design optimization for minimization of

flooding seen in past experiments. In addition to controlling the length-scale of nanostructures, surface engineering must also ensure minimization of surface defects so that localized droplet pinning is eliminated. Additionally, any impurities including non-condensable gases must be removed during manufacturing in order to avoid premature flooding of the condensate on the surface and degradation of the nanostructured coating during operation in the field [1, 176–181, 183–185, 187, 188, 190–192, 198–200, 206, 219, 220]. This multifaceted coating conundrum is an open problem in liquid-vapor phase-change research and this work underscores that significant rewards exist for high-heat-flux cooling once the fusion of fundamental science and engineering surmounts these obstacles. Finally, examining the impact of thermophysical fluid properties on the limits of jumping droplet condensation heat flux reveals that water is a competitive working fluid for many thermal management applications with only Li and Hg offering enhanced performance for cooling systems at higher temperatures, >523 K (>250 °C), and ethanol as an alternative for temperatures <373 K (<100 °C).

# CHAPTER 9

# MEASURING JUMPING DROPLET HEAT FLUX IN VACUUM

*To tame the savageness of man and gentle the*
*life of this world...he who learns must suffer.*
*And even in our sleep, pain that cannot forget*
*falls drop by drop upon the heart,*
*and in our own despair, against our will,*
*comes wisdom to us through the awful grace of God.*

– Aeschylus, 545-455 B.C.

## 9.1 Introduction

Wide-bandgap transistors incorporating gallium nitride (GaN) and silicon carbide (SiC) are catalyzing the development of higher power density and higher efficiency converters by providing lower parasitics, such as on-state resistance, package inductance, and output capacitance, and smaller physical package size [74, 105, 107, 168, 221]. Yet, as the package size decreases and the power processed remains the same (or possibly increases), the surface area to cool the device dramatically decreases and the capacity to extract heat with conventional methods decreases. For example, employing thermal interface materials [79] constrains improvements in power density and specific power of the complete system due to the necessity for bulky heat sinks [101, 101, 159, 168, 222]. The integration of efficient cooling with chip-scale wide bandgap transistor packages would improve reliability and device performance by maintaining lower device junction temperatures [74, 101, 101, 168].

To ameliorate this concern, directed cooling mechanisms are required to mitigate hotspots and catalyze further increases in power density [170–172]. One thermal management approach for extracting heat involves liquid-vapor phase-change cooling, which exploits the capacity of latent heat to remove large amounts of energy from localized hotspots during phase transition. Methods for incorporating phase-change materials into heat sinks

for power electronics have focused primarily on hybrid heat sinks with metal foams [223] and alkane isomers such as n-eicosane [224,225]. Similarly, liquid to gas phase-change with refrigerants has been employed as a passive means to cool downhole electronics for drilling applications [226]. This transition (i.e. solid to liquid or liquid to gas) acted as a passive cooling mechanism to mitigate heat from the high peak power transients of low duty-cycle pulsed power supplies for applications such as aircraft landing gear or downhole drills [223,226–228]. While phase-change heat transfer is commonly applied to low duty-cycle power electronics converters like aircraft landing gear using waxes that transition from solid to liquid [223], few commercial power electronics systems utilize closed-loop evaporation and condensation-based phase-change cooling techniques. Motivated by the recent demonstration of controllable jumping-droplet electronics cooling on suitably designed superhydrophobic surfaces in ambient conditions [1,176,177], we experimentally investigate the hydrodynamics and heat transfer physics in the pure vapor environment of an open vapor chamber to benchmark the thermal management of GaN devices.

## 9.2 General Principles of Jumping Droplet Vapor Chamber Operation

Figure 9.1 depicts the closed-loop behavior of the jumping droplet process and highlights how this scheme can be integrated into a dense electronics assembly for directed cooling. This system comprises a vapor chamber containing a colder surface connected to a larger heat sink or a cooling loop and a hotter surface containing an array of hotspots. While GaN transistors were selected to represent generic power electronics hotspot generators, these heat generating devices could be any passive (i.e. inductor, capacitor), active (i.e. transistor, diode, etc.), or support logic (e.g. gate driver, digital isolator, microcontroller, etc.) component. The hotspots are enclosed within the vapor chamber in order to avoid any series thermal impedances from contact mechanisms like solder or thermal interfaces between the cooling fluid and other surfaces like heat spreaders or the hotspots themselves. To avoid safety hazards from high-voltage switches and to ensure a robust, highly reliable design, this scheme requires a thin electrically isolating coating layer for the hot side of the vapor chamber. The thickness of the coating is

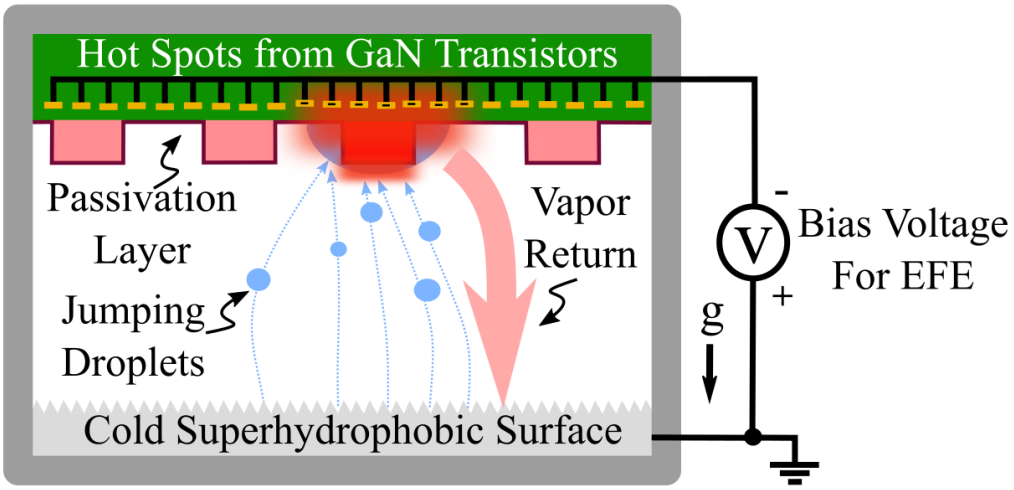


Figure 9.1: Schematic showing how external electric fields inside of a vapor chamber can be employed to guide jumping droplets toward hotspots independent of gravity. Heat is extracted from the electronics via evaporation, and vapor returns without a wicking structure to the cold surface where it is spread via condensation.

based primarily on the voltage isolation requirements of the electronics. A wide variety of polymers with high dielectric strength such as $SiO_2$ and Parylene exist which enable coatings that provide sufficient electrical isolation without becoming a significant barrier to heat transfer [174]. Moreover, the hot surface can be functionalized for enhanced performance such as promoting wicking of liquid toward hotspots with superhydrophilic nanostructures [174]. A key benefit of jumping droplet vapor chambers [1, 176–180, 183, 186, 189, 191–193, 198–201, 229] over other state-of-the-art vapor chambers and cooling schemes is the wickless liquid transport from the condenser to evaporator. Figure 9.1 demonstrates how, instead of relying on wick structures, cold droplets jump independent of gravity from the nanostructured superhydrophobic surface, are guided toward the hotspots using externally supplied electric fields, extract heat from the hot spot during evaporation, and return to the cold plate as hot vapor. Thus, the heat transfer process is not limited by the need for external pumping or capillary forces to drive liquid return to the hotspot. The lack of pumping required is a key benefit due to: (1) alleviation of aspect ratio design requirements governed by the need for liquid return [175], (2) elimination of additional thermal resistances from wick structures, and (3) simplified manufacturing

and integration.

## 9.3 Experimental Method and Observations

Building on observations from investigations of jumping droplet cooling in ambient conditions [1, 176, 177, 186], we began by exploring the governing physics behind jumping droplet heat transfer inside of a well-controlled vacuum chamber in order to reduce the amount of non-condensable gases, which develop a diffusion mass transfer barrier and severely limit performance [84, 230, 231]. While the vast majority of vapor chamber research involves assemblies that do not permit imaging of the vapor space, Figure 9.2a underscores how the custom experimental setup built around a 24" (0.6 m) cube vacuum chamber (Kurt J. Lesker) offers the unique capability to visualize coupling between heat dissipation and hydrodynamics. To observe dynamics within the vapor space, the chamber contains multiple 6" optical viewports, allowing access to a high-speed video camera (Photron FASTCAM Mini AX200 coupled to an InfiniProbe TS-160 lens).

Automating a large portion of the data collection and instruments for the experimental setup facilitated the rapid testing of different nanostructured coatings, surface cleaning methods, and cold plate materials with the electronics testbed shown in Figure 9.2b-d. To ensure the rapid transition from condensation to evaporation, the testbed was designed with the capability of switching between hot and cold liquid loops in order to adjust the temperature of the cold plate. As depicted in Figure 9.2a, the chiller-cooling loop can be isolated from the experimental setup with a series of valves and a bypass loop. As a result, hot fluid can be passed through the chamber from a separate heating bath (Polyscience SD07R-20-A12ER) in order to enable non-intrusive cleaning of a flooded surface and repeated tests at the same vapor pressure via thermal cycling of the cold plate as in Figure 9.3. To quantify the heat transfer enhancement from jumping droplets, we used a copper (Cu) cold plate (Wakefield-Vette 120455) functionalized with a nanoengineered superhydrophobic surface [232] as depicted in Figure 9.2c (see Appendix B for fabrication details). Briefly, after cleaning the Cu cold plates, a CuO superhydrophilic surface was created by immersing the cold plate in a heated alkaline bath. Next, chemical

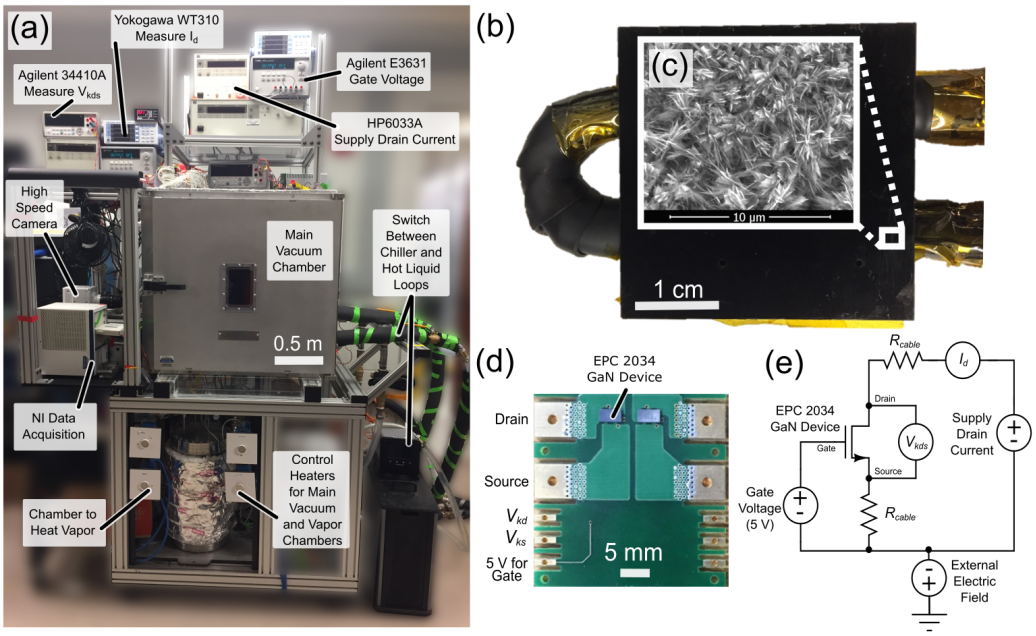


Figure 9.2: (a) Image of the chamber test bed used to conduct the jumping droplets electronics cooling experiments. (b) Copper cold plate having (c) CuO nanostructures with HTMS in order to ensure superhydrophobicity. Each transistor on a (d) custom power device testbed both generated heat and (e) served as a high-sensitivity heat flux sensor.

vapor deposition of a fluorinated silane (heptadecafluorodecyltriethoxysilane, HTMS) yielded a superhydrophobic surface with apparent advancing and receding contact angles of 172.1 ± 1.9° and 168.5 ± 6.7°, respectively (MCA-3, Kyowa Interface Science Ltd). Figures 9.2d and 9.2e highlight how the GaN transistors served both as hotspots and as heat flux sensors [1,174,176,177]. The junction temperature of the GaN device was tracked in real time during experiments by measuring the dc electrical resistance $R_{dson}$, which eliminated the need for attaching thermocouples to the GaN devices [1, 174, 176, 177]. During the experiments, the highest rate of condensation occurred at the condenser locations closest to the hotspot [180] since this is the smallest diffusion path for hot vapor to return to the cold plate. Similar to the behavior observed in the ambient environment [1, 176, 177], the external electric fields enabled enhancement of both heat flux and the duration of cooling by offering a larger area for replenishment of cold condenser liquid. Electric fields also help to magnify heat spreading and to reduce the rate of droplet accumulation and ultimate flooding on the superhydrophobic surface. The improvement is due largely to the capacity of the electric field to extend

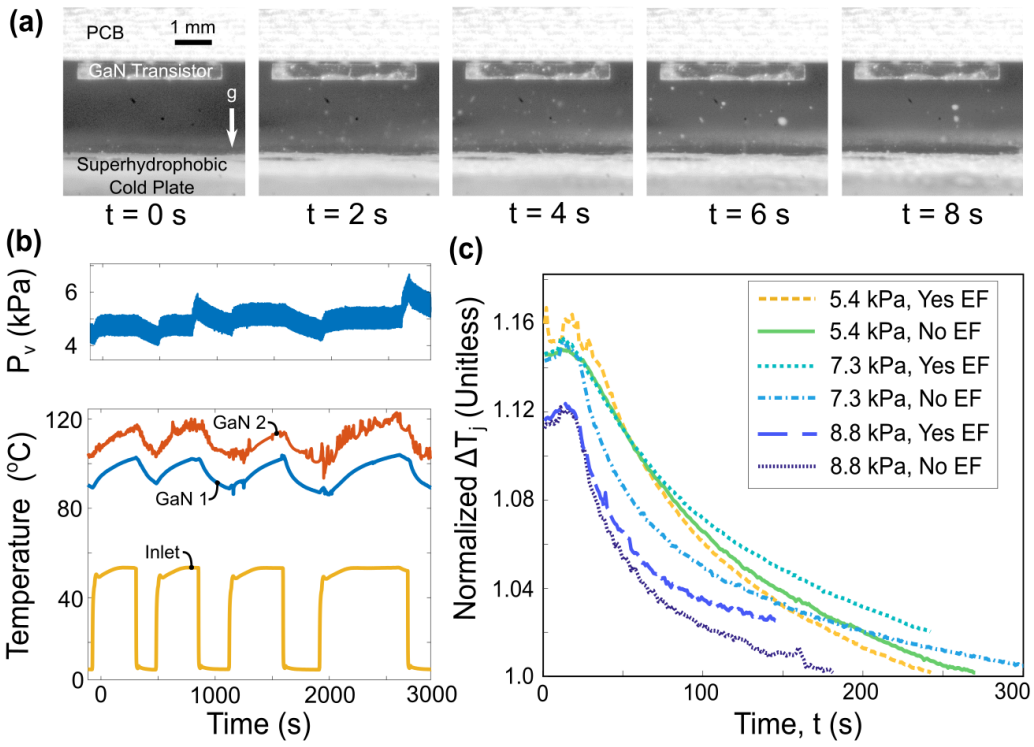


Figure 9.3: (a) Time-lapse images with corresponding (b) real-time data capture highlighting how thermal cycling enables several measurements to be obtained for the same vapor pressure, $P_v$. (c) Normalized change in the GaN junction temperature, $T_j$, with and without an applied electric fields (EF) during jumping droplet cooling. The measurements highlight a small and measurable improvement for all vapor pressure conditions, which had an uncertainty of $\pm 0.1$ °C. For clarity, error bars are not shown.

the region to which droplets can be attracted to cool the hotspot, which can be observed during the experiment as many droplets entering the frame and plane of focus change their trajectory and are attracted toward the hot GaN device. Interestingly, electric fields offer more than three orders-of-magnitude larger force on jumping droplets when compared to magnetic fields [1].

Figure 9.3a shows high-speed time-lapse images demonstrating the ability of electric-field-enhanced (EFE) jumping droplet condensation to cool spatially and temporally changing hotspots (see Appendix B for discussion of videos). This result was validated by switching the external electric field on and off for the two transistors and watching as the droplets were steered back and forth between the two transistors, demonstrating EFE condensation as a directed cooling scheme. Interestingly, imaging also revealed that the mass flux of droplets reaching a GaN device was <10,000 droplets per second.

Assuming an average droplet radius of 50 $\mu$m, this corresponds to a heat flux of $q''$ ~15 W/cm$^2$ (see Figure 8.2). Since the junction temperature, $T_j$, of each GaN transistor could be tracked with a propagated uncertainty of $\pm$ 0.8 °C (Figure 9.3b) and power dissipated, $P_D$, with an uncertainty of $\pm$ 2.1 mW, our heat flux measurements had a resolution of $\pm$ 20 mW/cm$^2$ (see Appendix B for more discussion about uncertainty). Figure 9.3c shows the normalized temperature difference, $\Delta T_j$, defined as $\Delta T_j(t) = \frac{T_j(t)}{T_j(t_1)}$ where $T_j(t_1)$ corresponds to the junction temperature after reaching the calibrated settling value based on the cold plate temperature. The transient cooling of the GaN devices was significantly lower than expected from theory and past experiments [186]. Figure 9.3c also highlights that enhanced cooling did not exist for a sustained period of time due to the transition to progressive flooding depicted in the final frames of Figure 9.3, which results in increasing jumping droplet departure diameter and an overall decrease in the jumping droplet mass flux.

For the experiments conducted here, electrical power was supplied to each GaN transistor prior to vapor supply to the evacuated chamber in order to determine the impact of radiation and to provide a calibration of performance as the cold plate temperature was cycled between cold (e.g. 20 $\pm$ 0.5 °C) and hot (e.g. 60 $\pm$ 0.5 °C). Prior to injecting pure water vapor, liquid water flowed through the cold plate at a rate of 22 $\pm$ 0.1 LPM (ThermoFisher Scientific SYS III) to ensure minimal thermal resistance from the coolant to the cold plate enabled by highly turbulent flow ($Re_D \approx$ 90,000, where $D = 5$ mm is the cold plate internal channel diameter). Pure vapor was allowed to flow until a steady-state surface temperature and vapor pressure, $P_v$, were achieved to ensure no condensation would occur. Based on the temperature of the cooling fluid (see Figure 10.6), $P_v$ was increased to ensure the supersaturation was less than the critical super-saturation for nucleation-mediated flooding [184, 191]. For example, for $P_v \approx$ 2.5 kPa, the coolant temperature was set to 20 $\pm$ 0.5 °C to ensure droplet jumping condensation. The change in $T_j$ for each GaN switch as well as an array of other temperatures inside of the setup (i.e. back of the PCB, chamber ceiling, chamber wall near the window, various locations on the cold plate, and inlet/outlet of the cold plate) were captured in real-time for all four phases of a single experimental run. Furthermore, imaging of initial nucleation once the coolant was routed into the cold plate, the period of jumping droplet condensation, the transition

to progressive flooding, and the process of evaporating the fluid from the cold plate by switching the inlet fluid to the hot supply were observed and recorded. For a single pressure condition, the experimental runs were repeated with and without applied electric fields ($\approx$ 100 V/cm). The entire experimental process was implemented for a range of pressures (2.5 kPa to 8.8 kPa). To characterize droplet jumping heat flux, $T_j$ was monitored for a given input power before and after jumping. For a fixed loss (input heat flux) prior to jumping, we would measure $T_j$ once steady state is reached for a variety of cold plate temperatures. Then, water vapor was injected into the chamber to initiate droplet jumping and GaN cooling. The new $T_j$ was noted once steady state was reached and the electrical input increased until $T_j$ approached the value of the non-jumping measurement. This approach ensured that only the contribution from droplet jumping was accounted for in the heat flux measurement, with fixed radiative components to the cold plate, as well as convection to the surrounding gas. For all experiments, the maximum dissipated GaN heat flux was <15 W/cm$^2$, indicating that significant limitations to droplet jumping cooling existed.

A second method of providing support for the low heat flux observations involves an examination of $\frac{\partial \Delta T}{\partial t}$ (Figure 9.3c) during experiments and comparing to other GaN device cooling methods. While the $\frac{\partial \Delta T}{\partial t}$ for aggressive phase-change cooling schemes like liquid bridge confined boiling [174] was $\sim$15 K/s, the $\frac{\partial \Delta T}{\partial t}$ for radiation/convection and jumping droplet EFE cooling were $\sim$0.01 K/s and $\sim$0.07 K/s respectively, which is a difference of over three orders-of-magnitude. Scaling the two results based on the maximum heat flux obtained by liquid bridge confined boiling ($\approx$ 100 W/cm$^2$) supports the other experimental evidence that heat fluxes during transient cooling of the GaN devices do not exceed 15 W/cm$^2$.

The high-fidelity heat transfer measurements do reveal a measurable improvement in cooling when the external electric field is applied. The maximum difference in heat flux for conditions without and with EFE was shown to be $\sim$5 W/cm$^2$ for only the first 20 seconds. High-speed video supports the observation that the surface flooded after $\sim$150 seconds for these experiments, which explains why the heat transfer started logarithmically approaching the maximum temperature difference on this timescale. Note that inverting the orientation of the setup for gravity-assisted jumping did not prevent surface flooding and did not significantly increase the maximum heat

flux observed due to jumping droplets. In fact, inversion of the experiment often promoted the formation of liquid bridges. Moreover, repeating the experiments for higher vapor pressures resulted in lower heat fluxes and temperature differences due to faster nucleation mediated flooding.

## 9.4 Investigating the Impact of Flooding

To explore the impact of flooding, we conducted additional condensation experiments using a variety of structured surfaces having varying length scales. Figure 9.4a depicts how the experimental setup was modified by inclusion of a mirror to observe simultaneously top-view condensation dynamics on five different nanoengineered samples. In order to provide a fair comparison with previous heat transfer characterizations, the flooding experiments were conducted for the same pressure range. Figure 9.4b shows top-view scanning electron micrographs of the structured superhydrophobic surfaces, including etched aluminum microstructures ($l \sim 10$ $\mu$m, etched Al), copper oxide microstructures ($l \sim 1\mu$m, CuO), titanium dioxide nanostructures ($l \sim 500$ nm, $TiO_2$), and aluminum oxy-hydroxide nanostructures ($l \sim 100$ nm, AlO(OH)). To attain superhydrophobicity and ensure all samples were coated with identical hydrophobic chemistry, all samples were conformally coated with HTMS. For fabrication details of all samples, see Appendix B.

Examining time-lapse images of the samples taken with a DSLR camera (Cannon EOS Rebel T6) at a frequency of 1 Hz (Figures 9.4b and 9.4c) revealed that flooding occurred first on etched Al (largest length-scale) and last on AlO(OH) (smallest length-scale). As previously hypothesized, the structure length-scale plays a critical role in flooding resistance, with smaller scale structures enabling higher discrete droplet nucleation densities without coalescence between neighboring unit cells of the structure [191]. Although demonstrated here to delay flooding, the use of smaller length scale structures did reconcile the difference in heat transfer measurements when compared to previous literature [180, 186, 192].

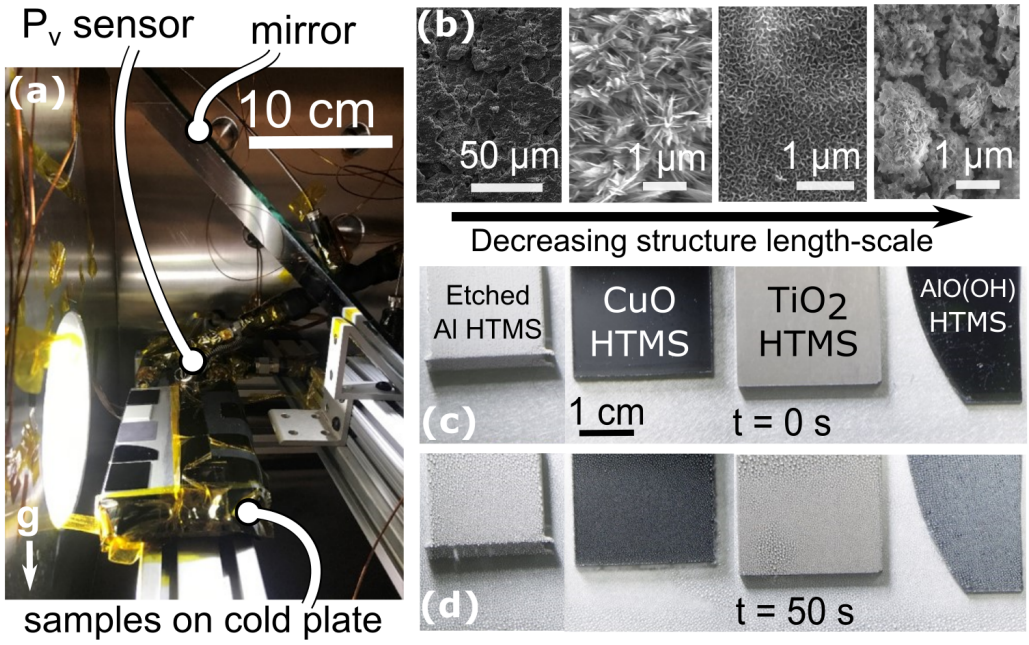


Figure 9.4: (a) Image of the experimental setup residing inside the test-bed (Figure 9.2a) used to obtain top-view images of the condensing samples with a mirror. (b) Top-view scanning electron micrographs of the structured samples used in the experiments. Top-view optical images of the structures samples (c) before and (d) after the injection of vapor in order to demonstrate how structure length-scale impacts flooding characteristics and jumping droplet behavior. All structures transitioned to the flooded condensation regime due to progressive flooding. Time t = 0 is defined as the time when condensate nucleation was first observed.

## 9.5 Conclusion and Future Work

In summary, the experimental observations highlight critical jumping droplet cooling limitations stemming from the inability of the superhydrophobic surface to eliminate flooding. Both high-speed video and heat transfer measurements support the hypothesis that jumping droplets cannot support high heat fluxes for even short timescales (∼30 seconds) with current state-of-the-art nanostructured surfaces. Future research is required to develop nanostructured surfaces that can both decrease the average radius of droplets departing the condensing surface as well as maintain this average departure radius in order to catalyze higher jumping droplet mass fluxes. In addition to engineering nanostructures of different length-scales and spatially controlled nucleation sites, surface engineering must also ensure that the conformal hydrophobic coatings prevent pinning and degradation [206, 218, 220]. Our

experimental observation of jumping droplet condensation time-dependent progressive flooding points to the need for more efficient removal mechanisms from the condensing surface once droplets depart. Interestingly, for confined, low-aspect-ratio devices such as vapor chambers, flooding ultimately yields self-assembled liquid bridges that connect the hot and cold surfaces. These liquid bridges can support heat fluxes exceeding 100 $W/cm^2$ via confined boiling [174] (see Chapter 10), which is the most likely mode of heat transfer in vapor chambers characterized in past literature [186, 192]. Our work signifies that while jumping droplet phase-change cooling holds promise, improvements to prevent flooding are required.

# CHAPTER 10

# SELF-ASSEMBLED LIQUID BRIDGE CONFINED BOILING ON NANOENGINEERED SURFACES

*I think like a pessimist and I work like an optimist. Life is full of surprises! Yes, at 95, I'm in the lab every day. I'm still working. What would I do, just retire and wait to die? No, I don't think so.*

– John B. Goodenough, 1922 - Present (Nobel Prize 2019)

## 10.1 Introduction

Emerging applications such as electrified transportation and next generation data centers require more compact, lightweight, and efficient electronics in order to improve system-level metrics such as vehicle range or computational density [159, 160, 168]. With the increased market acceptance of highly efficient, fast-switching wide-bandgap devices, opportunities exist for developing compact, three-dimensional (3D) integrated electronics [98–101, 107, 169]. Yet, the ability to remove heat from the internal hot spots of highly integrated packages constrains design and is a formidable obstacle to realizing the full potential of wide bandgap devices [98–101,159,160,168,169]. Conventional methods for thermal management such as single-phase air and liquid cooling are insufficient due to their inability to achieve high heat fluxes (<40 W/cm$^2$), constraints on operational temperatures (120–150 °C limit of electronics), and inability to handle spatial and temporal shifts in hot spots. More advanced cooling methods such as flow boiling or single-phase microchannel cooling attain high heat fluxes, but at the significant cost of large pressure drops and flow instabilities [170, 173, 233–236]. Furthermore, the size and weight of the pumps required for these schemes presents an integration challenge for mobile applications where volumetric (kW/L) and gravimetric (kW/kg) power density are paramount for achieving system-level objectives [98–101, 159, 160, 168, 169]. To address these stringent thermal management design requirements, we have developed a high heat flux, two-

This chapter includes work published in part in [174].

phase cooling scheme that employs confined pool boiling directly on wide bandgap devices within dense assemblies.

By placing a nanoengineered superhydrophobic condenser surface parallel to the hot electronics in the form factor of a vapor chamber or thermal ground plane (TGP), condensation of water vapor forms on the cold condenser surface. While conventional vapor chambers and TGPs seek to avoid condenser flooding, here the condenser surface is engineered to have an advancing contact angle of $\approx 150^\circ$ with a finite contact angle hysteresis of $\approx 10^\circ$ in order to limit coalescence induced droplet jumping [1, 176–180, 183]. As a result, condensing droplets coalesce and promote flooding, ultimately bridging the gap between the cold plate and electronics, enabling confined boiling and evaporation. Figure 10.1 depicts one realization of this liquid bridge (LB) confined boiling (LBCB) phenomenon, comprised of a hot gallium nitride (GaN) wide bandgap transistor on a printed circuit board (PCB) placed horizontally above a cold plate having a superhydrophobic coating inside of a vapor chamber. Due to the substantial temperature difference between the cold plate and hot electronics at low water vapor pressures ($\approx$1.55 kPa), efficient heat transfer via evaporation and vigorous subcooled, confined boiling in the liquid bridge can occur. Vapor bubbles can form during boiling within the LB that enable efficient mixing and transport of the subcooled liquid to quench the hot spots and to enable efficient heat spreading. Unlike flow boiling, the confined boiling technique developed here is passive and does not require pumping or flow control mitigation. Moreover, the LBCB approach deviates from previous confined boiling studies, which have focused primarily on horizontally parallel plate orientations with forced fluid flow and vertically parallel plate orientations with and without forced flow [170, 173, 233–236]. In addition, the LBs self-assemble between the cold surface and the hot electronics, which protrude down from the PCB. The tailored roughness and surface energy of the superhydrophobic coating enable water vapor to condense and to coalesce rapidly with neighboring droplets [178, 179], forming larger droplets that can bridge the gap between the condenser and hot electronics. For our LCLB thermal testbed, rigorous heat transfer measurements and optical high-speed imaging were employed to quantify the improvement in heat flux for various operating conditions, demonstrating heat fluxes $>100$ W/cm$^2$ with opportunity for further enhancement. The LBCB cooling scheme

developed here not only demonstrates a novel mechanism of direct high heat flux dissipation and spreading from hot spots, but offers design guidelines for enabling the development of fully 3D integrated electronics as well as insights regarding the heat transfer phenomena occurring inside low aspect ratio (height/width) vapor chambers and TGPs.

## 10.2 Experimental Methods

### 10.2.1 Thermal Testbed

To quantify the heat transfer enhancement of LBCB, a thermal testbed was constructed having a cold plate coated with a nanoengineered superhydrophobic surface and wide bandgap transistors to serve both as the hot spots and as the heat flux sensors. Depicted in Figure 10.2,

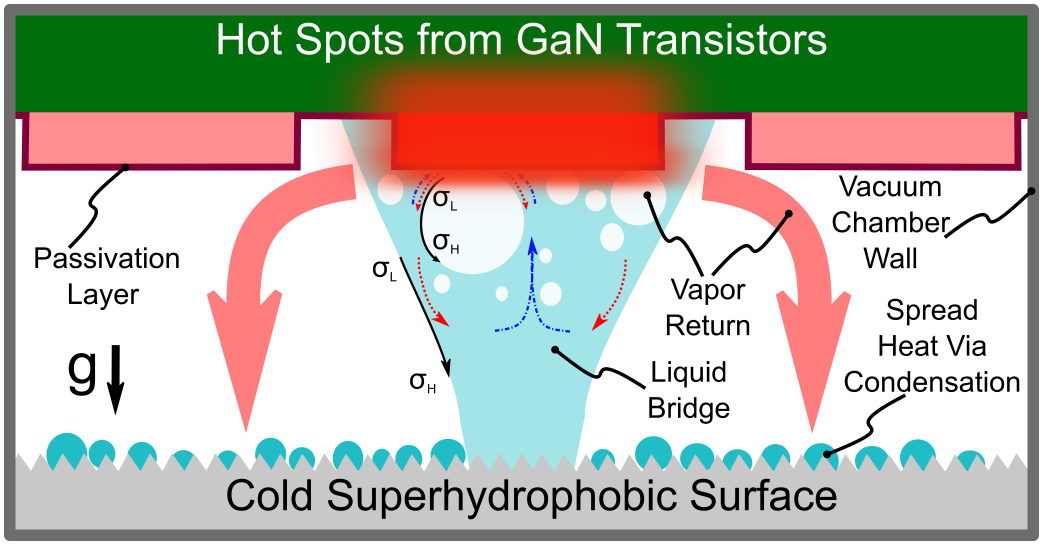


Figure 10.1: Schematic depicting the confined boiling method involving self-assembled liquid bridges. In addition to thermally induced Marangoni flows, effective heat spreading via condensation on the nanoengineered superhydrophobic surface enhances heat transfer. Black solid arrows depict Marangoni forces pointing from regions of low surface tension ($\sigma_L$) to high surface tension ($\sigma_H$). Red and blue dashed arrows depict qualitative representations of hot and cold fluid streamlines, respectively. Vacuum chamber wall depicted for a finite vapor chamber device, not indicative of the experiments conducted herein.

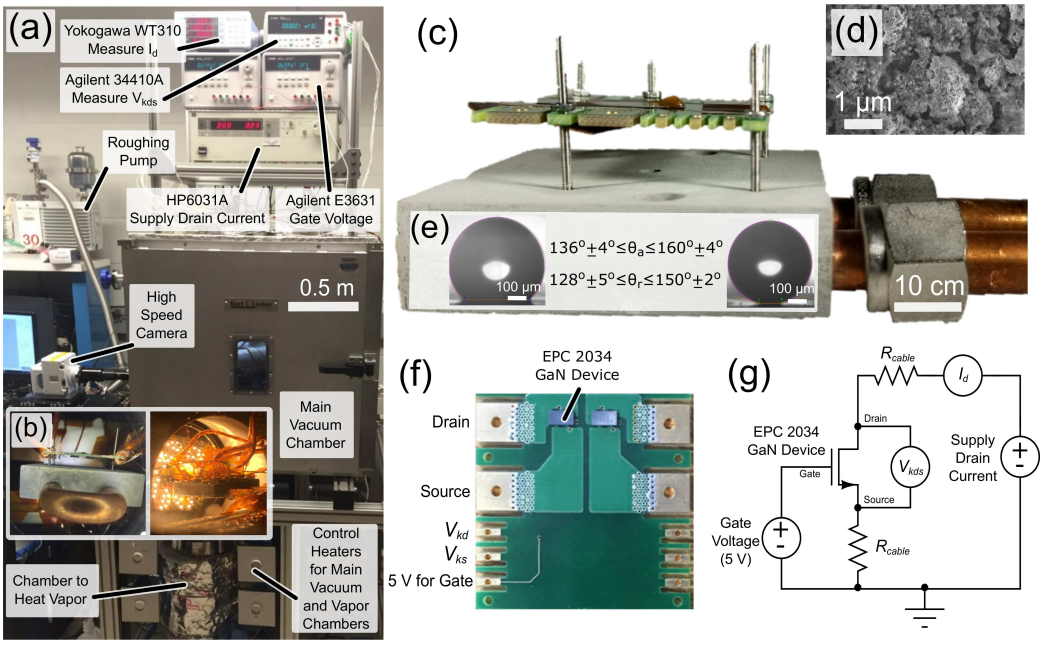


Figure 10.2: Experiments were conducted (a) within a vacuum chamber with (b) viewports illuminated with a custom light source for high-speed video and photography and feedthroughs to connect power supplies and measurement equipment to the electrical testbed. The distance between the (c) cold plate with an aluminum (d, e) superhydrophobic coating and a (f, g) circuit can be varied to probe different conditions for the high heat flux cooling of the wide bandgap transistor. Heat flux was determined based on a calibrated mapping of junction temperature to on-state resistance (f) via a high-precision measurement (see text for details)

the experimental setup was constructed in a 24" x 24" x 24" (0.6 m x 0.6 m x 0.6 m) vacuum chamber (Kurt J. Lesker). The chamber was designed with four 6" diameter viewports for external lighting and high-speed video access with a high-speed camera (Photron FASTCAM Mini AX200 coupled to an InfiniProbe TS-160 lens). Normally, imaging within a vapor chamber device is difficult and requires destructive techniques or particle beam methods [237, 238]. The experimental setup devised herein was developed solely to enable imaging within the vapor space of the vapor chamber. Furthermore, the need for vacuum was necessitated by the critical requirement to remove all non-condensable gases which develop diffusion barriers during condensation and evaporation phase change and severely limit performance [84]. The feedthroughs for the vacuum chamber enabled: (1) initial evacuation of the chamber (Edwards E2M30) down to 1.33 Pa in order

to remove non-condensable gases, (2) supply of saturated water vapor from a separate controlled heating chamber, raising the chamber vapor pressure, $P_{sat}$, to ≈1.55 ± 0.05 kPa during the experiments, and (3) active control of the cold plate temperature, $T_{cp}$, to achieve subcooling, $T_{sub} = T_{sat}$ - $T_{cp}$, of approximately 1.5°C below the saturation temperature, $T_sat$, with an external chiller (Thermo Fischer Scientific SYS-III) operating at ≈21 ± 0.08 liters per minute (LPM). During experiments, water vapor condensed over the entire cold plate, not just underneath the hot devices.

The electrical feedthroughs of the chamber routed power from a power supply (Keysight HP6031A) biased in current-limited mode outside the chamber to the electronics under test. Signals from a network of K-type thermocouples placed at key locations inside the chamber (cold plate inlet and outlet pipes, back of PCB, chamber wall) were also passed through feedthroughs. Since the GaN transistor (EPC2034) junction temperature and internal on-state resistance had a strong linear dependence [1, 107, 176, 177], the on-state resistance was tracked in real time with data acquisition and analysis (National Instruments PXI chassis and LabVIEW) via careful measurement of the drain current, $I_d$, with a power analyzer (Yokogawa WT310) and the drain-to-source voltage drop, $V_{kds}$, via Kelvin connections at the terminals of the device and a multimeter (Agilent 34410A) as shown in Figure 10.2g. As a result, the real-time resistance measurement enabled the high-precision mapping of electrical measurements for on-state resistance to junction temperature, $T_j$. The electrical measurements had higher accuracy and precision when compared to thermocouples [1, 176, 177]. The electrical testbed (Figure 10.2f) was designed with external connection points for ease of assembly inside of the vacuum chamber such that the largest protrusion from the PCB was the GaN device in order to promote LB formation with the electronics package.

### 10.2.2 Nanoengineered Surface Fabrication

To fabricate the nanoengineered superhydrophobic (SHP) cold plate (Figure 10.2c), a previously developed method was employed [239, 240]. Briefly, a commercially available Al cold plate (120455 Wakefield-Vette, 57.2 mm square) was ultrasonically treated in acetone and rinsed with ethanol, 2-

propanol, and DI water for 5 minutes each. After cleaning, the cold plate was dried in a clean N2 stream. The cold plate was then immersed in 5M HCl solution for 15 minutes in order to induce a microscale roughness, followed by removal and rinsing with room-temperature deionized water. Next, an immersion step with hot deionized water (90 °C for 1 hour) enabled boehmite ($Al_2O_3 \cdot xH_2O$) formation on the microstructured Al surface with sharp, knife-like structures having length scales approaching ≈300 nm (Figure 10.2d). To functionalize the surface, Heptadecafluorodecyltrimethoxy-silane (HTMS) was deposited using vapor phase deposition by placing the Al cold plate in a container with a vial of 1 mL HTMS toluene solution (5% v/v). A lid was placed on top to seal the container, followed by heating in an atmospheric pressure oven at 80 °C for 3 hours. This process allowed for the development of a highly conformal coating as the HTMS molecules evaporate from solution and re-deposit on the cold plate. Ellipsometry (Woollam VAS Ellipsometer) conducted on three different spots on a polished aluminum substrate revealed an average HTMS coating thickness of 2.6 ± 0.5 nm. Contact angle measurements (MCA-3, Kyowa Interface Science Ltd.) of ≈300 nL droplets on the HTMS coated structured Al cold plate showed advancing/receding contact angles having a range from $\theta_{a,app}/\theta_{r,app} \approx 136 \pm 3.1^\circ$ / $128 \pm 4.2^\circ$ to $160 \pm 4.1^\circ$ / $150 \pm 2.3^\circ$ (Figure 10.2e). The large spatial variation in contact angle was caused by the manufacturing-induced macroscale roughness present on the Al cold plate prior to micro- and nanostructuring, which introduced roughness inhomogeneities and added pinning sites. The presence of macroscale roughness, however, was not considered to be deleterious. Combined with the regions of very high superhydrophobicity, the roughness and inhomogeneity enhanced flooding of the surface and hence the LB formation rate.

### 10.2.3 Constant Junction Temperature Experimental Procedure for Measuring Heat Flux

The gap distance, $G$, between the top of the PCB and the cold plate was varied using 1.5 mm diameter, 0-80 threaded stainless steel rods and nuts, which minimized conduction heat transfer via the spacers while simplifying the process of changing $G$. Past approaches utilizing the transistor as both

the high sensitivity thermocouple and heat generator have typically tracked changes in junction temperature, $T_j$, for constant input power, $Q_{in}$, in order to determine improvements in heat flux [1, 176, 177]. Since maintaining constant $T_j$ is more representative of a real-world thermal management scenario, constant $T_j$ measurements were employed to determine the increase in heat flux due to LBCB. Prior to LB formation, $I_d$ was set such that $T_j \approx 30°C$. Once the LB formed, $T_j$ decreased. Therefore, the power, and thus $I_d$, were actively varied in order to keep $T_j$ constant before and after LB formation. Based on the increase in power processing for the same $T_j$, the improvement in heat flux was quantified.

## 10.3 Results and Discussion

### 10.3.1 Mechanisms Governing LB Stability and Heat Transfer

Based on the choice for nanoengineered surface wettability to enhance flooding, the orientation of the parallel plates with condenser on bottom was selected intentionally. If the parallel plate orientation had been reversed such that the condenser was on top, gravitational force would have detached droplets after overcoming the weak surface adhesion between the water and coated surface due to low contact angle hysteresis ($<10°$) on the condenser. The orientation of the plates against gravity (cold side down) ensured that LB formation was more stable due to the higher adhesion between the liquid and PCB when compared to the superhydrophobic cold plate. Furthermore, thermally induced Marangoni forces (Figure 10.3) helped to hold the bridge together due to temperature-dependent surface tension differences at the hot GaN device and cold condenser. The Marangoni forces in our orientation (Figure 10.1) also induced flows to guide hot liquid away from the electronics and toward the cold plate [241, 242] as shown in Figure 10.3a, promoting convection and LB stability. A secondary mechanism promoting heat transfer involved Marangoni-induced flow inside of the LB surrounding formed bubbles [241,242]. As bubbles grew, the Marangoni flows around each bubble drove cold liquid from the cold plate toward the hot spot for re-quenching as depicted qualitatively in Figure 10.3b.

To better understand the forces acting during LCLB, we performed a

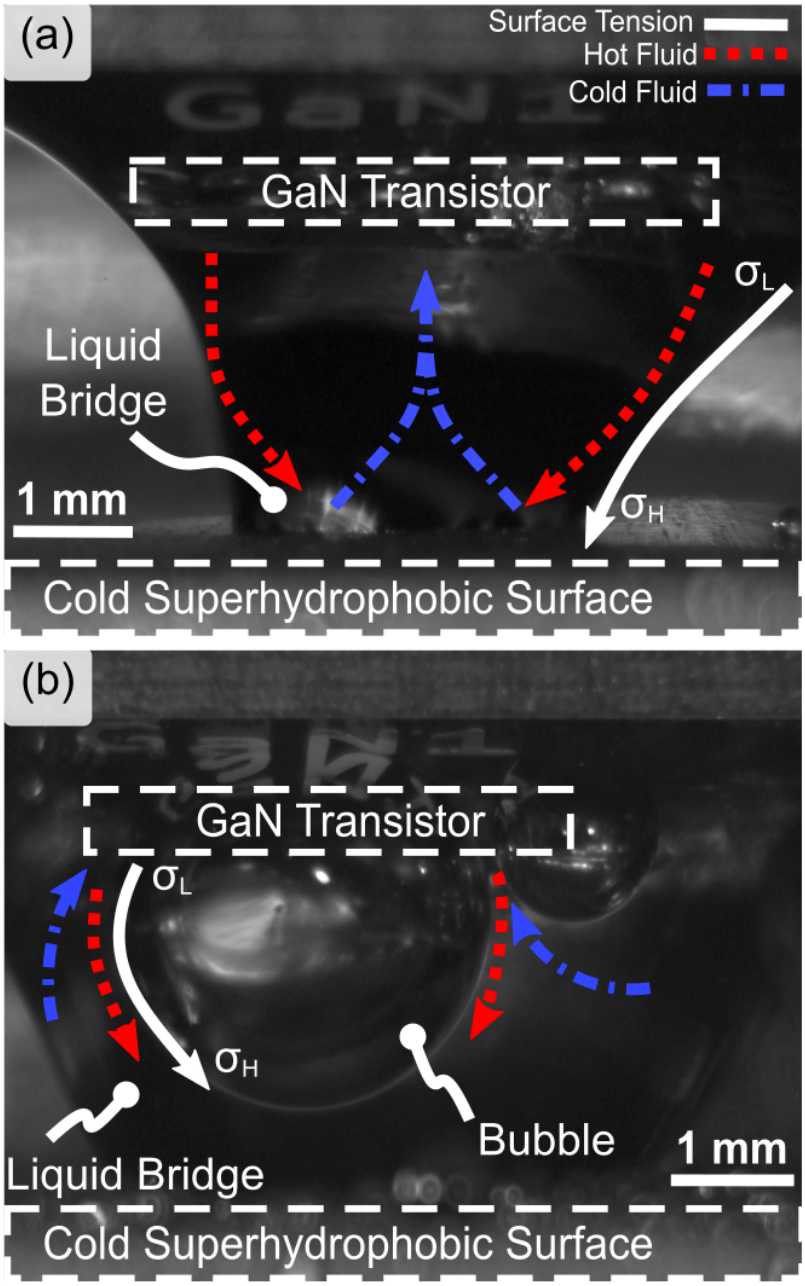


Figure 10.3: High-speed optical side-view images demonstrating how differences in thermally induced surface tension (white solid lines) for the (a) LB as a whole and (b) bubbles within LBs create Marangoni forces and flows that drive the cold condenser subcooled liquid (blue, dash-dot line) toward and hot liquid (red, dashed line) away from the hot surface of the GaN transistor. Both Marangoni forces help to enhance heat transfer process.

scaling analysis of the governing forces [243, 244]. Surface tension driven flow dominates when the characteristic timescale associated with Marangoni flow, $\tau_M$, is smaller than the characteristic time of density gradient mediated flow or buoyancy, $\tau_B$ [244]. Calculation of the Marangoni timescale,

$$\tau_M = \tau_d/\mathrm{Ma}, \tag{10.1}$$

required an estimate of the timescale for thermal diffusion,

$$\tau_d = a^2/\kappa, \tag{10.2}$$

and the dimensionless Marangoni number for pure water,

$$\mathrm{Ma} = |\alpha| a \Delta T_M/\kappa\mu, \tag{10.3}$$

where $\kappa = 1.41 \cdot 10^{-7}$ [m$^2$/s] is the thermal diffusivity, $\mu = 1 \cdot 10^{-3}$ [kg/m·s] is the dynamic viscosity, and $\alpha$ = -1.55 $\cdot 10^{-4}$ [kg/K·s$^2$] is the change in water liquid-vapor surface tension with respect to temperature. The characteristic length, $a$, for the edge of the LB and for the bubbles inside of the LB was half of the gap spacing between the condenser and evaporator, $G/2$, and the bubble radius, $D_b/2$, respectively (black arrows in Figure 10.5(b)). Similarly, the temperature differences along the liquid-vapor interfaces ($\Delta T_m$) of the LB edge and bubble height were ≈1 °C and ≈20-30 °C, respectively. The assumption of $\Delta T_m$ ≈20-30 °C for bubbles forming within the LB was deemed appropriate given that the maximum temperature difference between GaN junction and cold-plate surface was 40 °C. Using characteristic bubble radii $a$ ≈ 100 $\mu$m and LB half-heights $a \approx 1$ mm resulted in Ma ≈ $10^3$ for both cases. At the LB boundary and bubble, $\tau_m \approx 6 \cdot 10^{-3}$ and $\tau_m \approx 1 \cdot 10^{-4}$, respectively.

While buoyant forces in the studied LBCB configuration were negligible (bottom side cooled), inversion of the system orientation (bottom side heated) would result in significant buoyant forces. In the inverted case, the Rayleigh number,

$$\mathrm{Ra} = \alpha_t g a^3 \Delta T_m/\kappa\mu, \tag{10.4}$$

and corresponding buoyancy characteristic timescale,

$$\tau_B = \tau_d/\mathrm{Ra}, \tag{10.5}$$

need to be considered. Assuming a pure water thermal expansion coefficient of $\alpha_t = 3 \cdot 10^{-4}$ [$K^{-1}$] and $g = 9.81$ [$m/s^2$], Ra $\approx 100$ and $\tau_B \approx 10^{-2}$ s. The scaling analysis supports our hypothesis that Marangoni forces dominated both LB and bubble dynamics as $\tau_M < \tau_B$ and Ra $<$ Ra$_{crit} \approx 1700$ needed to initiate Rayleigh-Bernard convection cells between the two parallel sections [243, 244].

A secondary and key phenomenon promoting enhanced heat transfer in LBCB involves pool boiling within the LB. Traditionally, boiling from a hot spot submerged in a large, idle, subcooled pool is limited only by how quickly bubbles can depart the hot surface in order to promote quenching with cold liquid [195, 196, 245]. Depending on bubble size, the growth and departure process can be governed by different physical phenomena. As cold water quenches the surface and a bubble nucleates, the bubble is smaller than the thermal boundary layer thickness, limiting the growth rate due to inertia. In contrast, as the bubble size exceeds the thermal boundary layer thickness, growth becomes thermally limited due to a decrease in the degree of superheat between the hot surface and the fluid nearby. The boiling heat flux is governed by the transition from inertia-controlled bubble growth to thermally controlled bubble growth. Various strategies for increasing the frequency of bubble formation and maintaining primarily inertia-controlled growth dynamics have been examined in order to enhance the pool boiling heat transfer primarily in both unconfined and confined pools [246–250]. The LBCB approach is capable of achieving heat transfer enhancement with the use of self-assembled LBs that maintain the confinement of a small volume of subcooled liquid due to surface tension forces and help maintain inertia-controlled bubble growth due to confinement (condenser hot spot separation).

### 10.3.2 Liquid Bridge Hydrodynamics

Liquid bridge self-assembly via the coalescence of large droplets on the cold, nanostructured condenser surface was observed utilizing high-speed imaging as depicted in Figure 10.4a (see supplementary video S1 described in Appendix C). The PCB was designed such that the GaN devices would be the tallest component (smaller spacing to the condenser) as LBs form preferentially adjacent to larger protruding features from the upper parallel

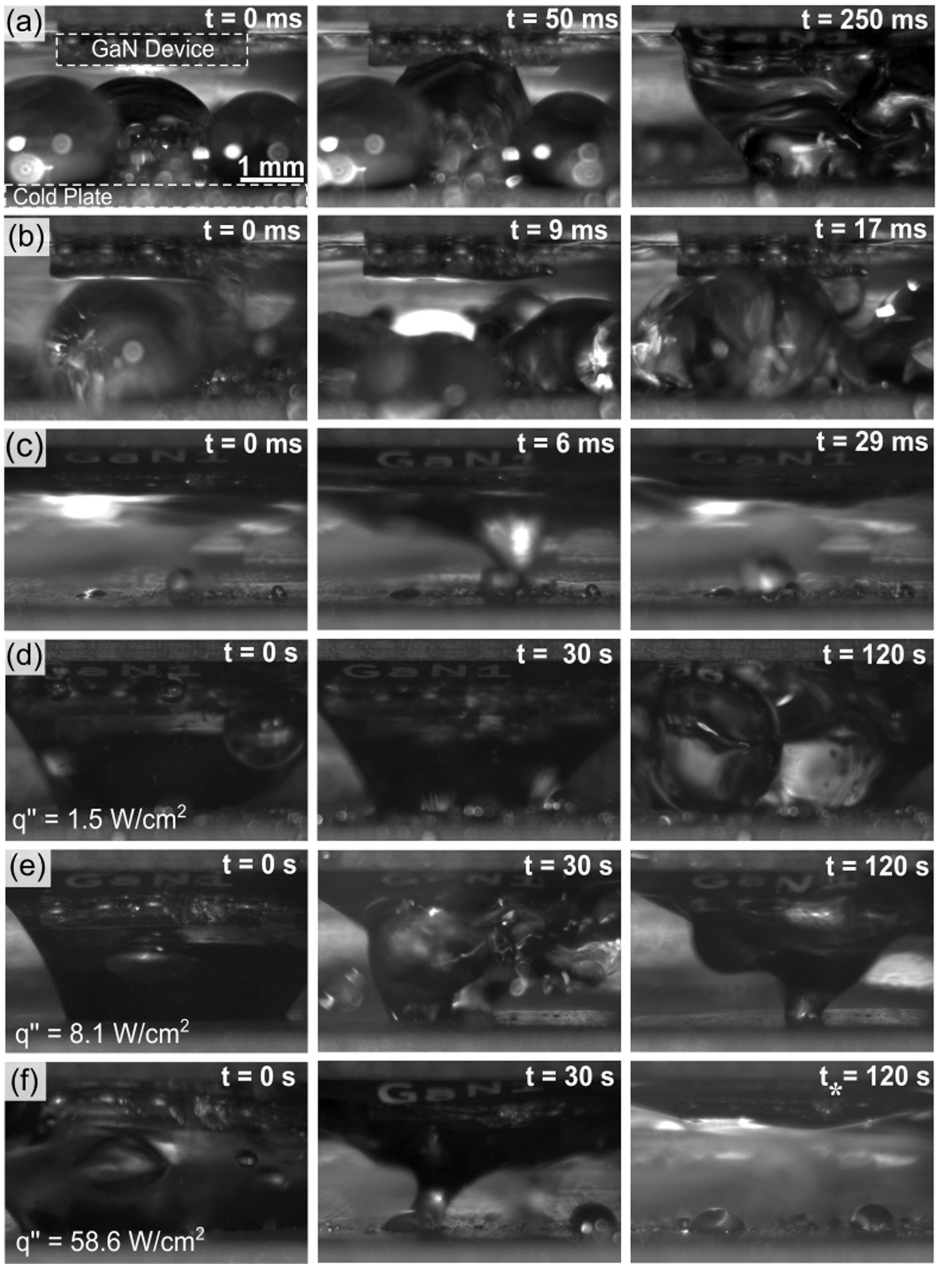


Figure 10.4: High-speed time-lapse images of the LB formation process showing three important physical phenomena governing LB mechanics: (a) initial bridge formation due to coalescence of large ($\sim$ 1.5 mm) droplets, (b) bridge collapse and reformation at low ($< 5$ W/cm$^2$) and moderate ($< 20$ W/cm$^2$) heat fluxes, and (c) temporary bridge reformation for moderate and high heat fluxes ($> 20$ W/cm$^2$). The LB lifetime was directly correlated to the (d) low, (e) moderate, and (f) high heat flux. The GaN device was turned off at $t_*$ since sufficient cooling for steady operation was no longer provided. Images obtained at a frame rate of 1000 fps.

plate. Furthermore, LB formation and lifetime also benefit from the fact that a majority of vapor is generated by the local hot spot, therefore enhancing the condensation rate on the cold plate adjacent to the hot spot. The high local vapor concentration ensures that the largest saturation pressure, and thus supersaturation, is in the region of the GaN device, promoting local condensation and LB formation. While surface tension and Marangoni forces helped maintain LB stability, Figure 10.4b highlights how boiling induced bubbles cause the LB to burst, collapse, and reform (see supplementary Video S2 described in Appendix C). Unlike conventional pool boiling, bubbles nucleating inside the confined LB do not have to perform as much boundary work on the surrounding liquid to grow, and therefore, are not inertia limited. As shown in Figure 10.4b and 10.4c, bubbles quickly grew ($\sim$ 1 ms), causing the LB to burst. As the LB collapsed (Figure 10.4b), the reformation process collected liquid from the cold plate and formed a new LB. Figure 10.4c highlights a LB lifetime mechanism where a complete detachment of the LB occurred (see supplementary Video S3 described in Appendix C) and a bursting bubble within the detached film enables the bridge to 'scoop up' condensate droplets growing near to the hot spot [18]. Thus, as bubbles grow and burst within the LB, the LB can be permanently reestablished, temporarily reestablished, or 'scoop up' condenser liquid and return to a detached film-state. Our experimental observations showed that these three modes of LB lifetime and reformation behavior were functions of hot spot heat flux, the amount of condensate on the cold plate, and spacing between the condenser and hot spot. For example, spacing greater than the capillary length of water, $\approx$2.5 mm, has differing forces governing LB formation and heat transfer.

The LB reformation process contributed to enhancing the heat transfer by bringing cold liquid to quench the hot surface. For moderate ($q'' < 20$ W/cm$^2$, see supplementary Video S4 described in Appendix C) and higher heat fluxes ($q'' > 20$ W/cm$^2$, see supplementary Videos S5 and S6 described in Appendix C), a secondary LB formation behavior was observed characterized by bubbles forming inside the remaining film on the hot GaN device. The bubbles grew, burst, and temporarily re-established the LB with the cold plate, which again enabled cold liquid to be reintroduced into the film (Figure 10.4c). The secondary LB behavior was observed near the end of the LB lifetime for the moderate and high heat flux conditions (Figure 10.4). For

moderate ($q'' < 20$ W/cm$^2$) and low ($q'' < 5$ W/cm$^2$) heat fluxes, the bridge lifetime exceeded 120 and 300 seconds, respectively. Interestingly, even at high heat fluxes ($q'' > 20$ W/cm$^2$), the LB was able to provide enhanced cooling for more than 30 seconds due to the vigorous, subcooled, confined boiling and contributions from the temporary bridging phenomenon shown in Figure 10.4c. Furthermore, the re-establishment of the LB enabled highly efficient boiling and thin film evaporation [251–254] to exist at the end of the LB lifetime for the high heat flux cases shown in Figure 10.4f. Additionally, the Marangoni flow induced around bubbles inside the LB attached to the hotspot, in combination with the large superheat of the GaN device and subcooling of the cold plate, helped to promote enhanced heat transfer.

### 10.3.3 Liquid Bridge Confined Boiling Heat Transfer

Using the data obtained from our constant $T_j$ experiments (see Sec. 10.2.3), we constructed the LB confined boiling curve as shown in Figure 10.5a. In order to understand the thermal dissipation pathways during the LBCB process, we developed analytical heat transfer models based on thermal resistance networks. Approximately 90% of the heat generated by Joule losses in the junction of the GaN transistor were conducted to the device front case ($R_{j-w} = 0.45$ K/W), primarily due to the thermal resistance from the junction to the front side of the GaN being roughly one ninth that of the corresponding thermal resistance from the junction to the back side [255], as noted in the inset of Figure 10.5b. The high spreading resistance of the PCB and limited cooling options on the opposite side of the PCB also contributed to the low amount of heat routed through the back side of the GaN device. Thus, for varying input powers, $Q_{in}$, the temperature of the GaN device front side where boiling occurred was determined from $T_w = T_j - 0.9 Q_j R_{j-w}$ and the degree of superheat from $\Delta T = T_w - T_{sat}$. Here, $T_{sat}$ was calculated based on the best-fit line approximation of the water vapor saturation pressure, $P_{wv}$ shown in Figure 10.6. Heat flux ($q''$) was calculated by dividing the measured increased power dissipated by the junction of the GaN transistor ($Q_{in}$), while maintaining the same junction temperature as the calibration case before the bridge was formed, by the package area ($A_{GaN}$).

For gap spacing, $G = 2.5$ mm, the LBCB method was found to enable $q''$

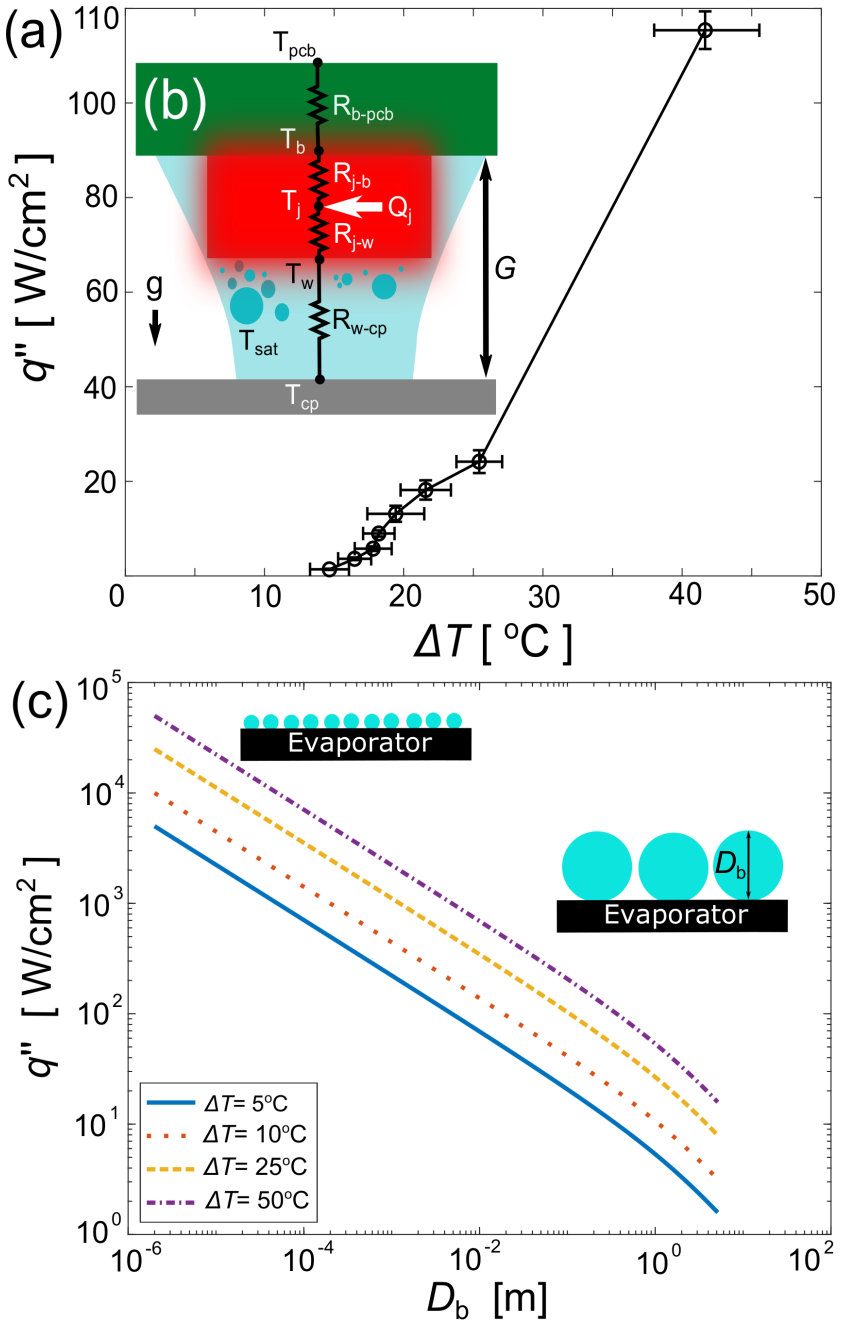


Figure 10.5: (a) Measured GaN device heat flux dissipation ($q'' = Q_{in}/A_{GaN}$) as a function of GaN-to-fluid temperature difference ($\Delta T$) for subcooled LBCB at $G = 2.5$ mm. For self-assembled LBCB, $q'' > 100$ W/cm$^2$ prior to reaching CHF. Inset (b): Thermal resistance diagram for the LBCB experiment, highlighting the minimization of chip-to-coolant thermal resistance for enhanced hot spot cooling. (c) Impact of departure bubble diameter ($D_b$) on calculated $q''$. Inset: Schematics of adjacent bubbles residing on a hot evaporator surface.

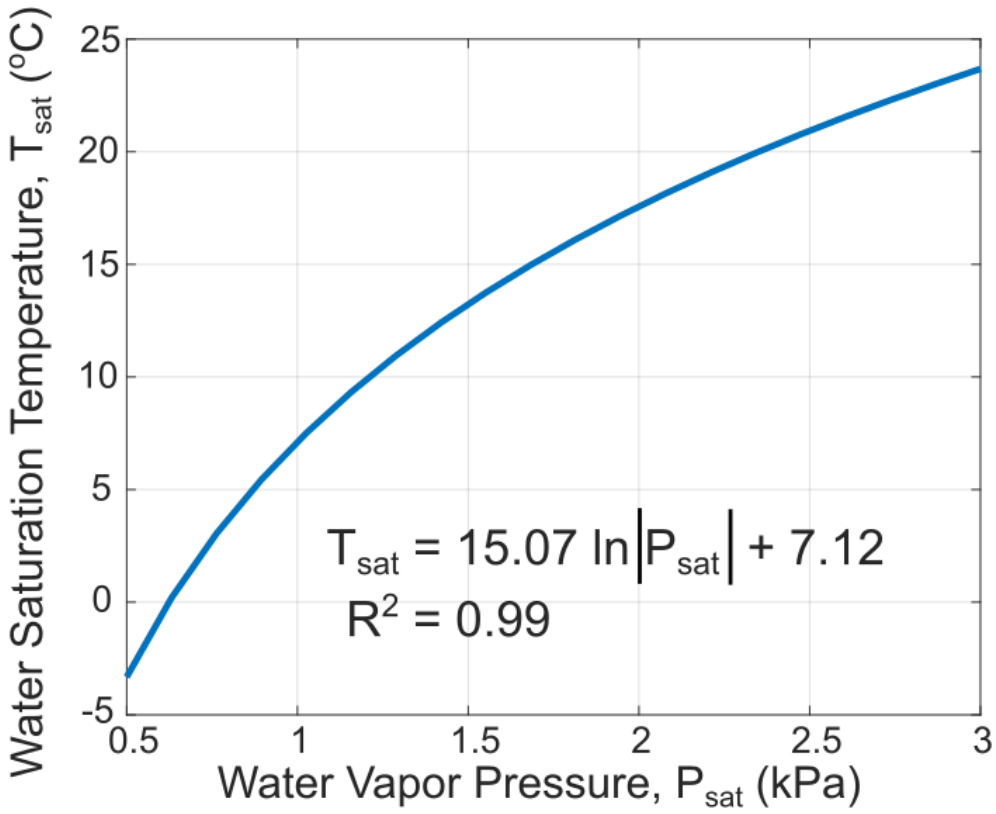


Figure 10.6: For this vapor chamber, the water saturation temperature ($T_{sat}$) and the degree of subcooling for the nanoengineered superhydrophobic cold plate must be calculated based on the measured water vapor pressure ($P_{sat}$). This is the best-fit line from measured data available from standard reference manuals [256].

$\approx$ 100 W/cm$^2$ and heat transfer coefficients of $\bar{h} = q''/\Delta T \approx 50$ kW/m$^2$K. The maximum heat flux was achieved while searching for the critical heat flux (CHF) by allowing both $Q_{in}$ and $T_j$ to increase freely and tracking the change in both variables. For the current experiments, the CHF was not experimentally observed due to limitations on the current rating of the electrical feedthroughs. To test our hypothesis of stable LB formation and its effect on heat transfer, increasing the spacing to $G = 5$ mm resulted in a heat transfer decrease to $\bar{h} \approx 25$ kW/m$^2$K for the same temperature difference due to larger bubble formation. Furthermore, increasing $G$ resulted in LB length scales larger than the capillary length scale of water ($< \approx$2.5 mm), making it more difficult for LB formation to initiate and maintain stability once initiated.

### 10.3.4 Model Development

In order to elucidate the heat transfer physics governing LBCB, we utilized the Mikic-Rohsenow nucleate pool boiling model [32,33]. The pool boiling heat flux can be calculated as

$$q'' = 2D_b^2 n \Delta T \sqrt{\pi k_f \rho_f c_{p,f} f} \tag{10.6}$$

where $f$ is frequency of bubble departure [Hz], $n$ is the nucleation site density [sites/m$^2$], $D_b$ is the bubble departure diameter [m], $\Delta T$ is the wall superheat [°C], and $k_f$, $\rho_f$, $c_{(p,f}$, are the working fluid thermal conductivity [W/m·K], density [kg/m$^3$], and specific heat [J/kg·K], respectively, evaluated at the saturation temperature $T_{sat}$ (Figure 10.6). A scaling analysis highlights that $q'' \sim D_b^2 n \Delta T \sqrt{f}$. Assuming a square lattice of bubble nucleation sites on the pool boiling surface, then $n \sim 1/D_b^2$, and therefore, the scaling analysis reduces to

$$q'' \sim \Delta T \sqrt{f}. \tag{10.7}$$

The departure frequency, $f$, and thus, $q''$ can be related to the bubble departure diameter since the time required for a bubble to grow [195] to a size $D_b$ is

$$t_b = 0.75\Big((t_b+1)^{\frac{3}{2}} - (t_b)^{\frac{3}{2}} - 1\Big), \tag{10.8}$$

hence $f \sim 1/t_b$. Figure 10.5c highlights how both $f$ and $q''$ increase as $D_b$ decreases. Therefore, to maximize heat transfer performance, the geometry, orientation, and surface roughness for both the condenser and evaporator should be engineered to ensure that $D_b$ is minimized. One method for achieving minimized $D_b$ involves reducing $G$. For $G = 2.5$ mm, the scaling analysis underscores that the empirical observations for $q''$ are of the correct order of magnitude. In addition to the ability to control maximum bubble size tightly, the developed LBCB results emphasize the importance of heat spreading from the hotspot via both conduction and two-phase boiling and evaporation. The LB evaporates at the macroscopic contact line along the PCB and GaN transistor prior to re-condensing on the larger cooled nanostructured surface, thereby enhancing heat spreading and heat rejection.

A secondary mechanism enabling efficient heat transfer of LBCB is the length scales employed in the experimental setup. Past studies have shown that enhanced CHF can be achieved in pool boiling by ensuring inertia-

controlled bubble formation that is limited to within the thermal boundary layer [250]. Although subcooled boiling yields an unsteady thermal boundary layer, care was taken to facilitate bubble formation dynamics in the inertia-controlled regime by maintaining a small gap spacing between the condenser and GaN device.

In order to identify LBCB design guidelines, we utilized our heat transfer measurements and models to determine when LB formation is stable and how to maximize $q''$ for a variety of nanostructured surfaces, setup geometries, and orientations with respect to gravity. Both the apparent advancing contact angle, $\theta_{a,app}$, and the apparent contact angle hysteresis, $\Delta\theta = \theta_{a,app} - \theta_{r,app}$, are important parameters governing LB formation stability. Similarly, G and the angle of the setup with respect to the horizontal, $\Theta_s$, are free design parameters. While $T_{sub}$ and $P_{sat}$ could also be design parameters, they were assumed to be constants in order to reduce the dimensions of the design space considered. Figure 10.7a depicts an example of the design space for feasible LB scenarios on a smooth condenser surface having $\theta_{a,app} = \theta_a = 90°$. Figure 10.7b highlights via a projection of the semi-spherical cap how $\theta_a$ impacts

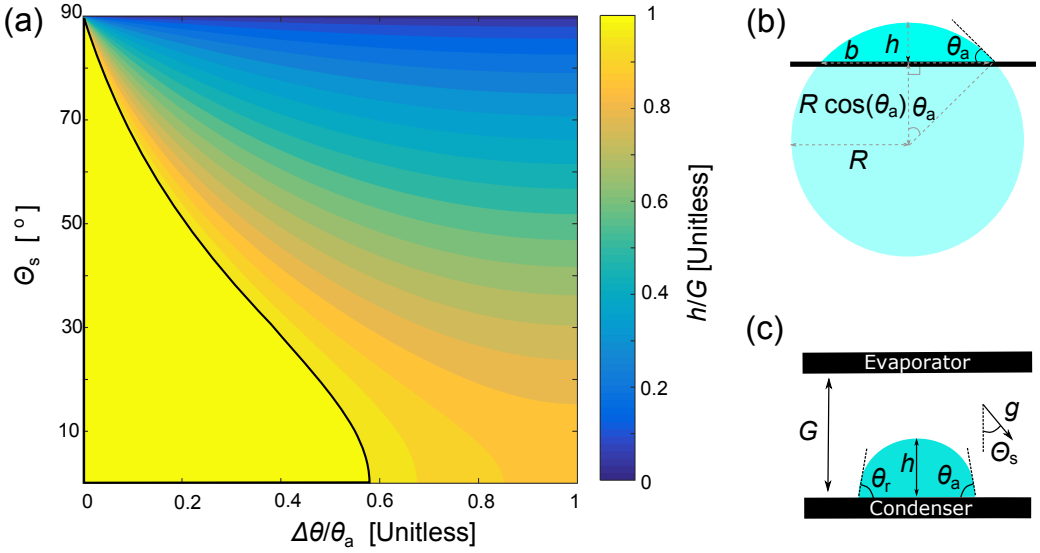


Figure 10.7: (a) Regime map of stable LB formation showing feasible designs (yellow) as a function of normalized contact angle hysteresis ($\Delta\theta/\theta_a$), and orientation with respect to gravity ($\Theta_s$). Schematics of (b) relation between height of the droplet ($h$) and condenser wettability ($\theta_a$), and (c) gap between the evaporator and the condenser ($G$). Model results shown are for $\theta_a = 90°$ and $G = 5$ mm.

droplet height,

$$h = R\Big(1 - \cos(\theta_a)\Big). \tag{10.9}$$

It is reasonable to assume that hemispherical droplets will form and easily bridge the gap between the evaporator and condenser in this work where $G$ $< 5$ mm since the Bond number,

$$\mathrm{Bo} = \rho_f g L^2/\sigma < 0.85, \tag{10.10}$$

where the assumption for the characteristic length was $L = G/2$ and those for the material parameters for the water used in calculations were: surface tension of $\sigma = 0.072$ [N/m], density of $\rho_f = 998.2$ [kg/m3], and local acceleration due to gravity of $g = 9.8$ [m/s2]. Including $\Theta_s$ into our analysis (Figure 10.7c), we show that gravitational body forces impact the maximum radius of droplet growth prior to shedding, which would result in no LB formation [179] for $G > \hat{R}$ where

$$\hat{R} = \left[\Big(6\sin(\theta_e)\sigma\Big(\cos(\theta_r)-\cos(\theta_a)\Big)\Big)/\Big(\pi\rho_f g\cos(\pi/2-\Theta_s)\Big(2-3\cos(\theta_e)+\cos^3(\theta_e)\Big)\Big)\right]^{\frac{1}{2}} \tag{10.11}$$

and $\theta_e$ is the apparent equilibrium contact angle

$$\theta_e = \cos^{-1}\Big(0.5\cos(\theta_a) + 0.5\cos(\theta_r)\Big). \tag{10.12}$$

Assumptions for the material parameters for the water used in calculations were the same as those for (10.10).

After calculating $h$ based on $R = \hat{R}$ and varying $G$, $\theta_a$, $\Delta\theta$, and $\Theta_s$, the sub-space of stable LB formation was identified based on $h/G$. When $h/G > 1$, the droplet growing on the condenser is large enough to physically contact the opposing hot surface prior to sliding off via gravitational body force, and therefore will form a LB. Figure 10.7 shows the required condenser wetting characteristics to facilitate LB formation for all system orientations (yellow shaded region bounded by the black line). For varying $G$, the model clearly indicates that a wide range of nanoengineered surfaces are suitable for LB formation. Figure 10.7a shows that for $\theta_a = 90°$, the region of feasible designs for all system orientations includes a large range of contact hysteresis achievable with current functionalization techniques ranging from

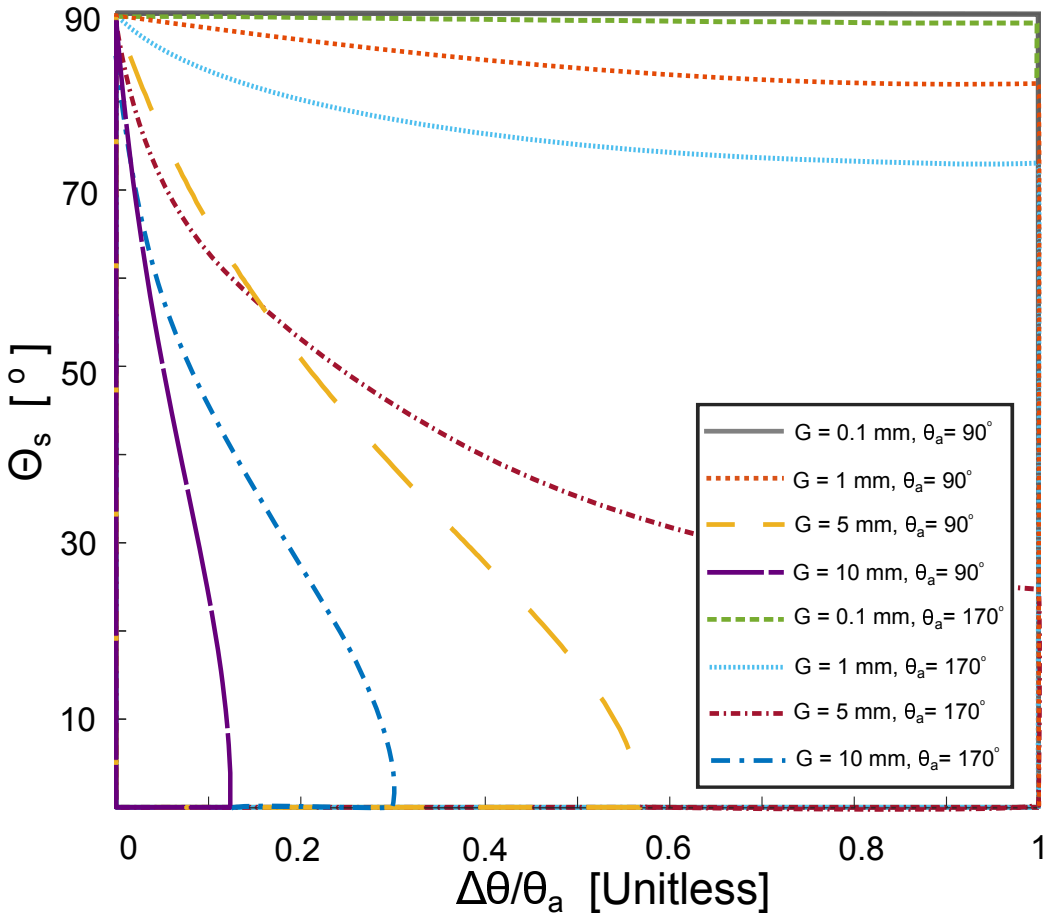


Figure 10.8: Regions with feasible design spaces for varying nanostructured surface roughness, contact angle hysteresis, setup geometry, and orientation with respect to gravity given variations in the system design parameters: $G$, $\theta_a$, $\Delta\theta/\theta_a$, and $\Theta_s$. Feasible nanoengineered surface designs ($\theta_a$ and $\Delta\theta/\theta_a$) and system orientations ($\Theta_s$) must stay within the region bounded by the fronts depicted for specific design decisions for $G$ and $\theta_a$.

polymeric coatings and self-assembled-monolayers ($\Delta\theta \approx 20°$) [189, 257], to liquid-like polymer brushes and liquid infused surfaces ($\Delta\theta \approx 2°$) [258–260]. While the developed guidelines center around a conservative scenario of a horizontal evaporator located above a condenser, this analysis highlights that, even for $G = 10$ mm, LBCB is stable for all orientations and geometries as long as $\Delta\theta/\theta_a < 0.1$ (Figure 10.8). It is also important to note that, at droplet length scales larger than the capillary length, droplets cease to have spherical shape and gravitational effects become pronounced, leading to puddle formation [261]. Figure 10.9 highlights how the size of the acceptable design area increases with decreasing $G$ and increasing $\theta_a$. Interestingly, as $\Theta_s$

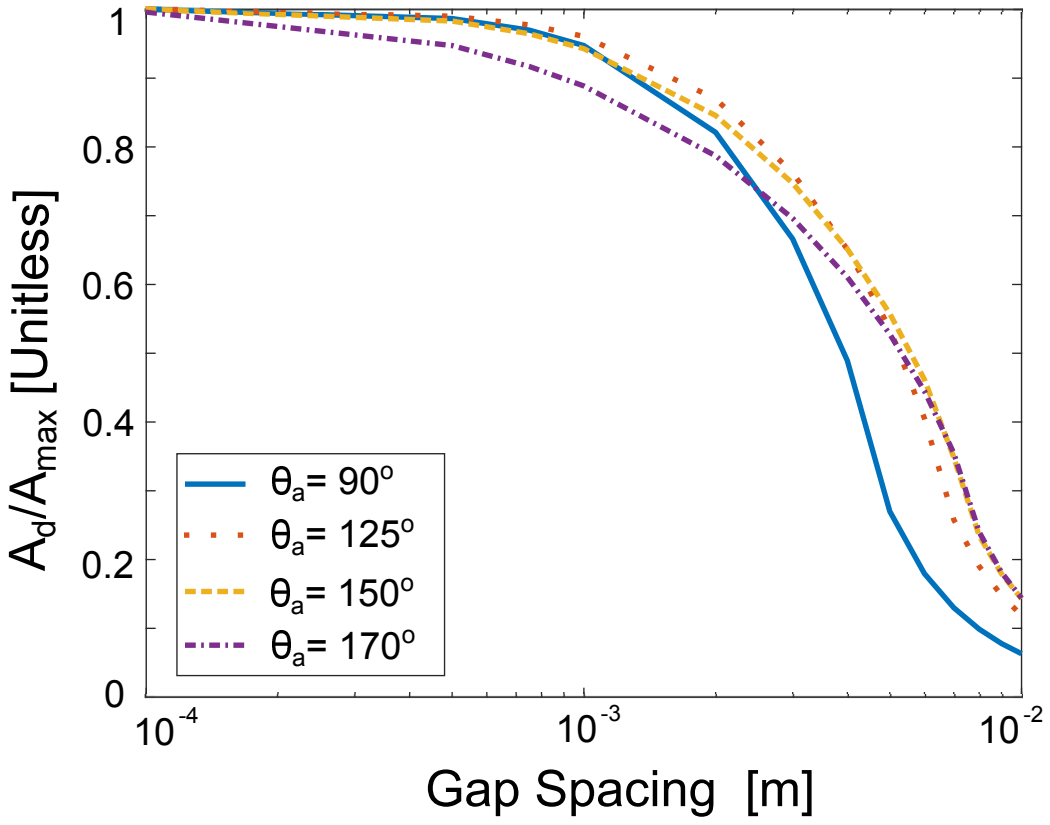


Figure 10.9: Utilizing a unitless ratio of the maximum design space area ($A_{max}$) and the resultant area ($A_d$) from the feasible design spaces based on $\theta_a$, $\Delta\theta/\theta_a$, and $\Theta_s$, the impact of $G$ and $\theta_a$ on the number of design spaces can be determined. If the ratio is equal to 1, then the liquid bridge will form for all possible $\theta_a$, $\Delta\theta/\theta_a$, and $\Theta_s$. As this unitless ratio decreases, care must be taken to ensure that the surface roughness, geometry, and orientation are controlled such that the frequency of liquid bridge formation is not jeopardized. As $G$ increases, surface roughness can be modified to ensure that the normalized design space is maximized.

increases to 180°, where the evaporator would be facing up (Figure 10.7c), the condenser surface would need to be more hydrophilic so that the LB lifetime can be prolonged due to strong attraction to the cold nanostructured surface.

### 10.3.5 Implications

In addition to the heat spreading and heat transfer advantages of LBCB, other benefits exist. Using LBCB enabled vapor chambers, one can overcome the obstacles created by thermal interface materials (TIMs), which are at

the heart of conventional electronics cooling strategies [79]. While TIMs provide mechanical compliance and often electrical isolation between the fragile electronics and a heat sink, TIMs create a thermal bottleneck due to their lower thermal conductivity ($\sim$ 1 W/m·K), which ultimately limits the power density of the system [98–101, 159, 160, 168, 169]. Eliminating the need for TIMs by enabling ultra-low thermal resistances and enhanced spreading realized with boiling heat transfer directly from electronics offers a significant improvement over state-of-the-art and enables a new design space for the development of dense electronic assemblies. For example, LBCB could enable the design of dense, high-power electronic assemblies with low-duty-cycle (pulsed) operating conditions such as defense systems, downhole drills, or radar. In addition to the low thermal resistance, LBCB offers efficient heat spreading by leveraging the high latent heat of vaporization of water [178, 179, 229].

Moreover, to avoid the potential of liquid water creating a short circuit for the electronic components, the tests here were operated only with direct current (dc) conduction where the joule losses were varied based on drain current. Future work should incorporate a commercially available thin ($\sim$ 100 nm), high dielectric strength, passivation coating (Figure 10.1), that can ensure fidelity of the current approach in all conditions without shorting, demonstrating a path for integration in practical operational environments. Another practical consideration for power electronics designers involves the high-frequency common-mode current that flows through the TIM, which acts as the dielectric medium for a parasitic parallel plate capacitance between the heat sink and fluctuating potential at the drain pin of the transistor. This noise current can create electromagnetic interference (EMI), which can violate federal regulations and degrade converter reliability [98–101, 168, 169]. While the gap between the electronics and the heat sink with the LB will be much larger than a gap filled with TIM, water is known to have a higher relative permittivity than many TIM materials [262]. Yet, the collapsing and reforming behavior of the LB may cause the impedance of this high-frequency capacitor to change dynamically, which could cause a spreading effect of the spectrum over the course of a measurement and better overall EMI performance.

In addition to the LBCB vapor chamber device utility, the observation of LB formation inside of an active vapor space having a superhydrophobic

condenser surface puts in perspective the wide range of measured heat fluxes reported in the literature for different jumping droplet phase-change cooling schemes [1, 176, 177, 180, 183, 186, 191–193, 229, 263]. While the vast majority of vapor chamber research involves assemblies that do not permit imaging of the vapor space, the experiments presented here offer the unique capability of examining how heat dissipation and hydrodynamics couple to one another inside the vapor space. The observed presence of LB formation at elevated heat fluxes most likely occurred in past jumping droplet vapor chamber characterization experiments, where the vapor space had characteristic thicknesses smaller than the capillary length of water (≈2.5 mm). Indeed, the discrepancy between previously reported droplet jumping maximum heat fluxes of ≈10 W/cm$^2$ in an the open vapor chamber system [1, 176, 177] and ≈500 W/cm$^2$ in a closed device [186] indicates that LB formation was highly probable in the closed device, but not observable due to the closed system architecture.

Analogous to jumping droplet vapor chambers [1, 176, 177, 180, 183, 186, 191, 193, 229, 263] and thermal diodes [192], the LBCB method demonstrated here leverages wickless liquid transport from the evaporator to condenser. Since the cold liquid is returned to the hot spot via self-assembling LBs, the heat transfer via LBCB is not limited by the need for external pumping or capillary forces to drive liquid return to the hot spot. The lack of pumping required is a key benefit due to: (1) alleviation of aspect ratio design requirements governed by the need for liquid return [175, 264], (2) elimination of additional thermal resistances such as wick structures, and (3) simplified manufacturing and integration. Moreover, this LBCB is also different from jumping droplet vapor chambers since flooding that invariably exists is no longer detrimental to heat transfer. Besides bubble formation within the LB, vapor return for very efficient heat spreading on the condenser also exists through the open cavity of the vapor chamber (Figure 10.1). While the highest rate of condensation occurs at condenser locations closest to the hot spot [192], maximizing the collection of condensate that forms away from the hot spot can be addressed in three ways: (1) by controlling the density of hot spots, (2) functionalization of the hot spot surface, and (3) the aspect ratio (height/width) of the LCLB vapor chamber. Since the LBCB approach is proposed for dense electronic assemblies, hot spot spacing has important implications for heat transfer effectiveness. Appreciable spacing between hot

spots can increase LB lifetimes and magnify heat spreading by offering a larger area for LB replenishment of cold condenser liquid. However, if hot spot spacing is too large (dilute limit), condenser liquid located away from the LB may reside unused. While denser hot spots enhance the pool boiling effects within the LB, a denser array of hot spots would require supplying sufficient liquid from the sides-to-center of the hot spot array in order to avoid large temperature gradients. Thus, a tradeoff exists between hot spot density and condensate utilization. In addition to direct LB formation on hot spots (Figure 10.1), the functionalization of the PCB with a porous superhydrophilic coating would benefit LBCB performance. The inclusion of a wicking superhydrophilic layer on the PCB enables large coalesced droplets, which form LBs away from hot spots to provide condensate liquid to the hot spots.

Besides vapor chamber hot spot cooling, the high previously reported heat fluxes during jumping-droplet thermal diode operation [192] exceeding the flooding limit ($> 10$ W/cm$^2$) of CuO superhydrophobic nanoengineered surfaces [191, 193, 263] most likely stemmed from the formation of LBs within the diode. Interestingly, LBCB enables the development of a new type of thermal diode utilizing only LBs as a passive method to transfer heat selectively in one direction. Analogous to passive jumping droplet thermal diodes [192], integration of a superhydrophilic evaporator and superhydrophobic condenser enables stable heat flow in the forward direction (evaporator to condenser) via LB formation. However, the reverse direction would have limited heat transfer due to the accumulation of working fluid on the wetting evaporator surface, eliminating LB formation and thus heat transfer.

This LBCB phenomenon is also unique due both to the nature of the LB self-assembly process and the capacity of the LB to facilitate boiling in a pool confined only due to surface tension. The ability to promote enhanced heat transfer via favorable Marangoni flow establishment makes the proposed approach advantageous when compared to phase-change techniques having negative-feedback mechanisms associated with higher heat fluxes. Moreover, by keeping the gap spacing between the condenser and evaporator less than the thermal capillary length, inertia-controlled bubble formation was maintained, which enabled enhanced CHF. Furthermore, the impact of subcooling the cold plate on effectiveness of the heat transfer via

LBCB cannot be understated and needs to be explored further in order to incorporate subcooling into the LBCB design rules. Future work will seek to further characterize the boiling curve for the developed LBCB cooling method in order to identify the maximum possible CHF and to understand how different design parameters for the LBCB vapor chamber system impact CHF. Besides impacting the estimate of the heat flowing through the LB, higher order modeling could result in an increase of the effective wall surface area, which would impact $q''$. Moreover, the impact of gap spacing, subcooling of the cold plate, and wettability of the condenser on the lifetime and cooling capability of the LBCB cooling method need to be examined. While Marangoni forces dominated buoyant forces for the gap spacings considered here, buoyant forces begin to dominate for inverted architectures (hot spot on bottom) with $G \geq 14$ mm.

The scaling and design rules presented in Sec. 10.3.1 governing liquid bridge stability and heat transfer, and in Sec. 10.3.4, were intended to establish an initial framework for identifying the key governing parameters in the Marangoni dominated regime ($G$ <14 mm). In addition to flow-governing forces (Marangoni vs. buoyancy), we also considered forces governing the shape of the condensate droplets in the context of LB formation (gravity vs. capillarity). Small condensate droplets like those studied here lead to hemispherical droplet shapes and the aforementioned LB formation physics since capillarity dominates. As the condensate grows without touching the hot spot, i.e. ($Bo \gg 1$), gravity becomes the dominant driving force. In the gravity-dominated regime ($Bo \gg 1$), the hemispherical droplet shape approximation is no longer valid, resulting in the formation of irregular puddles on the condensing surface. Given that $Bo > 3$ for droplets having diameters $D_b > 10$ mm, puddle formation on the condenser surface in some orientations and spacings will inhibit LB formation. This crossover of multiple fundamental forces points to the need for future numerical model development of LB formation dynamics, collapse, and reformation to account for different regimes in order to determine LB stability and LBCB feasibility for chamber geometries outside of the design space examined here.

The liquid quenching of the hot spots via the proposed LBCB technique is appealing since direct cooling methods for electronics eliminate the need for thermal interface materials and this approach offers a simple path to integration with 3D electronics assemblies. Yet, more work is needed to

optimize the thickness of any electrical passivation such that: the LB does not compromise long-term reliability of electrical performance due to shorting the device during switch-mode operation, this enhanced heat transfer pathway is not degraded by the thermal resistance of the passivation layer, and the final thermal management scheme does not degrade the overall EMI performance of the circuit. The confined boiling technique developed here holds great promise for enabling the development of fully 3D integrated electronics packaging via high heat flux dissipation and thermal routing from internal hot spots.

## 10.4 Conclusions and Future Work

In summary, we have developed and studied the heat transfer mechanisms and hydrodynamic phenomena present in LBCB. Through detailed experiments and modeling, we show enhanced hot spot heat dissipation rates of $> 100$ W/cm$^2$ and heat transfer coefficients approaching 50 kW/m$^2$K. The demonstrated performance approaches that of classical pool boiling while at the same time helping to overcome the design obstacles of high-power-density electronics packaging. In stark contrast to single-phase cooling, pumped flow boiling, and other high heat flux and heat spreading methods like vapor chambers and confined boiling schemes, the developed LBCB approach is entirely self-contained and does not require a pump or internal wicks to re-supply liquid to the hotspot or a TIM for connecting the hotspot with the heat spreader. We use analytical models to develop generalized design rules for alternate orientations and vapor chamber geometries. The simplicity of integration without compromise on heat transfer performance, along with the simultaneous removal of unwanted parasitic thermal resistances, presents a significant benefit of LBCB compared to the state-of-the-art, and has the potential to facilitate ultra-compact system integration.

# CHAPTER 11

# BENCHMARKING THE BENEFITS OF DIRECTED COOLING

*Engineering is a useful purpose for man. We work for the world, not for ourselves. Yet, research alone is not enough. Education is what takes research and makes a true change for humanity. Learn and apply! Nothing is impossible as long as you put your heart and mind into them.*

– William L. Everitt, 1900-1986 (UIUC Engineering Dean 1949-1968)

## 11.1 Introduction

Figure 11.1 underscores the challenge of simultaneously increasing both efficiency and power density for a converter since this would disrupt the Pareto-front established by industrial state-of-the-art designs. Comparing

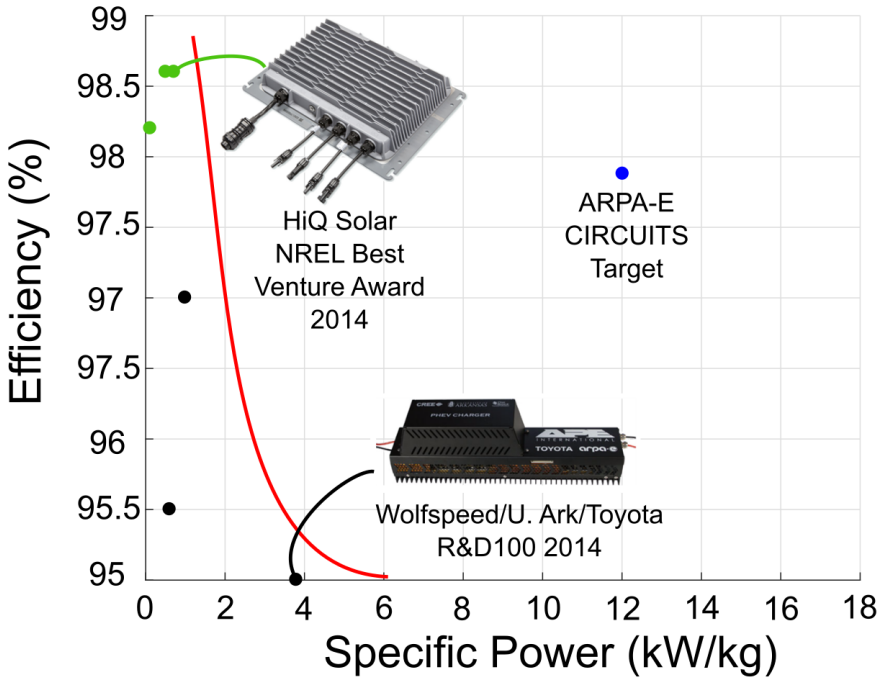


Figure 11.1: Power converter efficiency is in competition with both volumetric and gravimetric power density. Data for survey synthesized from [265–270].

and contrasting solar inverters and automotive bi-directional chargers demonstrates clearly how application requirements govern design choices. Solar inverters prioritize efficiency as a primary energy source and an automotive bi-directional charger seeks the highest possible power density to enable enhanced system performance (e.g. larger variety of packaging options inside of the vehicle, increased range, faster charging times by increasing the power rating for the same volume and weight). Realizing the disruptive increase in these figures of merit in Figure 11.1 for a 6.6 kW bi-directional electric vehicle (EV) charger is the goal of the ARPA-E Creating Innovative and Reliable Circuits Using Inventive Topologies and Semiconductors (CIRCUITS) program and requires equitable electro-thermal co-design of the power converter and thermal management solution. Section 11.2 highlights the development of a compact, lightweight cold plate capable of dissipating the target loss profile. Lessons learned from examining directed cooling schemes motivated the investigation of the opportunities and engineering challenges of integrating these schemes with power transistors. Section 11.3 emphasizes the promising results for the directed cooling of coated GaN devices with water routed by an additively manufactured manifold.

## 11.2 Developing Advanced Cold Plate

The high-performance cold plate developed to reject the heat generated by the hot spots inside of a packaged 6.6 kW bi-directional charger also enables an apples-to-apples comparison between the proposed directed cooling scheme and this advanced cold plate. This section outlines the design and characterization of this conventional thermal management method (i.e. advanced cold plate and thermal interface materials (TIMs)).

### 11.2.1 Designing and Fabricating an Advanced Cold Plate

The path of development for this advanced cold plate comprised: (1) several iterations of design and simulation (Figures 11.2 and 11.3) in order to converge on a high performing solution and (2) fabrication and extensive subsystem testing via custom-developed thermal testbeds and surrogate

power electronics evaluation modules (Figure 11.5). Having completed mechanical validation, future work will examine the system-level performance with the 6.6 kW bi-directional charger prototype and results can be compared against the measurements obtained with the thermal testbed of Figure 11.5.

First, the roughly 190 W of loss from the electronics was not rejected uniformly over a large surface. Figure 11.2 highlights that the densely packed electronic components can be segmented into six different zones with unique power dissipation (i.e. 30 W in region 1, 50 W in both regions 2 and 3, 30 W in region 4, and 15 W in both regions 5 and 6) and heat flux requirements. For example, region 1 was the most difficult to cool since this portion of the converter had the closest packing of small surface area components. Manufacturing a single path for fluid to flow through the cold plate did not enable extraction of enough heat from both the high heat flux areas and the lower heat flux portions of the design, like regions 5 and 6, for all of the electronics to have remained within the target temperature range. Thus, a multichannel design was proposed to provide equitable flow to all regions of the cold plate and also reduce the overall pressure drop. Figure 11.3 demonstrates how the highest velocity flow remains

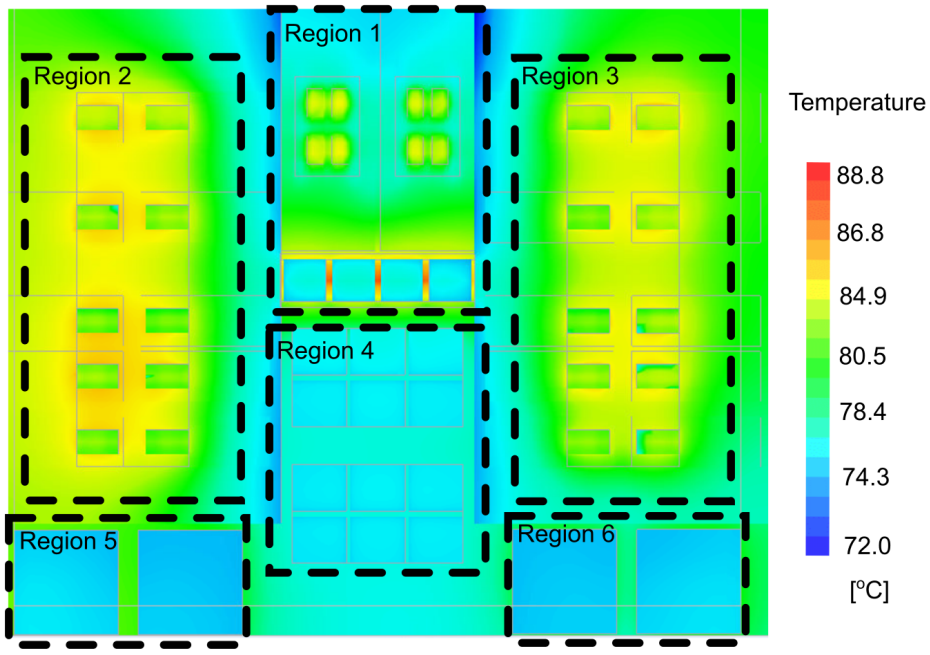


Figure 11.2: Sufficient heat transfer exists with the cold plate design so that the hottest temperature estimate would remain below 90 °C for all six regions.

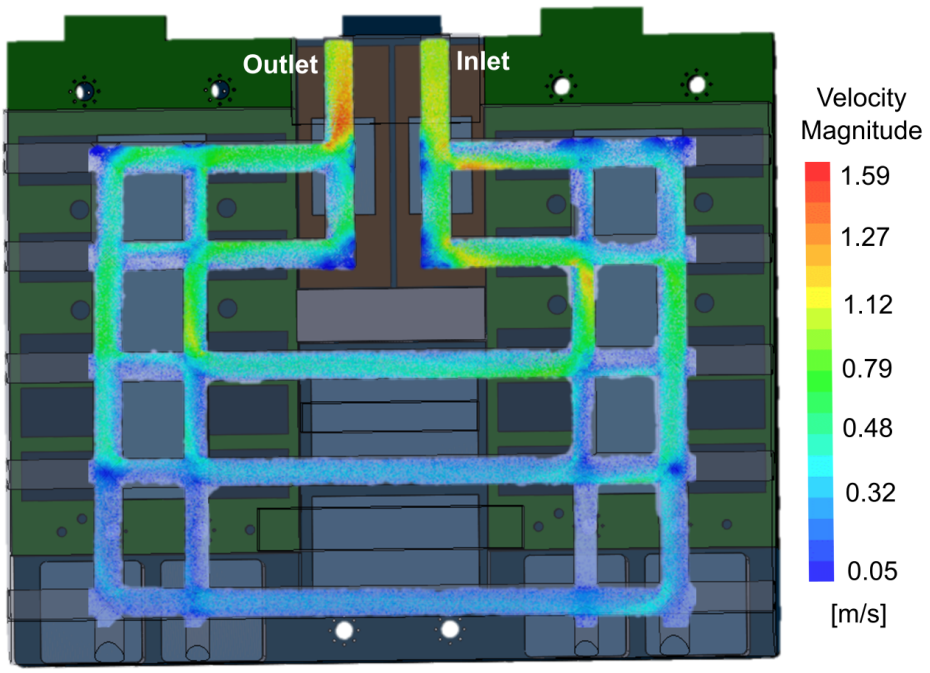


Figure 11.3: A network of internal channels for the advanced cold plate was designed to ensure minimal pressure drop and sufficient fluid flow for all regions.

within the loop surrounding region 1 with the inlet and outlet pipes located directly above the highest heat flux components. Similarly, two parallel paths through regions 2 and 3 reduced the temperature gradient across the cold plate and improved the isothermal distribution for these interleaved converters. A single, slow-moving fluid path easily rejected the losses from regions 5 and 6 since these were the lowest heat flux components. Overall, the simulations from ANSYS Icepak demonstrated that this design had promising performance as a thermal management solution with a maximum temperature rise of $\sim$19 °C for a fluid inlet temperature of 70 °C.

Manufacturability and integration constraints were paramount throughout the design process. For example, selecting 6063 aluminum as the material provided high thermal conductivity (220 W/m·K) and low density (2.7 g/cm$^3$), and was readily machinable. The multichannel design depicted in Figure 11.4a enabled subtractive manufacturing of the cold plate from a single rectangular bar of 6063 aluminum. The 5 mm channel diameters reduced the risk for internal clogging and facilitated the use of extra-long drill bits with sufficient rigidity to fabricate the entire length of each channel. The ends of each channel were sealed with J-B cold weld epoxy since this provided

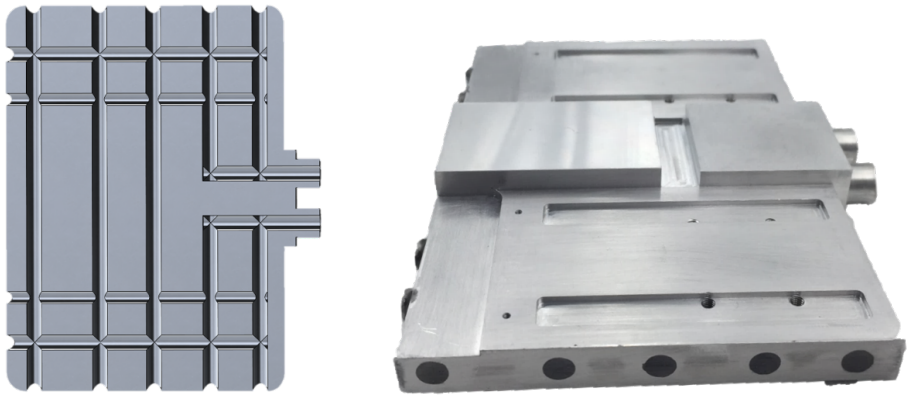


Figure 11.4: Advanced cold plate was fabricated (a) with a multichannel design and (b) from a single piece of high thermal conductivity 6063 aluminum to mate with a multi-layer electronics assembly.

sufficient strength for the temperatures and pressures in this system and welding caps could have warped the cold plate. Machining posts at the inlet and outlet offered several benefits: (1) Tapping a hole to mate with a male connector requires extra material above and below the channel so the posts facilitate the thinnest possible design (i.e. reducing both weight and volume). (2) The overall component count decreases since a flexible pipe can be easily secured to the post with a hose clamp and no additional connectors are required. (3) The total number of points where a leak might occur is reduced. The top surface of the cold plate depicted in Figure 11.4b was machined to accommodate the varying height profile of the electronics mated with these surfaces since the hotspots resided on printed circuit boards at different vertical heights. For the final step of integration, a clay TIM is placed between the cold plate and the electronics to provide mechanical compliance given that variations in the height of these components exist due to tolerances in manufacturing.

### 11.2.2 Testing the Advanced Cold Plate

Since the goal for this co-design effort centers around achieving high power density, the first metrics to examine are weight and volume. With maximum dimensions of 105 mm x 128 mm x 15 mm, the cold

plate had an overall volume of 0.17 L, which was 19% lower than the goal of 0.21 L and satisfied this design requirement. With regard to weight, the complete thermal management solution (including two hose clamps, TIM, and the cold plate) was 300 g, which was 25% lower than the goal of 400 g. The fluid testbed shown in Figure 11.5a was designed to benchmark the hydrodynamic performance of the cold plate comprising a flow meter (Kobald MIM-1210GG5C3T0), differential pressure sensor (Omega MMDWB015BIV10B2C0T4A6CES), absolute pressure sensor (Omega MMA150V10B2C0T4A6CE), four-wire RTDs (REOTEMP AT-PX1123YLR4S1T2T), and a chiller (PolyScience N0772046-6160T21E4Q1NR). Calibration of the setup using the standard k-value method [204] accounted for the pressure drops due to the connectors, metal tees used to attach sensors, and additional pipping between the setup and the cold plate. For flow rates less than 2.9 LPM, the maximum pressure drop did not exceed 100 mBar, which was the requirement established for this project. Simulated and experimental pressure drop results agreed within roughly 10%, which indicated that remaining differences were most likely due to roughness of the internal channels of the cold plate not modeled in ANSYS

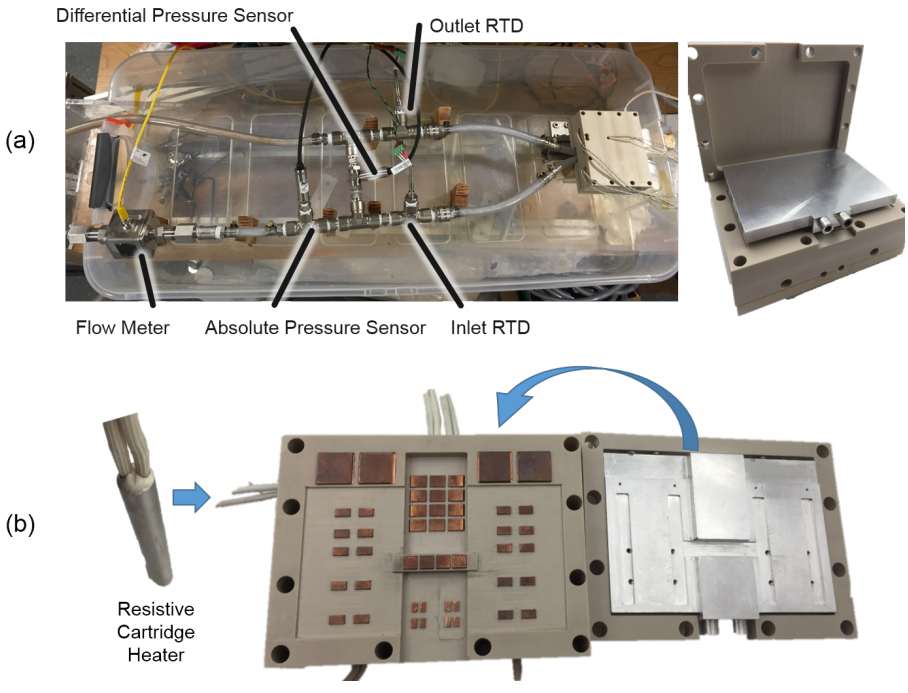


Figure 11.5: Advanced cold plate performance was benchmarked both for (a) pressure drop and (b) maximum hotspot temperature.

Icepak. The heat rejection capability of the cold plate was characterized with a custom thermal surrogate shown in Figure 11.5b comprising PEEK insulation surrounding copper blocks cut to have the dimensions of each electronic hot spot and heated with individually controlled cartridge heaters. This method for benchmarking a cold plate provided valuable insight without the need of final converter hardware, which enables the rapid prototyping of this type of thermal management solution. For the flow rates between 1 and 3 LPM, the maximum hotspot temperature for any of the heaters did not exceed 95.2 $\pm$ 1.8 °C, which was a hotspot in region 1 of the electronics assembly. The difference in maximum temperature predicted by ANSYS Icepak and measured in the laboratory was at first considered anomalous. Searching for the source of this discrepancy prompted an examination of the thermal conductivity of the TIM.

### 11.2.3 Probing Thermal Conductivity for Commercial Thermal Interface Materials

TIMs, important implementation materials for modern electronics cooling strategies [79, 101, 147], are also a key obstacle to achieving improvements in power density. While TIMs provide mechanical compliance and often electrical isolation between the fragile electronics and a heat sink, the low thermal conductivity (between 1 and 10 W/m·K) of TIMs creates a thermal bottleneck and ultimately increases the size and weight of the heat sink in order to improve heat flux through this pathway. Measuring the performance of TIMs is crucial for improving the fidelity of models for rapid prototyping and optimization of the cold plates. Based on experimental performance of power converters being cooled with both conventional and advanced methods, we observed that the TIMs were not performing as well as the datasheets suggested was possible. This experimental survey seeks to reexamine the IEEE Standard 98-2002 and ASTM D5470-06 thermal interface material characterization standards. Through a survey of commercial TIMs, changes in thermal conductivity were probed based on variations in pressure (5% to 80% compression of TIM) and environmental conditions such as humidity (40% to 90%) and heat flux (1 W/cm$^2$ to 100 W/cm$^2$). Figure 11.6 depicts the custom experimental testbed constructed to evaluate the TIM performance

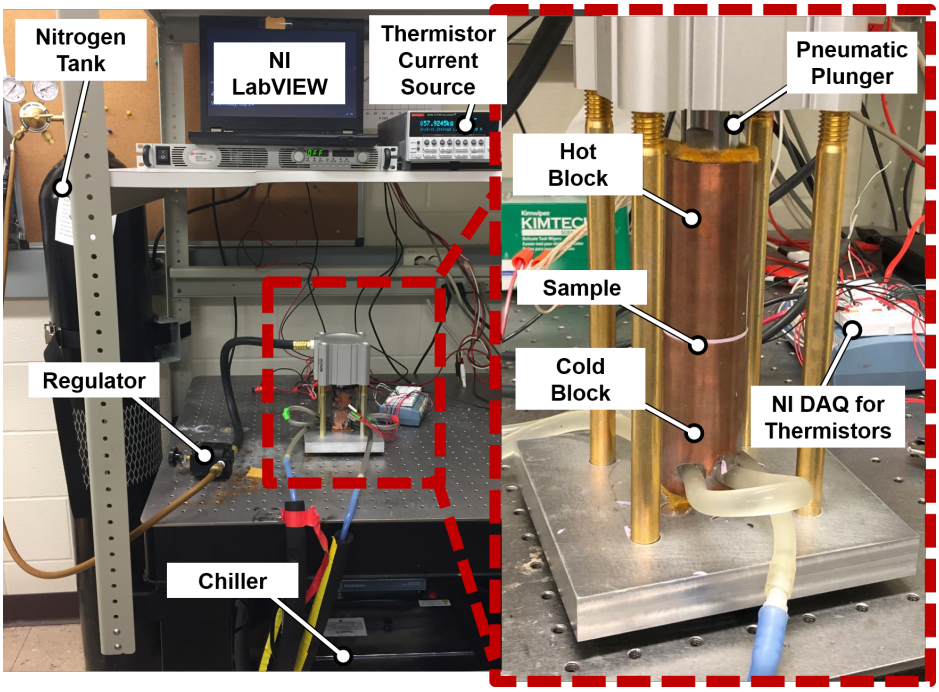


Figure 11.6: Custom testbed for evaluating the thermal conductivity of commercial TIMs.

including: hot and cold copper blocks with six thermistors, TIM sample under test, nitrogen gas and a plunger system for applying pressure to the samples, and LabVIEW for automated control and data acquisition for the experiments. Thermistors were placed at 2 mm increasing intervals above and below the sample. By tracking the change in temperature for each of these known sensor locations and the sample thickness, the heat flux through the sample, and subsequently, the thermal conductivity, could be calculated for varying pressures. Preliminary experiments revealed that the datasheets [271–273] for a survey of commercial TIMs regarding thermal conductivity disagree with experimental measurements by 40% to 70%. These initial results help resolve the difference between simulated and measured maximum hotspot temperature for the advanced cold plate. On-going work is expanding this analysis to capture a comprehensive survey of commercial TIMs in order to inform the modeling and optimization of future thermal management solutions.

## 11.3 Directed Cooling of Electronics with TIM-less Packaging

With an understanding established of the key loss generating mechanisms in power converters and the vast potential of TIM-less thermal management techniques, the remainder of the dissertation research focused on developing a framework of electro-thermal design rules to realize improvements in volumetric and gravimetric power density through the directed cooling of hotspots. Another compelling reason to explore the directed cooling aspect of this electro-thermal problem involves the co-design of an additively manufactured manifold for routing the fluid to the hot spots. On one hand, additive manufacturing of a plastic manifold offers clear opportunities for enabling custom routing of cooling channels toward hot spots and lightweighting of the overall manifold through material selection and structural optimization to reduce unnecessary mass. Yet, the flexibility of additive manufacturing to create geometries and structures that cannot be realized with traditional subtractive fabrication methods is a key ingredient for realizing a TIM-less packaging scheme by empowering every gram or cubic centimeter within the assembly to serve a useful purpose. For example, routing fluid to hot spots and enhancing heat transfer can be achieved through additively manufactured features within the channel, the intentional placement of passive and active components within the channel, or a combination of both design choices.

Realizing a denser assembly of these capacitors and wide-bandgap transistors than is possible with an advanced cold plate requires reimagining the approach to packaging power electronics. Figure 11.7 underscores how the need for TIMs to enable compliance and electrical isolation is eliminated by promoting enhanced heat spreading and directed cooling of hot spots via the vapor deposition of a thin, conformal layer of parylene on top of the components. Thermal test vehicles (Figure 11.7) were designed based on the loss profile specifications for the 15 kW/L, 6.6 kW bi-directional charger ARPA-E project and constructed to validate this avant garde cooling approach for realistic levels of heat dissipation. Considering the constraints of the extreme environmental conditions found in automobiles and the design requirements for standard cooling loops (i.e. working fluid, pressure drop, flow rate, inlet and outlet temperatures, etc.), an energy balance

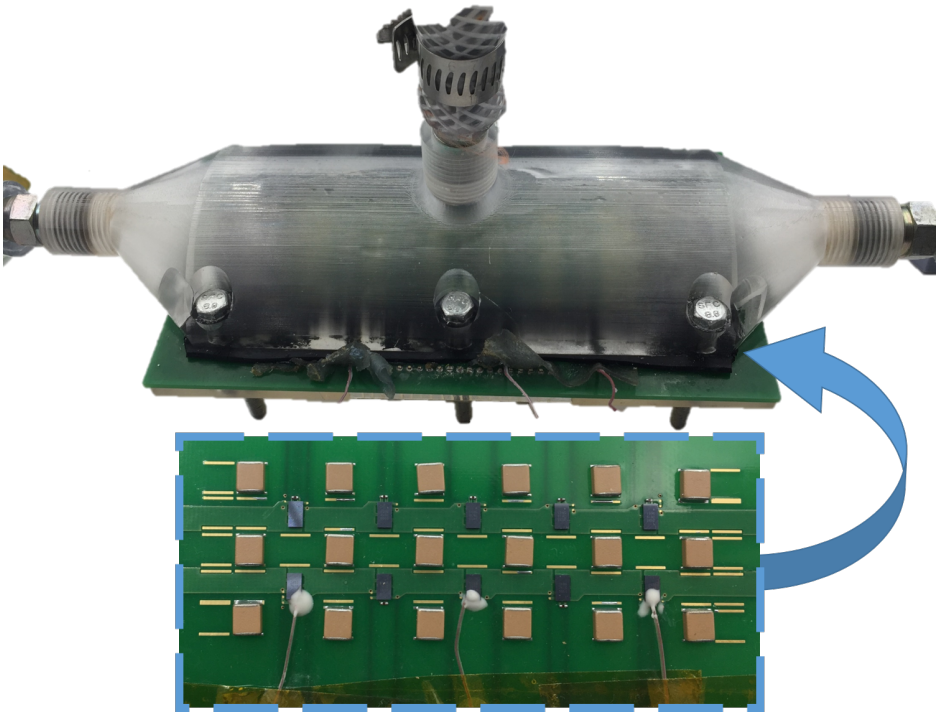

Figure 11.7: A TIM-less directed cooling scheme with single-phase water impinging on hot electronics coated with parylene.

highlighted that rejecting heat via water offered considerable design freedom for pursuing different TIM-less, direct cooling schemes. By configuring the GaN transistors to operate as lossy diodes, the power loss and device temperature could be determined by tracking changes in the voltage drop across each device. These insights were correlated with measurements from thermocouples bonded to the top of the coated GaN devices using high thermal conductivity epoxy (Duralco 128 Resin) in order to gain a more complete picture of the thermal circuit. Measurements from the lab with the thermal testbed depicted in Figure 11.5a revealed that GaN devices could dissipate over 2X more power while maintaining a hotspot temperature less than 100 °C compared to what could be achieved with the advanced cold plate.

Future work can achieve even more significant improvements by optimizing the manifold and electro-thermal layout of the converter simultaneously. Moreover, the transition to two-phase pumped flow has strong potential to offer significant benefits over other state-of-the-art cooling techniques since the thin coating provides electrical isolation without inhibiting heat transfer.

# CHAPTER 12

# CONCLUDING THOUGHTS

*There is no good in anything until it is finished.*

– Genghis (Temüjin) Khan, 1162-1227

Extracting heat efficiently from ultra-compact electronics assemblies requires unconventional heat transfer mechanisms such as phase-change or directed cooling on coated components. Liquid-vapor phase-change cooling has significant potential to facilitate the development of highly dense electronics by leveraging latent heat during the phase transition to remove heat from electronics hot spots.

After reviewing the origins and operational principles of power converters, the difficulty of sufficiently cooling next-generation wide bandgap power transistors was elucidated with a direct comparison to heat fluxes for extreme environments like rocket reentry and the surface of the Sun. Realizing the significance of converter power density to both system design and society at large through the carbon footprint of the subsystem and system life-cycles, special care was given to describing the best-practices for measuring first- and second-order loss mechanisms both in ambient and extreme environments. Given these insights about how and where losses will be generated in a packaged power converter, two unconventional forms of liquid-vapor, phase-change cooling were examined during the course of this research. First, scaling analysis for heat flux of jumping droplet condensation, involving time-scales, mass flux estimates, and the hydrodynamic behavior of jumping droplets, revealed that significant opportunity exists for jumping droplet condensation as long as the average jumping radius decreases (i.e. allowing more droplets to jump per second and increasing the amount of useful cooling time before the surface floods). While a custom vacuum chamber was developed to measure heat flux for jumping droplet cooling of electronics, experimental mass flux measurements aligned with predictions from the theory that an obstacle involving the durability of the nanostructured coatings still exists and must be addressed before scientists and engineers can realize the full potential of jumping droplet phase-change cooling.

Realizing that the other form of liquid-vapor phase-change involves bubble formation during boiling, the nanostructured coatings were modified to increase the flooding rate in order to promote the formation of self-assembled liquid bridges, and subsequently, extremely efficient confined boiling directly on top of the GaN transistor. Next, a fair comparison between a combination of state-of-the-art cold plate and thermal interface material thermal management solution and a combination of a plastic additively manufactured manifold to route fluid over the conformally coated power transistors, revealed superior performance of the directed cooling approach both for higher heat flux and simultaneously lower pumping power than alternative methods.

All in all, this dissertation contributes to the development of volumetrically and gravimetrically dense power converters by shedding light on new design frontiers for dense electronics packaging.

# APPENDIX A

# SCALING ANALYSIS FOR JUMPING DROPLET CONDENSATION HEAT FLUX LIMITS

## A.1 Derivation of Jumping Droplet Timescale

From experiments and modeling [200, 201] reported in Figure A.1, the coalescence time ($\tau_c$) has been shown to be:

$$\tau_c \approx \left(\frac{\rho R^3}{\gamma}\right)^{\frac{1}{2}}. \tag{A.1}$$

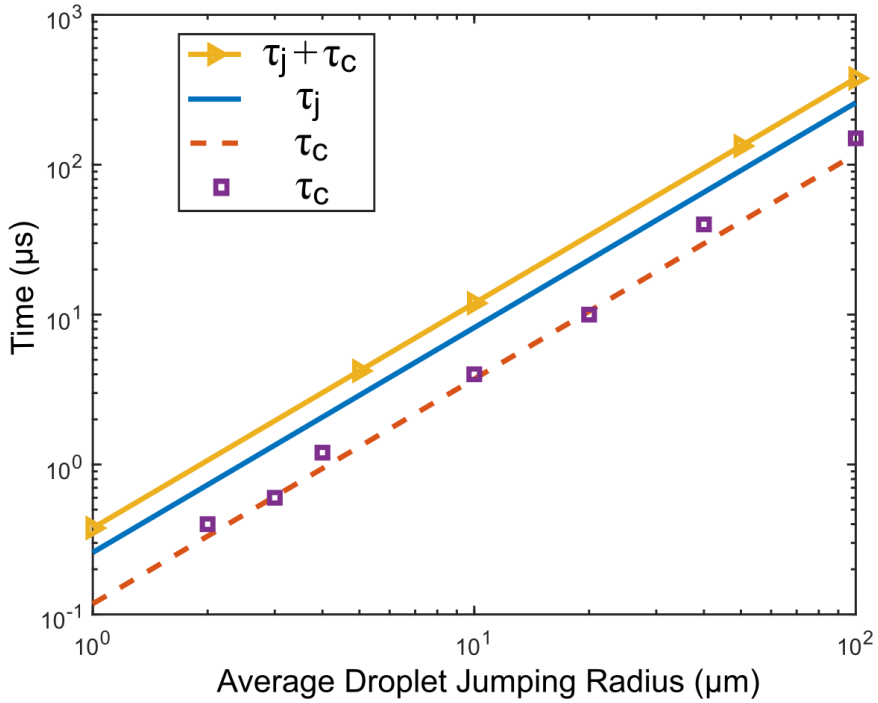


Figure A.1: Experimentally measured and modeled coalescence times given average droplet jumping radius, $R$. Purple squares correspond to experimental measurements from [200] and the remaining lines are based on the models and measurements from [201].

Depicted in Figure A.1, the jumping time ($\tau_j$) can be related to the coalescence time by [200, 201] via

$$\tau_j \approx 2.2\tau_c. \tag{A.2}$$

The release time ($\tau_r$) is the time required to travel greater than $R_m$ away from the surface, which can be found by taking the initial jumping velocity:

$$v_j \approx 0.23\left(\frac{\gamma}{\rho R}\right)^{\frac{1}{2}}, \tag{A.3}$$

and $\tau_r$ determining directly as:

$$\tau_r \approx \left(\frac{R_m}{0.23\left(\gamma/\rho R\right)^{\frac{1}{2}}}\right) \approx 4.35R_m\left(\frac{\rho R}{\gamma}\right)^{\frac{1}{2}}. \tag{A.4}$$

For the growth timescale of the droplets ($\tau_g$), previous studies have shown:

$$\tau_g \approx R\left(\frac{\partial R}{\partial t}\right)^{-1}, \tag{A.5}$$

which represents the amount of time required for a droplet to grow to finite size, $R$, assuming the radius-dependent growth rates, $\left(\frac{\partial R}{\partial t}\right)$, as shown in Figure A.2. This is a conservative assumption as the growth rate of droplets will be higher at lower radii during the growth, resulting in a longer timescale estimate.

Scaling analysis [198, 199] shows that the growth rate of the droplet dominates ($\tau_t \sim \tau_g$) and is governed mainly by the vapor-to-surface temperature difference, $\Delta T$, the coating thermal conductivity, $k_c$, the working fluid thermal conductivity, $k_f$, the coating thickness, $\beta$, and the Nusselt number, $Nu(\theta, Bi)$, which is a function of the droplet apparent advancing contact angle, $\theta$, and the droplet Biot number, $Bi$, based on the base radius:

$$\tau_t \sim R\left[\frac{\Delta T\pi R^2\left(1-\frac{R_m}{R}\right)}{\left(\rho h_{fg}\pi R^2(2+\cos(\theta))(1-\cos(\theta))^2\right)\left(\left(\frac{\beta}{k_c sin^2(\theta)}\right)+\left(\frac{\pi R}{k_w \sin(\theta) Nu(\theta,Bi)}\right)\right)}\right]. \tag{A.6}$$

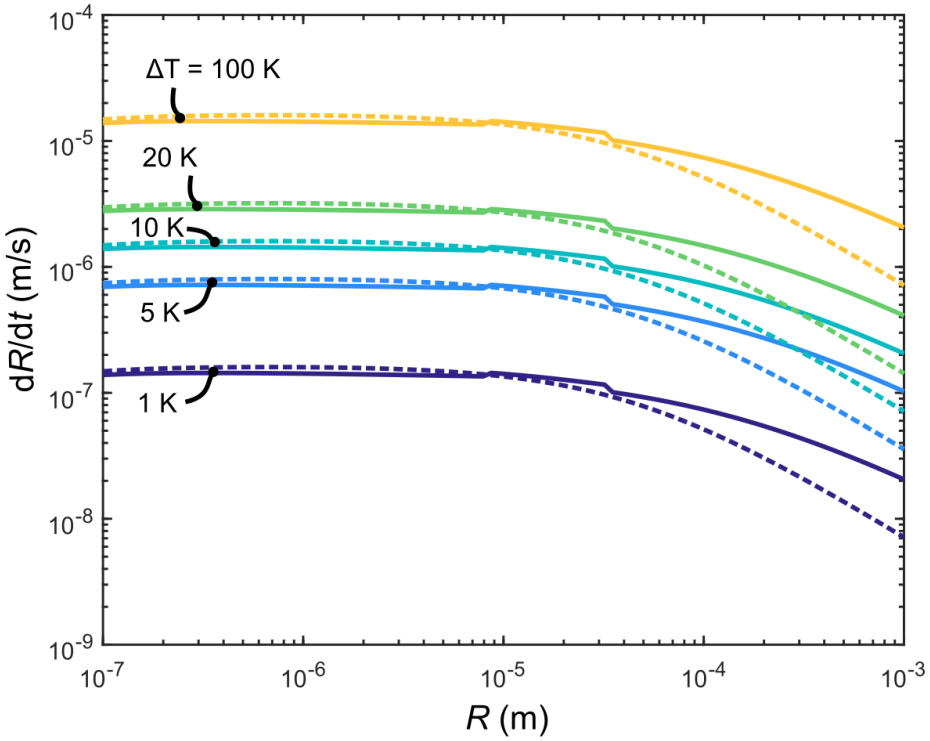


Figure A.2: Individual droplet growth rate $\left(\frac{\partial R}{\partial t}\right)$ as a function of droplet radius ($R$) for a variety of $\Delta T$. Solid and dashed lines are based on models from [198] and [199] respectively.

As the average radius of the droplets increases in Figure A.2, the droplet growth behavior becomes more like that predicted via the fundamental model by [84] for dropwise condensation. For smaller droplets and temperature differences, the droplet growth behavior is governed primarily by population theory for the stochastic formation of droplets [198, 199]. After comparing via scaling analysis the timescales of Figure A.2 with the timescales of Figure A.1, the droplet growth timescale ($\tau_g$) estimated for the relevant temperature differences common in electronics cooling applications (10 K $< \Delta T <$ 100 K) is the longest timescale by at least two orders of magnitude.

In fact, to the best of our knowledge, all previous studies have assumed the opposite (i.e. $\tau_g \gg \tau_c$ and $\tau_g \gg \tau_j$). It is worth noting that at high $\Delta T$, $\tau_t$ reduces and approaches $\tau_c$ or $\tau_j$. Since $\tau_t$ is a summation of all three timescales, both $\tau_t$ and $\tau_g$ approach $\tau_c$ or $\tau_j$ since $\tau_g \ll \tau_c$ or $\tau_g \ll \tau_j$. For this work, we maintain the distinction between $\tau_t$ and $\tau_g$ for clarity throughout the derivations.

## A.2 Derivation of Scaling for Heat Flux

First, heat flow can be related to the condensate mass flux and the latent heat of vaporization:

$$\dot{q} = \dot{m} h_{fg}. \tag{A.7}$$

Realizing that each droplet has mass, $m$, and the number of droplets that can jump per second is $N$, then the heat flow becomes:

$$\dot{q} = N m h_{fg}. \tag{A.8}$$

Next, droplet mass can be translated into droplet volume:

$$\dot{q} = N V \rho h_{fg}. \tag{A.9}$$

Substituting the volume of one droplet and the ratio of a total reference area, $A_r$, and the total number of droplet-producing unit cells for a specific time constant, $A_d \tau_t$, yields:

$$\dot{q} = \left(\frac{A_r}{A_d \tau_t}\right)\left(\frac{4\pi R^3}{3}\right)\rho h_{fg}. \tag{A.10}$$

The area of a unit cell for a droplet of radius, $R$, is $A_d = 4R^2$, hence:

$$\dot{q} = \left(\frac{A_r}{4R^2 \tau_t}\right)\left(\frac{4\pi R^3}{3}\right)\rho h_{fg}. \tag{A.11}$$

Dividing by the reference area yields a heat flux of:

$$q''_\tau = \left(\frac{1}{\tau_t}\right)\left(\frac{\pi R}{3}\right)\rho h_{fg}. \tag{A.12}$$

Thus, the condensation heat flux scales with:

$$q''_\tau \sim \left(\frac{\rho h_{fg}}{\tau_t}\right). \tag{A.13}$$

## A.3 Derivation of Scaling for the Maximum Hydrodynamic Limit Heat Flux

Assuming that all departing droplets are small enough such that the Reynolds number is low and the Stokes flow is present, the drag force can be simplified to:

$$F_D \approx 6\pi\mu_v R v_v. \tag{A.14}$$

Applying Newton's second law on the droplet:

$$F_D \approx m|a| \sim m\left(\frac{v_j}{\tau_j}\right). \tag{A.15}$$

Combining these insights via scaling analysis:

$$6\pi\mu_v R q'' \sim m\left(\frac{v_j}{\tau_j}\right), \tag{A.16}$$

and realizing that the vapor velocity is related to the heat flux yields:

$$\left(\frac{6\pi\mu_v R q''}{\rho h_{fg}}\right) \sim \left(\frac{4\pi R^3}{3}\right)\left(\frac{\rho v_j}{\tau_j}\right). \tag{A.17}$$

Substituting the coalescence timescale and simplifying this expression results in:

$$\left(\frac{R^2\rho\gamma}{\rho R^2}\right) \sim \left(\frac{\mu_v q''}{\rho_v h_{fg}}\right), \tag{A.18}$$

and reduces to:

$$\gamma \sim \left(\frac{\mu_v q''}{\rho_v h_{fg}}\right). \tag{A.19}$$

This yields the following relationship for the maximum hydrodynamic heat flux:

$$q''_h \sim \left(\frac{\rho_v h_{fg}\gamma}{\mu_v}\right). \tag{A.20}$$

Note, the aforementioned analysis assumes that the droplet departure velocity is negligible compared to the vapor velocity close to the limit. Indeed, further analysis in Section 8.3 reveals that at the limits, the vapor velocity approaches the sonic limit which makes our approximation accurate (i.e. $v_j \ll v_{sonic}$).

## A.4 Examining Different Working Fluids for Jumping Droplet Heat Transfer

While no experimental evidence for the jumping of gallium exists in the literature, likely due to the fact that the temperature requirements to achieve a sufficient vapor pressure for jumping to occur would require special visualization methods, significant experimental analysis of the thermophysical material properties of gallium have been reported. Jumping with Ga is possible by reducing the oxygen from the chamber in order to prevent the formation of oxide layers. To do this, a reducing environment such as $H_2$ gas would be used to remove the oxide prior to closing the vapor chamber and sealing it from any oxidizing environment.

## A.5 Investigating Interaction of Three Heat Flux Limits

For a subset of working fluids, Figures A.3 – A.8 explore how the overall critical heat flux for each liquid is governed by different timescales.

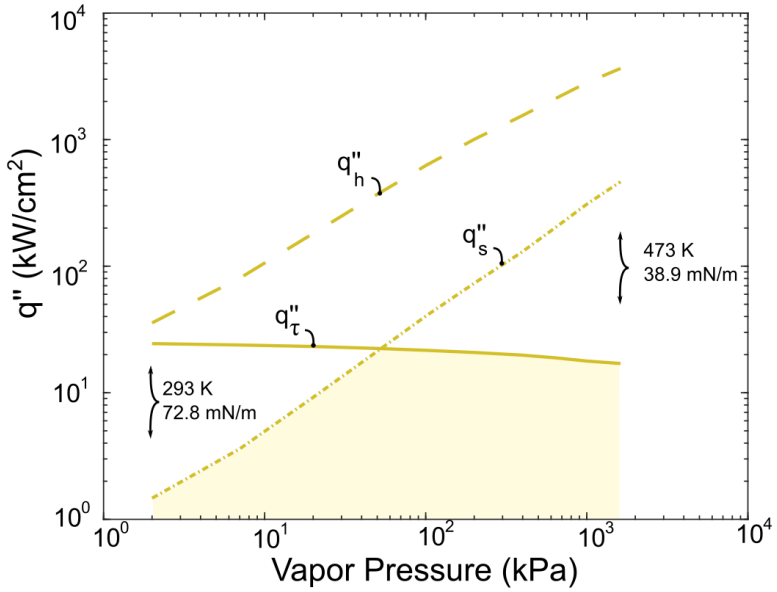


Figure A.3: Comparing all of the heat flux limits for water in order to identify the critical heat flux limit, $q''_{crit}$, and the region where droplet jumping heat transfer will exist. For water, $q''_{crit}$ is governed by the timescale, $q''_{\tau}$, and sonic, $q''_{s}$, limits.

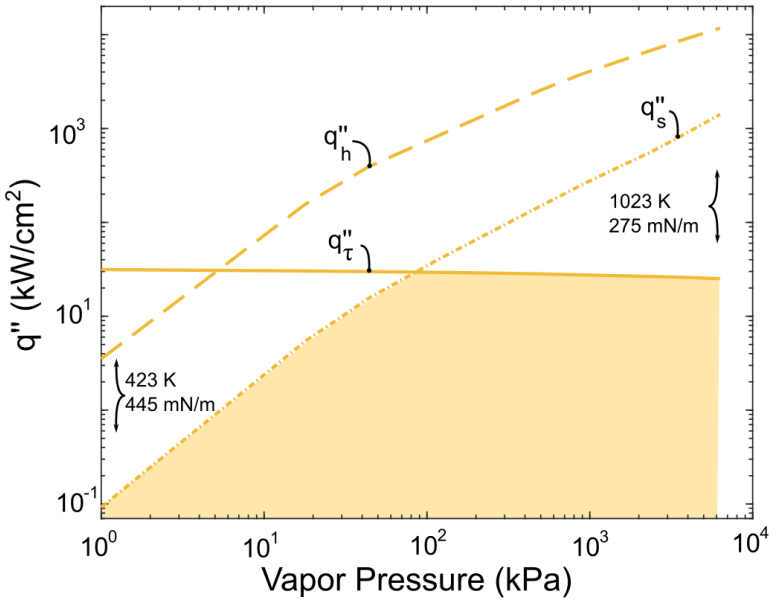


Figure A.4: Comparing all of the heat flux limits for Hg in order to identify the critical heat flux limit, $q''_{crit}$, and the region where droplet jumping heat transfer will exist. For Hg, $q''_{crit}$ is governed by the timescale, $q''_{\tau}$, and sonic, $q''_{s}$, limits.

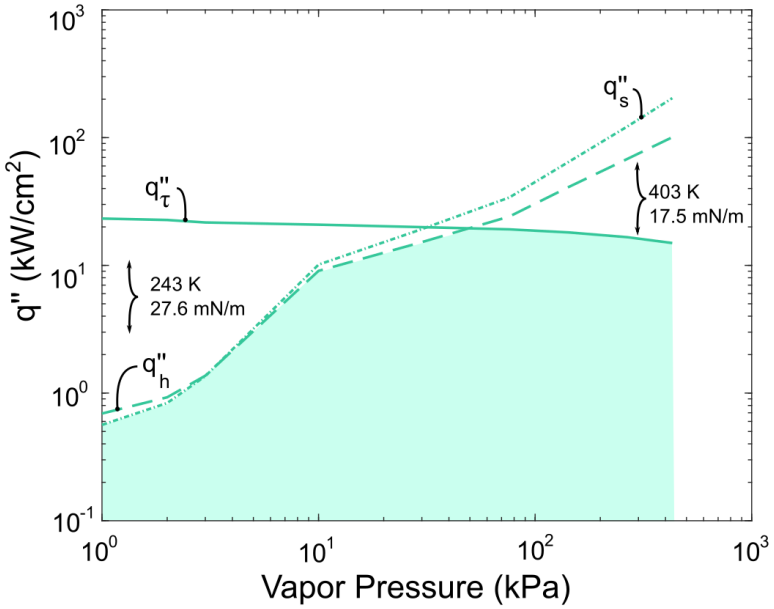


Figure A.5: Comparing all of the heat flux limits for ethanol in order to identify the critical heat flux limit, $q''_{crit}$, and the region where droplet jumping heat transfer will exist. For ethanol, $q''_{crit}$ is governed by all three timescales.

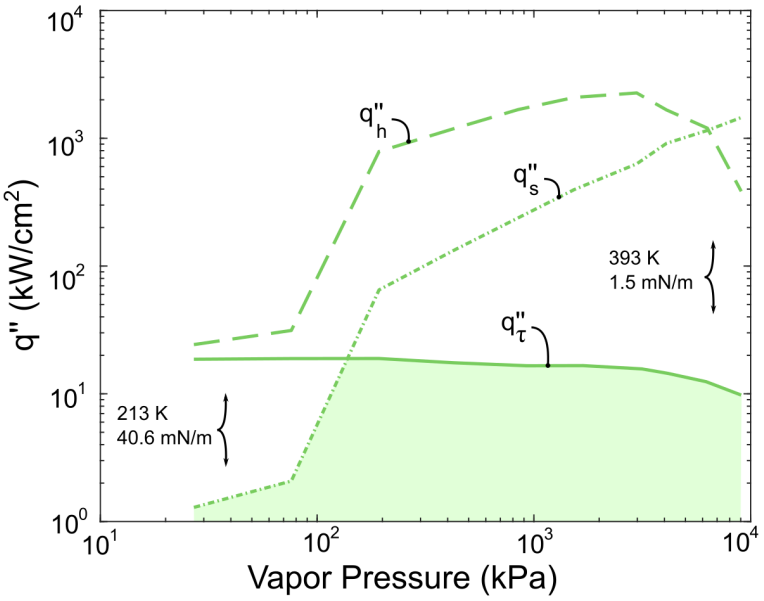


Figure A.6: Comparing all of the heat flux limits for ammonia in order to identify the critical heat flux limit, $q''_{crit}$, and the region where droplet jumping heat transfer will exist. For ammonia, $q''_{crit}$ is governed by the timescale, $q''_{\tau}$, and sonic, $q''_{s}$, limits.

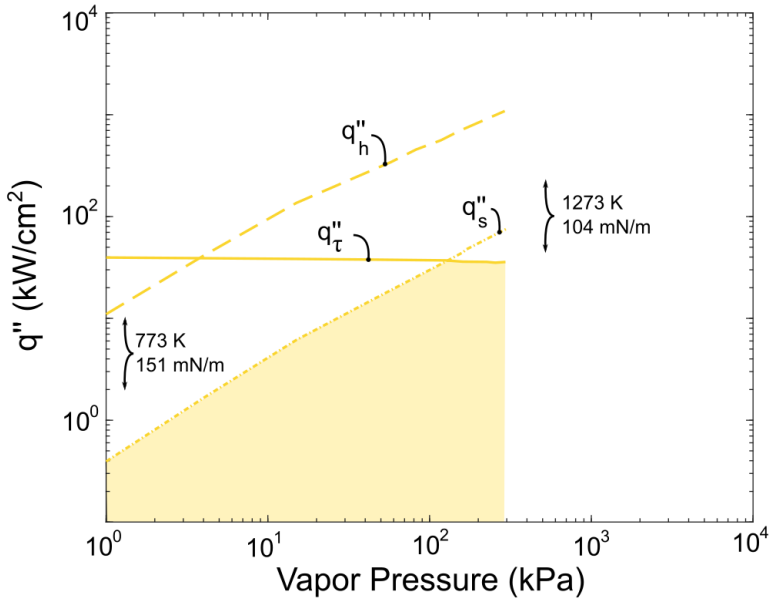


Figure A.7: Comparing all of the heat flux limits for Na in order to identify the critical heat flux limit, $q''_{crit}$, and the region where droplet jumping heat transfer will exist. For Na, $q''_{crit}$ is governed by the timescale, $q''_{\tau}$, and sonic, $q''_{s}$, limits.

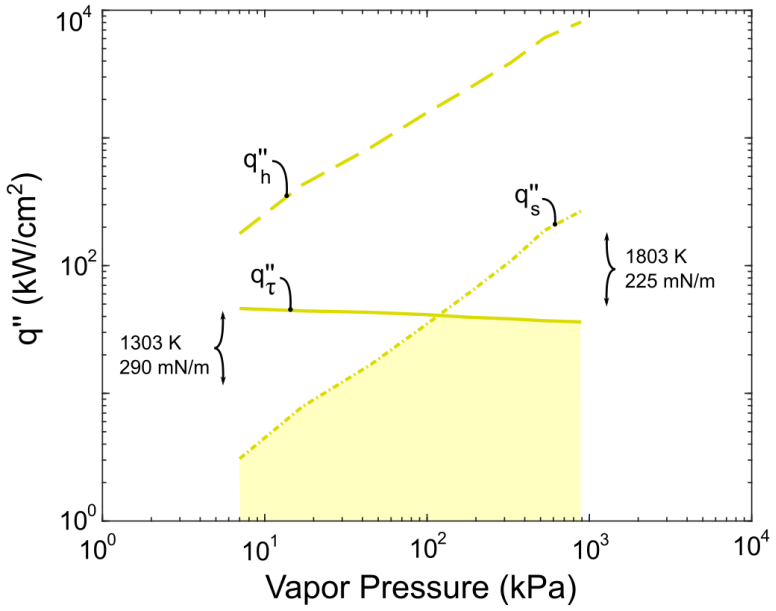


Figure A.8: Comparing all of the heat flux limits for Li in order to identify the critical heat flux limit, $q''_{crit}$, and the region where droplet jumping heat transfer will exist. For Li, $q''_{crit}$ is governed by the timescale, $q''_{\tau}$, and sonic, $q''_{s}$, limits.

# APPENDIX B

# NANOENGINEERED SURFACE FABRICATION AND VIDEOS OF JUMPING DROPLET ELECTRONICS COOLING

## B.1 Fabrication of Superhydrophobic Surfaces and Additional Details of Experiments

Figure B.1 demonstrates how the copper (Cu) cold plates are cleaned, structured, and functionalized in order to become superhydrophobic [191, 232]. Functionalized micro/nanostructured copper oxide (CuO), titanium dioxide ($TiO_2$), and boehmite (AlO(OH)) surfaces were fabricated from smooth Cu, Ti, and Al, respectively, as follows. We used commercially available 2 x 2 cm flat Cu-110 (Part no. 8963K402, McMaster), Ti-Grade 5 (Part no. 9039K15, McMaster) and Al-6061 (Part no 89015K151, McMaster) tabs as the base metal surfaces for our experiments. Each metal tab was initially cleaned by dipping for 10 min in acetone, ethanol, and

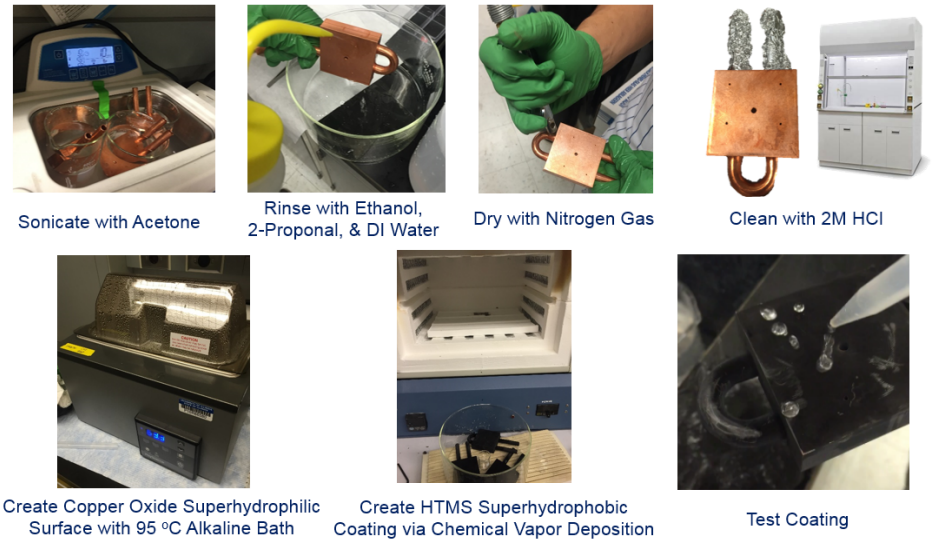


Figure B.1: Images showing the steps used for fabricating superhydrophobic structured surfaces used for jumping-droplet electronics cooling.

isopropanol, in succession, followed by rinsing with deionized (DI) water. The tabs were then dipped into a 2.0 M hydrochloric acid (Sigma-Aldrich) solution for 10 min to remove the native oxide layer on the surface, then rinsed multiple times with DI water and dried with clean nitrogen gas. Microstructured CuO and nanostructured $TiO_2$ surfaces were formed by immersing the cleaned Cu and Ti tabs into a hot (90 ± 3 °C) alkaline bath of $NaClO_2$, NaOH, $Na_3PO_4{\cdot}12H_2O$, and DI water (3.75:5:10:100 wt%) for 10 min. Nanostructured boehmite surfaces were formed by immersing the cleaned Al tabs into a boiling (≈100 ± 4 °C) DI water bath for 60 min. The structured CuO, $TiO_2$ and Al(O)OH surfaces were then functionalized by depositing heptadecafluorodecyltrimethoxy-silane (HTMS, CAS no. 1873-88-7, Sigma-Aldrich) by chemical vapor deposition. Briefly, samples were placed adjacent to a HTMS-toluene (CAS no. 108-88-3, Sigma-Aldrich) solution (5% v/v) in a sealed glass container inside an atmospheric pressure furnace (Blue M, Lindberg) at 80 °C for 3 hours. This process deposited a highly conformal low surface energy coating onto the samples, rendering them superhydrophobic. For the etched Al samples, a 2.5 cm sample was placed in HCl (5 M) for 15 min. The length scale of the microstructures was 50 microns. The sample was subsequently coated with HTMS using the previously described HTMS atmospheric-pressure CVD method.

Figures B.2 - B.4 provide additional information about the vacuum chamber testbed instrumentation, method for illuminating the samples, and

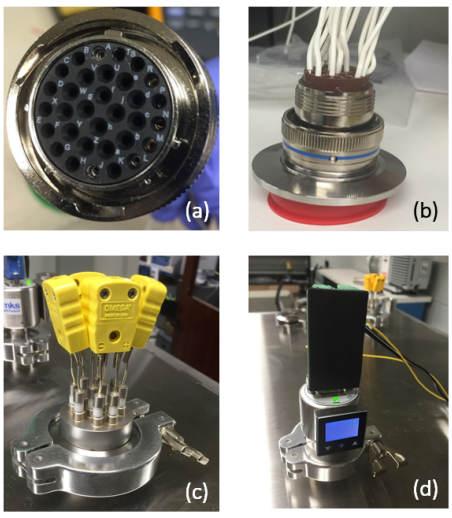


Figure B.2: Images of the vacuum chamber (a-b) electrical, (c) thermocouple, and (d) pressure sensor feedthroughs.

approach for capturing top-view images of the nanostructured surfaces.

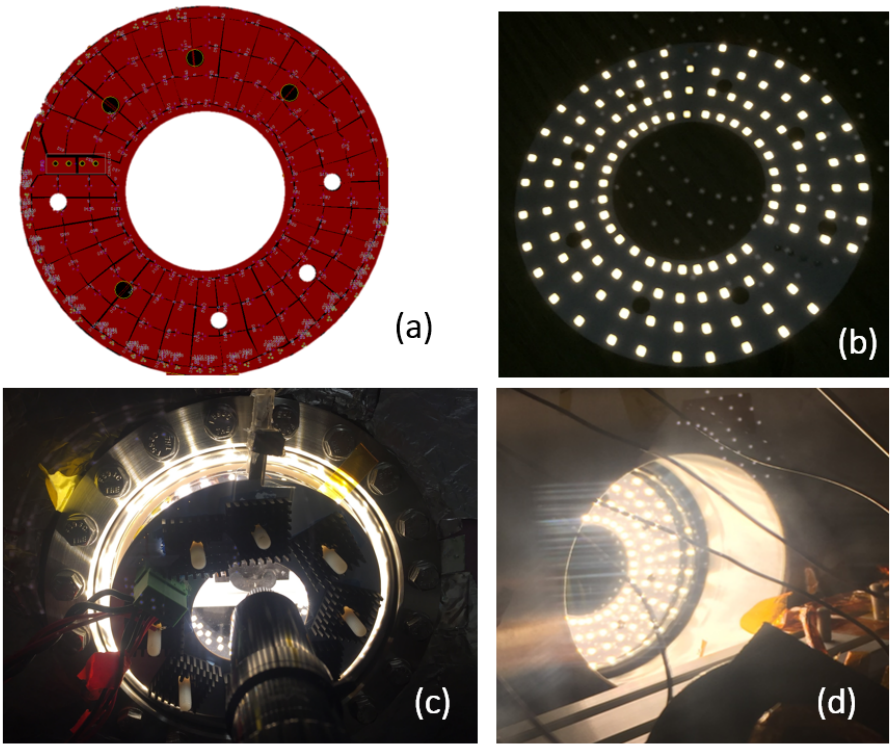


Figure B.3: A custom light source was (a) designed, (b) tested, and (c-d) integrated with the vacuum chamber experimental setup in order to provide an efficient ring light surrounding the high-speed camera as depicted in (c).

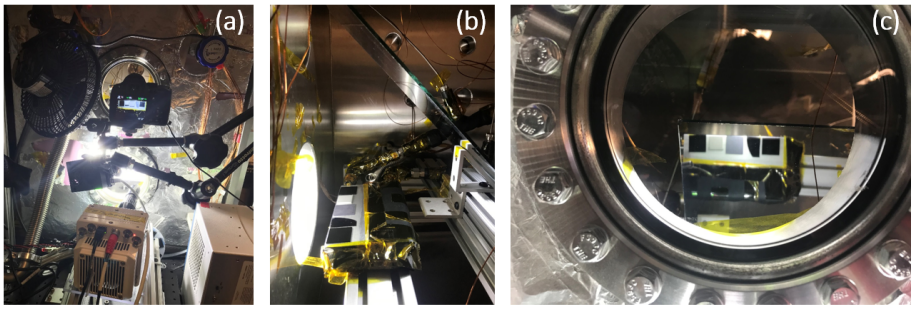


Figure B.4: (a) Image taken of the outside of the chamber showing the high-speed camera as it investigates jumping behavior for each sample with a simultaneous DSLR camera capturing the droplet density via a mirror. (b) Image of the experimental setup from inside the chamber looking from the side (door) with the mirror integrated for top-view imaging. (c) Image from the DSLR camera showing the top-view of the samples.

## B.2 High-Speed Videos of Jumping Droplet Behavior

All videos were captured using a Photron FASTCAM Mini AX200 camera coupled to an InfiniProbe TS-160 lens. The EPC 2034 GaN transistor has packaged dimensions of 4.6 mm x 2.6 mm x 0.51 mm (length x width x height not including solder bumps). All of the video pixel-to-mm conversions were determined using the 4.6 mm package length of the transistor as a calibrated reference in the Photron FASTCAM Viewer software using the Display Scale menu. Using the HandBrake open source video transcoder and the VLC open source media player, the videos were compressed and saved as .avi files.

**VideoS1AppB20fps.mp4** This video highlights the spatial control of jumping droplets using external electric fields. The video was captured at 900 frames per second (fps) and is played back at 30 fps. The size of the video is 655 x 452 pixels.

**VideoS2AppB20fps.mp4** This video highlights the electric field enhanced cooling of a GaN transistor. The video was captured at 900 frames per second (fps) and is played back at 30 fps. The size of the video is 1280 x 720 pixels.

## B.3 Measurement Uncertainty

Propagating uncertainty of all measurements based on standard definitions involves addition in quadrature where each term is the quotient of the device error and the measurement [137, 138]. For example, according to the manufacturer [141], a voltage measurement of 34 mV has both a range error (0.1% of 100 mV scale) and read error (0.2% of 34 mV) for a combined uncertainty of $\pm 168$ $\mu$V. Similarly, a 4.99 A current measurement [274] also has range and read errors combining to be $\pm 15$ mA. Thus, the resulting 169.7 mW power dissipation has a propagated uncertainty of $\pm 0.99$ mW. Given that the area used for calculating the heat flux has minimal uncertainty compared to the error of the power measurement based on scaling analysis, the resulting addition in quadrature is $\pm 20$ mW/cm$^2$.

# APPENDIX C

# SUPPLEMENTAL VIDEOS OF LIQUID BRIDGE CONFINED BOILING

All videos were captured using a Photron FASTCAM Mini AX200 camera coupled to an InfiniProbe TS-160 lens. Details regarding the fabrication of the superhydrophobic coating and the vacuum chamber at the heart of this experimental setup can be found in Section 10.2 of the main text. The EPC 2034 GaN transistor has packaged dimensions of 4.6 mm x 2.6 mm x 0.51 mm (length x width x height not including solder bumps). All of the video pixel-to-mm conversions were determined using the 4.6 mm package length of the transistor as a calibrated reference in the Photron FASTCAM Viewer software using the Display Scale menu. The size of all videos is 768 x 512 pixels, which at 0.0094 mm/pixel represents dimensions of 7.2 x 4.8 mm. Using the HandBrake open source video transcoder and the VLC open source media player, the videos were compressed and saved as .avi files.

**VideoS1AppC20fps.avi** This video highlights the process of self-assembling for the liquid bridge between the superhydrophobic coated cold plate and the gallium-nitride (GaN) transistor. The video was captured at 1000 frames per second (fps) and is played back at 20 fps. Before the self-assembled liquid bridge forms, a dc current of 5 A is flowing through the GaN transistor, which is a small heat flux of approximately 2.3 W/cm$^2$. Once the bridge forms, the dc current is immediately increased to 15 A (heat flux of approximately 14 W/cm$^2$).

**VideoS2AppC20fps.avi** This video demonstrates how quickly a liquid bridge can be reestablished after the bridge bursts due to bubble formation during the boiling process. The video was captured at 2000 fps and is played back at 20 fps. This is a moderate heat flux condition of approximately 16.6 W/cm$^2$ (dc current of 16 A).

**VideoS3AppC60fps.avi** This video highlights the temporary bridge reformation, or frog tongue behavior, that extends the lifetime of this cooling mechanism by resupplying subcooled liquid to the hotspot. This mode of bridge behavior exists in the second regime of bridge lifetime. The video was captured at 2000 fps and is played back at 60 fps. This is a moderate heat flux condition of approximately 16.6 W/cm$^2$ (dc current of 16 A).

**VideoS4AppC20fps.avi** This video demonstrates the first regime of liquid bridge behavior for moderate heat flux condition of approximately 14 W/cm$^2$ (dc current of 15 A). In this regime of bridge lifetime, complete detachment of the bridge does not last very long and only serves to scoop up more subcooled liquid to quench the hot GaN transistor once the bridge reforms. The video was captured at 1000 fps and is played back at 20 fps.

**VideoS5AppC20fps.avi** This video underscores the temporary bridge reformation, or frog tongue behavior, that extends the lifetime of this cooling mechanism at high heat flux condition of approximately 60 W/cm$^2$ (dc current of 30 A) by resupplying subcooled liquid to the hotspot. This mode of bridge behavior exists in the second regime of bridge lifetime. The video was captured at 1000 fps and is played back at 20 fps.

**VideoS6AppC20fps.avi** This video captures the vigorous boiling that exists at high heat flux for the liquid bridge for the first regime of bridge lifetime. Eventually, the violent bubble formation causes the bridge to burst and subcooled liquid to be collected into the reformed bridge. In this regime of bridge lifetime, complete detachment of the bridge does not last very long. The test conditions are for a high heat flux condition of approximately 60 W/cm$^2$ (dc current of 30 A). The video was captured at 1000 fps and is played back at 20 fps.

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