INALN/GAN HIGH ELECTRON MOBILITY TRANSISTORS FOR VENUS SURFACE EXPLORATION

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DOCTOR OF PHILOSOPHY

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Abstract

Historical and proposed missions to the surface of Venus have been severely limited in both scope and duration by the lack of robust microelectronics that can operate within Venus' extreme environment. Traditional silicon technology cannot survive on Venus without the use of expensive and bulky active cooling measures due to the scalding surface temperature of ≈465°C. To address this technological gap and enable extended duration robotic surface exploration on Venus, I propose the use of wide-bandgap gallium nitride (GaN) technology for uncooled microelectronics (e.g., sensors, micromechanical resonators, transistors).

In this thesis, I present original research on the design and microfabrication of InAlN/GaN high electron mobility transistors (HEMTs), which leverage a two-dimensional electron gas (2DEG) conducting channel and can provide sensing, power, and telecommunications for a Venus lander or rover. I explore the use of several Schottky gate electrode materials that are attractive candidates for reliable high-temperature operation. The experimental results from electrically characterizing HEMTs utilizing these gate materials up to 600°C in air for durations of up to 6 days are presented. I then analyze Schottky barrier properties and make recommendations for engineering superior Schottky contacts. The electrical operation of HEMTs exposed to simulated Venus surface conditions (465°C, >90 bar, supercritical CO_2 ambient) for up to 10 days is presented. Finally, I present the first every demonstration of an uncooled GaN device successfully operating *in situ* simulated Venus surface conditions. The *in situ* experiment concluded after 5 days and 21 hours of device operation, which is a 70-fold greater duration than the ≈2 hour record operating length of silicon-based microelectronics used on the Venera 13 mission. As a whole, these contributing proof-of-concept experiments support the use of the InAlN/GaN HEMT platform and provide a road map for further maturing this technology for uncooled microelectronics.

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Ph.D. years were not only professionally fulfilling, but also encompass huge personal milestones we've marked together like getting married and having our son. Thank you for being a true partner while we continue to build our wonderful life with Rhone, Casper, and Beanie. I love you. And finally, to my son, Rhone, who was in utero when I defended and has been patiently sitting in his bouncer while I finish writing this thesis: thank you for simply existing. You were the motivation I needed to kickstart into high gear and see this degree through to the very end. You're an accomplishment that can't be topped; everything else is just a bonus.

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Chapter 1

Introduction

1.1 Planetary Science Objectives for Venus Surface Exploration

Venus is often referred to as Earth's twin or "sister planet" because of their similar size, mass, and composition. The scientific reasons to explore Venus are compelling; despite its location in the same part of the solar system and similar attributes to neighboring Earth, the two planets are starkly different. NASA has outlined several key planetary science objectives for future Venus surface missions including detailing the mineralogy, observing the seismology and metrology, and understanding chemical interactions between the atmosphere and the surface [12]. Long term missions beyond 2 Earth months to the surface of Venus are needed to make seismic observations and characterize atmosphere-surface chemistry over an extended duration. This data can illuminate the origin and diversity of terrestrial bodies, such as how Venus and Earth diverged in climate and geology. There are outstanding questions regarding the evolution of Venus, such as the extent and disappearance of ancient oceans it is believed to have hosted. Venus, which sits within the habitable zone, may have been the solar system's first hospitable planet, despite the smoldering inhospitable conditions in the present day. Deepening our understanding of Venus can help identity the factors that determine the origin and evolution of life on Earth. Further Venus study can help answer pressing questions regarding whether life evolved during the habitable period and how long the habitability period lasted [13]. We could learn how habitability can be lost on a planetary scale. Moreover, a surface study of the runaway greenhouse gas effect on

Venus can increase our understanding of the processes that control climate change on Earth-like planets [14–16]. Yet the mission funding necessary to facilitate detailed study of Venus has been extremely limited in favor of funding exploration of higher priority destinations like Mars. The reasons why Venus exploration has long been neglected by funding agencies will be discussed in subsequent sections.

1.2 Surface Mission Concepts and Target Durations

Target operational durations for conceptual Venus surface missions developed by NASA vary in ambition. NASA's Long Lived In-situ Solar System Explorer (LLISSE) project aims to develop a small Venus lander with an operational target of 60 Earth days, which is approximately one Venus "daylight period" and day/night transition [17, 18]. This would allow observation of processes on Venus that are dynamic with time of day and solar lighting conditions, such as the temperature profile, wind structure, and cloud formation and dissipation processes [15]. The Venus Flagship mission study, which encompasses a variety of designs including an aerobot, lander, orbiter, and SmallSat, is estimated to cost $3.7 billion and targets a mere 8 hours of surface science study from the lander [12]. The Venus Intrepid Tessera Lander (VITaL) concept to safely land in one of Venus' mountainous tessera regions aims to characterize chemistry and mineralogy, place constraints on the size and temporal extent of a possible ocean that may have existed on Venus, and characterize the morphology of surface units [19]. The total mission time of VITaL is 3 hours, including 2 in the surface environment. The thermal design relies on a phase change material, Lithium nitrate trihydrate (LNT), to provide cooling of the electronic decks for 2 hours. Perhaps most ambitious of all, a concept for a Venus sample return mission was previously considered in depth by NASA/JPL [20]. The idea was to use parachutes to drop small samplers on the surface. Once the soil or rock was collected, the samplers would be ballooned up to several small UAVs and transferred to a rocket. That mission concept was ultimately rejected due to significant probability of failure at several critical junctures, among them the thermal exposure of instrumentation during sample drilling [21]. The scope of these mission concepts is limited by the short durations necessitated by technical hurdles discussed later in this chapter. Increased mission operational times on the scale of weeks or months could offer significant advancements in the scientific knowledge of Venus, particularly by enabling remote control of the lander or rover. This would allow for human-in-the-loop decision

making in regards to where to drill or image for detailed sample analysis [22].

1.3 Previous Venus Surface Missions

A comprehensive timeline of previous missions to the surface of Venus is shown in Figure 1.1 [23]. In 1970, the Soviet Union's Venera 7 became the first spacecraft to ever land on another planet. It transmitted data from the surface of Venus for just 23 minutes. Two additional Soviet Venera missions reached the surface in 1972 and 1975, respectively. Venera 9 marked the first image ever taken of the surface of another planet. In 1978 both the Soviet Union and NASA sent missions to Venus, which transmitted data for 1 to 2 hours. In 1981, Venera 13 and 14 reached the surface. Microphones on the Venera 13 probe made the first recording of sound on another planet in an attempt to measure wind speed. Venera 13 transmitted data for 127 minutes. And finally, in 1985, the Vega missions reached Venus. This is the final chapter in the program of Russian exploration of Venus, which discovered most of what is known today about our neighboring planet. There has not been a Venus surface exploration mission in 37 years. Since that time, the additional information learned about Venus has come from orbiting spacecraft and satellites, which can have difficulty penetrating Venus' thick cloud cover and cannot address many of the lingering scientific questions about Venus.

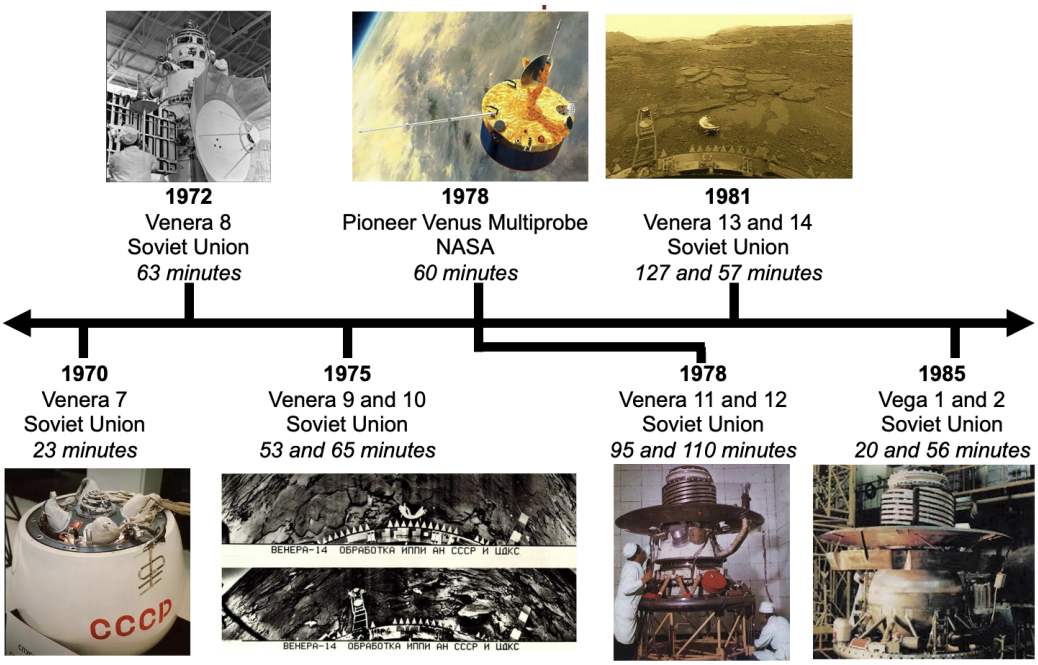

Figure 1.1: Timeline of previous Venus surface missions.

1.4 Venus' Extreme Environment

As discussed in the previous section, Venera 13 set the record for the longest operational lifetime of a Venus surface mission at 127 minutes, or just over 2 hours. Venera 13's lifetime is orders of magnitude shorter than the record length lifetime of a Mars surface mission, which is 14 years and 138 days set by NASA's Opportunity rover from 2004-2018. This disparity in operable mission lifetimes between Venus and Mars reflects the technical challenge of operating microelectronics within the extreme environment on the Venusian surface.

The surface temperature on Venus is a scalding 464°C and atmospheric pressure is 92 bars, equivalent to the pressure at a depth of 1 km in Earth's oceans [24]. The chemical composition of Venus' atmospheric is caustic and corrosive. The atmosphere is composed primarily of carbon dioxide (CO_2) rendered into a supercritical fluid, sCO_2, under the temperature and pressure conditions. Table 1.1 lists the first nine gas substituents on the Venusian surface and their percentage in the lower atmosphere determined by NASA [1]. SO_2, HCl, and HF are highly corrosive and toxic to humans at low ppm levels.

Due to these environmental conditions, it's a lot easier to study and explore Mars, where

Constituent	% in the lower atmosphere
CO_2	96.5
N_2	3.5
H_2O	0.003
SO_2	0.018
CO	0.0012
OCS	0.0051
H_2S	0.0002
HCl	5×10^{-5}
HF	2.5×10^{-7}

Table 1.1: The lower atmospheric gas composition on Venus [1].

the environment is far less hostile, than Venus, where the temperature can melt lead. This means the cost and technical risk for Venus missions is substantially higher for similar gains in planetary science knowledge. This is a large consideration during mission selection given that NASA has limited funding. The environmental conditions on Venus put it at a further disadvantage to receive funding because the habitability of present-day Venus is not up for dispute, and NASA's agenda has historically prioritized missions that directly relate to the search for extraterrestrial life. Humans will likely walk on Mars in the near future, which has garnered a level of public support that Venus has not. However, the increased knowledge of potentially habitable exo-worlds that could be gained by Venus exploration discussed earlier in this chapter should not be overlooked.

1.5 Technology Gap: Silicon Microelectronics

Among Venus' extreme environmental conditions, the high surface temperature poses the greatest obstacle to instrumentation. Despite the use of active and passive cooling measures, data transmission from Venera 13 to the orbiting satellite ceased after 2 hours due to failure of the silicon microelectronics [25]. The longevity and scope of proposed future missions to the surface of Venus are currently limited by the challenge of developing viable electronics. NASA has noted that the development of high-temperature electronics is key to enabling future Venus exploration for the long duration targets ($\geq$60 Earth days) [26]. The types of Venus surface instrumentation which require semiconductor microelectronic devices include mass and laser spectrometer control and read-out electronics, low-power sample handling processors to command a drill, and power system electronics to control switching and power

distribution [12].

Traditional microelectronics cannot operate at extreme high temperatures because they are based on silicon (Si) semiconductor technology like was used onboard Venera 13. Silicon transistors are the building blocks of all modern-day electronics. Despite continued rapid progress in enhancing silicon integrated circuit performance over the past few decades by scaling transistor size and increasing density, the hurdle of operating silicon microelectronics in high temperature environments remains due to band-gap and doping limitations. The operational temperature range of silicon transistors, even with special design considerations such as silicon-on-insulator (SOI) technology, is limited to about 350°C, well below Venus surface temperatures (Figure 1.2). At high temperatures, intrinsic carriers in a semiconductor (electrons and holes that contribute to conduction) are thermally activated into the conduction band and contribute to the current. In silicon, the intrinsic carrier concentration nears and then exceeds the doping concentration at extreme high temperatures, at which point the conduction can no longer be modulated and the device is not operational. Figure 1.3 shows intrinsic and extrinsic (doped) carrier concentrations as a function of temperature in several semiconductors [2].

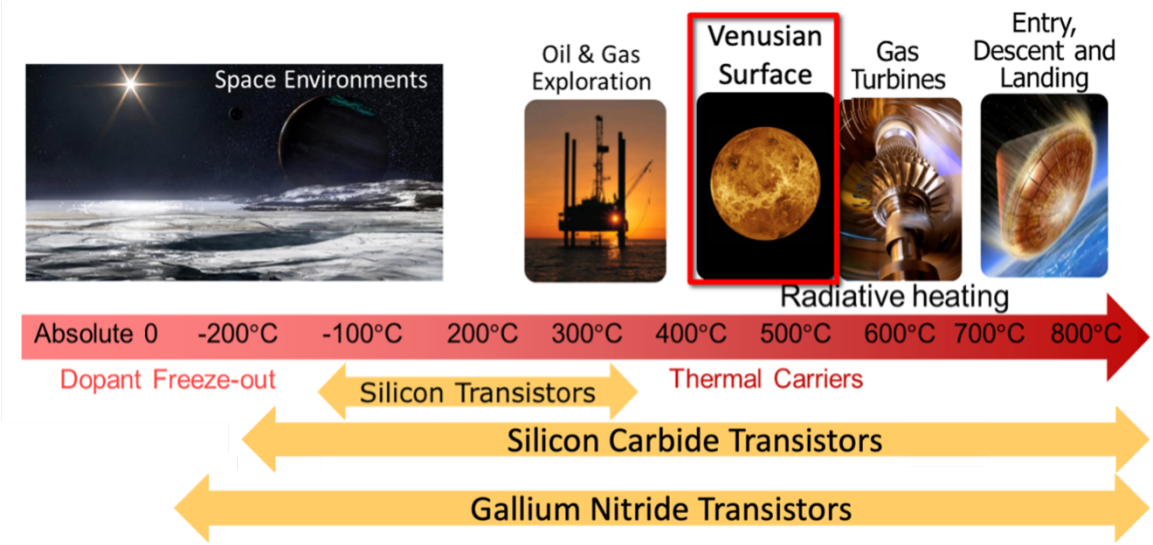

Figure 1.2: Extreme environment applications for microelectronic devices and the demonstrated operating range of silicon, silicon carbide, and galliun nitride transistors.

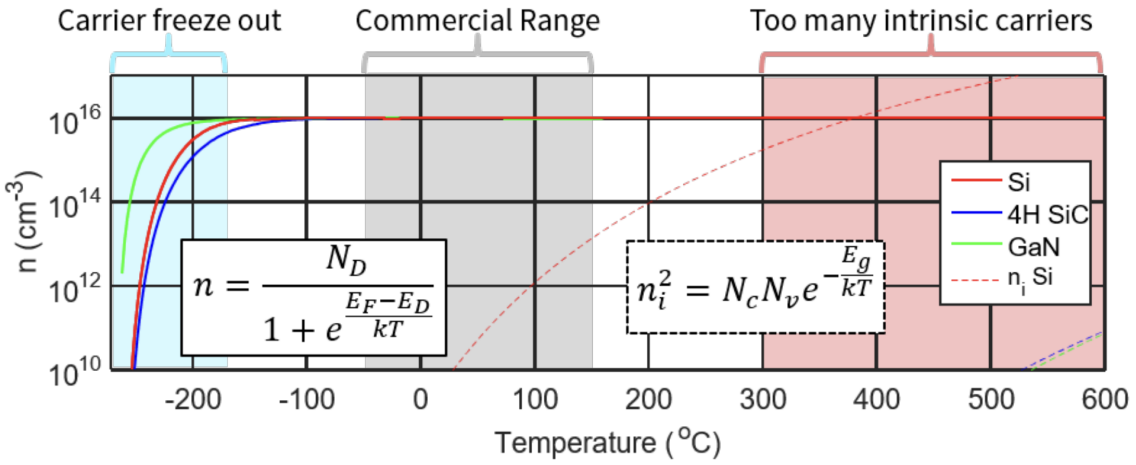

Figure 1.3: "Behavior of carriers in 1×10^{16} cm^{-3} doped silicon and wide bandgap materials varied with temperature" by Karen M. Dowling, retrieved from "Offset and Noise Behavior of Microfabricated Aluminum Gallium Nitride-Gallium Nitride Two-Dimensional Electron Gas Hall-effect Sensors" used under Attribution-NonCommercial 3.0 United States (CC BY-NC 3.0 US) [2]. Solid lines represent the n-type carrier concentration, n, while dashed lines represent the intrinsic carrier concentrations, n_i.

1.6 Potential Solution: Wide-Bandgap Semiconductors

Wide-bandgap (WBG) semiconductors such as silicon carbide (SiC) and gallium nitride (GaN) have recently emerged as promising material platforms for uncooled extreme environment electronics due to their stability at high temperatures, inherent radiation tolerance, and chemical resistance [27–29]. A comparison of key electrical properties in Si, SiC, and GaN are shown in Table 1.2. The intrinsic carrier concentrations in SiC and GaN are much lower than in Si due to their 3× wider bandgaps. These WBG materials do not suffer from the excessive carrier concentration issues experienced by Si at high temperature.

Property	**Si**	**SiC**	**GaN**
Energy Bandgap (eV) [30]	1.1	3.3	3.4
Intrinsic carrier concentration at 300°C [27]	1×10^{15}	1×10^{7}	1×10^{5}
Electron Mobility (cm^2/V-s) [30, 31]	1350	950	2150[1]
Highest Temperature of Operation (°C) [32–34]	350[2]	600	1000

Table 1.2: Electrical Properties of Si, SiC, and GaN.

[1] In 2DEG
[2] SOI

Silicon Carbide

SiC microelectronics have been pursued and matured for Venus surface exploration applications by researchers at NASA [35, 36]. In the most rigorous experiment demonstrating the viable operation of SiC microelectronics for Venus surface exploration to date, Neudeck *et al.* demonstrated the stable operation of SiC junction field effect transistor (JFET) integrated circuits under Venus surface atmospheric conditions for 60 days [36]. The devices were directly exposed (e.g. no packaging or cooling) inside the NASA Glenn Extreme Environment Rig (GEER) and tested *in situ* over the duration. The ICs experienced a small increase in frequency, primarily over the first 20 days of exposure, which the authors attributed to burn-in. This demonstration indicates SiC microelectronics could be a potential solution to long-lived Venus surface missions.

Gallium Nitride

While SiC and GaN are both competitive for high-temperature operation, the GaN material platform offers several advantages. First, GaN heterostructures have the unique ability to form a conducting channel called the two-dimensional electron gas (2DEG) without the use of doping like is necessary in Si and SiC. Unlike doped junctions, the 2DEG channel is unaffected by adverse dopant scattering and diffusion effects at elevated temperatures. Second, GaN heterostrucutres can achieve very high electron mobilities over 2× greater than in SiC, meaning that GaN can offer enhanced device performance for high frequency applications such as communications and timing (Table 1.2). Third, GaN devices have higher power efficiency than SiC devices due to lower conduction loses, which are highly dependent on the on-state resistance. This is advantageous for power-constrained applications, such as a Venus surface lander.

Previous studies on the high-temperature operation of GaN heterostructure devices in inert and air ambient are promising [4,6,7,34,37–41]. InAlN/GaN heterostructure high electron mobility transistors (HEMTs) have been reported to operate for 25 hours at 1000°C in vacuum [34]. Even with these recent breakthroughs, there have been no reported studies on the effects of exposure to a Venus surface environment on GaN microelectronics, or comparable assessments of GaN electronics operating wihtin Venus surface atmospheric conditions such as those reported for SiC. This can be attributed to the relative immaturity of GaN technology compared to SiC technology, which in turn led to NASA's dedication to advancing the development, complexity, and capabilities of SiC microelectronics for Venus

surface exploration. NASA has launched the High Operating Temperature Technology (HOTTech) program to support the development and maturation of other critical technologies for high temperature electronics that significantly enhance space exploration and discoveries to high-temperature, harsh environments like on Venus. Here, I present compelling proof-of-concept research towards maturing GaN microelectronics for Venus surface exploration that has been funded in part by the HOTTech program.

1.7 Thesis Overview

This thesis presents original research investigating the viability of InAlN/GaN HEMTs for Venus surface exploration applications. The case for future missions to Venus and the need for uncooled microelectronics that motivate this thesis work is covered in Chapter 1. The necessary background on the InAlN/GaN heterostructure, high electron mobility transistor operation and architecture, and relevant degradation mechanisms that present challenges to reliable high temperature device operation are presented in Chapter 2. In Chapter 3, the microfabrication process and metallization and passivation material choices and geometry schemes chosen during the design phase are covered. Chapter 4 and 5 present compelling proof-of-concept demonstrations of uncooled GaN heterostructure devices with various metallization and passivation schemes operating *in situ* hot air ambient and simulated Venus surface conditions for extended durations. Potential degradation mechanisms and their impact on electrical characteristics are discussed. For the first time, a GaN heterostructure device is demonstrated successfully operating under simulated Venus surface conditions in the form of an InAlN/GaN C-HEMT. The experiment concluded after 5 days and 21 hours. This work represents a 70× improvement in operating length over traditional Si microelectronics that lasted just over 2 hours on Venus' surface and required bulky active cooling. The results support the further maturation of this device and technology platform to provide a new uncooled microelectronics solution not only for space applications, but for other high temperature oxidizing and corrosive ambient applications including: down-hole oil and gas, CO_2 sequestration, and structural health monitoring for aircraft engines.

Chapter 2

Background

2.1 GaN Heterostructures

GaN is binary III-V WBG semicondcutor. GaN has a hexagonal wurtzite crystal structure. When the crystal lattice is grown in the [0001] direction, the surface is terminated in Ga atoms, which is known as Ga-polar. Figure 2.1 shows the crystal lattice with Ga-polartiy.

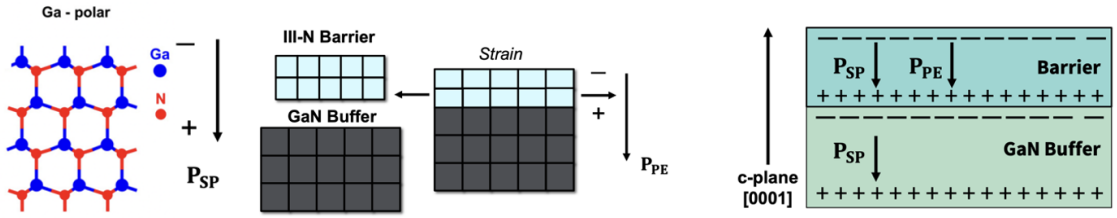

Figure 2.1: Spontaneous (left) and piezoelectric (middle) polarization illustrations. Polarization direction and charge accumulation depicted in a cross-sectional schematic of the GaN heterostructure (right).

Gallium Nitride heterostructures are formed by the epitaxial growth of a thin film of a III-N ternary alloy, such as Indium Aluminum Nitride (InAlN) or Aluminum Gallium Nitride (AlGaN) on top of bulk GaN. The III-N layer on top is referred to as the barrier layer and the underlaying GaN is the buffer layer. The GaN heterostructure can experience two forms of polarization. The first is spontaneous polarization, which is inherent in the GaN heterostructure even with zero strain in the system. Figure 2.1 depicts spontaneous polarization, P_{SP}. Because the wurtzite crystal lattice has intrinsic asymmetry due to the

differing electronegativities of the atoms, a dipole is formed by the Ga-N bond. The dipole segregation of the positive and negative charge concentrations in the unit cell causes the axis of the unit cell to extend in the c-plane direction and a spontaneous strain is present. Thus spontaneous polarization exists in the growth direction, which is the c-plane [0001]. On the macroscopic scale, these dipoles should cancel each other out. But in wurtzite GaN, the bonds along the c-axis are not the same length as the bonds perpendicular to the c-axis so the cancellation is not complete; thus, a net dipole exists along the c-axis.

The second form of polarization found in GaN heterostructures is piezoelectric polarization due to mechanical stress from lattice mismatch between the III-N barrier layer and the GaN buffer layer. Figure 2.1 shows spontaneous polarization, P_{PE}. Lattice mismatch refers to differing lattice constants, the distance between unit cells in a crystal lattice. The mechanical stress results in charge accumulation in the lattice. In the case of the frequently used barrier layer AlGaN, the strain in the system is usually tensile and the piezoelectric polarization P_{PE} is parallel to the spontaneous polarization, P_{SP}. The total polarization in the heterostructure is the combined spontaneous and piezoelectric polarization fields,

$$P_{TOTAL} = P_{SP} + P_{PE} \tag{2.1}$$

Figure 2.1 has a schematic of these polarization components and charge accumulation in the heterostructure.

2.2 InAlN/GaN versus AlGaN/GaN

The most common barrier layer used in GaN heterostructure devices is AlGaN, which exhibits both spontaneous and piezoelectric polarization on GaN. With Al-incorporation around 30%, spontaneous and piezoelectric polarization are about equal in the stack. However, the reliability of AlGaN/GaN devices at high-temperatures may be compromised by the stress resulting from the piezoelectric effect causing lattice defects [42]. By changing the barrier layer to Indium Aluminum Nitride, or InAlN, the reliability and performance of GaN heterostructure devices at high temperature may be enhanced. The InAlN barrier can be grown to be lattice-matched to the underlying GaN layer by achieving 17-18% In-incorporation [43]. With this composition of the barrier layer, tensile strain and piezoelectric polarization are not present in the heterostructure. This is particularly important at high temperature where strain relaxation has been reported in AlGaN/GaN to degrade

device performance due to the dependence of the 2DEG properties on piezoelectric polarization [44]. Strain effects in the system can become more prevalent at high temperatures and cause reliability issues, so the lattice-matched structure of InAlN is thought to provide higher reliability for ultra high temperature environments due to the absence of piezoelectric strain. Furthermore, the spontaneous polarization in the InAlN/GaN heterostructure is larger than in AlGaN/GaN heterostructure, contributing to significantly higher 2DEG density [45]. The high carrier density in InAlN/GaN HEMTs makes this platform attractive for strain and pressure sensing applications.

2.3 The Two-Dimensional Electron Gas

Due to the polarization effects described above, a two-dimensional electron gas, or 2DEG, will be induced to form at the barrier layer-GaN interface in these heterostructures. The location of the 2DEG is depicted in Figure 2.2. The 2DEG is a quantum well of electrons, essentially a thin highly conductive sheet. The electrons in the 2DEG are commonly accepted to originate from surface states that act as donors. These donor-like surface states are electronic traps that exist due to dangling bonds or other defects present at the barrier layer surface from the crystal lattice termination. Due to polarization-induced electric fields, there is a drop in potential along the InAlN conduction band. The discontinuity of the conduction band, ΔE_C, is due to differences in the conduction band potentials between InAlN and GaN. This results in the conduction band dipping below the Fermi level, creating the 2DEG quantum well. Figure 2.2 depicts the energy band diagram.

The density of electrons in the 2DEG is influenced by the thickness of the barrier layer [43]. In the case of AlGaN, the barrier layer thickness should be around 25 nm to ensure the full 2DEG density, whereas InAlN barrier layers can be scaled down to approximately 8 nm before 2DEG depletion occurs. This is attributed to pinned surface potential of 1.5 eV in AlGaN and only 0.4 eV in InAlN [43]. Thinning of the barrier layer while keeping high sheet carrier density is desirable because it can increase gate modulation control by reducing the gate to channel distance (e.g increase transconductance) [46]. Hence, this is another advantage of the InAlN barrier.

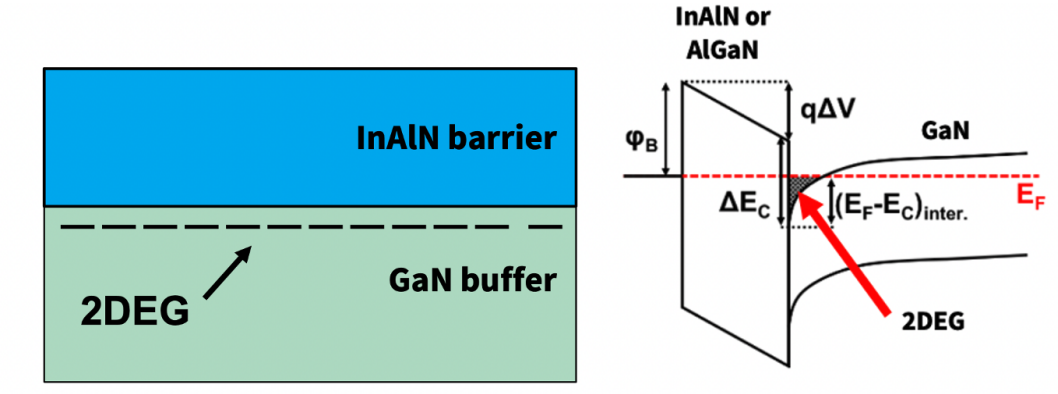

Figure 2.2: Simplified cross-sectional InAlN/GaN heterostructure showing the location of the 2DEG (left). Energy band diagram of a GaN heterostructure (right), adapted from Caitlin A. Chapin, retrieved from "High Temperature and Transient Behavior of GaN Heterostructure Based High Electron Mobility Micro-Pressure Sensors" used under Attribution-NonCommercial 3.0 United States (CC BY-NC 3.0 US) [3].

2.4 Advantages of the 2DEG at High Temperature

The GaN heterostructure is advantageous for high temperature applications because the 2DEG channel is unintentionally doped. This mitigates the deleterious adverse dopant scattering and diffusion effects experienced in the doped junctions necessary in Si and SiC. The 2DEG properties of InAlN/GaN heterostructures at high temperature in air have been experimentally measured using Hall-effect sensors. Figure 2.3 shows the electron sheet density, n_s, is stable up to temperatures as high as 576°C [4]. The 2DEG mobility, μ, follows a power law close to the -1.5 predicted by phonon scattering, which has been shown to be the limiting mechanism in InAlN/AlN/GaN at room temperature [47, 48]. The mobility is not limited by ionized impurity scattering, which determines charge transport in doped junction semiconductors [49].

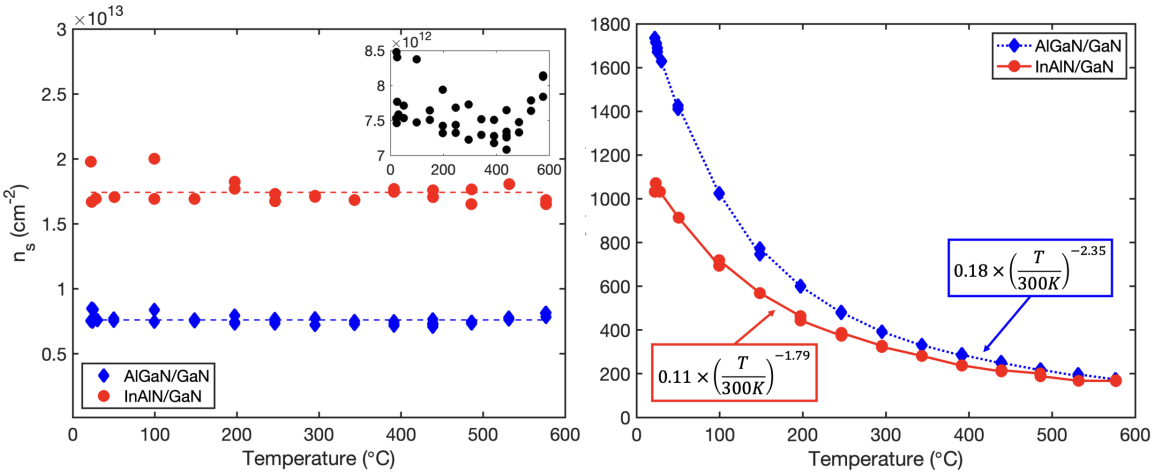

Figure 2.3: InAlN/GaN and AlGaN/GaN heterostructure sheet carrier density (left) and mobility (right) up to 576°C. Reprinted with permission from AIP Publishing [4].

2.5 Uncooled Monolithic Integration

InAlN/GaN HEMTs are further attractive for high-temperature operation because they offer the potential for monolithic integration. Future spacecraft landed on the surface of Venus will require a full suite of uncooled microelectronics for sensing parameters such as temperature, pressure, chemistry, radiation, and seismic activity, as well as transistors, passive components, and resonators providing the sensor readout circuitry and telecommunications with the orbiting satellite. Additionally, power microelectronics are necessary to control the power systems. Monolithic integration enhances the highest performance-to-cost ratio by increasing chip functionality at lower fabrication costs. Additionally, a monolithically integrated InAlN/GaN-on-Si chip can reduce the total footprint of the on-board microelectronics, which can help lower the mission size, weight, and costs or expand the mission scope by allowing space for additional instrumentation.

Several low-power lateral GaN heterostructure devices have been investigated for harsh environment operation at Stanford, including HEMTs, UV photodetectors, Hall-effect magnetic field sensors, and MEMS resonators [11,50] . The InAlN/GaN HEMT microfabrication process described in Chapter 3 allows for co-fabrication of many of these sensors and circuitry on one monolithically integrated circuit on a single die or chip. Figure 2.4 shows a concept for a monolithically integrated InAlN/GaN-on-Si chip.

The envisioned monolithically integrated chip would be capable of withstanding the

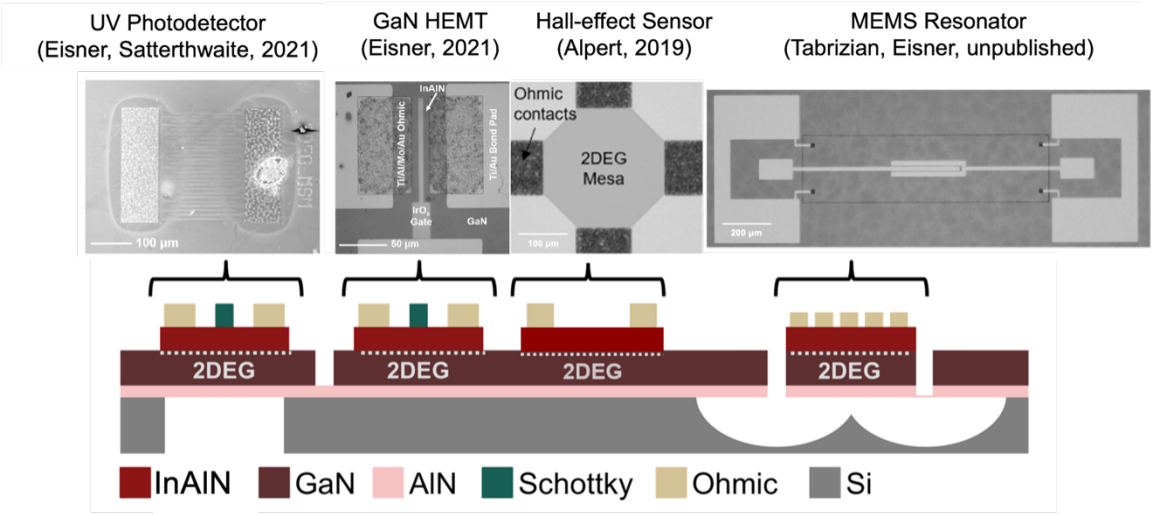

Figure 2.4: Concept for a single monolithically integrated InAlN/GaN-on-Si chip with several device architectures. Adapted from Caitlin A. Chapin, retrieved from "High Temperature and Transient Behavior of GaN Heterostructure Based High Electron Mobility Micro-Pressure Sensors" used under Attribution-NonCommercial 3.0 United States (CC BY-NC 3.0 US) [3].

extreme temperatures and corrosion on the Venusian surface completely uncooled without the need for bulky and costly thermal and chemical protection measures. Figure 2.5 depicts this idea with a microfabricated InAlN/GaN die packaged solely for electrical connectivity purposes operating onboard a Venusian rover (e.g. no shielidng from the environment).

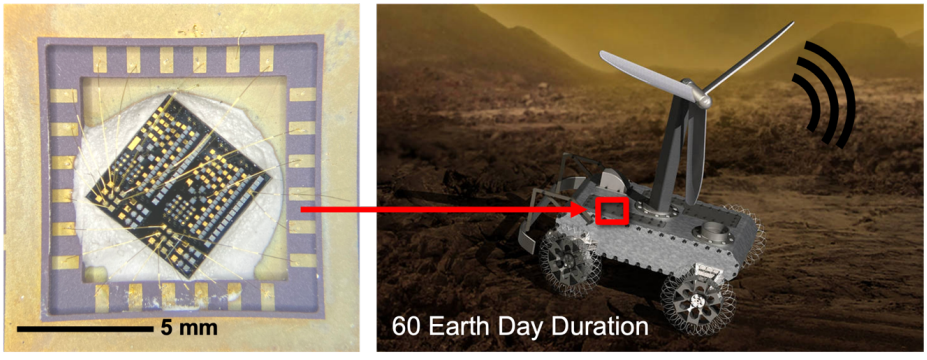

Figure 2.5: A packaged InAlN/GaN-on-Si chip (left) envisioned providing uncooled sensing and telecommunications on a long-lived Venus surface rover (right). Rover illustration adapted from [5].

2.6 The High Electron Mobility Transistor

To harness the outstanding electrical properties of the InAlN/GaN heterostructure, high electron mobility transistors (HEMTs) are fabricated. HEMTs are sometimes referred to as heterojunction field effect transistors (HFETs), a type of transistor that utilizes an electric field to modulate current in the semiconductor. A transistor is a semiconductor device used to amplify or switch electrical signals and power. Transistors are the basic building blocks of modern electronics. HEMTs leverage the 2DEG as the conducting channel (e.g. the electrons in the 2DEG are the charge carriers) and have three terminals: two Ohmic contacts called the source (S) and drain (D), and one Schottky barrier contact called the gate (G) between the two other terminals. The HEMTs discussed in this thesis are inherently normally-on and in the depletion mode, because the 2DEG channel is present in the heterostructure with zero applied bias. Normally-off, or enhancement mode, GaN HEMT technology where the device is off without applied bias can be achieved by modifications to the device structure, such as the addition of a p-type GaN layer under the gate, or recessing the gate [51].

Metal−Semiconductor Contacts

The three terminals of the HEMT device are metal-semiconductor (M−S) contacts. M−S junctions are a crucial component to microelectronic devices as they allow us to electrically control the semiconductor. The source, drain, and gate contacts discussed in this thesis are formed directly on the InAlN barrier layer. There are two types of M−S contacts: Schottky and Ohmic. Schottky contacts are rectifying, meaning that they block current flow in one direction, and allow current flow for the opposite polarity. Schottky contacts have an associated Schottky barrier height, which is the minimum energy required for electrons to surmount the M−S junction. The Schottky barrier height is desired to be as high as possible for high-temperature operation to minimize parasitic gate leakage currents, which will be discussed in further detail in Section 4.4.

Ohmic contacts exhibit non-rectifying behavior; they conduct for both polarities. Ohmic contacts obey Ohm's law and exhibit a linear response on an I-V curve. An ideal ohmic contact would have zero resistance and pass current without any voltage drop. Ohmic contacts are employed for the source and drain terminals, where the contact resistivity is desired to

be as low as possible. Low-resistance Ohmic contacts reduce source/drain parasitic resistances, which can improve HEMT device performance by lowering conduction losses and shortening parasitic delays in high-frequency operation. There are two primary types of Ohmic contacts: those with very low Schottky barrier heights that electrons can overcome, and those with thin barriers that electrons can easily tunnel through. The performance of both types of Ohmic contacts be improved by thermal annealing, which is a conventional step included in GaN HEMT microfabrication (Section 3.1).

HEMT as a Switch

The basic operating principle of the HEMT is analogous to an on/off switch. When the conductivity of the 2DEG channel is high and electrons can easily flow from source to drain, the device is "on" and the switch is closed circuit. Conversely, when the conductivity of the 2DEG channel is low and the high resistivity prevents electron flow from the source to drain, the device is "off" and the switch is open circuit. The 2DEG conductivity is modulated, and the device turned "on" or "off", by altering the voltage applied at the gate. The device can be operated in three regions depending on the magnitude of the applied drain and gate voltages.

Modes of Operation

Cut-off Region: In depletion-mode HEMTs, the application of a negative gate-to-source voltage (V_{GS}) generates an electric field that repels the electrons in the channel, depleting the 2DEG. Conversely, the application of a positive V_{GS}attracts electrons to the 2DEG and increases current flow through the channel. This is referred to as the field-effect. Increasing the magnitude of the negative V_{GS} increases the width of the depletion region, until the 2DEG is fully depleted and the high resistance between the source and drain effectively impedes the flow of drain current (I_D) from the drain to the source. This region of operation is referred to as the "off" or cut-off region, and the minimum magnitude negative gate voltage needed to switch the transistor off is referred to as the threshold voltage, V_{Th}, or the pinch-off voltage, V_p. Figure 2.6 depicts the the cut-off region on typical depletion-mode FET transfer and output curves, annotated as "Channel off".

Linear Region: When the drain-to-source voltage (V_{DS}) is less than the magnitude of V_{GS}, the switch is on and the HEMT behaves like a variable resistor. Modulating V_{GS} will alter

the 2DEG resistance, and I_D for a given V_{GS} will increase linearly with applied V_{DS}. This region of operation is referred to as linear or ohmic. Switching applications such as driving a motor or controlling a relay utilize HEMTs in this mode. Figure 2.6 shows the liner region annotated.

Saturation Region: When V_{DS} is increased further, the current through the 2DEG channel will reach its maximum value and I_D saturates regardless of further applied V_{DS}. The mechanisms of channel saturation in gated HEMTs are gradual depletion and pinch-off at the drain side due to the V_{DS} gradient, and velocity saturation in a partially depleted channel [52]. In this mode of operation, referred to as the saturation region, the HEMT is "on" and behaves as a constant-current source. The magnitude of the constant current is modulated by the applied V_{GS}. This mode has applications in small-signal amplification. Figure 2.6 is annotated with the saturation region.

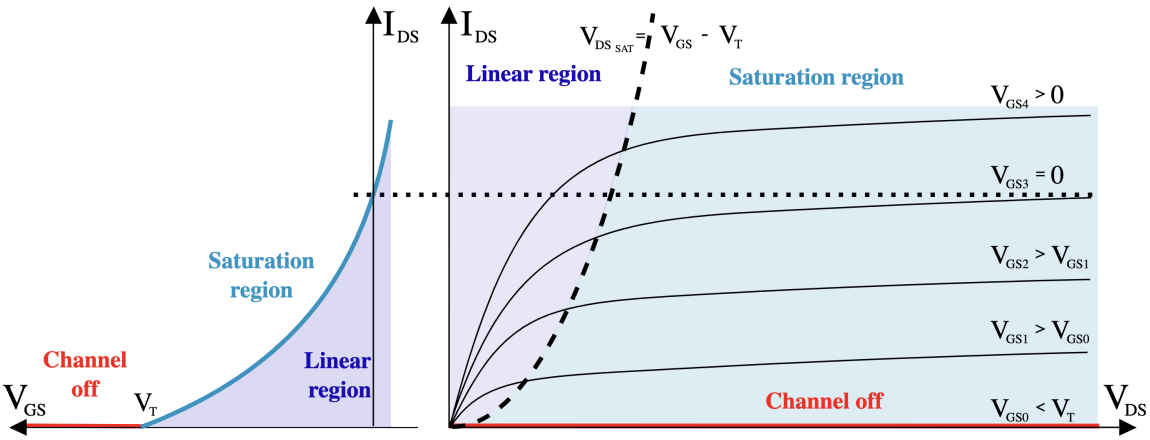

Figure 2.6: Characteristics of depletion-mode FETs, by Phirosiberia - Dispositivos Electrónicos II - Transistores unipolares ISBN848138630-8., CC BY-SA 4.0.

2.7 HEMT Demonstrations at High Temperature

While the stability of the GaN-heterostructure has been demonstrated up to 1000°C in vacuum, device failure is often reported to occur at much lower temperatures due to degradation mechanisms associated with the Ohmic and Schottky contacts and passivation schemes, which will be discussed in the next section [34].

The reduction in gate leakage is critical for high-temperature operation because it is the major source of OFF-current in depletion-mode HEMTs and leakage mechanisms (e.g., thermionic emission, thermionic trap-assisted tunneling) are generally inversely proportional to $e^{1/kT}$ [53–57]. Multiple approaches have been explored to develop GaN-heterostructure HEMTs with high ON/OFF ratios and low leakage currents including: introducing gate dielectrics for metal−insulator−semiconductor (MIS) structures (e.g., Hf_2O, TaO_xN_y) [58, 59], surface treatments prior to gate deposition (e.g., O_2 plasma + HCl, SF_6 plasma, KOH) [60–62], post evaporation gate anneals (e.g. N_2/H_2, N_2) [61, 63], backfill of mesa isolation [63], use of unannealed ohmic contacts to avoid trap introduction [64], and the use of conductive refractory metal oxides (e.g., Ir/Al oxide) [65]. While enhancement-mode InAlN/GaN devices have reached ON/OFF ratios of 10^{12} [66], RT ON/OFF ratios for depletion-mode InAlN HEMTs are reported in the range $10^3 - 10^7$ [62, 67, 68], with Herfurth *et al.* achieving the only 10^{10} performance by utilizing an ultrathin barrier [37]. Chen *et al.* demonstrated an Al_2O_3 passivated d-mode InAlN/GaN-on-Si HEMT utilizing an N_2 annealed Ni Schottky gate with RT ON/OFF ratio of 10^7 [68] and Ganguly *et al.* reported a d-mode InAlN/GaN-on-SiC HEMT using a KOH surface treatment and a Ni/Au gate with RT ON/OFF ratio of 10^6 [62].

There have been several compelling high-temperature studies of InAlN/GaN HEMTs in inert ambient or in vacuum utilizing different Schottky gate and dielectric stacks. Herfurth *et al.* demonstrated a high ON/OFF ratio of 10^{10} at RT and 10^6 at 600°C in vacuum in an ultra-thin body InAlN/GaN HEMT with Cu/Pt gate metal deposited onto a 1.5nm native oxide on the surface [37]. In the most extreme test of the InAlN/GaN HEMT to date, Maier *et al.* demonstrated a lattice-matched InAlN/GaN HEMT with a molybdenum gate metal and SiN passivation for 25 hours in vacuum at 1000°C [34]. However, ON/OFF ratio is not reported. There have been no studies on high-temperature (>300°C) operation of depletion-mode InAlN/GaN HEMTs in air or corrosive ambient. It is necessary to investigate the effects of the air environment on high-temperature performance of these devices because not all applications permit hermetic sealing to protect from the environment, including Venus surface exploration applications. The effects of oxidation on the contact metallization, barrier layer surface, and 2DEG charge density must be further studied for the InAlN/GaN material platform.

2.8 Degradation Mechanisms in GaN HEMTs

Degradation mechanisms are the physical, chemical, thermodynamic, mechanical or other processes that worsen device performance. Device "failure", and the difference between partial or total failure, is subjective; the tolerance limits for semiconductor device reliability are determined by application. Common tolerance limits for commercial-off-the-shelf (COTS) semiconductor devices are within ± 20% over the temperature range, which is usually -40°C to +150°C. Some applications require higher reliability than others and will therefore require parameter tolerances to be kept within narrower limits. In this work, the term "failure" is only used to refer to total, permanent device failure (e.g. the device no longer conducts current on the same order of magnitude).

Reliable operation of InAlN/GaN HEMTs at high temperature is frequently limited not by the heterostructure itself, but by premature failure of the contact metallization or passivation scheme. Reported high-temperature degradation mechanisms associated with the contacts include gate sinking, metal accumulation that leads to ball-up, gold diffusion, and electromigration.

Electromigration

Electromigration (EM) refers to the transport of atoms by current flow in a material. With high current density, the dissipation of heat in a material can break down and physically move atoms via electron flow. The breakdown of the material due to EM can cause absences and deposits of the material, such as voids and local accumulations. EM is a widespread degradation mechanism in microelectronics that most commonly effects the malleable metals in the semiconductor device stack, such as the Ohmic and Schottky contacts. EM can cause total device failure, as well as shorts and open circuits. EM effects are substantially worsened at high temperature due to material softening. Device geometry can also enhance the deleterious effects of EM. For example, because current density will be higher at corners, abrupt changes in the contact shape or edges can increase EM effects. Maier *et al.* identified Cu electromigration under large signal RF operation as the cause of failure while operating InAlN/GaN HEMTs at 900°C in vacuum [6]. Break-up of the source Ohmic contact metallization under strong-field was identified as the failure mode in InAlN/GaN HEMTs during 700−800°C temperature cycling in vacuum [7]. Figure 2.7 shows the retreated Cu gate metallization and damage to the source contact region after biasing. In both cases, no

metal diffusion into or alloying with the InAlN barrier layer occurred, demonstrating the reliability of the heterostructure itself.

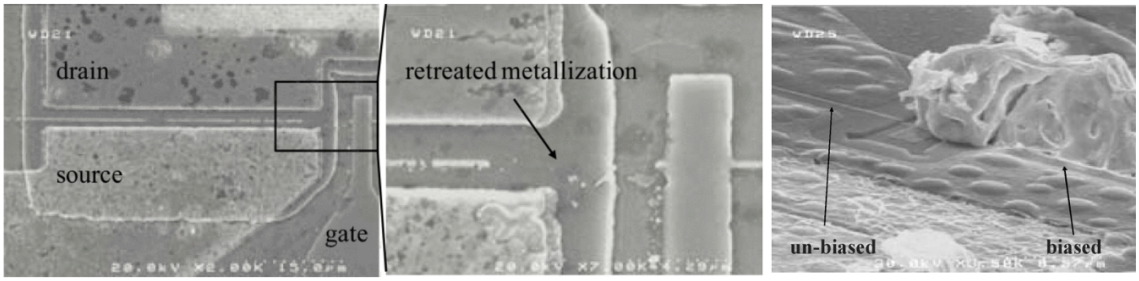

Figure 2.7: Electromigration-induced damage to InAlN/GaN HEMT metallization after high temperature operation. Virgin device (left) and device after 900°C testing under vacuum (middle), showing retreated Cu metallization. Adapted from [6]. Topology of the source Ohmic contact showing metal accumulation on the biased pad after 700-800°C testing under vacuum (right), adapted from [7] © 2010 IEEE.

Metal Diffusion

During the microfabrication process for GaN HEMTs described in Section 3.1, Ohmic contact formation requires a high temperature anneal so the metals can diffuse and form intermetallic compounds. The processing conditions for different metal stacks are optimized to achieve low resistivity. However, further thermal exposure during high temperature storage or operation can deteriorate the integrity of the contact. Undesired metal diffusion is a leading cause of device degradation in GaN HEMTs. While electromigration requires electrical activation, metal diffusion occurs at elevated temperatures without an applied bias. The diffusion lengths of metals increase with temperatures, and mobile metal atoms can migrate and cause accumulations or voids. Maier *et al.* found that diffused Au in Ni/Au HEMT gate metallization replaced Ni on the barrier layer surface, which is identified as a prime failure source after 700°C exposure [7]. Figure 2.8 shows a cross-sectional TEM image of the degraded Ni/Au gate.

Gate Sinking

Gate sinking is another cause of device degradation in GaN HEMTs. During gate sinking, the gate material will diffuse down and consume the underlying barrier layer or insulator

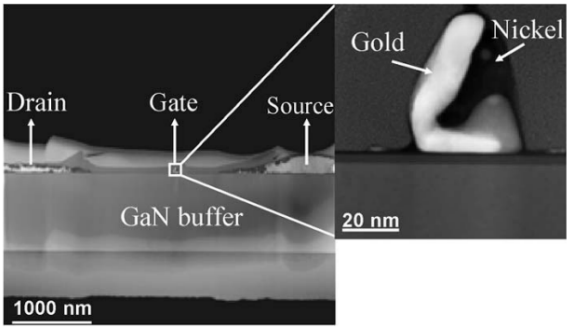

Figure 2.8: Cross-sectional STEM image of the InAlN/GaN HEMT after 800°C exposure under vacuum. Au has diffused downwards underneath Ni in the gate region. Reprinted with permission from [7] © 2010 IEEE.

layer, in some cases making direct electrical contact to the 2DEG. The metal atoms can increase scattering in the channel and reduce mobility, or act as deep level traps to carriers in the channel [8]. Gate sinking can be due to metal diffusion, electromigration, or interfacial reactions between the gate material and oxygen adsorbed onto the barrier layer surface. Ao *et al.* reported the failure of AlGaN/GaN HEMTs after annealing at 700°C in N_2 ambient for 30 minutes due to diffusion of the Cu gate electrode down into the 2DEG [8]. Figure 2.9 shows the SIMS depth profile of the Cu/AlGaN interface after 5 minutes of 700°C anneal, where partial gate sinking is seen. Ostermaier *et al.* reported a high temperature-induced metal sinking effect seen in Ir-gated InAlN/GaN HEMTs attributed to the diffusion of oxygen adsorbed onto the barrier layer surface into the Ir layer at 500°C [69]. Wu *et al.* attributed high temperature-induced I_D reduction and V_{Th} shift to gate sinking after 175°C operation [70].

Oxidation of the Metallization

Another mechanism which may degrade device performance at high temperatures in oxidizing ambients such as air is oxidation, which can cause corrosion and volatilization of metals. This affects the integrity of the materials. The oxidation of as-deposited Mo gate metal, and the subsequent high-temperature volatilization in air that caused device failure at 400°C, is discussed in Section 4.2. Selvanathan *et al.* identified oxide formation on Ti/Al/Mo/Au Ohmic contacts after thermal storage at 850°C for 5 hours, causing non-linear $I-V$ characteristics and the surface discoloration shown in Figure 2.10 [9].

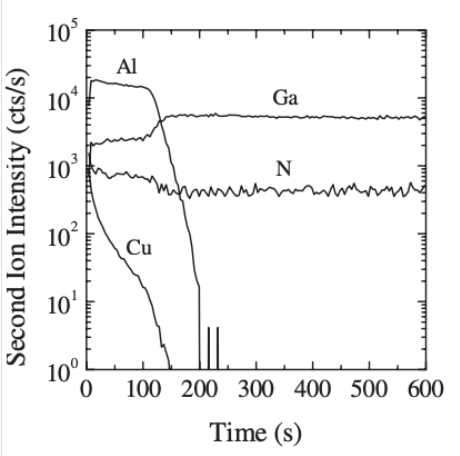

Figure 2.9: Partial gate sinking effects seen in the SIMS depth profile over the Cu gate on an AlGaN/GaN HEMT after a 5 minute anneal at 700°C. Reprinted with permission from John Wiley and Sons [8].

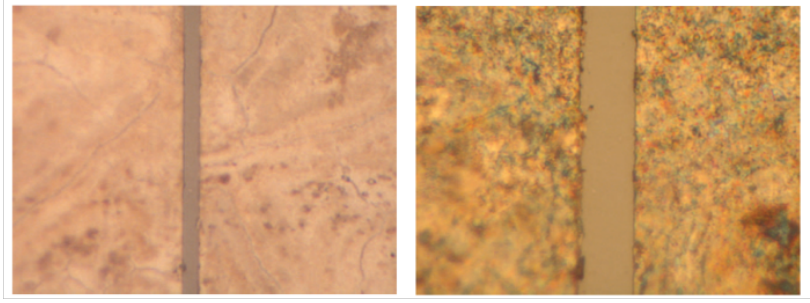

Figure 2.10: Ti/Al/Mo/Au Ohmic contacts to n-GaN before (left) and after (right) thermal storage at 850°C for 5 hours. Reprinted with permission from Springer Nature [9].

Passivation Cracks

An additional material is frequently coated onto the top of GaN HEMTs to "passivate" the device surface. The passivation layer has the advantage of shielding the GaN heterostructure from chemical reactions, contamination, and oxidation of the barrier layer. By isolating the heterostructure from its environmental conditions, the semiconducting properties of the device can be preserved. Passivation techniques can be particularly important in GaN devices to stabilize the donor-like states at the surface of the InAlN layer that are the origin of the electrons in the 2DEG. Inert materials with high chemical corrosion such as silicon nitride (SiN_x) and aluminum oxide (Al_2O_3) are frequently used to passivate the surface of GaN HEMTs. Yet, passivation is not without its drawbacks for high temperature

operation. While the InAlN/GaN HEMT system can be lattice-matched to mitigate stress in the heterostructure, the addition of a passivation layer frequently induces stress in the system. Passivations are normally amorphous. The resulting passivation films are brittle and can be non-stochiometric, which can lead to a thermal stress profile. This can be a reliability issue for high temperature device applications. As the temperature of operation is increased, thermal mismatch between the passivation and substrate can lead to cracking in the passivation layer. Maier *et al.* reported cracking in Si_3N_4-passivated InAlN/GaN-on-SiC HEMTs at 900°C around the mesa edge, which interfered with the gate metallization. An image of this passivation degradation is included in Figure 2.11.

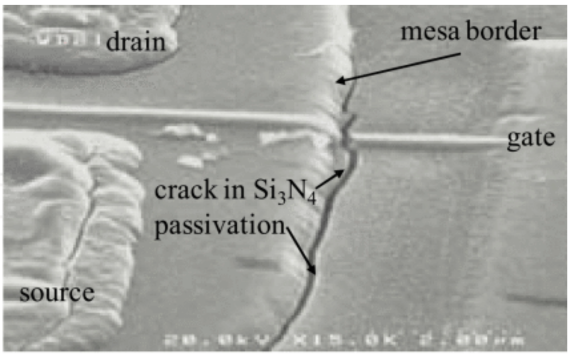

Figure 2.11: Si_3N_4 passivation cracks in an InAlN/GaN HEMT after 900°C failure. Reprinted from [6].

2.9 Summary

This chapter covered the fundamentals of GaN heterostructures, such as the polarization, 2DEG conducting channel, and InAlN and AlGaN barrier layers. Advantages of the InAlN/GaN heterostructure, such as avoiding dopant scattering effects at high temperature and the potential for uncooled monolithic integration of various devices on one chip, are discussed. The high electron mobility transistor (HEMT) is introduced, and the basic device components, modes of operation, and previous evaluations of GaN HEMTs operating at high temperatures are presented. Gate leakage currents remain a challenge to successful high temperature device operation, and previous high temperature investigations have been conducted in inert ambient or under vacuum. Therefore, the behavior of these devices in oxidizing or corrosive ambient at high temperature requires further study. The

chapter concludes with an overview of the primary mechanisms by which GaN HEMTs are known to degrade at high temperature. Previous research indicates that the degradation of InAlN/GaN HEMTs is limited not by the reliability of the heterostructure itself, but by the metallization and passivation schemes. The metallization can fail due to electromigration, metal diffusion, gate sinking, or oxidation, and the passivation can crack due to strain. Thus, these device components require further failure materials effects and analysis to increase the overall device reliability at high temperature.

Chapter 3

Microfabrication and Device Design

3.1 Fabrication Overview

In this section, the six main steps involved in the InAlN/GaN HEMT microfabrication process will be reviewed. All microfabrication was performed at the Stanford Nanofabrication Facility (SNF) and Stanford Nano Shared Facilities (SNSF). Figure 3.1 depicts the microfabrication processing steps.

3.1.1 Metal-organic chemical vapor deposition (MOCVD)

The first step in the InAlN/GaN HEMT microfabrication process is the growth of the InAlN/GaN-on-Si wafer structure (Figure 3.1). Metal-organic chemical vapor deposition (MOCVD) is an epitaxy technique used to deposit thin, high quality, single-crystal overlayers onto a crystalline substate. MOCVD is a common technology for producing III-V compound semiconductor wafers. During MOCVD, the substrate is placed into the reactor and heated. Gas containing the desired precursors is flowed over the substrate surface, where the precursor molecules decompose at high temperature and atoms deposit onto the surface of the wafer. The atoms are incorporated into the crystal lattice and the epitaxial structure is grown one atomic layer at time. The material composition of the layers is tailored *in situ* by changing the gas precursors. Typical substrates for GaN growth include

SiC, sapphire, Si, or GaN. III-Nitride growth on Si typically begins with an AlN nucleation layer because GaN cannot nucleate directly on Si. The AlN layer will reduce lattice mismatch-induced strain and threading dislocations and protect the Si from Ga doping and melt-back etching [71, 72]. The rest of the buffer layer further promotes nucleation and reduces misorientation [73]. Usually, the buffer layers are graded from AlN to $Al_xGa_{1-x}N$ to GaN through varying the Al composition, x . Between the GaN channel layer and InAlN barrier layer, a thin AlN spacer layer is sometimes included. This modification to the heterostructure has been shown to reduce roughness scattering at the interface and result in higher electron mobilities in the 2DEG channel [43, 74]. Finally, the InAlN barrier layer is deposited.

Due to the nature of the deposition process, the epitaxial layers are unintentionally doped (UID) despite the absence of a dopants in the growth recipe (e.g. no additional gas precursors are included). UID III-Nitride layers typically exhibit n-type conductivity with low background doping concentrations on the order of $\approx 10^{16} - 10^{19}$ cm^{-3} due to the incorporation of oxygen and silicon impurities during growth [75–77]. All of the wafers used for microfabrication in this thesis work were Ga-polar (Section 2.1).

Layer	**Material**	**Al Composition**	**Thickness (nm)**
4	InAlN	0.82	10
3	AlN	1	0.8
2	GaN	–	1000
1	Buffer	–	300
Substrate	Si	–	6.25×10^5

Table 3.1: InAlN/AlN/GaN-on-Si wafer structure used in Casper Run microfabrication.

The InAlN/GaN-on-Si wafer structure used in Casper Run fabrication grown via MOCVD was purchased from NTT-AT. The substrate was a 4-inch high-resistivity ($\geq$5000 $\Omega-$cm) Si (111) substrate. Table 3.1 lists the epitaxial layer stack details; layer 1 is directly grown onto the substrate and layer 4 is the top of the stack. The barrier layer thickness and Al composition were experimentally verified after growth. The total thickness of the epitaxial stack averaged 1292 nm. The sheet resistivity determined by eddy current measurement averaged 229 $\Omega/\square$ with standard deviation 6 $\Omega/\square$.

3.1.2 Mesa Isolation Etch

Following MOCVD growth of the heterostructure, the device active areas, or channels, are defined and electrically isolated from one another by mesa isolation etching (Figure 3.1 Step 2). The mesa isolation etch step also defines the alignment markers that are used in the subsequent lithography steps throughout the microfabrication process. First, direct-write lithography methods are used to create a patterned photoresist mask that coats and protects the device active areas. The wafer sample then undergoes an inductively-coupled plasma (ICP) reactive ion etch (RIE) which removes the InAlN barrier layer and part of the GaN channel in the areas of the wafer not covered by photoresist. The 2DEG no longer exists in the etched regions, and the device active areas are now referred to as "mesas" where the InAlN barrier layer and 2DEG channel are still present.

ICP-RIE etchers work by generating a plasma with an RF powered magnetic field. The chemically reactive plasma removes exposed material on the sample in the vertical direction through chemical and physical ion bombardment processes. The desired results of mesa isolation etching are minimized surface damage such as pitting, maintain Ga/N composition ratio, and smooth vertical mesa sidewalls. As is common in III-V heterostructures, the etch chemistry used in the ICP etch was chlorine-based $Cl_2/BCl_3/Ar$ plasma. A combination of Cl radical chemical reactions and Cl_2+ ion bombardment contribute to the GaN ICP etching [78]. BCl_3 plasma is added for native oxide removal, inhibiting lateral etching, reducing sputter desorption, and scavenging the water vapor [73, 79, 80].

The plasma etch recipe used in this work was developed and used at the SNF Oxford Instruments PlasmaPro System 100 III-V. This step does not require precise etch depths as long as the entirety of the 10 nm-thick InAlN layer is removed, so overetching into the GaN channel is performed to ensure device isolation. The Casper Run etch depth was estimated by atomic force microscopy (AFM) to be ≈80 nm.

3.1.3 Ohmic Contact Formation

The third step in the microfabrication process is formation of the ohmic M−S contacts (Figure 3.1 Step 3). Ohmic contact metallization is formed using lift-off processing. During lift-off, a mask of photoresist with an additional polymer lift-off layer underneath is patterned using lithography. A thin film of material is deposited over the entire sample surface area, and then the photoresist and lift-off layers are washed away so that the material film

only remains in the patterned regions. Electron bean evaporation, which is a physical vapor deposition technique, is used to deposit the ohmic metal films. During electron beam evaporation, a crucible containing the metal of interest, referred to as the "target", is bombarded by an electron beam generated by passing a current through a tungsten filament. The generated electron beam is focused onto the target by a strong magnetic field, and the metal atoms in the target are energized to evaporate into the gaseous phase. The gaseous metallic atoms then precipitate back into a solid, depositing over the sample surface. Once the chamber is pumped down to high-vacuum, various metals can be consecutively evaporated *in situ* the chamber by swapping the target, allowing for more pristine metal stacks that have not seen ambient except the top layer. After the ohmic metals are deposited, the sample is situated in a chemical bath overnight to lift the metals off the sample areas outside of the ohmic contact regions and complete the lift-off process. The Big Evaporator in the SNSF Microfab shop and AJA e-beam evapoartor at SNF were used for metal deposition.

Once the lift-off process is complete, the sample undergoes a rapid thermal anneal (RTA) in N_2 ambient to promote intermetallic compound formation. This crucial final step in the ohmic contact microfabrication process improves the contact resistivity and ensures non-rectifying behavior. The RTA is performed in the Allwin 610 Rapid Thermal Processing System at SNF.

3.1.4 Schottky Contact Formation

Figure 3.1 Step 4 shows the formation of the Schottky contact that serves as the gate electrode of the HEMT. The lift-off and evaporation process described above in ohmic contact formation is similarly used to pattern the Schottky metal in the regions of interest. If intentional oxidation of the Schottky metal is required, the sample will undergo RTA in O_2 ambient.

3.1.5 Passivation Deposition

The addition of a passivation layer on top of the sample is an optional step in the microfabrication process (Figure 3.1 Step 5). If passivation was required, aluminum oxide (Al_2O_3) was blanket deposited over the entire surface of the samples. The Al_2O_3 was atomic layer deposited (ALD). ALD is a chemical vapor deposition technique where a high quality crystalline thin film is slowly deposited one atomic layer at a time through sequential exposure

to separate self-limiting precursors. The precursors used here were Trimethylaluminum and H_2O and the substrate was held at 200°C. This thermal ALD recipe utilizes water vapor as an oxidant to avoid any oxygen plasma-induced damage. The deposition was conducted at the Fiji F202 System from Cambridge Nanotech at SNF. The thickness of the ALD Al_2O_3 layers was measured on an Si dummy that was in the chamber with the InAlN/GaN-on-Si samples duirng the run. Using the Woollam ellipsometry tool at SNF, the aluminum oxide thickness was determined to be 28 nm.

3.1.6 Passivation Etch and Bond Pad Metal Deposition

In the final microfabrication steps, the passivation is selectively etched back to expose the ohmic and Schottky pad regions for the deposition of probe/bond pad metal (Figure 3.1 Step 6). The samples coated with Al_2O_3 passivation were patterned using lithography, and the samples were etched in 20:1 BOE (Buffered Oxide Etch – 38% NH_4F, 2% HF, 60% H_2O). The Al_2O_3 etch rate was measured to be 32 nm/min using the Woollam and the Al_2O_3 passivated Si dummy wafer. To ensure total removal of the oxide, the BOE etch time was 2 minutes.

Finally, both passivated and unpassivated samples underwent a final lift-off and metal evaporation process to put down bond pad metal over the ohmic and Schottky pad regions. The addition of bond pad metal is necessary to enable wirebonding to the devices, which is required in several of the experimental test setups. The reasons why fresh metal must be deposited are two-fold:

1. The RTA process used during the ohmic contact formation significantly roughens the ohmic pad surface, which prohibits direct wirebonding. A smooth layer is needed on top.

2. The Schottky gate material is usually incompatible with gold wirebonding.

Therefore, a Ti/Au (20/200 nm) bond pad is formed over the rectangular contact probe/bond pad regions. The Ti is an adhesion layer and the Au is necesary to allow for bonding between a gold wire and a gold surface (Au−Au system), which avoids well-known issues of intermetallic compound formation, cratering, voiding, adhesion, and fragility in bonding between unlike material systems such as Au−Al.

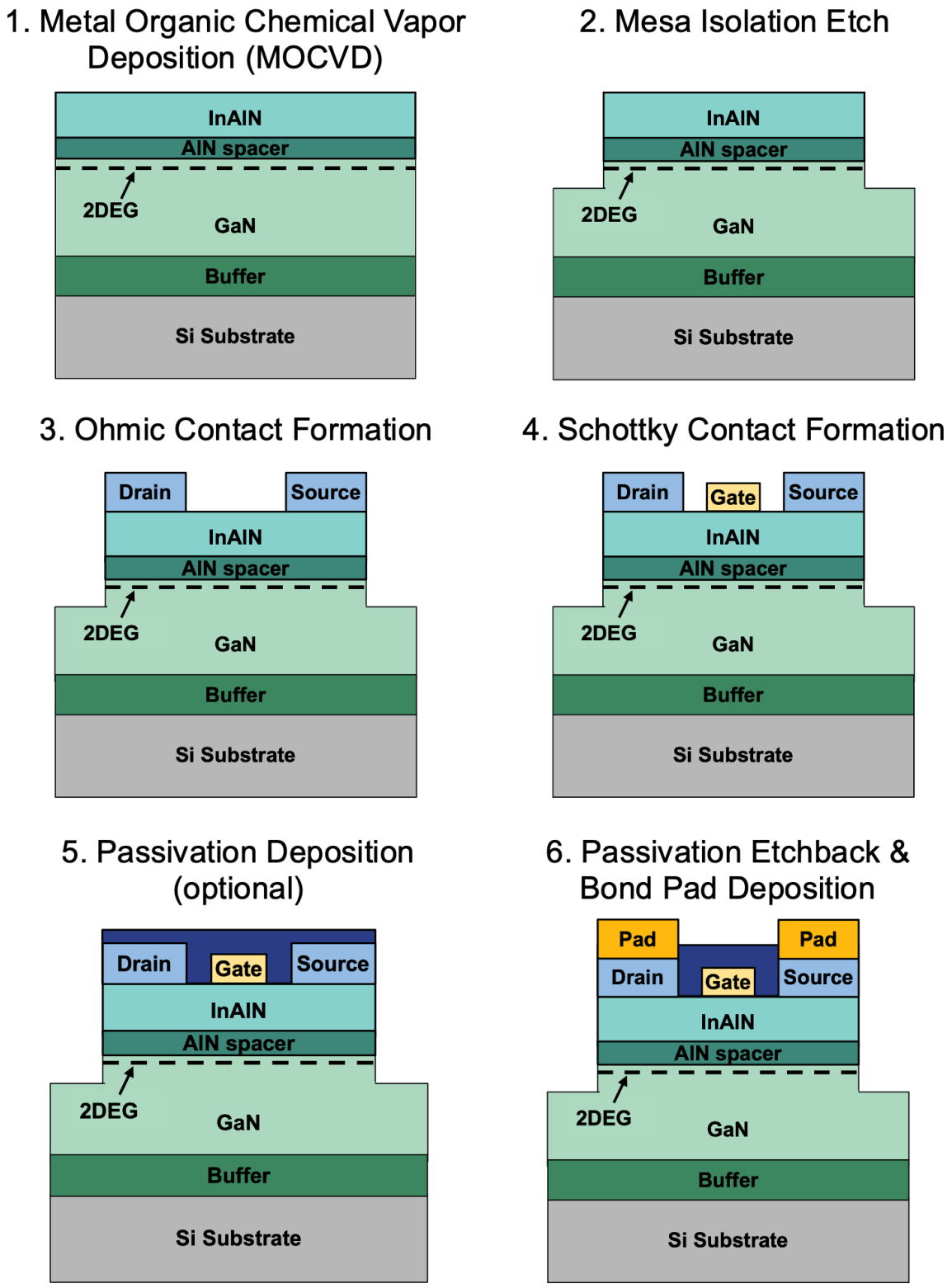

Figure 3.1: Cross-sectional device schematic of the InAlN/GaN-on-Si microfabrication processing steps.

3.2 Design Selections

3.2.1 Ohmic Metallization

Typical ohmic metal stacks to GaN and its heterostructures are multilayer and contain four metals: titanium (Ti), aluminum (Al), nickel (Ni), and gold (Au). Each metal in the stack serves a unique purpose. The Ti/Al layers are involved in the ohmic contact formation mechanism, which is two-fold. First, during the annealing process the Ti reacts with the underlaying III−Nitride layer to form TiN. The outdiffusion of N causes nitrogen vacancies, which act as donors and create a heavily n−doped region of III−N at the M−S interface that allows for tunneling [81]. Secondly, TiN spikes formed during the high temperature alloying penetrate the InAlN barrier down to the GaN channel layer, which creates a shorter conductive pathway between the contacts and the 2DEG, thus lowering the contact resistance and promoting electron transport [82, 83].

The inclusion of Al in the metal stack, in particular the Ti/Al ratio, influences the surface morphology, linearity, and contact resistance to GaN heterostructures. The effect of the Al layer on the complicated alloy reaction process is summarized in the following. The Al layer becomes liquid during the RTA process at a low melting point of 660°C [84]. Some portion of the liquid Al will react with the Ti layer to form a Ti−Al binary alloy phase. In the optimized Ti/Al ratio, enough Al is present to modulate the Ti from consuming too much N, which can lead to voids below the contact. If an excess of Al is included in the stack, the Al will consume too much Ti and prohibit TiN formation, leading to higher contact resistivity. Moreover, the liquid Al has been shown to diffuse upwards and react with the Au layer to form Al_2Au or $AlAu_4$ [84]. Excess Al can form Al−Ni intermetallics which consume Ni and degrade the blocking affect.

In addition to low contact resistance, smooth surface morphology is also sought in ohmic contacts. Surface roughness in an indication of non-uniform alloy composition in the stack, which often creates local lower resistivity regions where current crowding and heating become an issue. Moreover, low surface roughness allows for sharp edge acuity, which is necessary in short-channel HEMT devices with small critical dimensions.

In this thesis, two ohmic contact stacks were utilized on InAlN/GaN HEMTs: Ti/Al/Mo/Au and Ta/Ti/Al/Ni/Au. Selvanathan *et al.* showed the long-term thermal stability of Ti/Al/Mo/Au ohmic contacts to n-GaN at 500°C and 600°C after 25 hours [9]. The reported specific contact resistivity, ρ_c, was on the order of 10^{-6} $\Omega{\cdot}cm^2$. The inclusion of Tantalum (Ta)

prior to or instead of the Ti layer in the ohmic metallization stack has been explored for AlGaN/GaN HEMTs. Ta-based contact schemes reported in the literature include Ta/Ti/Al [85], Ta/Al/Mo/Au [86], and Ta/Ti/Al/Ni/Au [87]. Qiao *et al.* reported the measured resistivity of Ta/Ti/Al contacts as low as 5×10^{-7} $\Omega{\cdot}\text{cm}^2$ after annealing at 950°C, three orders of magnitude lower than the conventional Ti/Al comparison contact sample included in that study [85]. Mohammed *et al.* observed grain size in Ta-based and Ti-based contacts to AlGaN/GaN and found the latter to be smaller [86]. Ta/Ti/Mo/Au contact resistivity was reported to be 1.09×10^{-6} $\Omega{\cdot}\text{cm}^2$. Ti/Al/Mo/Au was reported to be 2.96×10^{-7} $\Omega{\cdot}\text{cm}^2$. Kim *et al.* has shown deposition of Ta prior to the common Ti/Al/Ni/Au stack decreases surface roughness in contacts to AlGaN/GaN HEMTs [87]. TaN/TiN formation at the M−S interface was observed in the Ta-based contacts, which had lower contact resistance compared to the Ti/Al/Ni/Au stack was achieved after annealing at a comparatively low temperature of 700°C. The same ohmic contact formation mechanism as TiN is proposed for TaN. The authors report the RMS roughness in the Ti/Al/Ni/Au and Ta/Ti/Al/Ni/Au stacks are 46.5 nm and 28.8 nm, respectively.

3.2.2 Schottky Metallization

The characteristics desired in the gate electrode of a GaN HEMT intended for high temperature operation are 1) high Schottky barrier height (SBH) 2) low electrical resistivity and 3) excellent thermal stability. Because most gate electrode materials degrade at high temperatures, current HEMT fabrication processes are limited to depositing the gate material last (e.g, after the ohmic contact anneal). An additional benefit of thermally robust gate electrodes is the compatibility with gate-first self-aligned fabrication processes that can reduce parasitic access resistances in the device. By the narrowest definition (melting point $>$ 2200°C), the five refractory metals are tungsten, molybdenum, niobium, tantalum and rhenium. A wider definition of refractory metals (melting point $>$ 1850°C) begs the inclusion of nine additional metals: titanium, vanadium, chromium, zirconium, hafnium, ruthenium, rhodium, osmium and iridium. Refractory metals are attractive Schottky metal contacts to GaN heterostructures intended for operation in extreme environments due to their high melting points and general chemical inertness. In this thesis, two refractory metals (Mo and Ir) and their oxides (MoO_3 and IrO_x) have been explored. The work functions of Mo and Ir are 4.6 eV and 5.25 eV, respectively. The Schottky barrier height of Mo to n-GaN was investigated by Ramesh *et al.* [88]. Using the $C - V$ method, the SBH of the

as-deposited Mo/n-GaN system was found to be 1.02 eV with ideality factor 1.29. After annealing at 600°C in N_2 ambient for 1 minute, the SBH was reduced to 0.73 eV and the ideality factor improved to 1.03. Furthermore, Mo was used as the gate material in the demonstration of InAlN/GaN HEMTs operating at 1000°C in vacuum [34]. Conducting refractory metal oxides have also been investigated as Schottky contacts to GaN HEMTs. In general, refractory metals are easily oxidized. The volatility of the resulting refractory metal oxides can vary greatly. After annealing at 700°C in N_2 for 1 minute, Kyaw *et al.* reported RuO_x-gated InAlN/GaN HEMTs had lower leakage and increased ON/OFF ratio in comparison with Ni/Au-gated devices [89].

However, another factor must be taken into account during materials selection for InAlN/GaN HEMTs intended for Venus surface exploration: potential chemical reactions with the constituents in the atmosphere. Figure 3.2 shows the reaction of elements tested in Venus surface conditions. Lucko *et al.* reported that a polished Mo foil sample had a thin surface layer of carbide followed by MoS_2 and MoO_3 layers after 30 days of exposure in the NASA GEER chamber, which was simulating Venus surface conditions [10]. After this research was published, an Au overlay was added to the Mo gate in the Casper Run devices in order to prevent the Mo from reacting with the Venusian atmosphere. Au was found to be chemically inert under Venus surface conditions [90]. Promisingly, Figure 3.2 shows that Ir has no reaction after extended exposure to Venus conditions, which is why it was chosen as the gate material to explore.

The thermal stability of Ir and IrO_x gates on AlGaN/GaN HEMTs has been previously investigated [91–93]. Vallo *et al.* intentionally oxidized electron beam evaporated Ir Schottky contacts at 500°C for durations between 1 and 10 minutes and investigated the electrical characteristics of the resulting devices [94]. It was found that increased oxidation time corresponds to increased SBH, decreased leakage currents, and positive shift in threshold voltage and peak transconductance, suggesting the possible use of this gate electrode platform for the formation of enhancement mode devices. A mixture of Ir and IrO_x in the O_2 annealed gate contact layers was elucidated by depth profiling, with higher IrO_x content seen in the devices oxidized for longer durations. In a follow-up study, Lalinksy *et al.* compared the microstructure and electrical characteristics of IrO_x-gated AlGaN/GaN circular HEMTs as a function of oxidation temperature [95]. The authors found that the as-deposited 15 nm Ir layer is transformed to the IrO_x phase at oxidation temperatures of 700°C and 800°C in O_2 ambient, and concluded that the oxidation process begins at the

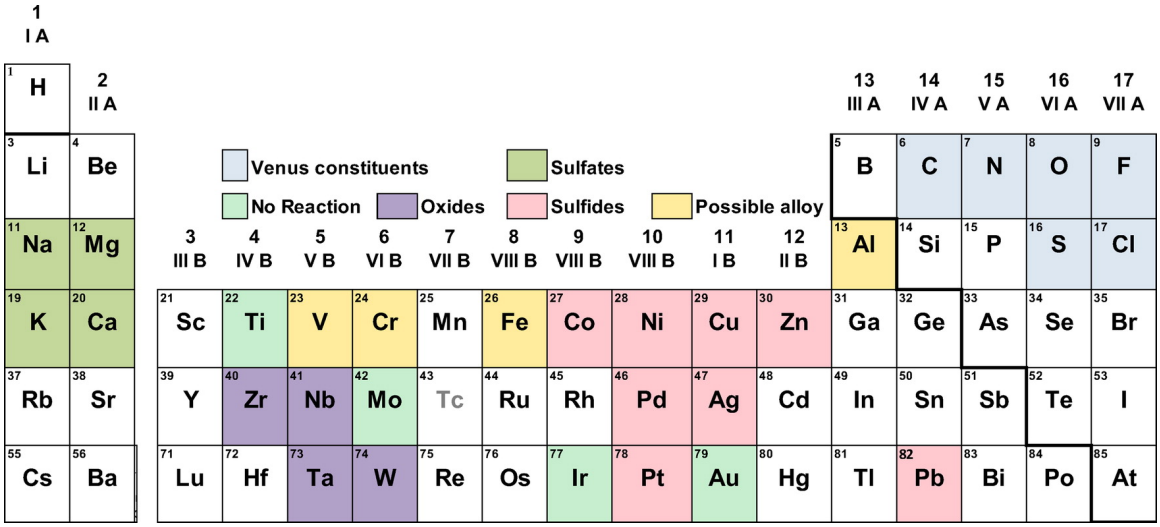

Figure 3.2: Partial periodic table of elements tested in Venus surface conditions. Reprinted with permission from [10].

top of the as-deposited Ir and progresses towards the Ir/AlGaN interface. Additionally, the leakage current in IrO_x-gated devices oxidized at 600–700°C for 1 min was improved by 5 orders of magnitude compared to as-deposited Ir-gated devices. Accelerated reliability testing of the IrO_x-gated AlGaN/GaN HEMTs oxidized at 800°C demonstrated excellent thermal stability of the devices for up to 24 hours of storage in air atmosphere at 450°C; an increase in SBH and decrease in leakage current was also seen after the 24 hour storage. The higher drain saturation current in the IrO_x versus Ir (as deposited) devices is attributed to higher 2DEG densities in the oxidized devices.

Ostermaier *et al.* reported an increased of 100% in the gate capacitance of Ir/Au-gated InAlN/GaN HEMTs with an ultrathin 2 nm barrier layer after annealing at 700°C [96]. The authors attribute the improved performance to the outdiffusion of oxygen from an interfacial layer present at the Ir/InAlN interface. At annealing temperatures lower than 700°C, $I-V$ and $C-V$ measurements indicate an inhomogeneous gate electrode material, attributed to local oxygen diffusion along grain boundaries. After annealing at 700°C, which increases the diffusion length of oxygen, the $C-V$ curve shows only one capacitance region, indicating the dispersion of oxygen in the Ir gate is homogeneous. Devices annealed at 700°C exhibit a 50% increase in transconductance and positive threshold voltage in comparison to as-deposited Ir devices. In addition, TEM analysis confirms the InAlN/AlN barrier layer thickness remains unchanged after annealing and the Ir metal does not diffuse into the

barrier. Intentional oxidation anneals have been reported to lead to outdiffusion of Ga to the barrier layer surface, causing a shift of the Fermi level at the service to the leve of Ga vacancies. Schottky barrier height increase and thermal staility can then follow due to this pinning of the Fermi level [95].

3.2.3 Passivation Selection

As described in Section 2.8, passivating the HEMT surface adds a layer of protection against environmental effects, but at the potential expense of the strain-free InAlN/GaN heterostructure system. Therefore, only a subset of devices were passivated with Al_2O_3. The rest were left bare so that no additional strain would be added to the lattice-matched InAlN/GaN system, and degradation mechanisms such as passivation cracking could be avoided. During the selection of passivation, the work of D. Lukco *et al.* was once again consulted [90]. The authors reported single-crystal sapphire (Al_2O_3) substrates were intact and had no chemical reaction after 10-day exposure in the GEER chamber.

3.2.4 HEMT Geometry

The conventional geometry of GaN HEMTs is rectangular or linear (L-HEMT). Figure 3.3 shows a diagram depicting the typical L-HEMT layout. The L-HEMT source, gate, and drain are parallel rectangles. An alternative device geometry is the annular or circular HEMT (C-HEMT), where the drain, gate, and source are concentric circles (Figure 3.3). L-HEMT devices fall into the category of enclosed layout transistors (ELTs). The C-HEMT layout offers several advantages over the standard L-HEMT layout. L-HEMT devices suffer from electric field crowding at the sharp gate edge, which causes local device breakdown. C-HEMTs generally do not have this issue because the electric field evenly distributes around the circular gate. Zhang *et al.* reported 50% higher breakdown voltages in GaN C-HEMTs compared to L-HEMTs [97]. Individual L-HEMTs generally offer smaller footprints than C-HEMTs, which is desirable for achieving large packing densities. However, De Lima *et al.* demonstrated size savings of 18.6% in C-HEMTs compared to L-HEMTs by using an overlapping gate geometry [98]. Additionally, higher effective (W/L) and faster transient switching was achieved in C-HEMT devices with minimized source and drain junction areas [98]. This implies the C-HEMT geometry is favorable for high frequency operation.

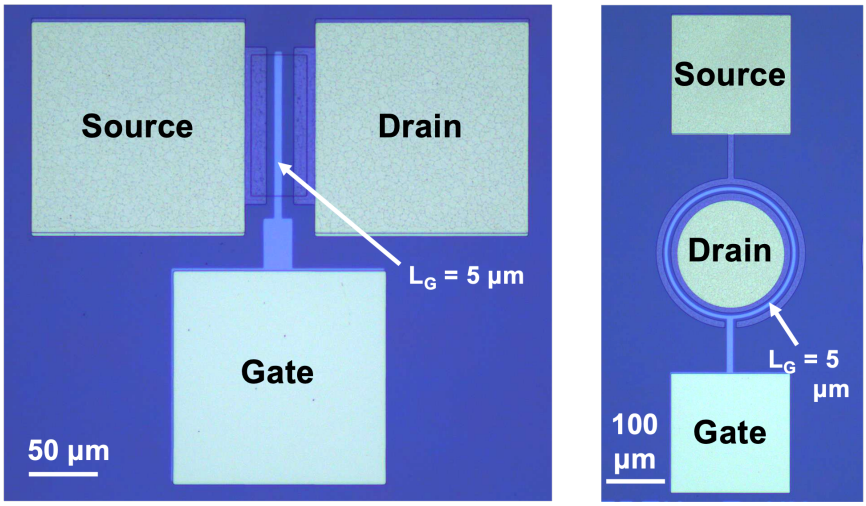

Figure 3.3: Top-view optical images of a microfabricated L-HEMT (left) and C-HEMT (right).

Another advantage of the C-HEMT transistor for extreme environment space applications is that ELTs are well-known to provide improved radiation hardness due to effective prevention of leakage currents [99]. Radiation hardening FETs against total-ionizing dose effects can be achieved by using the enclosed gate format, which eliminates the edges known to cause leakage paths in NMOS transitors [99, 100].

Furthermore, the C-HEMT geometry eliminates issues with the gate-mesa sidewall overlap region in L-HEMTs. The gate-mesa overlap regions are shown on the L-HEMT in Figure 3.4. As described in Section 3.1, plasma dry etching is commonly used to achieve device isolation. However, this microfabrication technique introduces reliability issues. First, a high density of traps is generated at the mesa sidewall due to plasma-induced damage. H.-C. Chiu *et al.* showed that GaN HEMTs with dry etched mesa sidewalls exhibited an additional trap activation energy level at high temperature, which is attributed to the mesa sidewall damage [101]. Second, the gate contact is in direct contact with the 2DEG in the region where it overlaps the mesa sidewall, forming a parasitic leakage path [101]. Additionally, this area is prone to gate sinking of the gate metal atoms into the 2DEG channel due to the direct contact. In the L-HEMT geometry, there are two gate-mesa sidewall overlap regions at each end of the mesa, which are necessary for complete channel modulation (Figure 3.4). C-HEMT geometry can reduce or eliminate these issues because device isolation is inherent to the concentric nature of the contacts. This means that mesa isolation plasma etching is

not necessary in C-HEMT microfabrication (Figure 3.4). Furthermore, because the drain pad is contained within the circular gate and source contacts, the parasitic off-state leakage path from the drain pad to the gate pad is not present in C-HEMT devices [102].

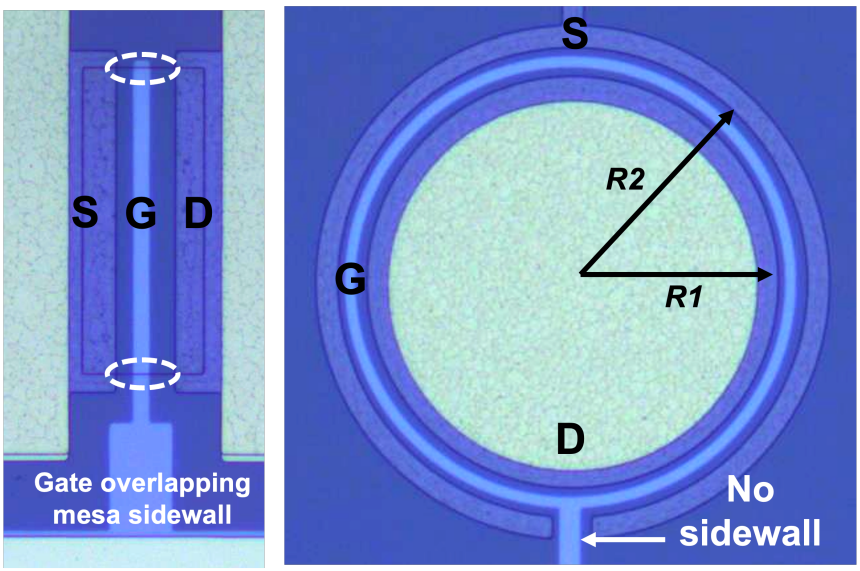

Figure 3.4: Close-up optical images of a microfabricated L-HEMT annotated with the gate-mesa sidewall overlap regions (left) and C-HEMT showing no mesa edge and critical dimensions (right).

Considering its merits for radiation-rich, high power, and high frequency applications, as well as the suppression of leakage currents and trap generation due to sidewall defects, the C-HEMT geometry is compelling and was pursued for high-temperature applications in this thesis in addition to traditional L-HEMT geometry.

The C-HEMTs were operated in internal drain bias configuration mode (IDBC). In this configuration, the inner concentric circle is biased as the drain and the outermost concentric circle is the source. IDBC has been shown to increase the drain saturation current compared to external drain bias configuration (EDBC) due to differences in the longitudinal electric field densities [103].

The effective aspect ratio for C-HEMTs is given by the following [104],

$$(\frac{W}{L})_{eff} = \frac{2\pi}{\ln \frac{R_2}{R_1}} \tag{3.1}$$

which was demonstrated to achieve good fitting between experimental and calculated $I_D -$

V_{DS} characteristics [104]. The two radii, R1 and R2, are the internal and external radii of the channel shown in Figure 3.4. The channel length, $L_{CH} = R2–R1$. The effect width, W_{eff}, can be written [105],

$$W_{eff} = \frac{W}{L} L_G = \frac{2\pi}{\ln \frac{R_2}{R_1}} L_G \tag{3.2}$$

3.3 Fabrication Runs

Two mega fabrication runs were completed for this thesis work: Casper Run and Vulcan Run. The full fabrication runsheets are included in Appendix A. Vulcan Run was completed first and represents the first generation of devices. Casper Run iterated on lessons learned from Vulcan Run metallization, and the C-HEMT geometry was added. Table 3.2 displays the Vulcan Run sample types. Table 3.3 shows the Casper Run sample types.

Sample #	**Material**	**Ohmic**	**Schottky**	**Bond Pad**	**Passivation**
1	InAlN/AlN/GaN	Ti/Al/Mo/Au	IrO_x	Ti/Au	–
2	InAlN/AlN/GaN	Ti/Al/Mo/Au	Mo	Ti/Au	–
3	InAlN/AlN/GaN	Ti/Al/Mo/Au	Mo	Ti/Au	Al_2O_3 (7 nm)
4	InAlN/AlN/GaN	Ti/Al/Mo/Au	Mo	Ti/Au	Al_2O_3 (18 nm)

Table 3.2: Vulcan Run sample types.

Sample #	**Material**	**Ohmic**	**Schottky**	**Bond Pad**	**Passivation**
1	InAlN/AlN/GaN	Ti/Al/Mo/Au	IrO_x	Ti/Au	Al_2O_3 (28 nm)
3	InAlN/AlN/GaN	Ti/Al/Mo/Au	Ir/Au	–	Al_2O_3 (28 nm)
5	InAlN/AlN/GaN	Ta/Ti/Al/Ni/Au	Mo/Au	Ti/Au	Al_2O_3 (28 nm)
7	InAlN/AlN/GaN	Ta/Ti/Al/Ni/Au	IrO_x	Ti/Au	–

Table 3.3: Casper Run sample types.

3.4 Additional Device Architectures

3.4.1 Hall-effect Sensors

Magnetic Field Sensing: Hall-effect sensors utilize the Hall effect to detect magnetic fields. These devices consist of a symmetrical large-area mesa region with four ohmic terminals. Current is applied across two parallel terminals, and voltage is measured across

the other set of parallel terminals. The resulting Hall voltage (V_H), which is perpendicular to both the applied current (I) and the external magnetic field (B), is defined as:

$$V_H = \frac{IBr_nG_H}{qn_s} \tag{3.3}$$

where r_n is the scattering factor of the material, G_H is the shape factor, q is the electronic charge, and n_s is the sheet carrier density. In most applications, the ideal Hall-effect sensor would exhibit a high sensitivity with respect to supply current and supply voltage to maximize the signal for readout. The sensitivity of a Hall-effect device with respect to supply current is referred to as the current-scaled sensitivity (S_i) and is inversely proportional to sheet carrier concentration,

$$S_i = \frac{V_H}{IB} = \frac{r_n}{qn_s}G_H \tag{3.4}$$

A reduction in the sheet carrier density of the 2DEG increases the sheet resistance of the device, leading to a drop in current under constant voltage conditions, and thereby increasing the current-scaled sensitivity. The sensitivity with respect to supply voltage, also known as the voltage-scaled sensitivity (S_v), is proportional to the electron mobility (μ_H) and is defined:

$$S_v = \frac{V_H}{V_sB} = \frac{r_nG_H}{Rqn_s} = \frac{\mu_H r_nG_H}{(L/W)_{eff}} \tag{3.5}$$

where V_s is supply voltage, R is the device resistance, and $(L/W)_{eff}$ is defined as the effective number of squares, or the ratio of the internal resistance to the sheet resistance [106]. The experimental characterization of Hall-effect sensors exposed in a Venus simulation chamber is described in Section 5.2.

Van der Pauw Method: Hall-effect sensors serve the dual purpose of enabling characterization of the 2DEG properties using the van der Pauw method. The van der Pauw method consists of a series of 4-point resistivity measurements made around the periphery of a sample. The technique is valid under the conditions that the sample is homogeneous, flat, and approximately 2-dimensional (thickness of 2DEG channel << area of sample), and the contacts are on the sample perimeter and as small as possible. Using the van der Pauw method, values for the sheet resistance (R_{SH}), carrier concentration (n_s), and mobility (μ)

in the 2DEG channel can be obtained experimentally. Section 5.2 describes device data collected using the Van der Pauw method.

3.4.2 UV Photodetectors

The experimental characterization of UV photodetectors is discussed in Section 5.2. The AlGaN/GaN photodetectors have a peak wavelength of 362 nm and exhibit high responsivity (R) and low dark current at room temperature [107]. The operating principle of these devices is based on metal-semiconductor-metal (MSM) photodetectors. In MSM detectors, two metal electrodes form a Schottky barrier on a semiconductor. The application of voltage across the electrodes generates a small dark current from the positive to negative electrode. When the device is exposed to UV light, electron-hole pairs are photogenerated, resulting in increased current. The photocurrent magnitude (I) scales with the intensity of the incident UV radiation. The photocurrent is directly proportional to the responsivity,

$$R = \frac{I}{P} \tag{3.6}$$

where P is the incident radiant energy. The photocurrent is also proportional to the gain, G, which is an important figure of merit for photodetectors and is defined as the ratio of charge carriers to the photon flux:

$$G = \frac{hc}{q\lambda}\frac{I}{P} \tag{3.7}$$

where λ is the wavelength of incident radiation, h is Planck's contact, and q is the electronic charge. While the AlGaN/GaN photodetectors operate similarly to MSM detectors, these devices do not include a metal Schottky electrode. Instead, the AlGaN barrier layer and underlaying 2DEG channel replace the metal. The mechanism of photocurrent generation is discussed in [107]. Additionally, the AlGaN/GaN UV photodetectors are arrayed in an interdigitated electrode design to increase responsivity and decrease response time [107].

3.5 Device Packaging

To perform *in situ* device characterization over extended durations and enable active testing in setups such as the XLab Venus chamber, samples must be packaged. Microelectronics packaging refers to the design and production of specialized enclosures that hold the sample

and allow for electrical interfacing with the larger system. Usually, packaging serves the dual purpose of protecting the sample from mechanical damage, electrostatic discharge, and environmental degradation. In some cases, the packaging is designed to stabilize the sample temperature. For harsh environment applications like space and military communications, or MEMS applications, ICs will normally be hermetically sealed. During the hermetic sealing process, the IC is placed into an enclosure and the lid is sealed via seam welding. The airtight seal ensures the IC is isolated from the surrounding environment and remains free of bacteria, moisture, oxygen, dust etc. NASA HOTTech grants, which funded part of this thesis work, aim to develop technologies that can survive with minimal packaging and no shielding from the environmental conditions on Venus. The reasoning for this goal is twofold: 1) the technical risk to the mission is reduced if the microelectronics can survive in the event that packaging aboard a Venus surface mission fails, and 2) the lack of mature and reliable 500°C capable, weather-resistant electronics packaging that would be needed for Venus surface exploration. Towards the maturation of packaging for Venus, the behavior of die attach, metal interconnects, and enclosure materials has been studied under experimental exposure to simulated Venus surface conditions by HOTTEch collaborators at the University of Arkansas [108]. Insights from that study have informed the choice of materials used in chip-level packaging pursued in this thesis.

Housing: Two types of sample housings or enclosures have been used in the experiments described herein. The first type are flat alumina boards which were custom produced by collaborators at the University of Arkansas and Makel Engineering, Inc. The boards were screen-printed and fired with a thick-film gold layer (3066/3068N wire-bondable Au Conductors, Ferro Corporation) to enable electrical connection, and in some cases the sample gold layer was used as the die attach material to adhere the die to the board. The other type of housing used was commercial off-the-shelf (COTS) ceramic dual inline packages (c-dip) and ceramic quad flat packs (cqfp) of various sizes and different pin-out configurations. The COTS packages were taken out of spec above their temperature rating of 400°C during experimentation.

Die Attach: Die attach is the material used to adhere the die to the housing. The epoxies used in this thesis were premixed. Once a thin layer was applied to the housing surface, the die was attached, and the sample was cured on a hot plate or in an oven according to the

instructions on the epoxy datasheet. Three different epoxies have been employed: Cotronics 989F-1 ceramic alumina adhesive fine grade (Section 4.5), PELCO high performance nickel paste (Sections 5.4 and 5.5), and Aremco 571 high temperature ceramic adhesive used on the active sample (Section 5.6). Instead of epoxy, Ferro Corporation's gold paste that was used during the screen printing process was also used as the die attach on the boards that held the passive samples described in Section 5.2 and Section 5.6.

Wirebonding: Wirebonding is the process of attaching a very thin wire between two points to form an electrical connection. In this thesis, the method used is ultrasonic wirebonding, where a wire is pressed against the surface of interest and vibrated at high-frequency for a short time to create the bond. For high-temperature packaging, gold wires are used. The wirebond is formed between the device's gold bond pad and the gold traces on the housing or enclosure. All wirebonding was performed at the West Bond 7476E Wedge-Wedge Wirebonder in SNSF.

Filter: Because the XLab Venus simulation chamber uses a grafoil gasket for sealing, an abundance of caution was taken to prevent possible carbon contamination of the samples in this test setup. Therefore, the packaging for the samples that entered the XLab Venus chamber included a 10 μm mesh stainless steel filter which was epoxied on top of the housing (Section 5.4 and Section 5.5).

Chapter 4

HEMTs Operating at High Temperature in Air

4.1 Overview

In the next two chapters, several proof-of-concept experiments and fundamental studies involving HEMTs exposed to high temperature ambient will be presented. This chapter will cover the characterization of InAlN/GaN-on-Si HEMTs and metallization schemes at temperatures up to 600°C for durations up to 6 days in air.

4.2 Suppression of Leakage Current at 300°C in MoO_3-Gated L-HEMTs

4.2.1 Motivation

Because HEMTs often exhibit significant gate leakage during high temperature operation, the choice of Schottky metal is critical. Increased gate leakage and reduced ON/OFF ratio are unsuitable for the design of high temperature electronics and integrated circuits. This section presents high temperature characteristics of depletion-mode molybdenum trioxide (MoO_3)-gated InAlN/GaN-on-silicon HEMTs in air. After a room temperature oxidation of the Mo for 10 weeks, the leakage of the HEMT is reduced over 60 times compared to the as-deposited Mo. The use of MoO_3 as the Schottky gate material enables low gate leakage, resulting in a high ON/OFF current ratio of 1.2×10^8 at 25°C and 1.2×10^5 at 300°C in

air. At 400°C, gate control of the InAlN/GaN 2DEG channel is lost and unrecoverable. Here, this permanent device failure is attributed to volatilization of the MoO_3 gate due to the presence of water vapor in air. Passivation of the device with SiN enables operation up to 500°C, but also increases the leakage current. The suppression of gate leakage via Mo oxidation and resulting high ON/OFF ratio paves the way for viable high temperature GaN-based electronics that can function beyond the thermal limit of silicon once proper passivation is achieved.

4.2.2 Experimental Methods

The HEMT devices were fabricated with an $In_{0.18}Al_{0.82}N$/GaN-on-silicon wafer purchased from NTT Advanced Technology Corporation. The GaN heterostructure, schematic of the gate evolution, and an optical image of the device is shown in Figure 4.1. Devices were isolated through BCl_3/Cl_2 ICP mesa etching, followed by evaporation of Ti/Al/Mo/Au (10/200/40/80 nm) ohmic contacts which were annealed at 850°C for 35 seconds in N_2. Molybdenum (30 nm) was evaporated as the Schottky contact and Ti/Au bond metal was patterned with liftoff. The Mo gates were left to oxidize at RT in air to form MoO_3 for ten weeks. The gate length of the HEMT is 1 μm, centered between source and drain (low power) in a 5-μm-long by 50-μm-wide 2DEG channel. The die was Vulcan Run sample type #2 (see Table 3.2 for details).

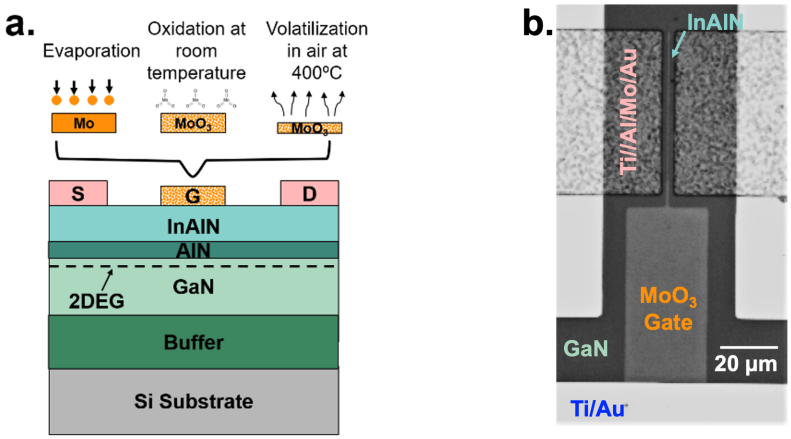

Figure 4.1: Schematic of InAlN/GaN heterostructure and molybdenum gate evolution due to high temperature exposure in air (a) and optical image of microfabricated HEMT transistor (b).

The high temperature response of the InAlN/GaN HEMTs was characterized on a Signatone Inc. high temperature probe station from RT to 300°C in 50°C increments in air, with a holding time of ten minutes at each temperature before data was acquired. To examine the return characteristics, measurements were then taken in 100°C increments as the temperature was ramped back down. Finally, the device was ramped directly up to 400°C and tested. Current-voltage ($I_D - V_{DS}$, $I_D - V_{DS}$, $I_D - V_{DS}$) measurements were taken on a semiconductor parameter analyzer (Agilent Technologies B1500A).

4.2.3 Results and Discussion

Figure 4.1 compares the $I_D - V_{GS}$ curves of the InAlN/GaN HEMT at 10 mV drain to source voltage one week after Mo deposition and 10 weeks after the deposition. The long duration between the first test and the second test enabled the MoO_3 to undergo a RT oxidation to MoO_3. The off current of the device drops by ≈60 times after the RT anneal, showing the oxidation process reduces leakage in the off state.

The high temperature response, $I_D - V_{DS}$, $I_D - V_{GS}$, and $I_G - V_{GS}$, after undergoing the 10-week RT anneal are shown in Figure 4.2. The large gate leakage is the dominate form of OFF-current when the device is operated below the threshold voltage (Figure 4.2). The $I_D - V_{DS}$ response shows the performance when ramping up to 300°C and then back down to 25°C. Solid lines represent measurements taken as the temperature was increased and dotted lines represent the measurements taken as the temperature is decreased. The characteristics show little difference in performance during temperature ramp up and ramp down.

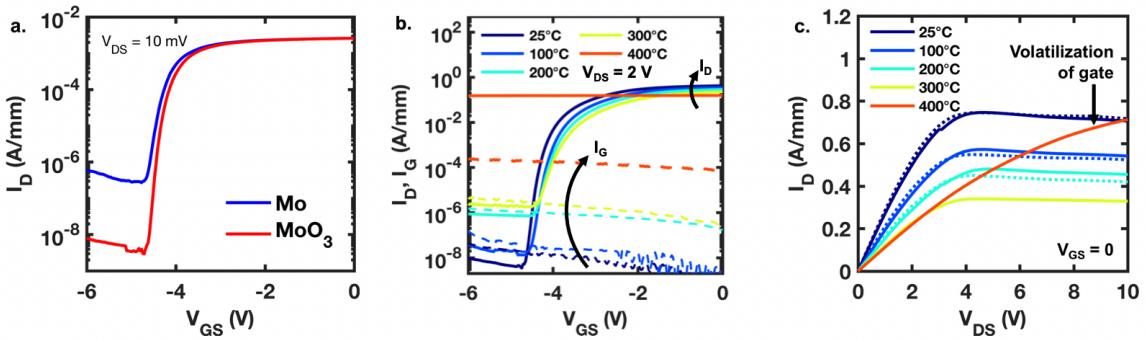

Figure 4.2: $I_D - V_{GS}$ curves comparing as-deposited Mo and MoO_3 (a). $I_D - V_{GS}$ (solid) and $I_G - V_{GS}$ (dashed) curves from RT to 400°C (b). $I_D - V_{DS}$ curves from RT to 400°C; dotted lines represent the return response while ramping down to RT from 300°C (c).

After testing to 300°C and performing elemental characterization, the device was brought directly up to 400°C. While the device showed promising performance up to 300°C, testing at 400°C caused non-recoverable device failure, due to loss of gate control, shown in Figure 4.2. After this failure at 400°C, the gate is no longer visible under an optical microscope. Auger electron spectroscopy (AES) is used to confirm the disappearance of the gate after exposure to 400°C. AES maps of the device after 300°C and 400°C exposure are shown in Figure 4.3. The AES data shows that the Mo elemental ratio goes from ≈34% to ≈6% after 300°C and 400°C exposure, respectively.

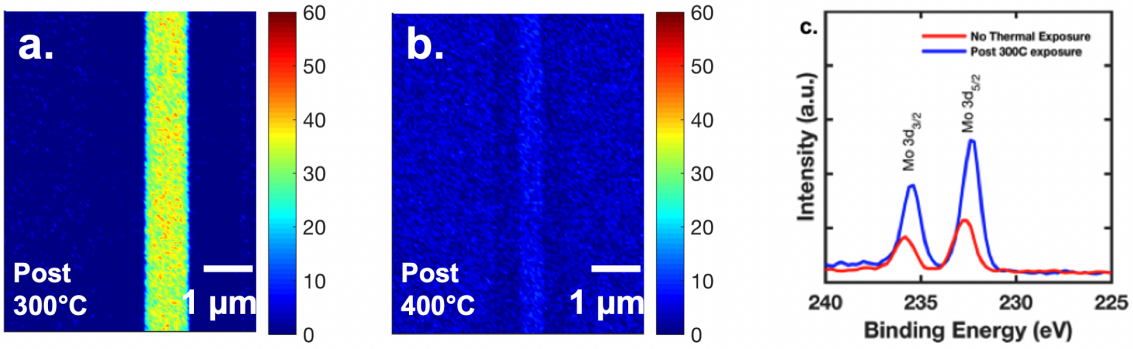

Figure 4.3: AES map of percent molybdenum after 300°C exposure (a) and after 400°C exposure (b). XPS plot of binding energy versus intensity of Mo $3d_{3/2}$ and $3d_{5/2}$ peaks (c).

X-Ray photoluminescence spectroscopy (XPS) measurements were taken to determine whether the Mo had remained a metal or had oxidized. Figure 4.3 shows the XPS spectra of the Mo $3d_{3/2}$ and $3d_{5/2}$ peaks after a 10-week RT anneal and after 300°C exposure. Fits find that the Mo $3d_{3/2}$ and $3d_{5/2}$ peaks are at 232.7 eV and 235.9 eV with no exposure to temperature and at 232.4 eV and 235.5 eV after 300°C exposure. Both of these sets of peaks match previously reported binding energies for the 3d orbital for MoO_3 [109, 110]. This shows that the molybdenum oxidizes even under RT conditions.

Previous work has shown that MoO_3 volatilizes when exposed to water vapor at elevated temperatures to form $MO_2(OH)_2$ [111, 112]:

$$MoO_3(s) + H_2O(g) \longrightarrow MO_2(OH)_2(g) \tag{4.1}$$

Thus, it is hypothesized that at 400°C the MoO_3 volatilizes in air at a rate significant enough to cause loss of the Schottky metal, likely due to reaction with water vapor. Temperatures under 400°C should not be thought of as safe because volatilization rates

are exponentially temperature dependent [111]. Thus, the 300°C operation would not be exempt from loss of the gate, but the volatilization occurs less quickly. While the unpassivated MoO_3 system is fragile and cannot exceed temperatures of 400°C, the initial device performance below 300°C is promising and surpasses the operational limits of silicon. The off current ($I_{D,off}$), the saturation current ($I_{D,sat}$) at $V_{DS} = 5$ V and $V_{GS} = 0$ V, and the ON/OFF ratio ($I_{D,on}/I_{D,off}$) of the device before failure are shown in Figure 4.4. Red markers and blue markers represent measurements taken as the temperature ramped up and ramped down, respectively. The ON/OFF ratio of the device is 1.2×10^8 and 1.2×10^5 at 25°C and 300°C, respectively. While the saturation current does not show degradation after 300°C exposure, the ON/OFF ratio decreases to 2.9×10^7 after returning to 25°C, which can be attributed to the increase in the OFF-state current. In Figure 4.4, the leakage current is increasing exponentially with increasing temperature and is attributed to thermionic emission, illustrating the challenge of maintaining large ON/OFF ratios at high temperatures.

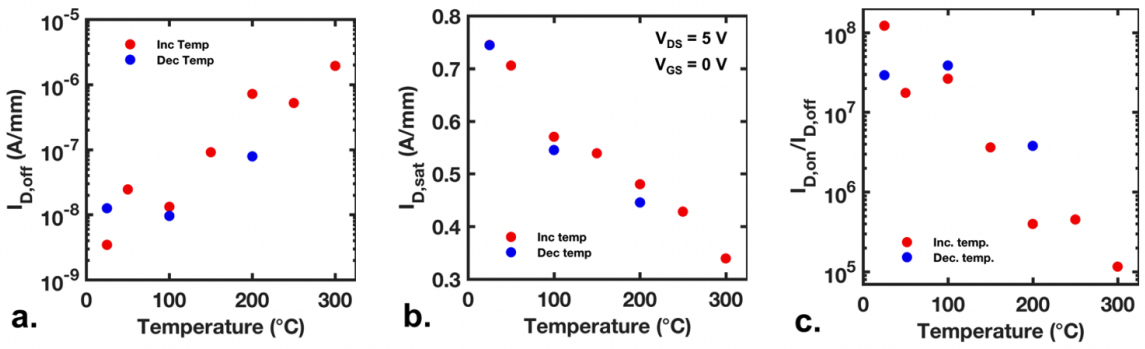

Figure 4.4: OFF-current (a), saturation current (b), ON/OFF ratio (c), vs. temperature.

The maximum transconductance ($g_{m,max}$), subthreshold slope (SS), and threshold voltage (V_{Th}) as a function of temperature are plotted in Figure 4.5. At 25°C, the SS is 75 mV/decade, and at 300°C, it is 187 mV/decade. These values are near the SS limits of 60 mV/decade and 110 mV/decade at 25°C and 300°C, respectively. The SS for high temperature operation is a critical parameter because it is expected to deteriorate linearly with temperature and represents the change in voltage required to transition from cut-off to saturation mode. The $g_{m,max}$ and the magnitude of V_{Th} both decrease with increasing temperature. The $g_{m,max}$ decreases with increasing temperature at a rate proportional to $T^{-0.97}$. Generally, $g_{m,max}$ is expected to deteriorate at a rate of $T^{-1.5}$, due to mobility

degradation at the same rate. The slower degradation of transconductance with temperature is attributed to the decrease in the magnitude of V_{Th}, which creates a competing effect.

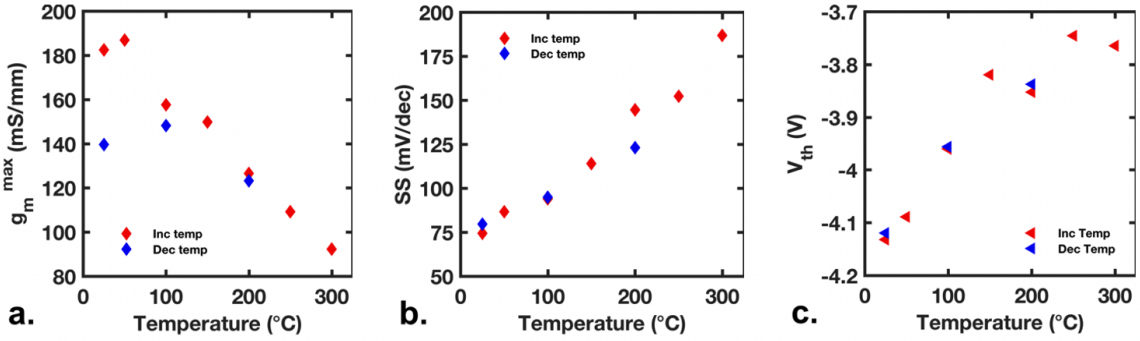

Figure 4.5: Max transconductance (a), subthreshold swing (b), threshold-voltage (c), vs. temperature.

To protect the MoO_3 gate, several passivation schemes were tested including atomic layer deposition (ALD) of SiO_2 and Al_2O_3. The MoO_3 gates were damaged by the precursors during ALD processing and no devices survived for testing. This illustrates the fragile nature of the MoO_3, and careful design of passivation schemes is needed to leverage the MoO_3 system at elevated temperatures. Additionally, the MoO_3 was passivated with 50 nm PECVD silicon nitride (SiN) and survived. Testing the passivated MoO_3-gated HEMT up to 500°C the device survived. However, the leakage decreased even above the leakage of the as-deposited Mo-gated devices. The on-off ratios were 7.6×10^3 at RT, 110 at 300°C, and 15 at 500°C. It has been shown that SiN creates extra leakage paths at the passivation-III-nitride interface and through the barrier layer bulk, causing an increase in gate leakage current [113,114]. This work initially aimed to utilize the same material platform previously demonstrated by Maier *et al.* by leveraging Mo as the gate and SiN for passivation on InAlN/GaN heterostructures [34]. This work was done in air, a more extreme environment to the vacuum used in the Maier work. This work illustrates that when operating in air it is not enough to simply leverage Mo because MoO_3 volatilizes in the presence of air without passivation. However, SiN leakage paths must also be reduced for high ON/OFF ratio and high temperature operation.

4.2.4 Conclusions

High ON/OFF drain current ratios were found for d-mode MoO_3-gated InAlN/GaN HEMTs of 1.2×10^8 at 25°C and 1.2×10^5 at 300°C in air. Catastrophic device failure seen at 400°C in air is believed to be due to rapid volatilization of the oxidized molybdenum gate in the presence of water vapor. XPS results show that the electron-beam evaporated Mo is oxidized even without high temperature exposure after several weeks in air. It is confirmed with AES that only trace amounts of molybdenum remain on the surface of the InAlN layer after exposure to 400°C. The addition of SiN passivation enabled device operation up to 500°C but reduced the ON/OFF ratio by 5 orders of magnitude. While the results of MoO_3-gated InAlN/GaN HEMTs in air are promising for their low leakage and high ON/OFF ratio, the volatilization of the oxidized molybdenum in the presence of water vapor needs to be prevented through careful passivation choice.

4.3 Analyzing IrO_x-gated HEMT Behavior up to 600°C

4.3.1 Motivation

The purpose of this experiment was to determine the effects of geometry and passivation on the operation of InAlN/GaN HEMTs with novel IrO_x gates at temperatures exceeding the 400°C limit of the MoO_3-gated HEMTs, as well as to determine the maximum temperature limit of this class of devices in an oxidizing ambient.

4.3.2 Experimental Methods

For this purpose, one die each of Casper Run sample type #1 and sample type #7, henceforth referred to as Sample A and Sample B, were selected for testing (see Table 3.3 for details). Both samples have IrO_x gates; the primary difference is that Sample A is passivated with Al_2O_3 and Sample B is unpassivated or bare. The room temperature electrical properties of the 2DEG were measured on both samples using Hall-effect devices with van der Pauw geometry. For Sample A and Sample B respectively, the sheet resistances at room temperature were 280 $\Omega/\square$ and 293 $\Omega/\square$, the carrier mobilities were 831 $cm^2/V{\cdot}s$ and 917 $cm^2/V{\cdot}s$, and the sheet electron densities were 2.68×10^{13} cm^{-2} and 2.32×10^{13} cm^{-2}.

Three C-HEMTs on each sample were tested. The devices had critical dimension L_G = 5 μm, and L_{CH} = 10, 15, or 20 μm, respectively. One L-HEMT device on each sample, with

gate centered between source and drain and the same critical dimension L_G =5 μm, was also tested. The L-HEMT channel width and length were 100 μm and 20 μm, respectively. The InAlN/GaN samples were placed inside of the Signatone open air probe station on the surface of the heated chuck. Current-voltage measurements were collected at various step points during temperature cycling from 25°C to 600°C and back using an Agilent B1500A semiconductor parameter analyzer. The temperature reported in the plots is the chuck temperature measured by the internal thermocouple. The sample surface temperature was estimated by monitoring the resistance of platinum thin film resistance temperature detectors (RTD) adhered with epoxy to the surface of dummy InAlN/GaN-on-Si die also situated on the heated chuck. The chuck was held at each temperature of interest for approximately 10 minutes prior to data collection to allow for the die surface to reach thermal equilibrium. The probe station dark box door was closed during the experiment and the samples were not illuminated. $C-V$ measurements were performed on the Schottky diodes at 25°C prior to heating.

4.3.3 Results and Discussion

C-HEMTs:

Figure 4.6 and Figure 4.7 show the transfer and output characteristics of Sample A C-HEMTs with varying L_{CH} during heating from 25°C to 600°C and upon return to 25°C. The output characteristics were normalized by W_{eff} according to 3.2. Two interesting phenomena are apparent. First, the I_D has increased upon return to 25°C compared to the initial value. Second, the ON/OFF ratio is degraded upon return to 25°C due to larger $I_{D,off}$ in the cut-off regime. The device also appears to suffer from current collapse after the high temperature exposure. Figure 4.8 and Figure 4.9 show the transfer and output characteristics of Sample B C-HEMTs. All 3 of the devices fail to operate at 600°C and do not recover upon return to 25°C, indicating permanent device failure. Loss of gate control can be seen in the transfer characteristics. While the L_{CH} = 10 μm device demonstrates the most severe degradation with no drain current flow at 600°C, the larger L_{CH} = 20 μm device maintains a small drain current at 600°C. This implies a geometric effect on the high temperature device performance. These results show that the C-HEMT devices must be passivated in order to operate at temperatures as high as 600°C. The failure mechanism in the unpassivated devices is likely induced by oxidation and may include further oxidation of the IrO_x gate material into different oxide species.

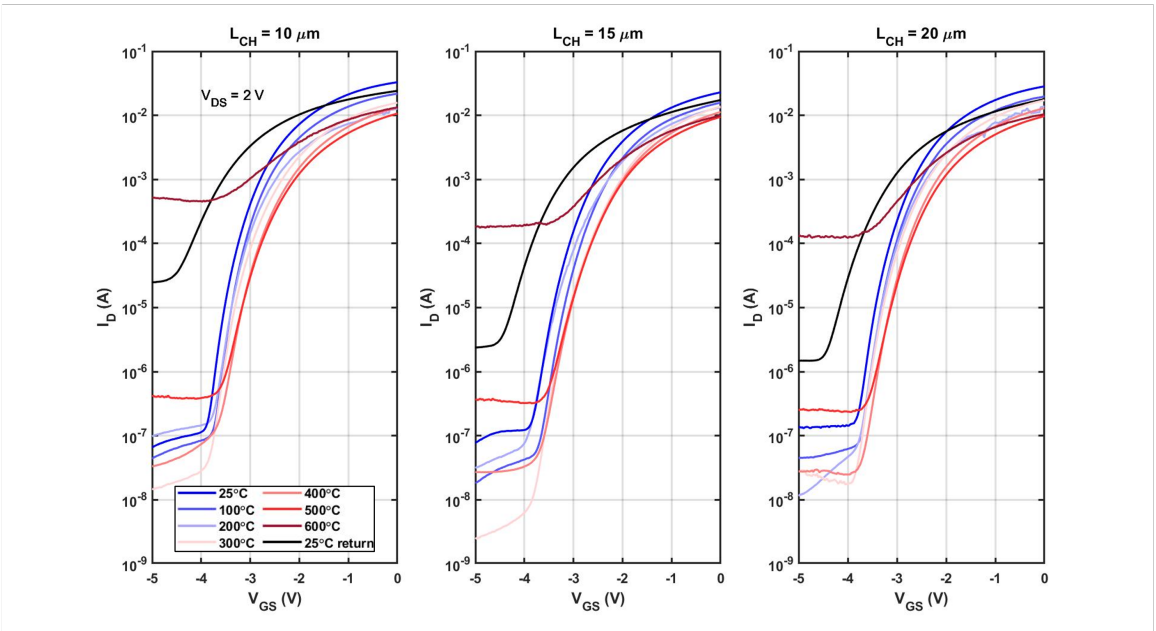

Figure 4.6: Sample A transfer characteristics of the 10 μm (left), 15 μm (middle), and 20 μm (right) channel length C-HEMTs up to 600°C in air.

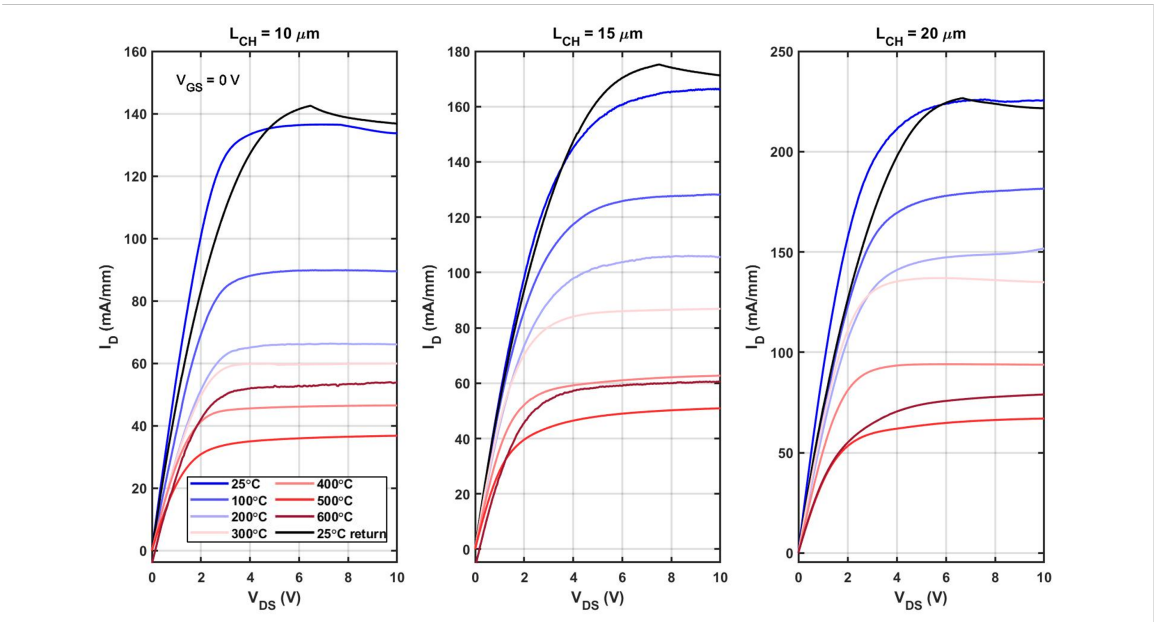

Figure 4.7: Sample A output characteristics of the 10 μm (left), 15 μm (middle), and 20 μm (right) channel length C-HEMTs up to 600°C in air.

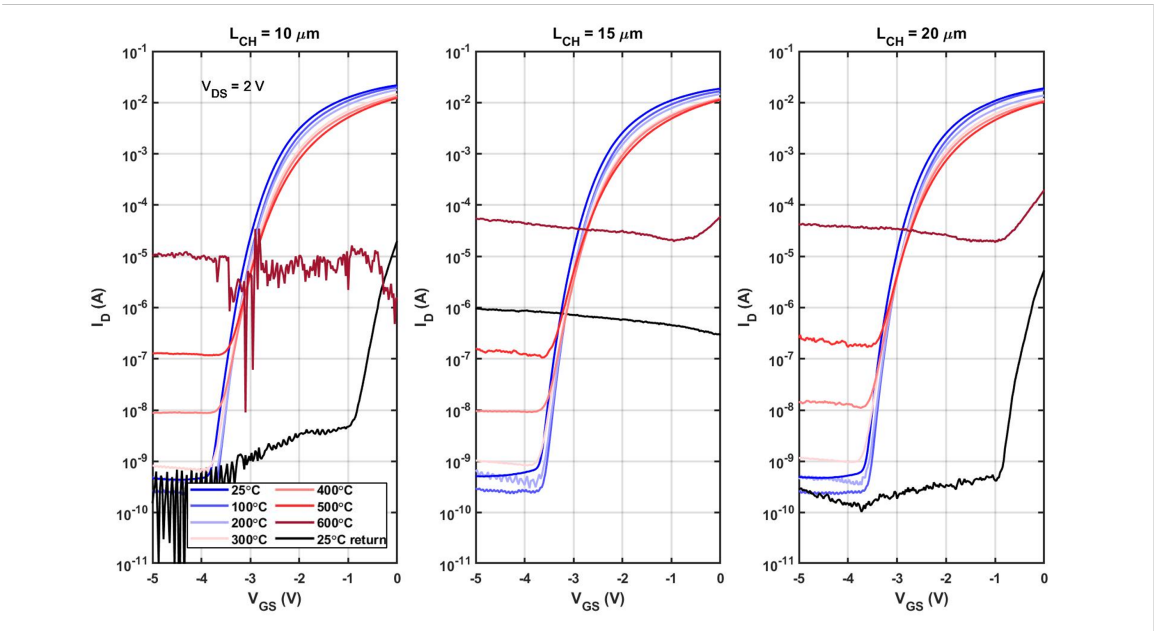

Figure 4.8: Sample B transfer characteristics of the 10 μm (left), 15 μm (middle), and 20 μm (right) channel length C-HEMTs up to 600°C in air.

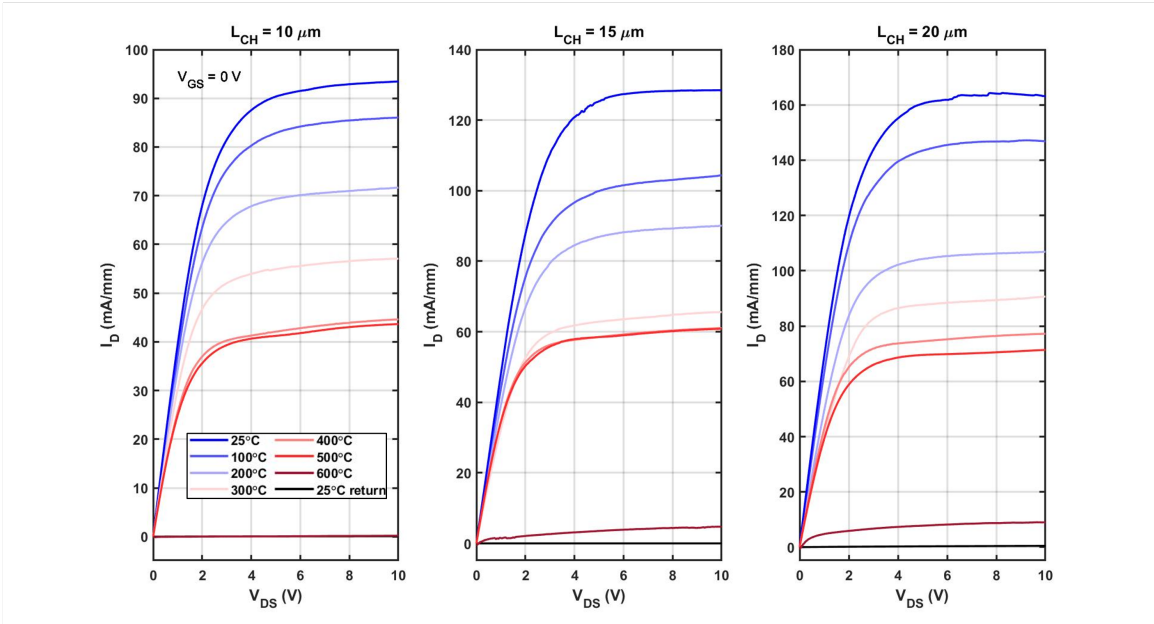

Figure 4.9: Sample B output characteristics of the 10 μm (left), 15 μm (middle), and 20 μm (right) channel length C-HEMTs up to 600°C in air.

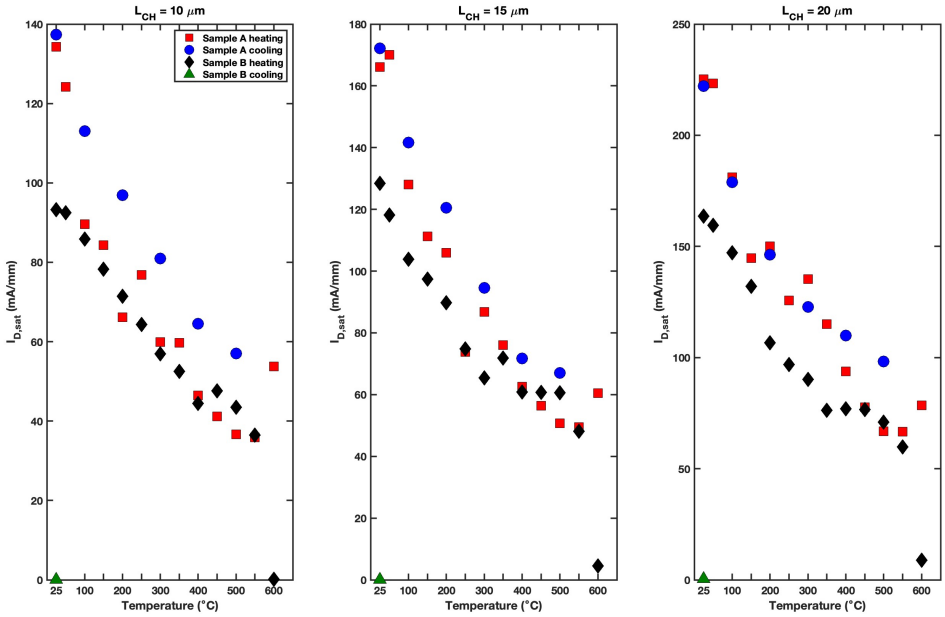

Figure 4.10: $I_{D,sat}$ of Sample A and Sample B 10 μm (left), 15 μm (middle), and 20 μm (right) channel length C-HEMTs during heating up to 600°C and cooling back down to 25°C in air.

The extracted $I_{D,sat}$ during heating and cooling for both Sample A and Sample B C-HEMTs are shown in Figure 4.10. Because Sample B C-HEMTs were not working at 600°C, cooling characteristics were not collected on the way back down to room temperature. Only the 25°C return data was collected on this subset of devices. The addition of Al_2O_3 passivation layer causes an increase in the sheet electron density, and corresponding reduction in the sheet resistance, resulting in an larger drain saturation current in Sample A versus Sample B devices at room temperature. The decline in the drain saturation current with high temperature in both samples is largely due to the decrease in electron mobility in InAlN/GaN due to increased scattering, as well as a decrease in the saturation carrier velocity [4]. The temperature dependency of $I_{D,sat}$ can be expressed as [115]:

$$I_{D,sat} = I_{D,sat0} \times T^{\alpha} \tag{4.2}$$

where $I_{D,sat0}$ is the value of $I_{D,sat}$ at 25°C and α is the temperature coefficient. Generally, it is expected that $\alpha \approx$-1.5, which is the rate of mobility degradation with temperature. The

α value of Sample A C-HEMTs with different channel lengths L_{CH} = 10, 15, and 20 μm is -1.186, -1.191, and -1.098 respectively, during heating. The larger channel length device displays the weakest current dependence on temperature.

Figure 4.11 shows the threshold voltage for Sample A and Sample B as a function of temperature. The sheet carrier density variation induces differences in the threshold voltage. The higher n_s in the passivated Sample A devices results in a larger magnitude V_{Th} at room temperature in order to modulate the channel and turn the device off. The positive shift in threshold voltage at high temperature is caused by the decrease in $I_{D,sat}$, while the subsequent increase in $I_{D,sat}$ during cooling seen in Figure 4.10 explains the negative V_{Th} shift during cooling.

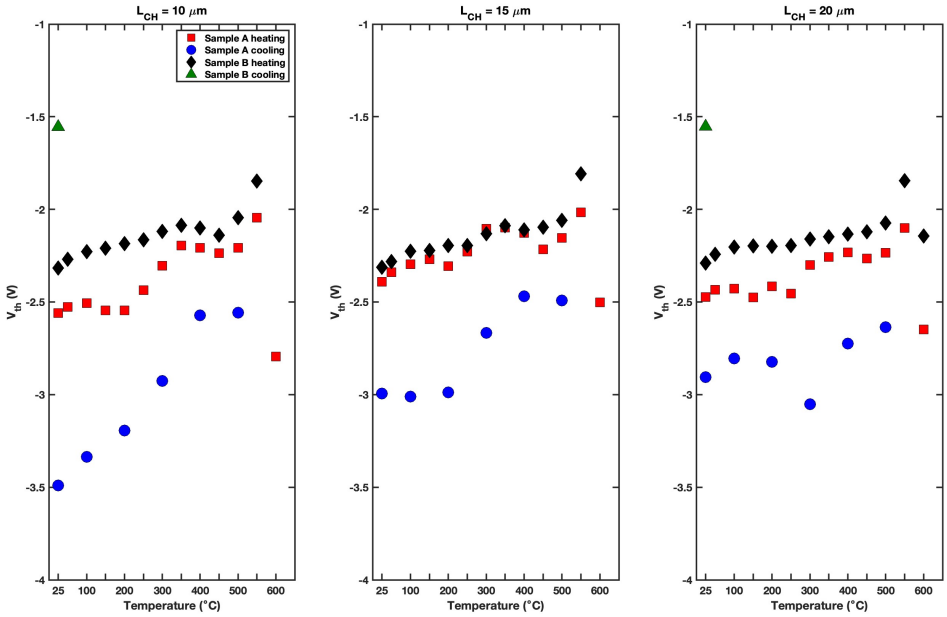

Figure 4.11: V_{Th} of Sample A and Sample B 10 μm (left), 15 μm (middle), and 20 μm (right) channel length C-HEMTs during heating up to 600°C and cooling back down to 25°C in air.

The extracted ON/OFF ratio ($I_{D,on}/I_{D,off}$) and OFF-current ($I_{D,off}$) of the Sample A and Sample B C-HEMTs over the temperature cycle are shown in Figure 4.13 and Figure 4.14, respectively. The ON/OFF ratio decreases with temperature due to increasing drain OFF-current. Increasing $I_{D,off}$ could be due to the increased conductivity of the GaN

buffer with increasing temperature, which causes buffer layer leakage [34, 116].

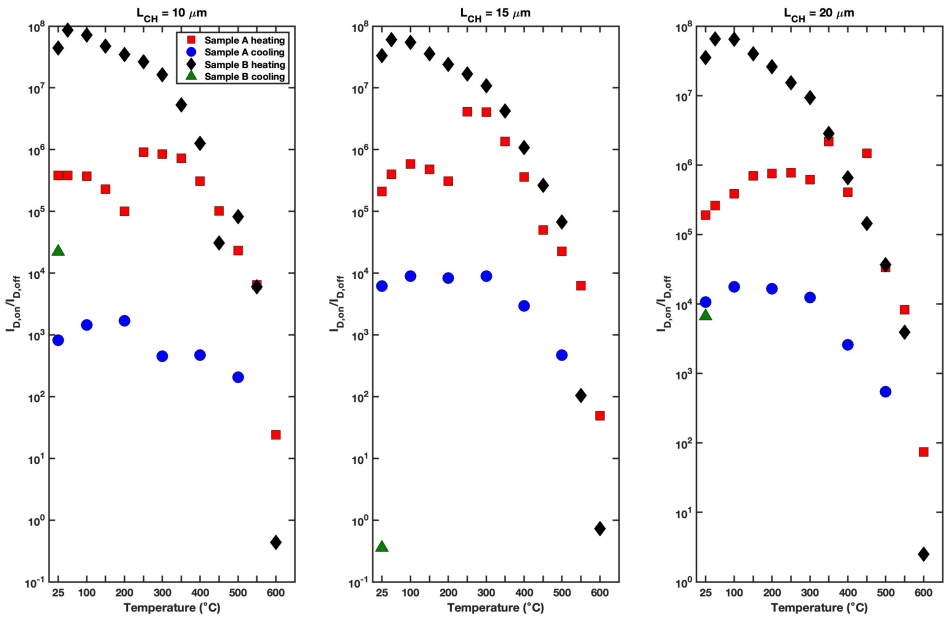

Figure 4.12: $I_{D,on}/I_{D,off}$ of Sample A and Sample B 10 μm (left), 15 μm (middle), and 20 μm (right) channel length C-HEMTs during heating up to 600°C and cooling back down to 25°C in air.

Figure 4.14 shows I_G extracted in the cut-off mode during heating and cooling for the C-HEMTs on both samples. Sample A devices have higher gate leakage originally, indicating that surface passivation leakage may be contributing. The gate leakage currents in Sample A and Sample B devices increase with temperature, with less temperature dependency seen at temperatures above 400°C in the Sample A C-HEMTs. The detailed investigation into the IrO_x gate leakage current transport mechanisms and Schottky barrier heights up to 500°C is reported in Section 4.4. During cooling, the Sample A C-HEMTs exhibit less pronounced I_G temperature dependency. In the $L_{CH} = 10$ μm C-HEMT, the gate leakage current during cooling is less than during heating at temperatures above 300°C, while in the $L_{CH} = 15$ μm C-HEMT I_G during cooling is less than during heating at temperatures above 200°C. In the $L_{CH} = 20$ μm C-HEMT, the gate leakage currents are all smaller during cooling than during heating. This I_G trend dependency on geometry indicates that surface leakage currents may play an important role in the Al_2O_3 passivated Sample A devices, or

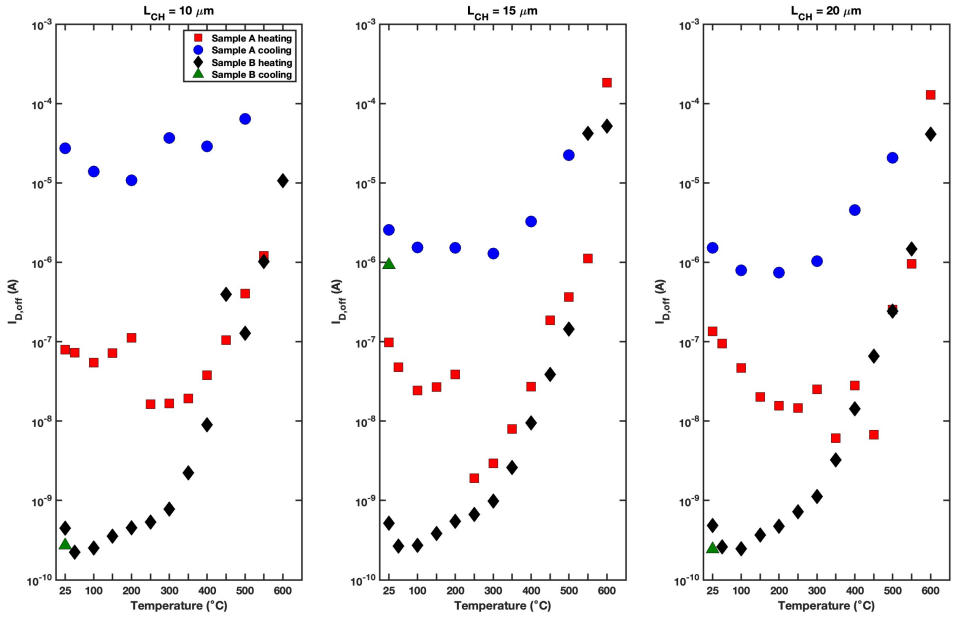

Figure 4.13: $I_{D,off}$ of Sample A and Sample B 10 μm (left), 15 μm (middle), and 20 μm (right) channel length C-HEMTs during heating up to 600°C and cooling back down to 25°C in air.

a virtual gate effect is occurring.

L-HEMTs:

Figure 4.15 and Figure 4.16 shows the transfer and output characteristics of L-HEMTs on Sample A and Sample B, respectively, during heating from 25°C to 600°C and upon return to 25°C. Both the passivated (Sample A) and unpassivated (Sample B) L-HEMTs fail at high temperature. The Sample A L-HEMT fails at 600°C and does not recover normal transfer characteristics upon return to 25°C such that it could be reliably implemented into a circuit. The Sample B L-HEMT begins to fail 400°C and no longer operates as a switch at 600°C and also does not recover normal function upon return to room temperature.

4.3.4 Conclusions

The Sample A C-HEMT devices were found to operate at 600°C in air for 10 minutes and upon return to RT, with degraded performance. The Sample B C-HEMTs failed to demonstrate channel modulation capabilities and drain currents were significantly reduced

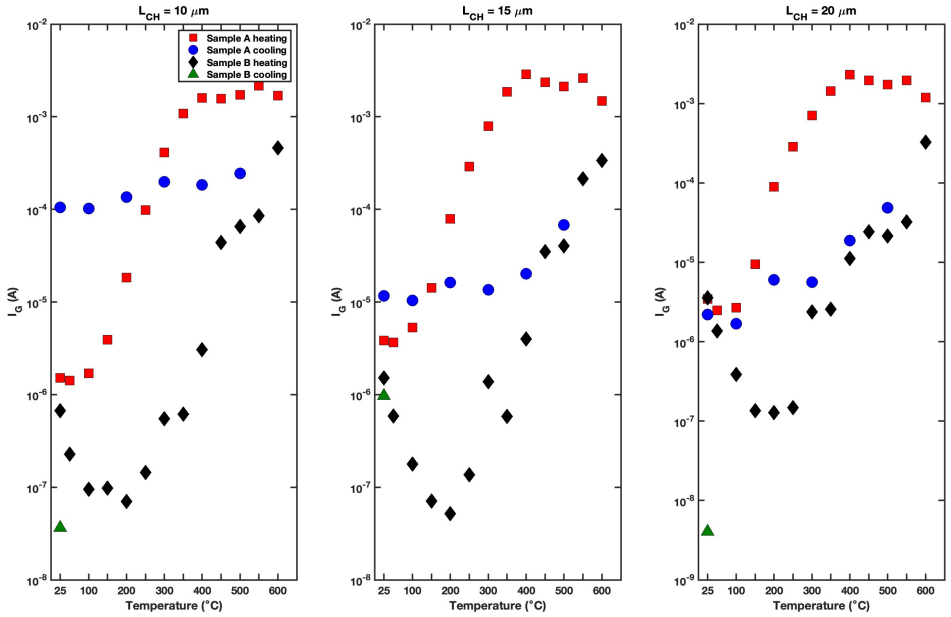

Figure 4.14: I_G of Sample A and Sample B 10 μm (left), 15 μm (middle), and 20 μm (right) channel length C-HEMTs during heating up to 600°C and cooling back down to 25°C in air.

at high temperature, suffering permanent device failure at 600°C. Neither Sample A nor Sample B L-HEMTs operated at 600°C, and neither recovered upon return to RT. These results show that Al_2O_3 passivation, and the circular HEMT geometry, are superior for high temperature oxidizing ambient operation, and demonstrate the viability of IrO_x Schottky contacts for use on extreme environment InAlN/GaN HEMTs with careful choice of passivation and geometry. This platform is promising for Venus surface applications because the surface temperature of 464°C is well within the operable temperature range of the Sample A C-HEMTs.

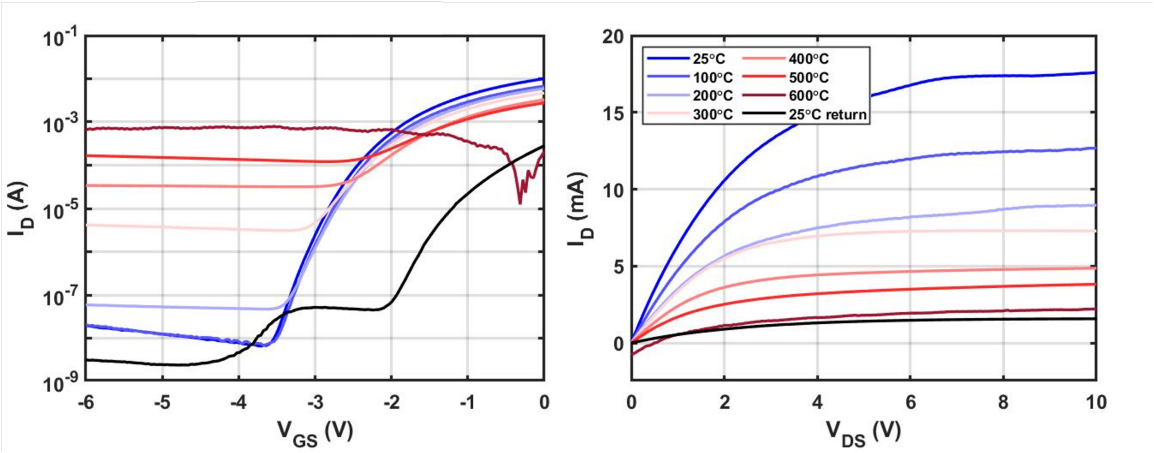

Figure 4.15: Sample A L-HEMT transfer (left) and output (right) characteristics up to 600°C in air.

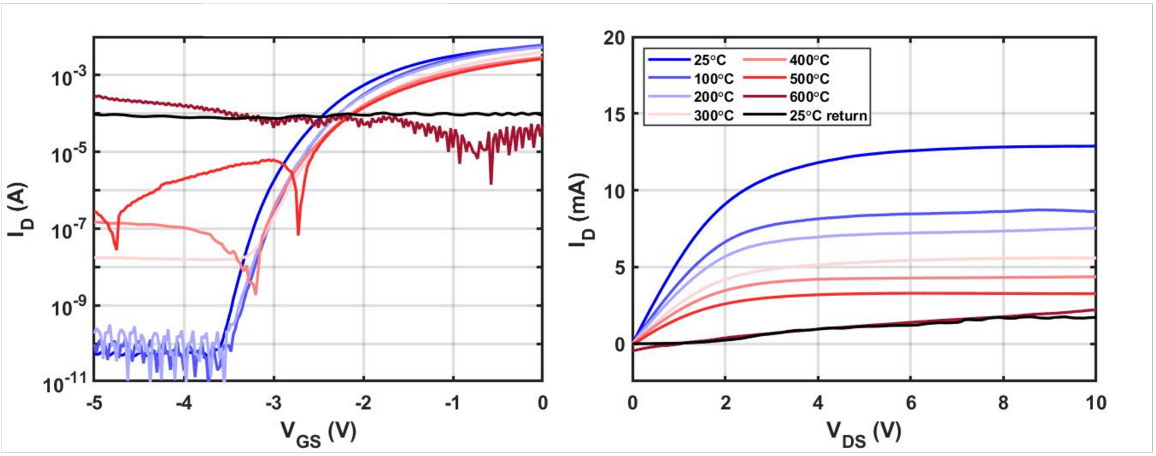

Figure 4.16: Sample B L-HEMT transfer (left) and output (right) characteristics up to 600°C in air.

4.4 Investigation of IrO_x Schottky Barrier Contacts up to 500°C

4.4.1 Motivation

High excess reverse leakage current through the Schottky gate remains a lingering performance challenge for HEMT operation in high-field and high-temperature conditions

[117–119]. The adverse effects of high leakage currents include large off-state power consumption, decreased linearity in high-power amplifiers, and enhanced burden on drive circuitry due to limited range of the gate voltage swing. Elucidating the quality of the barrier interface, as well as the dominant gate leakage mechanisms and their temperature dependencies, is critical to further progress this device and material platform performance for hot environment applications. This section reports the investigation of barrier height and current transport mechanisms in InAlN/GaN Schottky barrier diodes with intentionally oxidized iridium oxide (IrO_x) gate contacts across a wide temperature range.

4.4.2 Introduction

A wide range of Schottky barrier heights to InAlN/GaN structures have been reported in the literature. A phenomenon frequently reported in Schottky contacts to InAlN is experimental barriers height that are significantly lower than theoretical barrier heights predicted by Vegard's law [120]. For Ni-based Schottky contacts to InAlN, reported barrier height values vary between 0.63-2.43 eV at room temperature [120–124]. Room temperature barrier heights in Pt-InAlN and Pd-InAlN Schottky contacts are reported to be 0.84-2.9 eV and 2.12 eV, respectively [122, 125, 126]. The large discrepancy in reported values can be partially attributed to whether the study considered the influence of Schottky barrier inhomogeneity, which is discussed in detail later in this section. Accurate extraction of the Schottky barrier height is necessary to evaluate the potential of the gate electrode material for HEMT applications, where minimized leakage current and maximized drain current, transconductance, and breakdown voltage are required.

Several investigations of the gate leakage mechanisms in InAlN/GaN Schottky contacts have been reported. Turuvekere *et al.* identified Poole-Frenkel emission as the primary gate leakage mechanism in InAlN/GaN HEMTs at low to medium reverse bias and Fowler-Nordheim tunneling as the dominant gate leakage mechanism beyond the threshold voltage [127]. The authors also identified significant trap-assisted tunneling current in the region near zero bias. Ganguly *et al.* formulated a modified Poole-Frenkel model that considers polarization fields to explain gate current transport in InAlN/GaN HEMTs at lower reverse bias, while Fowler-Nordheim tunneling was identified as the main current component at high reverse bias [128]. Arslan *et al.* observed a nearly temperature-independent tunneling current via dislocations intersecting the space-charge region at low forward bias [121]. Poole-Frenkel emission in InAlN/GaN HEMTs operated in reverse bias was also reported by

Arslan *et al.* [129]. Kotani *et al.* found the reduction of dislocation density effective in reducing leakage current originating from Poole-Frenkel emission in the low reverse bias region, but no similar reduction in leakage at high bias where field-enhanced emission was dominant [130]. Liang *et al.* have identified trap-assisted tunneling as the main process of reverse current transport in ultrathin InAlN/GaN HEMTs [131]. Lugani *et al.* reported two leakage mechanisms in reverse-biased InAlN/GaN Schottky diodes: trap-assisted tunneling and, in thicker barrier layers, Fowler-Nordheim tunneling [132]. These investigations of gate leakage currents in InAlN/GaN structures are limited in temperatures $\leq$ 102°C (≈375 K) [118, 121, 128, 129], $\leq$ 200°C (≈473 K) [127, 131], and $\leq$ 300°C (≈573 K) [130].

In this study, we extend the temperature range of investigation of Schottky contacts to InAlN/GaN structures up to 500°C (773 K) to give detailed information about the Schottky barrier height and current transport mechanisms at temperatures of interest to extreme environment applications. To this end, we have fabricated large-area InAlN/GaN Schottky diodes with intentionally oxidized iridium (IrO_x) gate electrodes. IrO_x is a conductive metal oxide with a high work function. Lalinsky *et al.* reported the high temperature stability of IrO_2-gated AlGaN/GaN HEMTs subjected to 450°C ambient air for 24 hours [95]. The authors of this article have previously studied the improved performance of IrO_x-gated InAlN/GaN HEMTs after 10-day exposure to simulated Venus surface conditions (460°C, supercritical CO_2 ambient, 92 bar) [133]. Here, we report the first detailed study on the current transport mechanisms of the IrO_x Schottky gate interface to a GaN heterostructure. Towards this end, the current-voltage characteristics of IrO_x/InAlN/GaN Schottky diodes are measured at various temperatures from 25°C to 500°C in air. The Schottky barrier height is evaluated considering inhomogeneity at the IrO_x-InAlN interface by assuming a double Gaussian distribution. Conventional and modified Richardson plots are analyzed to verify this methodology. Various current transport mechanisms, including trap-assisted tunneling, Poole-Frenkel emission, and Fowler-Nordheim emission have been modeled and fit to the experimental data at reverse bias. Their associated parameters are extracted and discussed in detail.

4.4.3 Experimental Methods

The Schottky diodes are Casper Run sample type #1 (see Table 3.3 for details). Schottky diodes are fabricated on a lattice-matched $In_{0.18}Al_{0.82}N$/AlN/GaN-on-Si wafer grown via MOCVD (Table 3.1) The circular device active region was defined by a BCl_3/Cl_2 inductively

coupled reactive ion mesa etch. Ti/Al/Mo/Au (15/60/35/50 nm) metals were evaporated, lifted off, and annealed in N_2 at 850°C for 30 s to form the ring-shaped Ohmic contact around the perimeter. Next, a 15-nm-thick film of Ir was evaporated, lifted off, and intentionally oxidized at 800°C for 1 min in O_2 to form a concentric, circular Schottky gate contact. Lalinsky *et al.* found these oxidation process conditions to form IrO_2 throughout the entire resulting 25-30 nm gate contact thickness on AlGaN/GaN HEMTs [95]. Here, we refer to the gate electrode stack as IrO_x because the exact oxide composition of the intentionally oxidized iridium stack was not verified. The transformation of the Ir contact into IrO_2 on AlGaN films proceeds from the top down towards the semiconductor interface during the oxidation process [95]. At the temperature of oxidation (800°C), oxygen has a long diffusion length in Ir, which is highly reactive [96]. In addition to the top-down oxidation process occurring from the O_2 ambient, it can be assumed that at such high temperatures the Ir near the interface is simultaneously reacting with any adsorbed oxygen that was present on the InAlN surface. At the IrO_2/AlGaN interface, an IrO_2 and Ga_2O_3 interlayer is formed [95]. The Ga_2O_3 interlayer cannot be present in InAlN due to the absence of Ga. This implies that no interlayer is formed and the contact is homogeneous IrO_2. However, other studies have shown that a very thin (1-2 nm) "nearly native" Al_2O_3 is formed during 800°C O_2 annealing of unmasked InAlN [134]. This thin Al_2O_3 interlayer has been employed as gate oxide insulation in HEMTs, which can improve the gate leakage current of Schottky contacts [135]. Due to the high temperature of oxidation required to form this aluminum oxide interlayer, the layer is considered thermally stable at the lower experimental temperatures reported here (≥500°C), and changes in Schottky barrier height cannot be attributed to interlayer material changes. Therefore, we conclude that if such an Al_2O_3 interlayer has formed in addition to the IrO_2, it could be a contributing factor to the high thermal stability of the Schottky contacts investigated in this work.

The devices were blanket passivated by 25 nm of Al_2O_3 deposited via atomic layer deposition. Finally, the passivation was selectively wet etched, and Ti/Au (15/200 nm) was evaporated and lifted off over the Ohmic and Schottky regions to allow for electrical contact and probing via bond pads (BP). Figure 4.17 shows a top-view optical image of the microfabricated diode and the cross-sectional device schematic, annotated with dimensions.

Current-voltage ($J-V$) measurements from −7 to +3 V were conducted on the diodes across a wide temperature range from 25°C to 500°C in air on a Signatone probe station. The InAlN/AlN/GaN-on-Si die was placed directly onto the surface of a heated chuck, and

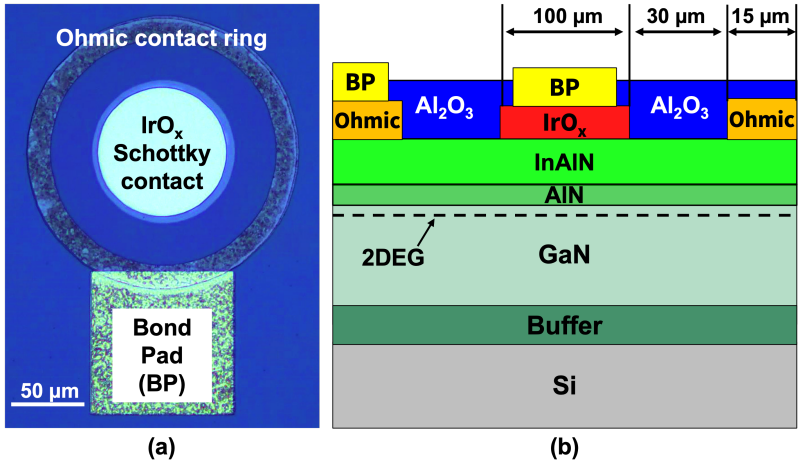

Figure 4.17: Top-view optical image of the microfabricated IrO_x/InAlN/GaN Schottky diode (a) and cross-sectional device diagram with dimensions (b).

the chuck was held at each temperature for approximately 10 minutes prior to data collection to allow for the die surface to reach thermal equilibrium. The probe station dark box door was closed during the experiment and the diodes were not illuminated. Capacitance-voltage $(C-V)$ measurements were performed at 25°C prior to heating.

4.4.4 Results and Discussion

The $(J-V-T)$ response of the IrO_x/InAlN/GaN Schottky diodes across the temperature range is shown in Figure 4.18. Several current transport mechanisms are identified, and their various dominant operating regions are labeled on the plot. The presence of each mechanism is detected and validated by applying the corresponding transport model to the experimental data. The modeling procedure and associated extracted parameters for each current transport mechanism are discussed in detail in the following sections.

Region I - Thermionic emission

Values for the Schottky barrier height (SBH) and ideality factor are calculated for each temperature by analyzing the current density in low forward bias. The current transport mechanism in this region is assumed to be thermionic emission (TE), which is the transport of thermally activated carriers with energy greater than or equal to the conduction band energy at the Schottky interface. The TE process is depicted in the conduction band edge

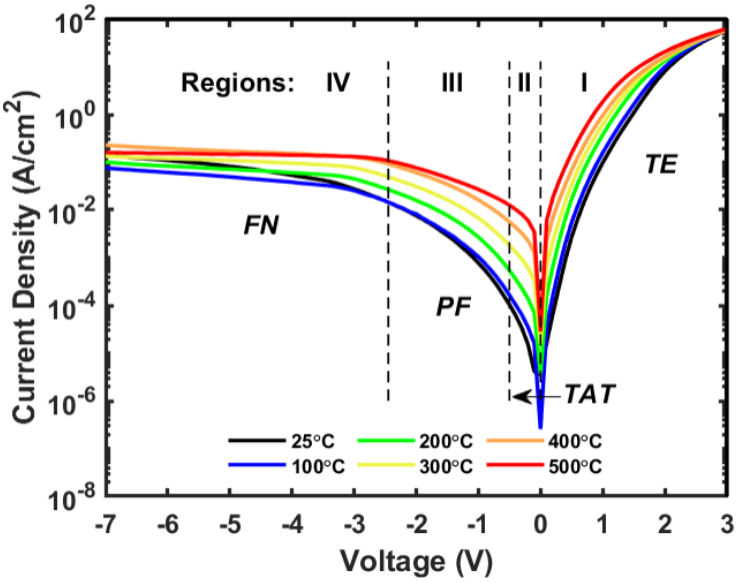

Figure 4.18: Measured $J-V$ characteristics of the Schottky diode from 25°C to 500°C. The dominant current transport mechanisms and their associated regions are labeled.

diagram in Figure 4.19, and the region where TE dominates current flow is labeled Region I on Figure 4.18. TE-induced current can be described by the ideal diode equation [127],

$$J_{TE} = J_0 \left[\exp\left(\frac{qV}{nk_BT}\right) - 1 \right] \tag{4.3}$$

where J_0 is the reverse saturation current density, n is the ideality factor, q is the charge of an electron, k_B is the Boltzmann constant, and T is the absolute temperature. The reverse saturation current density is:

$$J_0 = A^* T^2 \exp\left(-\frac{q\phi_{ap}}{k_BT}\right) \tag{4.4}$$

where A^* is the effective Richardson constant (55.7 $A \cdot cm^{-2} \cdot K^{-2}$ for InAlN), and ϕ_{ap} is the apparent SBH calculated using this method. By neglecting the last term, Equation 4.3 can be rearranged and the TE current density approximated,

$$\ln\left(J_{TE}\right) \approx \ln\left(J_0\right) + \frac{qV}{nk_BT} \tag{4.5}$$

when $V > 3k_BT$. Figure 4.20 shows the plot of $\ln(J_{TE}) - V$ from 25°C to 500°C. Linear

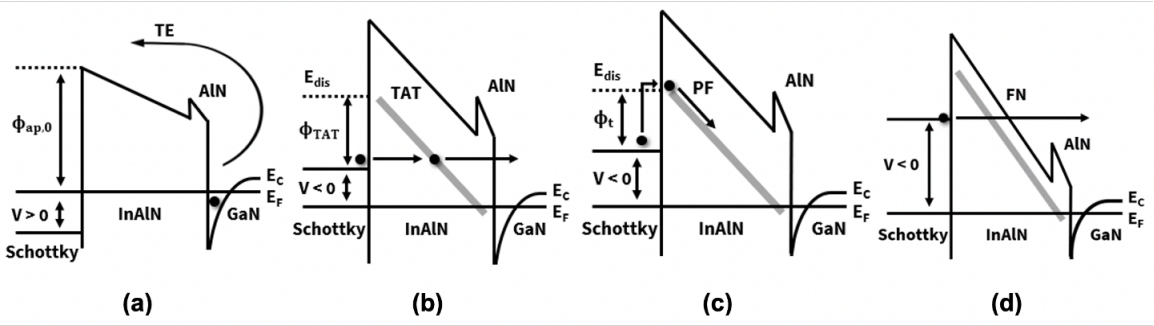

Figure 4.19: Conduction band edge diagrams of current transport mechanisms in IrO_x/InAlN/GaN Schottky diode. Thermionic emission (TE) at forward bias ($V > 0$) is shown in (a); trap-assisted tunneling (TAT) shown in (b), Poole-Frenkel (PF) emission shown in (c), and Fowler-Nordheim (FN) tunneling shown in (d) are dominant in the low, medium, and high reverse bias ($V < 0$) regions, respectively. Continuum of states is depicted by the gray line.

fitting is performed at low forward bias where the effects of series resistance are small and the current exponentially increases as predicted by Equation 4.3. Current saturation due to series resistance can be seen at higher biases in Region I on Figure 4.18. As predicted by Equation 4.5, the experimental data in Figure 4.20 shows good linearity across the temperature range, demonstrating the validity of assuming the prevalence of thermionic emission in this region (e.g., $J \approx J_{TE}$). The intercepts and slopes of the linear fits yield values for J_0 and n, respectively. Figure 4.20 inset shows the variation of J_0 with temperature. The apparent SBH can then be calculated,

$$\phi_{ap} = \frac{k_B T}{q} \ln\left(\frac{A^* T^2}{J_0}\right) \tag{4.6}$$

The variation of the SBH and ideality factor across temperature obtained from the $J_{TE} - V - T$ analysis is shown in Figure 4.21. The values for ϕ_{ap} increase from 0.67 eV to 1.48 eV between 25°C and 500°C. The values for n decrease from 4.13 to 2.54 between 25°C and 500°C. The inset of Figure 4.21 shows ϕ_{ap} versus n. The inset data display two clear distinct linear trends with temperature, which are denoted Range A in the moderate temperature regime between 25°C to 200°C (≈300 K to 473 K), and Range B in the high temperature regime from 300°C to 500°C (573 K to 773 K).

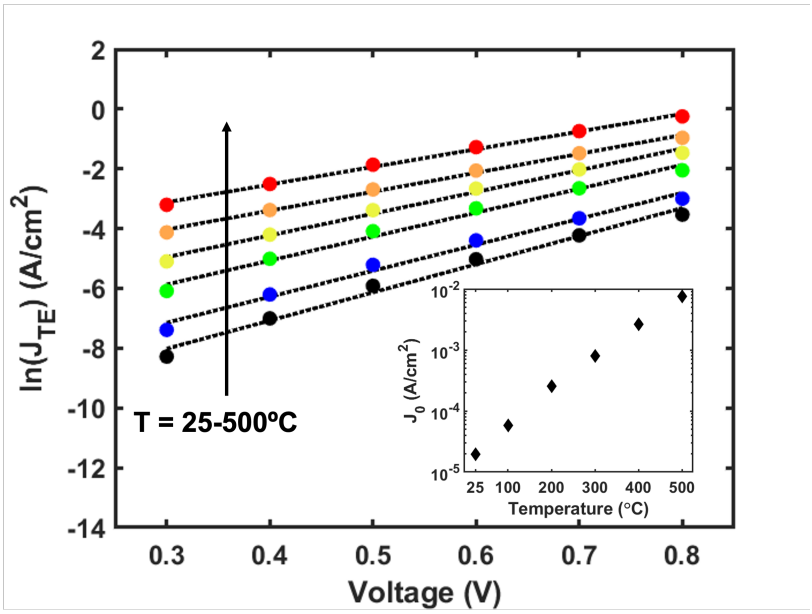

Figure 4.20: Thermionic emission plot $\ln(J_{TE}) - V$ from 25°C to 500°C. Experimental data are shown as circles. Linear fits are represented as dotted lines. Inset shows the measured reverse saturation current values, J_0, versus temperature.

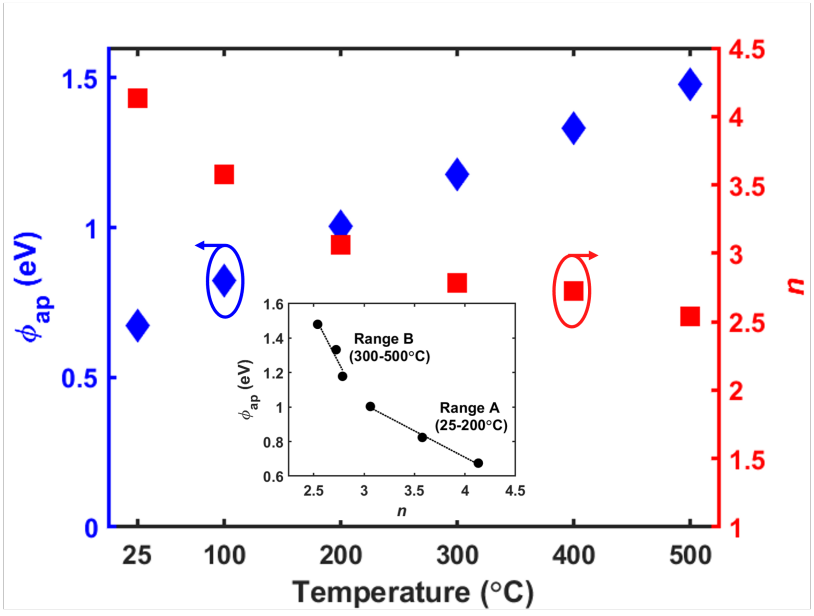

Figure 4.21: Apparent barrier height, ϕ_{ap}, and ideality factor, n, from 25°C to 500°C obtained from the $J_{TE} - V - T$ analysis. The inset shows ϕ_{ap} versus n, which has two distinct linear regions. Linear fits are represented as dotted lines.

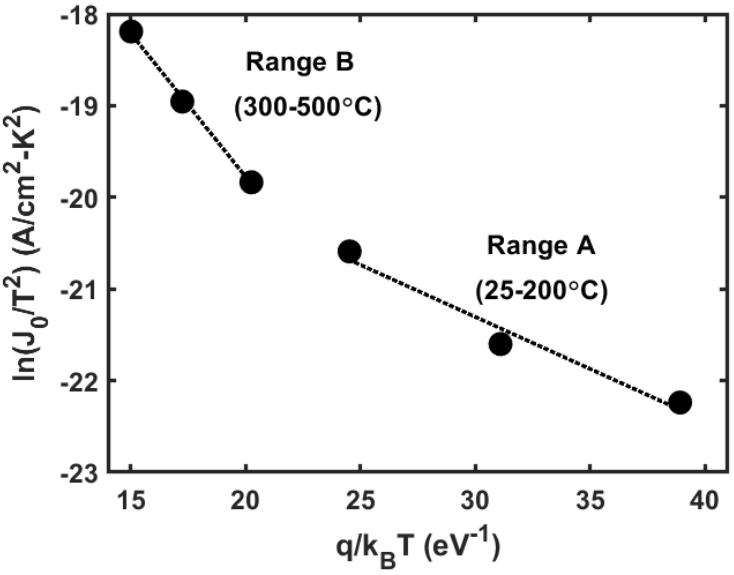

Figure 4.22: The conventional Richardson plot $\ln(J_0/T^2)$ versus q/k_BT. Linear fits are represented as dotted lines.

Another common method used to calculate the SBH is to utilize a conventional Richardson plot based upon the Richardson-Dushman equation,

$$\ln\left(\frac{J_0}{T^2}\right) = -\frac{q\phi_R}{k_BT} + \ln(A^*). \tag{4.7}$$

This equation is based upon an Arrhenius-style analysis where ϕ_R is the activation energy required for electrons to surmount a barrier of that height at the Schottky junction. The conventional Richardson plot $\ln(J_0/T^2)$ versus q/k_BT is shown in Figure 4.22. In agreement with the ϕ_{ap} versus n plot in the Figure 4.21 inset, two distinct trends corresponding to temperature Range A and Range B are seen in the conventional Richardson plot in Figure 4.22. Table 4.1 lists values for the Richardson constant A^* and barrier height ϕ_R extracted from the linear fits of Figure 4.22 data in Range A and B. The effective Richardson constants in both ranges are orders of magnitude lower than the theoretical value of 55.7 $A \cdot cm^{-2} \cdot K^{-2}$ for InAlN [120]. The barrier heights are also much lower than the apparent values calculated and shown in Figure 4.21 and indicative of an Ohmic contact, which cannot physically be the case here due to the rectifying behavior evident in the $J-V-T$ characteristics in Figure 4.18. Therefore, the effects of Schottky barrier inhomogeneity are considered and

Range	**Temperature (°C)**	ϕ_R **(eV)**	A^* $(A \cdot cm^{-2} \cdot K^{-2})$
A	25-200	0.11	1.68×10^{-8}
B	300-500	0.31	1.35×10^{-6}

Table 4.1: Conventional Richardson plot extracted parameters

further explained in the next section.

Schottky Barrier Inhomogeneity

The low effective Richardson constants extracted from Figure 4.22 as well as the observed increase in ϕ_{ap} and decrease in n with increasing temperature as seen in Figure 4.21 are both indications of Schottky barrier inhomogeneity (SBI) in III-N structures [136–138]. SBI refers to the lateral spatial non-uniformity of barrier height across the Schottky-semiconductor interface. SBI in III-N devices has been attributed to the presence of quantum dot-like structures on the barrier surface [126], alloy composition fluctuation in the barrier layer [136], surface trap states [139], metal oxide formation at the M−S interface [139, 140], and voids under the Schottky contact [141]. SBI has also been reported to depend on the gate metal or material chosen [140]. In the case of the IrO_x/InAlN Schottky interface, inhomogeneity is unsurprising because the imperfect nature of the contact is two-fold: the interface is not atomically perfect because the Ir metal was evaporated and not epitaxially grown onto the InAlN barrier layer, and TEM on intentionally oxidized IrO_x gates show the existence of polycrystalline grain boundaries within the oxide [95]. Material variations at the interface will cause local variation in the electric field, and therefore non-uniform barrier height. At low to moderate temperatures, current transport will be dominated by lower energy electrons. At higher temperatures, electrons are sufficiently thermally energized to be able to cross at higher height barrier locations. This is the cause of the apparent increase in ϕ_{ap} with increasing temperature. Because n is an indicator of the interface quality and should approach unity in the case of a perfect Schottky junction, SBI can also explain the decrease of n with increasing temperature. At higher temperatures, current will flow more uniformly through the contact since the electrons will have sufficient thermal energy to cross higher barrier height patches, effectively increasing the area of the contact.

To describe SBI, a Gaussian distribution of low and high barrier height spots, which reflects the variation in electric field potential at the Schottky-semiconductor interface, can

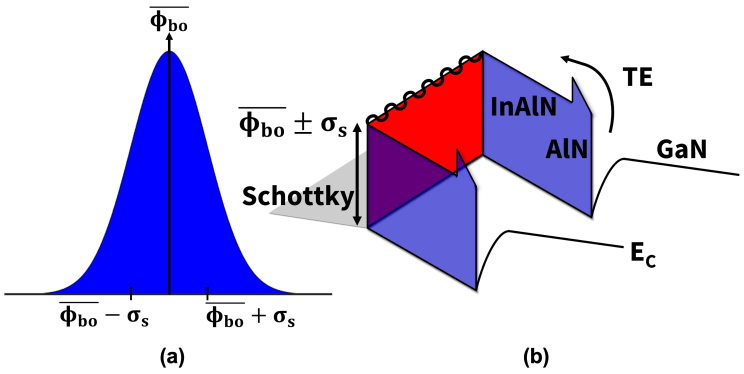

Figure 4.23: Gaussian probability distribution of barrier heights (a) and conduction band edge diagram depicting barrier inhomogeneity (b).

be applied [142, 143]. This phenomenon has been experimentally confirmed in III-N structures [144]. The Gaussian distribution function describing the barrier height inhomogeneity is [137, 145],

$$P(\phi_B) = \frac{1}{\sigma_s\sqrt{2\pi}} \exp\left[-\frac{\left(\phi_B - \overline{\phi_{bo}}\right)^2}{2\sigma_s^2}\right] \tag{4.8}$$

where $\overline{\phi_{bo}}$ is the mean barrier height and σ_s is the standard deviation. Figure 4.23 depicts the Gaussian probability distribution of barrier heights and conduction band edge diagram with barrier inhomogeneity. The reverse saturation current density can then be modified to include the Gaussian probability function,

$$J_s = \int J_0(\phi_B) P(\phi_B) d\phi_B \tag{4.9}$$

where $J_0(\phi_B)$ is the reverse saturation current from a single barrier height. Substituting Equations 4.4 and 4.8 into Equation 4.9 and carrying out the integration over all barrier heights yields,

$$J_s = A^* T^2 \exp\left(-\frac{q\phi_{ap}}{k_B T}\right). \tag{4.10}$$

The apparent barrier height and ideality factor are then taken:

$$\phi_{ap} = \overline{\phi_{bo}} - \frac{q\sigma_s^2}{2k_B T} \tag{4.11}$$

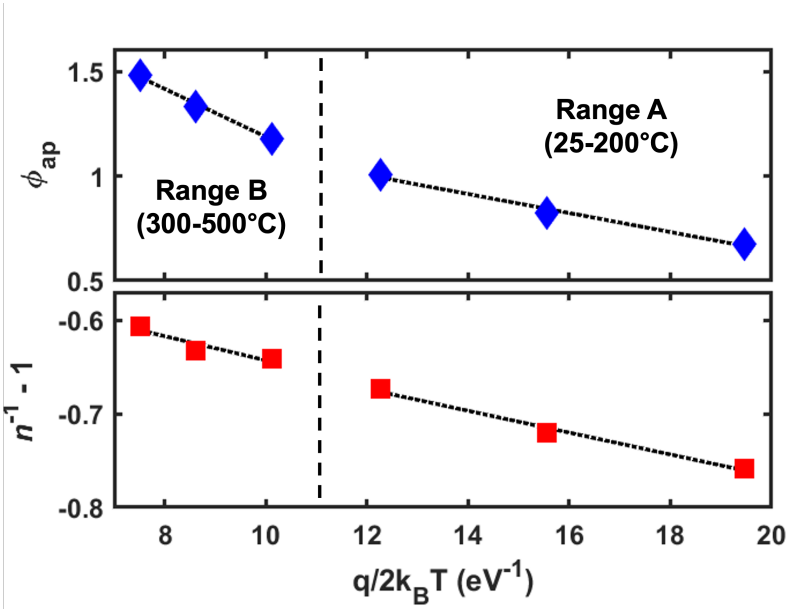

Figure 4.24: ϕ_{ap} and $n^{-1} - 1$ versus $q/2k_BT$ plots. Linear fits are represented as dotted lines.

Range	**Temperature (°C)**	$\overline{\phi_{bo}}$ **(eV)**	σ_s **(eV)**	ρ_2 **(eV)**	ρ_3 **(eV)**
A	25-200	1.55	0.21	0.53	0.01
B	300-500	2.33	0.34	0.51	0.01

Table 4.2: Gaussian distribution analysis extracted parameters

$$n^{-1} - 1 = \rho_2 - \frac{q\rho_3}{2k_BT}. \tag{4.12}$$

ϕ_{ap} and $n^{-1} - 1$ are both plotted versus $q/2k_BT$ in Figure 4.24. The intercepts and slopes of the fits of ϕ_{ap} versus $q/2k_BT$ yield values for $\overline{\phi_{bo}}$ and σ_s, respectively, in Range A and B. Likewise, the fit of $n^{-1} - 1$ versus $q/2k_BT$ gives values for ρ_2 and ρ_3, which are voltage coefficients that quantify the barrier height distribution deformity with applied bias. Table 4.2 lists the extracted values of $\overline{\phi_{bo}}$, σ_s, ρ_2, and ρ_3 for temperature Ranges A and B. The values of ρ_2 and ρ_3 are similar between the temperature ranges, implying the voltage coefficients are largely temperature independent. The standard deviation σ_s is an indication of the homogeneity of the barrier, which is 13.8% of the barrier height in Range A and 14.5% of the barrier height in Range B.

After finding the Gaussian distribution parameters, Equations 4.4 and 4.10 can be used

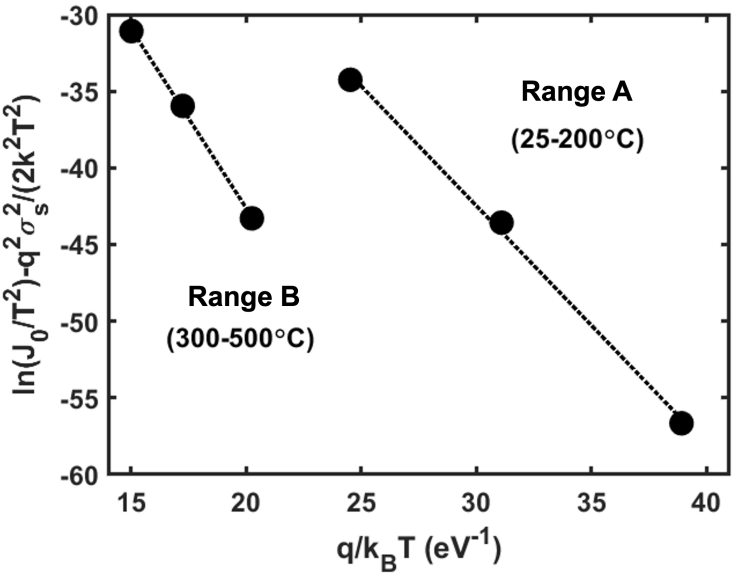

Figure 4.25: Modified Richardson plot. Linear fits are represented as dotted lines.

to construct a modified Richardson plot [137],

$$\ln\left(\frac{J_0}{T^2}\right) - \frac{q^2\sigma_s^2}{2\left(k_BT\right)^2} = \ln\left(A^*\right) - \frac{q\overline{\phi_{bo}}}{k_BT}. \tag{4.13}$$

The modified Richardson plot shown in Figure 4.25 exhibits good linearity in both ranges. Extracted parameters are listed in Table 4.3. The barrier heights calculated from the slope of the modified Richardson plot shown in Figure 4.25 are in good agreement with the mean barrier heights calculated from the Gaussian distributions using Equation 4.11: 1.56 eV and 1.55 eV in the moderate temperature Range A, and 2.34 eV and 2.33 eV in the high temperature Range B. The A^* values calculated from the intercept of the fits in the modified Richardson plot in Figure 4.25 are shown Table 4.3. Unlike the A^* values calculated from the conventional Richardson plot and listed in Table 4.1, the A^* values calculated from the intercepts of the fits in the modified Richardson plot are close to the theoretical value for InAlN of 55.7 $A \cdot cm^{-2} \cdot K^{-2}$. The discrepancy between the theoretical A^* value of 55.7 $A \cdot cm^{-2} \cdot K^{-2}$ and calculated A^* values of 75.62 $A \cdot cm^{-2} \cdot K^{-2}$ and 61.87 $A \cdot cm^{-2} \cdot K^{-2}$ in Ranges A and B could be due to discrepancies between the theoretical effective mass (m_n^*=0.3 to 0.4m_0 for InAlN) and the experimental effective mass [146]. The

Range	Temperature (°C)	$\overline{\phi_{bo}}$ (eV)	A^* ($A \cdot cm^{-2} \cdot K^{-2}$)	m_n^*
A	25-200	1.56	75.62	$0.63m_0$
B	300-500	2.34	61.87	$0.51m_0$

Table 4.3: Modified Richardson plot extracted parameters

experimental effective mass is calculated in each range using the below equation,

$$A^* = \frac{4\pi q m_n^* k_B^2}{h^3} \tag{4.14}$$

where h is Planck's constant. The calculated m_n^* values are listed in Table 4.3.

The feasible A^* values yielded by the modified Richardson plot analysis suggests that the IrO_x/InAlN/GaN Schottky diode behavior is accurately described by a double Gaussian distribution of Schottky barrier heights to account for SBI. Furthermore, literature supports the application of multiple Gaussian distributions to capture unique behavior across temperature ranges in III-N devices [145].

Region II - Trap-Assisted Tunneling

In the reverse bias regime, the contribution of thermionic emission to gate leakage is assumed trivial due to the large barrier heights found above. Instead, a variety of other current transport mechanisms are evaluated in Regions II-IV shown in Figure 4.18. At very low reverse bias, trap-assisted tunneling (TAT) has been shown to dominate in InAlN devices [127]. TAT is the defect-assisted tunneling of electrons from the Schottky contact through a band of localized trap states in the InAlN barrier. The energy band diagram depicting the TAT mechanism is shown in Figure 4.19 and the region where the TAT model is applied is labeled Region II on Figure 4.18. The current density due to TAT is given by [147],

$$\ln(J_{TAT}) = \ln(C_1) - \frac{C_2}{E} \tag{4.15}$$

where C_1 is a temperature-dependent parameter and

$$C_2 = \frac{8\pi\sqrt{2qm_n^*}}{3h}\phi_{TAT}^{\frac{3}{2}} \tag{4.16}$$

where ϕ_{TAT} is the energy level below the conduction band edge corresponding to the trap. The plot of $\ln(\phi_{TAT})$ versus $1/E$ is shown in Figure 4.26. The goodness of the linear fit

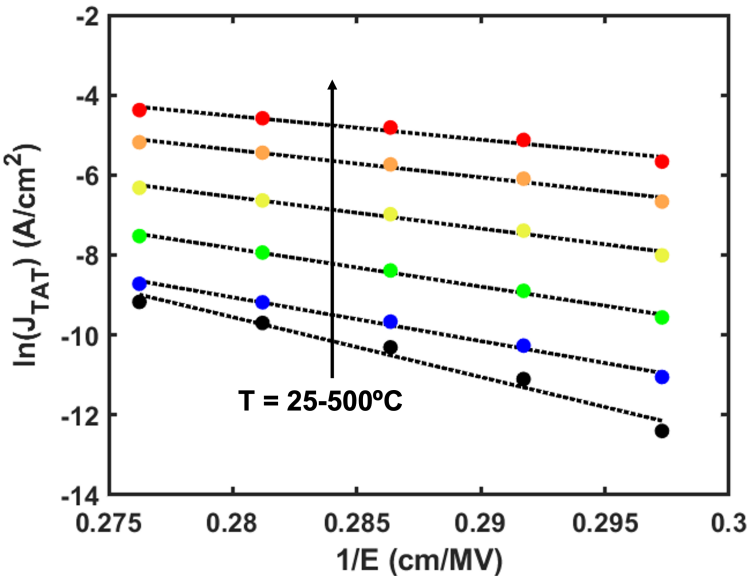

Figure 4.26: Trap-assisted tunneling plot $\ln(J_{TAT})$ versus $1/E$. Experimental data are shown as circles. Linear fits are represented as dotted lines.

increases with temperature, which can be expected due to the temperature dependency of this mechanism. As evidenced by Equation 4.15, the intercept of the linear fit to experimental data in Figure 4.26 gives a value for C_2. Equation 4.16 is rearranged to calculate ϕ_{TAT} values across temperature. The extracted ϕ_{TAT} are listed in Table 4.4 and correspond well with the range for InAlN/GaN HEMTs reported in literature of 1.2 eV to 4.55 eV [131]. The trap energy level decreases with increasing temperature because thermally energized electrons require less electrical energy to be activated, and the width of the forbidden band decreases with increase in temperature [131]. It has been hypothesized that structural defects caused by N vacancies in the InAlN barrier may be responsible for TAT current [148].

Region III - Poole-Frenkel Emission

Poole-Frenkel (PF) emission is another trap-assisted tunneling model that describes the thermal emission of electrons from the Schottky material or trap levels in the barrier very close to the Schottky material Fermi level into a continuum of states in the barrier layer that exist due to conductive dislocations. PF emission is strongly influenced by temperature and field strength. PF has been shown to dominate current transport in InAlN/GaN HEMTs at medium reverse bias, where the reverse bias magnitude approaches but remains less than

Temperature (°C)	ϕ_{TAT} (eV)
25	2.52
100	2.04
200	1.87
300	1.64
400	1.50
500	1.36

Table 4.4: Trap-assisted tunneling (TAT) energy levels across the temperature range

the threshold voltage (e.g., $|V_R| < |V_{TH}|$) [127–129]. The energy band diagram depicting PF emission is shown in Figure 4.19 and the bias range where PF dominates is labeled Region III on Figure 4.18. To quantify PF emission, the vertical electric field strength across the barrier must be found using the equation [127],

$$E = \frac{q\left(\sigma_b - n_s\right)}{\varepsilon_r \varepsilon_0}. \tag{4.17}$$

Here, $\sigma_b = P_{InAlN} - P_{GaN} \approx 2.8 \times 10^{13}\ cm^{-2}$ is the bound polarization charge at the heterointerface, n_s is the carrier concentration of the two-dimensional electron gas (2DEG), $\varepsilon_r = 9.8$ is the static dielectric constant for InAlN, and ε_0 is the vacuum permittivity [122, 149–151]. To find the 2DEG concentration, $C-V$ measurements were conducted on the Schottky diodes at 25°C and 10 kHz. The 2DEG density was calculated as a function of applied voltage by integrating [152],

$$n_s = \int \frac{C}{qA} dV. \tag{4.18}$$

The calculated $E-V$ is shown in Figure 4.27. $C-V$ experimental data and the calculated 2DEG density are displayed in the Figure 4.27 inset. The threshold voltage, V_{TH}, is the x-intercept of the tangent to the steepest part of the $C-V$ curve, which is -3.1 V. With increasing reverse bias, the 2DEG is depleted until n_s approaches zero at the threshold. Thus, the electric field, and subsequently the current, saturate at reverse biases larger or equal to the threshold voltage (e.g., $|V_R| \geq |V_{TH}|$).

The current density due to PF emission is described [127],

$$J_{PF} = CEexp\left[-\frac{q}{k_B T}\left(\phi_t - \sqrt{\frac{qE}{\pi \varepsilon_i \varepsilon_0}}\right)\right] \tag{4.19}$$

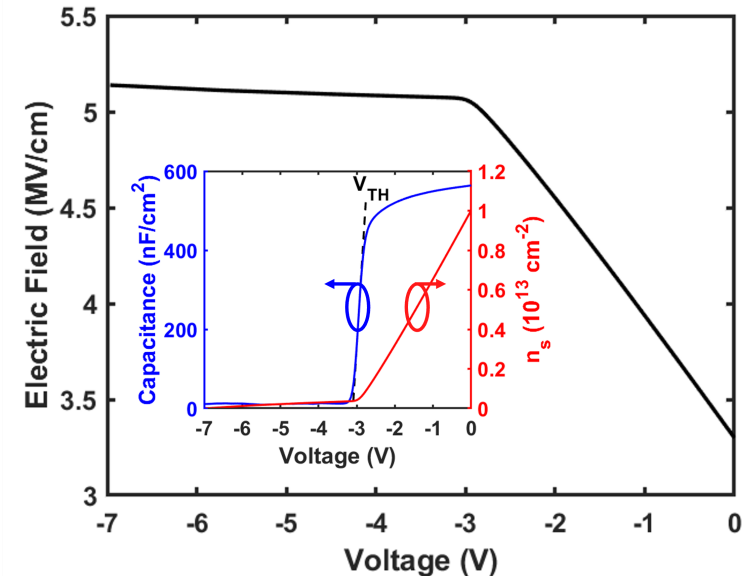

Figure 4.27: Calculated electric field as a function of voltage $(E-V)$ plot. $C-V$ experimental data and the calculated 2DEG density are displayed in the inset.

where C is a constant, ϕ_t is the activation energy for trap-assisted emission, and ε_i is the high-frequency dielectric permittivity. Rearranging Equation 4.19 and assuming PF emission dominates, $\ln(J_{PF}/E)$ should be a linear function of $\sqrt{E}$,

$$\ln\left(\frac{J_{PF}}{E}\right) = m\,(T)\,\sqrt{E} + c\,(T) \tag{4.20}$$

with

$$m\,(T) = \frac{q}{k_B T}\sqrt{\frac{q}{\pi\varepsilon_i}} \tag{4.21}$$

$$c\,(T) = -\frac{q\phi_t}{k_B T} + \ln(C). \tag{4.22}$$

Figure 4.28 shows $\ln(J_{PF}/E)$ versus $\sqrt{E}$ across temperature. The plot has three distinct linear regions based on the strength of the electric field: low-field, mid-field, and high-field. Using 4.20, values for $c(T)$ and $m(T)$ were extracted from the linear fits in each region. Figure 4.29 displays $c(T)$ and $m(T)$ values versus q/k_BT, and linear fits in the high-temperature and mid-temperature ranges are represented by dashed lines. Multiple field-dependent PF regions, and two temperature ranges, were similarly found by Zhu *et*

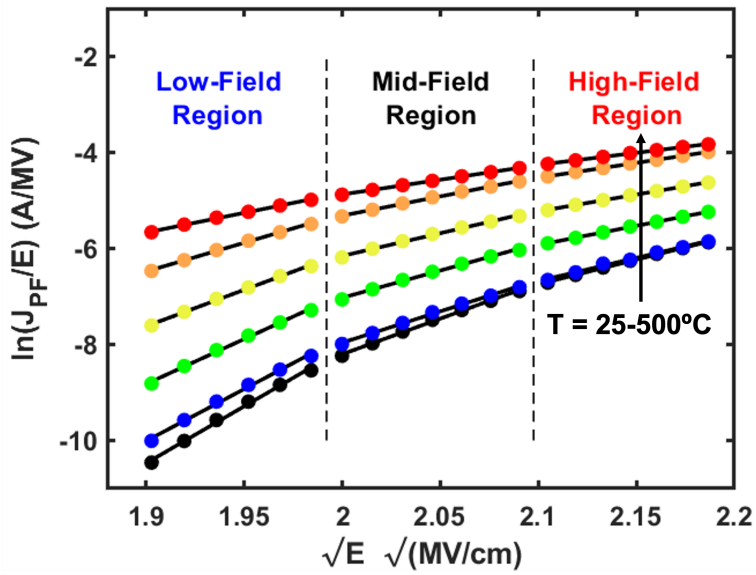

Figure 4.28: Poole-Frenkel emission plot $\ln(J_{PF}/E)$ versus $\sqrt{E}$. The plot has three distinct regions: low-field, mid-field, and high-field. Linear fits are represented as dotted lines.

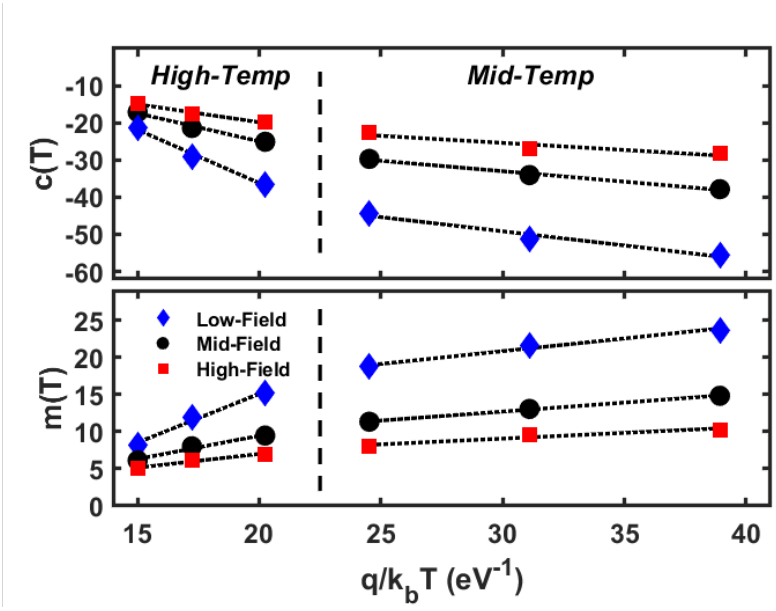

Figure 4.29: Extracted c_T and m_T values versus q/k_BT. Low-field, mid-field, and high-field values are shown, and linear fits are represented as dotted lines.

Temperature (°C)	Low-Field ϕ_t (eV)	Mid-Field ϕ_t (eV)	High-Field ϕ_t (eV)
25-200	0.76	0.56	0.38
300-500	2.87	1.51	0.97

Table 4.5: Poole-Frenkel (PF) emission activation energies.

al. on Al_2O_3/AlGaN/GaN HEMTs [153]. Weaker temperature dependency in the mid-temperature range indicates PF emission may be less dominant at moderate temperatures, where other trap-assisted mechanisms may be playing a role [153]. From 4.22, values of ϕ_t are calculated using the slope of the $c(T)$ versus q/k_BT fits in Figure 4.29 and listed in Table 4.5. At low fields and higher temperature PF emission is via deep traps (e.g., large ϕ_t), while at high fields and moderate temperature emission is via shallower traps. Reported PF trap activation energies in the literature are for Ni-based Schottky contacts to InAlN and vary from 0.12 eV to 0.65 eV at temperatures ≤473 K [127,129,131,147]. These values correspond to the ϕ_t values extracted in the mid-temperature range in this study (≈300 K to 473 K) of 0.38 eV to 0.76 eV.

From Equation 4.21, the high-frequency dielectric constant, ε_i, is calculated in the high-field region where PF emission is strongest and is found to be 5.79. This is close to the reported experimental ε_i of InAlN of ≈6.2 (between $\varepsilon_{AlN} = 4.77$ and $\varepsilon_{InN} = 8.4$) [128]. It can be concluded that PF emission is dominant in Region III of Figure 4.18 from the linearity of the fits in Figure 4.29, ϕ_t values in the mid-temperature regime that align with reported values from other studies, the strong temperature and field dependency of ϕ_t, and ε_i value that is close to reported experimental and theoretical values.

Region IV - Fowler-Nordheim Tunneling

Fowler-Nordheim (FN) tunneling describes the transport of electrons through the barrier via quantum tunneling [154]. At large reverse biases approaching and exceeding the threshold voltage (e.g., $|V_R| \geq |V_{TH}|$), the large electric field across the InAlN barrier effectively thins to a triangular potential well such that electrons can easily tunnel through to the 2DEG channel and contribute to current flow. The energy band diagram depicting FN tunneling is shown in Figure 4.19 and the region where FN tunneling is dominant is labeled Region IV on Figure 4.18. The saturation of the current at larger reverse biases in Region IV of Figure 4.18 is due to saturation of the vertical electrical field as shown in Figure 4.27.

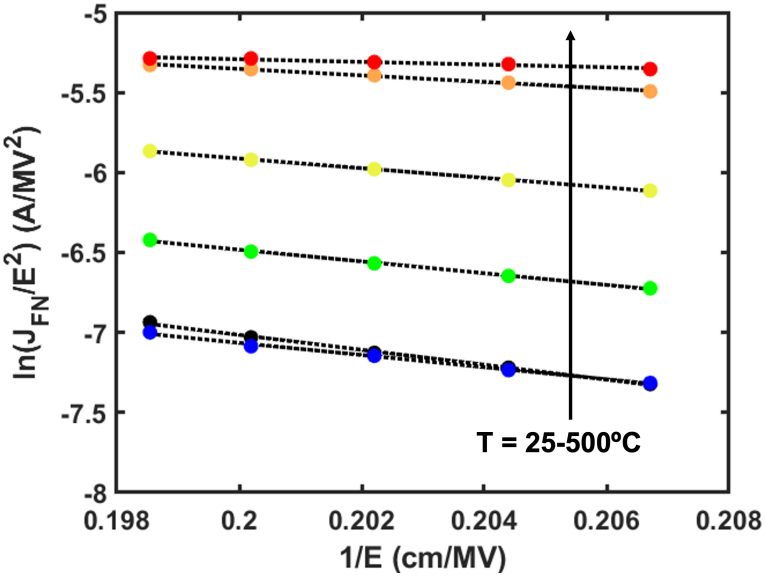

Figure 4.30: Fowler-Nordheim tunneling plot $\ln\left(\frac{J_{FN}}{E^2}\right)$ versus $1/E$. Experimental data are shown as circles. Linear fits are represented as dotted lines.

For ideal FN tunneling, the current density can be described [155, 156],

$$J_{FN} = \alpha E^2 \exp\left(-\frac{\beta}{E}\right) \tag{4.23}$$

where α is a proportionality constant and

$$\beta = \frac{8\pi}{3qh}\sqrt{2m_n^*\phi_{eff}^3} = 6.83 \times 10^7 \left(\frac{m_n^*}{m_0}\right)^{\frac{1}{2}} (\phi_{eff})^{\frac{3}{2}}. \tag{4.24}$$

Rearranging Equation 4.23 yields

$$\ln\left(\frac{J_{FN}}{E^2}\right) = \ln(\alpha) - \frac{\beta}{E}. \tag{4.25}$$

By constructing and applying a linear fit to the $\ln\left(\frac{J_{FN}}{E^2}\right)$ versus $1/E$ plot displayed in Figure 4.30, values for α and β are found. The extracted β value and Equation 4.24 are then used to calculate an effective barrier height for tunneling, ϕ_{eff}, in eV. The calculated ϕ_{eff} values across temperature are listed in Table 4.6. The average ϕ_{eff} value extracted over the temperature range is 0.71 eV, with standard deviation 0.24 eV. This is

Temperature (°C)	ϕ_{eff} (eV)
25	0.98
100	0.85
200	0.83
300	0.73
400	0.56
500	0.31

Table 4.6: Effective barrier heights for FN tunneling across the temperature range.

in line with ϕ_{eff} values in the literature for InAlN/GaN that range from 0.62 eV to 2.3 eV [127, 128, 147, 148]. Despite Equation 4.23 containing no temperature-dependent term, the extracted effective tunneling height decreases with increasing temperature. Previous studies have similarly shown a reduction in barrier height for tunneling with increasing temperature in GaN HEMTs and broadly MOS structures [157, 158]. Additionally, the FN equation requires the assumption of a value of effective mass, which in this case is $0.3m_0$, to calculate ϕ_{eff}. However, because the temperature swing is so wide in this experiment, we propose the value of effective mass in InAlN may be expected to change significantly as has been shown in AlGaN/GaN heterostructures [159].

Reverse Leakage Current Model

Using the relevant extracted parameters and Equations 4.15, 4.19, and 4.23, the TAT, PF, and FN currents were modeled as a function of electric field and displayed in Figure 4.31. The electric field strength range corresponds to the reverse bias Regions II, III, and IV in Figure 4.18, correspondingly. Two temperatures, 25°C and 500°C, were chosen to validate the model and the results are overlaid on top of the experimental data for those temperatures. As can be seen in Figure 4.31, the modeled currents are in very close agreement with the experimental data, which demonstrates the validity of the methodologies presented in this study.

4.4.5 Conclusions

InAlN/GaN Schottky diodes with novel conductive iridium oxide (IrO_x) Schottky electrodes were fabricated. The Schottky barrier height inhomogeneity was investigated and both the mean barrier heights and standard deviations were reported at moderate and high temperatures. The methodology used is supported by the analysis of Richardson plot parameters.

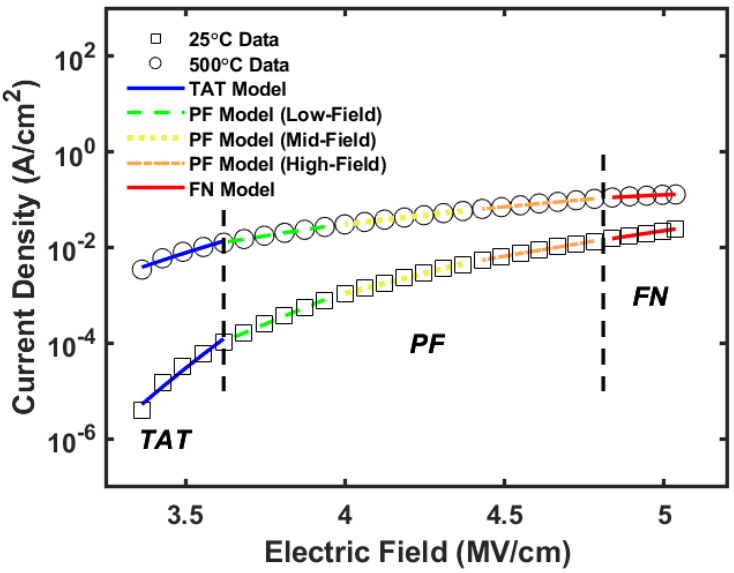

Figure 4.31: Trap-assisted tunneling, Poole-Frenkel emission, and Fowler-Nordheim emission models fit to the electric field. Experimental data at 25°C to 500°C are displayed as square and circular markers, respectively.

In reverse bias, three current transport mechanisms were identified: trap-assisted tunneling at low reverse bias, Poole-Frenkel emission at medium reverse bias, and Fowler-Nordheim tunneling at high reverse bias. We have studied the temperature-dependency of these mechanisms up to very high temperatures of 500°C (≈773 K) previously unreported for InAlN devices. The parameters for each mechanism were used to create a current versus electric field model, which closely followed the experimental data at 25°C and 500°C. These results provide valuable insight into the mechanisms contributing to undesirable reverse leakage currents in InAlN/GaN HEMTs operating at high temperature, and furthermore indicate IrO_x Schottky gates to InAlN/GaN HEMTs could be a viable solution for very hot extreme environment applications. The performance of this Schottky contact may be further improved in the future by epitaxial growth on free-standing GaN substrates instead of Si to reduce dislocation density and leakage current due to PF emission [130]. The quality of the IrO_x-InAlN interface may be improved through addition of a thin AlN cap layer that has been theorized to increase barrier heights and reduce leakage currents in AlN/InAlN/GaN heterostructures [128]. Alternatively, treating the InAlN barrier surface with N_2 plasma

prior to Schottky material deposition and oxidation could be employed to reduce the interface state charge and leakage currents due to TAT [131].

4.5 Mo/Au-gated C-HEMT Operating at 476°C in Air for 6 Days

4.5.1 Motivation

The objective of this experiment was to determine the maximum operational time at Venus surface temperatures for InAlN/GaN C-HEMTs with Mo/Au gates (Casper run sample type #5, Table 3.2) and assess their performance against IrO_x-gated C-HEMTs. Maier *et al.* previously demonstrated the operation of Mo-gated InAlN/GaN L-HEMTs at 1000°C in vacuum for 25 hours [34]. Here, the experiment is conducted in a hot oxidizing ambient (air) which is known to cause induce additional device failure mechanisms not see in vacuum such as oxidation (see Section 2.7).

4.5.2 Automated Measurement Test Setup

An experimental test setup was designed to automate the *in situ* electrical characterization of multiple HEMTs over extended periods of time. The instrumentation used in the test setup is a semiconductor parameter analyzer (Supplier: Agilent; Model: B1500A), USB modular switching matrix (Supplier: Agilent; Model: U2751A), and laptop. Figure 4.32 shows a block diagram of the experimental setup. The hardware used in the setup includes a breakout board, assembly of single stranded wire, triaxial cables, ethernet cable, GPIB to USB adapter cables, and c-dip (Supplier: Kycoera, P/N: KD-S78382-H). Pycharm integrated development environment (IDE) software was used for Python programming and the package PyVISA was used to control the SPA and switching matrix.

Before packaging, the functionality of the C-HEMTs was verified on the probe station by probing. The devices were packaged using the methods outlined in Section 3.4 with the ceramic alumina adhesive. Figure 4.33 shows an image of the wirebonded C-HEMT and the packaged sample die. Male circular pin connectors are then crimped onto the c-dip package leads and inserted into female circular pin connectors that are crimped onto the ends of the assembly wires. The opposite ends of the assembly wires are screwed into the breakout board terminals. Four additional wires run from breakout board terminals to jack

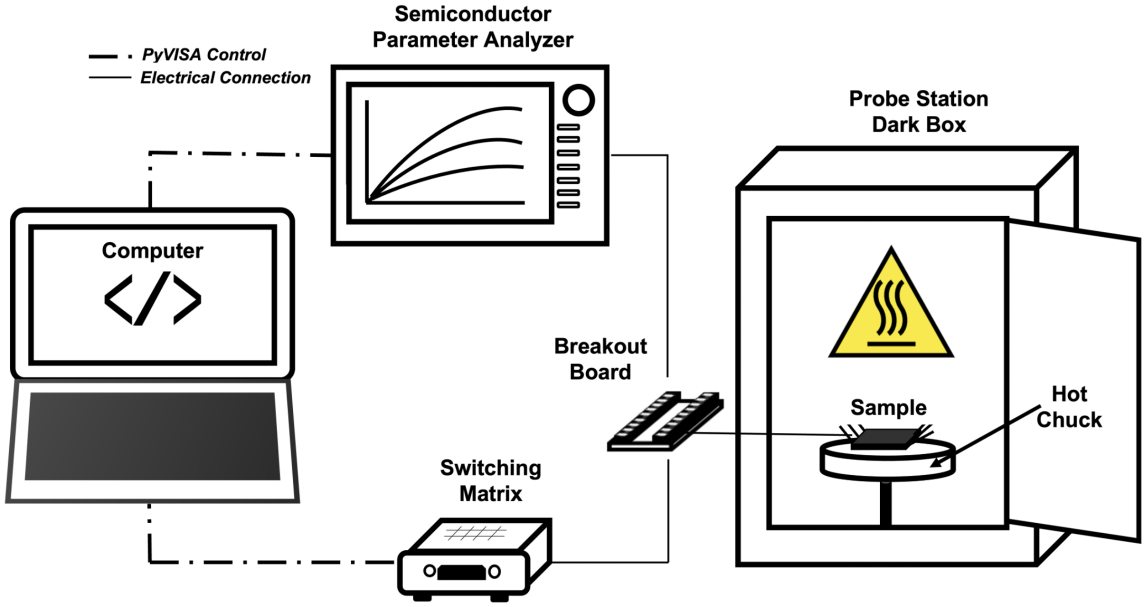

Figure 4.32: Block diagram of the automated measurement test setup developed to operate devices at high temperatures on the probe station for extended durations.

connectors; one side of each connector is soldered with a wire while the other side is hooked up to a triaxial cable providing a connection to one SMU of the SPA. Each of the breakout board terminals, numbered 1 through 25, corresponds to an electrical connection on the switching matrix. By programming with PyVISA to open and close specific switches on the switching matrix, each device can be electrically isolated for characterization. Once the correct electrical connections are configured, the PyVISA program triggers the SPA to start the desired test routine. PyVISA completes this protocol for each device in turn at every set time interval.

4.5.3 Experimental Methods

Three C-HEMTs co-fabricated on one die were characterized *in situ* hot air ambient. All of the devices had critical dimension $L_G = 5$ μm. Two of the devices had $L_{CH} = 15$ μm and the other device had $L_{CH} = 10$ μm.

In addition to the active sample, an additional dummy die of Casper Run sample type #5 was packaged identically in another c-dip package. A platinum thin film resistance temperature detector (RTD) (Supplier: TE Connectivity; Item: NB-PTCO-002) was attached

to the to surface of the dummy die using a thin layer of the epoxy. Figure 4.33 shows the sample and RTD packages prior to testing. In order to take into account temperature discrepancies between the packaged sample surface and the heated chuck controller read-out, the temperature was calculated from the RTD reading. The average RTD temperature reading over the course of the experiment was 476°C.

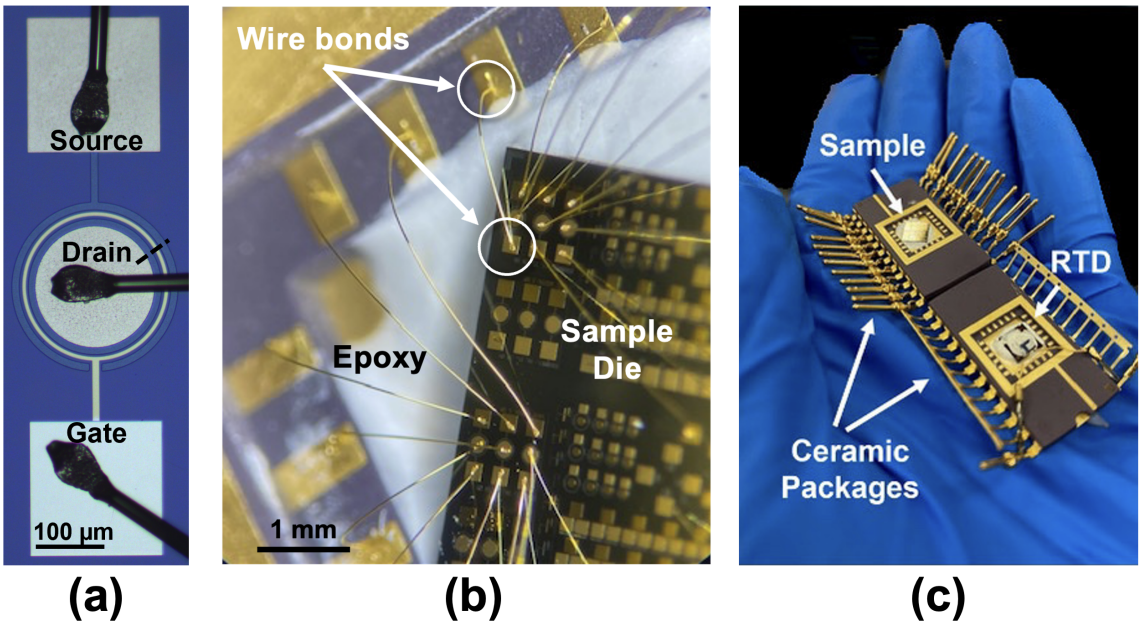

Figure 4.33: Optical images of the wirebonded C-HEMT (a), close-up of the packaged sample die showing the wirebonds and epoxy (b), and the sample and RTD ceramic packages prior to testing (c).

Devices were characterized at intermediate temperatures from 100°C to 400°C in 100°C increments during the temperature ramp from 25°C to 476°C. The sample was held at each intermediate temperature point for 10 minutes prior to electrical characterization in order to allow the sample temperature to stabilize and saturate.

Once the device reached approximate Venus surface temperature (476°C), $I_D - V_{DS}$ and $I_D - V_{GS}$ data were collected on each of the three c-HEMTs every 15 minutes for the first 30 hours, after which time the data was collected every hour for the remaining duration of the experiment. This was done solely to provide high resolution on the exact time to failure in the event the devices failed in a short period of time (e.g. on the time-scale of several hours).

The experiment was concluded after 144 hours at temperature due to failure of the

test setup. The heated chuck temperature destabilized and fluctuated wildly after one of the cooling water lines to the chuck's interior thermocouple detached. The equipment was shut off and the sample was immediately brought back to room temperature. The electrical characterization after return to room temperature was not examined because the sample was subjected to thermal cycling and shock while the output power to the chuck was oscillating in an unpredictable manner.

4.5.4 Results and Discussion

Figure 4.34 shows device characteristics during heating at $V_{GS} = 0$ V and $V_{DS} = 2$ V, respectively. The drain current decreases during heating due to decreased mobility and velocity saturation. The gate leakage current first decreases from 25°C to 200°C, and subsequently increases from 300°C to 470°C. However, ON/OFF ratio remains high with increasing temperature due to decreasing OFF-current. This could be due to decreased surface leakage to the drain as the Al_2O_3 passivation layer is thermally annealed [160]. This initial device operation during heating was promising; the ON/OFF ratio remains stable and high indicating a good range of bias points available for circuit-level implementation.

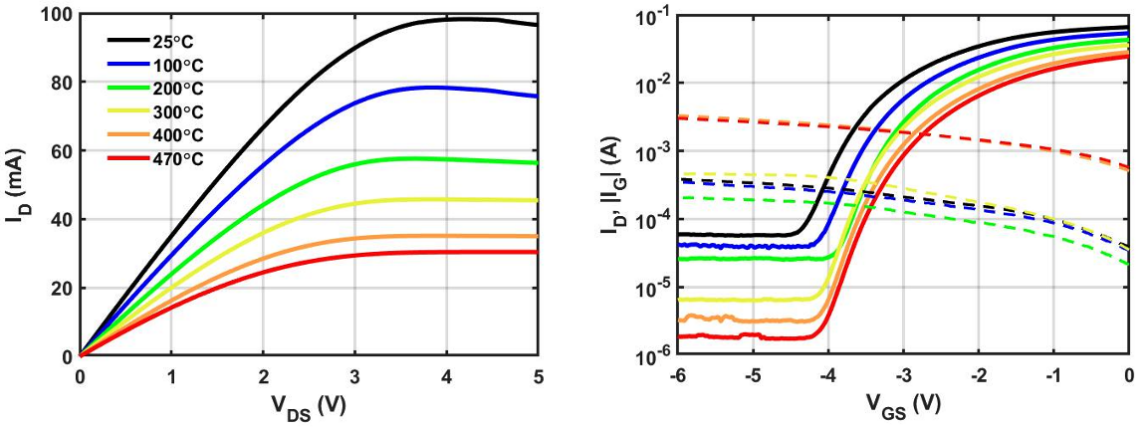

Figure 4.34: C-HEMT output (left) and transfer (right) characteristics collected during heating in air from 25°C to 476°C.

The device output and transfer curves collected at 476°C at multiple time points over the duration of the experiment are displayed in Figure 4.35. During the first 48 hours, the device performance suffers the most degradation. After this point, the device operation is stable. Figure 4.36 shows extracted device parameters of interest versus the time at

temperature. A substantial shift in the ON/OFF ratio and OFF-current occurs in the first 6 hours. Interestingly, the trend from that point onward is the opposite of what is expected: the ON/OFF ratio improves over the course of the experiment and the OFF-current continually decreases. Decrease in the gate leakage, which is also contrary to the behavior normally exhibited by C-HEMTs at high temperature, indicates that the Mo/Au Schottky barrier may be improving with time at temperature. The small shift in threshold voltage is explained by the small decrease in the drain saturation current seen in Figure 4.35. Because the saturation and cut-off characteristics of the device remain largely stable past the first few hours at temperature, the device may benefit from an intentional burn-in process in the future in order to precipitate the most severe shift in characteristics under supervised conditions prior to subsequent high-temperature operation with more stability.

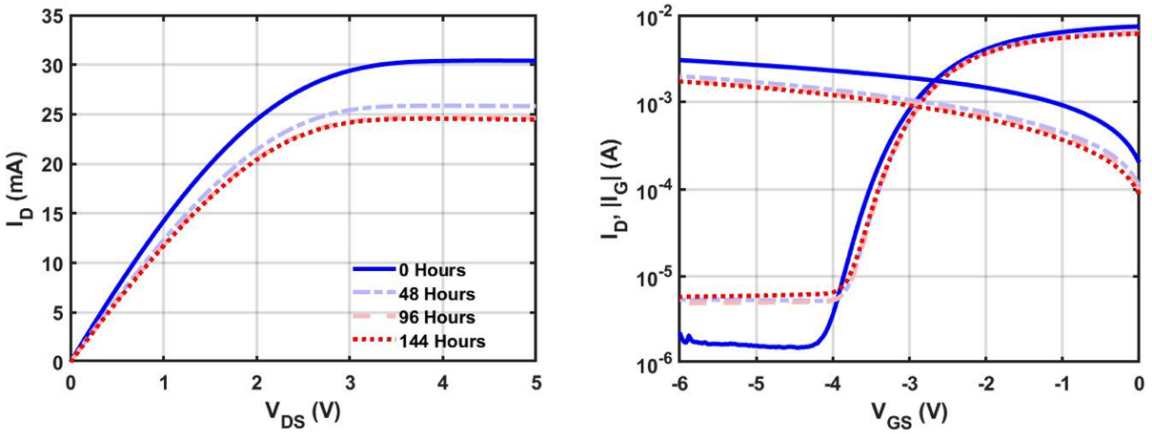

Figure 4.35: Select C-HEMT output (left) and transfer (right) characteristics collected at 476°C in air at various time points during the experiment.

4.5.5 Conclusions

These results demonstrate the DC operation of an InAlN/GaN C-HEMT at a very high temperature of 476°C, which is close to Venus' surface temperature, in oxidizing air ambient for an extended duration of 6 days. This experiment highlight the robustness of the selected device stack, which included Mo/Au Schottky gate contact, ALD Al_2O_3 passivation, and circular geometry. We believe this is the most rigorous high-temperature demonstration the InAlN/GaN HEMT operation at high temperature since Maiar *et al.* [34]. Additionally, this experiment was carried out in oxidizing air ambient instead of vacuum, which puts more

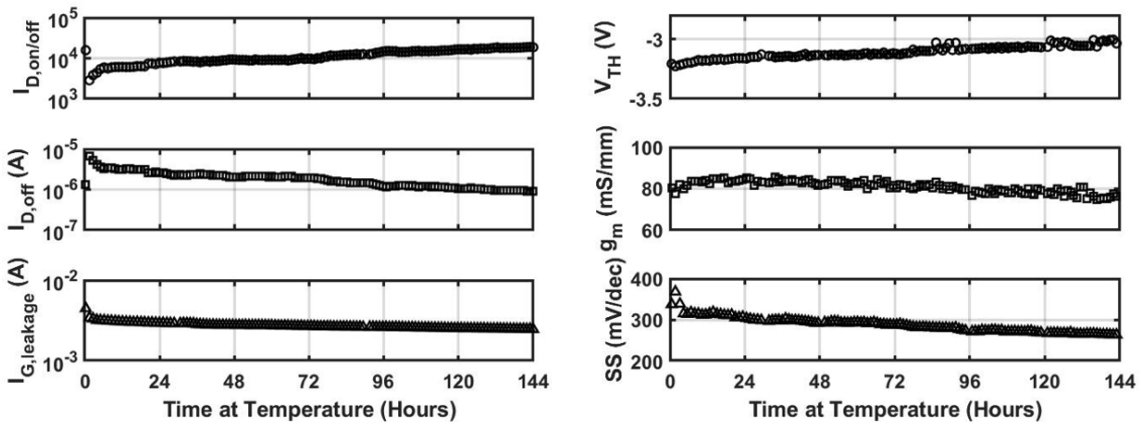

Figure 4.36: Extracted C-HEMT device parameters versus time at 476°C in air over the course of the experiment.

stress on the device. The survival of the device at these thermal conditions without any cooling measures is very promising toward the development of uncooled microelectronics for Venus surface missions. The experiment concluded prematurely due to failure of the heated chuck cooling system, and there is no reason to indicate the device could not have continued at temperature had this not occurred. The logical next step in testing the reliability of this device technology is repeating the experiment not just at Venus temperatures but at Venus pressure and atmosphere composition. That experiment is described in Section 5.5.

Chapter 5

HEMTs Operating Under Venus Surface Conditions

5.1 Overview

This chapter will focus on a series of experiments testing GaN heterostructure microelectronic devices under experimentally simulated Venus surface temperature, pressure, and atmospheric chemical composition. First, the results and insights gleaned from a 10-day passive exposure experiment conducted on several GaN 2DEG device architectures including HEMTs, Hall-effect sensors, and UV photodetectors will be discussed. This work was previously presented and published in the proceedings of the IEEE Aerospace Conference 2021 [11] © 2011 IEEE. This chapter then covers the design and build of a custom Venus simulation chamber equipped for *in situ* device characterization, and the passive testing of an Ir-gated C-HEMT in the chamber. The results demonstrating the operation of an InAlN/GaN C-HEMT *in situ* the custom chamber for up to 5 days and 21 hours are then presented. The final section of this chapter will outline the packaging and integration of an InAlN/GaN C-HEMT in preparation for future *in situ* testing within the NASA GEER chamber, which is a high fidelity replication of the Venus surface environment.

5.2 10-Day Venus Exposure Testing of GaN Microelectronics

This section describes the first assessment of the electrical integrity of GaN-based devices subject to Venus surface atmospheric conditions (≈460°C, ≈92 bar, corrosive supercritical

CO_2). Three unique device architectures were fabricated at the Stanford Nanofabrication Facility and exposed in a Venus simulation chamber for 244 hours (>10 days) at the University of Arkansas Center for Space and Planetary Sciences. The three device architectures tested were InAlN/GaN high electron mobility transistors (HEMTs), InAlN/GaN Hall-effect sensors, and AlGaN/GaN UV photodetectors, which all have potential applications in the collection and readout of sensor data from Venusian landers.

5.2.1 Motivation

The device types characterized in this exposure study were chosen due to their potential sensing and telecommunication applications on board a Venus lander. GaN HEMT devices can be used for pressure, chemical, and IR sensing [161–165]. Additionally, HEMTs have applications in read-out and transmission of sensor data to orbiters. Hall-effect sensors are often used for detecting the position and speed of rotating components (e.g., gears, motors) aboard a spacecraft, as well as monitoring the reliability of other on-board electronics via non-invasive current sensing. Ultraviolet (UV) photodetectors have applications in radiative heating characterization during atmospheric entry. This data can be used to improve thermal protection systems (TPS) on future Venus surface landers. Furthermore, these three GaN heterostructure device architectures have compatible fabrication flows, which would allow for monolithic integration of uncooled sensors with signal readout and transmission. Future maturation of this technology could substantially lower mission weight and cost by reducing packaging and shielding requirements.

5.2.2 Microfabrication

The HEMT devices were fabricated at the Stanford Nanofabrication Facility on an indium aluminum nitride ($In_{0.18}Al_{0.82}N$)/GaN-on-silicon wafer grown via MOCVD (Table 3.1. A 3D cross-sectional diagram of the devices and heterostructures are shown in Figure 5.1. HEMT active regions were isolated through a BCl_3/Cl_2 ICP RIE process. Ti/Al/Mo/Au (10/200/40/80 nm) ohmic contacts were e-beam evaporated, patterned via lift-off process, and rapid thermal annealed at 850°C for 35 seconds in N_2. Iridium (15 nm) was evaporated and patterned as the Schottky contact, followed by Ti/Au (20/200 nm) bond metal evaporation and patterning. The Ir gate metal was oxidized at 300°C for 5 minutes in O_2 via RTA to form IrO_x. The use of IrO_x gates on GaN HEMTs has been reported to reduce leakage currents compared to as-deposited Ir gates, and high-temperature operation has

been demonstrated [166–168]. The HEMT gate length was 5 μm, centered in a 20-μm-long by 100-μm-wide 2DEG channel.

The Hall-effect sensors were fabricated simultaneously on the same InAlN/GaN-on-Si wafer as the HEMT devices and underwent the same isolation and ohmic metal evaporation, lift-off, and anneal processes. The sensors were diced and removed from the fabrication run prior to the high-temperature oxidation anneal required for IrO_x formation on the HEMTs. A subset of the Hall-effect die was passivated with ≈20 nm of aluminum oxide (Al_2O_3) deposited through ALD. Vias were wet chemically etched to expose the underlying ohmic contacts. Both passivated and unpassivated devices were then patterned with Ti/Au evaporated metal bond pads. A schematic of the passivated devices is shown in Figure 5.1. Hall-effect sensor mesas are octagonal and 100 μm in width. Two of the sensors exposed in the Venus chamber (one unpassivated, one passivated) were regular octagons fabricated with contacts of equal length to the non-contacted sides of the mesa. The length of each side of these devices is 41.4 μm. One unpassivated irregular octagonal sensor with point-like contacts was also exposed. In this device, the length of sides without contacts is 5.66 times greater than the sides with contacts, which are 11.1 μm long. The difference in Hall-effect device geometries and corresponding effects on sensitivity are reported in detail in earlier work [169]. The sensitivity trends between the three devices in this experiment are consistent with the authors' prior work showing devices with point-like contacts have the highest current-related sensitivity and devices with equal sides have the highest voltage-related sensitivity [169].

The GaN heterostructure UV photodetectors were fabricated on an MOCVD-grown aluminum gallium nitride (Al0.25Ga0.75N)/GaN-on-silicon wafer purchased from DOWA, Inc. The cross-sectional device and heterostructure schematic is shown in Figure 5.1. The epitaxial stack consists of a 1.5 μm buffer structure on Si (111) followed by a 1.2 μm GaN layer, 1-nm-thick AlN spacer, 30-nm-thick AlGaN barrier layer and 1-nm-thick GaN cap. Similar to the HEMT/Hall-effect process, the photodetector microfabrication consisted of a BCl_3/Cl_2 mesa isolation etch to define the AlGaN fingers. The result is an array of 2DEG interdigitated transducers (IDTs). Ti/Al/Pt/Au ohmic metallization (20/100/40/80 nm) was evaporated, patterned via lift-off, and annealed for 35 s at 850°C in N_2 atmosphere. It should be noted that the photodetector devices utilize a Pt barrier layer in the ohmic metallization stack, while the HEMT and Hall-effect sensors have a Mo barrier layer.

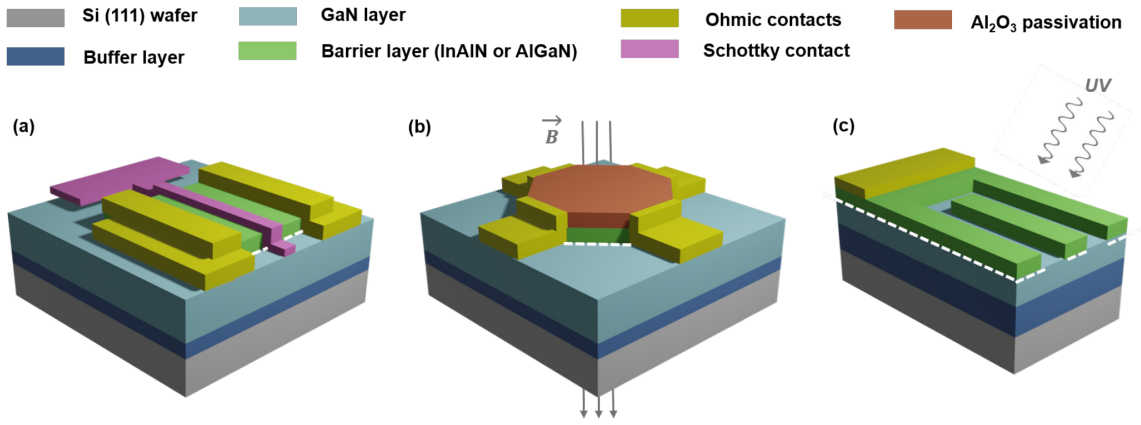

Figure 5.1: Cross-sectional schematic of the InAlN/GaN HEMTs (a), InAlN/GaN Hall-effect sensors (b), and AlGaN/GaN UV photodetectors (c) exposed to the Venus-simulant environment. Interfaces where the 2DEG is present are represented by white dashed line [11] © 2021 IEEE.

5.2.3 Experimental Methods

The HEMTs were characterized in air on a Signatone Inc. probe station equipped with a heated chuck. Current-voltage ($I_D - V_{DS}$, $I_D - V_{GS}$, $I_G - V_{GS}$) measurements were taken on a semiconductor parameter analyzer (Agilent Technologies B1500A). Using this setup, the HEMT devices were characterized at room temperature before and after the Venus simulation chamber exposure. Additionally, circular transmission line measurements (CTLM) of the ohmic contacts were taken. To compare the effects of the high-temperature supercritical CO_2 environment with high-temperature air exposure, a virgin 1 μm gate-length HEMT was characterized from room temperature to 600°C in air. In this experiment, the heated chuck was ramped from 25°C to 600°C in 100°C increments. The chuck was held at each temperature for 10 minutes before device data was acquired. After cooling back down to 25°C, the device was measured again.

The Hall-effect sensors were wire-bonded to a PCB and tested within a tunable 3D Helmholtz coil in an experimental setup described elsewhere [170]. Hall voltage measurements were conducted at room temperature. Current was sent across the device between two opposing contacts via a sourcemeter (Keithley 2400) and the resulting Hall voltage was measured across the other set of contacts using a multimeter (Agilent 34410A). The current-spinning technique described in [169] was employed to reduce the offset voltage. A switching matrix (U2715A) alternated measurement of the eight phases. The sensors and

coil were contained within MuMetal magnetic field shielding cannisters. The Hall-effect sensors were tested under a magnetic field of 2 mT and biased with current ranging from 60 uA to 0.9 mA. Additionally, measurements of mobility, sheet resistance, and 2DEG sheet density were taken of the samples that had been exposed to the Venus-analogue environment, as well as equivalent virgin samples, using the Lakeshore 8404 Hall measurement tool.

Six UV photodetectors were illuminated with 365 nm UV light at the open-air probe station and the photocurrent was measured on the semiconductor parameter analyzer. The photocurrent measurements were taken at room temperature.

The GaN-on-silicon die were mounted onto an alumina substrate for loading into the chamber. In order to attach the die, a thick-film gold layer (3066/3068N wire-bondable Au Conductors, Ferro Corporation) was screen printed on 98% alumina substrate (CoorsTek Inc.). After the firing process, 8835 gold cermet conductor (ESL 8835 (520C) 9802A, Electro-science Laboratories) was screen printed on the alumina substrate. Fabricated chips were attached to the printed gold paste followed by a 4-bar pressure to remove the air traps [108].

Venus surface atmospheric conditions were simulated within a 500 mL capacity stainless steel pressure vessel (Supplier: Parr Instruments) at the University of Arkansas Center for Space and Planetary Science. The vessel, referred to as the Venus simulation chamber throughout this section, is equipped with an internal thermocouple and exterior heating sleeve. As the chamber is heated, chamber pressure increases correspondingly. In this experiment, the chamber was pumped down to 37 mbar at room temperature and flushed with CO_2 at ≈4 bar to remove residual gas in the chamber. More CO_2 was introduced into the chamber until the desired starting pressure, calculated using the ideal gas law, was reached. The chamber was sealed and the heating sleeve was set. The chamber took ≈45 minutes to reach the temperature setpoint of 460°C and shortly afterwards the pressure stabilized to ≈96 bar. Under these conditions, the CO_2 is in a supercritical state. During the 244-hour run, the temperature and pressure were monitored and remained stable at 460°C ± 0.5% and 96 bar ± 2%.

After the run was complete, the heating sleeve was turned off and the hot gas was vented. The chamber was pumped down to 30 mbar and flushed with N_2 at ≈4 bar to remove any residual CO_2. The chamber was filled with ≈41 psi N_2 and the samples were retrieved from inside the chamber once the temperature reached 23°C. It should be noted

that N_2 and trace constituents of the Venus atmosphere were not included in the chamber during the exposure test.

5.2.4 Results and Discussion

HEMT

Figure 5.2 shows optical microscope images of the HEMT before and after exposure. In Chapter 2 several commonly reported high temperature degradation mechanisms involving the GaN HEMT contact metallization reported were discussed. After 10-day exposure in the Venus chamber, the ohmic contacts and bond pads on the HEMT were drastically darker. Color changes across the surface indicate lateral metal interdiffusion. The brown, purplish color on the gold bond pads is indicative of the formation of Au-Al intermetallic compounds. Au-Al compound formation (referred to as "purple plague") can lead to voiding and localized areas of high resistance across the contact. Despite the appearance of the bond pads, TLM measurements show the specific contact resistivity remained on the same order of magnitude (2.2×10^{-5} Ω·cm^2 before exposure and 3.7×10^{-5} Ω·cm^2 after exposure). This indicates that the Mo layer was an effective Al-Au diffusion barrier in the ohmic metallization region not overlapping with the bond pad.

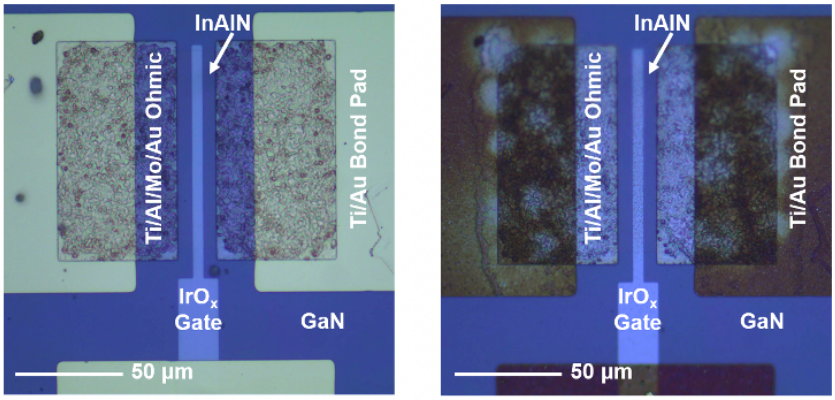

Figure 5.2: Optical image of the microfabricated HEMT before (left) and after (right) the 10-day simulated Venus exposure [11] © 2021 IEEE.

The DC output characteristics ($I_D - V_{DS}$) and transconductance (g_m) of the 5 μm gate-length HEMT before and after exposure are shown in Figure 5.3. HEMT parameters are reported in Table 5.1. Maximum drain saturation current ($I_{D,sat}$) and maximum transconductance ($g_{m,max}$) both increased after Venus chamber exposure. This behavior is attributed

to thermal detrapping in the InAlN/GaN heterostructure. While trapping phenomenon is still not fully understood in InAlN/GaN, thermal treatment has been demonstrated to be effective for detrapping purposes [70]. Moreover, it is possible that supercritical CO_2, which can penetrate deeply into the GaN heterostructure, could be interacting with residual gases in the chamber to anneal defects in the lattice [171,172]. However, drain current relaxation back towards pre-exposure values became more pronounced as the negative gate voltage was increased in the test routine post exposure (Figure 5.3). During $I_D - V_{DS}$ measurements, V_{GS} was stepped from 0 V to −3 V sequentially. The percent change from the pre-exposure drain current was +32% for $V_{GS} = 0$ V, but only +25% for $V_{GS} = -1$ V. The trend of decreasing percent change in drain current continues with further negative applied gate voltage. This drain current relaxation can be explained by the accumulation of negative charge trapped on defects induced by gate voltage steps [173]. In other words, the Venus chamber exposure likely led to detrapping or defect annealing in the lattice, causing a brief increase in drain current that was counteracted by re-trapping as the device was electrically characterized post-exposure. In the future, characterization of the trap states in the InAlN/GaN HEMTs before and after exposure could be accomplished by deep level transient spectroscopy (DLTS).

Parameter	**Symbol**	**Unit**	**Before Exposure**	**After Exposure**
Saturation Current	$I_{D,sat}$	A/mm	0.20	0.26
Off Current	$I_{D,off}$	A/mm	3.92×10^{-9}	5.35×10^{-9}
On/Off Ratio	$I_{D,on}/I_{D,off}$	–	3.36×10^{7}	3.28×10^{7}
Threshold Voltage	V_{Th}	V	-3.18	-3.22
Subthreshold Swing	SS	mV/dec	89	90

Table 5.1: HEMT electrical parameters before and after exposure in the Venus chamber.

Figure 5.3 illustrates $I_D - V_{DS}$ and $I_D - V_{GS}$ before and after exposure. The extracted OFF-current ($I_{D,off}$) and ON/OFF ratio ($I_{D,on}/I_{D,off}$) before and after exposure are comparable and on the order of 10^{-9} A/mm and 10^{7}, respectively (Figure 5.1). The gate leakage current (I_G) of the HEMT remains on the same order of magnitude after exposure (Fig. 5.1), while the drain current exhibits the small increase explained above (Figure 5.3). The threshold voltage (V_{Th}) of the HEMT is extrapolated in the linear regime (Table 5.1). V_{Th} was reduced by only ≈1.1% after exposure, further proof of the high thermal stability of the gate after subjection to Venus surface conditions. An Auger electron spectroscopy (AES) depth profile over the gate confirms that the composition remains IrO_x and the gate has

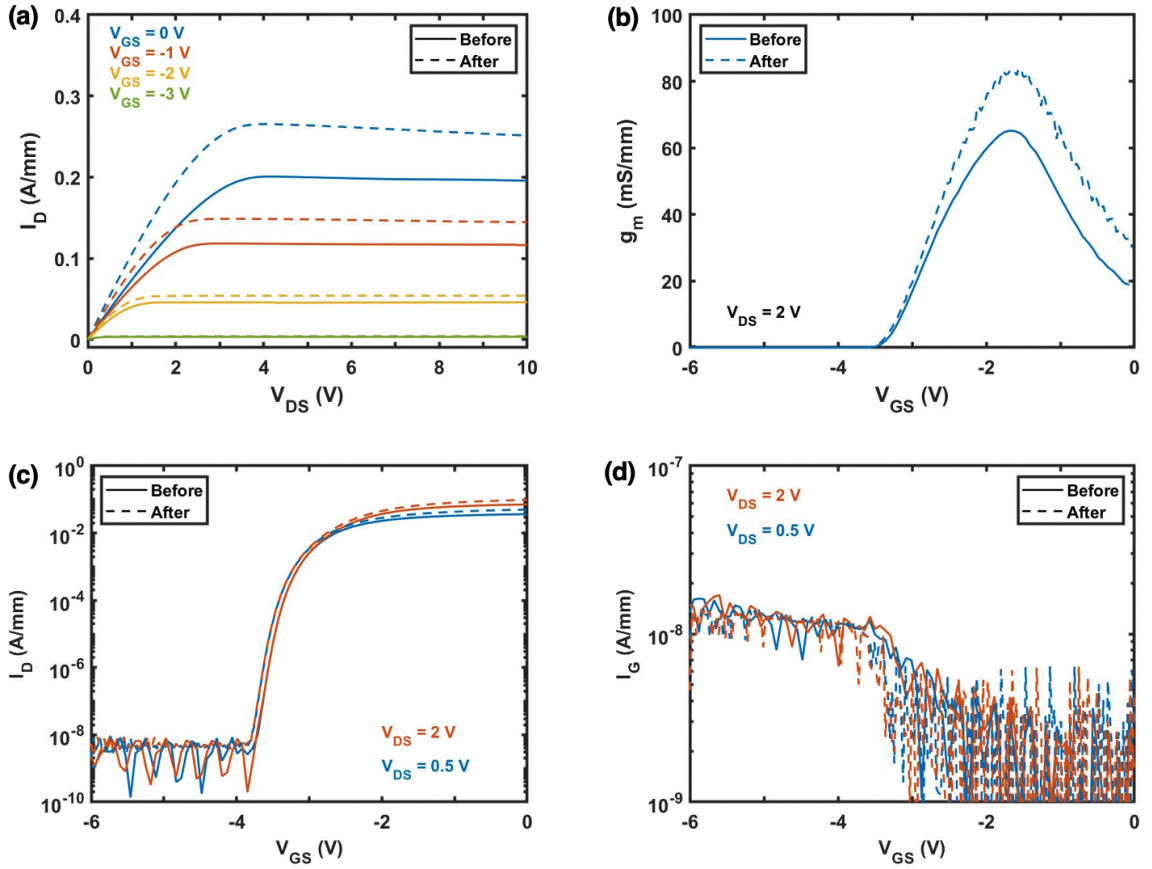

Figure 5.3: $I_D - V_{DS}$ (a), transconductance (b), $I_D - V_{GS}$ (c), and $I_G - V_{GS}$ (d) of the 5 μm gate-length HEMT before and after exposure in the Venus chamber [11] © 2021 IEEE.

not sunk down into the underlying substrate (Figure 5.4).

The transfer characteristics $I_D - V_{DS}$ and $I_D - V_{GS}$ of the virgin 1 μm gate-length HEMT characterized at high-temperature in air (as described under Experimental Methods) are displayed in Figure 5.5. When the temperature was increased to 300°C and 400°C, measurements show the occurrence of current collapse, which is consistent with the presence of deep traps in the HEMT [173]. The decrease in drain current with increasing temperature is expected and due to increased carrier scattering at elevated temperatures. However, permanent degradation of HEMT performance upon cooling back down to 25°C is also observed. V_{Th} is shifted by nearly +1 V and maximum drain saturation current is reduced substantially (Figure 5.6). The non-recoverability of HEMT characteristics after only short-term (10 minutes at each temperature point) high-temperature exposure is

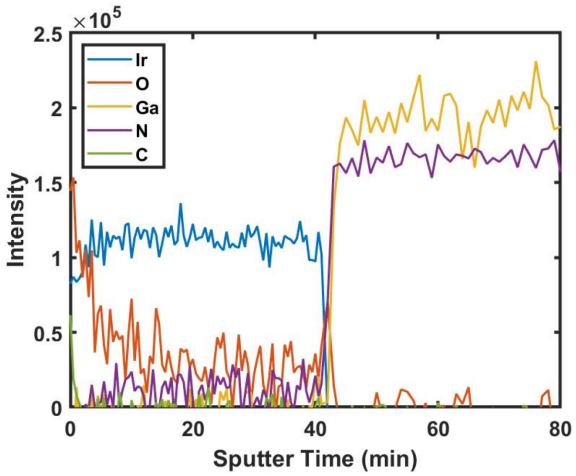

Figure 5.4: Post-exposure Auger depth profile over the IrO_x gate on the InAlN/GaN HEMT [11] © 2021 IEEE.

attributed to oxidation reactions in air. Instability of the IrO_x gate in air is thought the be the cause of the degraded device performance because ungated InAlN/GaN Hall-effect sensors from the same fabrication run exhibited near full recoverability of 2DEG properties after multiple thermal cycles up to 576°C and back in air [4]. These data highlight the need for careful consideration of the atmosphere (e.g. supercritical CO_2 vs. air) of the intended high-temperature application of unpassivated HEMT devices.

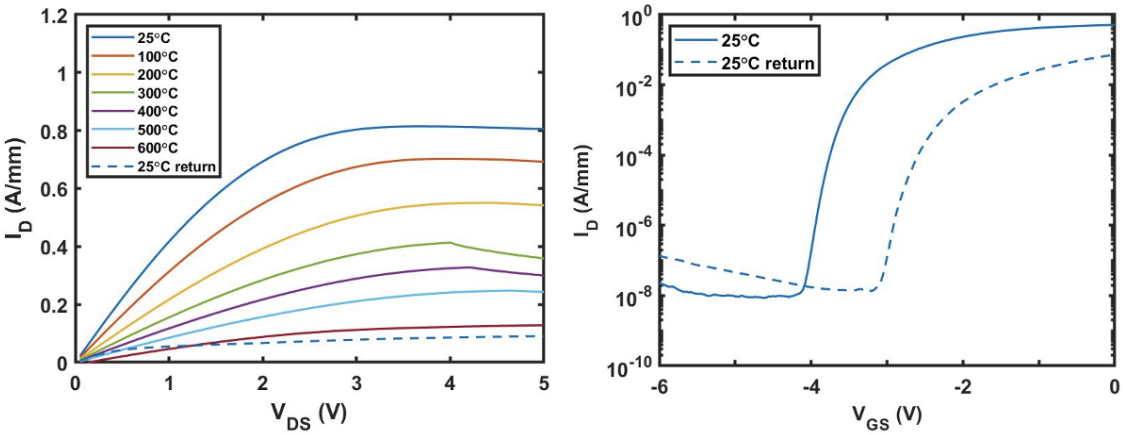

Figure 5.5: $I_D - V_{DS}$ (a) and $I_D - V_{GS}$ (b) of the virgin 1 μm gate-length HEMT characterized at high-temperature in air [11] © 2021 IEEE.

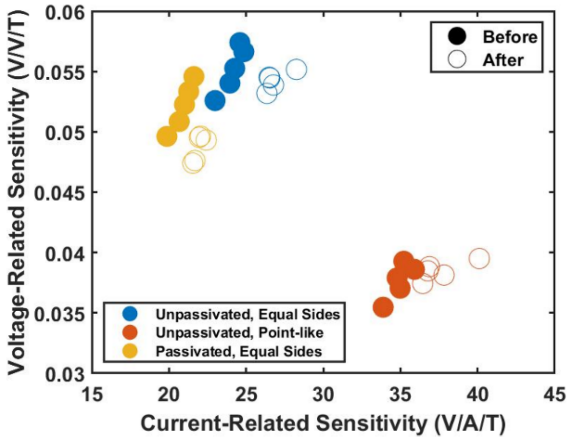

Figure 5.6: Voltage-related versus current-related sensitivity for the three Hall-effect sensors before and after exposure [11] © 2021 IEEE.

Hall-effect Sensors

Table 5.2 summarizes the 2DEG properties of InAlN/GaN Hall-effect sensors post-exposure as well as the properties of equivalent virgin devices. The differences in mobility, sheet carrier density, and sheet resistance between the virgin and exposed samples are within the tolerances of die-to-die variation and measurement setup limitations, suggesting that the 2DEG remained largely unaffected by prolonged exposure to Venus surface atmospheric conditions.

Sample	R_{SH} $(\Omega/\square)$	μ $(cm^2/V \cdot s)$	n_s (cm^{-2})
Unpassivated, Virgin	272	1124	2.03×10^{13}
Unpassivated, Post-Exposure	302	1076	1.92×10^{13}
Passivated, Virgin	252	1031	2.41×10^{13}
Passivated, Post-Exposure	248	1026	2.45×10^{13}

Table 5.2: Virgin and post-exposure Hall-effect sensor 2DEG properties.

The current-scaled and voltage-scaled sensitivities of the three InAlN/GaN Hall-effect sensors before and after exposure are shown in Figure 5.6. Table 5.3 and Table 5.4 report their average current-related and voltage-related sensitivities and the corresponding percent change, correspondingly. The current-scaled sensitivity increased in all three devices after exposure, with the largest increase of 11.4% seen in the unpassivated device with contacts equal in length to the non-contacted sides. The increase in current-scaled sensitivity, which is inversely proportional to sheet carrier density (Equation 3.4), indicates a small, permanent

decrease in n_s in both the passivated and unpassivated sensors after long-term exposure to the simulated Venus environment.

Device	$S_{i,pre}$ **(V/V/T)**	$S_{i,post}$ **(V/V/T)**	**% change** S_i
Unpassivated, Equal Sides	24.1	26.9	+11.4
Unpassivated, Point-like	34.9	37.6	+7.6
Passivated, Equal Sides	20.9	21.9	+5.0

Table 5.3: Current-related sensitivities of the Hall-effect sensors before and after exposure.

Device	$S_{v,pre}$ **(V/A/T)**	$S_{v,post}$ **(V/A/T)**	**% change** S_v
Unpassivated, Equal Sides	0.0552	0.0542	−1.7
Unpassivated, Point-like	0.0377	0.0385	+2.2
Passivated, Equal Sides	0.0521	0.0487	−6.6

Table 5.4: Voltage-related sensitivities of the Hall-effect sensors before and after exposure.

The small fluctuations in voltage-scaled sensitivity before and after exposure in both unpassivated Hall-effect sensors (equal-sided device: −1.7%; point-like contacts: +2.2%) are within the measurement limitations of the test setup (Table 5.3). However, the decrease in voltage-scaled sensitivity of the passivated device is larger (-6.6%), consistent with a small decrease in the device mobility after exposure (Equation 3.5). Though the InAlN/GaN heterostructure is lattice matched and therefore not prone to mechanical strain, the addition of an Al_2O_3 passivation layer adds tensile stress to the system [174]. High-temperature strain relaxation likely accounts for the decrease in mobility due to increased dislocation scattering, although further studies are needed to study the effects of supercritical CO_2 on ALD Al_2O_3.

UV Photodetectors

Figure 5.7 shows the photocurrent of the AlGaN/GaN UV photodetectors before and after simulated Venus chamber exposure. The photocurrent across the devices decreased by 38±2.9% on average after exposure. As an experimental setup control measure, a virgin photodetector die was tested simultaneously as the exposed die. The photocurrent of the four virgin photodetectors averaged only 1.47% less than the photocurrent of the six detectors prior to Venus exposure. This small difference in average photocurrent is due to die-to-die variation, indicating that the decrease in photocurrent of the detectors after exposure is indeed real and not an artifact of changes in the test setup.

The decrease in photocurrent post-exposure can be attributed to strain relaxation in

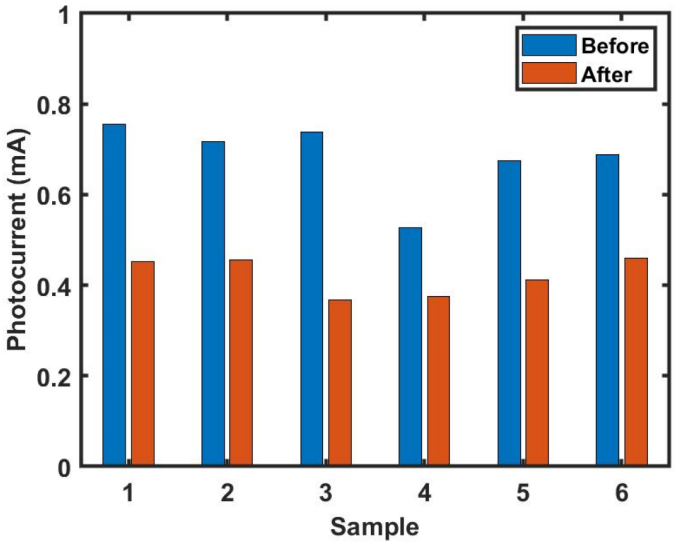

Figure 5.7: Photocurrent reponse of the 6 UV photodetectors under 365 nm illumination before and after Venus chamber exposure [11] © 2021 IEEE.

the AlGaN/GaN heterostructure. It is well established that mechanical stress in the AlGaN/GaN structure significantly influences the 2DEG carrier concentration and mobility. High-temperature induced strain relaxation can produce dislocations and cracks, which in turn reduce the 2DEG mobility via increased scattering [160, 175–178]. Decrease in 2DEG sheet carrier density, and the subsequent increase in sheet resistance, can explain the decrease in photocurrent after exposure.

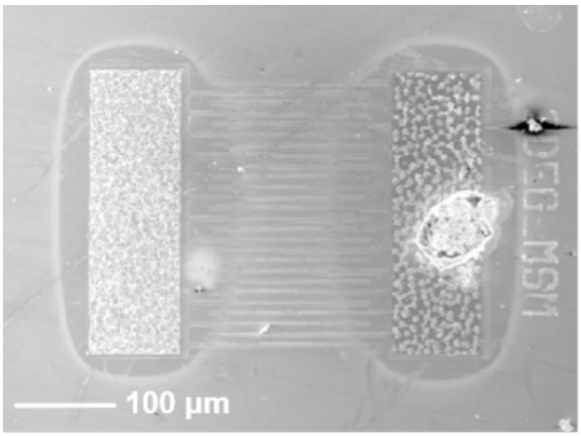

Figure 5.8: SEM image of UV photodetector after exposure in the Venus chamber. Contact with Al wire bond bump is shown on the right [11] © 2021 IEEE.

Another possible explanation for the decrease in photocurrent is degradation of the ohmic contact metallization. Scanning electron microscopy (SEM) images of the UV photodetectors after exposure in the Venus chamber show a halo of diffused metal surrounding the contacts and bleeding into the 2DEG IDT region (Figure 5.8). Lateral diffused metal could be acting as a reflection coating over the IDTs, thereby reducing photocurrent. Alternatively, if vertical diffusion occurred as well as lateral diffusion, the migrated metal could be degrading the 2DEG mobility through impurity scattering. Moreover, the SEM images reveal substantial morphological differences between the ohmic contacts with and without residual Al wire bond bumps. Changes to the surface morphology are consistent with a non-uniform contact-barrier layer interface, which can cause localized increased contact resistance and decrease the effective photocurrent readout. Future characterization of Ti/Al/Pt/Au CTLM structures can determine if the specific contact resistivity is increased after extended Venus surface atmospheric condition exposure.

5.2.5 Conclusions

In this study, we have characterized three unique GaN heterostructure device architectures before and after 10 days of exposure to simulated Venus atmospheric conditions of 465°C, ≈96 bar, and supercritical CO_2 ambient. After exposure, HEMT threshold voltage had shifted only ≈1% and gate leakage current remained on the same order of magnitude, demonstrating stability of the IrO_xgate under supercritical CO_2ambient. Increases in HEMT drain saturation current post-exposure are attributed to thermal detrapping, while subsequent drain relaxation under bias conditions is due to trapping. The stability of the threshold voltage, gate leakage current, and on/off ratio in the InAlN/Gan HEMTs make these devices excellent candidates for Venus lander missions. It was found that 2DEG properties of InAlN/GaN Hall-effect sensors were not significantly altered after Venus chamber exposure compared to virgin devices. Furthermore, the Hall-effect sensors exhibited a maximum average shift of +11.4% in current-scaled sensitivity and −6.6% in voltage-scaled sensitivity, suggesting near full recovery of sensing performance after the Venus environment exposure. However, the AlGaN/GaN UV photodetectors suffered a large decrease in photocurrent of ≈38% after the exposure, which is thought to be due to strain relaxation or degradation of the ohmic contact metallization. The stability of the InAlN/GaN HEMTs and Hall-effect sensors after 10-day exposure to a simulated Venus surface environment makes these devices attractive candidates for deployment on future Venus lander missions,

as well as in other harsh environments such as CO_2 sequestration and storage. Diminished photocurrent in the AlGaN/GaN UV photodetector after simulated Venus exposure requires further analysis to determine if the strain-dependence of the 2DEG properties precludes this class of devices from prolonged Venus surface operation. This study indicates Ti/Al/Mo/Au is a reliable ohmic contact to GaN-based devices for extreme environment operation, while Ti/Al/Pt/Au is questionable.

5.3 Venus Simulation Chamber Setup

5.3.1 Motivation

In order to simulate the environmental conditions on the surface of Venus in the laboratory, a custom pressure vessel, referred to as the XLab Venus simulation chamber, was designed and set up. The chamber is similar to the Venus simulation chamber at the University of Arkansas Center for Space and Planetary Sciences used for the exposure experiment described in the previous Section 5.2. The chamber at the University of Arkansas was not equipped with electrical feedthroughs to enable *in situ* measurements, while an electrical feedthrough assembly and automated measurement system were implemented on the XLab Venus simulation chamber to achieve this capability.

5.3.2 Pressure Vessel

The XLab Venus simulation chamber is a modified non-stirred, fixed head pressure vessel purchased from Parr Instrument Company (Model N4760HT). The cylindrical chamber body has a 2.5" inner diameter and 6.0" inside depth. The chamber capacity is 450 mL and the maximum allowable working pressure (MAWP) rating is 2000 psi at 500°C. The chamber head, cylindrical body, internal wetted parts, and external valves and fittings are constructed of T316 stainless steel. The head of the chamber is equipped with a needle valve and pressure gage affixed on top of a gage adapter, a safety rupture disc of Alloy 600 rated to 2000 psi at temperature, thermowell with a Type J thermocouple, and two 1/4" National Pipe Taper Fuel (NPTF) style adapters with custom cooling sleeves. The head also has an additional valve to allow the introduction of a second gas into the chamber. Figure 5.9 shows 3D renderings of the pressure vessel.

The chamber head is fixed on a bench top stand within a fume hood. The head and

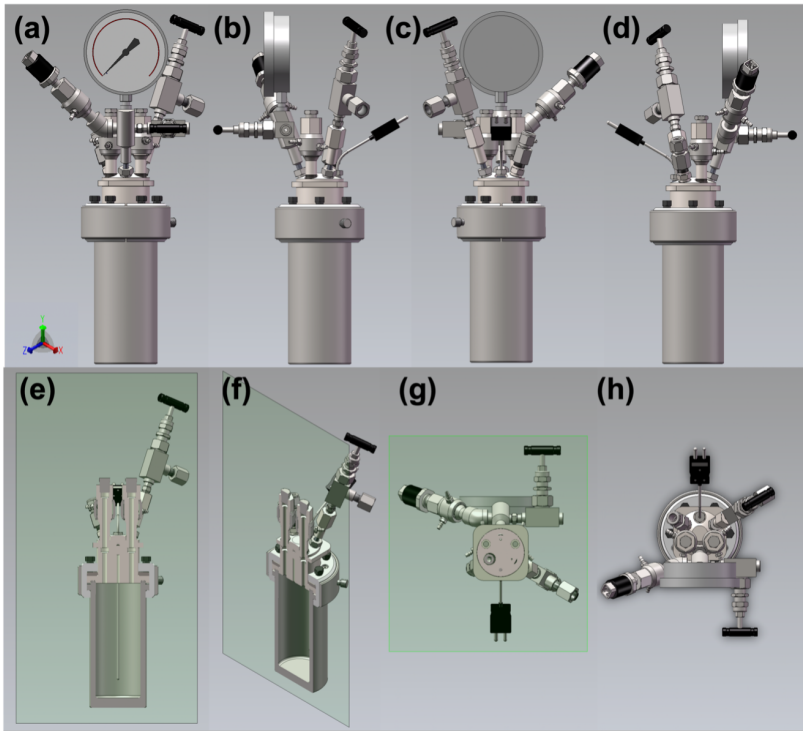

Figure 5.9: 3D rendering of the XLab Venus chamber from Parr Instruments. Views of the chamber from the front (a), right (b), back (c), left (d) and the chamber's front cross-section (ed), tilted cross-section (f), fixed head bottom (g) and fixed head top (h). Diagrams rendered by Parr Instruments.

the cylindrical body where the device under test (DUT) is situated are mechanically held together by a split ring closure with bolts that are torqued to ≈35 ft/lb each prior to pressurization. A flexible Grafoil gasket situated within a groove in the head where it mates with the body maintains the seal. Also attached to the bench top stand is a ceramic heating sleeve that can be raised and lowered as required. During heating, the sleeve is raised up to encase the vessel body. The interior temperature of the vessel is set by a PID temperature controller that digitally monitors the thermocouple reading and adjusts the power to the ceramic sleeve accordingly. The temperature controller also includes a pressure display module with transducer. The controller is attached to a laptop and the temperature and pressure outputs are recorded up to every minute in real time over the duration of an experiment using the software SpecView. While temperature can be controlled and read out by the temperature controller and SpecView, the pressure can only be read out; there is no mechanism for pressure control on the controller unit. High pressure

is achieved through heating; as the temperature inside the chamber rises, the pressure rises with it. The ideal gas law is used to calculate the required initial pressure required at the starting temperature, which was usually between 20°C and 25°C, to achieve the desired experimental pressure at the desired experimental temperature. The standard operating procedure to achieve Venus's surface conditions is as follows:

1. Place the sample in the chamber at room temperature.
2. Pump the chamber down to vacuum (-14 psi on the gauge).
3. Fill the chamber with CO_2 until pressure reaches ≈60 psi.
4. Repeat steps 2-3 five times total to remove the ambient air from the chamber interior.
5. Fill the chamber with CO_2 until the desired initial pressure is reached (≈540 psi).
6. Set the desired experimental temperature on the cooling sleeve (≈465°C)and begin heating.

5.3.3 Equipment

Ancillary equipment to the Venus simulation chamber setup include a vacuum pump, cooling water lines hooked up to the building water supply system, and stainless steel gas lines piped from the fume hood up through the ceiling to the gas cylinder racks in the next room where the CO_2 and N_2 tanks are stored. The cooling water runs to cooling sleeves surrounding the valves on the fixed head in order to keep the pressure bearing seals at lower temperatures than the chamber interior. One of the gas lines has an offshoot line with a valve pointing up into the back of the fume hood to allow for supercritical fluids and gases to be safely vented while still hot.

5.3.4 Electrical Feedthroughs

To allow for the collection of device data *in situ*, a custom modified high density multiple wire feedthrough gland was purchased from Conax Technologies. The feedthrough assembly consists of 4 electrically insulated 20 AWG wires. The wire material is Alumel, which is composed of 95% Ni, 2% Mn, 2% Al, and 1% Si and frequently used as the negative conductor in Type K thermocouples. The wires are electrically insulted by high temperature capable fiberglass and run through a stainless steel tube sitting in a sealing gland

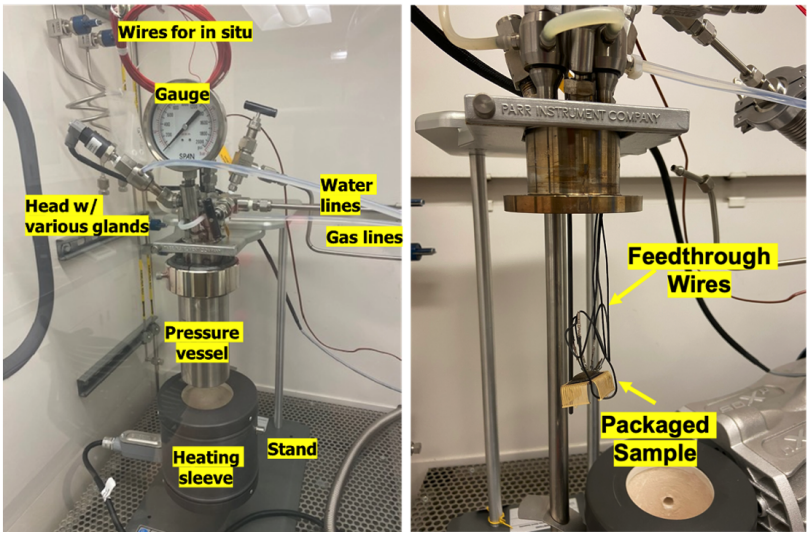

Figure 5.10: External (a) and internal (b) pictures of the XLab Venus Simulation chamber set up in the laboratory.

that can withstand and maintain the high pressure of the Venus chamber. The gland was installed into one of the 1/4" NPTF adapters on the head of the chamber. Cooling water is run through the adapter during high temperature experiments to ensure the integrity of the gland and wire feedthrough. The portions of the wires outside of the Venus simulation chamber and running through the stainless steel tube of the feedthrough are Kapton insulated (red wires in Figure 5.10). Because Kapton is unsuitable for use above 400°C, the portions of the wires inside of the chamber are insulated with high-temperature fiberglass sleeving (black wire portion in Figure 5.10).

5.3.5 Automated Measurement Setup

To start an experiment, the chamber was opened and the DUT was placed inside. For *in situ* or active tests, the die is packaged using the same materials and methods as described in Section 4.5. The auto measurement test setup described in Section 4.5 was used to collect *in situ* device data over the duration of the experiment. The *in situ* test setup in the XLab Venus chamber is identical to the test setup in air with the exception of the type of wire and insulation used. A diagram of the automated measurement setup modified for use in the XLab Venus simulation chamber is shown in Figure 5.11.

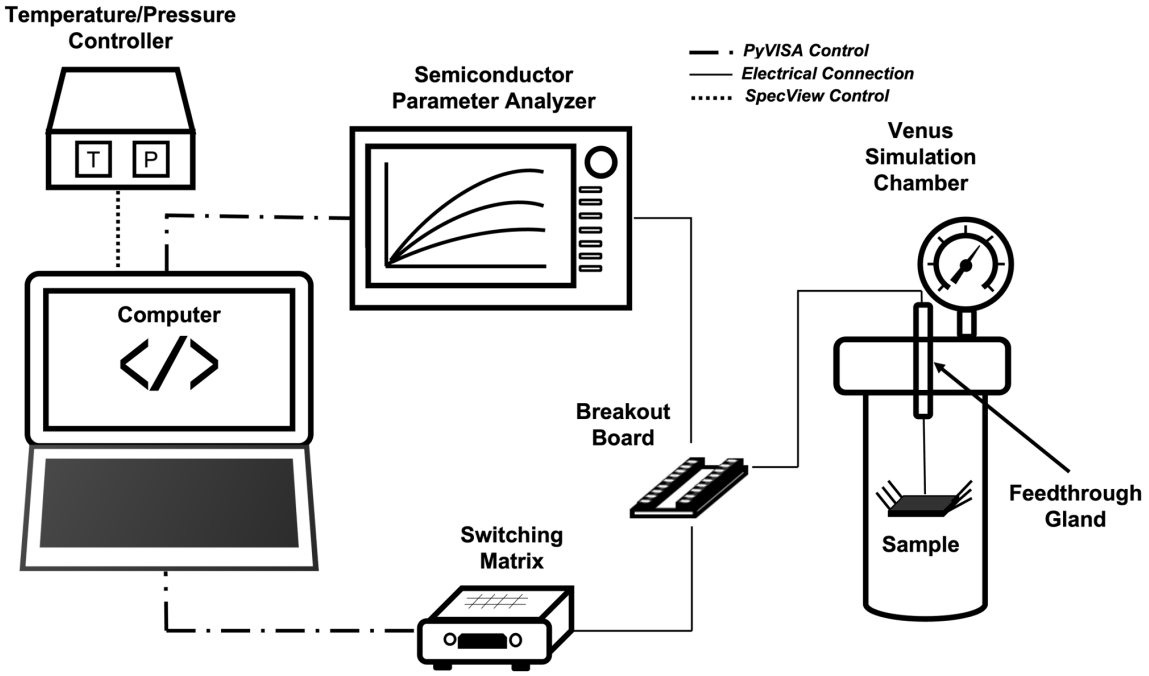

Figure 5.11: Block diagram of the automated test setup to collect device data *in situ* the XLab Venus simulation chamber.

5.4 4-Day C-HEMT Exposure Testing

5.4.1 Motivation

In order to verify the XLab Venus simulation chamber setup was working properly and the chosen sample packaging could sufficiently survive chamber conditions, a 4-day exposure experiment was conducted on a packaged InAlN/GaN C-HEMT die with Ir/Au gate metallization. Additionally, the experiment served as a valuable preliminary assessment of the reliability of Ir/Au Schottky contact gates to InAlN when subjected to Venus surface conditions.

5.4.2 Experimental Methods

A Casper run sample type #3 die was selected for testing (Table 3.3). The die was packaged according to the procedure outlined in Section 3.4. The electrical characteristics of three Ir/Au gated C-HEMTs with Al_2O_3 passivation were collected and compared prior to and

after the exposure, labelled pre-exposure and post-exposure. The gate length of the C-HEMTs is 1 µm and the channel widths were 10, 15, and 20 μm. The environmental conditions inside the chamber during the experiment were 1350 psi and 465°C in sCO_2 ambient. The sample was subjected to these simulated Venusian surface conditions for a duration of 4 days.

5.4.3 Results and Discussion

Optical images of the 3 C-HEMTs and the electrical characteristics of the 20-μm channel-width device are shown in Figure 5.12. The device ohmic contacts in the source and drain region are darker after exposure, indicative of material changes imitated by the high-temperature sCO_2 exposure. Device parameters also shifted post-exposure. The threshold voltage shifted from -4.2 V to -3.8 V (+9.5%), on/off ratio decreased from 6×10^5 to 7×10^4, and the drain saturation cu rent decreased from 53 mA to 37 mA (-30%). The post-exposure values are consistent with the occurrence of degradation mechanisms such as gate sinking and reduced 2DEG density; however, even the post-exposure values remain suitably high compared to state-of-the-art values.

5.4.4 Conclusions

The results are a further demonstration that InAlN/GaN C-HEMTs can survive within harsh sCO_2 environments such as the Venus atmosphere. The Ir/Au multilayer Schottky contact may provide adequate gate control despite the indication of potential gate sinking effects. Further studies are needed to assess the *in situ* performance of devices comprised of this HEMT material stack in order to assess the presence of electrically-activated degradation mechanisms such as electromigration (Section 2.8).

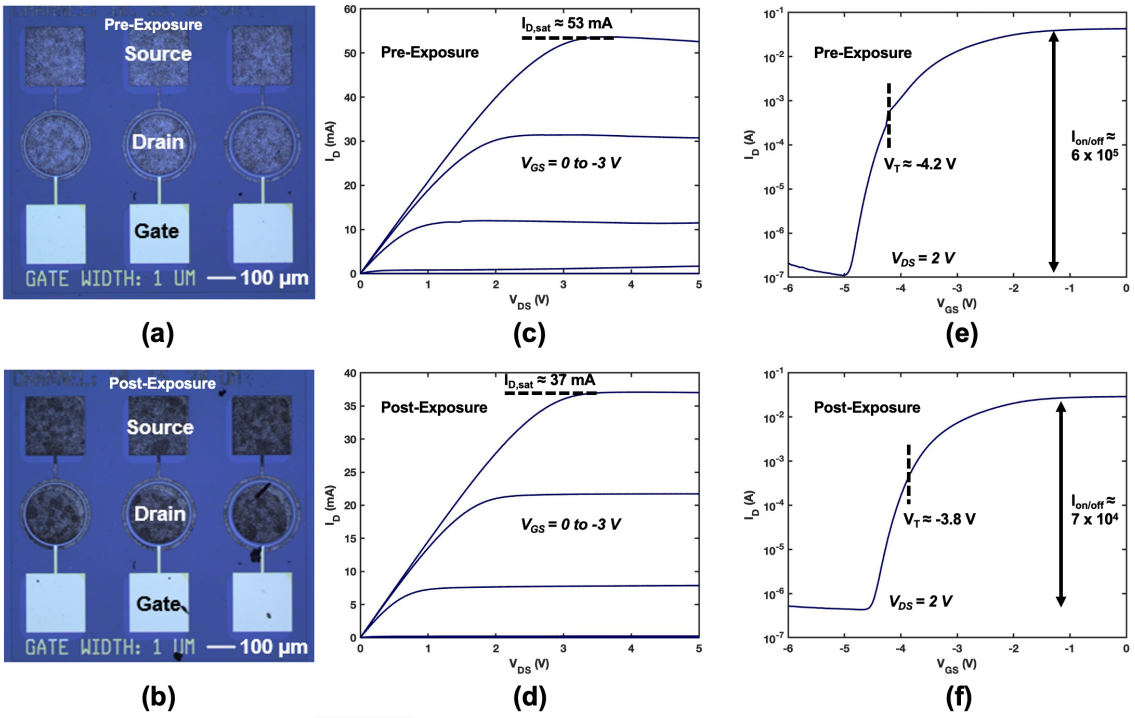

Figure 5.12: Optical images pre-exposure and post-exposure of 3 circular HEMTs (a, b), and $I_D - V_{DS}$ (c, d) and $I_D - V_{GS}$ characteristics (e, f) of the 20-μm channel-width device before and after 4-day exposure in the XLab Venus simulation chamber.

5.5 5-Day Operation of a C-HEMT *in situ* Simulated Venus Surface Conditions

5.5.1 Motivation

After the successful demonstration of Casper Run sample type #5 (Table 3.2 e.g. Mo/Au gate and Al_2O_3 passivation) operating at Venus temperatures in air for 6 days presented in the previous chapter (Section 4.5), this material and device architecture was selected for testing *in situ* the XLab Venus simulation chamber, which allows for assessment of device performance in sCO_2 ambient.

5.5.2 Experimental Methods

The die packaging was identical to the the C-HEMT die packaging in the passive exposure test described in the previous Section 4.5. Further details on the packaging procedure can

be found in Section 3.4. Several 5-μm gate-length C-HEMTs with channel widths 10, 15, and 20 μm were wirebonded in preparation for testing. Because the feedthrough gland into the chamber is limited to 4 wires, only one C-HEMT device was able to be tested *in situ*. The C-HEMT with the best electrical performance post-wirebonding was chosen. The device channel width was 15 μm. The packaged sample was loaded into the chamber and the pins associated with the source, drain, and gate on the C-HEMT package were each attached to a feedthrough wire. The fourth feedthrough wire was not used. The tension in the wires suspended the package within the chamber. The electrical connections and operation of the automated test measurement setup were verified, and the chamber was closed. The standard operating procedure to pressurize the chamber was conducted with ultra high purity 99.999% CO_2 (Section 5.3). The starting temperature and pressure of the chamber were 24°C and 528 psi, respectively. The chamber temperature was slowly ramped up and measurements were taken at 100°C, 200°C, 300°C, and 400°C until the desired test temperature of 465°C was reached. Once this temperature was reach, the automated test measurement setup program was executed to collect data every 15 minutes. Every measurement cycle consisted of two test routines: one sweeping the drain voltage ($I_D - V_{DS}$) and one sweeping the gate voltage ($I_D - V_{GS}$).

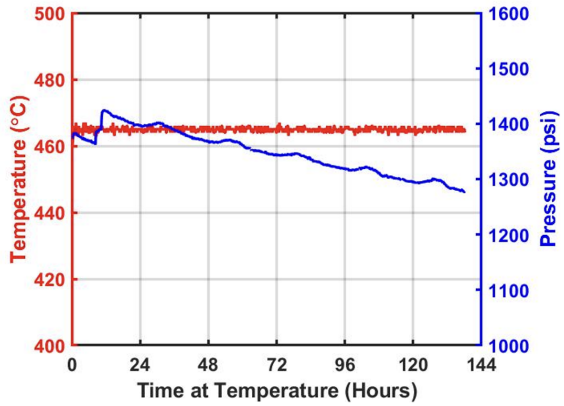

Figure 5.13: Temperature and pressure inside of the XLab Venus simulation chamber over the course of the 5-day *in situ* C-HEMT characterization experiment

Over the course of the nearly 6 day experiment, the chamber temperature and pressure, which were recorded every ten minutes and displayed in Figure 5.13, averaged 464.9°C and 1348 psi, respectively. The drop in pressure from a maximum of 1424 psi to a minimum of 1277 psi indicates that the chamber had a slow leak. Previous chamber leaks experienced

during initia testing originated from one of the valves fitted into the chamber head and not from the grafoil gasket sealing the chamber body shut. Because the C-HEMT devices do not posess a cavity, the variation in pressure is largely irrelevant to the experiment; the goal was to simulate the conditions that render CO_2 supercritical on Venus and the average pressure was very close to the 1350 psi found on Venus.

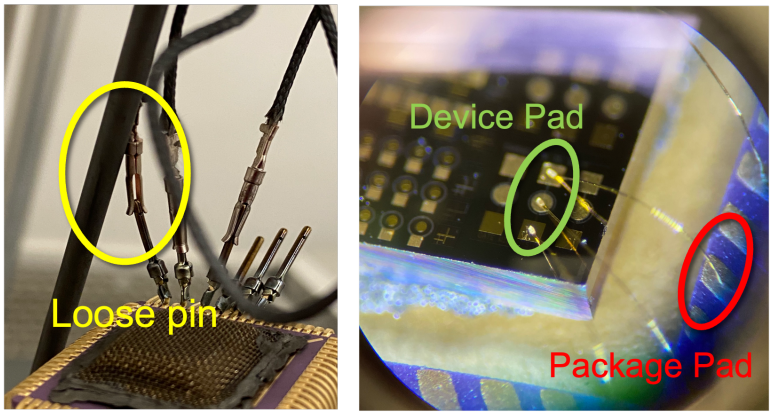

Figure 5.14: Optical image of the packaged sample inside the chamber with loose pin after 8.5 hours (left). Image of the device's source wirebond after 5 days 21 hours with pads labelled (right).

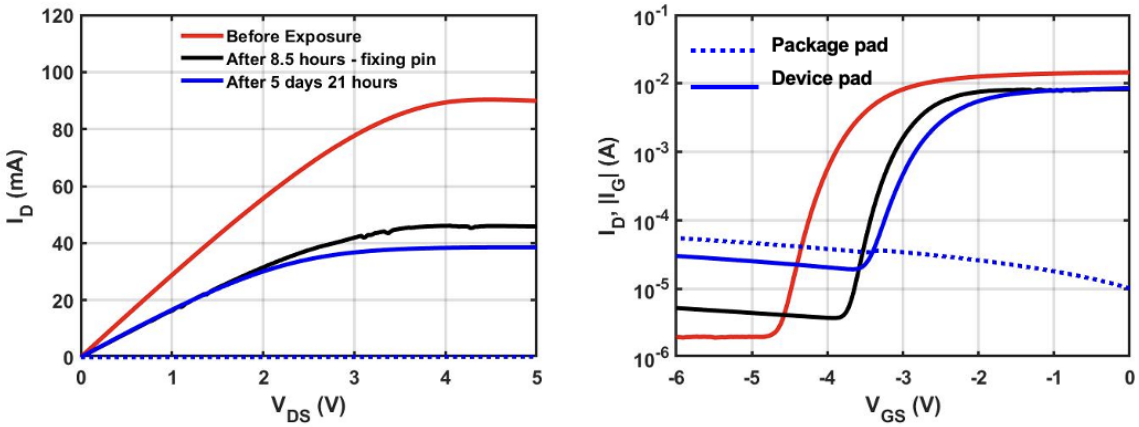

Figure 5.15: Electrical measurements taken at at 25°C initially (red) and at the 8.5 hour (black) and 5 day 21 hour marks (blue). Solid blue lines represent measurements taken touching the probes down on the device wirebonding pads; dashed blue lines represent measurements taken touching the probes down on the package wirebonding pads.

After 8.5 hours, the device appeared to have suffered electrical failure in the Venus

chamber. The drain current was extremely small and there was no gate control. The chamber was cooled down to room temperature and vented. Upon opening the chamber, it was apparent that one of the male pin connectors on the sample package had come loose from the female pin connector attached to the feedthrough wire. The loose pin was photographed and is shown in Figure 5.14. The disconnection was likely due to thermal relaxation of the feedthrough wires during Venus chamber exposure causing the tension in the wires, which were supporting the sample package, to change. After the loose pin was reattached, the device was operational again. At this time we took advantage of the pause in the experiment to collect sample data at room temperature, including optical microscope images and probe station measurements on both the active C-HEMT and a passive C-HEMT. In order to do so, the filter was removed from the top of the package and was not replaced due to the risk of knocking off wirebonds during the filter attachment process. The room temperature measurement on the active device collected on the probe station is shown in black in Figure 5.15. The sample was placed back into the chamber and hooked up to the feedthrough wires again. The chamber was pumped, purged, filled with CO_2, and brought directly back up to 465°C. The experiment was resumed.

After 5 days and 21 hours (141 hours total), including the first 8.5 hours of operation prior to the loose pin, the device again appeared to permanently fail. Upon cooling to room temperature, the device did not recover. The chamber was opened, and the pin connectors were examined. No obvious fault in the physical test setup could be found. The sample was removed from the chamber and characterized on the probe station. First, the probes were touched down on the gold package pads where the wirebonds terminated. The device electrical characteristics indicated device failure; there was virtually no drain current and complete loss of gate control (dashed blue lines in Figure 5.15). However, when the probes were touching down directly on the device's gold wirebonding pads, the device functioned properly. The device pads and package pads are circled on the image of the sample die in Figure 5.14. The tests conducted when the probes were in direct contact with the device pads are represented by the solid blue lines in Figure 5.15. Further testing revealed that the source wirebond was the cause of the issue, but under the optical microscope the wirebond looked normal and the bonds were verified to be intact by gently tugging on the ends with tweezers. This indicates that the wirebond suffered from a failure that was not externally visible. With no way to electrically contact the device source terminal *in situ* the chamber without a functioning wirebond, the experiment was concluded despite the

continued functional operation of the C-HEMT.

5.5.3 Results and Discussion

The output and transfer characteristics during heating at V_{GS}= 0 V and V_{DS} = 2 V, respectively, are shown in Figure 5.16. The drain current decreases with increasing temperature as expected due to reduced mobility [4]. The gate leakage current first decreases from 25°C to 200°C, and subsequently increases from 300°C to 465°C. The ON/OFF ratio follows the same trend. This phenomenon is indicative of the thermal activation of traps at moderate temperatures as the device stabilizes. In the future, DLTS could be used to confirm this theory. Nonetheless, the device retains good pinch-off and saturation characteristics across the temperature range with an ON/OFF ratio higher than 1×10^4 at 465°C.

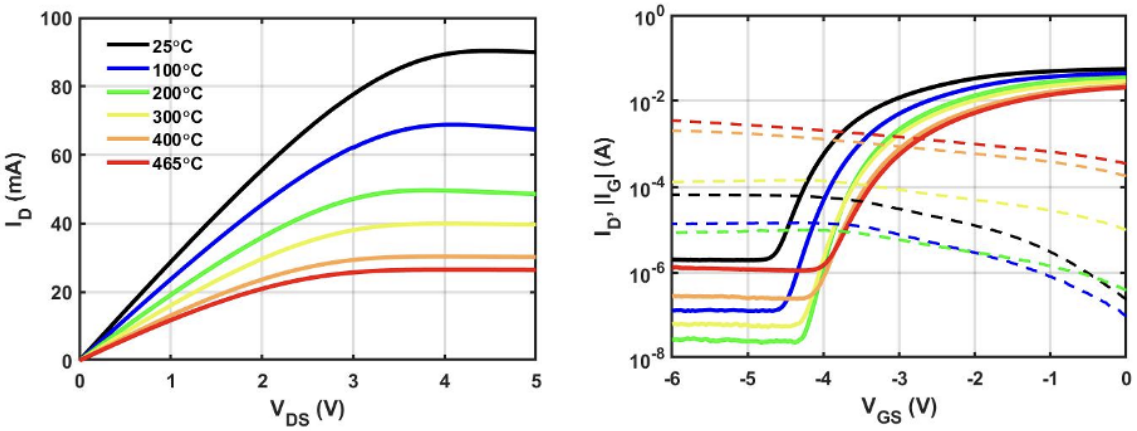

Figure 5.16: C-HEMT output (left) and transfer(right) characteristics collected during heating in the XLab Venus simulation chamber from 25°C to 465°C.

Figure 5.17 shows the device electrical data measured at 465°C at several time points over the duration of the Venus simulation. The device performance degrades the most substantially during the first 24 hours of the 141 hour experiment, after which point the rate of degradation slows and the device performance is largely stable.

The extracted key device parameters are shown in Figure 5.18, where it is apparent the most severe degradation occurs in the first 12 hours at temperature. The shift in the threshold voltage is due to the decrease in the drain saturation current seen in Figure 5.17. The ON/OFF ratio decreases in magnitude from 10^4 to 10^1 and the OFF-current increases from 10^{-6} to 10^{-3} A. The ON/OFF ratio decrease can only be partially explained by the

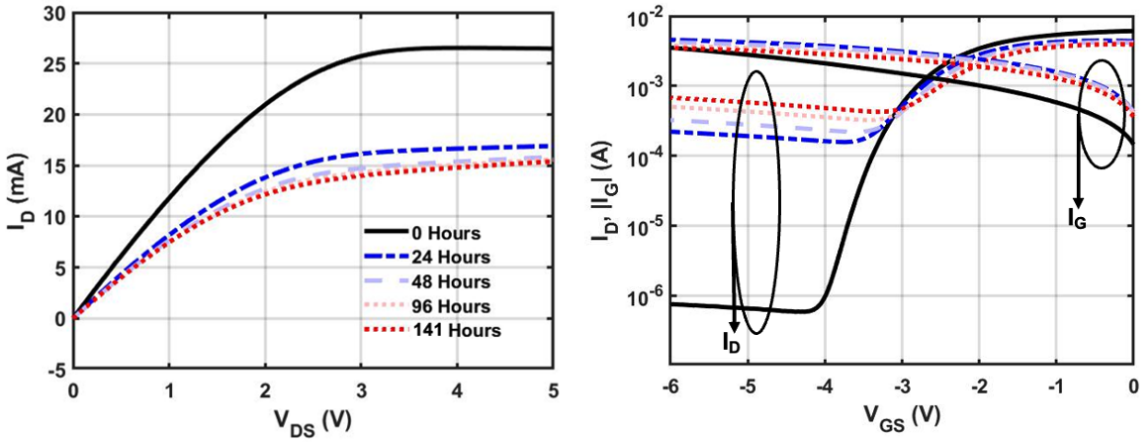

Figure 5.17: Select C-HEMT output (left) and transfer(right) characteristics collected at 465°C at various time points during the Venus simulation.

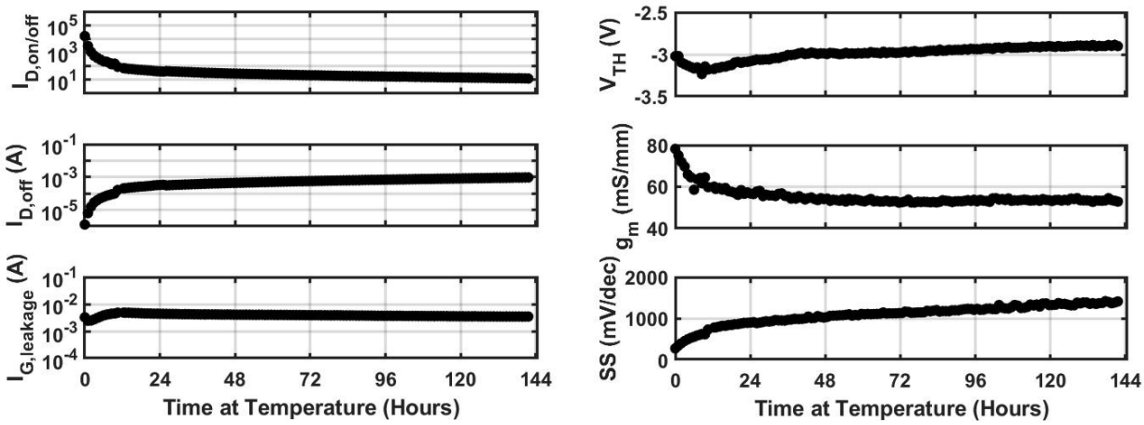

Figure 5.18: Extracted C-HEMT device parameters versus time at 465°C over the course of the experiment.

decrease in drain saturation current. Because the gate leakage current in the cut-off region experiences minimal increase over the time at temperature, the C-HEMT likely has another leakage path such as through the surface passivation. Alternatively, it is possible that the packaging itself (e.g. the wirebonds, package gold traces, electrical feedthrough wires) is introducing a parasitic pathway that is worsening with time at temperature. Further experimentation is needed, such as implementing four-point measurements, to negate any possible packaging effects on device performance. Still, this initial first demonstration of an InAlN/GaN C-HEMT operating under experimentally simulated Venus surface conditions

is promising; the device is operational after nearly 6 days; the drain current remains high and the gate still has control to modulate the 2DEG channel into the cut-off region.

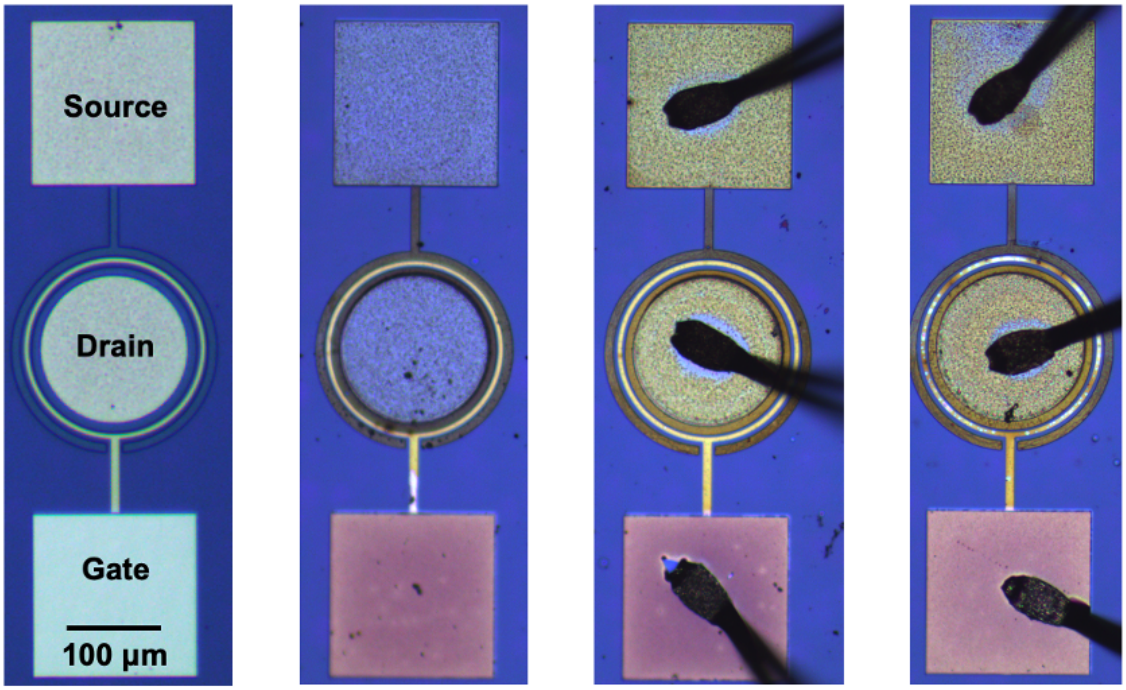

Figure 5.19: Optical images, from left to right: virgin DUT prior to experiment, unbiased device after the experiment, unbiased device with wirebonds after the experiment, and DUT after the experiment.

There were substantial visible discrepancies between C-HEMT devices with and without wirebonds, regardless of whether they were actively tested. The leftmost optical image in Figure 5.19 shows the virgin active C-HEMT prior to wirebonding and exposure to simulated Venus surface conditions. The image second from the left in Figure 5.19 shows a C-HEMT device that was on the sample die and exposed to Venus conditions but not biased. The device's source and drain wirebond pads have changed color from gold to blue, while the ohmic regions not covered by the Ti/Au wirebonding metal appear darkened brown. The gate wirebonding pad has changed color from gold to a brownish pink. Additionally, the gate region not covered by the Ti/Au wirebond metal appears brighter yellow gold in color. That could be due to material changes of the Al_2O_3 passivaiton layer overlaying the regions not covered in wirebond metal causing a change in the refractive index. In the third from the left image in 5.19, a C-HEMT device that was wirebonded but not tested *in situ* due to

the limited number of wires is pictured after the conclusion of the Venus chamber exposure. The appearance of the source and drain wirebond pads differs from the unbiased device that was not wirebonded shown in Figure 5.19 second from the left; the wirebonded device has gold colored ohmic pads. This indicates that the gold wirebond metal is diffusing down onto the ohmic device pads. Finally, the wirebonded device that was actively tested *in situ* the chamber is pictured after the exposure in the rightmost image in 5.19. The device also has golden source and drain probe pads, similar to the wirebonded but not electrically tested device shown in 5.19 third from the left. These results indicate that gold diffusion, precipitated by the gold wirebond, is occurring regardless of the application of an electrical bias. In other words, the diffusion is activated by the thermal conditions of the chamber and does not require the application of an electric field to move the metal, though it cannot be determined from these top-view images if electromigration effects have led to more severe metal diffusion in the actively tested device. Additionally, the active C-HEMT has several dark brown spots over the circular gate that are not seen on the passive wirebonded device. These spotted regions could be due to electromigration of the Mo/Au gate metal through the passivation layer on top, bubbling of the passivation due to localized self-heating of the gate, or another morphological change. Furhter material analysis such as SIMS depth profiling or cross-section STEM is needed to further qualify.

5.5.4 Conclusions

This first proof-of-concept experiment demonstrates that InAlN/GaN HEMTs can operate *in situ* extreme environmental conditions found on Venus. This experiment has pushed the boundary forward and demonstrated survival of this device type for nearly 6 Earth days, which is substantial progress towards the extended Venus surface mission goal of 60 Earth days. It was found that the Mo/Au-gated device improves performance up to 200°C in the chamber, above which the performance degrades. At 465°C, the most substantial shift in device characteristics is experienced in first 12 hours The experiment concluded due to a faulty wirebond and not device failure. Therefore, it is unknown how long the C-HEMT could have continued to operate past the 5 day and 21 hour duration. Additionally, the electrical results and optical microscopy indicate that the reliability of HEMTs for Venus surface exploration may not be limited by any part of the device, but instead limited by the packaging reliability. Advances in high temperature packaging technology, such as improved wirebonding or flip-chip technology, and circuit-level techniques to minimize

thermally activated parasitic pathways, would benefit the deployment of InAlN/GaN HEMT technology at high temperatures.

5.6 NASA GEER Implementation

5.6.1 Motivation

The NASA Glenn Extreme Environment Rig (GEER) facility is designed to simulate extreme environments, such as the Venusian surface. Previous research conducted at GEER facilities is described in Chapters 1, 2, and 3. Through High Operating Temperature Technology (HOTTech) grants awarded by NASA, this experiment allows for evaluation of technologies in the NASA GRC GEER facility under simulated Venus surface conditions towards demonstrating suitability for a long-lived lander on Venus. A variety of GaN heterostructure microelectronic devices and high-temperature packaging materials will undergo a 10-day passive exposure test inside of the 10-ton pressure vessel of the GEER chamber. Additionally, one InAlN/GaN C-HEMT device will be actively tested *in situ* during the same experiment. The GEER chamber experiment will be conducted at 470°C, 1350 psi and include the first nine chemical constituents by percentage understood to be in the Venus surface atmosphere listed in Table 1.1. The GEER chamber provides a higher fidelity replication of the Venus atmosphere than the University of Arkansas Venus simulation chamber (Section 5.2) and the XLab Venus simulation chamber (Section 5.3), which only included sCO_2 ambient. This will give valuable further insight into the chemical stability of the InAlN/GaN C-HEMT platform during exposure to the additional atmospheric trace constituents. The GEER chamber experiment for HOTTech devices has been delayed 2.5 years due to COVID-19 disruption to the schedule but is expected to commence in the near future (target: Winter 2023).

5.6.2 Passive Samples

A large quantity and variety of samples have been prepared for passive exposure testing inside GEER. Figure 5.20 shows six die fabricated by XLab members attached to an alumina board with 8835 gold paste to keep the die from moving around or flipping over inside of the GEER chamber. Five of the die are 5 mm x 5 mm InAlN/GaN-on-Si and AlGaN/GaN-on-Si: one Vulcan Run sample type #1, two Vulcan Run sample type #2, one Vulcan run

sample type #3, and one Vulcan Run sample type #4 (Table 3.2). Three of the die have HEMTs on them, and two of the die have Hall-effect sensors on them . Additionally, one 2 mm x 2 mm diamond die with 2-dimensional hole gas (2DHG) Hall-effect sensors and field-effect transistors is on the board [179]. Three III-N resonator samples prepared by collaborators at Jet Propulsion Laboratory, and five high-temperature packages prepared by the University of Arkansas are also included in the test.

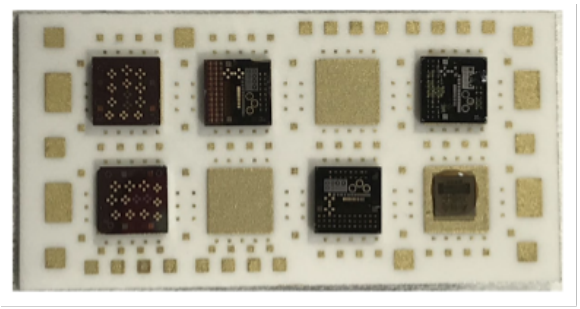

Figure 5.20: Image of board with six XLab die prepared for pasive GEER chamber testing.

5.6.3 Active Sample

The active test sample for the GEER chamber experiment is an InAlN/GaN-on-Si die. The chosen die has Ta/Ti/Al/Ni/Au ohmic metallization, IrO_x Schottky metallization, and no passivation layer. This corresponds to Casper Run sample type #7 in Table 3.3. The die was selected based on the promising results of the 10-day Venus simulation chamber exposure experiment described in Section 5.2 which showed improved post-exposure performance in unpassivated IrO_x-gated HEMTs. Various C-HEMTs, L-HEMTs, TLM, Schottky diodes, and leakage structures on the die were electrically characterized at 25°C in air using the Signatone probe station. The devices were visually inspected and imaged under an optical microscope. For redundancy, 3 C-HEMTs with $L_G = 1$ μm or 5 μm and $L_{CH} = 15$ μm or 20 μm were wirebonded at Stanford for *in situ* testing. Only one of these C-HEMTs will be electrically tested *in situ* GEER chamber due to a limited number of electrical feedthrough connections.

5.6.4 Packaging

The active test sample was packaged for *in situ* testing with assistance from Makel Engineering, Inc (MEI). The packaging is designed to allow the samples to be directly subjected

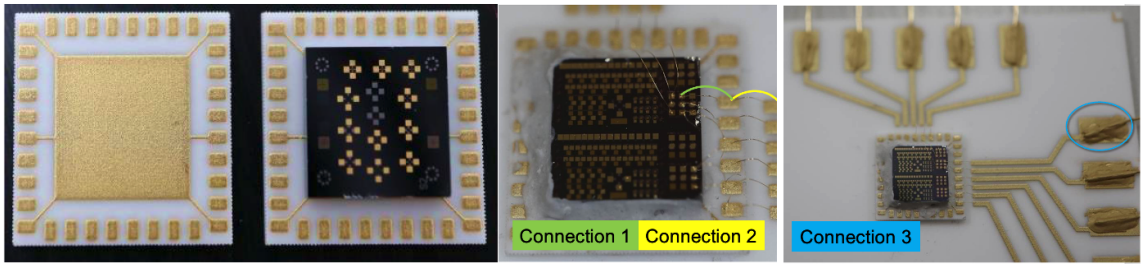

Figure 5.21: Images from left to right: chip carrier, chip carrier after attaching a test sample, active sample on chip carrier showing wirebond connections 1 and 2, active sample on chip carrier on multi-sensor package showing gold wire (connection 3). Leftmost two images courtesy of MEI. Die shown are 5 mm x 5 mm.

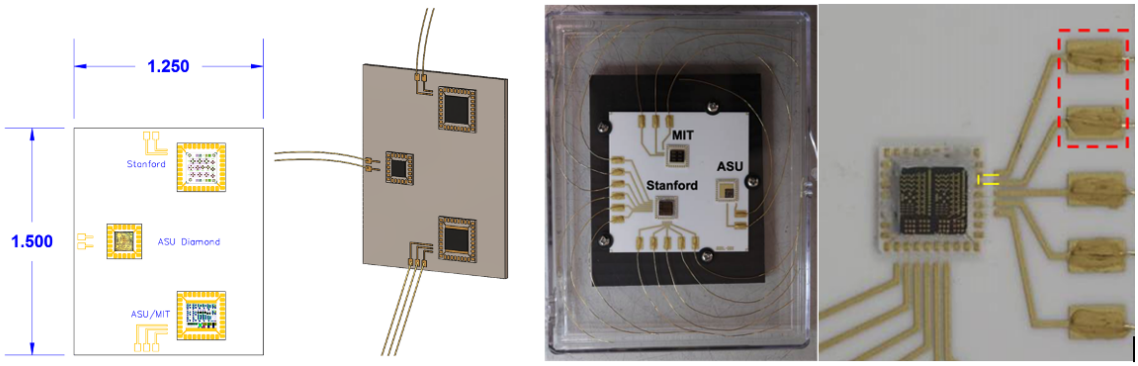

Figure 5.22: Images from left to right: draft schematic of the multi-sensor package design, 3D rendering of the multi-sensor package, the prepared multi-sensor package ready for testing, reference resistor on Stanford package with connections annotated by yellow and red lines. Schematic and 3D rendering courtesy of MEI.

to the full environmental conditions within the chamber and is intended to provide electrical connection only; it does not provide cooling or shielding of any kind. First, the active sample was attached to a 20-mil thick alumina chip carrier with a 4.5 mm die attach pad and gold traces. The sample was attached to the chip carrier using a high temperature aerospace grade inorganic compound epoxy, Aremco 571, and fired at 93°C in an oven to cure. Optical images of the bare chip carrier and a Stanford test sample attached to the chip carrier are shown in Figure 5.21. The chip carrier was attached to a larger 40-mil thick alumina multi-sensor package along with two additional samples on chip carriers fabricated by HOTTech collaborators at Massachusetts Institute of Technology (MIT) and Arizona State University (ASU). A mock-up of the multi-sensor package and a 3D rendered model

are shown in Figure 5.22. The dimensions of the final multi-sensor package and the number of gold traces differ from the model. An image of the final prepared muli-sensor package is also shown in Figure 5.22. The three C-HEMT devices were wirebonded from the device bond pads out to the gold traces on the chip carrier, labeled "Connection 1" in Figure 5.21. The gold traces on the chip carrier were also wirebonded out to gold traces on the multi-sensor package, labeled "Connection 2" in Figure 5.21. The gold traces on the multi-sensor package are affixed with 10-mil gold wires that will be attached to the electrical feedthrough wires running in and out of the GEER chamber for *in situ* device data collection (labeled "Connection 3 in Figure 5.21). In order to calculate the parasitic resistance of the ancillary device packaging (e.g. wirebonds, gold traces, and electrical feedthrough wires), a reference resistor was created by wirebonding between two gold traces on the Stanford chip carrier, which is schematically shown in the rightmost image of Figure 5.22. During the GEER chamber experiment, the resistance will be monitored *in situ*. This data can be used later to calibrate the DUT data to isolate device measurements from the electrically parasitic packaging. After packaging was completed, the electrical integrity of the multi-level wirebonds (Connections 1 and 2) were verified by $I - V$ measurements.

5.6.5 Automated Measurement Test Setup

A modified version of the auto measurement test setup described in Section 4.5.2 has been developed to collect electrical data on the Stanford, MIT, and ASU samples *in situ* GEER chamber. This modification effort was undertaken with collaborators at MIT. The primary difference between the two setups is that the SPA is swapped for two portable SMU devices. The parameter sweep values for the SMUs are designated in the PyVISA code, whereas on the SPA used in Section 4.5.2's setup the parameter sweeps were designated at the SPA itself. A block diagram of the setup is shown in Figure 5.23. A depiction of the test routine executed by the setup program is shown in Figure 5.24.

5.6.6 Conclusions

Samples have been prepared for both active and passive testing *in situ* NASA GEER, which is the highest fidelity replication of Venusian surface conditions on Earth. The active sample has been packaged using high-temperature compatible multi-level alumina and gold boards in conjunction with collaborators at MEI. The automated test setup has been modified with help from fellow HOTTech grant recipient research groups at MIT and ASU and

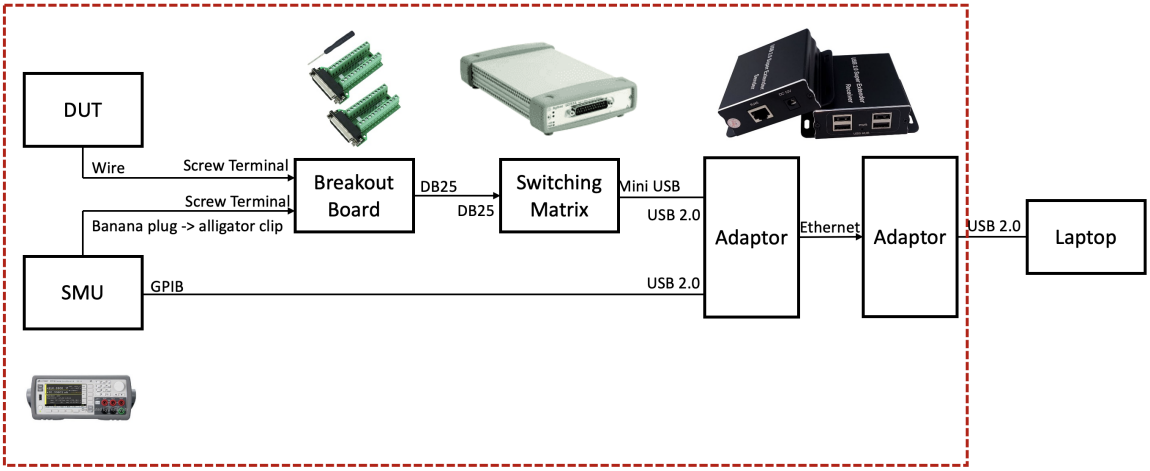

Figure 5.23: Block diagram of the automated measurement test setup developed for *in situ* device characterization at GEER. Diagram courtesy collaborator Mengyang Yuan at MIT.

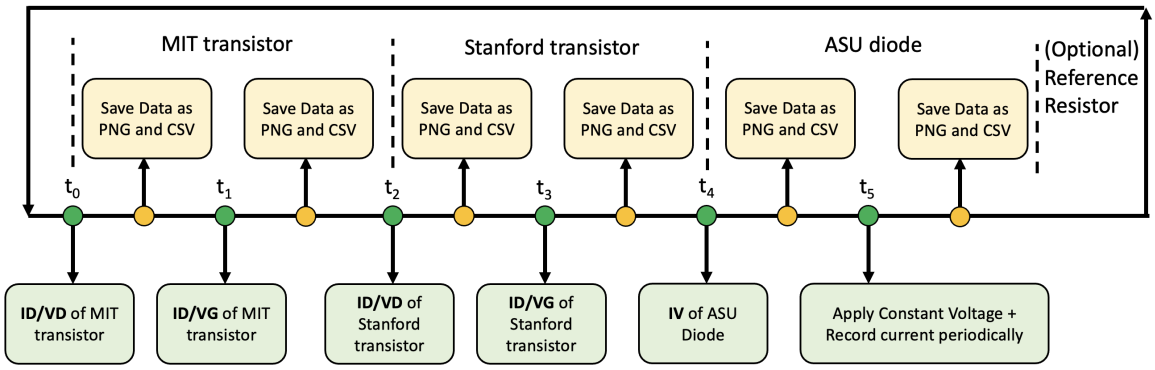

Figure 5.24: Diagram of the program executed by the Python program written for *in situ* device characterization at GEER. Diagram courtesy collaborator Mengyang Yuan at MIT.

will be used to collect *in situ* data on samples from all three institutions. In addition, a variety of passive samples will be placed in the chamber for exposure testing over the 10-day duration of the experiment. Passive and active samples have been electrically and optically characterized pre-exposure. Data collected *in situ* and post-exposure will be compared to the pre-exposure data. This experiment will be the most rigorous assessment of the viability of GaN heterostructure devices for Venus surface exploration to date.

Chapter 6

Conclusions

6.1 Thesis Summary

The motivation for this thesis was to develop suitable microelectronic devices that can reliably operate within the extreme environment conditions on the surface of Venus. Currently, the length and scientific agenda of proposed missions to Venus are restricted by the lack of capable electronics that can handle the scalding surface temperature of ≈465°C, which is above the operating limit of traditional silicon. Long duration missions to the surface of Venus are necessary to increase our understanding of the factors that influence the evolution of potentially habitable planets, such as how Venus and Earth diverged so drastically in their development. Towards this end, I have designed, microfabricated, and tested wide bandgap InAlN/GaN high electron mobility transistors (HEMTs), which can theoretically survive at Venusian temperatures and offer inherent radiation tolerance and chemical inertness. The HEMT device platform has the potential to be leveraged and modified for sensing, telecommunications, and power systems in one monolithically integrated chip to be deployed on-board a Venus surface rover or lander. Yet, key challenges remain to successful deployment of InAlN/GaN HEMTs in high temperature ambient. Towards this end, I have conducted research investigating the impact of device geometry, metallization schemes, and passivation layers on the high temperature operation of InAlN/GaN HEMTs in both oxidizing air and supercritical CO_2 ambient, which is the primary component of the Venusian atmosphere. Promising proof-of-concept experiments demonstrating uncooled InAlN/GaN heterostructure HEMTs with various metallization and passivation operating *in situ* simulated Venus surface conditions for long durations have been conducted. The high

temperature current transport mechanisms contributing to gate leakage current have been investigated in depth on novel IrO_x Schottky contacts. The circular device geometry and Al_2O_3 passivation have been identified as the superior combination for high temperature operation in air up to 600°C. In the first ever demonstration of a GaN heterostructure device operating *in situ* Venus surface conditions, an InAlN/GaN HEMT was successfully operated for 5 days and 21 hours inside of a custom built Venus simulation chamber. The outcome of this experiment is a a 70× improvement in operating length over traditional Si-based devices that lasted ≈2 hours on the Venusian surface even with the use of active cooling. Thus, this thesis work compels further maturating the InAlN/GaN HEMT platform for a new class of uncooled device solutions that will not only fulfill the need for suitable Venus microelectronics, but also open up new application spaces for uncooled microelectronics in additional high temperature oxidizing and corrosive ambient applications such as hyperpsonic re-entry systems, carbon capture and storage, and structural health monitoring for wind turbines and aircraft engines.

6.2 Key Contributions

The major technical contributions presented in this thesis are the following:

- Investigated the viability of multiple Schottky gate metallization schemes to InAlN for high temperature applications. The supression of leakage current up to 300°C in MoO_3-gated HEMTs was achieved. The high temperature current conduction in novel intentionally oxidized IrO_x Schottky contacts to InAlN/GaN was thoroughly analyzed, demonstrating successful operation up to 600°C. Furthermore, extended high temperature operation of Mo/Au-gated devices is demonstrated.

- Identified circular (C-HEMT) geometry and Al_2O_3 passivation as superior to the standard linear (L-HEMT) geometry and unpassivated barrier layers for high temperature applications in air.

- Designed and implemented a custom Venus simulation chamber in the laboratory, one of only a handful in the world, necessary to enable *in situ* device characterization.

- Characterized the impact of exposure to Venus surface conditions (sCO_2 atmosphere, 465°C, 92 bar) on GaN heterostructure devices. The results suggest the lattice-matched InAlN/GaN heterostructure is unaffected by the exposure while the AlGaN/GaN heterostructure may suffer from strain relaxation.

- Increased the technology readiness level (TRL) of the InAlN/GaN semiconductor platform from 2 to 5 by demonstrating the successful operation of an InAlN/GaN C-HEMT *in situ* simulated Venus surface conditions for the first time.

6.3 Ongoing and Future Work

- **NASA GEER Testing:** As discussed in Section 5.6, samples have been prepared for passive and active testing at NASA GEER facilities, where they will be exposed in a high-fidelity replication of Venusian surface conditions, including the primary chemical constituents in the atmosphere, for 10 days. The device selected for active electrical characterization over the course of the experiment is an unpassivated IrO_x-gated C-HEMT. The results of this experiment, which will be the most rigorous investigation of the InAlN/GaN semiconductor platform for Venus surface missions, will give valuable insight into the chemical stability of the selected HEMT device stack. Future work can build upon the findings from the GEER experiment to select or refine the material stack for the next iteration of InAlN/GaN HEMTs as necessary.

- **Improve XLab Venus Simulation Chamber Setup:** We plan to increase the fidelity of the simulated Venus environment through inclusion of N_2 and trace amounts of SO_2 in the XLab Venus simulation chamber. Outfitting the chamber with another feedthrough gland with more wires would allow for four-point measurement techniques to be implemented during device characterization, which would isolate the device performance from the parasitic resistance of the packaging. The packaging failure associated with the wirebonds prematurely ended the experiment characterizing the C-HEMT *in situ* the chamber, highlighting the need for further experimentation and iteration to determine the optimal sample packaging for use in the Venus chamber.

- **Failure Mode and Effects Analysis (FMEA):** Detailed material analysis of the various HEMT device stacks microfabricated over the course of this thesis work limited because it was outside of the scope. Instead, the spirit of this research was always

to design and fabricate an InAlN/GaN HEMT that could be demonstrated working under simulated Venus conditions. To this end, well-informed design decisions were made prior to the microfabrication process and iterated upon, and information on the performance of the materials in the stack was gleaned primarily by the electrical characterization. This leaves a lot of room for further materials failure analysis using techniques including but not limited to: SIMS depth profiling the gate and gate-mesa overlap region of IrO_x-gated HEMTs exposed to 600°C ambient (Section 4.3) to determine the oxide species and investigate gate sinking effects, detailed microscopy of the failed wirebond that necessitated the conclusion of the experiment characterizing the C-HEMT *in situ* the XLab Venus simulation chamber (Section 5.6), and XPS, Augur, EDS, and/or XRD to support the SEM analysis and investigate the metal out-diffusion from the ohmic contact and possible strain relaxation on the AlGaN/GaN photodetectors exposed to simulated Venus conditions (Section 5.2).

- **High Frequency Operation at High Temperatures:** The HEMT electrical characterization described in this thesis is limited to analog DC. High frequency analysis at both room and high temperature is the necessary next step to determine the merits of this device platform for RF applications, which will be necessary for on-board rover telecommunications and in some cases, to amplify and readout sensor data. In Chapter 1 we saw that limited large-signal analysis was performed by Maier *et al.* up to 1000°C in vacuum, which is promising. To achieve high frequency operation, the device geometry will need to be adapted from large-area to scaled gate lengths (submicron regime). This may prove a challenge to reliable high temperature operation because we have learned from this thesis work that the circular device platform is preferred to the linear format for high-temperature operation in oxidizing ambient. Careful and clever design will be necessary to maintain the shape factors that contributed to the success of the C-HEMT geometry such as a minimized gate-mesa overlap region while simultaneously scaling devices down in size.

- **Monolithic Circuit Integration:** As described in Chapter 1, the InAlN/GaN heterostructure allows for monolithic integration of various device architectures on one chip. In Chapter 3 we saw that multiple lateral device types have already been co-fabricated on one chip through this thesis work. In future microfabrication runs, the

mask could be modified to include a simple circuit designed to allow for HEMT readout from another sensor, such as a Hall-effect plate or micro-pressure sensor. The circuit complexity could be further increased in the future. The chip would reap the benefits of uncooled monolithic integration such as reduced footprint and cost savings from co-fabrication. This would be an advantage over traditional heterogenous integration strategies employed for GaN devices that require a silicon ASIC, which cannot be operated in high temperature ambient without cooling.

- **Radiation Testing:** The circular HEMT geometry lends itself to radiation tolerance, as discussed in Section 3.4. Furthermore, the WBG of the InAlN/GaN heterostructure infers inherent radiation tolerance compared to traditional Si microelectronics. Similarly to the case with high-temperature space applications, radiation-rich space applications would benefit from rad-hard electronics that can function without the need for shielding, which can be bulky and costly. Therefore, it would be intriguing to subject the InAlN/GaN C-HEMT device architecture to single event effect (SEE) or total ionizing dose (TID) radiation testing to investigate its potential for use in other space applications where radiation is a primary cause of microelectronic device failure.

6.4 Concluding Remarks

Excitingly, NASA has demonstrated renewed interested in funding dedicated Venus missions in just the last few years. In February 2020, NASA selected two new missions to Venus as part of the Discovery Program. Each mission was awarded approximately $500 million, and they're both expected to launch in the 2028-2030 timeframe. The DAVINCI+ (Deep Atmosphere Venus Investigation of Noble gases, Chemistry, and Imaging) mission will send both an orbiter and a descent probe to Venus and measure the composition of the atmosphere and take high-resolution images of the surface on the way down, though it is not expected to operate on the surface. The VERITAS mission consists of an orbiting spacecraft equipped with a synthetic aperture radar. VERITAS will chart surface elevations to 3D reconstruct the topography and confirm whether processes such as plate tectonics and volcanism are still active on Venus. While neither of these missions will operate on the surface, they are certainly a step in the right direction towards learning more about our sister planet. NASA's many missions to Mars over the past 70 years, which have included

nine orbiters and eight landers or rovers, have shown us that planetary exploration triggers public fascination. It is the hope of this Venus enthusiast that the two upcoming missions to Venus result in similar public interest and prompt the funding of further exploration of Venus, including the surface. Perhaps by the time NASA awards a long-lived Venus surface mission, we will have addressed the microelectronics technology gap with future maturation of uncooled InAlN/GaN high electron mobility transistors. In the meantime, GaN semiconductor technology will continue to revolutionize extreme environment, high power, and high frequency terrestrial and space applications. The future is bright for Venus.

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Appendix A

Microfabrication Runsheet

This Appendix contains the runsheet used during microfabrication of Casper run devices as described in Chapter 3.

Step					Equipment		Temperature	Pressure	Chemicals	RF power	Thickness
0	Clean										
	0.1	Dehydrate	5 mins		hotplate		110C				
	0.2	SRS100	20 mins	Water bath after	wbflexcorr		60C				
	0.3	SC1	10 mins	Water bath after	wbflexcorr		50C				
	0.4	SC2	10 mins	Water bath after	wbflexcorr		50C				
	0.6	Blow dry w/ N2 gun			wbflexcorr						
1	Mesa Litho										
	1.1	Dehydrate	5 minutes		hotplate		170C				
	1.2	HMDS	~20 mins		YES oven						
	1.3	Spin resist	40 sec		headway	5500 rpm			shipley 3612		1 um
	1.4	Pre-bake	1 min		hotplate		90C				
	1.5	Exposure			Heidelberg						
	1.6	Post Exp Bake	1 min		hotplate		115C				
	1.7	Develop	1 min		teflon baskets				MF 26A		
	1.8	Inspection			microscope						
	1.9	Hard bake	5 min		hotplate		110C				
2	Mesa Etch										
	2.1	Clean	15 mins	use Si dummy	OxIII-V	Clean			SF6, O2 plasma		
	2.2	Season	15 mins	use SiO2 wafer	OxIII-V	GaN Slow Etch	20C	10mT	BCl3 (25sccm), Cl2 (10sccm)	250 W ICP, 80 W Forward	
	2.3	AlGaN/GaN etch	60 s	No mounting needed	OxIII-V	GaN Slow Etch	20C	10mT	BCl3 (25sccm), Cl2 (10sccm)	250 W ICP, 80 W Forward	
	2.4	Inspection		clean PR of dummy	alphastep/AFM						
	2.5	AMI rinse							Acetone, Methanol, IPA		
3	Dicing										
	3.1	Spin Sp 3612	60 s		headway	5500 rpm			shipley 3612		1 um
	3.2	Hard Bake	5 min				115C				
	3.3	Disco Saw			Hub blade	Si recipe					
4	Clean										
	4.1	Dehydrate	3 mins		hotplate		110C				
	4.2	Descum	3 min		drytek	Follow recipe					
	4.3	AMI rinse									
	4.4	SRS-100	20 mins		wbflexcor 2		60C				
	4.5	Rinse	2 mins						DI water		
	4.6	Blow dry									
	4.7	AMI rinse							Acetone, Methanol, IPA		
5	Ohmic metal litho										
	5.1	Dehydrate	5 minutes		hotplate		110C				
	5.2	HMDS	30 mins		YES oven				Skip step if LOL after		
	5.3	Spin LOL	30 sc		headway	3000 rpm			LOL		
	5.4	Bake	5 min		hotplate		170C				
	5.5	Spin resist	60 sec		headway	5000 rpm			shipley 3612		1 um
	5.6	Pre-bake	1 min		hotplate		90C				
	5.7	Exposure			Heidelberg						
	5.8	Post Exp Bake	1 min		hotplate		115C				
	5.9	Develop	30 sec	teflon baskets					MF 26A		
	5.10	Inspection			microscope						
	5.11	Hard bake	5 min		hotplate		110C				
	5.12	Descum			drytek2	program 1					
	5.13	Weak ammunium hydroxide	10 sec	1L beaker	wbflexcorr				1:20 Amonium hydroxide to water		
6	Ohmic metal evaporation										
	6.1	Metal evaporation			Give to Tom Carver in SNSF	Ti/Al/Mo/Au					25/100/40/100
7	Liftoff										
	7.1	Soak in Solvent	overnight				RT		1165		
	7.2	AMI rinse	immediately						Acetone, Methanol, IPA		
	7.3	Dehydrate	5 min		hotplate		110C				
	7.4	SRS-100	20 mins		wbflexcorr		60C				
	7.5	AMI rinse							Acetone, Methanol, IPA		
	7.6	Dehydrate	5 min		hotplate		110C				
8	RTA										
	8.1	RTA	35sec	run dummies first	awin r	P 850 N2	850C	30s			
9	Schottky litho										
	9.1	Dehydrate	5 minutes		hotplate						

	9.2	HMDS	30 mins		YES oven						
	9.3	Spin LOL	30 sc		headway	3000 rpm					
	9.4	Bake	5 min		hotplate		160C				
	9.5	Spin resist	60 sec		headway	5000 rpm			shipley 3612		1 um
	9.6	Pre-bake	1 min		hotplate		90C				
	9.7	Exposure			Heidelberg						
	9.8	Post Exp Bake	1 min		hotplate		115C				
	9.9	Develop	30s		teflon baskets				MF 26A		
	9.10	Inspection			microscope						
	9.11	Hard bake	5 min		hotplate		110C				
	9.12	Descum			drytek2	program 1					
10	Schottky metal evaporation										
	10.1	Metal evaporation			Give to Tom Carver in SNSF				30nm Mo on some samples, 15nm Ir on others		
11	Liftoff										
	11.1	Soak in Solvent	overnight				RT		1165		
	11.2	AMI rinse	immediately						Acetone, Methanol, IPA		
	11.3	Inspection			microscope						
	11.4	RTA of gate metal if necessary									
12	Dicing										
	12.1	Spin Sp 3612	60 s								
	12.2	Hard Bake	5 min				115C				
	12.3	Disco Saw			Hub blade	Si recipe					
13	Passivation Deposition										
	13.1	Thermal Al2O3 ALD	Target 25 nm		Fiji2				30nm Mo on some samples, 15nm Ir on others		
14	Pass Etchback Litho										
	14.1	Dehydrate	5 minutes		hotplate		170C				
	14.2	HMDS	~20 mins		YES oven						
	14.3	Spin resist	40 sec		headway	5500 rpm			shipley 3612		1 um
	14.4	Pre-bake	1 min		hotplate		90C				
	14.5	Exposure			Heidelberg						
	14.6	Post Exp Bake	1 min		hotplate		115C				
	14.7	Develop	1 min		teflon baskets				MF 26A		
	14.8	Inspection			microscope						
	14.9	Hard bake	5 min		hotplate		110C				
15	Pass Etchback										
	15.1	Dehydrate	3 mins		hotplate		110C				
	15.2	BOE dip	1 min		wbflexcor 2						
	15.3	Rinse	2 mins						DI water		
	15.4	Blow dry									
16	Bond Pad litho										
	16.1	Dehydrate	5 minutes		hotplate						
	16.2	HMDS	30 mins		YES oven						
	16.3	Spin LOL	30 sc		headway	3000 rpm					
	16.4	Bake	5 min		hotplate		160C				
	16.5	Spin resist	60 sec		headway	5000 rpm			shipley 3612		1 um
	16.6	Pre-bake	1 min		hotplate		90C				
	16.7	Exposure			Heidelberg						
	16.8	Post Exp Bake	1 min		hotplate		115C				
	16.9	Develop	30s		teflon baskets				MF 26A		
	16.1	Inspection			microscope						
	16.11	Hard bake	5 min		hotplate		110C				
	16.12	Descum			drytek2	program 1					
17	Bond Pad metal evaporation										
	17.1	Metal evaporation			AJA evaporator				30nm Mo on some samples, 15nm Ir on others		
									Ti/Au		20/200 nm
18	Liftoff										
	18.1	Soak in Solvent	overnight				RT		1165		
	18.2	AMI rinse	immediately						Acetone, Methanol, IPA		
	18.3	Inspection			microscope						
	18.4	RTA of gate metal if necessary									
19	Dicing										
	12.1	Spin Sp 3612	60 s								

	12.2	Hard Bake	5 min				115C				
	12.3	Disco Saw			Hub blade	Si recipe					
13	Clean										
	13.1	SRS-100	20 mins		wbflexcor 2		60C				
	13.2	AMI rinse	2 mins						DI water		
	13.3	Blow dry									
	13.4	Inspection			microscope						