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Development of a Rapid Fatigue Life Testing Method for Reliability Assessment of Flip-Chip Solder Interconnects

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Development of a Rapid Fatigue Life Testing Method for Reliability Assessment of Flip-Chip Solder Interconnects

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by

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Abstract

The underlying physics of failure are critical in assessing the long term reliability of power packages in their intended field applications, yet traditional reliability determination methods are largely inadequate when considering thermomechanical failures. With current reliability determination methods, long test durations, high costs, and a conglomerate of concurrent reliability degrading threat factors make effective understanding of device reliability difficult and expensive. In this work, an alternative reliability testing apparatus and associated protocol was developed to address these concerns; targeting rapid testing times with minimal cost while preserving fatigue life prediction accuracy. Two test stands were fabricated to evaluate device reliability at high frequency (60 cycles/minute) with the first being a single-directional unit capable of exerting large forces (up to 20 N) on solder interconnects in one direction. The second test stand was developed to allow for bi-directional application of stress and the integration of an oven to enable testing at elevated steady-state temperatures. Given the high frequency of testing, elevated temperatures are used to emulate the effects of creep on solder fatigue lifetime. Utilizing the mechanical force of springs to apply shear loads to solder interconnects within the devices, the reliability of a given device to withstand repeated cycling was studied using resistance monitoring techniques to detect the number of cycles-to-failure (CTF). Resistance monitoring was performed using specially designed and fabricated, device analogous test vehicles assembled with the ability to monitor circuit resistance *in situ*. When a resistance rise of 30 % was recorded, the device was said to have failed. A mathematical method for quantifying the plastic work density (amount of damage) sustained by the solder interconnects prior to failure was developed relying on the relationship between Hooke's Law for springs and damage deflection to accurately assess the mechanical strength of tested devices.

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I would like to thank Dr. Huitink for the opportunity to discover new things about myself, and for challenging me to push the boundaries of my knowledge and abilities.

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C. J. Marbut, M. Montazeri and D. R. Huitink, "Rapid solder interconnect fatigue life test methodology for predicting thermomechanical reliability," Transactions on Device and Materials Reliability, vol. 18, no. 3, p. 412-421, June 2018.

List of Unpublished Papers

Chapter 2 -
C. J. Marbut and D. R. Huitink, "Review of Accelerated Testing Methods for Accessing Reliability of Electronic Packages," Journal of Electronic Packaging, pending, 2019

1. Introduction

The exponentially growing dependence upon electronics in many aspects of everyday life and in the world economy has placed great importance on electronics reliability. In the case of flip-chip devices such as ball-grid arrays (BGA), the critical components for determining reliability are most often the solder interconnects that join the die and substrate which endure thermomechanically induced stresses during operation. These stresses are induced through a phenomenon known as "coefficient of thermal expansion (CTE) mismatch", where large differences in CTE for the dissimilar materials of the package result in non-uniform expansion rates across the device. For the interconnects, the result of this non-uniformity are induced tensile or compressive stresses which lead to elastic and plastic deformation within the joints. Creep and fatigue induced crack nucleation and propagation weakens the mechanical integrity of the joints while simultaneously degrading electrical performance. Extensive cracking leads to increased electrical resistance within the circuit and once the plastic deformation (damage) becomes severe, the resistance increases will exceed sustainable levels and the device will cease to function correctly or even at all, a situation know as device death.

Current accelerated testing methods for assessing fatigue lifetime (useful life) of electronic packages focus on simulating this CTE mismatch through thermal cycling in an environmental chamber or power cycling induced heat generation using the device itself. In both cases an acceleration factor is used to simulate the manifold cycles of an operational lifetime of the device but on a truncated time scale. These methods have been in use for many decades and are well understood, however, they are also characterized by long test durations, high costs, and difficulty quantifying induced stress levels and mechanistic effects within the devices themselves. To address these weaknesses with traditional testing methods, a new testing

methodology was devised relying on mechanical inducement of stresses within flip-chip solder interconnects through quantifiable means.

A rapidly accelerated test method was created where through the use of springs and cyclic linear translation, shear stresses were induced in the solder interconnects of tested devices to simulate the fatigue behavior of devices under operation or traditional accelerated life testing. Under actual operating conditions, creep and fatigue occur alongside other damage processes such as diffusion, recrystallization, electromigration, and current crowding. With all of these threat factors comingled, it is difficult to define the amount of damage attributed to any one mechanism and quantifying the effects temperature and stress have on damage accumulation behavior becomes obscure. The rapid methodology allows the isolation of stress based failure mechanism to allow for greater understanding of the underlying failure mechanics at work. Extensive reductions in total test duration were also targeted in the design of this method to reduce time for design feedback and costs associated with extended test duration. The ability to conduct tests on actual functioning devices with relevant geometries while monitoring both mechanical fatigue and electrical performance *in situ* was a primary objective for this testing methodology. Additionally, the *in situ* characterization provides a wealth of data for use in assessing and quantifying failure mechanisms and metrics enabling a more holistic understanding of the factors influencing the reliability of a given device.

The following articles are included in this work to elaborate on current state of the art in accelerated testing, the methodology behind this novel accelerated testing method, and the performance of this new approach in practice. These articles were published or are pending publication and were originally written with an eye toward inclusion within this thesis and it is believed that they provide a comprehensive view of the field, the scope and objectives of this testing methodology, and the results that were achieved through its implementation.

2. Review of Accelerated Testing Methods for Accessing Reliability of Electronic Packages

Cody J. Marbut and Dr. David R. Huitink

Increasing demand for higher power, small form-factor devices has created new challenges for device reliability optimization. Smaller form factors while simultaneously providing higher power levels mean higher energy density which lead to higher operating temperatures. These temperatures have a very large impact on device reliability because of coefficient of thermal expansion (CTE) mismatch which induces mechanical stresses within the dissimilar materials of the device. These stresses are induced when the CTE of one material is not roughly equal to the CTE of an adjacent material. As these dissimilar materials heat up they will expand at different rates. This expansion will induce tensile or compressive stresses within the device (see Figure 2-1). Solder joints have been shown to be one of the components most vulnerable to these induced stresses. These stresses can cause both elastic and plastic deformation within these joints. The irreversible plastic deformation is predominantly due to creep and fatigue which ultimately leads to crack nucleation. When these cracks propagate across the solder material, the resistance of the joint increases until electrical failure is achieved rendering the device non-functional [[1]-[3]]. Ensuring mechanical reliability of power devices requires designers to engineer against void formation/propagation and evaluate existing devices for fatigue life. Evaluating the fatigue life or operating cycles-to-failure (CTF) is most often done through accelerated testing (AT).

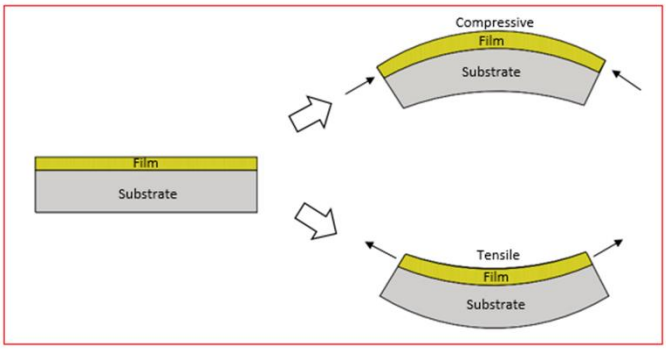

Figure 2-1: Results of CTE mismatch.

Accelerated testing experiments are conducted to collect information regarding predicted lifetimes and prominent failure modes within a given device. These tests are considered "accelerated" because test units are subjected accelerating variable levels far higher than those expected in real-world operating conditions using one or more accelerating variables such as temperature or stress [4]. This is done in an effort to acquire useful reliability data within a reasonable time window for an experiment (hundreds of hours rather than potentially tens-of-thousands of hours in actual operation). Lifetime at these accelerated conditions is then used to predict the operating lifetime (OLT) under standard conditions. Extrapolation of OLT is typically conducted using physically derived or empirically fitted models when a statistically significant amount of previous data is collected with similar test units. The two predominate types of accelerated testing used in industry are "quantitative" and "qualitative" accelerated tests. Quantitative tests are used to obtain failure-time data and degradation distribution for validating prediction models. Qualitative tests are used to test for product weaknesses and to study the root causes of device failure [4].

The primary requirements of an accelerated test are rapid results and accurate simulation or real-world failure mechanisms. For a testing method to yield beneficial results, it must induce causes and symptoms of failure congruent with those observed or expected in devices operating

under actual design conditions. In an effort to satisfy these requirements across a wide range of accelerating variables and applications, a large number of testing methods have been devised. Currently, the three most widespread AT methods used in electronic device reliability assessment are thermal cycling, power cycling, and thermal shock testing. Each of these methods has been used in industry quite successfully to develop expectations for device OLT. However, there are limitations to these methods such as duration and expense. To address these limitations, several novel AT techniques have been developed to provide much faster results at lower costs. This paper will examine the strengths and weaknesses of both these traditional and novel techniques for solder joint reliability assessment.

2.1 Common Accelerated Testing Methods

2.1.1 Thermal Cycling

Thermal cycling (TC) tests are conducted to evaluate the reliability of components and interconnects when subjected to mechanical stresses induced by alternating temperature extremes as an approximation of temperature swings during operation [5]. This is done in an effort to simulate the rise from low temperature to high temperature as a device powers on and begins to heat up to peak operating temperature followed by the drop as the device cools to the initial temperature (power off). To conduct the test, the test unit is placed inside a closed environment capable of transferring the device from one zone of high temperature (high setpoint) to another of low temperature (low setpoint). The test unit is made to remain in each zone for a specified dwell (soak) time which is the total time the device is to be at a given temperature for each cycle. The device is subjected to the temperature range for a specified number of cycles or until failure, as defined by the operator, occurs. Standards such as JESD22-A104D specify temperature ranges and soak times for specific certifications and ratings.

Ramp rate, dwell time, temperature range, and total number of cycles may all impact the overall acceleration factor (a metric for determining severity) of the test and their influence is dependent on failure mechanics and material properties involved. Increases in ramp rate can increase the strain rate experienced within the solder joints making ramp rate a useful acceleration variable for detecting weaknesses in the device which have a thermal rate-dependence [6]. Typically, a higher ramp rate will result in more damage accumulation over the course of the test. Dwell time serves to ensure that the test unit has reached the desire steady-state temperature. Generally, longer dwell times correspond to higher acceleration factors, especially at higher temperatures. This is due to creep behavior in the solder material which result from the high ratio of steady-state temperature to melting point, called the homologous temperature. Creep can occur if the testing temperature is greater than 0.45 to 0.6 of the absolute melting temperature for the solder material [[7]-[11]]. Additionally, longer dwell times lead to longer test durations, a result that is not always desirable in an "accelerated" test. When conducting a temperature cycling test, it is important to note that higher ranges between temperature extremes induce more strain into the device. During testing, failure can be monitored by collecting electrical performance data like resistance, and visual inspection can be used to detect crack formation. Cyclic rates of 1 – 3 cycles per hour (cph) are common. Depending upon the desired failure mechanism, faster rates can be used. Fatigue, cracking, delamination, ball bond integrity failure, and creep are common among flip-chip devices [[12],[13]].

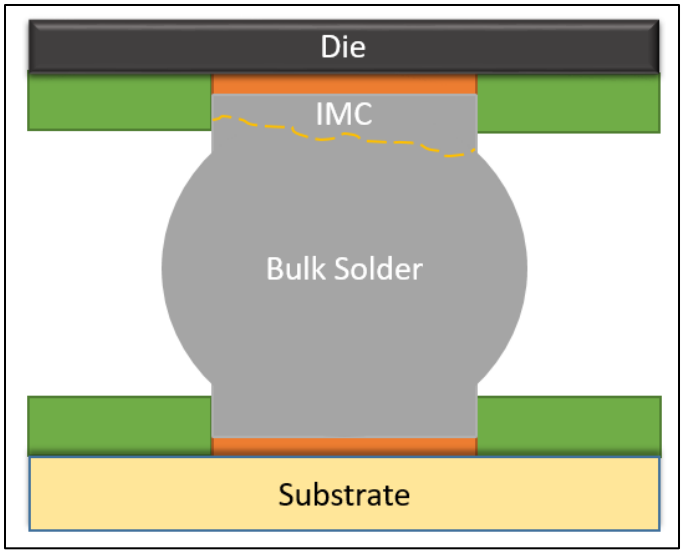

Figure 2-2: Interfacial cracking in solder interconnect.

The most commonly, fatigue cracking occurs between the bulk solder and the intermetallic layer in what is known as the interfacial region. Crack propagation is based upon the micro-structure and mechanical properties of the bulk solder [14]. Recrystallization of Sn is induced by thermal strain and elevated temperature, starting in the highly strained regions before expanding through the bulk material [12]. Due to a network of high-angle grain boundaries which extend through the interconnections and provide favorable propagation paths, recrystallization has been shown to enhance fatigue cracking [[12], [13]]. Recrystallization and dislocation motion are expected to be more thermally active at higher temperatures, causing a drastic decrease in shear strength [15]. The stress/strain distribution within the bulk material undergoing a thermal fatigue process has been shown to be non-uniform. Non-uniformity in the bulk material leads to grain slipping and plastic work accumulation with cycling [[12], [13]]. In moderate thermal stress states, strain can be released through plastic relaxation such as global recrystallization and solder exclusion. Once stress magnitude increases until plastic relaxation is not possible, crack initiation begins in the area of highest stress. Cracks are then propagated

through local recrystallization of solder grains. Thus, it can be said that the damage found in solder interconnections under thermal strain results from dislocation densities in the plasticized regions and increases with the accumulation of internal energy [[12]-[16]].

Thermal cycling has been used to evaluate solder reliability across a vast array of applications, though that list is too long to include here. Experiments of the reliability of all manner of devices from wafer level chip-scale packages (WLCSP) to full-scale power modules have been performed using thermal cycling techniques [[10],[17],[18]]. Sitek et. al. used thermal cycling to compare the reliability of long FR-4 and metal core PCBs, finding that solder interconnects on FR-4 substrates were two times more reliable than those on aluminum core circuit boards [19]. Singh et. al. determined that boards made using high-CTE glass had nearly five times the useful life (5300 cycles to 1100 cycles) of low-CTE glass substrates due to narrower difference between substrate and solder CTE [20]. In efforts to shorten test duration, more accurately simulate real-world conditions, or simply to explore new stress states, many researchers have begun combining thermal cycling with electrical or mechanical stress inducers. Such efforts are discussed in section 2.2.

2.1.2 Thermal Shock

Thermal shock (TS) testing is conducted to evaluate the reliability of electronic devices when exposed to sudden, drastic changes in temperature [21]. The device is transferred between extremes (hot – cold) with a transfer time not exceeding 20 seconds [21]. This ramp time must be short to ensure that the device experiences sudden, rapid temperature change rather than the more gradual temperature gradients seen in TC experiments. The test is designed to bring the device(s) to worst-case load temperature within a specified dwell time as measured by a thermocouple embedded in the body and located at the center of the heat load. The worst-case

load temperature is defined by the nature of the test and must adhere to standard within a specified range. Failure is assessed if parametric limits are exceeded, if hermeticity cannot be demonstrated, or if the device is non-functional after testing [21].

Some researchers have claimed that TS tests are more efficient than TC testing because they exhibit higher ramp rates and shorter MTTF values [[22], [23]]. However, care should be taken when conducting TS tests because failure modes are highly susceptible to thermal gradients that arise in the material [23]. The thermal gradients that develop in TS tests are higher than those created in TC testing. These thermal gradients contribute to buildup of inelastic strain. In a comparative study of thermal cycling and thermal shock tests, de Vries et. al. found that 1.5% of the total plastic strain in TS testing was attributed to inelastic strain [23]. In the case of TC testing, de Vries et. al. found no inelastic strain in the solder material. In TC testing, the primary source of stress is un-equal expansion due CTE mismatch between component materials. The presence of thermal gradients can induce additional stresses within the solder interconnects under TS testing conditions. The magnitude of these additional stresses will be dependent upon the thermal behavior of the test device under TS conditions [23].

Failure mechanism in solder interconnects under TS conditions are similar in many ways to failure mechanisms observed in interconnects stressed under TC conditions. Crack initiation in the interfacial region propagating into the bulk solder material precipitated by intermetallic compound (IMC) growth [[22]-[26]]. Tian et. al. found that this IMC growth was driven primarily by bulk diffusion and grain boundary diffusion within the microstructure of the solder material [26]. The presence of both thermal gradients and diffusion within solder interconnects under TS conditions can obscure or alter the failure mechanisms from those seen in real-world conditions, negatively impacting reliability predictions. Diffusion has been shown to follow

thermal gradients, creating the potential for radically different diffusion paths in some cases [27]. The magnitude of the impact on prediction accuracy would depend on the materials under study and the constraints of the test. Tian et. al., reported that the observed fracture behavior of SAC 305 interconnects transitioned from ductile fracture to brittle fracture modes as the number of TS cycles increased [26]. Anselm and Ghaffarian found that isothermal aging prior to thermal shock testing resulted in improved reliability for tin-lead solder quad flat no lead (QFN) assemblies [28].

2.1.3 Power Cycling

Power cycling (PC) tests are conducted to evaluate the ability of a device to withstand the stresses generated by CTE mismatch and non-uniform temperature distributions created by the on-off operating cycles of the device [29]-[[30]]. Unlike the other tests described above, in PC testing, the device, or internal or external heat source is supplied a current to simulate operating behavior and temperature range in a real-world environment. The power cycle ranges used in this test are designed to simulate the range of usage conditions. Unlike the other traditional tests, PC tests are not always specifically designed as highly accelerated tests or to create harsh conditions. This test is used to verify the performance of the component materials within the device, especially the solder interconnects [29].

The device is run through a prescribed temperature range, for a set number of cycles once the device is powered and the temperature extremes are calibrated. There are four main test types: constant power, variable power, constant cooling, and variable cooling [8]. The failure criteria once again include: parametric limits are exceeded, hermeticity cannot be demonstrated or if the device is non-functional after testing due to mechanical damage [29].

Comparative analysis of power cycling and thermal shock tests has shown that the primary cause of failure was generally the same. Crack nucleation and propagation assisted by recrystallization resulting from energy provided by the mechanical stresses generated during cycling was identified as the primary failure mode for both tests [31]. More detailed analysis revealed some key differences. Under power cycling conditions, IMC growth was accelerated. Researchers linked this to electromigration of Sn and Cu in the solder matrix, resulting in higher Sn flux and increased Cu6Sn5 growth at the anode side of the interconnect [31]. Additionally, recrystallization was seen to occur earlier during power cycling testing. This was attributed to the higher average temperatures, localized heating, and current flow related to PC testing [31]. In comparison with TC testing, higher maximum stresses developed in power cycling tests. This is largely due to the non-uniform temperature distribution common to most devices. Generally, a larger amount of temperature change is experienced by the die than the PCB which is not the case in TC testing. Because a functioning device does not necessarily achieve steady-state temperature distribution, stresses in high temperature regions tend to be more acute because it is more localized [[32]-[34]].

Due to the fact that power cycling typically relies on actual device operation to induce failure, many feel that it is a more accurate method for predicting fatigue life than TC or TS. The justification for this position is, that PC better simulates the real-world temperature gradients a device will experience in actual applications given that the non-uniform temperature distribution found in PC in combination with the different CTE of each component will make the solder material deform differently than in TC testing. PC testing is also considered a less conservative test because the temperature conditions are often much more mild averaged across the device.

2.1.4 Challenges with Common Methods

Each of the traditional accelerated testing methods discussed above have unique advantages making them useful for evaluating solder interconnect fatigue life in certain applications. However, one must be mindful of each method's unique weaknesses and limitations. All three methods are unable to evaluate CTF at rates greater than 6 cycles per hour. In testing that is supposed to be "accelerated", these low cyclic rates lead to significantly long duration tests. Given that it is often expensive to conduct these tests, the total cost of running an experiment over a long period can be prohibitive. Thermal cycling tests in particular are generally quite long in duration with test times of up to 6 months in industry applications. Additionally, care must be taken when using these methods to ensure that the expected failure mechanisms occur according to what is expected or reported in actual applications. Thermal cycling tests have been shown to increase thermal gradients which subsequently cause changes in the diffusion pathways along which microstructural changes occur. These tests are suited to applications where sudden large temperature changes may occur uncommonly, however, their use is limited for evaluating fatigue life under standard operating conditions. TC and TS are generally designed to create harsher than expected conditions, often resulting in overly conservative estimations of device lifetime. These over estimations can lead to unnecessary additional design time and the inclusion of excessive redundancy which increases device complexity and cost. PC is seen by many as the most true-to-life AT method, despite this, its utility is still limited by the relatively low cyclic rate.

Another weakness shared by all three traditional AT methods is less often considered. In each of these methods, thermal, mechanical and chemical processes are all influencing the solder

simultaneously. While this is accurate for simulating actual application conditions, it is nearly impossible to quantify what percentage of the damage was due to only one fatigue factor, and which occurred only as a result of a combination of factors. Physical and metallurgical interactions intersect in thermal environments, stress and diffusion intermingle and it becomes difficult to assign damage to each individual fatigue factor. In the case of power cycling, current effects such as electromigration (EM) also influence solder fatigue. Thus, to develop an understanding of what each threat factor is doing to the solder interconnects, these phenomena must be isolated and studied independently. Once a strong understanding of each is achieved, the greater thermo-electro-mechanical system can be evaluated with new found clarity. To that end, many alternative approaches to damage assessment and fatigue life prediction have been developed to enable new insight into solder interconnect reliability.

2.2 Additional Testing Methods

2.2.1 Thermo-Mechanical

Thermo-mechanical methods seek to develop a better understanding of the relationship between temperature and stress by combining and quantifying thermally and mechanically induced stress in one accelerated test or comparing performance across thermal and mechanical tests. Tests of this nature are useful in determining the magnitude of loads which a device can survive prior to stress induced failure. These tests are often characterized by a multi-point data collection scheme whereby temperature, resistance and stress are all monitored in-situ. This enables real-time study of changes in material strength, electrical performance, and the effects of various temperature gradients such as temperature ramping. Quantifying the magnitude of all these factors within the device as it is induced to fail can help provide new insight into material properties, architectural weaknesses, and design for reliability (DFR) guidelines.

A common alternative approach is to combine a traditional AT, such as thermal cycling, and introduce mechanical load or shock to the device during or after thermal cycling [35]-[37]. Yu et. al. observed that the impact of compressive loads, such as those due to expansion interactions with adjacent components, on solder joint reliability was not thoroughly understood [37]. They designed and fabricated a fixture that applied compressive loads to the package which were then placed in a temperature cycling chamber and cycled from 0 °C to 100 °C with a ramp time of 30 min. and a 15 min. dwell at peak temperatures. Crack propagation through the die-side interfacial region was still identified as the dominant failure mode, being observed in 66.7 % of all samples tested. However, diagonal cracking through the bulk solder material was identified only in the preloaded solder joints. The additional failure mode observed only in the preloaded samples indicated that the crack propagation pathways had been changed as a result of the compressive stress [37].

Karppinen et. al. looked at the combined effects of mechanical shock and power cycling of the reliability of interconnects in handheld devices [38]. The effects of thermal aging as a result of PC were on mechanical shock survivability evaluated for devices ages 1000, 3000, and 5000 power cycles. A 0.5 ms half-sine shock was generated with an initial magnitude of 1440 G. Mechanical shock and PC were conducted both concurrently and consecutively for both board-level and product-level testing. The results showed that the thermomechanical loading enhanced the growth of the IMC layer and the coalescence of intermetallic particles inside the bulk solder. The aging effects of PC after 1000 cycles initially improved drop-test performance, but additional cycling led to degraded shock reliability. No significant difference in reliability was observed between the concurrent and consecutive testing method [38].

Other researchers have devoted their efforts to improving traditional AT's themselves by directly addressing their inherent weaknesses such as long duration and slow ramp rates [[39], [40]]. In an effort to reduce the time required to conduct TC experiments, Tunga and Sitaraman proposed using laser moiré interferometry to examine strain contours in a pre-cross-sectioned solder joint [40]. Plastic and ceramic BGA's were cycled from 0 °C to 100 °C with the interferometer mounted on a fixture above the test vehicle inside the temperature chamber. Using the Coffin-Manson predictive model and the deformations observed by the interferometer, strain estimates were calculated and used to assign a predicted reliable lifetime to each package. By reducing the solder material under study and mounting the interferometer in the temperature chamber, the total time to generate life time predictions was reduced [40]. Metasch et. al. designed a system to measure the in-plane and out-of-plane displacement of flip-chip solder interconnects under TC conditions in an effort to get more data out of the traditional method [41]. By integrating the test sample into a frame with force and displacement sensors, they were able to make new observations on the behavior of solder when cycled between two temperature ranges, 10 °C to 90 °C, and -40 °C to 125 °C respectively. Monitoring the point where the material was no longer able to resist 50 % of its initial peak force value, Metasch et. al., found that a 50 % reduction in temperature range leads to 6 times as many cycles before failure [41].

Another common form of thermo-mechanical accelerated testing utilizes elevated isothermal in-situ heating or ex-situ aging to introduce thermal effects into failure mechanisms under more controllable conditions [[42]-[45]]. The rationale of these tests is that the peak stress will occur when an actual device reaches peak operating temperature. Also, solder becomes more vulnerable to deformation and diffusion as homologous temperature increases. So, these tests are designed to simulate that "worst-case" situation of high temperature and mechanical stress.

Fakpan et. al., utilized resistive heating elements to reach a steady-state temperature of 70 °C mounted near a center cracked tension (CCT) sample to evaluate the response of SAC 305 and Sn-37Pb solders to shear stress at elevated temperatures. The results of their experiments showed that the time-dependent creep crack growth rate of SAC 305 was higher than that of the Sn-37Pb solder for both room and elevated temperatures [44]. Lee et. al., evaluated the combined effects of thermal aging through TC with mechanical shock to determine the effect of fatigue life for 1 % and 3 % silver content Sn-Ag-Cu solder materials [45]. A composite board containing nine test vehicles that enabled each location to experience a different shock level and strain level from an input shock of 1500 G with a 0.5 ms half-sine pulse duration. Some of the shock samples were aged isothermally at 150 °C for 500 hours. For comparison, thermal cycling was conducted on aged and unaged samples. They found that more grain boundaries arose from thermal cycling than shock deformation. This was attributed the strength of Sn at the higher strain rates which prevented the storage of as much energy in the microstructure as was stored under TC conditions [45].

2.2.2 Mechanical

While some mechanical testing methods are conducted with a thermal component, many other purely mechanical reliability tests have been developed. Mechanical testing has the advantage of being very fast compared to traditional methods like TC and the characteristics of failure are much easier to interpret because damage is based solely of physics based first-principles. This combination of rapid reliability assessment coupled with, in many cases, intuitive failure mechanisms, makes mechanical testing uniquely suited for early design validation through concept prototyping. The added advantage of this is that, design validation does not need to wait until near the end of product development to discover potential weaknesses

because inexpensive, mechanically congruent test vehicles can be easily produced. Several categories of mechanical reliability test exist including; shock, bending, vibration, lap shear, and cycling loading. These categories are discussed below.

i) Mechanical Shock

In consumer electronics, JEDEC JESD22-B111 is used as the standard for mechanical shock reliability [[46], [47]]. The standard stipulates that a board containing 15 test devices with a footprint of 132 mm x 77 mm must be subjected to a 1500 G, 0.5 ms pulse shock. Most mechanical shock testing setups utilize a drop-tower to accelerate the device to achieve the desired acceleration prior to impact. Mechanical shock tests are well suited to applications where the device may experience a sudden, high-G impact such as portable electronics and military applications. Lall et. al., evaluated the survivability of electronic missile components under extreme shock conditions of up to 50,000 g [48]. Fu et. al., used mechanical shock tests to compare standard Bi-Sn and resin reinforced Bi-Sn to determine if the resin could be used to overcome the inherent brittleness of Bi containing solder [49].

In their evaluation of aging effects on solder interconnect shock performance, T.-K. Lee et. al. conducted mechanical shock tests at 150 G, 200 G, 250 G, 300 G, and 340 G with isothermal aging profiles of 500 h at 75 °C, 100 °C and 150 °C [49]. Intermetallic growth behavior of both NSMD and SMD solder pads were studied for comparison. The greatest reduction in performance was seen in SMD samples that were aged for 500 H at 75 °C, with a decrease from 3 cycles-to-failure under 200 G shocks to 2 cycles-to-failure under 150 G shocks. For samples aged at 100 °C, the performance level increased to 6 CTF under 150 G loading, while samples aged at 150 °C showed the greatest improvement with 5 CTF under 250 G loadings. In the case of NSMD samples, little difference was seen in performance between aging

profiles and test conditions. Thus, SMD pads where more susceptible to performance changes due to isothermal aging. Crack initiation and propagation were found to occur mostly at the substrate side IMC interface where an unstable hexagonal Cu_6Sn_5 microstructure was found to form in the 75 °C aged samples. This unstable microstructure was unique to the 75 °C aging profile and acted as the week interface along which fast crack propagation occurred. Additional testing at elevated, steady-state temperature (100 °C) revealed improved CTF performance for SMD samples in low shock input (100 G and 150 G) regimes [49].

ii) Bending

Mechanical bending tests of electronic components in industry are governed by JEDEC standard JESD22B113. Mechanical bending tests are better suited for providing data on relative component performance rather than a discrete pass/fail criterion [50]. Vandevelde et. al., induced mechanical stress into the components by applying four-point bending to the PCB. This bending causes absolute displacement of the top/bottom fiber of the PCB which simulates the expansion mismatch seen between the die and substrate of the device that is observed in TC testing [51]. The dominant failure mode was found to be cracking along the interfacial region of solder joint on the die-side. Experiments were conducted to determine if alternate failure modes would occur at higher loading frequencies but the researchers concluded that bending dwell times of 10 minutes were sufficient.

Given the fact that most solder interconnects fail at the interfacial region between the IMC layer and the bulk solder, Philippi et. al. utilized mechanical bending tests to evaluate the strength of Cu_3Sn alloy (a common IMC phase) microcantilevers shaped by focused ion beam milling (FIB) to common IMC layer thickness [52]. This was undertaken in an effort of estimate the critical defect size for Cu_3Sn in based on fracture toughness in bending. The researchers

concluded that critical defect size corresponded to grain size, finding a critical defect size of 258 nm for their samples [52].

iii) Vibration

Vibration testing is conducted to evaluate the effects vibration, such as that arising from transportation or operation, has on electronic devices. Vibration can induce stress in solder interconnects and repeated exposure or long duration can lead to fatigue failure. Studies can be conducted to evaluate the device under conditions similar to the end use conditions to evaluate long-term reliability of components in high vibration applications, such as automotive or portable electronics. To perform this test, the components under study are rigidly mounted or restrained by a case with suitable protection for the leads. The case itself is then rigidly fixed to the vibration platform with the leads secured to prevent excessive lead resonance [53]. Vibration is applied (typically with a shaker table) so as to simulate non-shipment vibration conditions to evaluate solder reliability. Standards such as JESD22-B103B.01 [53] dictate standard test conditions for peak-to-peak displacement, peak acceleration (G), cross-over frequency (Hz), and min/max frequencies (Hz). Typically, a complete sweep of frequency range from minimum to maximum and back is conducted in a logarithmic fashion in a period of 4 minutes. JEDEC stipulates a sweep rate of 1 decade/minute with 4 consecutive sweeps in each orientation X, Y, and Z for a total of 12.

Random vibration tests are conducted to evaluate the survivability of electronic devices during shipment. Devices are excited with a Gaussian random vibration which is applied for 30 minutes in each orthogonal axis for a total test duration of 90 minutes [53]. Vibration test parameters should be calibrated against the natural frequencies of the component. Accelerometers can be used to measure the natural frequencies and mode shapes of the test

vehicle under the boundary conditions of the test [54]. Typically, the first natural frequencies (1 for each orthogonal axis studied) are used because those frequencies are known to accelerate damage the most [55]. Failure is again often assigned if the test unit ceases to function, resistance spikes, or various visual inspections reveal significant damage. Batieha et. al., cautioned that random vibration test results could be particularly difficult to relate to long term performance [56]. Accelerated vibration testing is known to lead to continuous resonance frequency shifts caused by softening of the PCB, especially at higher amplitudes. Researchers observed a continuous drop in resonant frequency when testing at a 6 G amplitude however at 3 G amplitude, there was no significant change. Batieha et. al., concluded that tests should be limited to amplitude levels at which resonant frequency shifts remain negligible for the duration of the test [56].

Discerning the most common failure mode in solder interconnects under vibrational excitation can be more complicated than traditional thermal-based methods. Typically, fatigue cracking with in the interfacial regions are still the most common [[54]-[56]]. Solder pad cratering has been reported after even moderate cyclic vibration testing, also, intermetallic and bulk solder fatigue comingle. Additionally, brittle fracture was seen to vary more quickly with increasing load amplitude than did ductile fatigue. Due to this behavior, low amplitude testing can be conducted without significant PCB softening but softening occurs at high amplitudes [56]. Zhou et. al., recommended the use of constant amplitude harmonic excitation because the dynamic response of the test vehicle consists of only one mode rather multiple coupled modes [54]. Mode coupling can confuse assignment of failure mechanism to stress resulting from a specific mode shape. Additionally the strain history is harmonic, eliminating the need for cycle counting algorithms and damage accumulation will be constant. Using vibration testing, Chuang

et. al., were able to recommend the use of hypoeutectic alloys in solder applications expecting frequent vibration. Hypoeutectic Sn-Zn alloys did not enhance crack propagation rate unlike near-eutectic and hypereutectic Sn-Zn alloys when exposed to resonant frequencies in the 70 Hz range [57].

iv) Lap Shear

Shearing tests are generally conducted to evaluate the mechanical force or number or cycles at a specific shear magnitude required to destroy the capacity of the interconnect to function electrically. Often, the goal is to simulate the CTE mismatch induced mechanical stresses observed in typical thermal cycles during actual operation. Many types of shear tests are commonly used in industry such as ball impact test (BIT), high speed ball shear test (HSBS), and high speed cold ball pull test (HSCBP) [[58]-[61]]. In the test, individual solder balls receive a high speed mechanical loading which is often applied or even ramped up until the ball separates from the substrate. However, the solder balls in these tests are only joined on one side of the interconnect making the accuracy of predictions made about real applications where a solder column is fused to IMC at each end, suspect [61]. In lap-shear testing, a volume of solder is joined to PCB or other substrates at the top and bottom of the interconnect. These substrates are then pulled apart to generate shear stress within the solder while the shear force is measured with a load cell. The deflection of the solder column can be measured ex-situ by measuring the change in length of the assembly or in-situ using digital image correlation (DIC). Shear stress and shear strain are calculated using force, and deflection data respectively.

Lap-shear tests are very useful for making determinations about process quality and material properties such as solder creep strain response and ultimate shear strength [[61]-[63]]. Choudhury and Ledani evaluated the stress-strain response of Sn-3.5Ag solder which contained a

high fraction of Sn-3.5/Cu intermetallic compounds, finding that strain-to-failure was greatly affected by the presence of IMC's within the interconnect [62]. They reported that IMC volume fractions in the 40 % to 60 % range resulted in a large increase in shear strength (nearly 67 % in the case of 60 % IMC). Additionally, an IMC fraction of 80% was observed to result in a decrease in shear strength compared to 60 % IMC but was still stronger than a 40 % IMC volume fraction [62]. In their study of creep behavior in innolot solder alloy, Tao et. al. confirmed that temperature and applied shear stress greatly affect the material behavior of the solder alloy when conducting lap-shear tests at 25 °C, 75 °C, and 125 °C [63]. Higher creep rates were seen in conditions of high temperature and high applied stress.

Lap-shear tests' utility in assessing reliability and failure in actual applications are limited due to their dependence on using comparatively large volumes of bulk solder in non-practical solder arrangements. Additionally, most lap-shear tests do not account for the cyclic nature of shear stress as seen in device operation. Without the ability to test actual devices across a range of stress magnitudes consistent with those seen in applications due to temperature fluctuation during power cycling, lap-shear tests are ill-suited for providing design optimization guidance or rapid architecture reliability assessment in real world applications.

v) Innovative Alternative Techniques

Many additional test methodologies have been devised, with more being developed all the time. These methods seek to achieve more consistent, more accurate, or more rapid solder fatigue results than can be achieved with the traditional methods or other alternative test. Additionally, some of these methods are designed as tools to assist in the breakdown of the solder fatigue system into more easily studied component failure mechanisms. One novel solder fatigue test was developed by J. F. Liu et. al., where small solder samples can be tested using

impact of tensile/compressive loading to determine the effects of mechanical loading on reliability [64]. Observing that standard impact tests can result in varying velocities of the impact plate, Liu et. al. concluded that direct impact is not the best method for testing small solder joints which undergo brittle fracture under tension [64]. To address this, a miniature impact test instrument was designed where the specimen is attached between input and output bars, and impact is administered using a hollow striker which impinges on the back face of the strike plate. Long, thin bars are used to accommodate small samples, and allow for moderate strain rates because a sustained loading pulse is required [64]. Upon impact of the striker, the impact plate achieves a common velocity which generates a tensile pulse in the input bar. As compression commences, a velocity at the impact plate-specimen interface generates a compressive pulse. The recorded input wave is thus the superposition of the two pulses and is measured using strain gauges [64].

Dynamic compressive tests were conducted on small cylindrical 4043 Al specimens for comparison with a traditional Hopkinson bar system, and the results of the miniature impact tester correlated well with the results using the traditional system [64]. In addition to single impact testing, this test apparatus is capable of conducting pure shear testing of devices with the installation of specially designed adaptors. Adaptors were also created to test solder interconnects at loading angles of 0°, 15°, 30°, 45°, 60°, 75°, and 90°. The adaptors can be threaded to the input and output bars and the solder joint specimens are bonded to the adapters using cyanoacrylate adhesive [64].

In an effort to address the need for lap-shear testing machines which were more reasonably scaled to actual solder interconnects, Tao et. al., designed a miniature lap-shear testing unit with a load capacity suited to small samples (such as CSP) with a maximum tensile

force of 2.0 kN and a wide range of cross-head speeds (39 nm/s minimum) [65]. The machine has the capability to conduct tensile and compressive lap-shear tests, as well as, a cyclic loading ability. The sample is attached at one end to a bar which is fixed, and at the other to a motorized bar which provides the stroke that induces stress in the material. The stress is measured by a load cell attached to the fixed end and the shear stress is calculated. Evaluating lap joints of Innolot and SACBiNi solder alloys at different strain rates and temperatures using this setup, Tao et. al., observed decreases in ultimate shear strength (USS) for both alloys. At room temperature with a strain rate of 2.0×10^{-2} s^{-1}, USS values of 58.9 MPa and 61.1 Mpa were reported for SACBiNi and Innolot respectively, while at 125 °C with a strain rate of 2.0×10^{-4} s^{-1}, USS was decreased to 26.6 MPa and 29.5 MPa for SACBiNi and Innolot repectively [65]. Examining the microstructure of these joints, rupture was seen to start in the bulk solder material and propagated towards the interface with the thinnest IMC layer. Some vacancies were observed locally at the interface between IMC layers and the solder joint [65]. Higher quantities of Ni and Sb were seen to reduce strength and improve elongation to rupture.

Ohguchi et. al., utilized stepped ramp wave cyclic mechanical loading to evaluate the low-cycle fatigue life of SAC305 and Sn-37Pb solders [67]. Using stepped ramp waves (SW), the researchers were able to quantify creep strain in tensile and cyclic tensile-compressive loading without conducting creep tests. Fatigue tests were conducted using cyclic tension-compression loadings with different periods for a total strain amplitude of ±5 % at ambient temperature [67]. For comparison with other fatigue tests, triangular wave (TW) loading was also used. The SW tests were used to obtain stress-strain relations that were then used to evaluate the creep strains generated during the TW tests. Cylindrical ingots of SAC305 (gauge length 18 mm, gauge diameter 8mm) were subjected to a two-step fatigue process. First, TW loading was

used to determine the effect of period on fatigue life of the test units under tension-compression cycling. The tested units were then subjected to SW loading to identify creep deformation strain generated during the TW tests [67].

Four test conditions were selected to evaluate effects of time-in-tension and time-in-compression on the stress amplitude and the symmetry between stress-strain response in compression versus in tension [67]. Condition 1 stipulated a time-in-tension of 2 seconds with a time-in-compression of 20 seconds; for condition 2, these values were reversed. Conditions 3 and 4 alternated times of 2 seconds and 200 seconds between tension and compression. The results showed that larger differences in period result in larger differences in maximum absolute stress. Conditions 2 and 4 were seen to have higher stress on the compressive side while conditions 1 and 3 had higher stress on the tensile side. Conditions 3 and 4 were found to exhibit hysteresis loops that had a high degree of asymmetry [67]. Ohguchi et. al., concluded that creep strain accumulated on the side in tension greatly affects fatigue life in solder materials. These tests were performed in a manner quite useful for materials characterization studies, however, the test samples utilized did not adequately represent solder interconnects commonly found in device applications. If the method could be adapted to work with full-scale electronic devices, it may prove a useful method for predicting creep strain response of solder joints.

2.3 Summary of Techniques

Table 2-1 shows a comparison of all the accelerated testing methods outlined above. Of the methods presented here, power cycling is seen by many as the most true-to-life method for generating failure modes consistent with actual operating cycles. This makes PC an attractive option for predicting operating fatigue lifetime. However, PC is still slower than mechanical testing methods. Temperature cycling and thermal shock tests are uniquely susceptible to

diffusion due to the high thermal gradients involved in reaching test temperatures. Additionally, for all three testing methods, understanding the causes behind failure mode characteristics is made difficult because thermal, chemical, mechanical (and in PC electrical) threat variables are involved in interconnect fatigue simultaneously. The lack of this key understanding often results in test parameters which are intentionally pessimistic, creating harsher conditions than those seen in actual operation, leading to overly-conservative lifetime estimates. Thermo-mechanical methods are typically faster due to the use of combined mechanical and thermal stress inducement, leading to higher total stresses. These methods are perhaps the most useful for studying the effects of combined thermal and mechanical threat variables on fatigue lifetime. However, this approach can only produce accurate predictions if the specific mechanical and thermal conditions and how they will interact are known prior to testing so that proper test parameters can be selected. Due to the increased stress state of the system, coupled with mixing stress sources can result in unusual or false failure modes rarely (if ever) seen in actual working devices. Like TC, TS and PC, these methods often report "worst-case", overly-conservative lifetime estimations.

Table 2-1

Comparison of Accelerated Testing Methods

Method	Mech. Stress Inducer	Test Duration	Cyclic	Device Relevant Samples	Design Guidance	Lifetime Prediction Type
Temp. Cycling	CTE Mismatch	Slow	✓	✓	✓	General Fatigue
Therm. Shock	CTE Mismatch	Moderate		✓	✓	General Fatigue
Pwr. Cycling	CTE Mismatch	Slow	✓	✓	✓	General Fatigue
Mech. Shock	Shock/Impact	Rapid		✓	✓	Shock Fatigue
Bending	Shear/Tension/Compression	Moderate				General and/or Bending*
Vibration	Shear/Tension/Compression	Moderate		✓	✓	Vibration Fatigue
Lap Shear	Shear	Moderate				
Mech. Cycling	Shear	Rapid	✓	✓	✓	General Fatigue

** Bending tests can be used to examine bending fatigue lifetime specifically, or to simulate stresses induced by CTE mismatch for comparison with TC or PC methods.*

Mechanical testing methods generally have the benefit of shorter test duration which can significantly lower costs and product lead times. In the case of mechanical tests like mechanical shock, vibration, and bending, often the fatigue lifetime predictions are specific to a unique type of stress rather than the more general types of stress found due to CTE mismatch, Mechanical shock is an excellent way to evaluate the ability of a device to survive repeated large impact events. However, using MS to make predictions on general fatigue lifetime of a device due to CTE mismatch when under real-world power cycling or to compare predictions with TC for example is problematic. Impact testing generally creates unique failure modes that are not represented in CTE mismatch failures. Making CTE mismatch fatigue predictions using bending tests can give good results for general fatigue lifetime or for the more specific bending fatigue lifetime depending upon the parameters and intentions of the test. Bending has been used to simulate the stress conditions found in devices under PC and TC conditions to induce the same types of failure mechanisms. When conducted this way, the resulting fatigue life predictions can be considered as more accurate that making the same prediction using MS or vibration. Moreover, if a device is expected to the subjected to bending frequently during its lifetime, bending tests are critical to gaining insight into the overall reliability of the device by considering the impact of the bending itself, but this is less important for non-dynamic situations where bending in not the most prominent stress inducing phenomenon. Similarly, vibration tests are critical if a device is expected to endure vibration often during its useful lifetime but these tests do not create the conditions necessary to produce shear magnitudes and direction consistent with CTE mismatch, unlike mechanical cycling and temperature cycling methods.

Lap shear methods are perhaps the most useful methods for evaluating solder material properties and the effects of the solder processing procedure on interconnect microstructure

because all the damage is due to stresses which are easily understood using physics first principles. This makes damage assessment and responsibility assignment much easier, especially when coupled with the simplistic structure of most lap shear test specimens. Unfortunately, these methods are typically incapable of testing full-scale electronic devices, making them of limited value for generating fatigue lifetime predictions and certainly inferior to mechanical cycling methods where the microstructural changes, as well as actual device lifetime, can both be monitored in situ. The method developed by Liu et. al. is perhaps the most versatile approach discussed given the extensive versatility in testing configurations for generating different types of stress (including shear, tension/compression, and impact) but can only be used on a single small solder interconnect. The stepped ramp-wave approach is particularly useful in examining creep behavior within solder interconnects to determine its effect on fatigue life. It is also capable of providing some guidance as to design considerations, with [67] determining that creep strain accumulated on the side in tension had the greatest impact on lifetime, indicating that special care must be taken in designing the tension-side architecture.

The method discussed throughout the rest of this work was developed to address the weaknesses and limitations of the above reliability evaluation methods. The mechanical cycling method presented in this paper was designed to mimic the cyclic behavior of stresses induced in normal operational power cycling, with the aim of improving accuracy over single cycle tests like lap shear. Additionally, by cycling at high frequency (60 cycles/minute), test duration is significantly reduced enabling a reduction is associated costs. Another goal of this time saving strategy was to create a testing system that could be used to evaluate very early stage device designs to provide reliability analysis of prototypes to enhance the design decision-making process. Designed to test fully functional chip-scale devices and mechanically analogous dummy

chips, the method was designed with device specific adaptation capabilities in mind. The following section presents a paper published in the IEEE *Transactions on Device and Materials Reliability* [68], which details the methodology behind the testing procedure.

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Appendix: IEEE Reprint Authorization

The following article was originally published in the IEEE *Transactions on Materials and Device Reliability, vol. 18. **no. 3**, p. 412-421, 2018. It is included in lieu of a methodology section as that was what the article was written to convey. The method described therein was used to collect the data and perform the calculations discussed in later sections.*

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3. Rapid Solder Interconnect Fatigue Life Test Methodology for Predicting Thermomechanical Reliability

Cody J. Marbut, Mahsa Montazeri, and Dr. David R. Huitink

3.1. Abstract

A rapid reliability test methodology was devised for simulating mechanical stresses induced from thermal expansion induced shear in temperature cycling of flip-chip devices in order to de-convolute shear stress from thermal effects in typical environmental tests. Using controlled force application according to spring deflection, a test stand was created to mechanically apply shear stress to solder interconnects in flip chip devices at isothermal conditions. The shear stress was applied cyclically using a tribometer to simulate the mechanical stresses induced in the interconnects of a device during a thermal cycle while in operation or accelerated testing. In the mechanical application of shear, the control of loading and cyclic rate can be precisely controlled while monitoring key factors for observing crack propagation and damage. In doing so, this novel approach introduces the ability to directly correlate shear stress and plastic work accumulation (damage) to fatigue life in a generic device, utilizing help from finite element models alongside data acquisition. Using the obtained correlations, lifetime predictions through early stage design analysis are possible, paving the way for a-priori optimized design for thermomechanical reliability in flip-chip devices. The methodology presented herein creates the opportunity to eliminate costly lifetime testing on multiple electronic device designs/configurations, while also expediting any data collection needed for new materials or process related impacts to reliability.

3.2. Introduction

Reliability of electronic devices finds increasing importance with the electrification of transit, in addition to everyday tools, and entertainment devices. During normal operation, these devices regularly experience temperature cycling between ambient and operating temperatures. These thermal cycles induce stresses due to thermal expansion which may lead to failures such as interfacial cracking, void formation, reduced electrical performance, and delamination. Crack formation/propagation in interconnects is one of the leading causes of failures in Ball-Grid-Array (BGA) devices, particularly in high temperature applications [1]. Mechanical shear stresses caused by mismatched thermal expansion primarily cause this cracking and void formation among assembly materials such as solder interconnects. While selecting materials with similar coefficients of thermal expansion (CTE's) can improve reliability of a device be reducing these stresses, the increasing complexity of electronic packages, higher temperature operation of SiC and GaN-based power devices and their associated cost considerations necessitate certain materials and processes where stresses are unavoidable, such that methodologies for managing reliability are required.

3.2.1 Accelerated Environmental Testing

Most commonly, accelerated environmental testing methods are used to evaluate reliability of electronic devices and systems in order to demonstrate sufficient lifetime operation, or to down-select possible material or process candidates for a given device design. These environmental stress tests are aimed at evaluating time to failure (TTF), which can be extrapolated to device operating conditions using reliability acceleration models. Common thermomechanical packaging tests include temperature cycling (TC) (JESD22-A104 and IPC9701), thermal shock (TS) (JESD22-B106), and power cycling (PC) (JESD22-B105) [2-13].

Each of these methods offers some benefits and drawbacks, as illustrated in Table 3-1, but care must be taken that the failures induced are relevant to the actual operating environment of the evaluated electronic system

In thermomechanical testing, solder interconnect fatigue, cracking, delamination, ball bond integrity failure, and creep are common among flip-chip devices [3,4]. Fatigue cracking is most commonly found in the interfacial regions between the bulk solder and the intermetallic layer. These fatigue cracks propagate based upon the micro-structure and mechanical properties of the bulk solder [5]. Recrystallization of Sn is induced by thermal strain and elevated temperature starting in the highly strained regions before expanding through the bulk material [3]. Recrystallization has been shown to enhance fatigue cracking due to a network of high-angle grain boundaries which extend through the interconnections and provide favorable propagation paths [3,4]. Researchers have found that the stress/strain distribution within the bulk material undergoing a thermal fatigue process is not uniform. This non-uniformity leads to grain slipping and plastic work accumulation with cycling [3,4]. Thus, it can be said that the damage found in solder interconnections under thermal strain results from dislocation densities in the plasticized regions increasing with the accumulation of internal energy [3-6].

Table 3-1

COMPARISON OF COMMON RELIABILITY TESTING METHODS

	Thermal Shock	Thermal Cycling	Power Cycling
Ramp Rate (°C/min)	15+	10 - 15	3.8 - 11.5
Cycles/hr	1.8 - 6	1 - 3	2 - 6
Prim. stress source	CTE mismatch*	CTE mismatch	CTE mismatch
Thermal gradient risk	High	Moderate	Moderate

* Additional stresses due the thermal gradients can impact fatigue behavior and even alter observed failure mechanisms. Collated from sources [1-5, 8-10].

J.W.C. de Vries, et. al., found that this inelastic strain was caused primarily by increases in creep strain [7]. When comparing TC and TS results, they concluded that the TC tests exhibited no plastic strain while in TS testing, the inelastic strain accounted for 1.5% of the total plastic strain [7]. The primary source of stresses in TC testing is CTE mismatch between component materials. Additional stresses can be created by thermal gradients when testing the same system under TS conditions. The magnitude of these additional stresses in TS depends upon the thermal behavior of the device under study. Thus, for the same tested device, the MTTF could be significantly different for each test method. The principle failure modes may even differ between the two methods [7]. Even so, comparative analysis of power cycling and thermal shock tests has shown that the primary cause of failure was generally the same. Crack nucleation and propagation assisted by recrystallization resulting from energy provided by the mechanical stresses generated during cycling was identified as the primary failure mode for both tests [9], yet under power cycling conditions, IMC growth was accelerated along with recrystallization. Researchers linked this to electromigration of Sn and Cu in the solder matrix, resulting in higher

Sn flux and increased Cu_6Sn_5 growth at the anode side of the interconnect in addition to the higher average temperatures, localized heating, and current flow related to PC testing [9].

3.2.2 Acceleration Models for Life Prediction

Acceleration models intended to translate low-cycle fatigue damage induced during accelerated testing into estimates of actual lifetimes are often used when attempting to qualify electronics and prove robustness [1, 3-4]. Traditional models like Coffin-Manson power relationships often attempt to relate temperature ranges to lifetimes, however, become problematic when translating across differing designs which may have vastly different strain energies or plastic work density in failure risk materials. Notably, strain rate and energy cannot be directly accounted for in an extrinsic property like temperature delta, and so these models often vastly under predict lifetimes. The Norris-Landzberg model (or "modified Coffin-Manson") builds onto Coffin-Manson by compensating for anomalies of time-dependent and kinetic effects [4], yet it has been shown that the exponents in this equation are not consistent among package type, material, and geometries [4,10].

The net effect of these inconsistencies shows a need for the development of better mechanistic models that can more accurately describe failure acceleration and risk through applying a physics of failure approach. Some have offered FEA-based approaches to evaluating failure risk, such as Darveaux [11] and Engelmaier [12], however, these have issues with requiring extensive test validation in thermal cycling, which may not be adequately represented in FEA approaches which use simplifying assumptions about isothermal components and associated boundary conditions. As a result, an understanding of the effects of these stresses on interconnects, independent of the thermal aspects of the thermomechanical system, is required to best inform design to optimize device reliability. To achieve this, the physics of failure within a

given package must first be understood, particularly within the context of accelerated reliability testing. One of the major challenges with conventional accelerated testing methods is their dependence on temperature. In a thermal environment, there exist both physical and metallurgical interactions which impact fatigue life. Stress and diffusion are intermingled, and it becomes difficult to quantify what damage is due to which threat factor. Through removing the thermal factor and relying solely on mechanical stress, the chemical aspects of the threat environment are removed. This de-convolution of shear stress from temperature allows rigorous study of the physics-based material response to stress. Once a strong understanding of the stress response is achieved, the thermal impact on fatigue can then be reexamined with a strong foundation for determining what failure characteristics are unique to the thermal environment.

Additionally, the ability to expediently demonstrate reliability based on physical principles alone, which can then be extracted for incorporation into design analyses, as opposed to the typical design-specific reliability validation near the end of product development, is essential for rapid time-to-market with design for reliability as a priority. Moreover, wide bandgap power devices incur significant cost for reliability validation, so developing methods that are centered on the specific risk (such as solder fatigue) is important in reducing the development costs associated with qualification activities, especially where high temperature operation applies. In this work, a mechanistic approach is presented wherein high rate mechanical cycling data can be used for identifying physics of failure and translating into the thermomechanical reliability expectations for any given design.

3.3. Materials and Methods

The goal of this testing method is to replicate thermomechanically induced cyclic stresses through direct shear force application to a given flip-chip die as per Figure 3-1, and relate back to

thermally induced stresses in flip-chip assemblies. In this work, we have adapted a tribometer to interface directly with electronic test vehicles for applying a reciprocating load via spring forces. The tribometer operating in linear mode can be used to deflect the spring a fixed amount while measuring the resultant spring force applied to the device. Correspondingly, the average shear stress (τ) can be calculated using the relationship between the applied force and cross-sectional area of the solder interconnects supporting the die, and then related back to time to failure and any plastic strain created by the applied force.

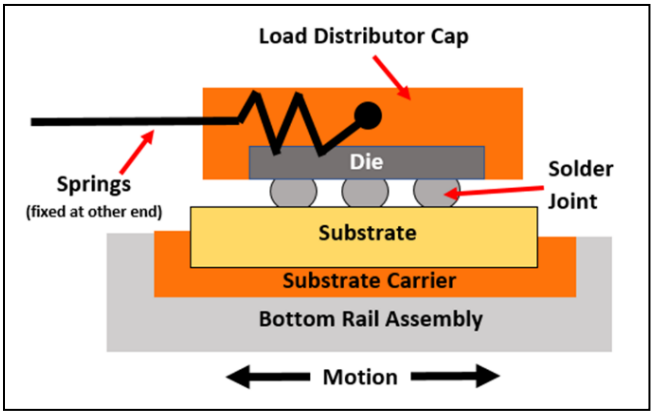

Figure 3-1: Loading condition for cyclic reliability tests.

In this demonstration, a test chip built to mechanically replicate a SiC MOSFET [13] made out of Si on a FR4 substrate is utilized for illustrating the methodology. The 3 mm x 4.4 mm test chip has thirteen 0.381 mm (15 mil) interconnects with 0.305 mm (12 mil) solder resist openings.

An adapter to facilitate this testing method had to meet several criteria. It needed to be capable of interfacing with the tribometer, the springs and the test chip such that only the solder interconnects of the test chip would oppose the motion. Additionally, the adapter was designed with the goal of being able to support multiple test chip designs. With these limitations in mind,

the final adapter concept was designed to be configured around chips of many different dimensions, by utilizing 3D printed device jigs for gripping the substrate and die, respectively.

The applied load is calibrated by using a 3D printed cartridge that takes the place of the substrate carrier (Figure 3-1). This cartridge has a raised rectangular prism located on the top center surface which has the same dimensions as the die. The load distributor cap interfaces the same way and the calibration test is carried out according to the same procedure. The magnitude of the load is then set to the proper value by changing the displacement setting on the tribometer. This requires multiple calibration runs until the desired load is achieved. The advantage of the dummy cartridge is that there virtually no deflection of the rigid ABS polymer component during the first several cycles. This means that the load reported for the first cycle with the dummy cartridge will be the peak reported for the first few cycles on a real device. Use of the 3D printed cartridge also ensures that there are no extraneous or unrecorded cycles on a test sample due to calibration before a test. The force values recorded for the calibration cycles are used to calculate the spring constant of the system by dividing each of them by the set stage displacement and taking an average. Once the proper load is set, the dummy cartridge is removed and the substrate carrier holding a device is inserted into the rail assembly. The same approach can be used at the end of a test to ensure that the stage displacement and spring constant remained the same throughout the test.

Using the data collected with the tribometer, characteristics of stress, deformation, and plastic work can be determined. Assuming the springs are not being plastically deformed (verified to be true) by the cyclic extensions and the displacement of the tribometer stage is set at a fixed value, such that any change in peak force values over cycling must be associated with the deflection of the test coupon and specifically the interconnects. An example plot of such data is

shown in Figure 3-2, showing the force vs cycle count for the test chip. Using the first cycle as a baseline (assuming no plastic deformation of the interconnects) the spring constant (k) for the system can be calculated with force and deflection given by the tribometer. This assumption is valid if the peak load reported for the first cycle matches that reported for the calibration cycle.

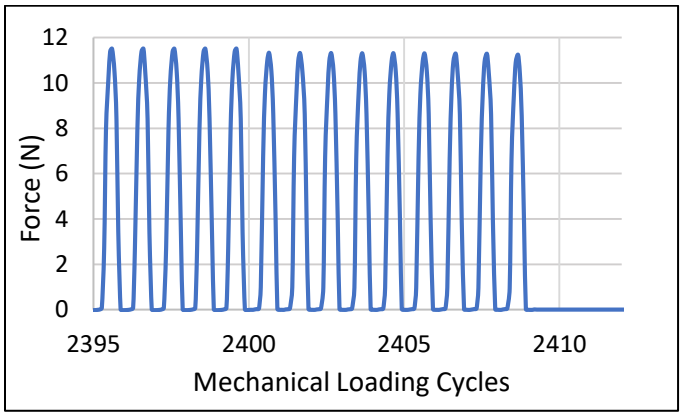

Figure 3-2: Representative plot for loading cycles for Sn63/Pb37 solder joints. Separation during 2409th cycle.

With the spring constant known, the relative deflection of the chip to the substrate can be calculated for each subsequent cycle. The deflection of each cycle at peak load (d_i) is seen to decrease proportionally with reported force values. By using the difference between the peak spring deflection of two adjacent cycles (i and i-1), effective deflection (δ) of the interconnects with respect to the substrate resulting from the i^{th} - 1 cycle can be calculated.

$$\delta = (d_{i-1} - d_i) \tag{3.1}$$

This requires the assumption that any deformation that caused reduced spring deflection was the result of work done during the previous cycle be valid. This value can then be used to calculate the plastic work (W_n) done during the i^{th} - 1 cycle. The force value of the previous cycle (F_{i-1}) is used due to two simplifying assumptions. One, all plastic deformation occurs at the time of peak force. Two, it is this deformation at the time of the previous peak force (F_{n-1}) which caused the

effective deflection of the ith cycle to be smaller than that of the ith - 1 cycle. Thus, the effective plastic work can be calculated.

$$For\ n = 0, W_n = 0$$

$$W_n = F_{n-1} * \delta, where\ n \geq 1 \tag{3.2}$$

From this equation, the total accumulated plastic work (W_T) can be calculated by summation of the values for W_n.

$$W_T = \sum_{1}^{n} W_i$$

Through these relationships, this testing methodology can quantify elastic and plastic deformation, peak and instantaneous average shear stresses, work, and cycles to failure (CTF). It is also possible to make several qualitative observations from the data. The ductile or brittle nature of the failure can be seen from visual inspection in addition to inference from analysis of the cyclic force data. The failure modes can also be characterized using microscopy to identify points of interest such as crack striations, pad failures, and the presence of solder necking.

Darveaux's model is used to calculate the steady state creep strain rate and the inelastic shear strain [14]. According to this model, the steady state creep strain rate of solder can be expressed as

$$\frac{d\gamma_s}{dt} = C_{ss}[\sinh(\alpha\tau)]^n exp\left(\frac{-Q_a}{kT}\right) \tag{3.3}$$

Where $\frac{d\gamma_s}{dt}$ is the steady state strain rate, k is Boltzmann's constant, τ is the peak applied shear stress, T is the absolute temperature, Q_a is the activation energy, n is a stress exponent, α is the constant that prescribes the breakdown of the power law dependence and C_{ss} is a constant [14].

The inelastic shear strain (γ_{in}) (see equation 3.6) is the sum of the creep strain (γ_c) and the time-independent plastic strain (γ_p) which are calculated using equations 3.4 and 3.5 respectively.

$$\gamma_c = \frac{d\gamma_s}{dt}\, t + \varepsilon_T \left[1 - \exp\left(-B\frac{d\gamma_s}{dt}t\right)\right] \tag{3.4}$$

In this equation, ε_T is the transient creep strain, and B is the transient creep coefficient, time (t) is in units of cycles for the calculations performed here.

$$\gamma_p = C_p \left(\frac{\tau}{G}\right)^{m_p} \tag{3.5}$$

where C_p and m_p are constants and G is the shear modulus. The total inelastic shear strain (γ_{in}) (see equation 6) is the sum of the creep and plastic strain. The constants used in the Darveaux calculations are found in Table 3-2.

$$\gamma_{in} = \gamma_c + \gamma_p \tag{3.6}$$

The thermal fatigue life (N_f) of a device can be estimated from isothermal failure data by using average inelastic strain energy density (ΔW) to model the creep response.

$$N_f = \varphi \Delta W^{\Phi} \tag{3.7}$$

In this equation, ϕ (always positive) and Φ (always negative) are constants for solder interconnects [15]. These constants can be found by creating a log-log plot of isothermal CTF and strain energy density. Strain energy density is calculated from the difference in peak shear for adjacent cycles and then averaged. This is because any decrease in shear is due to a decrease in force resulting from chip deflection. By using the change in shear between two peaks, only the strain energy used to cause the chip deflection is captured in the equation.

$$\Delta W = \sum_{i=1}^{n} \frac{(\tau_{i-1}^2 - \tau_i^2)}{2G} \tag{3.8}$$

Here G is the shear modulus and τ_i is the peak shear stress of each cycle before failure. The shear modulus is given by,

$$G = \frac{E}{2(1+\nu)}, \tag{3.9}$$

where E is Young's modulus and ν is Poisson's ratio as seen in Table 3-2.

Any reduction in shear is due to a reduction in shear force caused by decreased spring deflection resulting from chip deformation (the chip has been displaced toward to the neutral point by the spring). This plastic deformation was due to the inelastic strain generated in the solder material. Thus, the inelastic strain energy of that deformation is captured in the strain energy density equation. The strain energy density is related to plastic work through that inelastic strain. The plastic work is calculated from effective chip deflection between cycles and is the energy required to do the work of deformation due to material response to the induced strain. Therefore, plastic work is the inelastic strain energy. The calculations were conducted using the whole solder volume because all the joints were classified as effective through SEM inspection, meaning that there were complete bonds between pad-paste, paste-ball, ball-paste, and paste-pad as one goes up the interconnect from substrate pad to die pad. This classification was granted if there was significant cracking or necking visible on both sides, or in many cases, the solder ball was still solidly attached to one side (usually the die with ductile necking) and significant cracking occurred on the substrate side. When this was observed, the entire joint was said to have opposed the force and was treated as a load-bearing column.

TABLE 3-2

PROPERTIES of Sn63/Pb37 SOLDER (@ 25 ℃) [11]

C_{ss}	8.03E+04
α (1/kPa)	6.70E-05
n	3.3
Qa (eV)	0.7
ε_T	0.023
B	263
C_p	3.35E+11
m_p	5.53
k (eV/K)	8.62E-05
Poisson's Ratio	0.35
Young's Modulus (Pa)	7.59E+10
Shear Modulus (Pa)	2.81E+10

3.4. Experimental Methods

The test method was demonstrated to produce solder interconnect fatigue failures through cycling mechanical shear loading. Peak stress per cycle for 4 sample devices can be seen in Figure 3-3. The ductility of the material before and during the failure can be seen from the slope of the graphs. Tests 1 and 2 showed a more ductile fatigue behavior than test 3 and 4. The point of failure can be seen by the sudden large drop in peak force. In these tests, the device was fatigued to complete separation.

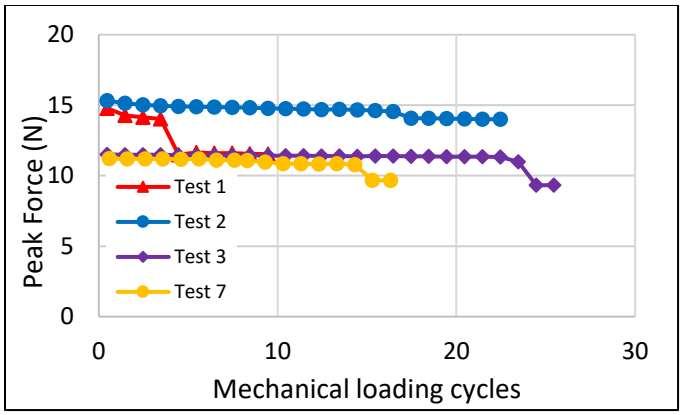

Figure 3-3: Peak force vs cycles for 4 identical test devices.

Analysis of the work-averaged effective stress compared with cycle-life agreed with predictions. Lower values of effective stress correlated to longer cycle life as seen in Figure 3-4.

Visual inspection of the tested samples showed crack striations and necking behavior. Additionally, pad adhesion failures were a common occurrence. Figure 3-5 shows two die-side solder bumps after cycling. Crack striations are clearly visible on the bulk material. The arrow indicates the direction of crack propagation.

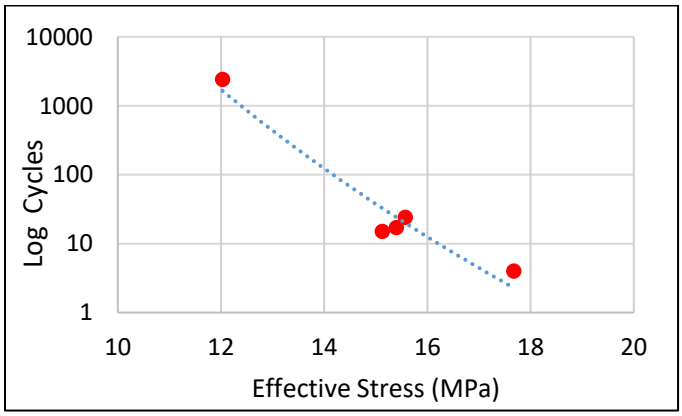

Figure 3-4: Log plot of cycles to failure vs work-averaged effective stress.

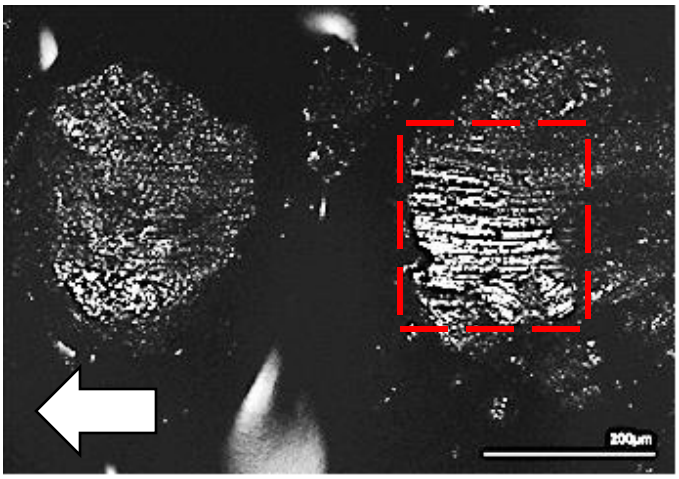

Figure 3-5: Confocal microscope with laser source image showing fatigue crack striations (in box) with smearing in the direction of slip (arrow) on die-side solder bumps.

The plastic strain rate was calculated for the plastic region of each cycle. The plastic region was assumed to be the area under the force vs. cycle plot in which the force values of the cycle of interest where all above the maximum force value of the next consecutive peak. The plastic strain rate calculated for each cycle was then plotted to examine the effect of cycling on the strain rate (Figure 3-6). The effective plastic (inelastic) strain was calculated using Darveaux's model at points along the loading curve (above the peak of the next consecutive cycle) and at peak load, and using the derivative of a curve fit to determine the strain rate for each peak. As the original strain values were quite small, a log scale was used for the curve fit. The bounds of the curve fit are determined by the peak load values for the cycle of interest and the next consecutive cycle. It is seen in the figure that strain rate increases in later cycles and then drops appreciably in the final cycle before failure. This increase is believed to be due to crack initiation and propagation in the interconnects as cycling continues. In future testing, in situ resistance measurements will enable observation of cracking in real-time. The resistance data can then be examined to determine if, and how much, cracking is occurring during the period of increased strain rate.

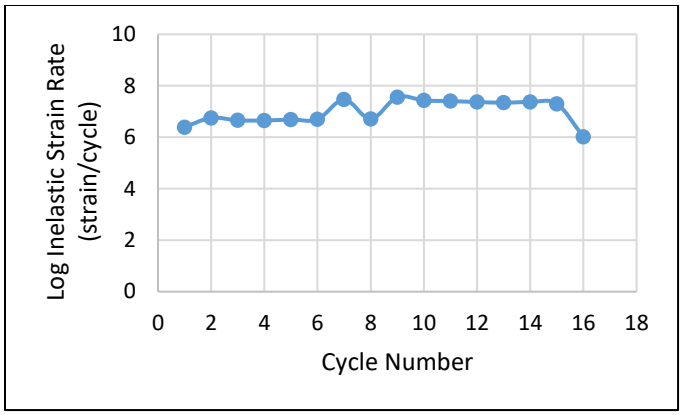

Figure 3-6: Effective plastic strain rate as a function of cycles for test vehicle 7 (Sn63/Pb37).

The estimated thermal fatigue life for these devices was modeled based on their isothermal CTF. The values used for calculating strain energy density can be seen in Table 3-2. Figure 3-7 shows the log-log plot of isothermal CTF and strain energy density. From the trendline of this graph, the constants for thermal fatigue model were determined. The thermal fatigue life prediction as a function of strain energy density is shown in Figure 3-8, using a model dependent upon Darveaux's creep strain model.

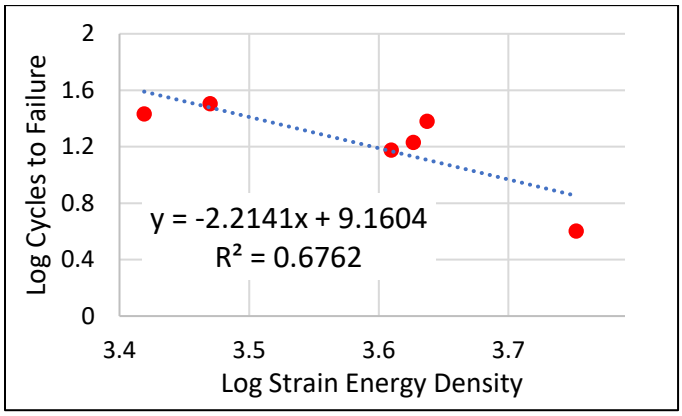

Figure 3-7: Log-log plot of isothermal CTF and strain energy density.

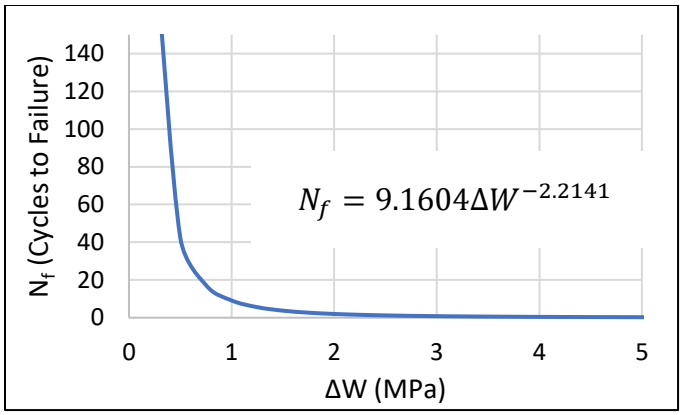

Figure 3-8: Thermal fatigue life prediction as a function of strain energy density.

3.5. Simulation Results

In order to better correlate the results of mechanical cycling to thermal cycling for use in predicting fatigue behavior in either operation or accelerated testing, it is necessary to compare the physical understanding of the solder interconnects' mechanical behavior in both types of stress environments. To compare the damage mechanisms in solder interconnects under the cyclic mechanical loading versus traditional temperature cycling tests, ANSYS 17.1 was utilized to perform Finite Element Analysis (FEA) on the examined flip-chip test vehicle. Figure 3-9 compares the maximum shear stress distribution under temperature cycling and cyclic shear loading on the most critical (i.e. highest failure risk) joint. Although there are some slight variations in the two, it is important to note that the peak stress locations are identical for the two test types, and the failure mode demonstrated in the mechanical testing (Figure 3-5) is consistent with both the simulation results, as well as with traditional solder fatigue failures in ball grid array and chip scale package (CSP) solder interconnects under thermomechanical testing.

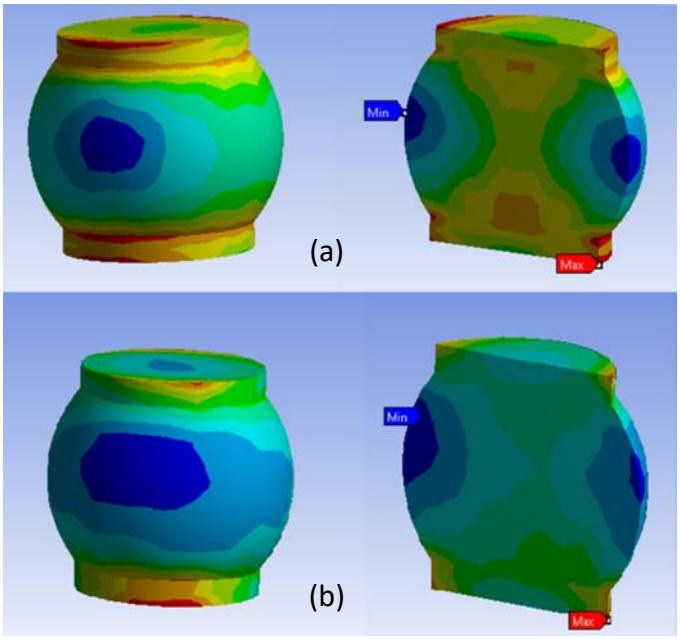

Figure 3-9: Equivalent stress distribution at the most critical solder joint during (a) temperature cycling and (b) shear load cycling.

Moreover, for creating a translation of the relationship between thermal cycling damage to the appropriate mechanical shear test protocol, the associated key damage parameters such as stress and plastic work accumulation must also be related. One key benefit of the mechanical approach is that it greatly reduces reliability test duration, as cyclic frequency can be increased up to fractional second cycle periods. As such it is important to evaluate both stress and creep-related damage accumulation in both cases. Plastic work density for temperature cycling and mechanical shear cycling (at room temperature: 22°C) were simulated for different stress conditions as shown in Figure 3-10a and 3-10b, respectively. Five standard thermal cycling ranges are considered here (JEDEC Conditions, J, N, G, B, and C) and compared with a sinusoidal applied shear force that represents the mechanical cycling method, ranging from zero to varying peak shear loads. The peak applied force is indicated for each mechanical cycling test simulation and results are depicted for three cycles of both experiments. According to the

simulation results, the maximum plastic work occurs during the first cycle in mechanical cycling, after which the plastic work increase per cycle remains relatively constant, which resembles the trend observed for the second and third temperature cycles for all temperature ranges.

This result appears to contradict the experimental assumption that there is no plastic work done in the first cycle. However, a close examination of how each method calculates this result can explain this contradiction. As the FEA calculations are node/element based, they do not account for any net deformation across the joint material and subsequent chip deflection as seen in the experimental tests. These FEA methods are consistent with current application in industry for estimating lifetimes or damage accumulation in TC, however, this is virtually impossible to measure experimentally. Thus, when calculating experimental plastic work, it is targeted at total chip displacement during applied stress cycles, and then volume averaging over the initial interconnect geometry.

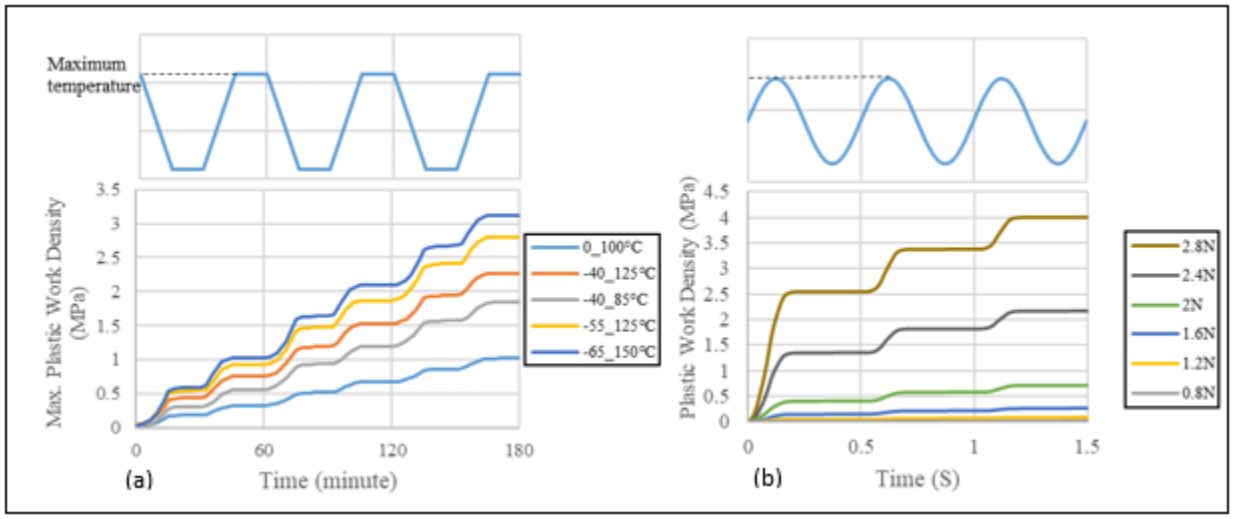

Figure 3-10: (a) Temperature profile and plastic work densities per unit time for five thermal cycling ranges (b) Force profile and plastic work densities for cyclic shear loading.

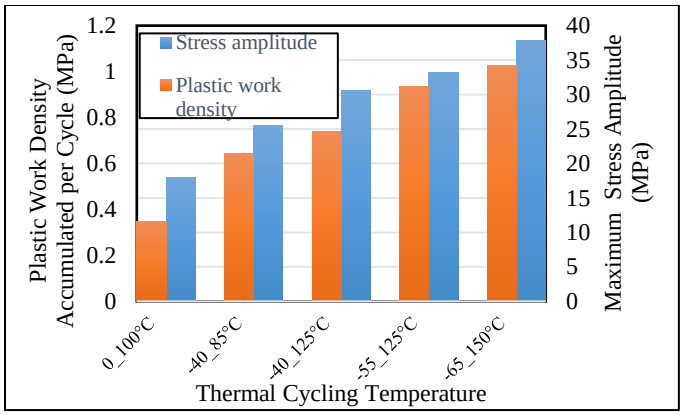

Figure 3-11: Calculated plastic work density accumulated per cycle and maximum stress amplitude during thermal cycling for different temperature ranges.

The maximum stress amplitude and plastic work density accumulation at the 3rd cycle of thermal loading of the test vehicle were determined, as shown in Figure 3-11. As the accumulated plastic work stays consistent after the second cycle, it represents the accumulated plastic work of the whole thermal cycling process.

Additionally, Figure 3-12 depicts the corresponding accumulated plastic work per cycle and principal stress amplitude in the solder joints for the shear force cycling methodology for a range of applied cycling shear loads, with the associated accelerated temperature tests that create a similar effect at the critical joints. The maximum stress amplitude is the variation of principal stress at the critical joint (joint that tolerate the maximum stress) during one cycle. Based on these graphs, a correlation between the stress amplitude and plastic work density between both test methods can be established. The results of mechanical cycling and temperature cycling tests that generate same stress amplitude are also shown in the Figure 3-12.

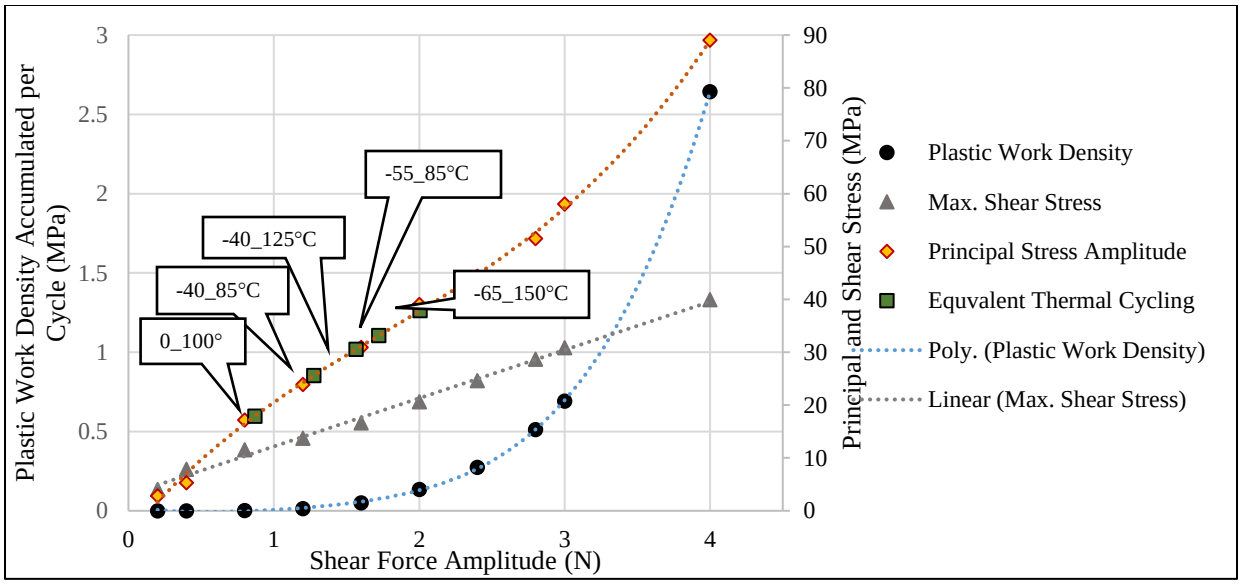

Figure 3-12: Calculated change in plastic work density per cycle and maximum principal stress amplitude during shearing force cycling (at room temperature, 22°C).

Based on the minimum and maximum temperatures, stress in solder joints may vary for different thermal cycling tests and a consistent relation between the maximum stress amplitude, as the main driving factor of thermo-mechanical fatigue, and maximum plastic work density cannot be found for every thermal cycling test. It is mainly because of viscoplastic behavior of solder material. Therefore, to relate the plastic work density accumulation per cycle of these two tests, the conversion coefficient *C* is calculated from the following equation,

$$\Delta W_{TC} = C\Delta W_{MC} \tag{3.10}$$

Where ΔW_{TC} is the increase in plastic work density (in Pa) in a thermal cycling test and ΔW_{MC} is the increase in plastic work density for mechanical cycling at 2 Hz. The conversion coefficient of the simulated mechanical test at room temperature is presented in Table 3-3 for different maximum shear stress. 15-minute dwell and ramping time is considered in all the thermal cycling simulations. Using this table, the number of cycles to failure for a thermal or mechanical cycling test can be estimated using Darveaux's fatigue model (equations 10-12)

where N_0 is the number of cycles required for crack nucleation and N_p is the number of cycles where crack propagation is the main contributor to plastic work density. N_T is the total number of cycles to failure. The equations shown below allow the calculation of equivalent mechanical cycles from TC data. To calculate the thermal cycles to failure from mechanical cycling data, ΔW_{MC} is used and the subscripts on the N terms are reversed to indicate mechanical data is being used. The constants used in the calculations are shown in Tables 3-3 and 3-4.

$$N_{0TC} = K_1 \Delta W_{TC}{}^{K_2} \tag{3.11}$$

$$N_{pTC} = \frac{a}{K_3} \Delta W_{TC}{}^{-K_4} \tag{3.12}$$

$$N_{TMC} = \frac{N_{0TC}}{C^{K_2}} + \frac{N_{pTC}}{C^{-K_4}} \tag{3.13}$$

Table 3-3

DARVEAUX'S CONSTANTS FOR Sn63/Pb37

a (m)	0.33
$K_1 \left(\frac{\text{cycles}}{\text{Pa}^{K_2}}\right)$	3.08E+10
K_2	-1.49E+00
$K_3\left(\frac{\text{m}}{\text{cycles} \cdot \text{Pa}^{K_4}}\right)$	1.16E-13
K_4	1.16E+00

Table 3-4

CONVERSION COEFFICIENT OF THERMAL CYCLING TO MECHANICAL CYCLING (@ 22°) MAX.

SHEAR STRESS AMPLITUDE OF MECHANICAL CYCLING TEST (MPa)	**0_100°C**	**-40_85°C**	**-40_125°C**	**-55_125°C**	**-65_150°C**
4.0	2.45E+04	4.56E+04	5.23E+04	6.61E+04	7.25E+04
7.5	1163.45	2147.04	2464.07	3112.11	3412.51
8.9	155.32	288.77	331.41	418.57	459.0
9.0	24.52	45.57	52.30	66.05	72.43
10.3	7.11	13.27	15.17	19.14	20.99
13.3	2.59	4.81	5.52	6.97	7.65
18.8	1.0	1.86	2.14	2.70	2.96
21.7	0.56	1.03	1.185	1.50	1.64
20.2	0.52	0.93	1.07	1.35	1.48
28.6	0.11	0.20	0.23	0.29	0.31

For example, a Si-based mock test vehicle of a flip chip SiC MOSFET with Sn63/Pb37 joints which was demonstrated to pass JEDEC TC-“B” condition at 1000 cycles, could alternatively be shown to meet the same criteria, using mechanical cycling at 2 Hz for 3110 cycles at a 13.3 MPa loading condition, completed within ~26 minutes. The same criteria could also be demonstrated at 28.6 MPa for 43.9 cycles, to be completed within 0.37 minutes. The large time difference between these two results is due to stress selection. When conducting a test, the conditions must be well posed. In order to generate equivalent levels of plastic work, higher shear stress amplitude or more cycles are required in mechanical cycling. However, considering that the fastest common temperature cycling frequency (3 cycles/hr.) requires 333.3 hours to achieve 1000 cycles, using a mechanical cycling test to simulate temperature cycling results in significant time savings.

3.6. Discussion and Results

The preliminary results demonstrate this approach as a viable alternative to commonly used environmental testing methods, which require expensive equipment that can often have their own reliability concerns, the associated time-consuming operation, and the large degree of uncertainty that comes from the combination of transient temperatures applied to device designs and materials which do not behave consistently across electronic package designs. This method seeks to eliminate some of the key obstacles and challenges encountered with using TC, PC or TS methods. In all of these methods, there exists a thermal component. In a high temperature environment, many additional damaging phenomena can occur in addition to CTE mismatch induced stresses, and may thereby confound the failure results when attempting to create acceleration models to predict actual operating condition lifetimes. For instance, oxidation, decomposition, and diffusion simultaneously interact with thermal stresses, in addition to possible electromigration commonly seen in PC testing. As diffusion has been shown to follow thermal gradients [16], chemical interactions in thermal-based testing are magnified. These interactions can create failure modes that are compounded with fatigue failure which may not always be present in non-accelerated operation.

In this new testing regime, the stresses are induced solely from mechanical stimuli. This has some advantages. By removing the temperature component completely, the complications in failure mechanics caused by thermal gradients are removed. As such, the effects of the mechanical stresses can be studied in detail. Moreover, future efforts, will evaluate elevated temperature (iso-thermal) mechanical testing, to further de-convolute temperature and stress effects, for better representation of the physical failure mechanisms taking place. With a deep understanding of the effects of mechanical shear stress on the solder system developed, the

results of this test methodology can then be paired with other testing methods (such as TC and PC) where non-mechanical effects are involved to create a holistic understanding of total stress environment. Due to the complex nature of that stress environment, the effects of each variable can be isolated and then utilized in the development of more accurate constitutive models, in determining and predicting damage accumulation leading to failure in flip-chip interconnects.

Since there will always be a temperature component in real-world application, these reliability effects will have to be considered in the design. Using this integrated approach, damage that arises from the individual factors normally compounded together in operation and typical acceleration tests can be identified independently, and thereby made clearer with the ability to inform optimized design for reliability. This novel method allows for in-depth study of the relationships between design, material selection, mechanical stress and failure. Thus, the effects of mechanical stress can be understood in detail, which becomes even more important in extreme operating environments where new materials may need to be developed for high temperature operation where there are not any standard environmental tests.

Simulation results show similarity in the equivalent and maximum shear stress distribution of the most critical joint during temperature and shear load cycling. Moreover, the mechanical creep behavior of the solder material can be modeled by Anand's viscoplastic model [17] with acceptable accuracy. The plastic strain rate, and therefore its plastic work, is highly related to the temperature. So, for an equal stress amplitude, solder material in temperature cycling experiences higher plastic work compared to the mechanical cycling. Therefore, the temperature effects on plastic work need to be modeled and account for in order to find the relationship between temperature cycling and mechanical cycling. Accordingly, by calculating the maximum stress amplitude in the solder joint for a specific thermal cycling range using FEA

simulation, equivalent mechanical cycling that generates a similar stress profile can be found which means related MTTFs, in terms of cycles, yet at greatly reduced testing time.

Additionally, when considering solder fatigue, the life time of the solder interconnects are often considered to be proportional to plastic strain [18-20] or plastic work (inelastic energy) [20-25]. Darveaux's equations are commonly used as the accepted method to estimate the life cycle of the solder interconnect, which relates the failure time under cyclic load to the plastic work density. The similarity in increase of plastic work density per cycle makes a strong case for the use of mechanical loading to simulate thermal operating cycles. As such, reliability relationships can be expected to follow similar trends, and CTF may likely correlate well with the number of cycles to failure predicted by the Darveaux method.

As Darveaux's empirical equation has a reasonable compliance with experimental results in this work, even for different cyclic loading conditions [6], the presented mechanical test methodology has the opportunity to aid in the development of physics-based acceleration models in precisely relating empirical stress/energy data for a given solder material and assembly process. Since the stresses are directly applied and associated displacement measured, it represents an efficient alternative to environmental testing, which though commonly used, creates vast amounts of uncertainty related to thermally dependent design impacts. Future work will establish the effects of strain rate, isothermal temperature changes, and materials, for developing reliability models that can be universally applied during the design stage without need for expensive validation, which becomes increasingly important as electrification of transportation systems require high reliability for safe operation, yet costs of wide bandgap devices and packaging are still high.

3.7. Conclusion

The methodology presented and demonstrated herein represents a significant opportunity to reduce the cost and time of reliability testing, particularly where new packaging methods and materials are needed to meet the demands of electric vehicle operation environments. In this work we demonstrated the opportunity to reduce testing time based on plastic work by at least 10x, depending on the material. In developing this rapid reliability translation technique, the design of future power devices can be optimized to limit mechanical failure risk during design stage to further increase power density and performance. Furthermore, once the contributions to failure of mechanically induced stresses are well understood, the contributions of each of the other factors become more easily separated and predicted using finite element simulations. Thus, we can begin to deconvolute the relationship between each of the contributing factors to the whole of thermomechanical reliability.

3.8. Acknowledgements

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3.9. References

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4. Expedited Fatigue Testing with *in situ* Resistance Monitoring for Failure Detection in Flip-Chip Solder Interconnects

To facilitate the testing methodology, two test stands were designed and fabricated to interface with a Nanovea T50 tribometer which acted as the prime mover within the assembly and supported the load cell for force measurement. Both test stands use the tribometer's integrated linear stage to translate the chip, thus stretching springs which are rigidly fixed at one end. As discussed in the previous section, this spring deflection generates the force which is transmitted to the solder interconnects in the form of shear stress by the testing apparatus. It was important to minimize friction within the system to ensure that the vast majority of the force recorded by the load cell was due to spring resistance rather than frictional resistance to the translation mechanism.

4.1 Test Apparatus 1: One-Directional Translation

The first system was capable of operation in a single mode where the shear load was only applied in one direction. The springs were attached to a two-part carriage that was fixed to the translating stage. The lower half of the carriage acted as a base, rigidly attached to the stage by screw type fasteners. The upper section of this carriage comprised the clamping system responsible for load distribution to the device, where a cap placed over the die of a test device (see Figure 3-1) was held in place by the vise system. This upper carriage assembly was attached to the lower carriage by a T-slot and flange system which ensured degrees of freedom in the translation direction. This freedom allowed the upper carriage to respond to deformations within the solder interconnects. As fatigue progresses, the solder joints deform in response to the force along its line of action (see Figure 4-1), thus moving the die, necessitating that the carriage move concurrently to maintain proper contact with the die. In this test configuration, the springs are

attached at one end to the free-sliding upper carriage and at the other end to a fixed arm attached to the load cell. As the springs are stretched, the resultant force was felt by this arm assembly and recorded by the load cell.

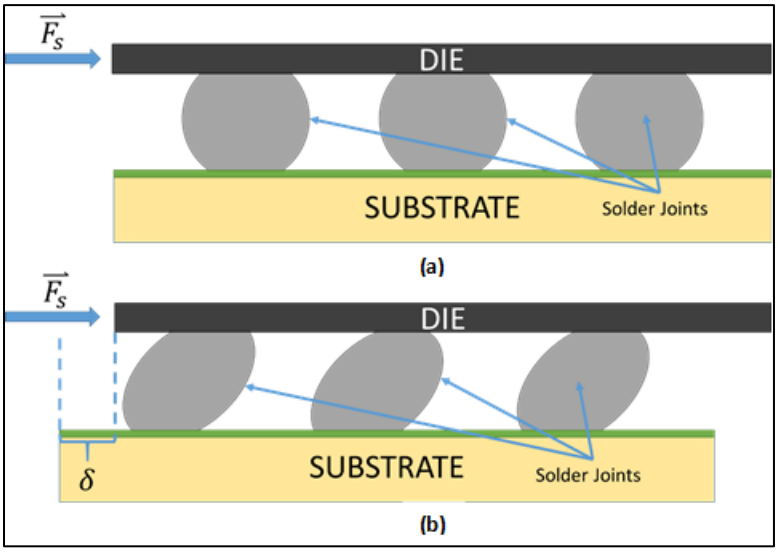

Figure 4-1: (a) Position of solder joints in untested sample. (b) Deformation of solder joints and die deflection (δ) after prolonged stress cycling.

This system was designed to accommodate a device footprint of up to 30 mm x 30 mm for both die and substrate. Given the spatial limitations of the stage, larger footprint devices were not possible, however, the testing methodology could certainly be scaled up with the use of another prime mover in place of the current tribometer. Force magnitude is determined by the spring constant of the springs selected with the limitation that maximum resultant spring force be ≤ 20 N which was the maximum safe load for the tribomerter load cell used in this project. All testing with this testing configuration was performed at room temperatures with a cyclic frequency of 1 Hz. Measurement resolution using this testing configuration was determined to be ± 0.0079 N. To ensure precision between tests, it is necessary to run a calibration test of the springs both before and immediately after performing a fatigue test. A full procedure for the

calibration test can be found in Appendix A. This testing apparatus is shown in fatigue testing configuration in Figure 4-2.

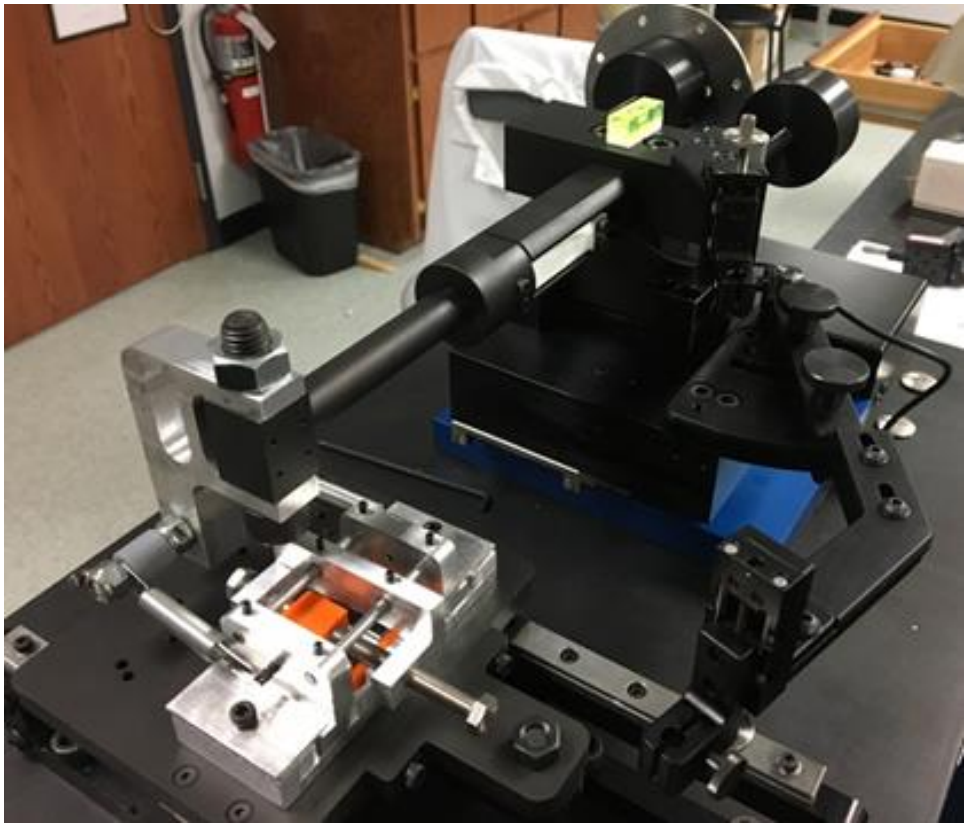

Figure 4-2: Test apparatus 1 and tribometer instrumentation.

4.2 Test Apparatus 2: Bi-Directional Translation

Given that creep is one of the main sources of fatigue in relevant solder interconnects under operational conditions, there was a need to emulate creep behavior within the reliability testing method without negatively impacting the rapid nature of the test. Leveraging the coupled temperature and time dependence of the creep mechanism, the second testing apparatus was designed to operate in elevated steady-state temperature environments to emulate room temperature creep behavior. This was achieved by designing the second generation apparatus to work inside a ring oven which was affixed to the T50 tribometer. The inclusion of the ring oven

resulted in a significant reduction in available space, necessitating an extensive redesign of the loading system. In this second iteration, the horizontal layout from the first design was flipped vertically, with the springs, loading cap, and free-sliding carriage all arrayed above the die of the test device. Additionally, a smaller stage was required that could operate within the confines of the oven. By switching out the stages, the effective translation distance was changed from +30 mm to ± 12 mm with the smaller stage with a resultant reduction in spring force for a given spring constant.

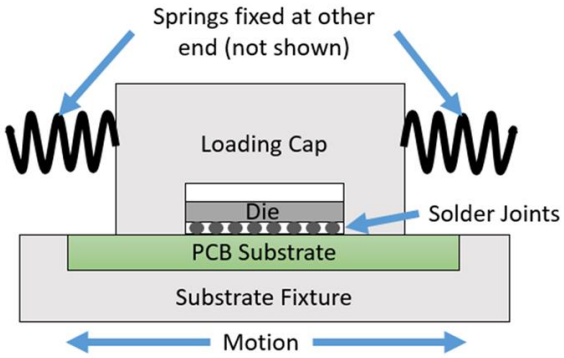

Figure 4-3: Schematic of the loading configuration for the second design iteration.

In this test configuration, the vise, upper carriage, and loading cap were replaced with a composite assembly where the sliding portion of the carriage and loading cap were directly coupled via screws. Additionally, the entire upper assemble is attached directly to the cantilevered load cell arm, saving space and making measurements more accurate since the springs engage directly with the arm via the upper assembly main bolt rather than through a dedicated transfer arm like that seen in the previous design iteration. Rather than the springs being attached outboard of the carriage, they were placed ahead of and behind the carriage, directly along the line of action (see Figure 4-3). Each spring is captured within the rail system with internal guides to prevent warping or bending of the springs as they compress and are fixed to the rail system at the opposite end of the spring from the carriage. This improvement ensured

that no rotational torque was placed on the die as the result of unbalanced springs, where one was slightly stiffer than the other. To reduce friction even further from the initial design, very low friction sleeve bearings and capture washers were used in the sliding assembly, resulting in force measurements which more accurately characterize the effective force experienced by the springs.

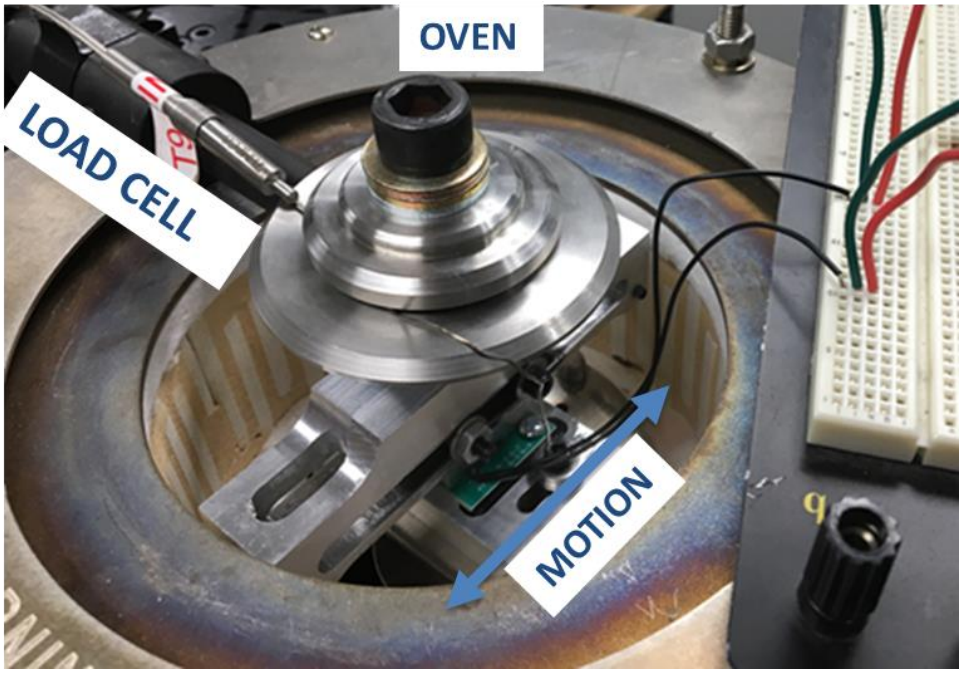

Figure 4-4: Test Apparatus 2 with load cell and resistance monitoring circuitry.

Another feature incorporated in the second configuration was the ability to monitor device circuit resistance and device temperature *in situ* as the solder interconnects undergo fatigue testing. To enable this capability, a new baseplate was designed with room for electrical leads to route under the upper assembly and a channel drilled into the center of the baseplate to allow for a thermocouple to rest under the device for the most accurate reading of *in situ* interconnect temperature (see Figure 4-4). The supported device footprint remains 30 mm x 30 mm with a maximum force of ± 20 N. Testing frequency remains 1 Hz for tests conducted using this configuration with a sensor resolution of ± 0.0092 N. This testing method can be used at

both ambient and elevated steady-state temperatures up to 440 °C. When testing at elevated temperatures, care must be taken to ensure true steady-state conditions.

4.3 Mechanical Cycling With Test Configurations

Both testing configurations use continuous sinusoidal loading profiles with the frequency set by the inputs made to the tribometer motor controller. Both testing configurations were designed to be as adaptable to new device geometries as possible while remaining compatible with the T50 tribometer hardware. The 3D printed substrate carriers and the loading caps (ABS and metal) can be configured to support a wide variety of devices quickly making the entire test stand very versatile, capable of testing many fully operational chip-scale and package-scale devices. Accurate testing with both methods requires that the spring coefficients of the springs used must be as close to identical as possible. The spring coefficients can be determined during the calibration tests prior to data collection. Spring wear and fatigue can be tracked by evaluating the spring coefficients before and after each test. Springs should not be used once the spring constants have begun to degrade.

Initial testing was conducted using a Si test chip designed as a non-functional mechanical analog (dummy die) of a SiC MOSFET device on an FR4 substrate. The 3 mm x 4.4 mm test chips were constructed with thirteen 0.381 mm (15 mil) solder interconnects with 0.305 mm SMD (Solder Mask Defined) solder resist openings. Testing focused on devices with lead-free Sn95/Sb5 interconnects with Sn42/Bi57.6/Ag0.4 solder paste in the openings and devices with eutectic (Sn63/Pb37) interconnects and paste. To determine the appropriate test load, die shear tests were conducted with die shear strengths of the lead-free units averaging 29 MPa and the die shear strengths for the eutectic units averaging 35.1 MPa. Based upon these results, fatigue testing was targeted at 50% of the recorded die shear strengths for each material set with a

frequency of 60 cycles per minute (1 Hz). The weakness of using these dummy die was in being unable to quantify failure by means other than complete die separation since the devices were non-conductive. For use with the *in situ* resistance capabilities of Test Apparatus 2, a new test device was designed and fabricated which possessed an active die with full electronic functionality. This new Test Vehicle 2 (TV2) was designed with forty 0.254 mm solder interconnects connected into a symmetrical daisy chain with additional pad locations to act as taps between interconnects for failure localization. Details of the design and the design process are included in Appendix C. These devices were tested at 30% of their average die shear strength (52.4 MPa) due to the safety limitations of the load cell with a frequency of 1 Hz.

4.4 Reliability Evaluation with Test Apparatus 1

Table 4-1: Results of Experimental Fatigue Tests with Apparatus 1

Cyclic Loading Results

Material Set: Sn95/Sb5 Sphere with Sn42/Bi57.6/Ag.04 Paste			
Sample #	**Cycles to Failure**	**Peak Effective Stress (MPa)**	**Strain Energy Density (Pa)**
1	**4**	**18.4**	**1761.7**
2	**17**	**16.2**	**1319.7**
3	**24**	**15.8**	**1351.8**
7	**15**	**15.4**	**1268.3**
Material Set: Sn63/Pb37 Sphere with Sn63/Pb37 Paste			
Sample #	**Cycles to Failure**	**Peak Effective Stress (MPa)**	**Strain Energy Density (Pa)**
10	**100435**	**15.8**	**10196.8**
11	**296443**	**15.8**	**10752.0**
12	**39778**	**15.2**	**9951.6**
13	**201328**	**16.9**	**12329.7**

All tests conducted with Apparatus 1 were conducted at 1 Hz with the dummy die device under ambient conditions. Using techniques discussed in Chapter 3 and the cycles-to-failure (CTF) for a given device, the amount of damage that was accumulated during testing as a result

of the applied shear stress can be assessed. Examination of Table 4-1 shows that the lead-free dummy die failed much more quickly than did the eutectic units. The shorter fatigue lives and lower strain energies recorded for the lead-free units were attributed to the lower shear strength of the lead-free material. The higher strain energy densities observed in the Sn63/Pb37 units reveal that the devices were able to survive higher accumulated strain energies most likely as a result of the induce shear stresses being a lower percentage of the devices' ultimate shear strengths. It can be seen from Figure 4-5 that work accumulation rate is much higher in the lead-free material for a given applied stress. When examining the relationship between accumulated work (damage) and CTF (Figure 4-6) it is clear that the two materials exhibit opposite trends with accumulated work decreasing with higher CTF for the lead-free materials, while accumulated work increases with higher CTF for the eutectic materials. The dissimilarity between these two trends may be due simply to the large difference in cycle lives between the two unit sets. Due to their substantially longer cycle lifetimes, the Sn63/Pb37 units were allowed more time to accumulate damage. Additionally, there was a large range between the fatigue lifetimes of the eutectic units with an early failure by unit 10 which may have been due to a processing defect that reduced the effective joint. A poorly bonded joint would have negatively impacted both the CTF and the sustained amount of plastic work before failure leading to the trend observed in Figure 4-6.

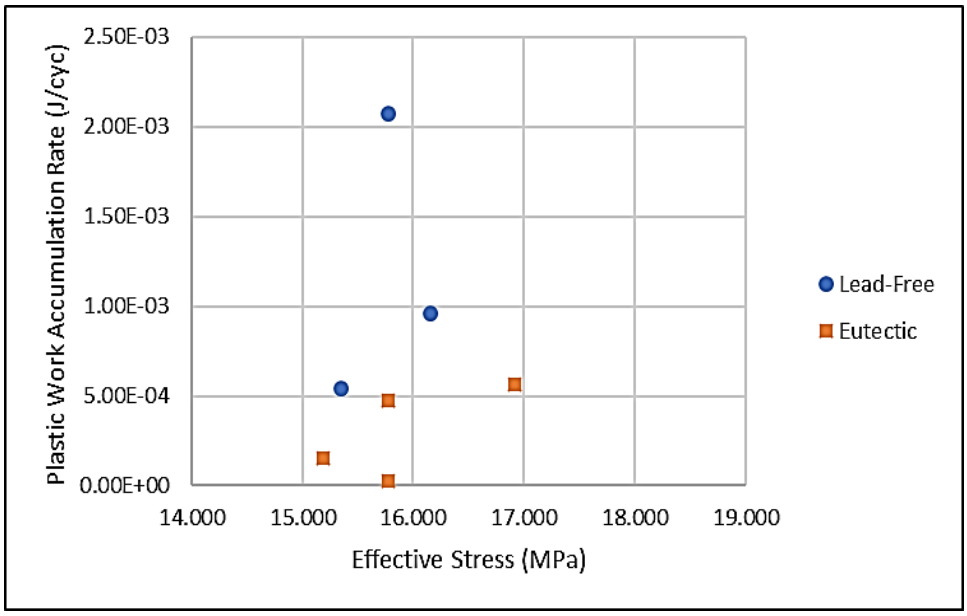

Figure 4-5: Plastic work accumulation rate versus effective stress.

SEM imagery coupled with the accumulation rate over the total test time where no force degradation was observed can be used to characterize the joint (see Figure 4-7). The number of cycles required to exceed the elastic limit can be determined and observations of joint ductility are readily formulated. The imagery also serves to reveal the location/s of the primary damage, enabling characterization of the effects of architecture, stress application rate, and damage accumulation on device reliability.

Once failure had occurred, the joints of each sample were examined to ascertain failure modes and assess the quality of each interconnect. In the lead-free samples, many of the joints were found to have failed to properly bond. To account for this discrepancy, a volumetric approach was taken where, the amount of damage accumulation was characterized as a function of the total solder volume under stress. The lead-free were observed to have very little or no damage or deformation of the solder spheres themselves during these joint examinations. The majority of the damage was seen within the solder paste in the pad opening and at the interface

between the paste and the bulk solder spheres (Figure 4-7). The paste was identified as the damaged material because it was seen to be located below the lip of the solder mask in the "well" of the joint. By comparison, the eutectic units exhibit damage more uniformly distributed throughout the solder columns with damage more frequently seen within the bulk solder spheres. From these observations, it was concluded that the volume of the material actually under stress in the lead-free units was primarily that of the paste solder material near the pads, while in the eutectic units, the entire available solder volume was opposing the stress. On that basis, volumetric work calculations were undertaken considering only the past volumes as effective joints in the lead-free devices. The entire available solder volume, including sphere and paste, was used in the calculations for the Sn63/Pb37 devices.

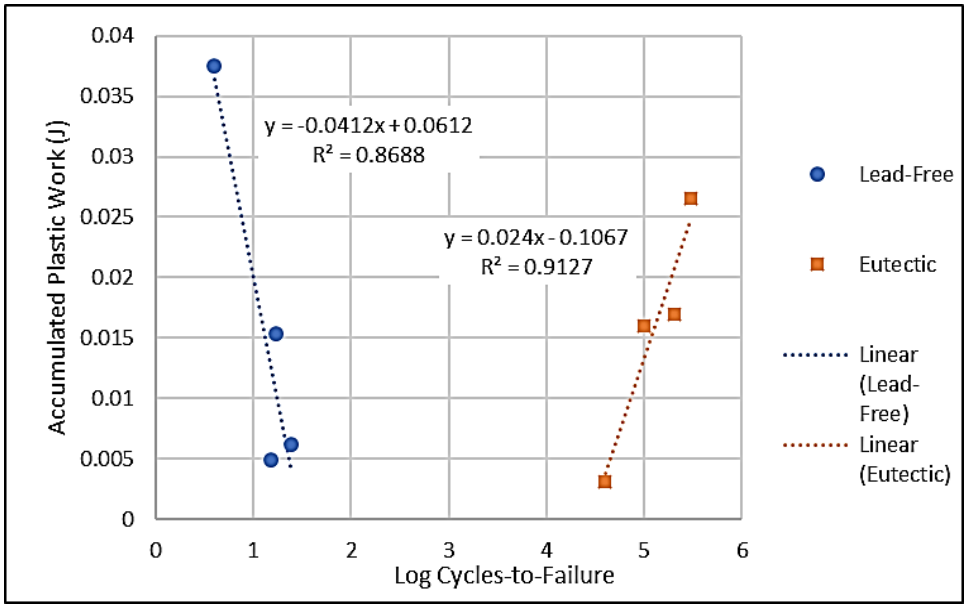

Figure 4-6: Accumulated plastic work versus log CTF.

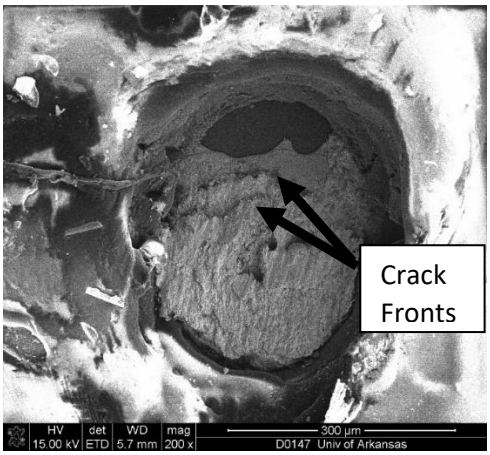

Figure 4-7: Top view SEM image of a Sn42/Bi57.6/Ag0.4 joint of a Si MOSFET. Multiple crack fronts are visible.

Examination of the load cell outputs for each test revealed that in all cases, the majority of damage was accumulating within a subset of the total number of cycles, generally those near the point of failure. This zone was termed the “accumulation zone”; all plastic work accumulated during the fatigue tests were attributed to cycles within this zone. The plastic work accumulation rate was calculated by dividing the total work accumulated by the number of cycles in this region for each sample. The cause of the difference between accumulation rate trends in Figure 4-5 may be the comparative ductility and shear strength of the joints of each individual sample. Figure 4-8 exhibits the load cell output for sample 7, showing a noticeable downward trend throughout the plastic region. A flatter trend with a shallower slope prior to failure would be expected for a more brittle sample with generally smaller accumulation region. Unit 3 is one such device, with an accumulation region that is only three cycles long.

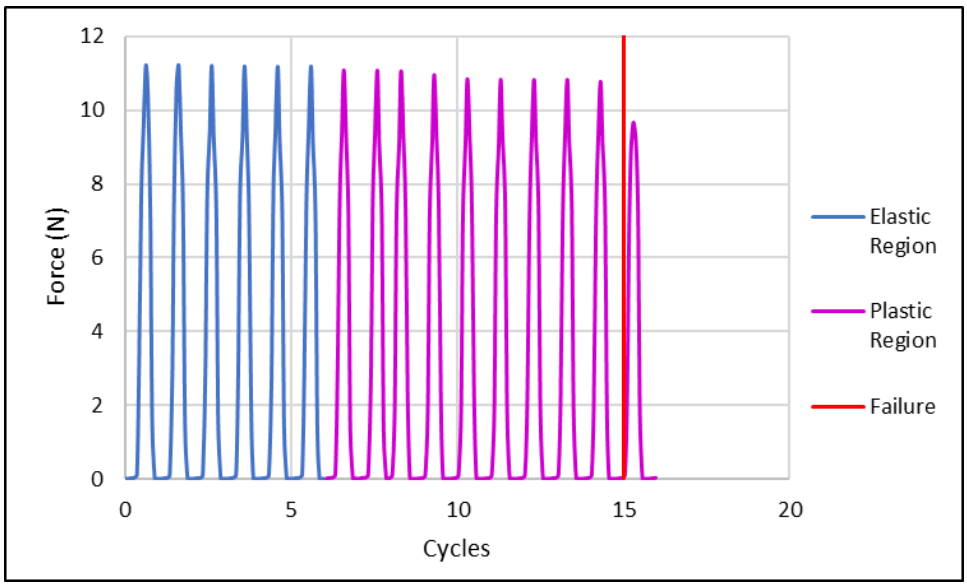

Figure 4-8: Load cell output for sample 7 showing force versus cycles with accumulation (plastic) region shown.

When these peaks were compared across material types, the eutectic material generally exhibited lower damage accumulation per cycle with a much flatter downward trends. For the eutectic devices, the apparent large accumulation regions seem to conflict with the brittle failure modes observed in the joints. This disagreement is resolved when the size of the accumulation region is considered as a percentage of the entire number of cycles prior to failure. The size of the accumulation regions for all dummy die samples are shown within Table 4-2 which illustrates that the lead-free interconnects were accumulating damage for a far longer percentages of their total CTF's as compared to the eutectic units. The size of the accumulation region for the Sn63/Pb37 dummy die never exceeded 0.4% of the total fatigue life in cycles. This result supports the conclusion that the eutectic failures were more brittle in nature, given that when the elastic limit was reached, and that the moment of fracture was so much shorter as a sub-set of the total time-to-failure (TTF). This conclusion was supported by SEM imagery taken of failed joints of each material (see Figure 4-9). In the case of the lead-free solder (Figure 4-9a), a more ductile failure, with more smearing behavior along the shear tip is observed. In the case of the

Sn63/Pb37 joint (Figure 4-9b), a large crack has split across the entire diameter of the bulk solder sphere, consistent with a much more brittle failure mode.

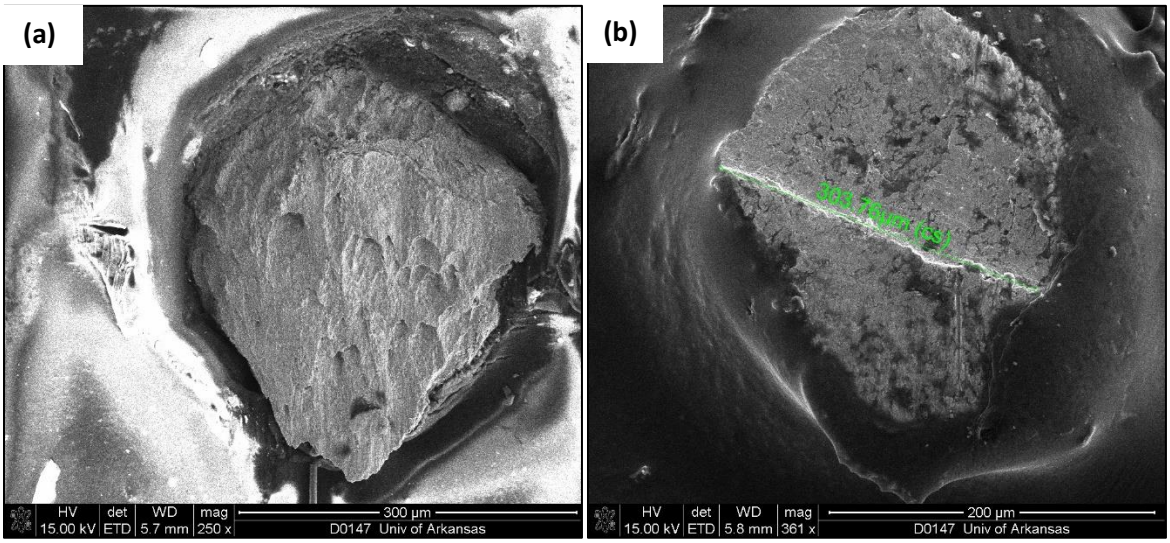

Figure 4-9: Top view SEM image of (a) deformation of chip-side joint in Sn42/Bi57.6/Ag0.4 solder paste of sample 2. (b) Bulk crack in Sn63/Pb37 material of die-side joint of sample 11.

Table 4-2: Calculated Damage Accumulation for Dummy Die Units

Plastic Work Accumulation Data

Material Set: Sn95/Sb5 Sphere with Sn42/Bi57.6/Ag.04 Paste

Sample #	Volumetric Plastic Work (J/mm³)	Accumumulation Rate (J/cyc)	Elastic Region (cyc)	Plastic Region (cyc)	Plastic cycles as percent of CTF
1	$6.91 \cdot 10^{-1}$	$1.25 \cdot 10^{-2}$	1	3	75%
2	$2.39 \cdot 10^{-1}$	$9.57 \cdot 10^{-4}$	1	16	94%
3	$1.26 \cdot 10^{-1}$	$2.07 \cdot 10^{-3}$	21	3	13%
7	$9.92 \cdot 10^{-2}$	$5.44 \cdot 10^{-4}$	6	9	60%

Material Set: Sn63/Pb37 Sphere with Sn63/Pb37 Paste

Sample #	Volumetric Plastic Work (J/mm³)	Accumulation Rate (J/cyc)	Elastic Region (cyc)	Plastic Region (cyc)	Plastic cycles as percent of CTF
10	$6.23 \cdot 10^{-2}$	$4.71 \cdot 10^{-4}$	100401	34	0.03%
11	$1.03 \cdot 10^{-1}$	$2.32 \cdot 10^{-5}$	295302	1141	0.38%
12	$1.20 \cdot 10^{-2}$	$1.54 \cdot 10^{-4}$	39758	20	0.05%
13	$6.60 \cdot 10^{-2}$	$5.65 \cdot 10^{-4}$	201298	30	0.01%

Plotting the plastic work density against the accumulation rate (Figure 4-10) revealed that both the amount of plastic work accumulated by the lead-free solder paste and the rate at which it occurred were significantly higher than in the case of the Sn63/Pb37 solder joints. Given that the ultimate shear strength of Sn42/Bi58 (27 MPa) is less than that of Sn63/Pb37 (34.5 MPa), it is intuitive that plastic deformation occurs more rapidly on both a per-cycle and overall CTF basis for the lead-free units, a deduction that is confirmed by the results of the fatigue tests.

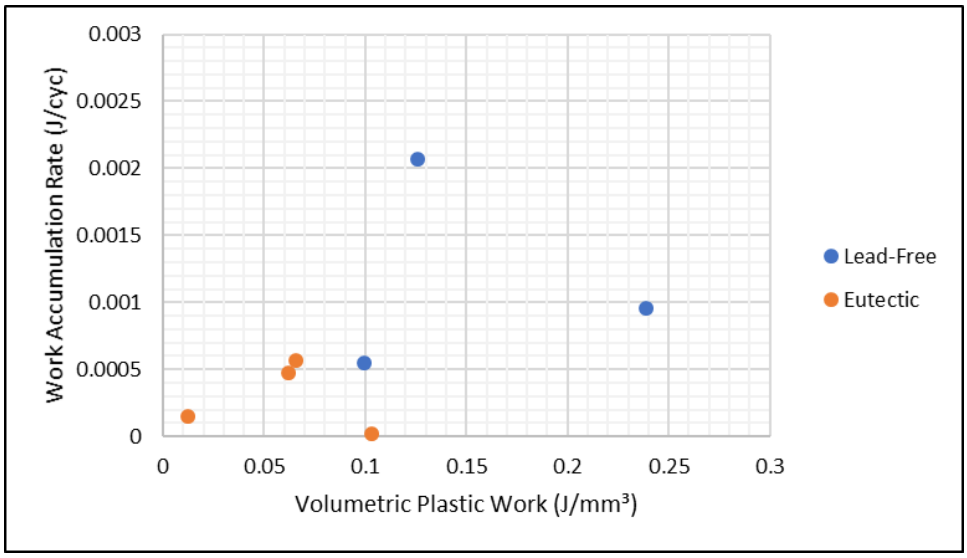

Figure 4-10: Volumetric Plastic work accumulation versus accumulation rate.

4.5 Elevated Temperature Testing with Apparatus 2

4.5.1 Dummy Die Test Chip

To evaluate the performance of the fatigue testing method at elevated temperature, both dummy die and TV2 units were tested using Apparatus 2. As stated previously, elevated temperatures were included to enhance the effects of creep given its coupled temperature and time dependence. This enhancement ensures that a device tested under accelerated conditions will experience failure modes more in line with expectations in the field. Additionally, elevated steady-state temperatures mimic operating conditions when a device is functioning at peak

temperatures during extended use. To extend the data set, two material sets were selected for use with the dummy die test chips; SAC 305 and Sn63/Pb37. Sn63/Pb37 was also used in TV2 for tests conducted with the *in situ* resistance monitoring functions enabled.

Using the dummy die, tests were conducted at 25 °C, 85 °C, 100 °C, and 110 °C (and 125 °C for SAC 305) to establish failure metrics for each material at various temperatures with an eye toward established behavior trends as devices cycle through a temperature range. Examination of the plastic work density for these tests reveals a unique trend; a clustering of data points where the total amount of work (damage) accumulated as a function of solder volume remained within a narrow band for all the testing temperatures (see Figure 4-11).

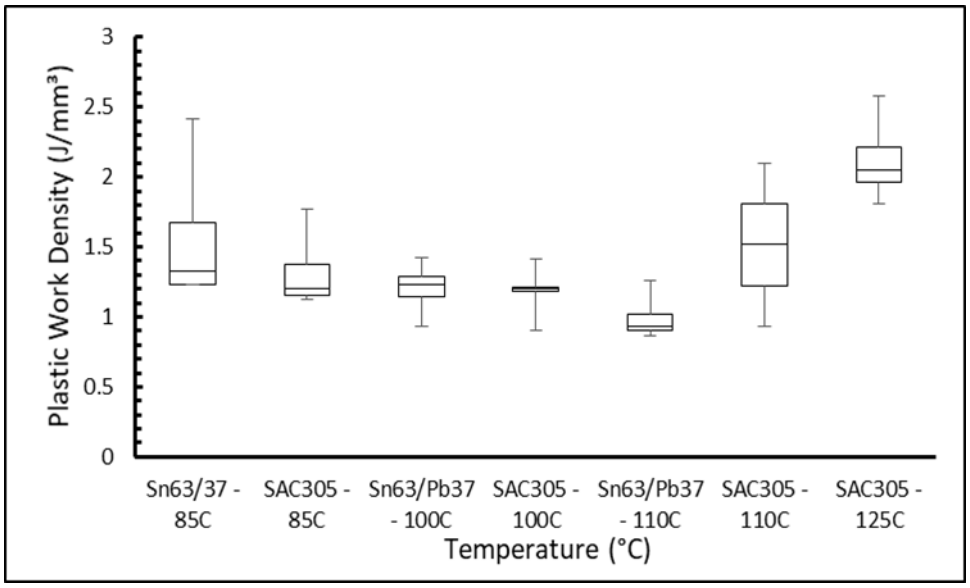

Figure 4-11: Plastic work density with temperature.

Examining the rate of work accumulation per cycle revealed that with increasing temperature the damage accumulation behaviors of the two materials were very different. Figure 4-12 details the relationship between work accumulation rates per loading (given the bi-directional nature, on cycle equals two loadings) and homologous temperature for the tested temperatures.

Homologous temperature is the ratio of operating temperature to the material's melting point and was chosen for use in this study in order to make a direct comparison between the two materials on the same scale. The trend for the eutectic Sn63/Pb37 dummy die show a much sharper slope to the curve with increasing temperature while the trend for SAC 305 units is much flatter with a more linear relationship between damage accumulation and increasing temperature.

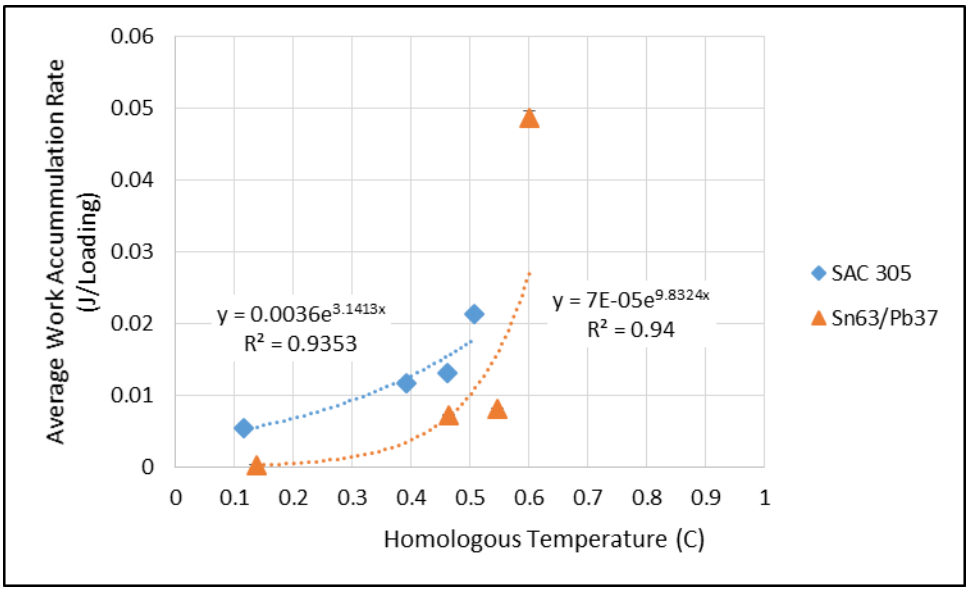

Figure 4-12: Work accumulation rate with increasing temperature.

The clustering effect seen in Figure 4-11 with all accumulated plastic work values for tested units of both material sets lying within a narrow band reveals that the amount of damage required to generate a failure within the dummy die device is independent of material or temperature. Rather, while required damage is constant, the TTF is reduced as temperature increases. Reinforcing this finding, the shear strain energy values for all the tested units of either material where found to lie between 12088.41 Pa and 14408.76 Pa ± 8% irrespective of test temperature. There was no relationship between temperature and strain energy density with both high and low values occurring within each temperature zone for each material. Given that in this application, the shear stress accounts for all energy input into the system as

plastic work, the accumulated plastic work and shear strain energy density are linked. When this is considered, the relatively constant nature of the one value supports the findings about the other.

The primary conclusion that can be drawn from Figure 4-12 is that temperature will have a larger effect on rates of damage accumulation in devices constructed using Sn63/Pb37 solder interconnects, and thus a greater impact upon CTF. SAC 305 has a higher melting point, likely giving the material a greater ability to endure test temperatures without noticeable damage accumulation, ultimately resulting in longer test durations. The damage accumulation behavior of the tested materials is directly related to the ultimate shear strength and the ductility of each with the more ductile material accumulating the necessary damage for failure much more quickly through a predominately ductile necking /smearing mechanism.

Additionally, ductility is impacted by temperature with more viscoplastic behavior replacing brittle cracking in units which were tested at elevated temperature. A small increase in temperature can have a large effect on the mechanism by which failure occurs. Figure 4-13 illustrates this fact, detailing the effects of a 15 °C difference in temperature had on failure mode in two dummy die units with SAC 305 joints with one tested at 85 °C and the other at 100 °C. This 18% increase in temperature resulted in the dominant failure mode transitioning from brittle void formation and cracking to extreme viscoplastic behavior exhibited by extensive smearing of the solder.

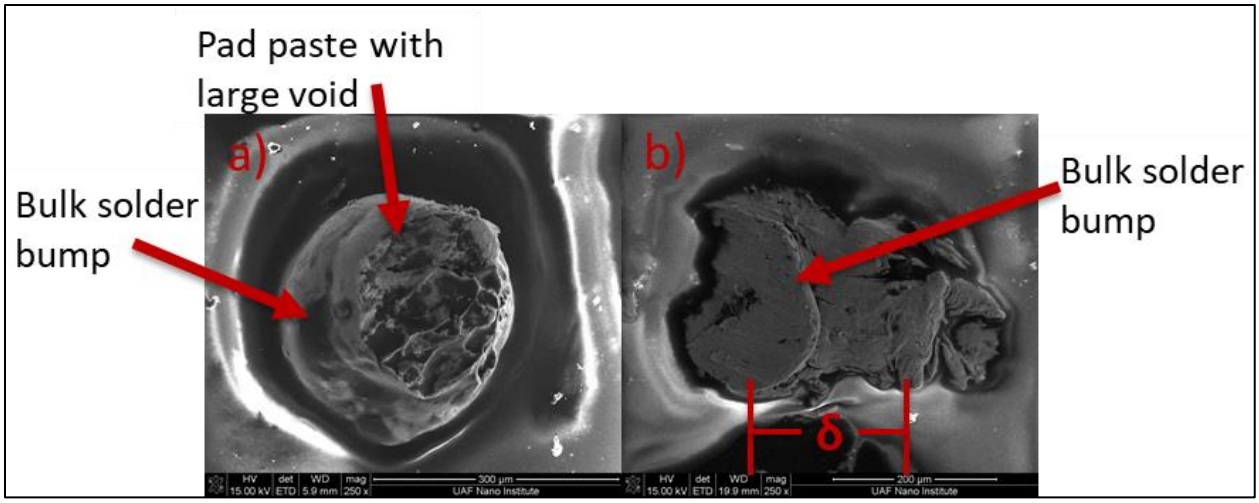

Figure 4-13: SEM Top view of (a) SAC 305 solder joint after failure when tested at 85 C. (b) SAC 305 solder joint after failure when tested at 110 C.

4.5.2 *in situ* Resistance Monitoring at Elevated Temperatures

Tests conducted using the TV2 devices confirmed that this second test unit was substantially stronger than the dummy die units tested previously, with much longer fatigue life times. Between the two test unit types, the total solder volumes are roughly the same (0.48 mm^3 or the dummy die and 0.46 mm^3 for TV2) but the cross-sectional area resisting the load in TV2 units (1.3 mm^2) is double that found in the dummy die units (0.7 mm^2) due to TV2 possessing many more solder joints. Larger joint cross-sectional area enables the TV2 units to sustain much higher stresses for longer periods, leading the longer fatigue lifetimes recorded. Figure 4-14 details the CTF results for the TV2 tests for the tested temperatures. All TV2 units were assembled with Sn63/Pb37 solder joints and tested with a loading frequency of one cycle-per-second (1 Hz).

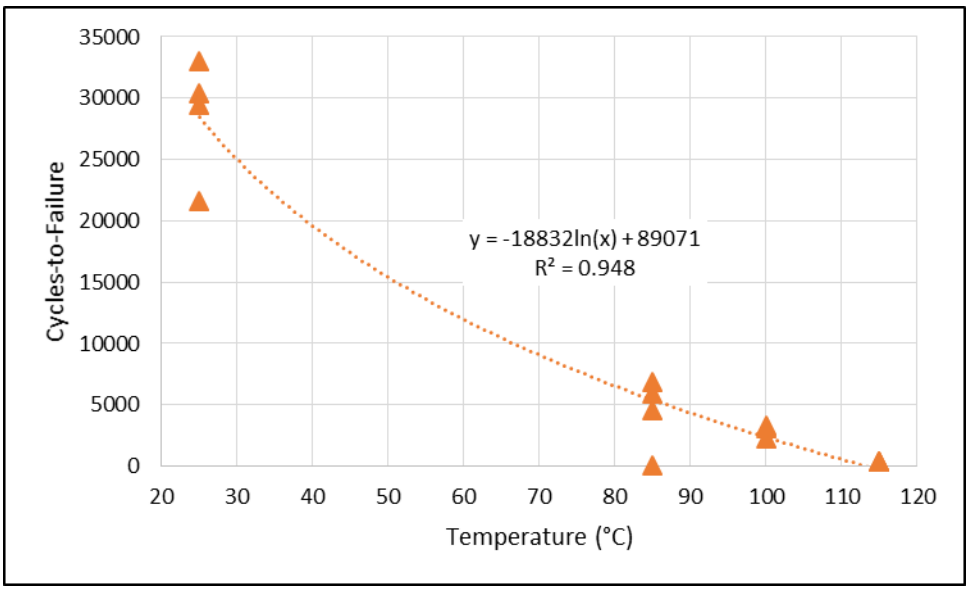

Figure 4-14: Cycles-to-failure for all TV2 units at test temperatures.

Resistance monitoring was conducted for these tests to evaluate the point of failure, defined as the point at which total circuit failure occurred. Total circuit failure was defined as the moment a high resistance event, such as a spike occurred with a resistance increase of 30% over the starting value. Thirty percent was chosen because in industry, a 30% increase in resistance is enough to seriously hamper device performance. In many cases, these high resistance events occurred in the form of resistance spikes which exceeded the resistance monitoring systems detection limit (500 Ω), indicating massive degradations in performance due to the thermomechanically induced damage. As would be expected, the achieved CTF for tested units decreased dramatically with elevated temperatures from an average of 28623.9 ± 14% CTF for the 25 °C tests to an average of 340.1 ± 3% for the 115 °C tests, representing an 84x reduction in reliability. The relationship between device reliability and temperature can be seen to be logarithmic, with temperature becoming increasingly impactful on fatigue lifetime.

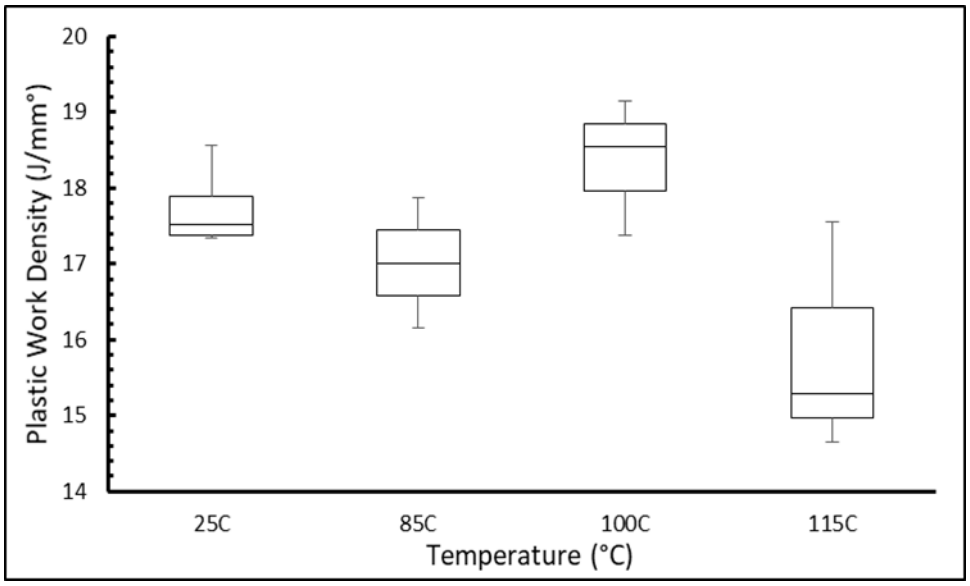

Figure 4-15: Plastic work density with respect to temperature for tested TV2 units.

Fatigue tests of TV2 units conducted with Apparatus 2 revealed similar trends to those seen with the dummy die devices. Examination of the total plastic work accumulated by the joints during testing at different temperatures again showed that the total energy value of accumulated damage required to induce circuit failure remained nearly constant irrespective of test temperatures. Figure 4-15 shows that for all testing temperatures, the plastic work density values ranged between 19.1 J and 14.6 J, a spread of 4.5 J. The slight downward trend is attributed more to the severely limited number of cycles before failure at the higher temperatures. Due to the much earlier failure times, the solder joints did not have as much time to accumulate damage. The standard deviation of all the damage values across all testing temperatures was ± 1.2 J/mm^3, a value corresponding to only 7% of the average plastic work accumulated across all devices; 17.3 J/mm^3.

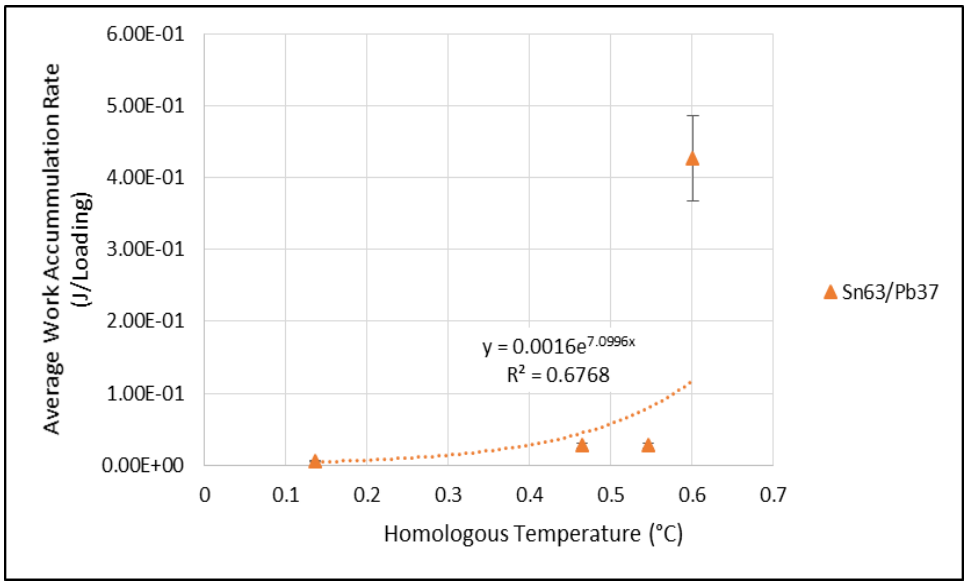

Figure 4-16: Average plastic work accumulation rate changes with temperature.

Plotting the average plastic work accumulation of devices tested at each temperature (see Figure 4-16) on the homologous scale provides information about the way damage accumulation is effected as temperature approaches the material's melting point. Examining the damage accumulation behavior, it is seen that the rate increases between the 25 °C, 85 °C, and 100 °C tests are relatively small followed by a very large plastic work accumulation rate increase for the 115 °C tests. While the individual rate values are larger, the shape of the curve and relative positioning of the data points are nearly identical to the trend observed for the dummy die which also had Sn63/Pb37 solder joints (see Figure 4-12). Typical deviation of approximately ± 14 % from the temperature specific average accumulation rates were observed for the first three temperatures. However, the standard deviation for the rate values of the 115 °C test units was ± 19%, likely due to larger variations in plasticity with the elevated temperature for those devices with some units experiencing slightly more plasticity in response to the higher temperature.

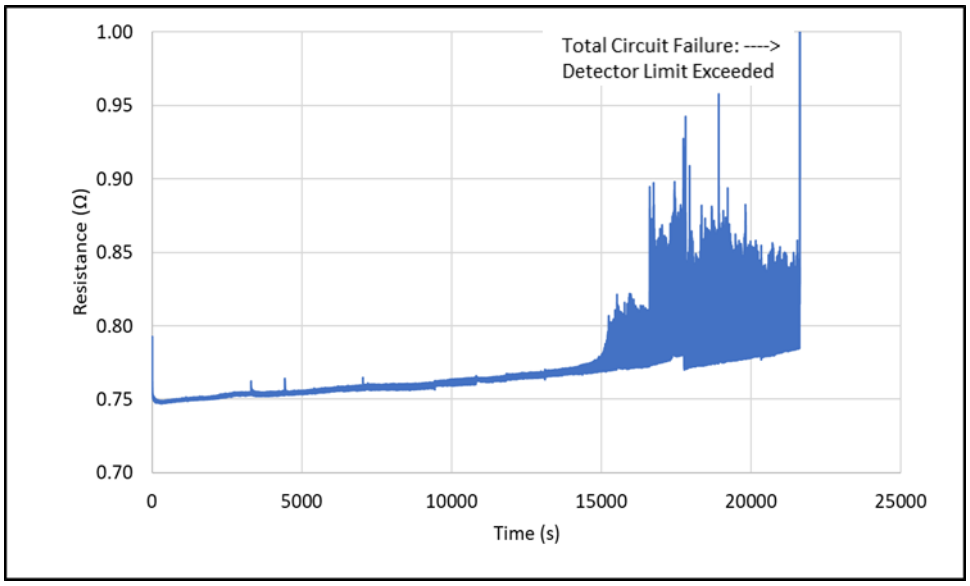

Figure 4-17: *in situ* resistance plot for 25 °C Test 1. Failure coincides with total circuit breakdown exceeding resistance detection limit (500 Ω).

As mentioned above, for tests conducted with TV2, the primary metric for determining failure was electrical performance monitoring through *in situ* resistance measurement. Resistance monitoring while the device is under test allows for qualitative and quantitative observations about the state of the device at any point during the test. The resistance curve for Test 1 at 25 °C is shown in Figure 4-17. In this case, a 30 % failure did not occur prior to a total circuit breakdown resulting in a resistance spike exceeding 500 Ω, thus this point at 21,621.4 cycles was recorded as the point of failure. However, examination of the figure shows extensive resistance changes prior to the point of failure with most major resistance events occurring after the 15,000 cycle mark. This sudden onset of significant resistance fluctuation is indicative of the onset of extensive cracking. From the 15,000 cycle mark onward, peaks and valleys indicate the opening and closing of cracks in response to changes in loading application direction.

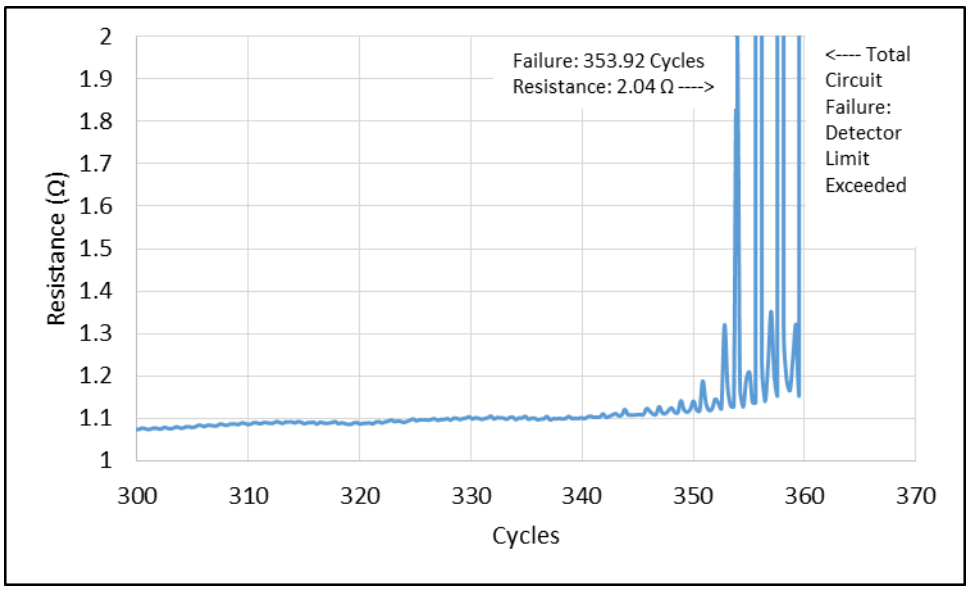

Figure 4-18: *in situ* resistance plot for 115 °C Test 1. Greater than 30% increase occurs at 353.92 cycles and prior to total circuit breakdown.

Figure 4-18 shows the resistance changes over the course of Test 1 at 115 °C where a 30% resistance increase did occur at 353.92 cycles and prior to total circuit failure at 359.2 cycles. Comparing these two resistance curves, it is clear that less cracking occurred prior to failure in the 115 °C test. As expected, the increased temperature had a severe negative effect on the total fatigue lifetime of the device, however, not through brittle cracking. The relative lack of cracking prior to failure for the high temperature device was attributed to the predominant failure modes experienced by devices tested at 115 °C; ductile necking and smearing. Consistent with theory and behaviors observed in the dummy die tests (see Figure 4-13), TV2 devices tested at the higher temperatures experienced more ductile failure due to increased viscoplastic behavior in response to the additional thermal energy. This behavior allowed the solder joints to deform and stretch in response to the stress, thus maintaining the electrical connection relatively unchanged until the damage accumulated reached a point where joint separation finally did occur. In depth analysis of the failure kinetics can reveal the mechanical principles behind these behaviors.

5. Failure Mechanics Analysis: Fatigue and Creep Induced Microstructural Changes

For any reliability analysis, the reasons "why" and "how" a device failed are just as important as the "when" at which failure occurred. By examining the microstructure and the fracture surfaces of the failed joints, a better understanding of the material's response to the applied stress can be developed. Additionally, microstructural changes under stress can further clarify why the dummy die units failed so much more quickly than the TV2 units. As discussed previously, the total solder volumes of all interconnects per device for the dummy die and TV2 were nearly identical (0.48 mm^3 and 0.46 mm^3 respectively). However, the solder volume of an individual interconnect of the dummy die was 0.037 mm^3, over three times the volume per joint for TV2 (0.011 mm^3). Li *et. al.* studied the effect of solder volume on shear fracture behavior on solder interconnects and found that increased joint volume led to more IMC growth at a constant growth rate via diffusion process where growth rate increased with increase solder volume [1]. The metallurgical reaction of the Cu/Sn/Cu diffusion couple which is present at the interface between the pad surface and the solder material was studied by Yin *et. al.*, who determined that two intermetallic phases result from this diffusion phenomenon [2]. The intermetallic species Cu_3Sn and Cu_6Sn_5 were reported with bulges of the single-crystalline Cu_6Sn_5 seen to form on the Cu_3Sn segments. Void formation was observed at these locations with subsequent void growth resulting in breakage. Thus, IMC growth accelerated cracking within the solder joints particularly near the interface is consistent with resistance spikes associated with the presence of cracks which are opening and closing under load observed in tests conducted at lower temperatures (see Figure 4-17). Thus, the increased volume per joint rendered the dummy die units more susceptible to cracking, negatively impacting their fatigue life which resulted in the much shorter cycles-to-failure reported as compared to the TV2 units.

The two primary failure mechanisms inherent in solder joint failure are fatigue and creep. Creep is expected to dominate deformation kinetics when the material is at temperatures above half its absolute melting point (T_m) while under load [3-4]. Below the 50% threshold, fatigue will play a more active role in the overall failure mechanism at work within the joints. Examination of Figures 4-12 and 4-16 reveals that of the temperatures tested, only 110 °C and 125 °C for SAC 305 and 100 °C, 110 °C, and 115 °C for Sn63/Pb37 exceeded this threshold. As a result, the primary failure kinetics for test temperatures below this threshold were dominated by fatigue failure. This is evidenced by examination of the fracture surfaces of the joints which were tested at the lower temperatures. Fatigue is the result of lowering material strength due to the repetitive mechanical loading of the joints and subsequently, the repetitive application of stress. Typically, fatigue failures occur when a small crack initiates at the location of maximum stress, which Figure 3-9 indicates is near the interface between the solder joint and the pad surface; right at the IMC layer. The crack then propagates over continued cyclic loading. Figure 3-5 clearly shows crack striations in the fracture surface of a eutectic joint tested at ambient temperature which are consistent with fatigue fracture; the striations indicating the position of the crack tip for each cycle.

Upon examination, the fracture surfaces observed at the lower testing temperatures are consistent with brittle failures due to the predominance of intergranular cracking often along a single plane [5]. Additionally, brittle cracking often occurs within thick sections of material, in this case the bulk solder spheres, and often requires very little plastic deformation. Figure 5-1 illustrates the intergranular cracking through a bulk Sn63/Pb37 solder sphere from a TV2 unit tested at 25 °C. The crack front extends in an almost perfectly planar fashion, indicating that the crack propagated along a specific crystallographic plane.

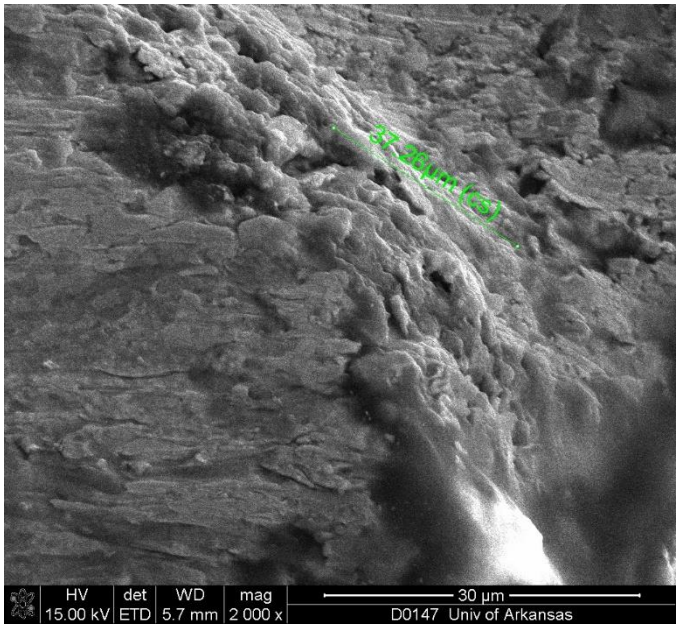

Figure 5-1: Intergranular cracking in a Sn63/Pb37 joint from a TV2 unit tested at 25 °C.

As the test temperature increases, approaching that 50% T_m, the fracture surfaces of failed joints begin to change, incorporating more aspects of ductile failure indicative of creep mechanics. Solders become more ductile with increasing temperature in conjunction with a decrease in ultimate strength. Due to the dual dependence of creep upon stress and temperature, this decrease in strength coupled with higher temperature leads to increased creep behavior with enhanced viscoplasticity leading to more extensive plastic deformation. At the intermediate temperature of 85 °C, the fracture surfaces of failed joints begin to exhibit some of the attributes of both brittle and ductile failure mechanisms. Figure 5-2 depicts a SAC305 solder joint from a dummy die sample tested at 85 °C. A large crack front through the bulk solder sphere can be seen which is associated with the final fracture. However, the presence of three large, elongated voids indicate microvoid formation which occurred as a result of transgranular fractures at the grain boundaries. Deformation slip is also indicated by the elongated nature of the voids. This slip occurs when the

resolved shear stresses, which are highest at a 45° angle to the applied load, reach the critical limit. More elongation of the voids indicates a higher degree of 45° slip.

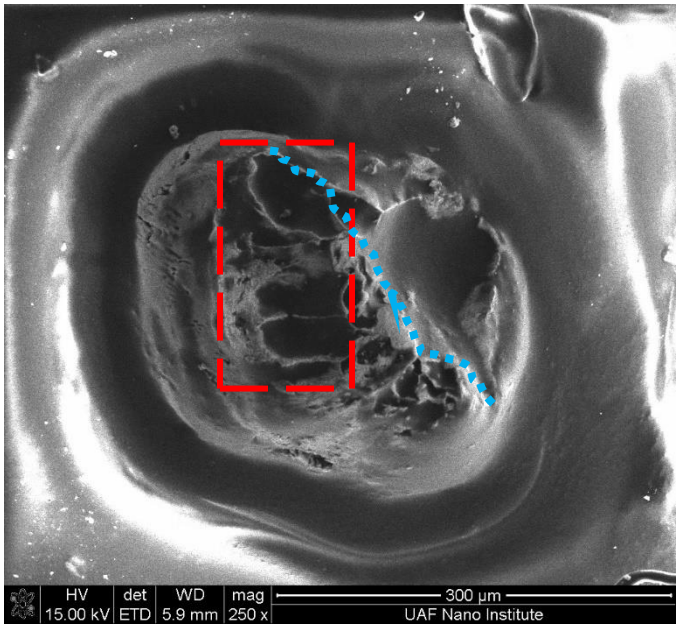

Figure 5-2: Top view SEM image of the fracture surface for a SAC305 joint which failed when tested at 85 °C. Elongated microvoids (dashed box) and a brittle crack front (dotted line) are visible indicating both ductile and brittle failure behavior.

At testing temperatures over the 50% T_m threshold, the higher temperatures enable dislocations within the solder to climb. Dislocation climb occurs when atoms move either to or from the dislocation line by diffusion, causing the dislocation to move in a direction perpendicular to the slip plane [5]. Climb controlled dislocation creep has been reported as the dominate failure kinetics mechanism for solder alloys due to the high dependence of secondary creep on stress and temperature [4]. Higher temperatures lead to increased creep strain rates which result in decreased time before stress rupture occurs. Thus, the devices tested at temperatures above the half melting point threshold fail after significantly shorter test periods than those tested at lower homologous temperatures. These failures are characterized by extensive plastic deformation and fracture surfaces which extended shear tips (see Figure 4-9a).

Often the entire fracture surface is the shear face leading to large numbers of elongated dimples present across the entire joint indicating voids which were stretched as a result of the shear load (see Figure 5-3). By examining the creep strain rate for a given device as cycling progressed, a better understanding of the failure kinetics can be obtained.

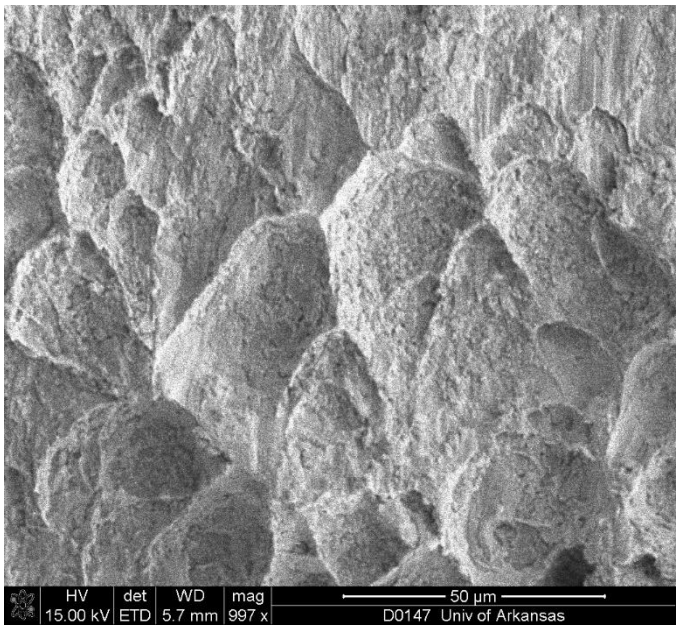

Figure 5-3: Elongated dimples in the fracture surface of a Sn63/Pb37 interconnect tested at 115 °C which are artifacts of microvoid formation within the material.

Using Darveaux's equations for inelastic strain discussed in section 3 (equations 3.3–3.6), creep strain and plastic strain were plotted as a function of cycles to determine the trend behavior for each type of strain as testing progressed for a given device. In all cases, across all temperatures, the creep strain is seen to increase as cycling continues indicating that dislocation climb and diffusion are occurring across an increasingly large volume of the material with an increasing rate. This is consistent with the "damage runaway" indicated by the ever larger drops in force reported for each subsequent cycle such as that seen in Figure 4-8. As the creep strain rate increases, the amount of deformation imparted with each cycle increases at an ever higher rate resulting in progressively lower force values prior to fracture. Example creep curves for each

tested temperature are shown below (see Figure 5-4(a-d)). From the graphs, it is clear that the rate of increase in creep strain with additional cycling become progressively higher with each increase in testing temperature.

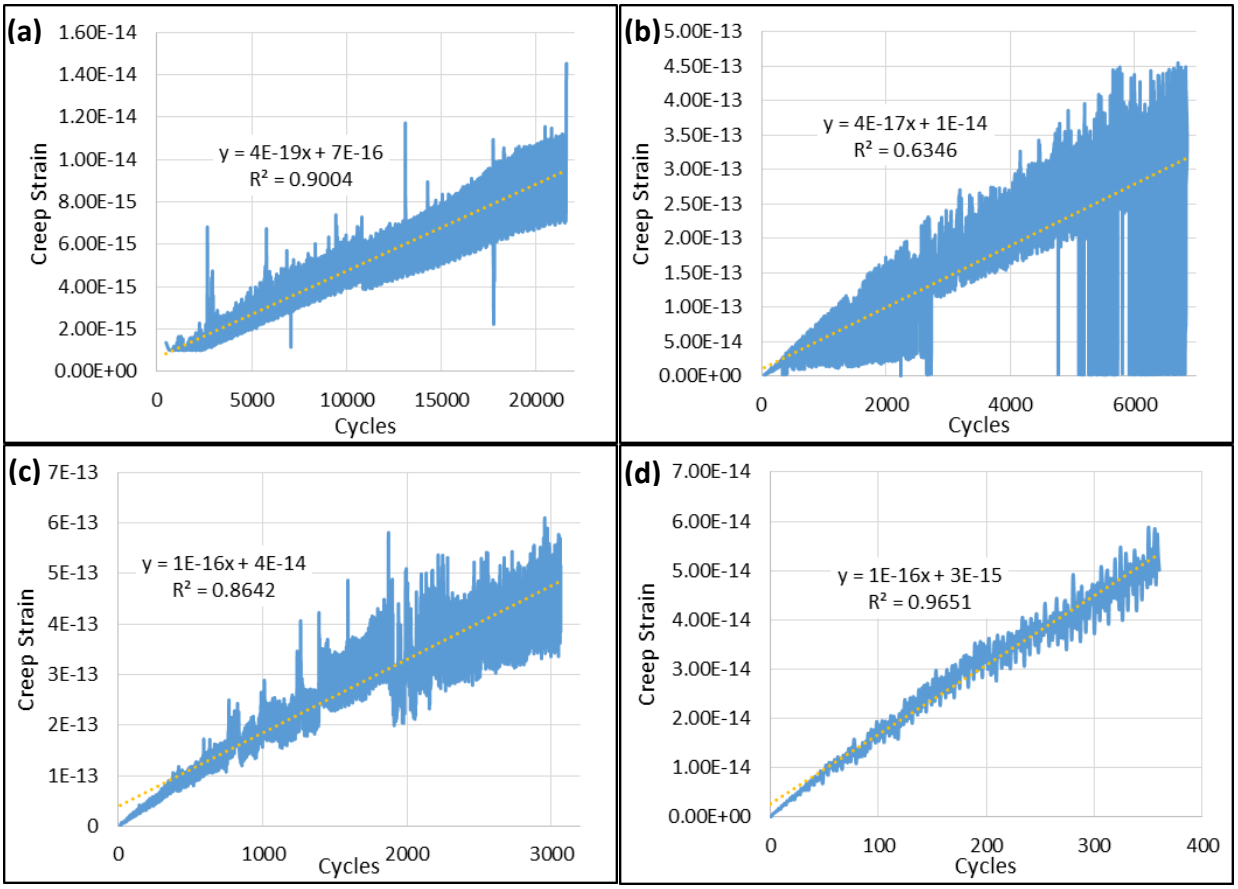

Figure 5-4: Creep strain curves for TV2 devices tested at (a) 25 °C (b) 85 °C (c) 100 °C and (d) 115 °C. The trendline denotes the rate of increase in creep strain as testing progressed, high slopes indicate high strain rate acceleration.

For the test temperatures above the 50% T_m threshold, the higher values for creep strain rate are the culprit behind the much shorter cycle times seen at these temperatures. Increased creep strain in the interconnects of these devices leads to a higher propensity for damage accumulation through dissociation climb, slip, and diffusion processes, ultimately curtailing the fatigue lifetimes of devices tested at high homologous temperatures. This relationship between temperature and creep strain rate explains the damage accumulation trends observed in Figures

4-12 and 4-16. The plastic work accumulation rate increases with increasing temperature due to increases in creep strain rate per cycle. Additionally, the manner in which a material accumulates damage, whether brittle or ductile failure, has been shown to depend on creep strain rate. With increased creep strain rate, the fracture surface will transition from predominately brittle failure modes to more ductile modes in response to the enhanced viscoplasticity. In the transient zone where operating temperature approaches, but does not exceed the 50% T_m threshold, the solder joints will endure both brittle and ductile fracture mechanics. Thus, a device operating through a temperature range in a real-world application will experience both types of fracture modes as well as both creep and fatigue. Understanding how this agglomeration of effects impacts the solder material will be critical to making accurate predictions about real-world fatigue lifetime.

5.1. References

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[3] K.-C. Wu and K.-N. Chiang, "Investigation of solder creep behavior on wafer level CSP under thermal cycling loading," in Proceedings of the International Conference on Electronics Packaging, 2014.

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6. Summary and Conclusions

A method was devised for evaluating the fatigue lifetime of flip-chip solder interconnects on a rapidly accelerated time scale through the use of applied shear stress. By utilizing the relationship between spring deflection and spring force, the amount of shear stress induced within the solder interconnects was quantified allowing for comprehensive examination of the failure mechanics and their effect on device reliability. *In situ* resistance testing enabled the evaluation of stress and damage accumulation on electrical performance for relevant device architectures. A method for calculating this damage accumulation in the form of work, was developed to enable accurate assessment of plastic deformation within the joints on a per cycle basis.

From the test results across two device architectures and two solder material sets, a pattern of total damage accumulation remaining constant with increasing temperature can be observed. While the values of accumulate plastic work were unique to the device type, for both test devices the amount of plastic work accumulated prior to failure by units of that type remained almost constant irrespective of temperature. In the case of the dummy die, this held true both the Sn63/Pb37 and SAC 305 material sets; devices with SAC 305 joints accumulated the same amount of damage as the devices with eutectic joints. Temperature still plays a key role in the ultimate strength (in this case shear strength specifically) of a device with increasing temperatures reducing the ultimate strength of a material. In these fatigue tests however, the shear stress applied to the tested units is not a significant enough percentage of the ultimate strength of the devices at the ambient or elevated conditions for this temperature dependency to greatly effect fatigue performance. In the case of the dummy die units with different materials, the cross-sectional area of material opposing the load was the same for all tested units. The

consistency of work values across material sets indicated that that particular amount of work was required to significantly disturb the geometry, reducing cross-sectional area and creating joint separations but this energy value was not dependent upon material. This reality means that the amount of work necessary to develop failure is primarily dependent upon interconnect geometry when the shear load is significantly below the ultimate shear strength of the material in question rather than on temperature or material. The same amount of work is thus necessary to generate a fixed amount of damage to a given geometry which is itself necessary to greatly degrade performance. It is hypothesized that there exists a stress threshold above which this no longer holds true as applied stress approaches ultimate strength. Above this threshold, work values required to generate cracking and joint separation will begin to vary from temperature to temperature, however, additional testing at higher stresses would be necessary to determine this threshold.

It is clear from the results that the rate of damage accumulation will become more severe as a device passes through that temperature during operation. This is where the effects of temperature are really felt, not in the total damage accumulated, but in how fast the device accumulates that damage. Temperature induced viscoplasticity results in drastic reductions in total CTF as increased ductility allows more plastic work to be done per cycle resulting in shorter fatigue lifetimes. It is apparent from Figure 4-12 that the way plastic work accumulation (read damage accumulation) changes with temperature will be dependent upon the material. In this study, SAC 305 was the stronger material, generally reporting longer fatigue lifetimes for a given temperature than the eutectic units. This strength was reflected in lower cyclic damage accumulation rates yielding a flatter rate of work accumulation rate change curve. Thus, a SAC 305 device will accumulate less damage as it swings through a power cycle in actual operation, ensuring greater reliability. However, the manner in which the solder joints accumulate damage

in this device will change as it achieves higher temperatures or cools down; brittle fracture at low temperatures and ductile fracture at high temperatures.

Creep and fatigue are responsible for the formation of these failures. Temperature and stress dependent dislocation creep is accelerated in solder interconnects which are stressed while above 50% of their absolute melting temperature. The increased rate of damage accumulation seen with increasing temperature is directly correlated to this enhanced creep behavior. Additionally, solder volume plays a role in the manner and amount of damage accumulated, with interconnects that have larger solder volumes experiencing failures more quickly than low volume solder interconnects. In industry applications, the two predominate failure mechanisms will occur within the same joints each time a device passes through the associated temperature, likely accelerating and enhancing each other with each passing cycle. Understanding this phenomena is necessary to make accurate predictions about solder fatigue behavior within a device operating across a given temperature range. Design and material selection are of greater importance to device reliability when assessing the fatigue life and mechanical reliability of flip-chip devices when operating sufficiently below the ultimate strength of the material than is the temperature range itself.

In situ resistance monitoring of devices undergoing fatigue testing can provide great insight into the failure behavior of the interconnects within the device. It can be used to assess both the onset of significant damage and the point at which that damage becomes unsustainable informing both design and material selection. In addition to the quantitative CTF data, resistance monitoring can provide qualitative information about the characteristics of the failure as it occurs. Examining Figures 4-17 and 4-18, the absence in the 115 °C test of multiple moderate intensity events associated with cracking like those seen in the 25 °C tests is symptomatic of the

increased viscoplasticity of solder material at elevated temperatures and the resultant ductility of the joints. In the case of elevated temperatures, the increased ductility allows deformation which maintains the electrical connection until damage approaches the plastic work threshold for that geometry and failure occurs.

Further research is required to answer the question; “How much acceleration is too much?”. Tuning acceleration to expected operating conditions would improve prediction accuracy and ensure more realistic failure characteristics. Furthermore, additional work is needed to develop translation factors between results obtained using this highly accelerated fatigue life testing method, and results obtained through the more traditional reliability testing methods to allow researchers to leverage the large body of knowledge pertaining to solder joint fatigue failure obtained previously. This knowledge could then be used to develop better interpretations of what CTF results obtained in this fashion mean for devices operating in real-world applications based on experience with other geometries and testing methods.

Appendix A

Load Calibration and Test Procedures

Load Calibration –

1. Install calibration cartridge into carrier baseplate. The proper cartridge to install should have an extrusion on the top side with the same dimensions as the die of the test device, to ensure relevance to the actual test procedure. The calibration cartridge is assumed (and verified) to exhibit minimal deflection under loading as compared with actual devices.
2. Mount the carrier baseplate to the stage by threading M4 screws into the center set of holes on the stage but do not tighten completely.
3. Enable force plotting from the software View tab drop-down menu, disable coefficient plotting. Enable the stage motor motion controller in the Help > Diagnostics menu. Use the manual control function to move the stage to the centerline of the total stage translation range to set the zero point for bi-directional translation.
4. Install the upper loading assembly to the tribometer arm by aligning the threaded hole in the top of the assembly with the mounting bracket on the arm. Insert the M12 screw through the bracket and tighten into the threads while ensuring that the assembly stays at a perfect 90° to the arm.
5. Slowly lower the arm down until the loading cap touches the die. Slide the carrier baseplate backward or forward until the loading cap seats over the die. Tighten the screws securing the baseplate to the stage. (For elevated tests, install thermocouple into carrier baseplate TC hole).
6. In the software, zero the load cell and select the New Test tab. Program the desired frequency and duration. For calibration checks, a duration of 10 minutes is sufficient.
7. Ensure that the equipment is installed properly (see Figure A1) and all screws are tight. Begin the test. Note the peak force values that occur for both the positive and negative translation directions. These values will be used to calculate the pre-test spring constants which are critical to accurately calculate plastic work during testing. Additionally, the peak values of test devices will be compared to those of the calibration to determine when force degradation begins.
8. Conduct this calibration both BEFORE and AFTER testing a device to check for spring degradation during the test.

Test Procedure –

9. After the calibration test has stopped, save the data to a .csv file. Raise the arm and remove the baseplate from the stage. Remove the calibration cartridge from the baseplate and install a test cartridge which contains the test unit.
10. Connect the wire leads from the device into the breadboard so that the four-point resistance probe leads are connected in series correctly. Note the starting resistance value of the device.
11. Repeat steps 2-6 above.
12. If conducting an elevated test, initiate heating using the oven. Ensure the device reaches desired steady-state temperature prior to starting test. Ensure that cooling air is flowing to the tribometer case using the air compressor.
13. To begin the test, it is necessary to enable data recording of both resistance, temperature and force simultaneously. To do this, input a recording time in the resistance/temperature program with a 15 second increase over the set test duration in the force recording software. Begin recording resistance prior to initializing the test. Begin the test, force data will begin recording. Note the peak force values during the first few cycles should be nearly identical to the peaks of the calibration. If not, something is wrong, stop the test and evaluate.
14. Monitor resistance during the test, when a resistance spike over 30% of the original value occurs, stop the test. Stop resistance/temperature recording.
15. Save the resistance and force data to respective .csv files. Raise the arm and remove the test sample (be sure to allow it to cool first).

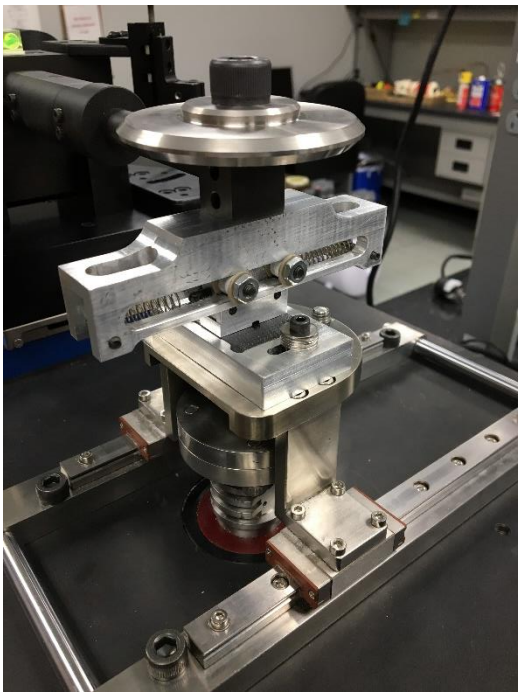

Figure A1: Fully assembled Test Apparatus 2 with Dummy Die calibration cartridge installed.

Appendix B

Tabulated Data for Elevated Tests

Table B1: Tabulated data for Dummy Die test units

85C				* # Loadings = 2*CTF	
Sample #	CTF	Effective Joints	Plastic Work (J)	*Work Accumulation Rate (J/	Volumetric Plastic Work (J/mm^3)
SAC 305 - 1	30.5	13	3.20E-01	5.25E-03	1.246152029
SAC 305 - 2	166	13	2.72E+00	8.20E-03	10.59045299
SAC 305 - 3	80.5	13	2.89E-01	1.80E-03	1.125425628
SAC 305 - 4	37.66	13	2.99E-01	3.97E-03	1.162738398
SAC 305 - 5	20.25	9	3.15E-01	7.77E-03	1.768437814
Sn63/Pb37 - 1	25.54	13	3.16E-01	6.20E-03	1.231751491
Sn63/Pb37 - 2	4	8	3.82E-01	4.77E-02	2.414810533
Sn63/Pb37 - 3	17.06	10	2.82E-01	8.26E-03	1.425671671
100C					
SAC 305 - 6	15.66	13	3.12E-01	9.98E-03	1.216115993
SAC 305 - 7	8	10	2.33E-01	1.46E-02	1.178461955
SAC 305 - 8	16	13	3.64E-01	1.14E-02	1.416100467
SAC 305 - 9	13.75	13	2.31E-01	8.41E-03	0.900201672
SAC 305 - 10	10.33	12	2.85E-01	1.38E-02	1.202209485
Sn63/Pb37 - 4	10.25	13	2.40E-01	1.17E-02	0.935942555
Sn63/Pb37 - 5	38	13	3.19E-01	4.19E-03	1.240961443
Sn63/Pb37 - 6	17	10	2.82E-01	8.29E-03	1.425671671
110C					
SAC 305 - 11	53.28	13	5.39E-01	5.06E-03	2.09969315
SAC 305 - 12	5.63	13	2.40E-01	2.13E-02	0.932892988
Sn63/Pb37 - 7	1.7	11.5	2.13E-01	6.26E-02	0.936053985
Sn63/Pb37 - 8	3.23	9	2.23E-01	3.46E-02	1.255774113
125C					
SAC 305 - 13	9.13	13	4.66E-01	2.55E-02	1.812480655
SAC 305 - 14	20.25	13	6.63E-01	1.64E-02	2.581418513
SAC 305 - 15	13	13	5.36E-01	2.06E-02	2.085945391
SAC 305 - 16	11.30	13	5.18E-01	2.29E-02	2.015428561

Table B2: Tabulated data for Test Vehicle 2 (TV2) devices.

25C				* # Loadings = 2*CTF	
Sample #	CTF	Effective Joints	Plastic Work (J)	*Work Accumulation Rate (J/# Loadings)	Plastic Work Density (J/mm^3)
Sn63/Pb37 - 2	21621.4	37	313.9211977	7.26E-03	18.56928362
Sn63/Pb37 - 1	33030	40	322.8948215	4.89E-03	17.66759029
Sn63/Pb37 - 3	30393.2	40	316.9839218	5.21E-03	17.34416809
Sn63/Pb37 - 4	29451	40	317.6177349	5.39E-03	17.37884796
85C					
Sn63/Pb37 - 12	5944	40	326.5450758	2.75E-02	17.86731848
Sn63/Pb37 - 13	4545.244	39	287.9568793	3.17E-02	16.15991537
Sn63/Pb37 - 14	6832.722	40	310.93758	2.28E-02	17.013335
Sn63/Pb37 - 15	93	--	410.522751	2.207111564	--
100C					
Sn63/Pb37 - 16	3065.012	40	317.7161585	5.18E-02	17.38423333
Sn63/Pb37 - 17	2277.455	36	314.9136624	6.91E-02	19.14543476
Sn63/Pb37 - 18	3351.517	40	339.0893174	5.06E-02	18.5536922
115C					
Sn63/Pb37 - 8	353.92	40	267.5928712	3.78E-01	14.64167555
Sn63/Pb37 - 9	326.48	40	320.7554739	4.91E-01	17.55053323
Sn63/Pb37 - 10	334.0613	40	279.2531476	4.18E-01	15.27968202

Appendix C

Test Vehicle Design and Fabrication

Dummy Die –

Based on an existing design, dummy die test units were created using Si die that had been metallized with layers of copper over titanium. Dry film solder mask was applied to the die and patterned using photolithography on a Karl Suss MA150 aligner. Sodium carbonate was used as the developer, opening the SMD pads to the specified 0.254 mm diameter. The solder paste was then applied using vacuum EFD and the 0.381 mm solder balls were applied individually by hand, and then the die was passed through a Sikama reflow oven with the reflow profile dependent upon solder material type. Finally, the die and FR4 substrate were flip-chip bonded using a Finetek Die Bonder. Figure C1 shows the interconnect pattern and a completely assembled device.

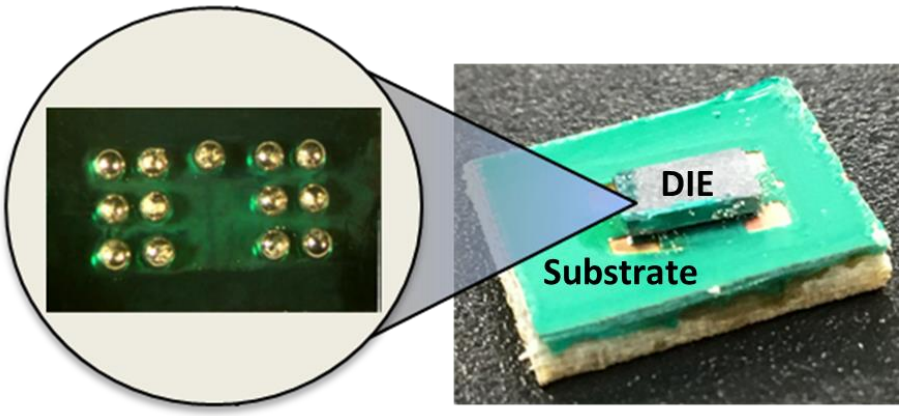

Figure C1: Test Vehicle Mk. I. "Dummy Die" of a POETS designed Flip-chip MOSFET developed by Sayan Seal and Dr. Alan Mantooth.

Used primarily to prove that the concept of the accelerated test would work, these devices were assembled as non-conductive and thus, not a capable of providing data on electrical performance degradation due to test conditions. These devices were assembled with three different solder material sets to evaluate the effects of material selection on reliability during testing. Materials used were: Sn95/Pb5 balls with Sn42/Bi57.6/Ag0.4 paste, SAC 305, and Sn63/Pb37. These units were tested at both ambient and elevated temperature.

Test Vehicle 2 (TV2) –

To fully utilize the *in situ* characterization capabilities of the test methodology, a fully-functional device which could be monitored for resistance changes was needed. A new test vehicle (TV2) was designed with these capabilities in mind. It was designed with an inner and outer ring of daisy-chains separated by a ring of platinum resistive heaters to allow on-device simulation of thermal loads. Additionally, temperature sensors were also included to accurately record interconnect temperature. However, these heaters and sensors were not used in the testing reported here. These devices were designed for 0.2032 mm solder balls with 0.154 mm SMD pad openings. The PCB, constructed of Roger's 4000 material, was designed with taps between each set of interconnects within a daisy-chain to allow for failure localization after testing through the use of continuity testing. Figure C2 illustrates the designs for both the die and substrate.

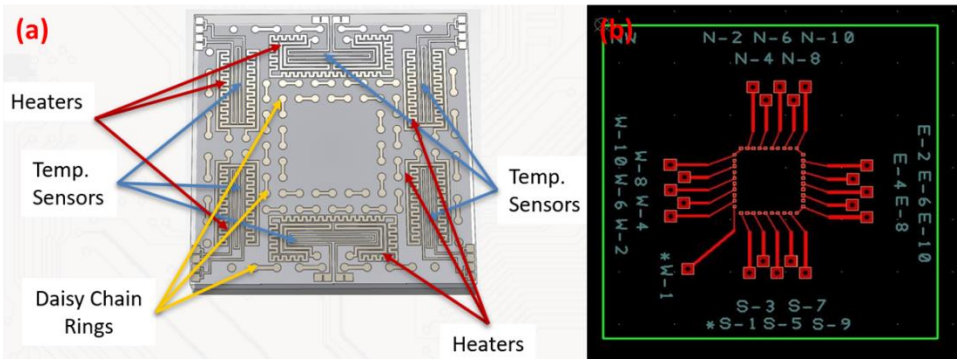

Figure C2: (a) Die side features (b) PCB design for test vehicle 2.

Fabrication of the PCB was contracted to a supplier while the die were fabricated in-house at the High Density Electronics Center at the University of Arkansas. A 4" Si Ti/Cu/Ti wafer was patterned using AZ4330 photoresist, exposed using a Karl Suss MA150 and etched using Ferric Chloride through a multi-step etching process until only Cu features remained on the surface of the wafer. Attempts to use the dry film solder mask used with the dummy die did not yield acceptable results, so the wafer was coated with SU-8 photoresist to act as the solder mask. The SU-8 was then patterned and exposed using the MA150 Aligner (see Figure C3). This wafer was then diced with an automated dicing saw and solder was applied, again using a manual method of solder ball placement. The ball bumping was done using a dental pick to place each ball in the SMD opening while the die was held fixed by a small fixture (see Figure C4). Finally, the bumped die was sent through the reflow oven and then flip-chip bonded using a Finetek Die Bonder.

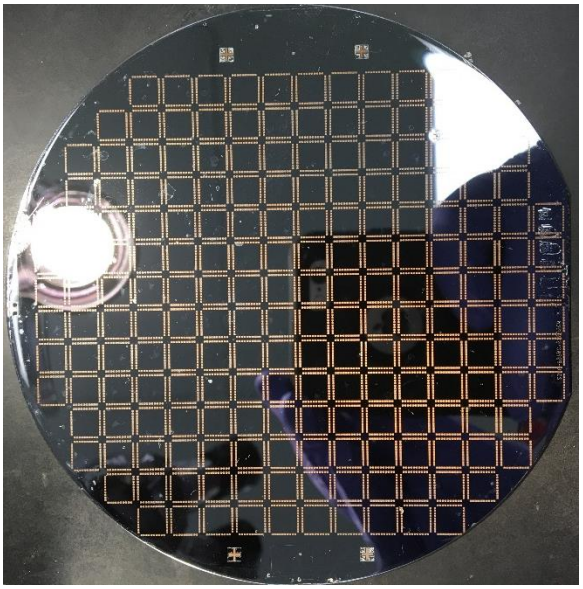

Figure C3: TV2 wafer after SU-8 deposition and patterning.

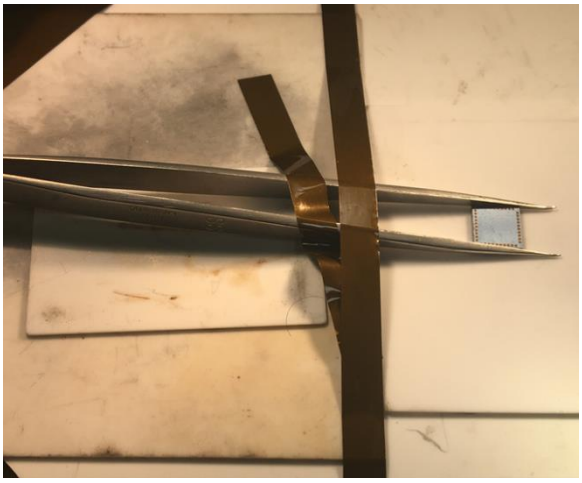

Figure C4: Temporary fixture for solder bumping. Ceramic tiles were used to allow the device to be slid out of the tweezers and placed directly in the reflow oven without being picked up.

The assembled test devices were then tested for continuity to ensure proper connections between interconnects. Once continuity was established, leads were soldered to the power input and output pads on the PCB which were connected to the four-point probe for resistance monitoring. These devices were tested until a 30% increase in resistance occurred, in some cases, this did not occur until the die was completely separated from the PCB. This behavior was confined to the elevated temperatures.

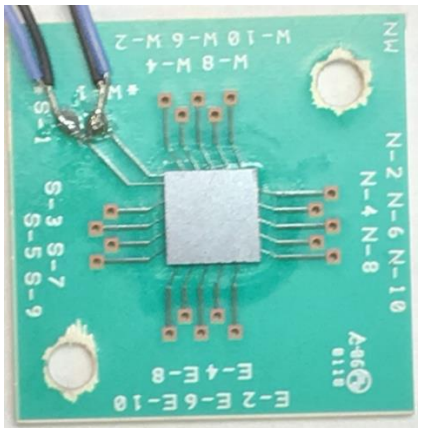

Figure C5: Assembled TV2 device with resistance monitoring leads.

Appendix D

Test Equipment Fabrication

The equipment used to adapt the tribometer for reliability testing was machined and fabricated out of Al7075 using manual and CNC manufacturing processes. Aluminum was used to reduce the total mass suspended by the arm to reduce wear on the tribometer. Relief cuts and "speed holes" were also integrated into the designs to further lighten the assembly. The parts were designed using SolidWorks software and SolidCAM was used to program the G code for CNC operations. Each part was machined from stock material which itself had to be designed and cut to specific dimensions. Careful consideration had to be given to the orientation of each part within the stock material with an eye toward practicality and reducing total milling time. Prior to beginning the milling process, the toolpaths (see Figure D1) for each milling operation were optimized to reduce total cutting time, wear on the cutter, and to ensure no unintended collisions or cuts were made. To achieve this optimization for each operation, feed rate (IPM), cutter speed (RPM), total number or cuts, total number of movements, and toolpath length all had to be correctly tuned.

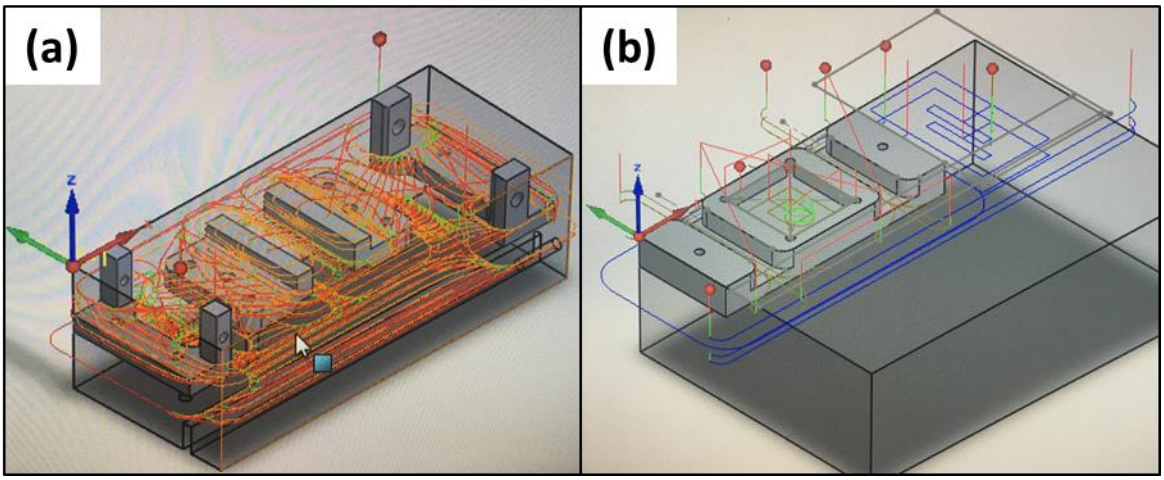

Figure D1: (a) Toolpaths for upper vise assembly components of Apparatus 1. (b) Toolpaths for machining of baseplate for Apparatus 1.

CNC milling operations were performed on a Lagunmatic 110 3-axis CNC mill with Mach3 software (see Figure D2). During the cutting operations, the feeds and speeds at which the operation took place were tightly controlled to reduce vibration, thus ensuring accuracy. Each

component was milled slightly oversize and then hand fitted to achieve very tight tolerances in the final assembly (see Figure D3).

Figure D2: CNC machining of arm attachment for Apparatus 1.

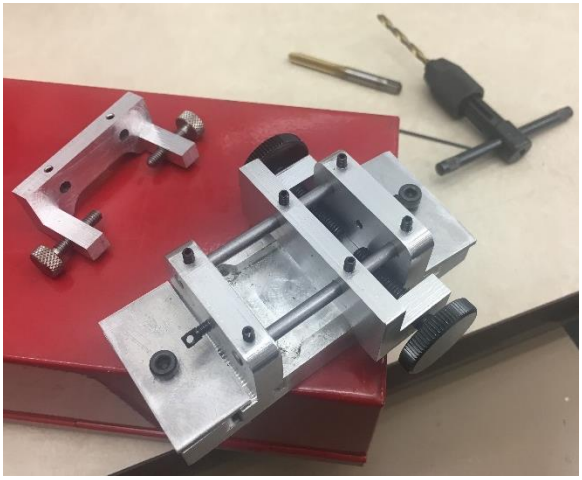

Figure D 3: Lower vise assembly on baseplate with large and small vises for Apparatus 1.