# ELECTRICAL, THERMAL, AND STRAIN-DEPENDENT CHARACTERIZATION OF TRANSITION METAL DICHALCOGENIDE-BASED DEVICES

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# Abstract

For over half a century, the performance of integrated electronics has significantly improved by reducing the dimensions of silicon-based logic and memory devices. However, as silicon scaling approaches its limits, researchers are investigating new materials for transistors, memory, and their three-dimensional (3D) integration on the same chip to enable higher density and better energy efficiency. Two-dimensional (2D) materials, in particular semiconducting transition metal dichalcogenides (TMDs), have demonstrated excellent electrical properties even in atomically thin films. In addition, these materials are promising for 3D architectures due to their ability to be integrated with various device structures at low temperatures. In this thesis, I will describe various experimental techniques to study TMD-based memory and transistors.

First, I study switching behavior in resistive memory devices based on molybdenum ditelluride ($MoTe_2$). I use scanning thermal microscopy (SThM) combined with electro-thermal simulations to investigate heating in the devices during operation. The SThM measurements, together with electrical measurements and transmission electron microscopy imaging, help uncover the switching mechanism in these devices and provide the first thermal insights into the operation of such TMD-based resistive memory.

Next, I demonstrate a simple pulsed voltage measurement technique to reduce hysteresis due to charge trapping in current-voltage measurements of $MoS_2$ transistors. I compare devices fabricated from exfoliated and synthetic $MoS_2$, with $SiO_2$ and $HfO_2$ gate insulators, using both DC and pulsed voltage measurements. The hysteresis is reduced by ~80% in all devices at modest voltage pulses of ~1 ms applied to the gate of the transistors, enabling accurate extractions of threshold voltage and field-effect mobility.

Finally, I explore the effects of strain on the optical and electrical properties of monolayer TMDs. First, photoluminescence measurements of $MoTe_2$ with tensile strain reveal narrowing of the optical band gap and indicate reduced exciton-phonon intervalley scattering. Next, I apply tensile strain to $MoS_2$ transistors and demonstrate an improvement in current and mobility by up to a factor of two. These results suggest that strain might play an important role for integrated 2D electronics, as it has for silicon. This work improves our understanding of TMD-based devices, which are promising for both logic and memory in next-generation electronics.

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# Chapter 1

# Introduction

## 1.1 Moore's Law and Transistor Scaling

In the last half-century, miniaturization of the components in integrated circuits has dramatically improved electronics. The basic building block of these circuits is the transistor, which was first created by William Shockley, John Bardeen, and Walter Brattain at Bell Labs in 1947 [1,2], and has evolved greatly since the first demonstration, a germanium point-contact transistor. The silicon metal oxide semiconductor field-effect transistor (MOSFET) (shown in Figure 1.1a) has been used in integrated circuits since the 1960s because of silicon's abundance, stable native oxide, ease of manufacturing, and good electrical performance [3]. In 1965, Gordon Moore observed that the number of transistors on integrated circuits had doubled approximately every two years and predicted that this trend would continue [3,4]. This exponential trend, illustrated in Figure 1.2, is known as Moore's Law and has been a driving force in the semiconductor industry for the last several decades. Moore's Law also translates to a reduction in cost over time and has led to rapid improvements in central processing units (CPUs) and memory chips.

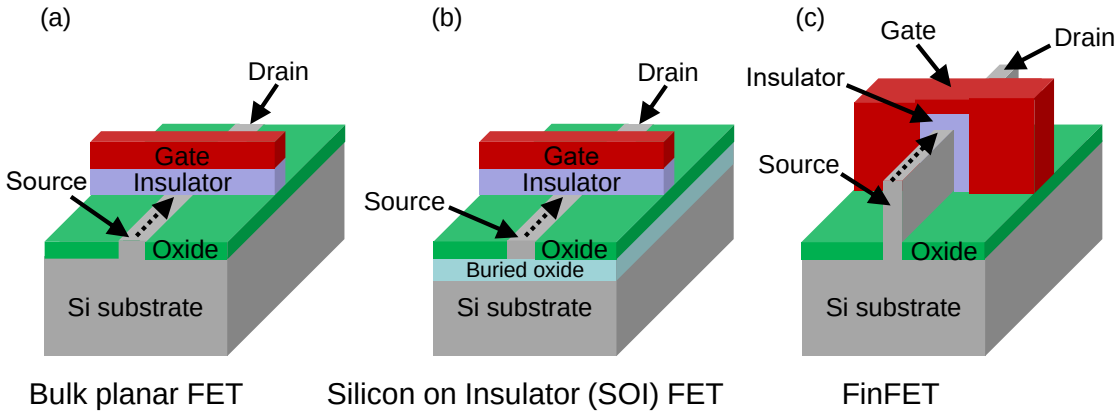


Figure 1.1: Schematic of different n-type transistors, including (a) bulk planar field-effect transistor (FET), (b) silicon on insulator (SOI) FET, and (c) tri-gate or FinFET. The dotted arrows show the direction of electron flow in the channel, from the source to the drain.

Miniaturization of transistors, or scaling, has enabled Moore's Law to continue steadily for the last 50 years. From the 1970s to the early 2000s, silicon transistors followed classical scaling, also known as Dennard scaling. The device dimensions (length $L$ and width $W$), voltage, current, and capacitance were scaled by $1/k$, while the doping concentration increased by a factor of $k$ and the power density and electric field remained constant [5]. Robert Dennard outlined these principles, which were then adopted by industry, in 1974 for scaling of devices to enable improvements in transistor density, switching speed, and power dissipation (shown in Figure 1.2). The scaling factor $k$ was ~1.4 for several decades, which roughly led to a doubling in transistor density every two years, nicely following Moore's Law [6].

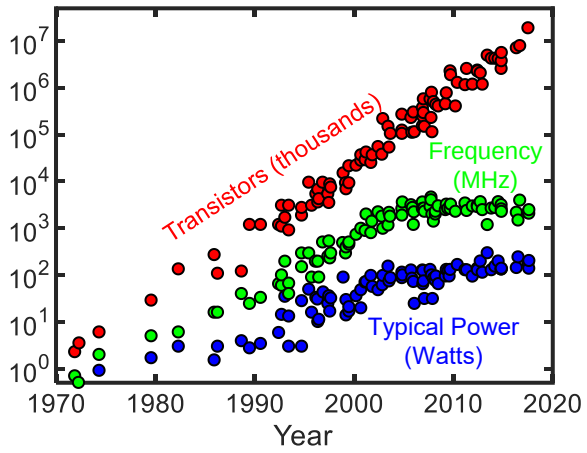


Figure 1.2: Plot of number of transistors per chip, clock frequency of transistors, and power dissipation of transistors from 1970 to 2018. Data collected by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, C. Batten, and K. Rupp (https://github.com/karlrupp/microprocessor-trend-data).

However, over time it became increasingly difficult for industry to continue scaling at this rate. Scaling the $SiO_2$ gate insulator down to ~1.2 nm resulted in increasing gate leakage current via direct tunneling through the insulator [6,7]. Increased doping density also caused decreased mobility from scattering and increased source and drain junction leakage from band-to-band tunneling [6]. To reduce this parasitic junction capacitance and leakage current and improve gate control, some companies moved from bulk planar silicon MOSFETs to silicon on insulator (SOI) FETs [7], as shown in Figure 1.1b. Another major

issue was that supply voltage ($V_{DD}$) scaling could not be maintained because it led to reduced threshold voltage ($V_T$) and increased off-state leakage current (and consequently standby power) [6,7]. Rather than continuing to scale as $1/k$, $V_{DD}$ instead scaled as $\epsilon/k$, as suggested in Dennard's subsequent papers on generalized scaling theory [8,9]. As a result, power density in chips increased from the late 1900s until the early 2000s (see Figure 1.2). The clock frequency, which had increased steadily from the 1970s, started to plateau in the early 2000s to prevent overheating of chips (see Figure 1.2) [10]. Instead of increasing clock frequency, industry increased the number of cores in processors to continue improving computing speeds [11].

As classical scaling slowed down due to the issues mentioned above, structural and materials innovations were made to continue improvements in performance, during an era known as equivalent scaling. In the early 2000s, the technology node became mainly a marketing term and no longer corresponded to the minimum feature size of the transistor. First introduced in Intel's 90 nm technology node, strain was applied to the channel of MOSFETs to increase drive current and mobility [12-14]. Uniaxial compressive tensile strain was applied by selective SiGe deposition in the source-drain regions for PMOS transistors, while uniaxial tensile strain was applied through a high stress nitride film deposited on top of the NMOS transistors, as shown in Figure 1.3a-b [13,14]. The use of strain in Intel's 90 nm and 65 nm nodes enabled significant performance benefits even though the gate oxide did not follow traditional scaling rules due to gate leakage issues [15,16]. However, performance improvements due to strain alone were not sufficient—beginning with Intel's 45 nm node, a hafnium-based high dielectric constant (high $\kappa$) gate dielectric replaced silicon dioxide to allow for a thicker dielectric but thinner equivalent oxide thickness (EOT = $t_{HfO2} \times \kappa_{SiO2}/\kappa_{HfO2}$) without increasing leakage current [17]. In addition, a metal gate replaced polysilicon to eliminate polysilicon depletion and improve drive current [16,17] (see Figure 1.3c for a cross-sectional image).

As transistors continued to scale down, many challenges arose that negatively affected the device performance, known as short channel effects (SCE). Channel length modulation, drain-induced barrier lower (DIBL), threshold voltage reduction ($V_T$ roll-off), and degraded subthreshold slope (SS) are examples of SCE that can become more prevalent at short channel lengths [18]. These effects occur when the source and drain depletion regions

constitute a significant portion of the channel length. To avoid some of these SCE, all device dimensions, voltages, and doping levels must be scaled by the same factor to maintain constant electric fields [18]. However, in practice this is very difficult because of the issues mentioned earlier including higher leakage current at lower $V_T$, defects and leakage issues with thin gate oxides, reduced mobility, and more parasitics with increased channel doping [18].

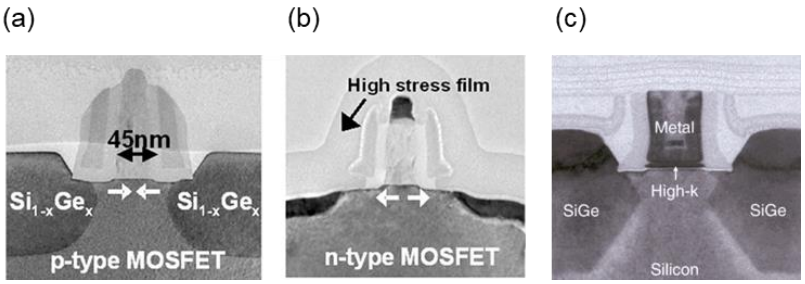


Figure 1.3: Transmission electron microscope (TEM) cross-sectional images of (a) a p-type Si MOSFET under compressive strain via implantation of $Si_{1-x}Ge_x$ in the source and drain regions and (b) a n-type Si MOSFET under tensile strain via deposition of a high stress film on top of the transistor [13]. (c) TEM cross-sectional image of a Si FET with a high-*k* dielectric and metal gate [17].

The scale length ($\Lambda$), which represents the decay length of the electric field lines from the source and drain regions into the channel region, is given by $\Lambda = \sqrt{\frac{\varepsilon_s}{\varepsilon_{ox}} t_s t_{ox}}$ for SOI transistors [19]. This equation contains the relative permittivity of the semiconductor and oxide ($\epsilon_s$ and $\epsilon_{ox}$, respectively) and the thicknesses of the semiconductor and oxide ($t_s$ and $t_{ox}$, respectively). The gate length is typically limited to a few times the scale length to minimize SCE [19,20]. To decrease the scale length, the semiconductor and oxide thicknesses must be reduced. In addition to SCE, another challenge for short channel transistors involves reducing the contact resistance ($R_C$), which is the resistance between the source (or drain) contact to the semiconductor channel. As the channel length decreases, $R_C$ becomes a larger percentage of the total device resistance ($R_{tot} = 2R_C + R_{ch}$) compared to the channel resistance ($R_{ch}$) and limits the on-state current [21].

Industry implemented a new device structure called the "FinFET" or "Tri-Gate transistor" in the 22 nm node to reduce SCE by improving electrostatic control, which also led to higher drive currents than planar FETs [16,22]. In the FinFET, shown in Figure 1.1c,

the channel protrudes from the bulk silicon and the gate surrounds the channel on three sides, enabling lateral scaling of the gate length and thus decreased device footprint and lower gate capacitance. FinFETs are fully depleted, which allows for steeper subthreshold slope and therefore lower leakage current [16,22]. In addition, they require lower channel doping, which leads to higher mobility and lower variability [16]. FinFETs have been used for the 22 nm, 14 nm, and 10 nm nodes, with reduction in fin height, fin width, and device pitch facilitating further scaling and performance improvements.

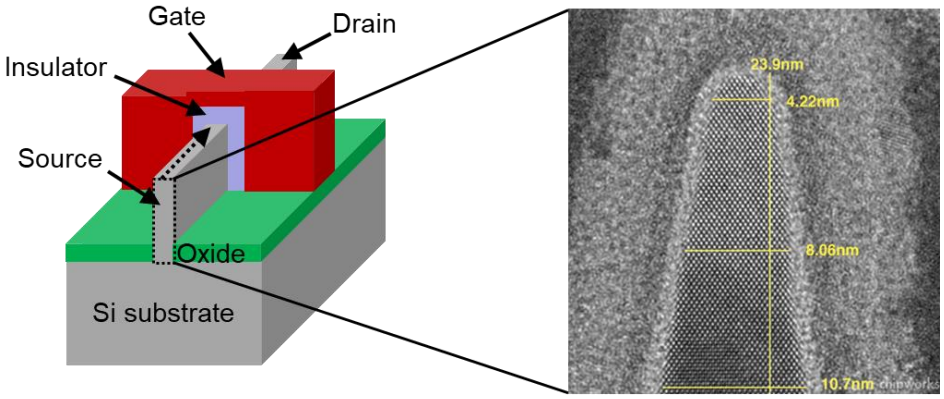


Figure 1.4: Schematic of a Si FinFET with a high resolution transmission electron microscope (TEM) cross-sectional image on the right showing individual silicon atoms. The fin width and fin height of a 14 nm node FinFET are illustrated (Source: Intel).

However, state-of-the-art FinFETs are beginning to face fundamental challenges with the Si channel. Figure 1.4 shows a transmission electron microscope (TEM) image of a 14 nm node Intel FinFET, with ~40 Si atoms visible along the width of the fin. Scaling of the fin width cannot continue indefinitely since it is approaching the atomic limit. Additionally, as the thickness of silicon decreases, it suffers from issues such as thickness variation and interface roughness [23-25]. These issues can lead to $V_T$ shift and mobility degradation due to scattering [23-25], which will be discussed later in this chapter. In future technology nodes, multi-gate transistors such as gate-all-around (GAA) nanowire or nanosheet transistors, similar to those shown in the schematic and TEM images in Figure 1.5a-b, will likely be implemented to allow for even better electrostatic control of the channel [16,20,26]. However, these transistors will still face challenges related to surface roughness and mobility degradation of ultrathin silicon.

One solution which will be explored in this thesis is to replace silicon with a novel channel material that will not suffer from these issues, even at the atomically thin limit. These materials, known as two-dimensional (2D) materials, are very promising and are being investigated for device applications in both academia and industry. However, aside from issues facing transistors for improved logic, there are other challenges at the architecture level that are inhibiting computing performance, including a performance gap between logic and memory. To address challenges related to improving architecture as well as increasing transistor density, three-dimensional (3D) heterogeneous integration of logic and memory will be discussed in the next section as a promising method to continue improving computing performance.

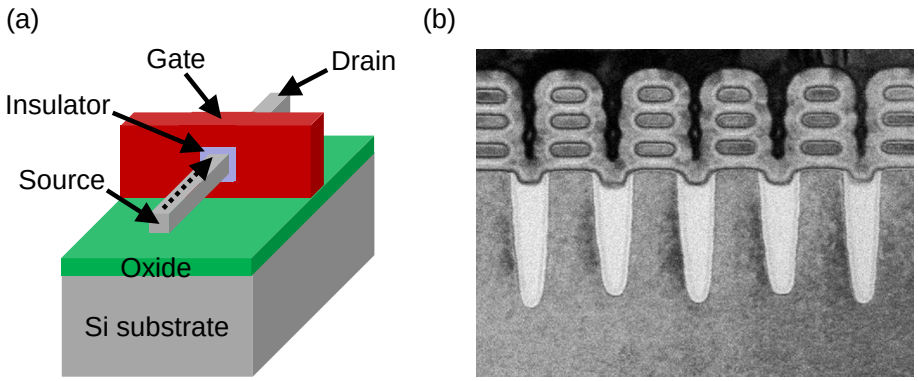


Figure 1.5: (a) Schematic of a n-type Si gate-all-around (GAA) transistor. The dotted arrow shows the direction of electron flow in the channel. (b) Cross-sectional TEM of a stacked nanosheet GAA transistor (Source: IBM).

## 1.2 Three-Dimensional (3D) Heterogeneous Integration of Logic and Memory

Computers currently use the von Neumann architecture, in which the central processing unit (CPU) and main memory are located on separate computer chips, as displayed in Figure 1.6a. The CPU includes the arithmetic logic unit (ALU), control units, registers, and cache memory for data that is frequently accessed, but the main and secondary memory are located off-chip [27]. The different types of memory form a hierarchy that have a tradeoff between access time and cost (see Figure 1.6b) [27,28]. The cache is typically made of static random access memory (SRAM), which is the fastest and most expensive memory. DRAM is used in the main memory and is also quite fast and expensive. SRAM and DRAM are volatile, meaning that they lose their information when the power is removed from the

cells. Secondary storage consists of Flash memory (either NAND or NOR) or hard disk drives (HDD) which are non-volatile, i.e. they keep their information when power is removed. Flash memory and HDD are much slower and cheaper than DRAM and SRAM.

Over time, the performance of processors has improved considerably in terms of speed and bandwidth as the technology has advanced and the number of cores has increased [27]. On the other hand, DRAM has not improved at the same rate and has much lower bandwidth and higher latency than processors, leading to an increasing performance gap between memory and processors over time [27]. Limited bus connections between the CPU and main memory also lead to delays in memory accesses for the processor. These issues have caused the so-called "memory wall," which refers to the issue of memory limiting processing performance [29-31]. Significant time and energy are wasted in accessing memory off-chip, rather than only in performing the computation [32].

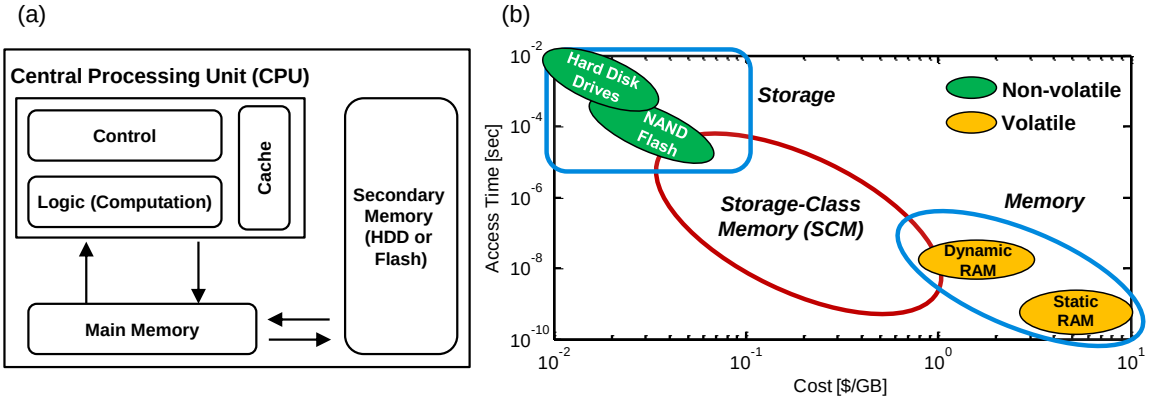


Figure 1.6: (a) Block diagram of von Neumann computer architecture. (b) Plot showing access time vs. cost of hard disk drives (HDD), NAND flash, dynamic random access memory (DRAM), and static random access memory (SRAM). An emerging class of memory called storage-class memory is also illustrated in the gap between storage and memory (adapted from [28]).

Researchers have developed ways to improve cache memory and DRAM speeds, but they are not sufficient to keep up with the need for accessing large amounts of data in the age of big data and artificial intelligence. One way to reduce the time and energy used by the processor to access data from memory is to integrate logic and memory onto the same chip. Many researchers have proposed three-dimensional (3D) heterogeneous integration of logic and memory by stacking alternating layers and using dense connections between them, as shown in Figure 1.7 [6,10,29,30,32]. However, microprocessors and memory used

in technology today may be difficult to integrate together on such a 3D chip because they are fabricated using different technologies [10,29,33]. In addition, silicon processing temperatures can exceed 1000 °C, and such temperatures used to fabricate devices on upper levels of a chip could damage underlying devices, Cu interconnects, and interlayer dielectrics. Consequently, researchers are studying new types of memory, known as emerging memory technologies, that can be fabricated on the same chip as microprocessors. Novel materials that can be integrated onto such chips at lower temperatures must be investigated for both transistors and memory. Two-dimensional materials are promising candidates for devices on these 3D chips and will be discussed in detail in Section 1.4.

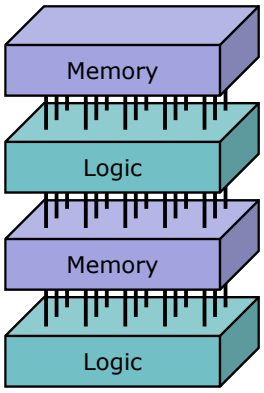


Figure 1.7: Schematic showing three-dimensional (3D) integration of logic and memory on the same chip, with dense connections between the layers.

## 1.3 Emerging Memory Technologies

As mentioned earlier, memory used in computers is either fast, expensive, and volatile (as in the case of memory like DRAM and SRAM) or slow, cheap, and non-volatile (as in the case of storage like HDD and Flash). There is a gap between these two categories of "memory" and "storage," and researchers are exploring new technologies that can fill this gap—known as "storage class memory" [28,34]. Non-volatility and high density are two main desired attributes for these technologies. Many candidates for storage class memory have emerged over the years, including spin transfer torque magnetic random access memory (STT-MRAM), phase change memory (PCM), resistive random access memory (RRAM), and conductive bridge random access memory (CBRAM).

STT-MRAM consists of an insulating material (tunnel barrier) sandwiched between two ferromagnetic layers, one that has a fixed magnetization (the reference layer) and one that has variable magnetization (the free layer) [34,35], as illustrated in Figure 1.8a. A current is used to switch the magnetization of the device between the high resistance state (HRS) and low resistance state (LRS) via the spin transfer torque effect, depending on whether the magnetization between the two layers is misaligned or aligned, respectively [34,35]. STT-MRAM has relatively low write energy, high speed, and high endurance but suffers from a low resistance ratio between the HRS and LRS [33-35].

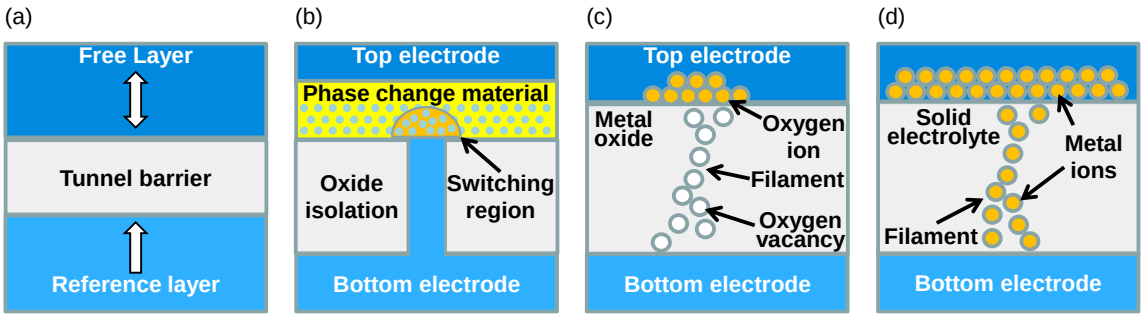


Figure 1.8: Schematic cross-sections of (a) spin transfer torque magnetic random access memory (STT-MRAM), (b) phase change memory (PCM), (c) resistive random access memory (RRAM), and (d) conductive bridge random access memory (CBRAM) (adapted from [33]).

A PCM cell includes a phase change material (typically germanium antimony telluride, or $Ge_2Sb_2Te_5$) between two electrodes, as depicted in Figure 1.8b. In PCM, the resistance of the phase change material switches between the HRS and LRS as the device transitions between amorphous and crystalline states, respectively [28,33,34]. An annealing step with a long voltage pulse heats the device above its crystallization temperature and "sets" the device to the LRS, while a melt-quench step with a short voltage pulse heats the device above the melting temperature and quenches it quickly, causing it to "reset" back to the HRS [28,33,34]. The back electrode is often confined in a "mushroom" cell configuration to heat (and thus switch) only a small region of the GST (see Figure 1.8b). PCM has a good HRS/LRS resistance ratio, high device density, and high speed, but requires a relatively large reset current because the device is switched via Joule heating [28,34].

RRAM and CBRAM both consist of insulating layers between two electrodes, as shown in Figure 1.8c-d. In RRAM, the insulating layer is typically a metal oxide like $HfO_2$

or $Al_2O_3$ and the electrodes are inert metals. In RRAM, under a high enough electric field, oxygen ions migrate between the electrodes and the oxygen vacancies form a conductive filament, in a process called "forming," which switches the device to the LRS [33,34,36]. The conductive filament can be broken and re-formed to switch the device between the HRS and LRS, respectively, by using an electric field of suitable polarity. For unipolar RRAM, the polarity of the electric field does not matter, but for bipolar RRAM the bias needed for breaking and re-forming the filament must be of opposite polarity. These processes are called the RESET and SET steps.

In CBRAM, the insulating layer is typically a solid electrolyte, one of the electrodes is an active metal like silver or copper, and the other electrode is an inert metal [33,34,36,37]. The active electrode oxidizes into metal ions, which then migrate under an electric field and form a conductive filament during "forming" [33,34,37]. The filament can similarly be broken and re-formed between the HRS and LRS with different polarity electric fields. RRAM and CBRAM have good endurance and speed, but one of the challenges they face is variability because the resistance as well as the number, size, and location of filaments can vary between cycles [33,34,36,37]. It is difficult to determine the number and location of filaments within a device without using a destructive method such as transmission electron microscopy (TEM). A technique called scanning thermal microscopy (SThM) will be discussed in Chapter 2 which can be used to determine size, location, and surface temperature of devices in steady state and during switching.

These emerging memory technologies, unlike traditional memory, have the advantage of being fabricated at low temperatures, allowing them to be monolithically integrated in a 3D chip [33]. They also consist of relatively thin layers that can be stacked on the chip without occupying a large volume. Thus, layers of logic and memory can be fabricated on the same chip with dense interlayer connections, facilitating fast movement of data between them. Such a 3D chip with layers of logic and memory will lead to much more compact and energy efficient computing. As mentioned earlier, 2D materials are very interesting for both transistors and memory due to their atomically thin nature and unique properties. The following section will focus on basic properties of 2D materials as well as their use in transistors, memory, and other devices.

## 1.4 Two-Dimensional (2D) Materials

Two-dimensional materials are layered materials with covalent bonds in plane and weak van der Waals forces out of plane. As illustrated in Figure 1.9, graphene, hexagonal boron nitride (h-BN), black phosphorus (BP), and transition metal dichalcogenides (TMDs) are some examples of 2D materials that span the spectrum from semi-metals to semiconductors to insulators with varying electrical, thermal, mechanical, and optical properties. Due to the inherent layered nature of these materials, their surfaces and interfaces are pristine and free from dangling bonds, unlike bulk materials like Si and Ge [38]. Graphene, arguably the most well-known and studied 2D material, is a single layer of graphite and was first isolated and electrically tested by Kostya Novosolov and Andre Geim in 2004 [39]. A semi-metal with zero band gap, graphene consists of a hexagonal sheet of carbon atoms and has high electrical and in-plane thermal conductivity and high mobility. However, due its lack of band gap, graphene transistors have a very low current on/off ratio (the ratio between the current in the on and off state of the transistor) of ~10 at room temperature, making them unattractive for digital electronic applications. However, after graphene became well-known, researchers began studying other 2D materials, and now over 1000 layered 2D materials have been theoretically predicted [40].

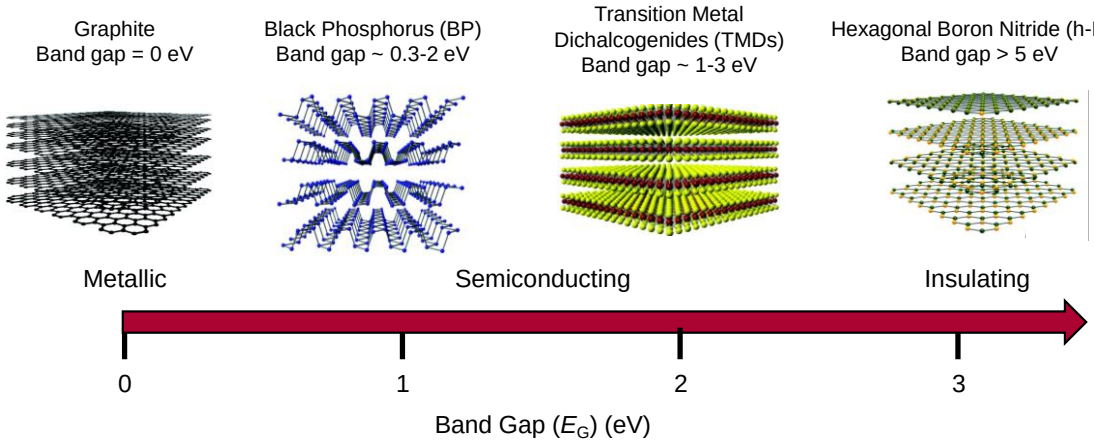


Figure 1.9: Schematic of various two-dimensional materials with different band gaps (adapted from [41]).

h-BN is a 2D insulator with band gap greater than 5 eV. It has a hexagonal structure like that of graphene and similarly has high thermal conductivity [42]. h-BN has gained attention for use as gate dielectrics, air stable encapsulation layers for other 2D materials,

heat spreading layers, and switching layers in RRAM [42-46]. BP is a 2D semiconductor with a puckered honeycomb structure and has band gaps ranging from 0.3-2 eV [47], depending on the layer thickness. It has higher mobility than many of the semiconducting 2D materials, making it useful for transistors and other device applications. However, BP is extremely air sensitive and must be encapsulated or handled in a glove box, limiting its widespread use in practical devices [48].

TMDs, another widely studied class of 2D materials, consist of transition metal atoms covalently bonded to chalcogen atoms (S, Se, and Te). The general formula is $MX_2$, where M is the transition metal and X is the chalcogen. The layered structure of the TMDs is illustrated in Figure 1.9, with the layer thickness typically around ~6-7 Å [49]. The most studied TMDs are the Mo- and W-based dichalcogenides in Group VI, and in particular molybdenum disulfide ($MoS_2$) has received the most attention because of its stability, mature growth, and good performance n-type transistors [50-56]. TMDs can exist in different phases, including the 2H or 3R semiconducting phases or the 1T or 1T' semi-metallic phases, where the 1T' phase is a distorted version of the 1T phase [57,58]. The H, R, and T refer to hexagonal, rhomboidal, and tetragonal symmetry, as shown in Figure 1.10. Most group VI TMDs naturally exist in the semiconducting 2H phase, except for $WTe_2$ which exists in the 1T' semi-metallic phase [57,58]. $MoTe_2$ has the lowest energy phase boundary between the 2H and 1T' phases, and studies have predicted that strain, gating, and temperature can induce a phase change between the 2H and 1T' phases [58-60].

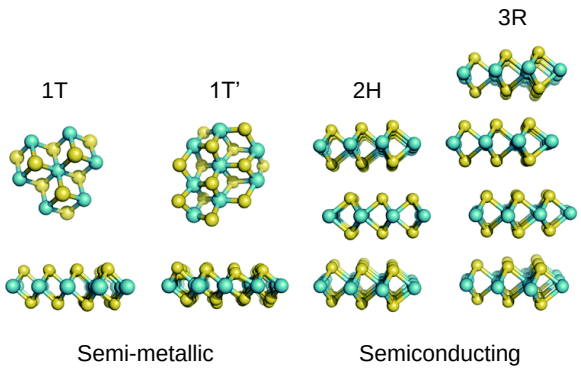


Figure 1.10: Different phases of the TMDs. The 1T and 1T' phases are semi-metallic, and the 2H and 3R phases are semiconducting (adapted from [57]).

The hexagonal Brillouin zone and electronic band structure of monolayer (1L) and bulk $MoS_2$ are shown in Figure 1.11. 1L TMDs have optical band gaps between 1-2 eV [53,61-63] and electronic band gaps between 1.3-2.5 eV, depending on the material, while multilayer TMDs have smaller band gaps [64-69]. The notable difference between the optical and electronic band gaps stems from the large binding energies of excitons (or bound electron-hole pairs) in 2D materials due to strong Coulomb interactions between electrons and holes [70]. Multilayered TMDs have indirect optical band gaps, while 1L TMDs have direct optical band gaps, making them interesting for optoelectronics.

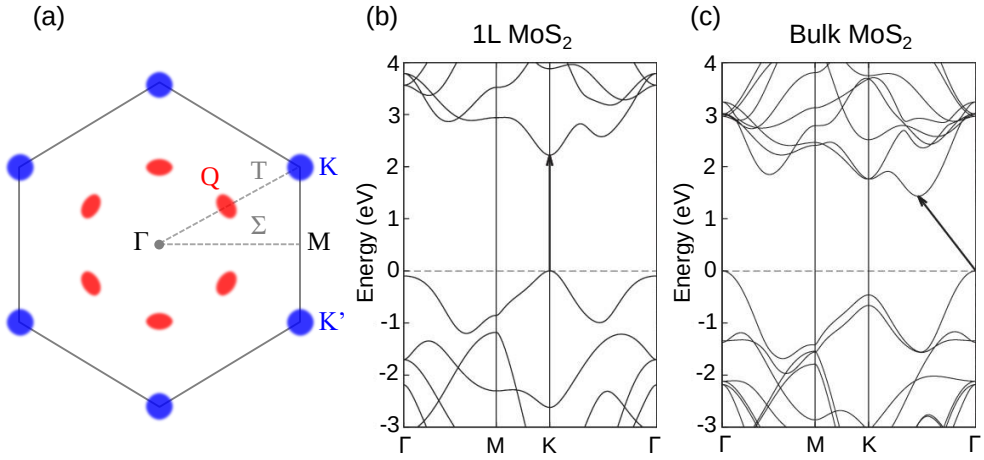


Figure 1.11: (a) Hexagonal Brillouin zone of 2H TMDs. Band structures of (b) 1L $MoS_2$ and (c) bulk $MoS_2$, calculated by density functional theory (DFT) (adapted from [71]).

TMDs can be grown using both top-down and bottom-up methods, including chemical vapor transport (CVT) [72], solid-source chemical vapor deposition (CVD) [53], or metal organic chemical vapor deposition (MOCVD) [73,74]. In CVT, stoichiometric $MX_2$ powder is placed in a quartz ampoule, vacuum sealed, and heated to ~800 °C. Iodine is typically used as the transport agent, and a temperature gradient of ~100 °C is maintained across the tube. After about two weeks, the growth yields bulk crystals which can then be exfoliated into thin layers using tape, either Scotch tape or low-residue thermal release tape (Nitto Denko RevAlpha series). Pieces of the bulk crystal are placed on the tape, which is gently pressed into a substrate, typically $SiO_2$/Si or PDMS, and then slowly peeled away. The exfoliation process results in a random distribution of flakes of different sizes and thicknesses. A weak $O_2$ plasma on the substrate before exfoliation can be used to make the surface hydrophilic and promote adhesion of thinner flakes. A microscope with an

objective of 50x-100x is then required to search for desired flakes. Figure 1.12a shows a picture of Scotch tape with bulk crystals of $MoTe_2$, and Figure 1.12b-c shows optical images of 1L and few-layer $MoTe_2$.

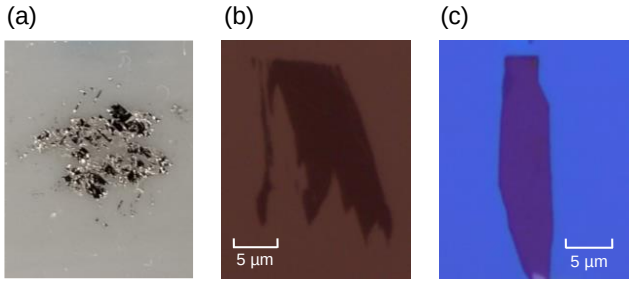


Figure 1.12: (a) Picture of bulk $MoTe_2$ crystals on a piece of Scotch tape. (b) 1L and (c) few-layer $MoTe_2$ exfoliated from the bulk crystals in (a).

In solid-source CVD, solid chalcogen (such as S or Se) and transition metal oxide (such as $MoO_3$ or $WO_3$) precursors are placed in a tube furnace (shown in Figure 1.13a). The substrate is treated with perylene-3,4,9,10 tetracarboxylic acid tetrapotassium salt (PTAS) as a seeding layer, and the furnace is held at atmospheric pressure and heated to 700 °C-850 °C to promote lateral epitaxial growth [53]. The growth conditions can be tailored to produce either continuous films or discrete triangles. Figure 1.13b-c shows an example of discrete triangles near the edge of the chip and a continuous film of 1L $MoS_2$ near the center of the chip. The films are mainly 1L with some bilayer (2L) islands in the center of the grains, which are hundreds of microns in size [53]. However, the 2L regions on the 1L films do not noticeably affect the electrical properties of devices [56]. TMDs can be grown on a variety of substrates, including quartz and various oxides like $SiO_2$, $Al_2O_3$, and $HfO_2$ on Si. One of the challenges with CVD growth of 2D materials is control and uniformity of growth over the entire sample. In addition, the temperature required for CVD growth must be lowered for these materials to be compatible with certain applications with low thermal budgets such as back-end-of-the-line (BEOL) transistors [32].

MOCVD uses gaseous precursors, allowing for more control over the growth than in solid-source CVD, and demonstrations of growth on a 4-inch wafer have been reported [74]. In addition, MOCVD can be performed at lower temperatures than solid-source CVD, [74] making this growth method promising for BEOL transistors. However, the MOCVD process is harder to implement and yields smaller grain sizes than CVD, leading to a trade-

off between well-controlled growth and good electrical performance of devices. In this thesis, only CVD-grown 1L films and thin layers exfoliated from CVT-grown bulk crystals are used in our devices.

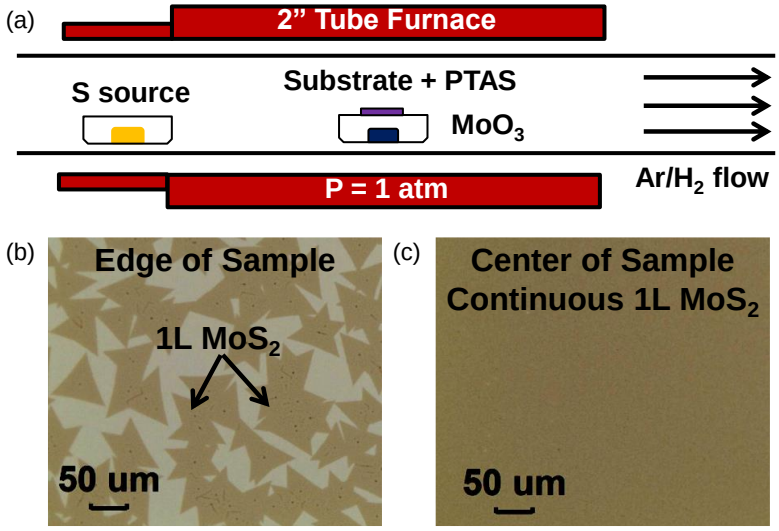


Figure 1.13: (a) Schematic of chemical vapor deposition (CVD) furnace used to grow 1L $MoS_2$. Optical image of (b) discrete triangles of 1L $MoS_2$ at the edge of the sample and (c) a continuous film of 1L $MoS_2$ near the center of the sample.

After either exfoliating TMD flakes from a bulk crystal onto a substrate or growing 1L films using CVD, the material can subsequently be transferred to another substrate or device structure, if needed. Transferring exfoliated flakes involves a dry transfer process using a polydimethylsiloxane (PDMS) stamp with precise alignment of flakes onto desired substrates, and will be discussed in detail in Chapters 2 and 4. 1L CVD-grown TMD films can be transferred using a polymer-assisted process, which will be discussed further in Chapter 5. The ability to transfer films of these materials to arbitrary substrates is useful for many device and materials applications such as 3D integration of logic and memory, as discussed in Chapter 1.4.

Raman and photoluminescence (PL) spectroscopy are optical techniques often used to characterize TMDs. The Raman set-up includes a monochromatic laser in the visible or infrared region of the electromagnetic spectrum to probe the vibrational modes of the material that are Raman-active. Most of the light incident on the material scatters elastically, but some amount of light scatters inelastically, and the Raman system measures this shift in energy arising from the vibrational (phonon) frequencies [75]. Raman can be

used to differentiate between materials and can give estimates of the amount of strain and doping in the material. Figure 1.14a-b shows the phonon dispersion of 1L $MoS_2$ [75] and a Raman spectrum of 1L $MoS_2$ measured with a 532 nm laser. The primary Raman-active modes for 1L $MoS_2$ are the E' and $A_1$' modes, which are known as $E_{2g}$ and $A_{1g}$ in the bulk, respectively [75]. As discussed in Chapter 5, the E' mode is sensitive to in-plane strain while the $A_1$' peak is sensitive to doping [75], so these measurements can provide much useful information about the material.

PL spectroscopy is another common technique to study 1L TMDs, because they are direct band gap materials and have very strong PL signals. Thus, PL is useful for distinguishing between 1L and thicker samples, which have much weaker PL response. PL also involves a monochromatic laser whose energy must be larger than the optical band gap of the material to excite electrons from the valence band to the conduction band. Figure 1.14c shows a typical PL spectrum of 1L $MoS_2$ measured with a 532 nm laser, with the main peak at ~1.8 eV arising from the direct band gap transition at the *K*-point (see Figure 1.11b), known as the A exciton [49,76]. The weaker peak at ~2 eV is due to a higher energy transition at the *K*-point, known as the B exciton, which results from spin-orbit band splitting in the valence band [49,76]. PL peaks, like Raman peaks, are also sensitive to strain and doping, making PL spectroscopy another valuable technique for characterization of TMDs [77-80].

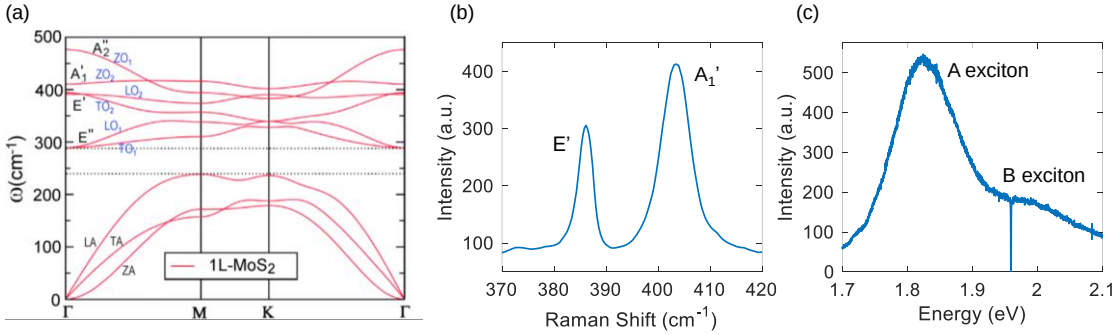


Figure 1.14: (a) Calculated phonon dispersion of 1L $MoS_2$ [75]. (b) Raman and (c) photoluminescence spectra of 1L $MoS_2$, both measured with a 532 nm laser.

The moderate band gaps, sub-1 nm thickness, and pristine interfaces of 1L group VI TMDs make them ideal for scaled transistors. 1L TMD transistors are expected to have better immunity to short channel effects based on scale length theory because of better

electrostatic control at ultrathin channel thicknesses [19,20]. Many experimental studies have demonstrated current-voltage (*I*-*V*) characteristics of TMD-based transistors with carrier mobilities in the range of 10-100 $cm^2/V/s$, depending on the material, semiconductor thickness, and carrier density [38,51,56,81,82]. These materials have reasonable mobilities even in the atomically thin limit, unlike bulk materials. Figure 1.15 shows significant degradation in mobility for SOI and germanium on insulator (GOI) transistors below channel thicknesses of ~3 nm, in part due to surface roughness effects [23-25,83], while TMDs maintain mobilities around 10-100 $cm^2V^{-1}s^{-1}$ and graphene has even higher mobility for a sub-1 nm film. Nevertheless, researchers in this field are investigating ways to improve mobility, including by channel doping [84-86] and by applying strain [87-89], which is a major focus of this thesis and will be discussed in Chapters 4-5. Even if the mobility can be improved, however, extracting an accurate value for mobility can be difficult due to hysteresis in the *I*-*V* characteristics resulting from charge trapping in the device. A simple method involving pulsed electrical measurements to reduce hysteresis and extract the "true" mobility of $MoS_2$ transistors will be introduced in Chapter 3.

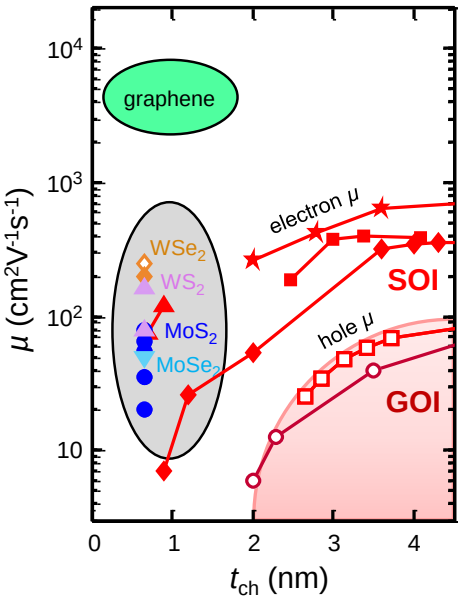


Figure 1.15: Experimental mobility ($\mu_{FE}$) vs. channel thickness ($t_{ch}$) for various 2D materials, silicon on insulator (SOI), and germanium on insulator (GOI), with all channels in contact with $SiO_2$ and measured at room temperature (adapted from [51]). Filled symbols refer to electron mobility and hollow symbols refer to hole mobility. Different symbols refer to different studies.

TMD transistors have also achieved high on-state currents and low off-state currents. On-state currents greater than 500 μA/μm have been measured for double-gate short-channel $MoS_2$ transistors [90] and by using channel doping techniques which utilize charge transfer from sub-stoichiometric oxides [54,84]. Due to the relatively large band gaps and effective mass ($m^* \sim 0.45m_e$ for 1L $MoS_2$ [91]) of 1L TMDs, transistors based on these materials have achieved off-state currents below 1 fA/μm [90,92,93], which is much lower than those of Si FETs [92]. Low off-state currents are promising for low-power devices or for access transistors in DRAM because they enable reduced power consumption [90,92,93].

Low semiconductor-to-metal contact resistance ($R_C$) is necessary to achieve efficient current injection from the metal to the semiconductor, and this has been a major challenge for 2D semiconductors. Many research efforts on reducing contact resistance have led to contact resistance less than 1 kΩ·μm using ultra-high vacuum (UHV) metal contact deposition [51,55], doping of the 2D semiconductor [54,84], or phase changing the semiconductor to a semi-metal underneath the contacts [94]. However, further reduction in contact resistance is necessary for high performance devices and continues to be an active area of research within the field of TMD electronics.

In addition to transistors, 2D materials have recently been researched for memory, including as heat confinement layers in PCM [95,96] or as switching layers in RRAM [44,97-101]. The low out-of-plane thermal conductivity of many 2D materials allows them to act as effective thermal insulation [102], resulting in lower switching currents in PCM [95,96]. Using ultrathin TMDs rather than conventional bulk metal oxides for RRAM could enable lower switching voltages while maintaining high on/off resistance ratios [98]. 2D materials are also promising for 3D RRAM, due to their atomically thin nature, permitting ultrathin and scaled devices with relatively easy stacking of layers. They also have the capability to be integrated into such 3D RRAM at low temperatures, as discussed earlier. Resistive memory based on 2D materials will be demonstrated in Chapter 2.

Apart from conventional electronics on rigid substrates, TMDs have also gained interest for flexible electronics applications such as flexible sensors, displays, and wearable devices. They are encouraging for these applications due to their good electrical performance, atomically thin nature, flexibility, and ability to withstand large amounts of

strain. TMDs like $MoS_2$ have been shown to withstand up to ~11% strain [103], whereas bulk materials like Si can only withstand up to ~1.5% strain before rupture [104]. Organic molecules, amorphous oxides and semiconductors, and semiconducting polymers have been used for flexible electronic devices, but they often suffer from low mobility and drive current [105]. Experimental studies have demonstrated that TMDs are piezoresistive, which means that their resistance changes with strain, making them useful for strain sensing applications [89,106-110]. TMDs for strain sensing applications will be explored in Chapter 5.

Many applications, including transistors, memory, and flexible electronics, for TMDs have thus far been discussed. However, these materials are still relatively new to the field of nanoelectronics and are still in the research phase. Many aspects of the fundamental properties and physics need to be further explored, and device characteristics such as drive current, mobility, and contact resistance for transistors need to be improved. In addition, TMDs for memory have been demonstrated, but the switching mechanism is still not well understood. In this thesis, we perform many characterization techniques to improve our understanding of TMD-based devices. We perform electrical measurements, including pulsed and temperature-dependent measurements, to extract important electrical properties like threshold voltage and mobility of transistors and switching voltages of memory. We use thermal measurements and modeling of memory to study heating of devices during operation. Optical measurements like Raman and photoluminescence spectroscopy shed light on vibrational, optical, and electrical properties and provide insight into the phonon dispersion and band structure of TMDs. We also perform strain-dependent measurements to tune the properties of materials and devices.

## 1.5 Thesis Organization

This work primarily focuses on characterization of TMD-based devices using many different experimental techniques. Chapter 1 of this thesis provided a brief history of semiconductor device scaling, a discussion of three-dimensional integration of logic and memory, and an introduction to 2D materials, including their use in transistors, memory, and flexible electronics applications. In Chapter 2, we demonstrate resistive memory based on molybdenum ditelluride ($MoTe_2$) with gold electrodes. We show bipolar switching of

devices with different thicknesses and electrode areas. Scanning thermal microscopy (SThM), an atomic force microscope technique used to investigate heating in the devices during operation, reveals evidence of localized switching at conductive "plugs" formed during switching. We compare our experimental data to electro-thermal simulations to gain insight into the size and temperature of the switching regions. Transmission electron microscopy (TEM) images indicate that the switching results in Au migration between electrodes, which is a thermally-activated process. However, the initial "forming" mechanism may be caused by defect generation or Te migration within the $MoTe_2$.

Chapter 3 introduces a simple pulsed measurement technique to reduce hysteresis due to charge trapping in current-voltage measurements of $MoS_2$ transistors, facilitating more accurate characterization. We study hysteresis and charge trapping in both exfoliated and CVD-grown $MoS_2$ transistors with $SiO_2$ and $HfO_2$ gate insulators, using DC and pulsed voltage measurements at different temperatures. We demonstrate a reduction in hysteresis by ~80% with ~1 ms pulse widths in all devices, and applying shorter pulse widths (~1 μs) eliminates up to 99% of hysteresis for some devices. Our technique enables unique values of field-effect mobility ($\mu_{FE}$) and threshold voltage ($V_T$), regardless of voltage sweep direction. We also use a tunneling front model to estimate the depths of charge traps in our gate dielectrics.

In Chapter 4, we study ultrathin $Mo_{0.91}W_{0.09}Te_2$, a semiconducting alloy of $MoTe_2$, via Raman, photoluminescence (PL), and absorption spectroscopy measurements. We find that $Mo_{0.91}W_{0.09}Te_2$ has similar optical spectra to $MoTe_2$ with shifts in some of the peaks due to the addition of W atoms. We apply tensile strain for the first time to 1L $MoTe_2$ and 1L $Mo_{0.91}W_{0.09}Te_2$ to tune the band structures of these materials, and we find that their optical band gaps decrease by ~70 meV at ~2.3% tensile strain. As the strain increases, the linewidths of the PL and absorption peaks decrease, which we attribute to decreased exciton-phonon intervalley scattering.

The strain-dependent measurements from Chapter 4 motivated us to study electrical measurements of 2D materials with strain, because weaker intervalley scattering of electrons and phonons can lead to higher carrier mobility. Thus, Chapter 5 focuses on optical and electrical measurements of $MoS_2$ with strain. Raman and PL spectroscopy are used to confirm the amount of strain applied to the $MoS_2$ and measure the decrease in the

optical band gap. We demonstrate an improvement in drive current and field-effect mobility of $MoS_2$ transistors using uniaxial tensile strain. The electrical properties continuously improve with increasing levels of strain, and the devices return to their initial state upon release of strain. We also show a gate voltage-dependent gauge factor up to ~200 for 1L $MoS_2$, which is among the highest values reported for 1L $MoS_2$ devices. These results demonstrate the importance of strain engineering for 2D materials and suggest that these materials are useful for applications in strain sensing.

Chapter 6 summarizes the conclusions of this work and proposes future directions for the work presented in this thesis. We also provide an outlook on 2D materials for various device applications and conclude that these materials are very promising candidates for scaled electronic devices.

# Chapter 2

# $MoTe_2$-Based Resistive Memory

## 2.1 Introduction

Two-dimensional (2D) materials have gained much interest in the last decade for scaled electronics, with most studies focusing on transistors based on these materials. More recently, they have been incorporated into memory devices [111], either as heat confinement layers in phase change memory (PCM) [95,96], or as switching layers in resistive memory devices [44,97-101]. These materials are promising for 3D integration of memory with logic, due to their atomically thin nature and ability to be integrated with other substrates or devices at low temperatures.

Transition metal dichalcogenides (TMDs) have also been suggested for phase engineering applications because many Group VI TMDs can exist in both semiconducting and metallic phases [49,58]. Molybdenum ditelluride ($MoTe_2$) is particularly interesting for these applications because it was predicted to have the lowest-energy phase boundary between the semiconducting and metallic phases [58]. While some studies have demonstrated switching in TMD-based memory, the switching mechanism remains unclear and could result from a localized semiconductor-to-metallic phase change, ion migration causing (reversible) conductive regions, or interactions with the electrodes [97,98,100,101].

The switching mechanism can either be thermal in nature like in PCM or have a thermally-activated component like in resistive random access memory (RRAM), yet such aspects have not been investigated to date in TMD-based memory devices. Understanding the switching mechanism and role of temperature is particularly important for 3D memory chips because high temperatures reached during operation in one memory cell can

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This chapter was adapted, with permission, from I. M. Datye, M. Muñoz Rojo, E. Yalon, S. Deshmukh, M. J. Mleczko, E. Pop, "Localized Heating and Switching in $MoTe_2$-Based Resistive Memory Devices," *Nano Letters*, vol. 20, pp. 1461-1467, 2020. Copyright 2020 American Chemical Society.

significantly change the temperature and thus the performance of a neighboring cell, known as thermal crosstalk [112]. In addition, resistive memories such as RRAM and CBRAM have gained much interest as emerging non-volatile memories but face issues with variability due to the random nature of filament formation. Techniques to study the location and heating of individual filaments in devices are often destructive or unreliable [113-115], so new techniques are needed to better understand these emerging memories.

In this work, we use scanning thermal microscopy (SThM) to examine the thermal origins of switching behavior in $MoTe_2$-based resistive memory devices with varying $MoTe_2$ thickness and electrode area [116]. We obtain spatial temperature maps of these devices under electrical bias and find evidence of localized heating due to conductive plugs which form during switching. Because the SThM measurements only probe the temperature at the surface of the devices, we correlate our measurements to electro-thermal simulations to obtain insight into the size and temperature of the conductive region *within* the $MoTe_2$. We also perform cross-sectional transmission electron microscopy (TEM) of memory devices after switching and find that the conductive plugs likely result from contact metal (here Au) migration between the top and bottom electrodes. However, control experiments on $MoTe_2$ devices with graphite electrodes also show forming, suggesting this is initially triggered by Te or defect migration, rather than only by Au conductive bridge formation.

## 2.2 Sample Preparation

### 2.2.1 Device Fabrication

First, $MoTe_2$ is grown by chemical vapor transport (CVT), which yields bulk crystals [72,117]. $MoTe_2$ powder (ESPI Metals $MoTe_2$, 99.9%) is sealed in a quartz ampoule with iodine flux (Alfa Aesar, 99.99+%) at 5 mg/cm$^3$. The temperature of the central hot zone of the tube is maintained at 800 °C with a 100 °C thermal gradient during 14 days of growth. We then exfoliate thin layers (~10-55 nm thick) of $MoTe_2$ onto $SiO_2$/Si substrates.

Figure 2.1a shows a side-view schematic of our $MoTe_2$ devices, depicting the layered $MoTe_2$ between Au electrodes. The Au bottom electrode (BE) is patterned by electron beam (e-beam) lithography and deposited by e-beam evaporation with a thickness of 45 nm. After exfoliation, the $MoTe_2$ is transferred onto the Au BEs by a transfer process

described in Section 2.2.2. E-beam evaporated $SiO_2$ (~65 nm) is deposited on top of the $MoTe_2$ to electrically isolate the bottom and top electrodes. The top electrode (TE) is patterned and deposited the same way as the BE and has a thickness of ~80 nm. Finally, we deposit ~10 nm $Al_2O_3$ by atomic layer deposition (ALD) as a protective capping layer [118] above the TE, as shown in Figure 2.1a. The exfoliation, transfer, metal lift-off, and ALD steps are all performed in a $N_2$ glove box with <3 ppm $O_2$ and <1 ppm $H_2O$ to prevent surface oxidation of the $MoTe_2$. Figure 2.1b displays optical images of two $MoTe_2$ devices (Device 1 and Device 2). Device 1 has Au TE area of 4.5 × 4.5 $\mu m^2$ and $MoTe_2$ thickness $t_{MoTe2}$ ~ 30 nm, while Device 2 has Au TE area of 0.7 × 0.4 $\mu m^2$ and $t_{MoTe2}$ ~ 55 nm.

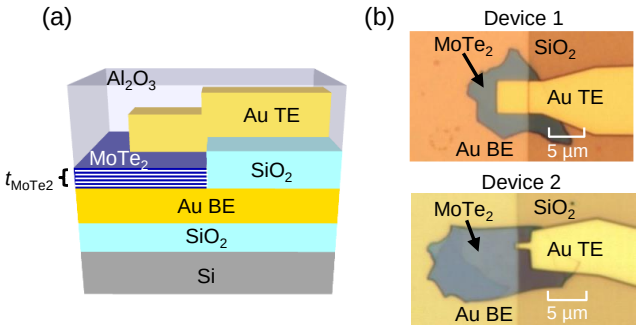



Figure 2.1: (a) Side-view schematic of $MoTe_2$ devices with a $SiO_2$ isolation layer between the Au top and bottom electrodes, as well as an $Al_2O_3$ capping layer. (b) Optical images of two devices, Device 1 ($t_{MoTe2}$ ~ 30 nm) and Device 2 ($t_{MoTe2}$ ~ 55 nm) with top electrode areas of 4.5 × 4.5 $\mu m^2$ and 0.7 × 0.4 $\mu m^2$, respectively.

### 2.2.2 2D Material Transfer Process

The procedure for transferring 2D layers that have been mechanically exfoliated onto $SiO_2$/Si chips is outlined below. A microscope with a heated stage and a micromanipulator inside a $N_2$ glove box (with <3 ppm $O_2$ and <1 ppm $H_2O$) are needed to perform the transfer.

1. Spin-coat a thin layer of polypropylene carbonate (PPC) on a hemispherical polydimethylsiloxane (PDMS) stamp, as in Ref. [119]. Attach PPC/PDMS stamp to a glass slide.
2. Place the 2D material sample on the stage inside glove box with carbon tape or other adhesive and find the flake of interest under the microscope.
3. Using the micromanipulator, lower the PPC/PDMS onto the 2D material sample until they are in contact.
4. Heat stage to 80°C and then allow it to cool down to 40°C.

5. Slowly lift the PPC/PDMS stamp from 2D material. The flake of interest should lift off of the $SiO_2$/Si chip and remain attached to the PPC/PDMS stamp.
6. Place target substrate on stage using carbon tape and find the region of interest.
7. Align PPC/PDMS stamp and press it onto target sample until they are in contact.
8. Heat stage to 110°C and wait 5 minutes.
9. Slowly peel stamp off the sample. The 2D material should remain on the target substrate.
10. Soak sample in acetone to remove PPC residue and rinse with IPA.

## 2.3 Electrical Characterization

We perform electrical measurements with a Keithley 4200-SCS using Keithley Interactive Test Environment (KITE) software in a Janis vacuum probe station. Figure 2.2a-b shows measured direct current vs. voltage (*I*-*V*) curves of the two devices, with the arrows illustrating the direction of the voltage sweep. The devices typically have initial resistances of 1 kΩ to 1 MΩ (depending on TE area and $t_{MoTe2}$). At higher voltages, the devices undergo a "forming" step during a DC *I*-*V* sweep. We use a current compliance (10 μA to 10 mA) and external series resistor (0.2 to 1 kΩ) to limit the amount of current. The devices transition to a low resistance state (LRS) with resistances $R_{LRS}$ = 40 to 800 Ω, depending on the current compliance and series resistance used. When a voltage sweep of the opposite polarity is performed, the devices switch to a high resistance state (HRS) (the "RESET" step), and they transition back to the LRS after the polarity of the sweep is reversed again (the "SET" step). Figure 2.2b shows bipolar switching of Devices 1 and 2.

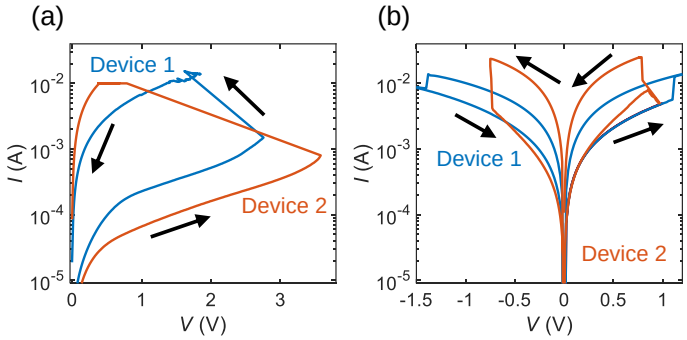
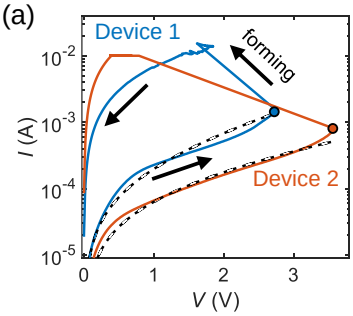



Figure 2.2: (a) Measured *I*-*V* characteristics showing forming of Devices 1 and 2, with the arrows corresponding to the voltage sweep direction. (b) Measured *I*-*V* characteristics showing bipolar switching of Devices 1 and 2.

(a)




(b)

| | $\epsilon_i$ | $\sigma_0$ (S/m) | $E$ (eV) |
|---|---|---|---|
| Device 1 | 12 | 700 | 0.4 |
| Device 2 | 12 | 4000 | 0.29 |

Figure 2.3: Measured *I-V* curves of Devices 1 and 2 from Figure 2.2a (solid colored lines), with data before forming fit to a modified 3D Poole-Frenkel equation (dashed black lines). Black arrows represent the measurement direction. The circled data points signify ($V_{forming}$, $I_{forming}$). (b) Fitting parameters from 3D Poole-Frenkel equation used to fit the *I-V* curves.

We use a modified three-dimensional (3D) Poole-Frenkel equation [120-122] to fit the *I-V* curves of Devices 1 and 2 during the forward sweep, as shown in Figure 2.3a. The model takes into account the effects of donors and traps and is used to model the conduction mechanism in these devices before forming. The fitting parameters used in the model are the high frequency relative dielectric constant $\epsilon_i$ of $MoTe_2$ [123], conductivity $\sigma_0$ (includes mobility, density of states, and donor and trap densities, as described in Ref. [120]), and activation energy *E*. Figure 2.3b shows the fitting parameters used for Devices 1 and 2.

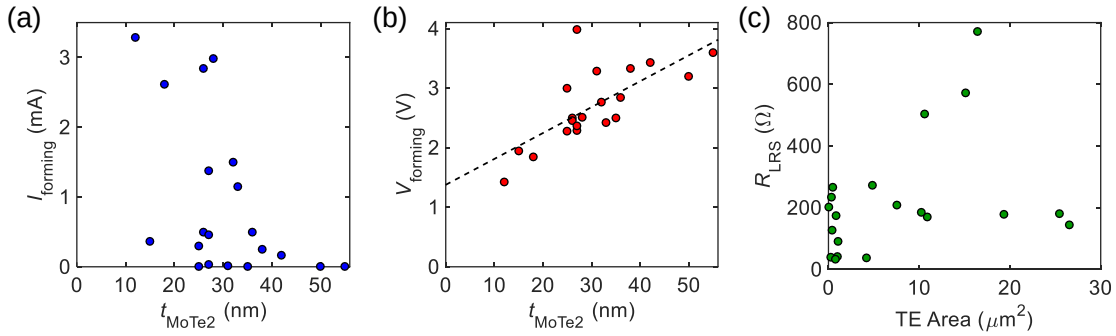



Figure 2.4: (a) Forming current ($I_{forming}$) vs. $MoTe_2$ thickness ($t_{MoTe2}$) for several $MoTe_2$ devices. (b) Forming voltage ($V_{forming}$) vs. $t_{MoTe2}$. The dashed line represents a linear fit. (c) Low resistance state $R_{LRS}$ as a function of TE area for the same set of devices.

We measured ~20 devices with similar forming and bipolar switching to that of Devices 1 and 2. We present data on forming current ($I_{forming}$) and forming voltage ($V_{forming}$) vs $t_{MoTe2}$, and low resistance state ($R_{LRS}$) vs. TE area for several $MoTe_2$ devices in Figure 2.4. The dashed line in Figure 2.4b is a linear fit to the data, with slope 0.04 V/nm, which is the average forming field, and y-intercept of 1.38 V. $R_{LRS}$ has no dependence on top electrode

(TE) area, which suggests that switching results in the formation of conductive regions smaller than the area of the top electrode.

## 2.4 Scanning Thermal Microscopy (SThM)

### 2.4.1 Measurement Details and Calibration Process

To gain insight into the thermal origins of the device switching behavior, we use scanning thermal microscopy (SThM). SThM is an atomic force microscope (AFM) technique wherein a specialized AFM probe is used in physical contact with a device to measure its surface temperature [124-126]. A voltage applied to the device induces Joule heating, which in turn causes the SThM probe to heat up. The electrical resistance of the probe changes with temperature, leading to a change in the output voltage ($\Delta V_{SThM}$) of the SThM. $\Delta V_{SThM}$ is proportional to the temperature rise of the device surface ($\Delta T_S$) above the ambient. The spatial resolution of these SThM probes is typically ~100 nm (depending on environmental conditions and calibration) [102,124-127], making it preferable to other techniques such as gate resistance thermometry, which gives average device temperature [128], or Raman thermometry, which has good material selectivity but a diffraction-limited spatial resolution of ~0.5 μm [102,125].

The SThM used in these experiments is from Anasys Instruments and was added to an MFP-3D AFM from Asylum Research. The probes are model PR-EX-GLA-5 from Anasys Instruments, which consist of a thin Pd line on $Si_3N_4$ with a resonant frequency of ~50 kHz and a spring constant of ~0.1 N/m. SThM measurements are performed in passive mode with a bias of 0.5 V. The scans are performed at a rate of 0.8 Hz and contact mode set point of 0.5 V, i.e. an estimated force of ~5 nN. We perform all measurements at room temperature with 20-30% humidity. Measurements are either performed in steady-state, in which a constant voltage is applied to the device and the probe is scanned to obtain spatial temperature maps, or during operation, in which the voltage is swept while the SThM probe is held in a ~10 nm × 10 nm area on the device surface above the hot spot.

We calibrate the SThM probe by measuring metal lines of varying nominal width (50 nm to 750 nm) with the same probe, and we convert the SThM voltage to temperature using the known temperature coefficient of resistance (TCR) of the metal lines. The metal lines are capped with an $Al_2O_3$ layer (comparable to the one on our memory devices) to account

for similar capacitance effects and similar thermal (boundary) resistance at the probe-sample interface. The electrical capacitance coupling of the SThM to the device is also more than two orders of magnitude smaller than that of the memory device due to the large difference between the SThM probe area and the device area.

The calibration estimates the combined heat transport through direct heat conduction, convection, and a water meniscus at the probe-sample interface, resulting in an effective thermal exchange radius $r_{th}$. Our calibration yields a width-dependent calibration factor $F(w)$, which is constant for $w > 200$ nm but decreases for $w < 200$ nm (see Ref. [127], which uses the same calibrated probe as we use in our measurements). This suggests $r_{th} \sim 100$ nm, which is in good agreement with previous work by Puyoo *et al*. [129]. Since our $MoTe_2$ device features are larger than 200 nm in this work, we use $F = 6.5 \pm 0.5$ mV/K.

We note that the calibration process must be performed for each probe used, and we can only obtain surface temperature estimates from SThM images taken with a calibrated probe. A probe can be used on many devices, depending on the surface roughness and measurement conditions. Our devices have low surface roughness (<2 nm) and we use the same measurement conditions across samples, so we find that we can take >100 thermal maps before the probe physically degrades and the SThM signal changes become evident.

The SThM images typically have an offset and slope, even with no applied voltage. Using the SThM image at 0 V applied to the device (see Figure 2.5), we fit a line through one row of the data and subtract the slope from the image to flatten it. We repeat this process for one column of the data. Next, we subtract the offset from the image to bring the average to 0 V. For all subsequent images at higher bias, we similarly flatten the images and subtract the offset using the values from the 0 V image.

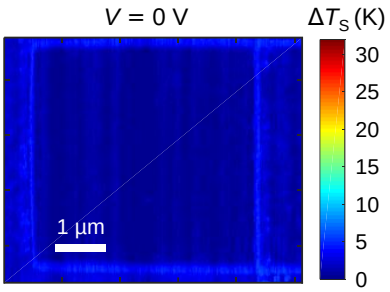



Figure 2.5: SThM image of Device 1 with applied voltage of 0 V. This image is used to flatten all other SThM images taken on Device 1. The mapped temperature in the color bar is at the top of the $Al_2O_3$ layer (~10 nm) which covers this device.

### 2.4.2 SThM Images During Steady-State Operation

Figure 2.6a shows a schematic of the setup, with the SThM probe on top of the $Al_2O_3$ surface. The $Al_2O_3$ (or some other insulator) is needed to electrically isolate the probe and the TE. Figure 2.6b displays an AFM image of the TE region of Device 1 (in the LRS), illustrating a bump (~15 nm high) that emerged on the Au TE after the forming step. An SThM image is simultaneously taken with no bias applied to the device and is used to flatten all subsequent images at nonzero bias, as discussed in Section 2.4.1. We then apply a voltage to the TE while grounding the BE (without a series resistor), as illustrated in Figure 2.6a. Figure 2.6c-d shows SThM images of Device 1 with input power $P$ ~ 1.6 mW and 2.5 mW, respectively, and the color bar shows the $\Delta T_S$ range (0-30 K) using a calibration factor $F = \Delta V_{SThM}/\Delta T_S = 6.5 \pm 0.5$ mV/K [127]. The images show a hot spot on the TE, matching the location of the bump in Figure 2.6b, becoming larger and hotter as we increase the input power. This localized heating suggests the formation of a conductive plug, and similar results have been observed for ~10 other devices. We point out that this is the first direct observation of localized switching visualized through thermal mapping TMD-based memory devices.

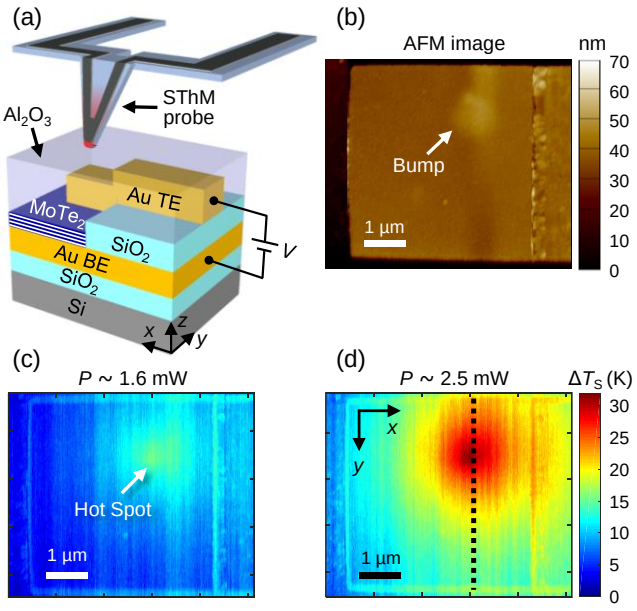



Figure 2.6: (a) Schematic of SThM setup, showing the probe on the surface of the $Al_2O_3$ capping layer and above the Au TE region. (b) AFM image of the top electrode region of Device 1, which is in the low resistance state. SThM images of Device 1 at power inputs of (c) $P$ ~ 1.6 mW and (d) $P$ ~ 2.5 mW. The color bar shows the temperature rise at the surface of the $Al_2O_3$ ($\Delta T_S$), which was obtained using a calibration factor of 6.5 mV/K.

We note that the edges of the TE appear clearly in the higher input power images (Figure 2.6c-d) and seem to heat up. However, because this nonzero SThM voltage is also measured at the edges of the electrodes during the 0 V scan (see Figure 2.5), we are confident that this is not a result of heating at the edges of the electrodes. Instead, this nonzero SThM voltage is observed at the edges because the measurement is affected by the topography of the sample. We also point out that the gradual topography change from the bump on the TE in Figure 2.6b does not affect the SThM signal (and therefore the accuracy of the mapped temperature), as shown in Figure 2.5. Only drastic topography changes, like the edges of our top electrode (~80 nm tall), appear to affect the SThM signal because the thermal exchange radius will be partially truncated while the SThM probe goes over a sharp step (see Figure 4 in Ref. [129]).

## 2.5 Electro-thermal Simulations

### 2.5.1 Simulation Details

We recall that SThM measures the *surface* temperature at the top of the $Al_2O_3$ layer covering the devices. Thus, we perform 3D finite element electro-thermal simulations using COMSOL® Multiphysics to estimate temperature rise *within* the plug ($\Delta T_{plug}$) when the device is under bias, in addition to the diameter of the conductive plug ($d_{plug}$). An electrical model is used to apply a voltage between the TE and BE, and a thermal model is used to predict the temperature distribution. The two models are coupled via Joule heating and temperature-dependent material properties (see Table 2.1).

The bottom of the Si substrate is held at ambient temperature ($T_0$ = 293 K), and the outer boundaries are treated as insulated (adiabatic). We model the $MoTe_2$ layer as two regions, the conductive plug and the rest of the film, with different electrical conductivity values $\sigma_{plug}$ and $\sigma_{film}$. We assume a ratio $r_\sigma = \sigma_{plug}/\sigma_{film} = 100$ between the two regions, based on the change in resistance of our devices before and after forming. We model the plug and film resistances in parallel to obtain the measured $R_{LRS} \sim 167\ \Omega$ at $V = 0.65$ V for this device, as shown in Eq. (1):

$$R_{LRS} = \frac{t_{MoTe2}}{\sigma_{plug} A_{plug} + \sigma_{film} A_{film}} \quad (1)$$

We also include a temperature dependence term in the $MoTe_2$ film electrical conductivity $\sigma_{film}$, based on exponential fits to electrical conductivity σ vs. $T$ of unformed devices. The σ used for the $MoTe_2$ film and conductive plug in our simulation are given in Eqs. (2) and (3), respectively:

$$\sigma_{film} = \frac{t_{MoTe2}}{R_{LRS}(r_\sigma A_{plug} + A_{film})} e^{0.007(T-T_0)} \quad (2)$$

$$\sigma_{plug} = \frac{r_\sigma t_{MoTe2}}{R_{LRS}(r_\sigma A_{plug} + A_{film})} \quad (3)$$

Table 2.1: Material properties used in electrothermal simulations, where $T_0$ = 293 K.

| | σ (S/m) | k (W/m/K) |
|---|---|---|
| Au (electrode) | $1.4 \times 10^7/[1 + \alpha(T - T_0)]$ | $\sigma L_0 T$ (= 100 at 293 K) |
| $SiO_2$ | $1 \times 10^{-12}$ | 1.4 (Ref. [130]) |
| Si | $2 \times 10^4$ (for doping of $2 \times 10^{19}$ $cm^{-2}$) | 95 (Refs. [131,132]) |
| $MoTe_2$ (film) | See Eq. (2) | 10 (in plane) 1.5 (out of plane) [133] |
| $MoTe_2$ (plug) | See Eq. (3) | |

The electrical conductivity of Au is $\sigma_{Au} = 1.4 \times 10^7$ S/m with a temperature dependence based on a measured temperature coefficient of resistance $\alpha = 0.0025$ $K^{-1}$ for thin Au films [134]. The thermal conductivity of Au is estimated using the Wiedemann-Franz Law with $k_{Au} = \sigma_{Au} L_0 T$, where the Lorenz number is $L_0 = 2.44 \times 10^{-8}$ $W\Omega K^{-2}$ (see Table 2.1). The thermal boundary resistance (TBR) is applied at various interfaces to model heat fluxes and temperature gradients. The TBRs for Au-$SiO_2$ and $SiO_2$-Si interfaces are 10 $m^2KGW^{-1}$ and 3 $m^2KGW^{-1}$, respectively [130,135]. We average $\Delta T_{surf}$ from simulations across the thermal exchange radius of the SThM probe to get the expected Gaussian averaging from thermal measurements. From these simulations, we estimate the range of $\Delta T_{plug}$ for the different $d_{plug}$ and applied voltage values.

### 2.5.2 Simulation Results

We correlate our experimental results to 3D electro-thermal simulations performed using finite element modeling (COMSOL® Multiphysics). These simulations allow us to estimate the temperature of the conductive plug during operation as well as the plug

diameter ($d_{plug}$), based on the surface temperature obtained by SThM. Figure 2.7a shows the $\Delta T_S$ profile of Device 1 along the black dashed line in Figure 2.6d. This reveals broad heating of the entire TE, including $\Delta T_S > 15$ K at the edges, due to significant lateral heat spreading.

We find that among the simulation parameters, the thermal boundary resistance (TBR) at the $MoTe_2$-Au interfaces plays a key role, yet it is among the least well-known inputs (e.g. compared to thermal conductivities of Au or $SiO_2$). The simulated $\Delta T_S$ profiles in Figure 2.7b show the closest agreement with the SThM data for TBR ≈ 70 $m^2KGW^{-1}$ and $d_{plug}$ from 250 to 350 nm. The estimated TBR is equivalent to a thermal boundary conductance (TBC = 1/TBR) of ~14 $MWm^{-2}K^{-1}$, which is very similar to that found for other 2D materials [96,102]. We note the peak $\Delta T_S$ increases with increasing $d_{plug}$, unlike in metal-oxide RRAM devices [127]. Our simulations suggest this behavior is due to the electrical conductivity of the plug being only ~100× higher than that of the surrounding $MoTe_2$ unlike in metal-oxide RRAM where the conductive filament conductivity is $>10^{10}$ higher than that of the insulating metal-oxide surrounding it [136,137]. Therefore, the film surrounding the conductive plug in our devices also contributes to current conduction (and heating).

Figure 2.7c shows a cross-sectional view of the simulated temperature distribution within the device for $d_{plug}$ = 300 nm and $P$ = 2.5 mW. The image has been cropped to focus on the conductive plug region (the silicon is actually 20 μm thick in our simulations). As expected, the hottest region is in the $MoTe_2$ where the conductive plug is formed, with a peak $\Delta T_{plug} \approx 223$ K. There is substantial heat dissipation into the electrodes and the substrate, resulting in much cooler temperatures at the top and bottom surfaces. The simulated surface and $MoTe_2$ plug $\Delta T$ for different power inputs is displayed in Figure 2.7d. At $P$ = 2.5 mW, the peak $\Delta T_S$ ranges from ~33 K to 39 K (corresponding to the SThM measurements), while the estimated peak $\Delta T_{plug}$ ranges from ~200 K to 235 K for the different plug diameters. $\Delta T_{plug}$ has a larger range because it is more sensitive to plug diameter than $\Delta T_S$. Heat dissipation in the TE also limits our ability to accurately extract $\Delta T_{plug}$, which could be better estimated by reducing the TE thickness in future work. (The thicknesses of the $MoTe_2$ and top $SiO_2$ layers should also be reduced, due to required step coverage.)

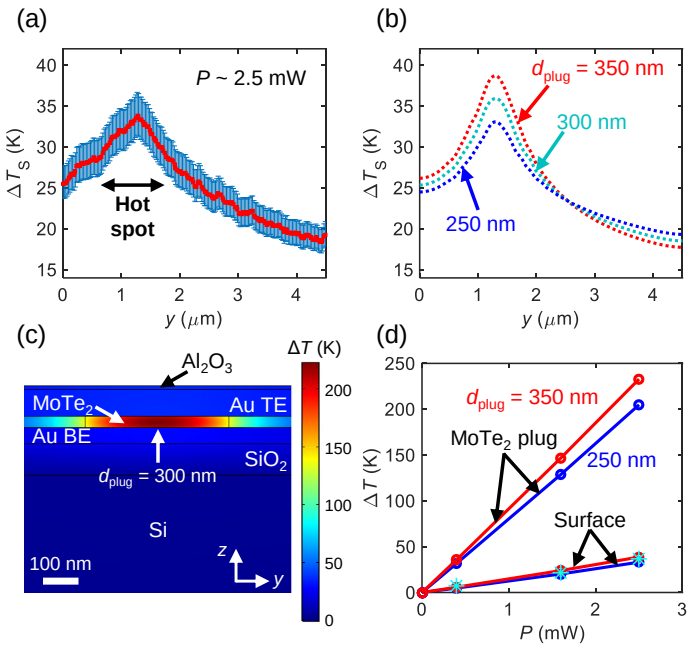



Figure 2.7: (a) Surface temperature profile from SThM measurement along the black dashed line in Figure 2.6d, with error bars. (b) Electro-thermal simulations of $\Delta T_S$ profiles for conductive plug diameters $d_{plug}$ ranging from 250 to 350 nm at $P$ ~ 2.5 mW. (c) Simulation of $\Delta T$ along cross-section of device at $P$ ~ 2.5 mW for $d_{plug}$ = 300 nm. (d) Simulated $\Delta T$ vs. $P$ for different $d_{plug}$ inside the $MoTe_2$ plug and at the surface of the device. The cyan stars correspond to $\Delta T_S$ from SThM measurements.

## 2.6 SThM Measurements During Device Switching

In addition to steady-state measurements, we also sweep the voltage while holding the SThM probe stationary and in contact with the device surface directly above the conductive plug. This allows us to measure $\Delta T_S$ while switching the device between the LRS and HRS. Figure 2.8a shows an optical image of the device (Device 3) with $t_{MoTe2}$ ~ 27 nm and TE area of 2.5 × 2.6 μm$^2$. The *I-V* measurements during bipolar switching (using an external series resistance of 220 Ω) and the corresponding $\Delta T_S$ from SThM are displayed in Figure 2.8b-c. The curves in Figure 2.8b are labeled with "SET" or "RESET," corresponding to a transition to the LRS or HRS, respectively. $\Delta T_S$ reaches between 50 and 115 K when the device switches between the two states. Assuming $d_{plug}$ between 250 and 400 nm, we use our simulations to estimate the maximum $T_{plug}$ during the first RESET and SET measurements to be ~650-750 K and ~530-630 K, respectively. During the second RESET and SET measurements $T_{plug}$ is estimated to be ~700-850 K and 650-800 K, respectively. We note that SThM measurements cannot capture fast temperature transients (the thermal

time constant of Pd-based probes is ~300 μs [126] and the sampling time of our SThM system is ~3 ms), so the plug and surface may reach even higher temperatures (and possibly the semiconducting-to-metallic transition temperature [59,138,139] for $MoTe_2$, ~920-1170 K) during bipolar switching.

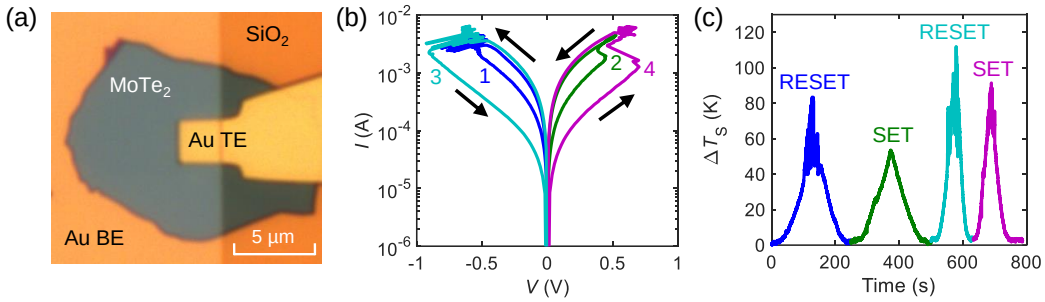



Figure 2.8: (a) Optical image of Device 3 with $t_{MoTe2}$ ~ 27 nm and TE area of 2.5 × 2.6 μm$^2$. (b) *I-V* measurements of Device 3 showing 2 switching cycles (with a series resistance of 220 Ω). The number next to each curve corresponds to the order of the measurements. (c) $\Delta T_S$ from SThM measurements as a function of time, taken simultaneously with the *I-V* measurements in (b) of the same color. $\Delta T_S$ was calculated from $\Delta V_{SThM}$ using a calibration factor of 6.5 mV/K.

## 2.7 Temperature-Dependent *I-V* Measurements

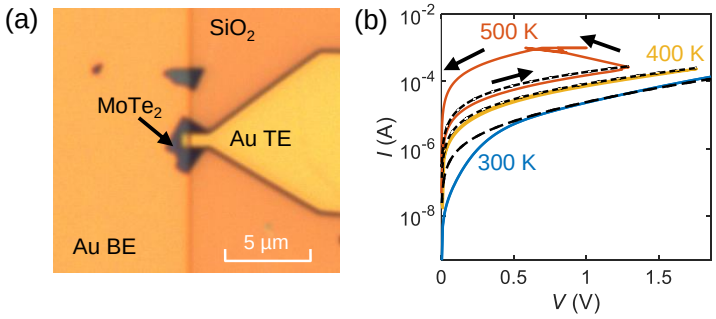



Figure 2.9: (a) Optical image of Device 4 with $t_{MoTe2}$ = 16 nm and TE area of 0.45 × 0.9 μm$^2$. (b) Forward-backward *I-V* measurements from 0 to 2 V at varying ambient temperature (solid colored lines). The *I-V* data before forming are fit to a modified 3D Poole-Frenkel model (dashed black lines).

To determine the effect of temperature on forming voltage, we also take temperature-dependent electrical measurements of a $MoTe_2$ device with $t_{MoTe2}$ = 16 nm and TE area $A$ = 0.45 × 0.9 μm$^2$ (Device 4, shown in Figure 2.9a). We perform forward-backward sweep measurements at $T_0$ = 300 K, 400 K, and 500 K ambient temperature using a sweep range of 0 to 2 V and an external series resistance of 1000 Ω. We fit the *I-V* curves (before

forming) to a 3D modified Poole-Frenkel model, as in Figure 2.3, with $\epsilon_i$ = 10, $\sigma_0$ = 500 S/m, and $E$ = 0.37 eV. At ambient temperatures of 300 K and 400 K, the device remains in the unformed state following forward-backward *I-V* sweeps. At $T_0$ = 500 K ambient temperature, we observe device forming at ~1.3 V (see Figure 2.9b). These measurements, in addition to the SThM measurements above, reveal that the forming mechanism has a thermally-activated component.

## 2.8 TEM Cross-sections and EDS Elemental Maps

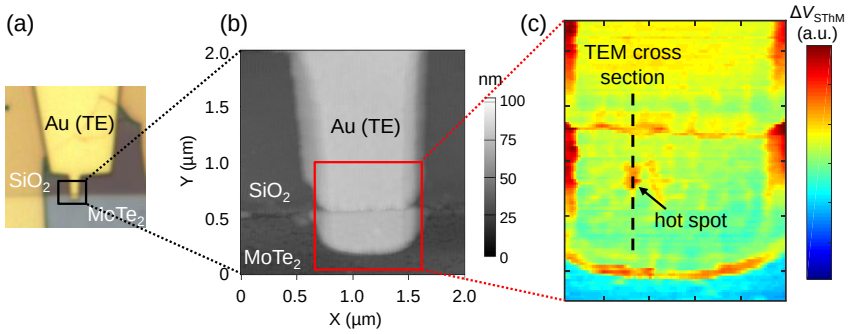



Figure 2.10: (a) Optical and (b) AFM images of Device 2. (c) SThM image showing the region of the device corresponding to the red box in (b). The vertical black dashed line is drawn along the hot spot (marked by arrow) where the TEM cross-section was taken, for Figure 2.11.

Next, we perform transmission electron microscopy (TEM) and energy dispersive spectroscopy (EDS) of Device 2 after switching. The device was cross-sectioned at the location of the conductive plug, which was determined by SThM, as shown in Figure 2.10. We use these SThM images to determine the location of the conductive plugs for the transmission electron microscopy (TEM) study. Therefore, we do not use a calibrated probe for these measurements since we only need qualitative thermal maps rather than surface temperature estimates. Figure 2.11a shows the TEM image of Device 2 across its active region, which was switched to the HRS before TEM imaging. Figure 2.11c-e shows EDS elemental intensity maps of Au, Mo, and Te, respectively. These maps reveal Mo and Te vacancies near the edge of the Au TE and Au within the $MoTe_2$ layer, suggesting that Au has migrated from one electrode to the other, displacing Mo and Te atoms. This migration likely results in the bump seen in the AFM image of Figure 2.6b.

We also see some evidence of O displacing Mo and Te atoms (Figure 2.11g), which could be due to partial oxidation during fabrication. However, we do not expect O migration to be the primary cause of switching due to the low resistances measured in our devices, unlike in metal-oxide RRAM [127]. Switching in metal-oxide RRAM is often attributed to oxygen vacancies that form a conductive filament, which effectively reduces the device resistance [140]. We do not expect oxygen migration to reduce the resistance of our devices, because $MoO_x$ is more resistive than $MoTe_2$ [141].

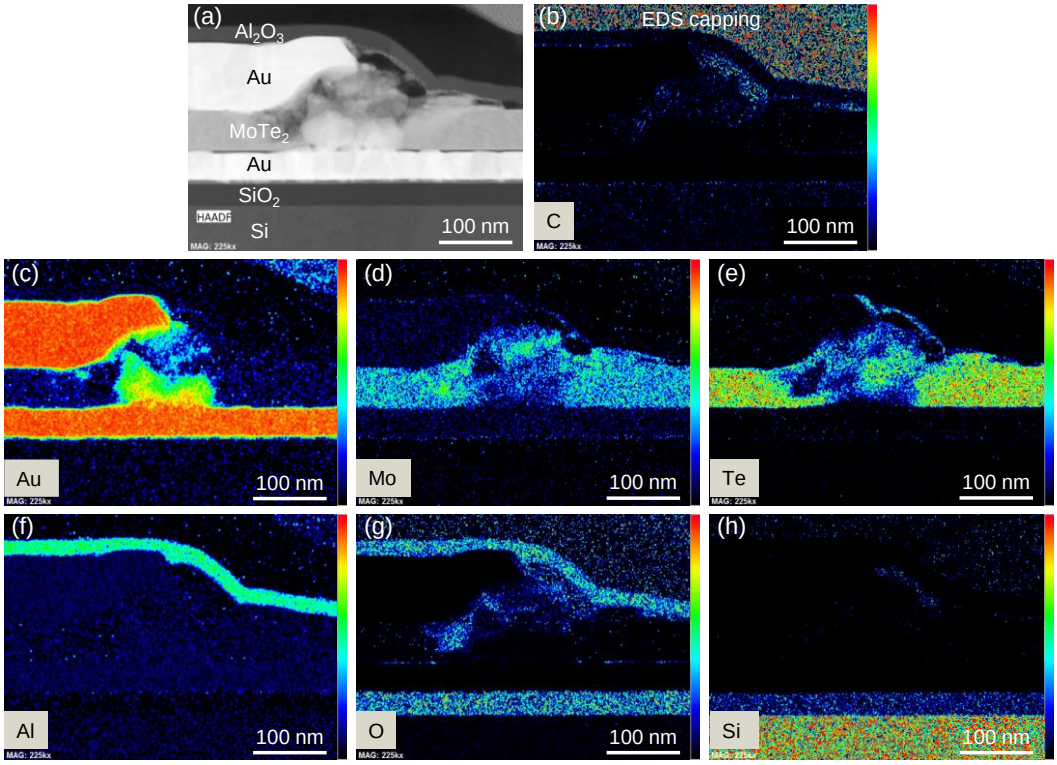



Figure 2.11: (a) High-angle annular dark-field (HAADF) TEM cross-section of Device 2, which was switched to the HRS before imaging. EDS elemental intensity maps showing (b) the EDS capping layer, (c) Au, (d) Mo, (e) Te, (f) Al, (g) O, and (h) Si atoms. The color bar shows the relative concentration of atoms, with red corresponding to the highest and black corresponding to the lowest.

SThM and TEM images of a different device (Device 5), initially in the LRS before TEM imaging, are shown in Figure 2.12 and Figure 2.13, respectively. Device 5 has $t_{MoTe2}$ = 50 nm and a TE area of 2.2 × 1.9 μm$^2$. Mo and Te vacancies in the $MoTe_2$ film and Au diffusion between electrodes are similarly observed in these images. The Au migration, like metal ion migration in conductive bridge random access memory (CBRAM) [142,143], might explain the very low resistances measured (as low as ~40 Ω in some

cases) when the devices are switched to the LRS (see Figure 2.4). During the RESET measurement, the Au bridge between electrodes likely breaks, causing an increase in resistance.

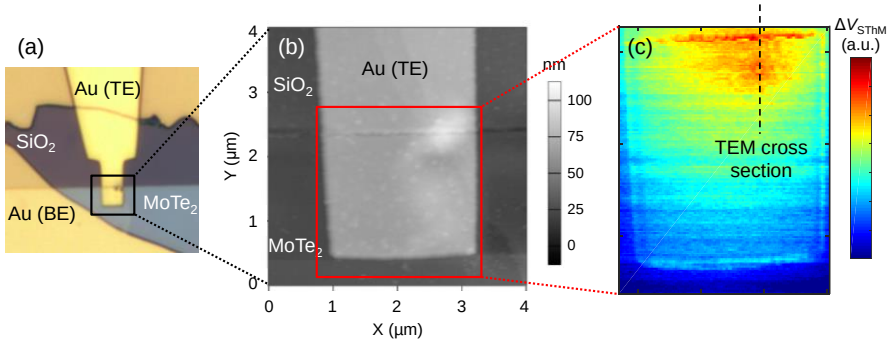



Figure 2.12: (a) Optical and (b) AFM images of Device 5 with $t_{MoTe2}$ = 50 nm and TE area of 2.2 × 1.9 μm$^2$. (c) SThM image showing the region of the device corresponding to the red box in (b). The vertical black dashed line is drawn along the hot spot where the TEM cross-section was taken, for Figure 2.13.

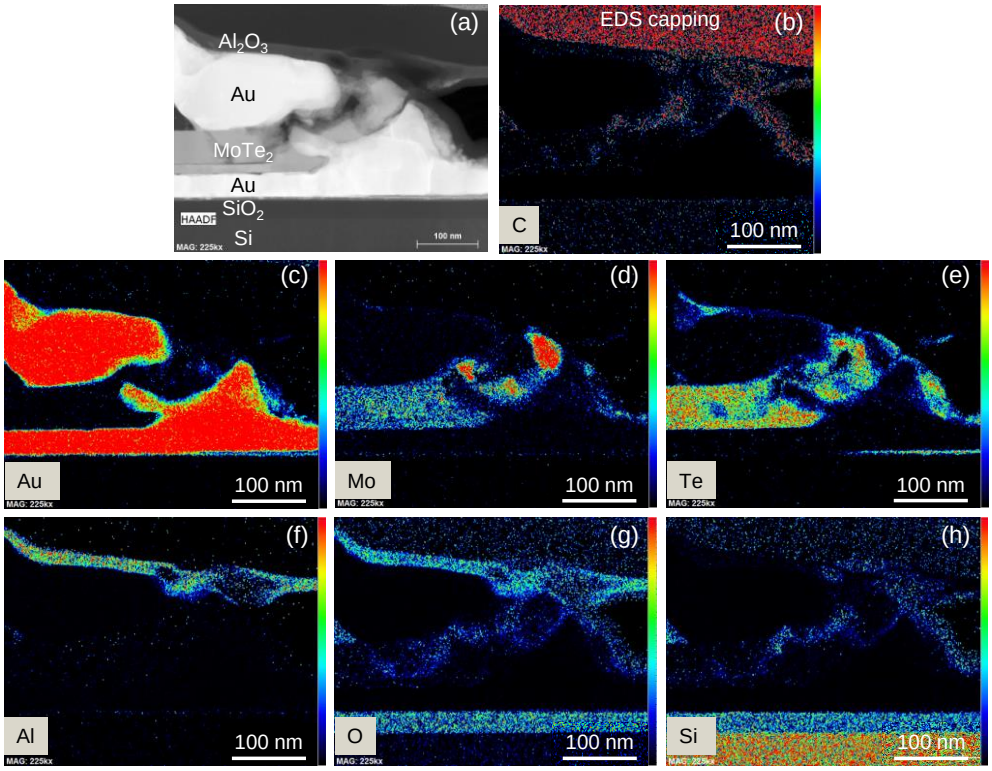



Figure 2.13: (a) HAADF TEM cross-section of Device 5, which was switched to the low resistance state before imaging. EDS elemental intensity maps showing (b) the EDS capping layer, (c) Au, (d) Mo, (e) Te, (f) Al, (g) O, and (h) Si atoms. The color bar shows the relative concentration of atoms, with red corresponding to the highest and black corresponding to the lowest.

We note that Au migration has been observed in other thin film devices, including memory devices, from thermal stress during operation [144,145]. We estimate current densities over $10^5$ A/cm$^2$ in the Au electrodes during the forming step and even higher during bipolar switching, which are sufficiently high to cause Au migration [146,147]. The Au migration can also occur at defects in the Au or in the $MoTe_2$ [100,148], where local current densities are larger. Though metal ion diffusion from the electrodes has often been reported in other types of devices and is of concern with regard to reliability and endurance in memory, this phenomenon has only recently been reported in TMD-based resistive memory devices [97,100]. We use Au electrodes in this study because it has often been used as a good contact metal to TMD semiconductors [51,149]. In addition, we find that $MoTe_2$ has good adhesion to Au during the transfer process due to the affinity of Au to chalcogen atoms [150,151]. (We observe that the $MoTe_2$ delaminates from other metals such as Pt or TiN during fabrication.)

## 2.9 $MoTe_2$ Device with Graphite Electrodes

To test other conductive (but non-metallic) electrodes, we also fabricate similar devices with graphite, which is an ultra-flat semi-metal, as the top and bottom electrodes. The same fabrication and transfer processes used for the $MoTe_2$ devices with Au electrodes are used here for devices with graphite electrodes, except that Pd is used to contact the graphite films. Figure 2.14a-b shows a schematic and optical image of such a device (Device 6) with $t_{MoTe2}$ ~ 29 nm, graphene bottom electrode thickness $t_{Gr,BE}$ ~ 14 nm, graphene top electrode thickness $t_{Gr,TE}$ ~ 5 nm, and TE area of ~40 μm$^2$. *I-V* measurements shown in Figure 2.14c reveal that at $V = 0.1$ V, the device has a resistance of ~15 MΩ, and at ~3.2 V it transitions to the LRS with ~1.6 kΩ. A series resistor with $R = 1$ kΩ was used for these measurements. We were unable to RESET the device back to the HRS using either voltage polarity, possibly due to the additional series resistance of the graphite. The same behavior (stuck in LRS after forming) was reproduced on another device with graphite electrodes.

Thus, the different behavior between the devices with Au and graphite electrodes suggests, first, that initial forming of the $MoTe_2$ is not triggered by metal ion migration from the electrodes and, second, that further bipolar switching only in devices with Au electrodes is caused by conductive metal bridging, as seen in the TEMs discussed earlier.

This mechanism is different from that of ref. [101], which suggested bipolar switching due to localized phase change induced by an electric field. However, different initial forming and switching mechanisms among different studies cannot be ruled out because there may be differences in sample quality (e.g. Te vacancies [152]) and processing (e.g. oxidation [153]). For example, a thin oxide layer on the $MoTe_2$ surface could rupture in a filamentary manner, leading to highly localized electric fields, current flow, and subsequently a phase change in the pristine $MoTe_2$ beneath. Such an effect was recently observed in $Ge_2Sb_2Te_5$-based phase change memory with a thin oxidized electrode, which switched at lower current than control devices due to oxide filament formation [96]. (We do not expect such an oxide and such highly localized electric fields in our devices due to careful processing in a $N_2$ glove box.) Other potential causes of forming could be defect (i.e. vacancy) generation or Te migration [153,154]. Immediately after forming, the current (and power) density is quite high, leading to significant Joule heating and causing Au migration, which is a thermally-activated process. Subsequent switching between the LRS and HRS is likely caused by the breaking and forming of these Au conductive plugs between the electrodes, as suggested by our cross-sectional TEMs.

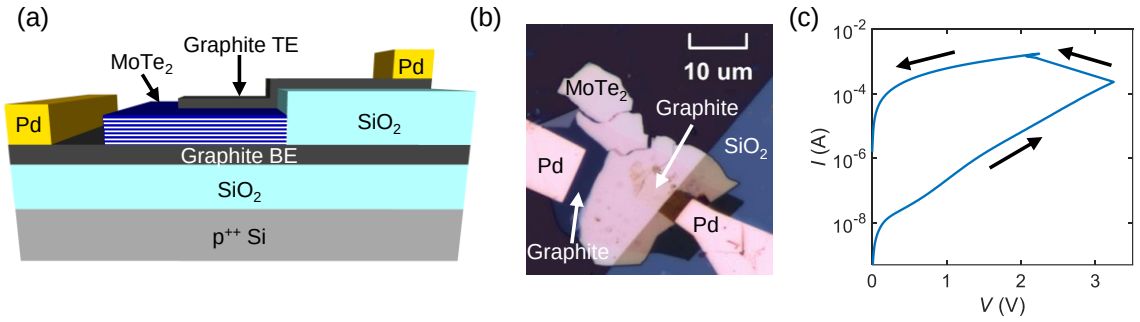



Figure 2.14: (a) Schematic and (b) optical image of a graphite-$MoTe_2$-graphite device with Pd contacts to the graphite (Device 6). (c) Measured *I-V* curve showing device forming at ~3.2 V, with an external series resistance of 1000 Ω.

## 2.10 Conclusion

In conclusion, we observed localized heating during operation of $MoTe_2$-based memory devices and measured their surface temperature using SThM for the first time. Together with temperature-dependent electrical data and TEM images, these SThM measurements reveal that both the forming and switching mechanisms have thermally-activated components. While the initial forming process may be caused by defect

generation or Te migration, subsequent bipolar switching appears due to Au migration from the electrodes. Nevertheless, simulations suggest that high internal temperatures during switching could also cause localized phase change in the $MoTe_2$. Beyond this study, the SThM technique can also be applied to other traditional or emerging resistive memory devices to determine the location and temperature of switching regions, which is essential for understanding and optimizing such data storage.

# Chapter 3

# Pulsed Voltage Measurements of $MoS_2$ Transistors

## 3.1 Introduction

Two-dimensional (2D) semiconductors like molybdenum disulfide ($MoS_2$) are promising for applications in low-power electronics due to their electrical properties, atomically thin nature, and lack of dangling bonds [38,155]. The electrical characteristics, including current drive, mobility, and current on/off ratio, of $MoS_2$ field-effect transistors (FETs) have been widely studied over the last several years [38,51,53,155-161]. However, DC electrical measurements of these and most novel devices often exhibit hysteresis in their current vs. gate voltage ($I_D$-$V_{GS}$) measurements. Hysteresis, defined here as the difference in threshold voltage ($V_T$) between the reverse and forward voltage sweeps ($\Delta V_T$), typically depends on voltage sweep rate, sweep direction, sweep range, and environmental conditions during the measurement [158,162-164].

The difference in $I_D$-$V_{GS}$ curves is due to trapped charges on the surface of the $MoS_2$, in the gate dielectric, at the $MoS_2$/dielectric interface, or in the $MoS_2$ itself [158-161,163,165-167]. Electrostatic screening by adsorbed water molecules, with electric dipoles aligned along the gate-induced electric field, has also been proposed as a contributor to this hysteresis [157,158,168]. As field-effect mobility ($\mu_{FE}$) and $V_T$ are often extracted from $I_D$-$V_{GS}$ sweeps in the forward or reverse direction, hysteresis in DC measurements leads to uncertainty in the electrical characteristics of such 2D devices. While hysteresis can be reduced through device encapsulation, e.g. with a high-quality $Al_2O_3$ dielectric [169] the majority of new and prototype devices are often tested without encapsulation or in air, where their electrical evaluation remains challenging.

Pulsed voltage measurements can reduce hysteresis in the $I_D$-$V_{GS}$ curves of transistors if the pulse width times are less than the time constant of charge traps. This technique has

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This chapter was adapted, with permission, from I. M. Datye, A. J. Gabourie, C. D. English, K. K. H. Smithe, C. J. McClellan, N. C. Wang, E. Pop, "Reduction of Hysteresis in $MoS_2$ Transistors Using Pulsed Voltage Measurements," *2D Materials*, vol. 6, p. 011004, 2019. Copyright 2019 IOP Publishing.

been used for graphene, carbon nanotube, and organic FETs to suppress hysteresis, but has not been applied to most of the TMDs including $MoS_2$ [162,164,170-172]. In this study, we apply voltage pulses to the gates of $MoS_2$ transistors to eliminate hysteresis, examine charge trapping, and extract device parameters (like mobility) that represent the intrinsic behavior of these devices [173]. Using this simple yet effective technique, hysteresis is nearly eliminated, which we quantify as a reduction by more than 80% under all conditions tested (~99% in some cases), and the extracted mobility converges to a unique value. We apply this technique to FETs fabricated using both exfoliated and synthetic, chemical vapor deposition (CVD) grown $MoS_2$, as well as different gate dielectrics ($SiO_2$ and $HfO_2$). We compare the different types of devices and examine the effects of air versus vacuum and temperature-dependent measurements on hysteresis. Finally, we use a tunneling front model to examine the depths of charge traps in our gate dielectrics.

## 3.2 Measurement Methods

We measure DC and pulsed transfer characteristics with a Keithley 4200-SCS and 4225-PMU using the Keithley Interactive Test Environment (KITE) software. While specialized, impedance-matched test structures and equipment are generally used for high-speed measurements [174], we find that such precautions are not needed if specific measurement guidelines are followed, greatly simplifying the set-up. Our guidelines are as follows.

First, we measure DC transfer curves to identify the non-negligible hysteresis. Next, we switch our instrumentation to pulse-measure units (PMUs) for pulsed measurements. After enabling the waveform capture test mode for a transient measurement, we set the timing parameters. Since each typical DC sample takes >250 ms to acquire, we use a pulse width $t_{on} \leq 250$ ms to reduce hysteresis. In some cases, we find that $t_{on} > 250$ ms can also reduce hysteresis because of charge de-trapping during the off time, $t_{off}$ (see Figure 3.1e). Additionally, we keep our rise and fall times ($t_R$ and $t_F$ respectively) $<0.1t_{on}$. For each PMU, we set the current range to the smallest value greater than the peak DC currents to ensure proper measurement range, resolution, and timing. As a result, the noise floor is increased during pulsed measurements. To test the worst-case cable, chuck, and pad capacitive charging scenario, we set the gate bias to the maximum $V_{GS}$ applied in our DC

measurements. As seen in Figure 3.1f, immediately after the rise of the pulse, there is a decay in current caused by a combination of parasitic capacitances and trapped charges. Since $I_D$-$V_{GS}$ sweeps with PMUs report spot means of current during the 75-90% section of the pulse [175] (red region in Figure 3.1f), if that portion of the transient appears to overlap with charging currents from parasitics, we select a larger $t_{on}$. Otherwise, if the parasitics do not interfere with the sampling region, we measure pulsed $I_D$-$V_{GS}$ sweeps with the present timing parameters. This process is repeated with smaller $t_{on}$ until hysteresis is eliminated.

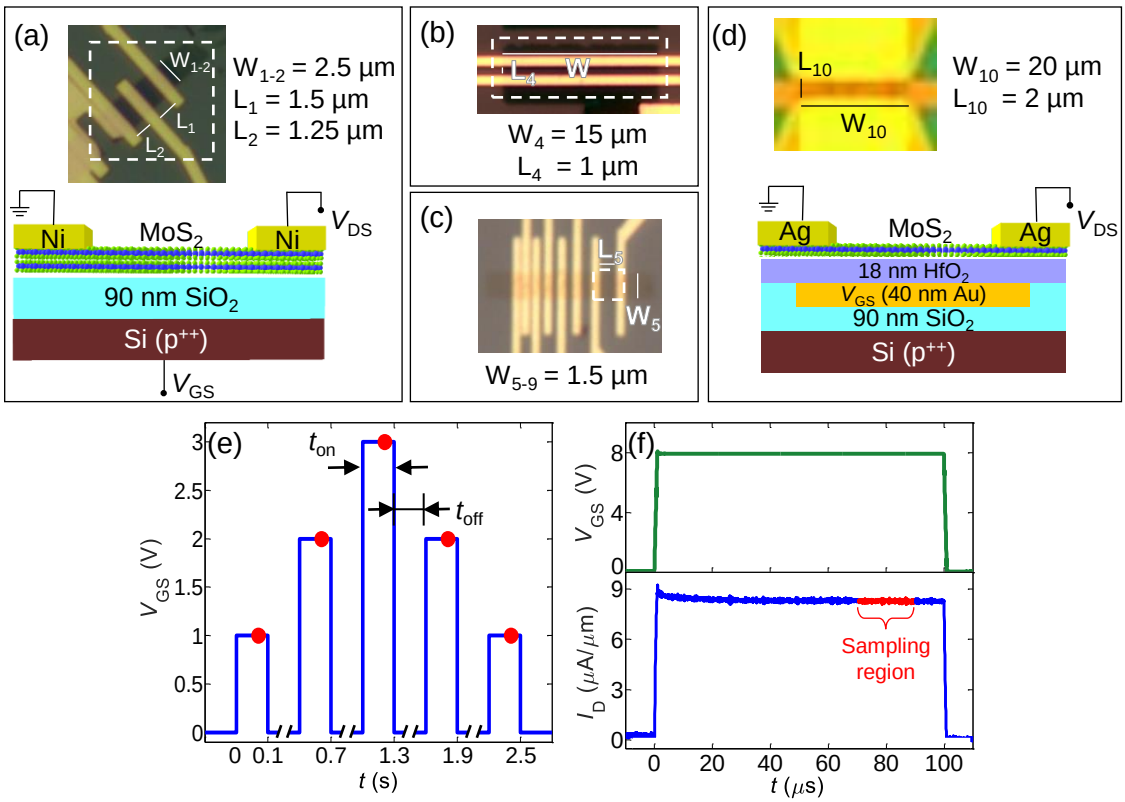


Figure 3.1: (a) Optical image of Devices 1 and 2 (Device 3 not shown), with ~5 nm thick exfoliated $MoS_2$, and cross-section schematic of the same devices. (b) Optical image of the back-gated 1L exfoliated device (Device 4) on 90 nm $SiO_2$/Si with Au source/drain contacts. (c) Optical image of all global back-gated chemical vapor deposited (CVD) monolayer devices (Devices 5-9) on 30 nm $SiO_2$/Si with Ag/Au source/drain contacts. (d) Optical image (top) and schematic cross-section (bottom) of the local back-gated CVD-grown 1L device (Device 10) on 18 nm $HfO_2$ with Ag/Au contacts. (e) Pulse train showing gate voltage pulses as a function of time with the on and off times indicated. (f) Transient plot showing $V_{GS}$ pulsed at 8 V and the resulting $I_D$ with the measurement taken during the 75-90% section of the pulse (shown in red).

## 3.3 Results and Discussion

Four types of $MoS_2$ transistors were examined in this work: exfoliated multi-layer (ML) and monolayer (1L) devices with global back-gates, as well as CVD-grown monolayer devices with global and local back-gates. All $MoS_2$ channels were lithographically patterned and etched into rectangles using either $XeF_2$, which was used for exfoliated devices, or $O_2$, which was used for CVD devices (conditions for $XeF_2$ and $O_2$ etches can be found in the supplements of Refs. [51] and [56], respectively). Contacts to all devices were patterned by optical lithography or electron-beam (e-beam) lithography with either Ni, Ag, or Au contacts, consistent with previous studies from our group [51,56]. Optical images of all devices are shown in Figure 3.1a-d. Typical global and local back-gated device schematics with biasing set-ups are displayed in Figure 3.1a,d respectively. Figure 3.1e-f shows the pulsed measurement scheme discussed in Section 3.2. We introduce each device configuration in the sections below and then make comparisons between the different devices, discussing the overall results.

### 3.3.1 Exfoliated Multi-Layer $MoS_2$ Devices

Exfoliated ML (~5 nm thick) $MoS_2$ devices were prepared as described in Ref. [51], here with Ni contacts (40 nm) on $SiO_2$ (90 nm) and Si ($p^+$) substrates, which also serve as global back-gates. Figure 3.1a shows an optical image and a schematic of Devices 1 and 2 with channel lengths $L_1$ = 1.5 µm, $L_2$ = 1.25 µm, and widths $W_{1,2}$ = 2.5 µm. Device 3 (not shown) has dimensions $L_3$ = 1.7 µm and $W_3$ = 1 µm. DC and pulsed drain current ($I_D$) measurements are performed by forward and backward sweeps of gate voltage $V_{GS}$ from -15 V to 25 V, with drain voltage $V_{DS}$ = 1 V. We vary the pulse widths from $t_{on}$ = 500 µs to 500 ms, with $t_{off}$ = 500 ms and rise and fall times $t_{R,F}$ = 10 µs (see Figure 3.1e-f and Section 3.2 for more details).

Figure 3.2a-b shows the DC and pulsed $I_D$-$V_{GS}$ measurements of Device 1 at room temperature in air and in vacuum (~$10^{-5}$ Torr), respectively, after annealing in the vacuum probe station at 250 °C for 2 hours. The forward and reverse sweeps, as well as the hysteretic difference in threshold voltage between the two sweeps ($\Delta V_T$), are indicated in Figure 3.2a. For simplicity, each $V_T$ is extracted using the constant current method at $I_D$ = 0.7 µA/µm [176]. These n-type $MoS_2$ devices are dominated by donor-like trap states

[18,157], as follows. Under negative $V_{GS}$, the Fermi level in the $MoS_2$ channel moves closer to the valence band. The traps above the Fermi level are emptied of electrons and have positive charge, causing a negative $V_T$ shift. Under positive $V_{GS}$, electrons fill the charge traps, rendering them neutral and leading to a positive $V_T$ shift. Electrons remain trapped until the reverse sweep, during which they de-trap [177,178]. This is illustrated in the band diagrams of Figure 3.2c, which show how electrons trap and de-trap under positive and negative $V_{GS}$.

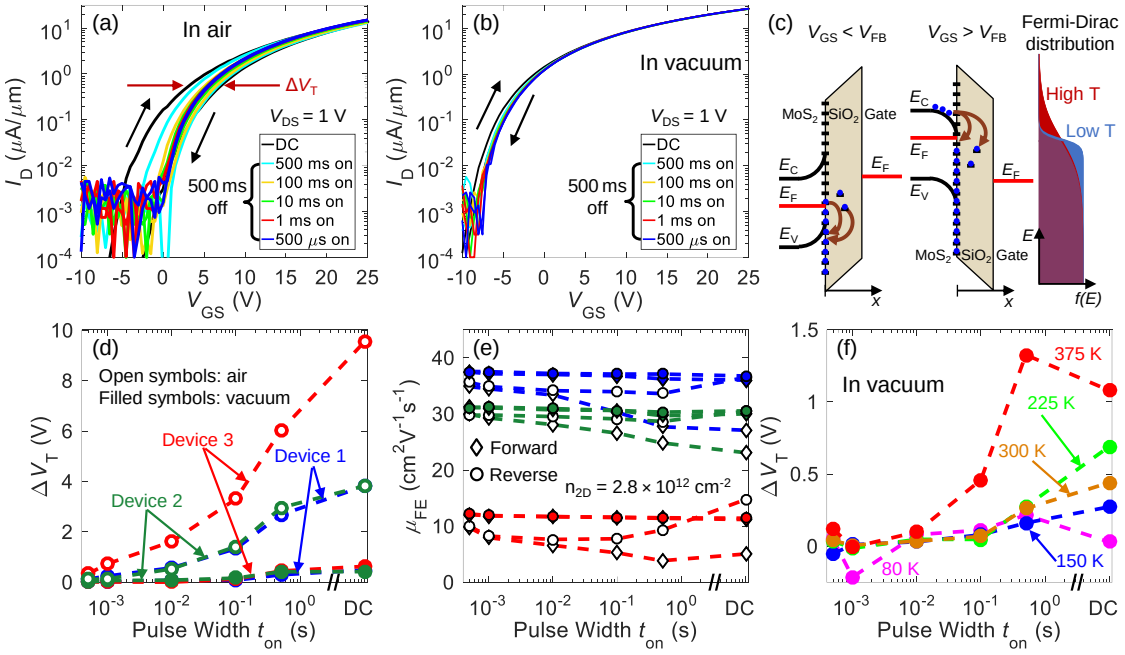


Figure 3.2: Measured transfer curves in (a) air and (b) vacuum of Device 1 (exfoliated multi-layer $MoS_2$) for DC and pulsed measurements at room temperature with $t_{on}$ from 500 µs to 500 ms and fixed $t_{off}$ = 500 ms. The pulsed measurements have a higher noise floor than DC measurements because the Keithley 4200 must have a set current range for pulsed measurements. (See Section 3.2.) (c) Energy band diagram illustrating charge trapping in the on and off states of the transistor. Fermi-Dirac distribution of electrons is shown at low (blue) and high (red) temperature. (d) Hysteresis ($\Delta V_T$) of Devices 1-3 as a function of pulse width, from DC down to 500 µs pulses. Open circles represent measurements in air, closed circles are in vacuum (~$10^{-5}$ Torr). (e) Estimated $\mu_{FE}$ of Devices 1-3 at a carrier density of $2.8 \times 10^{12}$ $cm^{-2}$ from forward (diamonds) and reverse (circles) sweeps in vacuum (filled symbols) and in air (unfilled symbols). (f) Temperature dependence of hysteresis $\Delta V_T$ for DC and pulsed measurements of Device 1 in vacuum. These plots correspond to the devices shown in Figure 3.1a.

The $V_T$ shift causes the forward $I_D$-$V_{GS}$ curve to look "stretched" and the reverse "compressed," leading to clockwise hysteresis. Clearly, these effects also render any field-

effect mobility estimates from such DC measurements to be incorrect with respect to the "true" mobility of the device. In contrast, pulsed measurements (as in Figure 3.1) minimize hysteresis when $t_{on}$ is smaller than the time constants of most traps, and smaller than alignment times of water molecule electric dipoles. A short $t_{on}$ prevents traps from becoming populated [164,172] or water dipoles from becoming aligned with the gate-induced field [157,158,168]. Additionally, during $t_{off}$, some of the trapped charge de-traps [160,162] and surface-adsorbed water dipoles relax and become unaligned.

Figure 3.2d shows a reduction in $\Delta V_T$ as the pulse widths ($t_{on}$) decrease for Devices 1-3, both in air and in vacuum. We note that $\Delta V_T$ is larger in air than in vacuum due to increased charge trapping from air and water adsorbates and the effect of water dipoles on the surface [157,158,160,163,165,168,179,180]. This suggests that *top surface* contaminants in air are more influential than $MoS_2/SiO_2$ interface traps or bulk traps, because performing DC measurements in vacuum leads to a reduction in $\Delta V_T$ of ~90%. However, as these devices have $\Delta V_T$ ~ 0.5-1 V for DC measurements even after the 250 °C vacuum anneal and 12 hours in vacuum, we conclude that surface traps do not account for all the hysteresis in these devices. The $MoS_2/SiO_2$ interface likely has charge traps from dangling bonds at the surface of the $SiO_2$, and the hysteresis may result from shallow traps at the interface during the $V_{GS}$ sweep [181,182]. Other sources of traps stem from defects in bulk $SiO_2$ and the few-layer $MoS_2$ itself [159,161,162,165,181,183].

Quantitatively, with modest pulses of $t_{on}$ = 1 ms and $t_{off}$ = 500 ms applied to all devices, $\Delta V_T \leq 0.73$ V in air and 0.07 V in vacuum, which corresponds to a reduction in hysteresis by ~92% and ~84%, respectively, compared to DC measurements. At the shortest pulse width ($t_{on}$ = 500 μs), hysteresis is reduced by nearly 97% and 90% in air and vacuum, respectively. Accounting for the oxide thickness, we can convert this "residual hysteresis" into an effective surface trap density ($N_{it}$):

$$N_{it} = \frac{1}{q} C_{ox} \Delta V_T , \tag{4}$$

where $C_{ox} \approx 38$ nF/cm$^2$ is the capacitance per unit area of the 90 nm thick $SiO_2$ used here and $q$ is the elementary charge. Thus, we estimate $N_{it}(\text{air}) \leq 1.8 \times 10^{11}$ cm$^{-2}$ and $N_{it}(\text{vacuum}) \leq 1.7 \times 10^{10}$ cm$^{-2}$ at $t_{on}$ = 1 ms. For these devices, this implies that at least ten times more hysteresis is caused by surface-adsorbed contaminants or water dipoles (pulsed

measurements in air) than is trapped in $MoS_2$ defects or the $SiO_2$ interface beneath (measurements in vacuum). We note that the density of defects in the $MoS_2$ could be higher, but not all defects are active charge traps. In addition, due to the thinness of the $MoS_2$ itself, most charge traps within it are likely to have very fast time constants, much faster than our pulse times. Nevertheless, for a highly scaled equivalent oxide thickness (EOT) of 1 nm, the equivalent hysteresis would be less than ~8.2 mV and ~0.78 mV, much smaller than a scaled 1 V supply voltage.

We calculate the field-effect mobility $\mu_{FE}$ as

$$\mu_{FE} \approx \frac{L}{WC_{ox}V_{DS}}\frac{dI_D}{dV_{GS}}. \quad (5)$$

We note that $\mu_{FE}$ is an underestimate of the actual mobility since we do not account for contact resistance in our measurements. $\mu_{FE}$ for all three devices is reported at a carrier density of $n = 2.8 \times 10^{12}$ cm$^{-2}$, where $n$ is estimated assuming a linear charge dependence on the gate overdrive voltage, $n \approx C_{ox}(V_{GS} - V_T)/q$. The plot of $\mu_{FE}$ for Devices 1-3 in air and in vacuum vs. pulse width is shown in Figure 3.2e, at room temperature. As $t_{on}$ pulse widths decrease, the mobility values extracted from the forward and reverse sweeps converge to a single value. Therefore, pulsed measurements enable the extraction of a unique mobility value, while $\mu_{FE}$ extracted from forward or reverse DC measurements would be either an under- or an over-estimate, respectively. This observation could, in part, explain the large spread of $MoS_2$ mobility values reported in the literature when extractions were performed purely from DC forward (or backward) sweeps.

We have also performed temperature-dependent DC and pulsed measurements in vacuum. The hysteresis is largest at 375 K, as shown in Figure 3.2f, suggesting the presence of thermally activated traps [160,170]. The measured $\Delta V_T$ at 150 K, 225 K, and 300 K display similar trends as a function of $t_{on}$ and have the highest values during DC measurements. $\Delta V_T$ is effectively eliminated at all temperatures when $t_{on} \leq 10$ ms, demonstrating that most traps have time constants longer than 10 ms. $\Delta V_T$ at 80 K is smaller than at any other temperature for the DC measurement and is nearly constant with decreasing pulse width. This apparent freeze-out of traps at low temperature is consistent with previous studies [164,179,184,185].

The behavior of hysteresis with respect to temperature matches our expectations based on the temperature-dependence of charge trapping mechanisms [171]. The capture rate of electrons is proportional to $T^2 \exp\left[\frac{E_F - E_C}{k_B T}\right][1 - f(E_T)]$, where $T$ is temperature, $E_F$ is the Fermi level, $E_C$ is the conduction band edge of $MoS_2$, $k_B$ is the Boltzmann constant, $E_T$ is the energy level of the trap, and $f(E_T)$ is the Fermi Dirac distribution at energy $E_T$ [186]. The emission rate of electrons from trap states is proportional to $T^2 \exp\left[\frac{E_T - E_C}{k_B T}\right] f(E_T)$ [186]. The first exponential term will dominate in most cases for both the capture and emission rates, but broadening of the Fermi function can also slightly modify these rates, as shown in Figure 3.2c. If $E_F > E_T$, the capture rate will be larger than the emission rate at both high and low temperatures, leading to hysteresis. Due to the exponential dependence on temperature, however, the capture rate at high temperatures will be significantly larger than at low temperatures, which agrees with our observation of larger hysteresis at 375 K than at 80 K or 150 K. At lower temperatures, the electron capture and emission rates are greatly reduced, effectively 'freezing' the traps in their current states, resulting in minimal to no hysteresis. If $E_F < E_T$, the emission rate will be larger than the capture rate, which will not contribute much to hysteresis since the trap states are more likely to remain empty.

### 3.3.2 Exfoliated Monolayer $MoS_2$ Devices

As before, we prepare $MoS_2$ devices by exfoliation from bulk $MoS_2$ onto $SiO_2$ (90 nm) and Si ($p^+$) substrates. Monolayer (1L) regions are identified by optical contrast and confirmed with Raman and photoluminescence measurements (see Figure 3.3). We fabricate FETs with Au contacts (40 nm thick) using methods described previously (see Section 3.4 for a discussion on the effect of different contact metals on hysteresis). An optical image of Device 4 (with dimensions $W_4$ = 15 μm and $L_4$ = 1 μm) can be seen in Figure 3.1b. Similar to the ML devices, we anneal these FETs in vacuum at 250 °C before the measurements. DC and pulsed measurements are then performed, without breaking vacuum, by a forward and backward sweep of $V_{GS}$ from -30 V to 30 V with $V_{DS}$ = 1 V. Again, pulse widths vary from $t_{on}$ = 500 μs to 500 ms, with a $t_{off}$ = 500 ms and $t_{R,F}$ = 10 μs.

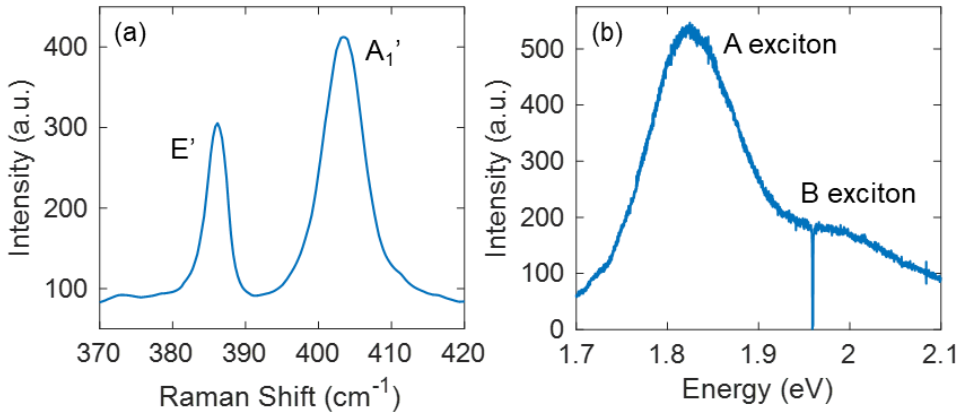


Figure 3.3: (a) Raman and (b) photoluminescence (PL) spectrum of the 1L exfoliated $MoS_2$ flake. The A exciton in (b) corresponds to the energy of the optical band gap of 1L $MoS_2$. The peak separation of the E' and $A_1$' peaks in (a) and the A exciton peak position and intensity in (b) provide confirmation that the $MoS_2$ is 1L.

The transfer $I_D$-$V_{GS}$ curves from the DC and pulsed measurements are shown in Figure 3.4a. While these transfer curves may exhibit little hysteresis at DC, our pulsed measurement technique nevertheless provides additional insight into charge trap states present in the system. To illustrate this, we extract $\Delta V_T$ from our $I_D$-$V_{GS}$ curves, using the constant current method with $I_D$ = 1 µA/µm, for temperatures from 80 K to 450 K and plot them vs. $t_{on}$ in Figure 3.4b. Across all temperatures, we see that the hysteresis is reduced as $t_{on}$ decreases. The substantial increase in $\Delta V_T$ at 450 K is indicative of the presence of thermally activated traps, as seen in the ML devices [160,170]. For $t_{on} \leq 100$ ms, $\Delta V_T$ at 450 K is comparable to $\Delta V_T$ at lower temperatures, suggesting that most of the thermally activated traps have time constants >100 ms. The discrepancy of $\Delta V_T$ between $t_{on}$ = 500 ms and DC also suggests that the thermally activated traps have de-trapping time constants >500 ms. This occurs because DC measurements take ~250 ms per voltage step (see Section 3.2), meaning that pulsed measurements with $t_{on}$ = 500 ms bias the device for approximately twice as long as DC. If the thermally activated traps have de-trapping time constants greater than $t_{off}$, then we would expect more hysteresis at $t_{on}$ = 500 ms.

In addition to the thermally activated traps, we note that hysteresis at 150 K and 450 K is not completely eliminated at the shortest pulse width of 500 µs. We expect a shorter $t_{on}$ to eliminate this remaining hysteresis; however, $t_{on}$ < 500 µs is not possible with our set-up because parasitic capacitances, stemming from the use of our probe station chuck as a

global back-gate, cause a charging current on the same time scale as charge trapping, interfering with the drain current measurements. This highlights a limitation of the pulsed measurement technique when the substrate is used as a global back-gate. However, at 300 K, we find that hysteresis is reduced by ~88% at modest pulses of $t_{on}$ = 1 ms with $\Delta V_T$ ~ 0.08 V, corresponding to $N_{it} \approx 1.9 \times 10^{10}$ cm$^{-2}$ and $\Delta V_T$ ~ 0.78 mV at an EOT of 1 nm. For the best case ($t_{on}$ = 500 µs), hysteresis is reduced by ~92% to $\Delta V_T$ ~ 0.05 V. Additionally, we find that mobilities extracted from the forward and reverse sweeps converge to a single value at $t_{on} \leq 1$ ms, as shown in Figure 3.4c. Once again, the pulsed measurement technique yields a reliable mobility estimate, whereas using either the forward or reverse DC sweeps could yield inconsistent mobility values.

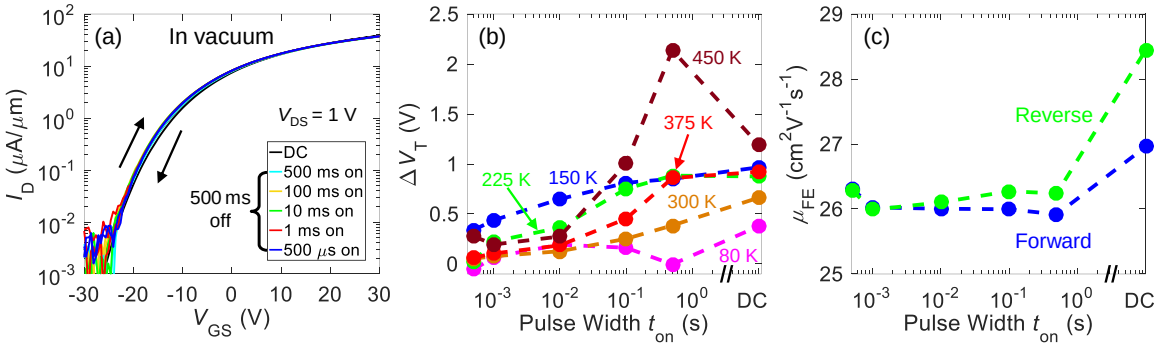


Figure 3.4: (a) Transfer curves of a 1L exfoliated $MoS_2$ device ($W$ = 15 µm, $L$ = 1 µm) with DC and pulsed measurements at room temperature, in vacuum, with $t_{on}$ from 500 µs to 500 ms and a fixed $t_{off}$ = 500 ms. This corresponds to Device 4 shown in Figure 3.1b. (b) Temperature-dependent hysteresis, $\Delta V_T$, for DC and pulsed measurements in vacuum, from 80 K to 450 K. (c) Estimated $\mu_{FE}$ from forward and reverse DC and pulsed measurements, in vacuum at room temperature.

### 3.3.3 CVD $MoS_2$ Devices (Global Back-Gate)

We also investigate $MoS_2$ devices grown by CVD directly on $SiO_2$ (30 nm) and Si ($p^+$) substrates, probing FETs with Ag/Au (20 nm/20 nm) contacts [53,56]. The $MoS_2$ channel width for Devices 5-9 is $W_{5\text{-}9}$ = 1.5 µm, and the channel lengths are $L_{5\text{-}9}$ = 50 nm, 100 nm, 200 nm, 600 nm, and 1 µm, as shown in Figure 3.1c. As before, the devices are annealed in the vacuum probe station at 250 °C, and subsequent measurements are performed without breaking vacuum, at room temperature. We perform DC and pulsed measurements by sweeping $V_{GS}$ from -5 V to 30 V with $V_{DS}$ = 1 V. As before, $t_{on}$ varies from 500 µs to 500 ms, with $t_{off}$ = 500 ms and $t_{R,F}$ = 10 µs.

Figure 3.5a shows the DC and pulsed $I_D$-$V_{GS}$ curves of Device 5 ($L$ = 1 μm) with the arrows indicating the forward and reverse sweeps. The reduction in hysteresis with decreasing pulse width is clearly illustrated in Figure 3.5b, where $V_T$ was extracted at $I_D$ = 1 μA/μm. The DC measurement for Device 5 has $\Delta V_T$ ~ 1.4 V, and hysteresis is reduced by ~89% at $t_{on}$ = 1 ms with $\Delta V_T$ ~ 0.08 V, corresponding to an active charge trap density of $N_{it}$ ~ 5.8 × $10^{10}$ $cm^{-2}$. The difference in the estimated $\mu_{FE}$ between the forward and backward sweeps (Figure 3.5c) for the DC measurement is ~5.7 $cm^2V^{-1}s^{-1}$ and reduces to just 0.24 $cm^2V^{-1}s^{-1}$ at $t_{on}$ = 1 ms. The latter is <2% of the estimated mobility (~16 $cm^2$/V/s), which thus converges to a unique value in the limit of these shortest pulses. As before, we note these mobility values include the contacts, and the intrinsic mobility of these films is higher, as discussed elsewhere [53,56].

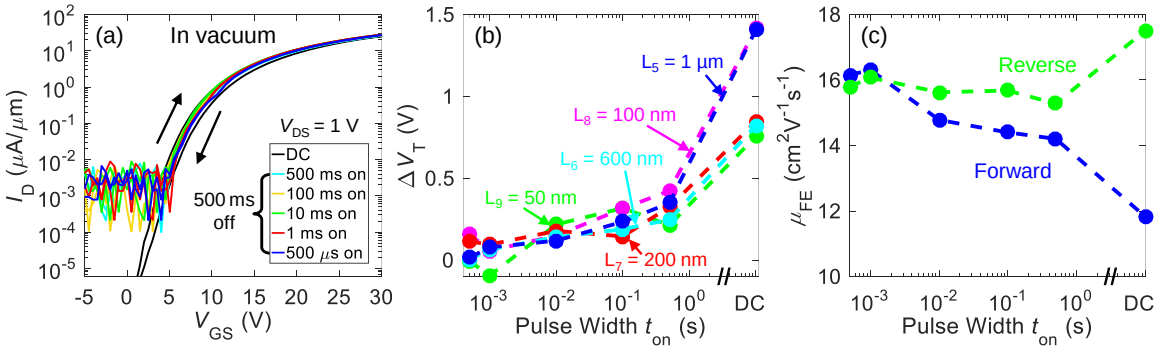


Figure 3.5: (a) Measured $I_D$ vs. $V_{GS}$ of a back-gated, CVD-grown 1L $MoS_2$ device (Device 5 with $W_5$ = 1.5 μm, $L_5$ = 1 μm) showing DC and pulsed measurements in vacuum at room temperature with $t_{on}$ varying from 500 μs to 500 ms and a fixed $t_{off}$ = 500 ms. (b) Hysteresis ($\Delta V_T$) as a function of pulse width for Devices 5-9 with $W_{5\text{-}9}$ = 1.5 μm and different channel lengths, as labeled. These correspond to the devices shown in Figure 3.1c. (c) Estimated $\mu_{FE}$ from forward and reverse sweeps in vacuum for DC and pulsed measurements of Device 5 ($L$ = 1 μm).

We compare $\Delta V_T$ for the different devices to determine the correlation between hysteresis and channel length, if any. Figure 3.5b reveals no clear trend of hysteresis with channel length, as all device lengths have the same trend in hysteresis vs. pulse width. Given that shorter channel devices have stronger effect of contacts [51], this suggests that the hysteresis observed in our devices is *not* a contact effect, and is largely due to active charge traps distributed along the device channel lengths.

### 3.3.4 CVD $MoS_2$ Devices (Local Back-Gate)

We also investigate devices with CVD-grown 1L $MoS_2$ *transferred* onto 18 nm of $HfO_2$ above a local Au back-gate (the $MoS_2$ was previously synthesized onto a separate $SiO_2$/Si substrate [53]). The process for transferring $MoS_2$ from the growth substrate onto local back-gates is as follows, similar to Ref. [187]:

1. Drop-cast PMMA A4 onto the growth substrate
2. Bake on a hot plate at 150 °C for 10 minutes
3. Place the chip in a glass petri dish with 1 M NaOH (aq.) solution heated to 80 °C
4. The NaOH will dissolve the $SiO_2$, causing the growth substrate to sink and the PMMA/$MoS_2$ to float on the surface
5. Use tweezers to transfer the PMMA/$MoS_2$ to a bath of deionized water and let it float on the surface for 30 minutes
6. Use tweezers to transfer the PMMA/$MoS_2$ to the $HfO_2$/Au local-back gated substrates
7. Point an $N_2$ gun directly on the PMMA to push out as much water as possible from beneath the PMMA/$MoS_2$
8. Place the new substrate on a room temperature hot plate and ramp up to 150 °C during a 20 minute time period
9. Soak in acetone for an hour to remove the PMMA
10. Perform a final rinse with methanol and dry with an $N_2$ gun

The source and drain contacts are patterned to overlap slightly with the local back-gate (Figure 3.1d), meaning that the $MoS_2$ channel is only gated through the $HfO_2$ dielectric and electrical hysteresis is entirely due to the $MoS_2$/$HfO_2$ interface. We study these devices because they typically present a more extreme level of hysteresis compared to the earlier test cases. In addition, the physically smaller local back-gate lowers parasitic capacitances, allowing pulse widths down to 750 ns to be used for device characterization. Figure 3.1d shows a schematic and an optical image of Device 10 with dimensions $W_{10}$ = 20 μm, $L_{10}$ = 2 μm, and Ag/Au (25/25 nm) contacts [56]. DC and pulsed measurements are performed in vacuum (after the anneal step described earlier) by a forward and backward sweep of $V_{GS}$ from -5 V to 8 V with $V_{DS}$ = 1 V, and $V_T$ extracted at $I_D$ = 1 μA/μm.

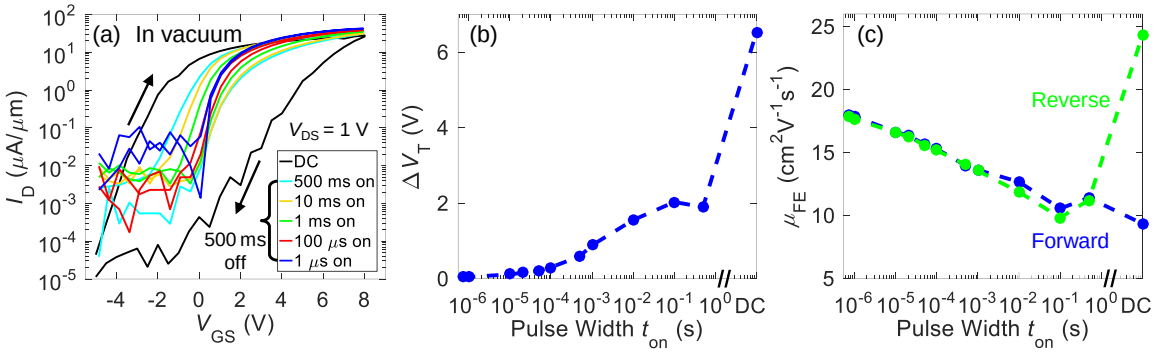


Figure 3.6: (a) Transfer characteristics of a CVD-grown $MoS_2$ device with local back-gate (Device 10 with $W_{10}$ = 20 μm, $L_{10}$ = 2 μm) for DC and pulsed measurements at room temperature with $t_{on}$ from 1 μs to 500 ms and a fixed $t_{off}$ = 500 ms. The measurements with $t_{on}$ = 100 ms, 500 μs, 50 μs, 20 μs, 10 μs and 750 ns are omitted for easier visualization. (b) Evolution of hysteresis, $\Delta V_T$, as a function of pulse width from DC down to 750 ns pulses in vacuum. For pulses below 1 μs, the hysteresis is reduced by 99%. (c) Estimated $\mu_{FE}$ from forward and reverse sweeps in vacuum. We note that mobility can be severely under- or overestimated (by up to 50%) if only forward or reverse DC sweeps are used.

We record both the DC and pulsed measurement $I_D$-$V_{GS}$ curves as seen in Figure 3.6a. We note that Figure 3.6a omits some of the pulsed measurements for easier visualization. Similar to observations for the other devices, the forward and reverse $I_D$-$V_{GS}$ sweeps converge to a single curve and $\Delta V_T$ decreases as the pulse width $t_{on}$ is reduced (Figure 3.6b). At $t_{on}$ = 1 ms, hysteresis is reduced by ~86% with $\Delta V_T$ = 1 V, which is still significant. The larger overall hysteresis in the *transferred* CVD-grown $MoS_2$ devices is attributed to traps introduced at the $MoS_2/HfO_2$ interface during the imperfect transfer process, and use of the $HfO_2$ dielectric which typically has higher trap densities than thermally-grown $SiO_2$ [188-190]. Thus, shorter pulses are needed to achieve $\Delta V_T$ values comparable to those of the other types of devices. At $t_{on}$ = 1 μs, we have $\Delta V_T$ ~ 0.075 V, corresponding to a ~99% reduction of hysteresis and an active charge trap density of ~3.7 × $10^{11}$ $cm^{-2}$. For an EOT of 1 nm, the equivalent hysteresis would be just ~17.1 mV. Thus, we demonstrate the elimination of hysteresis even for devices which suffer from higher trap densities (here due to the transfer process and the use of $HfO_2$ dielectric), proving the effectiveness of our measurement technique.

We also extract $\mu_{FE}$ versus $t_{on}$ as shown in Figure 3.6c. Once again, as the $t_{on}$ is shortened, the mobility converges to a single value between the forward and reverse sweeps. As we use a wider $t_{on}$ range for this device than for others, a clear trend of

increasing $\mu_{FE}$ with decreasing $t_{on}$ (particularly below 0.1 s) emerges. This trend could be the result of two competing phenomena affecting mobility: A transition from hopping transport to band transport (at shorter $t_{on}$), which increases mobility [156], and an increase in Coulomb scattering due to donor-like trap centers remaining positively charged during pulsed $I_D$-$V_{GS}$ measurements (i.e. not capturing electrons), which decreases mobility [43,155,191]. For this device, it appears that a transition from hopping to band transport (with decreasing $t_{on}$) dominates. Perhaps more importantly, in such devices with larger hysteresis, the field-effect mobility can be significantly under- or overestimated (by as much as 50%) if only the forward or reverse DC sweep is used, also revealed in Figure 3.6c.

## 3.4 Comparison of Devices

We now compare each device type to better understand the effects of the $MoS_2$ thickness, growth method and gate dielectric on charge trapping, all comparisons being for the measurements performed in vacuum after the anneal step. Figure 3.7a compares the estimated active charge trap density ($N_{it}$) as a function of pulse width $t_{on}$ with $t_{off}$ = 500 ms for all device types measured.

First, we compare the exfoliated devices, which all had 90 nm $SiO_2$/Si back-gates in common, but different contact metals (Au for 1L, Ni for ML). The different contact metals may account for the negative $V_T$ shift of ~10 V for the 1L device due to different Schottky barrier heights and contact resistances, as shown in other studies [50,192]. Because our measurements used pulsed $V_{GS}$ with constant $V_{DS}$ (not pulsed) and effectively eliminated hysteresis, we do not expect that the contacts play a large role in hysteresis, consistent with conclusions of the length-dependent measurements in Figure 3.5b. Despite this $V_T$ difference, Figure 3.7a shows that $N_{it}$ is only marginally higher for 1L than ML exfoliated $MoS_2$ FETs, at all pulse widths. The 1L of $MoS_2$ may be more strongly influenced by surface charge traps, causing additional hysteresis [165,193], although other studies contradict this by claiming that intrinsic charge traps between $MoS_2$ layers (within the ML devices) should be more influential [181,183]. A further study comparing devices with several different $MoS_2$ thicknesses is necessary to draw conclusions about the relationship between hysteresis and $MoS_2$ thickness.

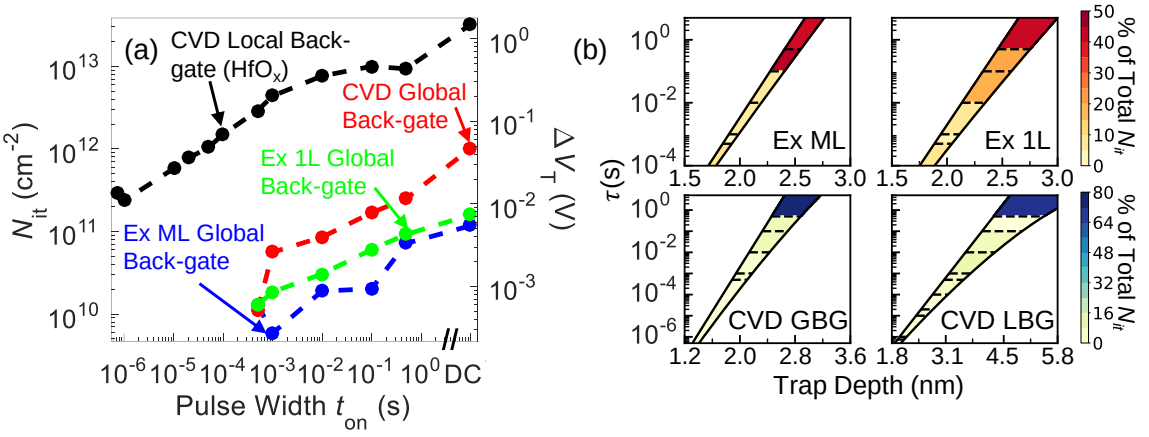


Figure 3.7: (a) Estimated active charge trap density ($N_{it}$) as a function of pulse width for the 4 different types of devices measured, in vacuum. ("Ex" = exfoliated, "CVD" = CVD-grown.) The right axis shows $\Delta V_T$ for each device scaled to an EOT of 1 nm. (b) Estimated tunneling time constants for a given trap depth into each device's respective oxide, for applied gate voltages of $V_{GS} = V_T$ (left line of each subplot) and $V_{GS}$ when $n = 10^{13}$ cm$^{-2}$ (right line of each subplot). The colors represent the proportion of total trap charge density found in the particular time constant and depth range. GBG = global back-gate. LBG = local back-gate.

Next, we compare the local back-gated (LBG) and the global back-gated (GBG) CVD-grown $MoS_2$ devices. Here, the $MoS_2$ growth conditions and device contacts are the same, but the gate dielectrics are different (18 nm $HfO_2$ for LBG, 30 nm $SiO_2$ for GBG) and the LBG device fabrication included a $MoS_2$ transfer step. Figure 3.7a reveals that the LBG device has much larger $N_{it}$ than the GBG device for all pulse widths. The contributing factors to this difference are the $HfO_2$ dielectric, which has an intrinsically higher trap density than $SiO_2$, and the imperfect $MoS_2$ transfer process, which can introduce defects and contaminants (see Section 3.3.4).

## 3.5 Tunneling Front Model

Finally, we can gain insight into the depths of active charge traps in our gate dielectric and the extent traps at those depths affect output characteristics by using a tunneling front model [194]. The tunneling front model calculates the trap time constant as a function of depth, $x$, and is given by:

$$\tau(x) = \tau_0 \exp\left(2\int_0^x K(x')dx'\right)$$

where $\tau_{0,SiO_2} \approx 6.6\times10^{-14}$ s [194] and $\tau_{0,HfO_2} \approx 1\times10^{-11}$ s [195] are characteristic time constants for $SiO_2$ and $HfO_2$ respectively, and *K(x)* is the effective barrier in the oxide. The barrier height can be written as $K(x) = \sqrt{2m_{ox}(\Phi_B - E(x))}/\hbar$ where $\Phi_B = \chi_{MoS_2} - \chi_{ox}$ and $E(x) = qFx$ with $F$ as the applied field and $q$ as the electron charge. To extract barrier heights, we use $\chi_{MoS_2}$ = 4.4 eV for ML flakes, $\chi_{MoS_2}$ = 4.25 eV for 1L flakes [196], $\chi_{SiO_2}$ = 0.95 eV [164], and $\chi_{HfO_2}$ = 2.65 eV [197]. The tunneling effective masses are $m_{SiO_2}$ = 0.42 $m_0$ [164] and $m_{HfO_2}$ = 0.2 $m_0$ [197] with $m_0$ as the electron mass. Lastly, the field, $F$, is given by $F = V_{ox}/t_{ox}$ where $V_{ox}$ is calculated numerically with the transcendental equation from [198]:

$$V_{GS} = V_0 + V_{th}\, ln\left[exp\left(\frac{n}{g_{2D}k_BT}\right) - 1\right] + V_{ox}$$

where $V_0 = E_G/(2q)$, $E_G$ is band gap energy, $V_{th} = k_BT/q$, $n$ is the electron density in the channel, $k_B$ is the Boltzmann constant, $T$ = 298K, and $V_{ox} = qn/C_{ox}$. The two-dimensional density of states is defined in [198] as $g_{2D} = g_s g_v m^*/2\pi\hbar^2$ where $g_s$ = 2 is the spin degeneracy and $g_v$ = 2 is the valley degeneracy [199].

Using these calculations, we obtain Figure 3.7b, which shows the tunneling time constants as a function of trap depth for two different biasing points. For each subplot, the left line is calculated for $V_{GS} = V_T$, and the right line is calculated for the $V_{GS}$ corresponding to $n = 10^{13}$ cm$^{-2}$. The bias range reflects the voltages we typically apply to our devices and allows us to determine expected charge trap depths. We see from the exfoliated and GBG CVD devices that the average trap depths range from ~1.8 nm to ~2.5 nm for time constants between 500 μs and 500 ms, respectively. However, the trap depths for the LBG CVD devices (on $HfO_2$) may reach as deep as ~5 nm at high bias and time constants of 500 ms. This difference is due to a larger electron affinity and smaller effective tunneling mass for $HfO_2$ than $SiO_2$.

The shaded regions in Figure 3.7b illustrate the percentage of total trap charge density found in a particular time constant range. There are notable differences between the exfoliated devices and CVD devices. For the CVD devices, we see that between 64-80% of the total trap density has a time constant greater than 500 ms, meaning pulse widths of 500 ms would be sufficient to eliminate most of the hysteresis. In contrast, only between

40-50% of the total trap density has a time constant greater than 500 ms in the exfoliated devices. This distinction suggests that the $MoS_2$ growth method and device fabrication process (including the high-temperature sulfur-rich ambient that the $SiO_2$ is exposed to during CVD growth) strongly influence the percentage of total trap density found in different trap time constant ranges. Nevertheless, we note that extremely stable and low-hysteresis CVD-grown devices have been recently reported after a high-quality $Al_2O_3$ encapsulation step [169].

## 3.6 Conclusion

In this chapter, we have described a simple pulsed measurement technique to reduce hysteresis in $MoS_2$ transistors by applying gate voltage pulses shorter than the time constants of trapped charge. We fabricate different types of $MoS_2$ devices (exfoliated and CVD-grown, as well as monolayer and multi-layer on different gate dielectrics) and measure $I_D$-$V_{GS}$ curves using both DC and pulsed measurements to compare hysteresis and charge trapping. The pulse widths necessary to eliminate hysteresis range from 1 μs to 1 ms, depending on the type of device. We demonstrate that our measurement technique successfully reduces hysteresis even for the most hysteretic devices, which in our case are transferred $MoS_2$ devices with $HfO_2$ as the gate dielectric. Though there is variability among the different devices with $SiO_2$ as the dielectric, we demonstrate a reduction in active charge trap density to $<1.4 \times 10^{10}$ $cm^{-2}$ across devices when $t_{on}$ = 500 μs.

We also show that while hysteresis in DC measurements hinders an accurate extraction of field-effect mobility, pulsed measurements allow extraction of the "true" mobility of $MoS_2$, which converges to a single value regardless of the voltage sweep direction. Conversely, we caution that estimating device mobility from hysteretic measurements could lead to errors as large as ~50%, potentially explaining some of the wide range of $MoS_2$ mobilities reported in the literature. Finally, we use a tunneling front model to quantify the depths of active charge traps in our gate dielectrics. The reproducible pulsed measurement technique demonstrated here can also be used to study the intrinsic properties of other low-dimensional and emerging devices which suffer from charge-trapping phenomena.

# Chapter 4

# Optical Properties and Strain-Tuning of $Mo_xW_{1-x}Te_2$

## 4.1 Introduction

Atomically thin layers of transition metal dichalcogenides (TMDs), such as $MoTe_2$, have been extensively studied for fundamental physics and applications [200,201]. Tuning their optical properties, which can be achieved through doping, alloying, strain, and heating, is crucial for understanding their light-matter interactions and for various applications in electronics and optoelectronics. The optical properties of atomically thin $MoTe_2$ have recently been characterized experimentally [62,202-205], and theoretical investigations have indicated that the aforementioned factors can significantly alter the material's band structure [58,60,206-208]. In particular, theory has predicted and measurements have demonstrated that alloying with tungsten or electrical gating of $MoTe_2$ can induce a phase change from a semiconducting to metallic state [60,206,209-212]. To date, however, few studies have experimentally examined the effects of strain on $MoTe_2$ or on $MoWTe_2$ alloys [213].

Here we investigate $Mo_{1-x}W_xTe_2$ with $x = 0.09$ and compare the properties of this alloy with the $MoTe_2$ compound [72]. For alloys with higher W content, i.e., $x > 0.09$, all reported growth processes have produced crystals in the 1T' phase. Therefore, this composition is close to the 2H phase boundary and should exhibit the lowest threshold for inducing a 2H to 1T' phase change by an external perturbation [211,214,215]. However, the optical properties of the 2H phase of $Mo_{0.91}W_{0.09}Te_2$ have yet to be investigated in detail and compared to those of $MoTe_2$. We study atomically thin crystals of the $Mo_{0.91}W_{0.09}Te_2$ alloy by Raman scattering, photoluminescence (PL), and absorption measurements, and compare the results with those for $MoTe_2$. We also measure PL while applying in-plane uniaxial

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tensile strain to the monolayer (1L) crystals of both compounds to alter their band structure, which has not been previously examined.

## 4.2 Crystal Growth, Characterization, and Sample Preparation

### 4.2.1 Growth of $Mo_{1-x}W_xTe_2$ Crystals

$Mo_{1-x}W_xTe_2$ crystals are grown using the chemical vapor transport (CVT) method. $Mo_{1-x}W_xTe_2$ powders with a nominal composition of $x = 0.15$ are synthesized by reacting stoichiometric amounts of molybdenum (99.999%), tungsten (99.99%) and tellurium (99.9%) powders at 750 °C for 5 days in vacuum-sealed quartz ampoules. For single crystal growth, approximately 1.5 g of poly-crystalline $Mo_{1-x}W_xTe_2$ powder and 0.1 g of iodine as a transport agent (99.8%, 4.7 mg/cm$^3$) are placed in HF-etched and vacuum baked quartz ampoules. Following several argon flush-evacuation cycles, the ampoules are vacuum-sealed. The CVT growth is conducted at 1000 °C in a single-zone furnace for 7 days followed by ice-water quenching. The growth produces monoclinic 1T'- $Mo_{1-x}W_xTe_2$ crystals that have been converted to the 2H phase by an additional vacuum annealing at 750 °C for 72 hours, followed by cooling to room temperature at 10 °C/hour.

### 4.2.2 Growth of $MoTe_2$ Crystals

$MoTe_2$ crystals are also grown using the CVT method. $MoTe_2$ molecular powder (ESPI Metals $MoTe_2$, 99.9%) is sealed in quartz ampoules with elemental iodine added as a transport agent (Alfa Aesar, 99.99+%) at 5 mg/cm$^3$. Ampoules are repeatedly purged and evacuated under argon before sealing. The crystals are grown for 14 days along a ~11 cm transport length, representing a 100 °C thermal gradient from a source hot zone kept at 800 °C.

### 4.2.3 Characterization of Crystals

Crystal phases of obtained $Mo_{1-x}W_xTe_2$ alloys are determined by powder X-ray diffraction (XRD) and aberration-corrected high angle annular dark field scanning transmission electron microscopy (Cs-corrected HAADF-STEM), as shown in Figure 4.1a-b. The XRD patterns of the powdered $Mo_{1-x}W_xTe_2$ crystals are obtained in the range of 10°

to 60° 2θ using a Philips X-ray diffractometer in the Bragg-Brentano geometry with CuKα radiation. Experimental lattice parameters are refined using the Materials Data, Inc., JADE 6.1 XRD Patterns Processing software (MDI JADE 6.1). HAADF-STEM images are recorded on an aberration-corrected FEI Titan 80-300 operating at 300 kV. The $Mo_{1-x}W_xTe_2$ crystals are crushed in ethanol and a drop of solution is deposited onto an amorphous Carbon (a-C) coated TEM grid (Agar Inc.). HAADF-STEM images are collected at a camera length of 100 mm corresponding to inner and outer collection angles of 70.6 and 399.5 mrad respectively.

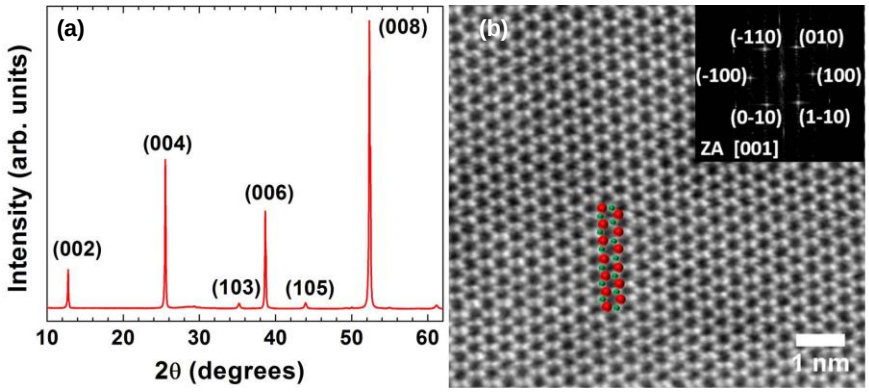


Figure 4.1: (a) Powder XRD pattern of 2H-$Mo_{0.91}W_{0.09}Te_2$. (b) High angle annular dark field scanning electron microscopy (HAADF-STEM) image of a 2H $Mo_{0.91}W_{0.09}Te_2$ sample together with an overlapped structural model; red (large) spheres: Mo/W atoms; green (small) spheres: Te atoms. Inset: Fast Fourier Transform (FFT) emphasizing the [001] zone axis.

The chemical composition of $Mo_{1-x}W_xTe_2$ alloys is determined using energy-dispersive X-ray spectroscopy (EDS) in a JEOL JSM-7100F field emission scanning electron microscope (FESEM) equipped with an Oxford Instruments X-Max 80 EDS detector. For quantitative analysis, EDS spectra are acquired from several 1×1 $\mu m^2$ areas on the sample at the following conditions: accelerating voltage 10 kV, working distance 10 mm, processing time 60 seconds with 15% deadtime. Spectra, as exemplified in Figure 4.2, have been fit and quantified using the AZtec software package in standardless mode. The W mole fraction in the $Mo_{1-x}W_xTe_2$ alloy, as determined from X-ray EDS, is $x = 0.09 \pm 0.01$ (see Figure 4.2). We note that the Te/(Mo+W) ratio in this sample has been measured to be $1.98 \pm 0.02$, which corresponds to the $Mo_{0.91}W_{0.09}Te_{1.98}$ composition. For simplicity, the

Te content in the formula is rounded to 2.0 and thus the alloy is represented by the $Mo_{0.91}W_{0.09}Te_2$ composition throughout this study.

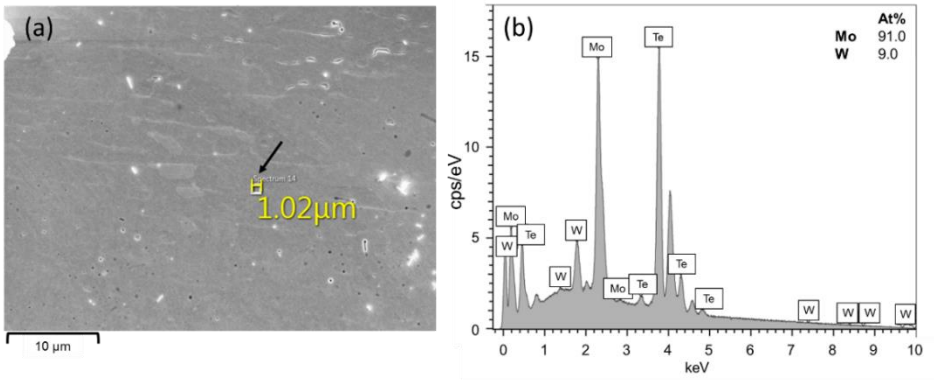


Figure 4.2: (a) SEM plan-view image of 2H-$Mo_{0.91}W_{0.09}Te_2$ sample surface. The black arrow points to the EDS spectrum sampled over ~1 $\mu m^2$ area. (b) Corresponding EDS spectrum measuring the 9 ± 1 atomic % W.

### 4.2.4 Sample Preparation

For the optical measurements without strain, we exfoliate $MoTe_2$ and $Mo_{0.91}W_{0.09}Te_2$ crystals from the bulk grown crystals onto ~1 mm thick polydimethylsiloxane (PDMS) substrates (base: curing agent ratios of 10.5:1 by volume) to obtain ultrathin flakes. The thicknesses of the atomically thin crystals are determined by Raman spectroscopy [62] and optical contrast.

For the optical measurements with strain, we transfer monolayer (1L) crystals from PDMS to polyethylene naphthalate (PEN) or polyethylene terephthalate glycol-modified (PETG) flexible plastic substrates using a stage heated to 40 °C with a micromanipulator to precisely position the crystals in the middle of the substrate. We press the PDMS onto the substrate using the micromanipulator and keep it in contact for 1 to 2 minutes. We slowly release the PDMS from the substrate, ensuring that the crystals do not break during the transfer.

The mechanical exfoliation is performed in ambient atmosphere and the transfer process is carried out in a $N_2$ glove box with generally <3 ppm $O_2$ and $H_2O$. We also spin-coat ~100 nm polymethyl methacrylate (PMMA) onto the $Mo_{0.91}W_{0.09}Te_2$ samples to act as an additional clamping layer, as well as an oxygen and moisture barrier. We have not observed degradation of the $MoTe_2$ and $Mo_{0.91}W_{0.09}Te_2$ samples during Raman or PL measurements on the time scale of days to weeks.

## 4.3 Optical Measurements of $Mo_{0.91}W_{0.09}Te_2$ and $MoTe_2$

### 4.3.1 Optical Measurement Details

The Raman spectroscopy measurements are performed with a commercial micro-Raman setup (Horiba Labram) in a backscattering geometry. A 100× objective (NA = 0.9) is used to collect the scattered photons, which are analyzed in a spectrometer equipped with a grating of 1800 lines/mm. The laser power on the samples is about 70 μW (for 532 nm excitation), 130 μW (for 633 nm excitation), and 200 μW (for 785 nm excitation), which is sufficient for obtaining a good signal-to-noise ratio. To ensure we do not damage the samples with these laser powers, we check the crystals optically for any visible damage between measurements and we also confirm that the intensities of the Raman peaks do not reduce over time. These measurements do not induce heating in the samples; we compare lower laser power measurements to higher laser power measurements to check for peak shifting which would imply heating.

The reflection contrast presented in Section 4.3.3 is calculated as $\Delta R/R = (R_{MoWTe2+substrate} - R_{substrate})/R_{substrate}$ where $R_{MoWTe2+substrate}$ and $R_{substrate}$ represent the reflectance of the thin $Mo_{0.91}W_{0.09}Te_2$ sample on the substrate and of the bare substrate, respectively. For a sample with sufficiently small absorbance on a thick transparent substrate, as in our case, we can determine the absorbance $\mathcal{A}$ of the unsupported thin $Mo_{0.91}W_{0.09}Te_2$ from $\Delta R/R$ as $\mathcal{A} = \frac{1}{4}(n_{substrate}^2 - 1)(\frac{\Delta R}{R})$ [216-218], where $n_{substrate}$ denotes the refractive index of the substrate [219]. We can thus probe the absorption spectra of sufficiently thin samples through measurements of their reflection contrast.

The reflection contrast setup consists of a quartz tungsten halogen source combined with a microscope using 100× objectives (NA = 0.95 and 0.9). The reflected light from the sample is dispersed by a monochromator onto a Peltier cooled Si or liquid-nitrogen cooled InGaAs CCD array. The peak positions and spectral widths (full width at half maximum) of the reflectance contrast measurements are extracted by fitting multiple Lorentzian line-shapes to the experimental data.

Photoluminescence (PL) measurements are performed in the same setup as reflection contrast with a 100× objective (NA = 0.95) to collect the backscattered emission. For excitation, we use a 633 nm (HeNe) or a 671 nm (solid-state) laser. The excitation power

level is around 10 μW. Backscattered laser radiation is suppressed by a long-pass filter in front of the monochromator.

The Raman measurements are performed on PDMS substrates, while the absorption and PL measurements are performed on PDMS and PETG substrates. All optical measurements are performed at room temperature and under ambient conditions.

### 4.3.2 Raman Spectroscopy of $Mo_{0.91}W_{0.09}Te_2$ and $MoTe_2$

We first perform Raman spectroscopy on $Mo_{0.91}W_{0.09}Te_2$ and $MoTe_2$ crystals exfoliated on polydimethylsiloxane (PDMS) substrates. Figure 4.3 and Figure 4.4 show the Raman spectra of 1L, bilayer (2L), trilayer (3L), four-layer (4L), and bulk $Mo_{0.91}W_{0.09}Te_2$ and $MoTe_2$ crystals for excitation wavelengths of 532 nm, 633 nm, and 785 nm. We note that the relatively small band gaps of ultrathin $MoTe_2$ and $Mo_{0.91}W_{0.09}Te_2$ (see Section 4.3.3) compared to other TMDCs enables the use of longer excitation wavelengths for resonant Raman spectroscopy [62,220,221]. We identify the following first-order Raman modes (zone-center phonons) in both materials: the out-of-plane $A_{1g}$ ($A_1'$ for odd, $A_{1g}$ for even layers), in-plane $E_{2g}^1$ ($E'$ for odd, $E_g$ for even layers), and out-of-plane $B_{2g}^1$ ($A_2''$ for 1L, $A_1'$ for odd, $A_{1g}$ for even layers), which is Raman inactive in 1L and bulk crystals [62,215,221-227]. For 1L $Mo_{0.91}W_{0.09}Te_2$, the $A_{1g}$ mode is at 172 $cm^{-1}$ and the $E_{2g}^1$ mode appears at 236 $cm^{-1}$. The weaker features at 200 $cm^{-1}$ and 345 $cm^{-1}$ have recently been attributed to second-order Raman processes [221] and appear to be stronger in $Mo_{0.91}W_{0.09}Te_2$ than in $MoTe_2$, possibly due to changes in the electronic structure with the addition of W.

After comparing the Raman spectra of the two materials, we observe that the $A_{1g}$ and $E_{2g}^1$ modes of $Mo_{0.91}W_{0.09}Te_2$ are slightly blueshifted and the $B_{2g}^1$ mode is slightly redshifted from those of $MoTe_2$ for 1L and 2L (see Table 4.1 for the Raman peak positions of both materials). We explain these observations as follows. Consider a simplified linear triatomic molecule model for which interlayer interactions in the 1L and 2L have little effect (*e.g.*, no splitting of the $E_{2g}^1$ mode). We then expect the increased W content in $Mo_{0.91}W_{0.09}Te_2$ to increase the effective mass of the transition metal atoms and to result accordingly in a redshift of modes compared to $MoTe_2$ [228]. This was reported for the $E_{2g}^1$ and $B_{2g}^1$ modes in alloys of Mo and W dichalcogenides (*e.g.*, $Mo_{1-x}W_xS_2$ and

$Mo_{1-x}W_xSe_2$) [229-233]. We observe this redshift in the $B_{2g}^1$ mode and the second-order Raman mode at 200 $cm^{-1}$. However, the frequency of the $A_{1g}$ mode depends more on bond strength than on mass of the transition metal, since this atom remains stationary in this vibrational mode [222]. Since W-Te bonds are stronger than Mo-Te bonds [234], adding W to $MoTe_2$ stiffens the bonds, leading, as in other TMD alloys [231-233], to a blueshift of the $A_{1g}$ mode. Interestingly, in contrast to other TMD alloys [230-233], we observe a blueshift of the $E_{2g}^1$ mode for 1L and 2L of the alloy compared to the $MoTe_2$ crystal. This blueshift also results from the increased bond strength, which apparently outweighs the influence of the increase in mass.

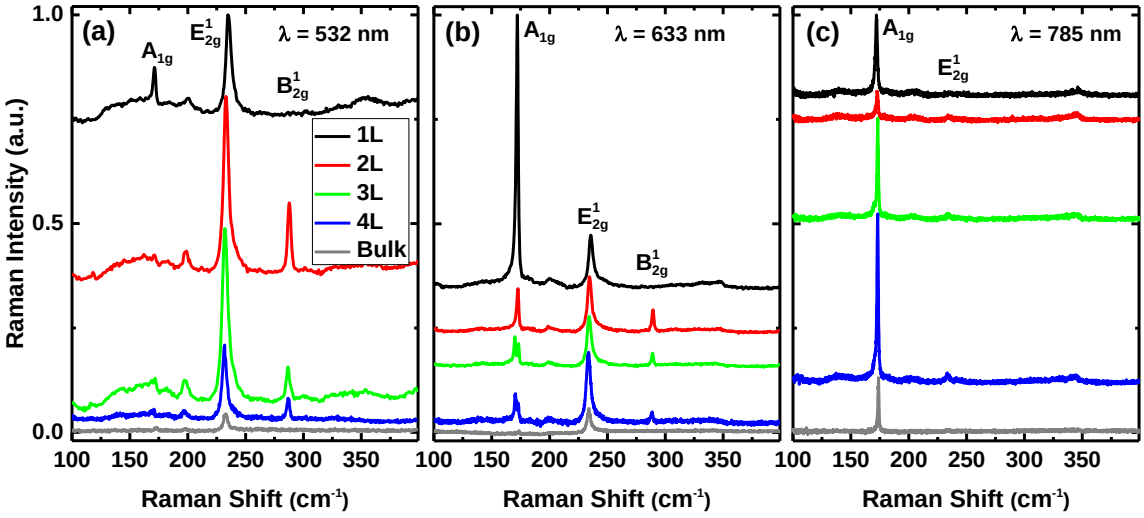


Figure 4.3: Raman spectra of 1L to 4L and bulk $Mo_{0.91}W_{0.09}Te_2$ (modes labeled according to bulk notation) for excitation wavelengths of (a) 532 nm, (b) 633 nm, and (c) 785 nm. The spectra are vertically offset for clarity.

Next, we examine the relative intensities of the Raman modes for different layer thicknesses in both materials. For 532 nm excitation, for both $MoTe_2$ and $Mo_{0.91}W_{0.09}Te_2$ crystals of all thicknesses, the $E_{2g}^1$ mode is stronger than all other modes. The $A_{1g}$ mode is strongest for 1L and becomes much weaker with increasing thickness (Figure 4.3a, Figure 4.4a). For 633 nm excitation, the $A_{1g}$ mode is enhanced compared to the $E_{2g}^1$ mode for 1L samples of both materials. We attribute the strength of this mode to a resonance effect associated with the excitation photon energy being close to that of the $A'$ or $B'$ excitons in the material (see Figure 4.5 for the $A'$ and $B'$ peak positions) [225,226]. For 2L crystals,

the $A_{1g}$ and $B_{2g}^1$ modes are comparable in intensity, but weaker than the $E_{2g}^1$ mode. For 3L and 4L crystals, the $A_{1g}$ mode splits into 2 peaks [$A_{1g}(R1)$ and $A_{1g}(R2)$], known as Davydov splitting [225,235], which are stronger than the $B_{2g}^1$ mode (see Figure 4.3b). The ratio of the $B_{2g}^1$ to $E_{2g}^1$ mode can also be used to identify thickness in few-layer crystals using both 532 and 633 nm excitation [202,223].

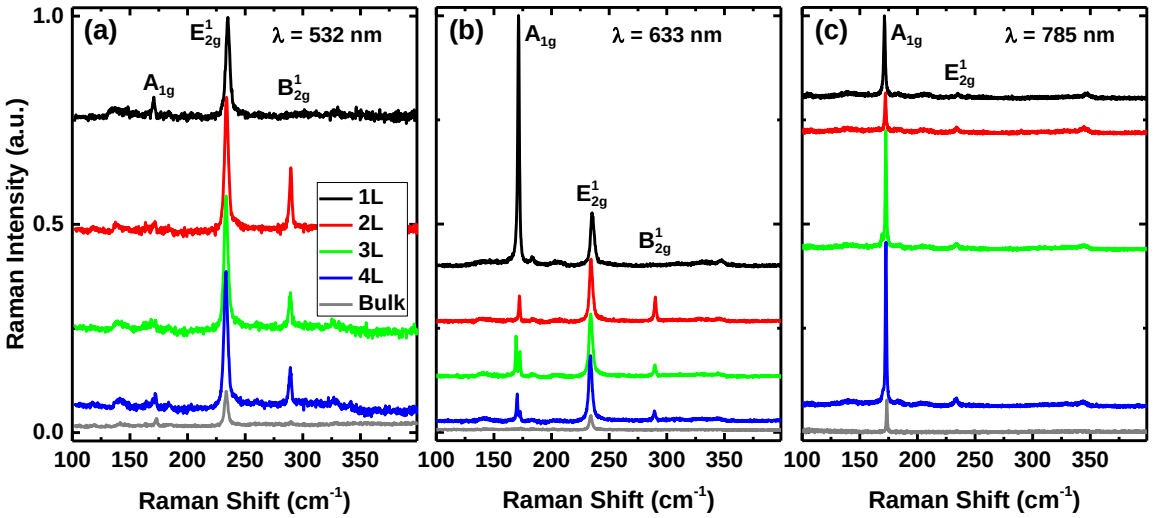


Figure 4.4: Raman spectra of 1L to 4L and bulk $MoTe_2$ (modes labeled according to bulk notation) using laser excitation wavelengths of (a) 532 nm, (b) 633 nm, and (c) 785 nm. The spectra are offset for clarity.

Using 785 nm excitation, we observe that the $E_{2g}^1$ mode is much weaker than the $A_{1g}$ mode for all layer thicknesses. For the thicknesses we have measured, the $A_{1g}$ mode is weakest for 2L and strongest for 4L crystals in both $Mo_{0.91}W_{0.09}Te_2$ and $MoTe_2$ (see Figure 4.3c and Figure 4.4c). The reason for this non-monotonic change of the intensity of the $A_{1g}$ mode with increasing thickness is unclear. The $B_{2g}^1$ mode does not appear in the 785 nm Raman spectra for any crystal thickness, as in the case of $MoS_2$ and $MoSe_2$ for excitation energies far from the $C$ electronic resonance (see Figure 4.5 for the $C$ peak position) [224,236]. Calculations have shown that the $A$ and $B$ excitons have wave functions that are mainly confined to the individual layers [224,236], and it has been predicted that for excitation energies near the $A$ and $B$ excitons, the active $B_{2g}^1$ mode of the few-layer crystals is inactive, as it is for 1L crystals. However, the wavefunction associated with the $C$ transition is calculated to be not confined to individual layers [237,238]. Hence, excitation

nearer to the $C$ feature, in this case 532 and 633 nm, yields Raman spectra with stronger $B_{2g}^{1}$ modes. The comparisons of the Raman spectra with three different excitation wavelengths presented here provides a rapid means of determining the thickness of ultrathin layers of $Mo_{0.91}W_{0.09}Te_2$ and $MoTe_2$.

Table 4.1: Raman peak positions of 1L and 2L $MoTe_2$ vs. $Mo_{0.91}W_{0.09}Te_2$ using laser excitation wavelengths of 532 nm, 633 nm, and 785 nm. All peak positions are in $cm^{-1}$. The modes are labeled according to the bulk notation.

| Wavelength of Laser | Mode | 1L | | 2L | |
|---|---|---|---|---|---|
| | | $MoTe_2$ | $Mo_{0.91}W_{0.09}Te_2$ | $MoTe_2$ | $Mo_{0.91}W_{0.09}Te_2$ |
| 532 nm | $A_{1g}$ | 171.5 | 171.8 | | |
| | $E^1_{2g}$ | 235.5 | 236.6 | 234.6 | 234.5 |
| | $B^1_{2g}$ | | | 290.3 | 289.3 |
| | | | | | |
| 633 nm | $A_{1g}$ | 171.0 | 171.8 | 171.7 | 172.5 |
| | $E^1_{2g}$ | 235.0 | 236.1 | 233.9 | 234.4 |
| | $B^1_{2g}$ | | | 289.5 | 289.1 |
| | | | | | |
| 785 nm | $A_{1g}$ | 171.3 | 172.2 | 172.2 | 172.8 |
| | $E^1_{2g}$ | 234.9 | | 234.3 | 234.6 |

### 4.3.3 Photoluminescence and Absorption Spectroscopy of $Mo_{0.91}W_{0.09}Te_2$

We have performed PL measurements to study the band structure of $Mo_{0.91}W_{0.09}Te_2$. Figure 4.5a displays the PL spectra of 1L to 4L and bulk $Mo_{0.91}W_{0.09}Te_2$ supported on PDMS substrates. We see that the PL intensity decreases, the peak position redshifts, and the spectral width (full width at half maximum) increases with increasing layer thickness. The 1L spectrum exhibits a single emission peak, with the maximum located at 1.10 eV and a width of 48 meV. The width of the 2L is 20 meV greater than that of the 1L. For the bulk, we find a much broader and weaker PL feature peaked at 0.98 eV.

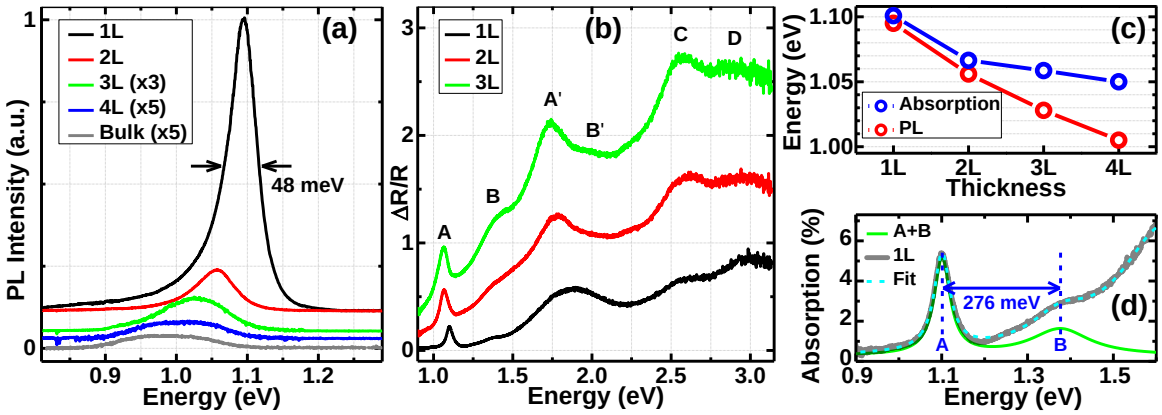


Figure 4.5: (a) PL spectra of 1L to 4L and bulk $Mo_{0.91}W_{0.09}Te_2$. 1L to 4L spectra are vertically offset for clarity. Black arrows indicate the width of 48 meV of the 1L spectrum. (b) Reflection contrast ($\Delta R/R$) spectra for 1L to 3L $Mo_{0.91}W_{0.09}Te_2$. (c) Comparison of the $A$ exciton and PL peak positions as a function of crystal thickness. (d) Absorption spectrum for the 1L in the near-IR, shown in terms of absorption for a free-standing layer. The green curve shows the contributions of the $A$ and $B$ excitons to the spectrum based on a fit (dotted line) to the experimental data.

In order to comment on the nature of the peaks observed in the PL spectra and understand the changes with increasing material thickness, we have also measured the reflection contrast ($\Delta R/R$) spectra of 1L to 3L $Mo_{0.91}W_{0.09}Te_2$ on PDMS substrates, as displayed in Figure 4.5b, to probe their absorption spectra (see Section 4.3.1 for details on the reflection contrast measurements). We expect to observe only direct optical transitions in the reflection contrast spectrum since the indirect transitions produce only weak contributions to the absorption spectrum. Several features are observed in the spectra of Figure 4.5b, and we expect them to arise from mechanisms similar to those in $MoTe_2$. Thus, we have labeled them according to the bulk assignments of Wilson and Yoffe [49] as was previously done for the case of $MoTe_2$ [62]. These spectroscopic features are associated with transitions in different parts of the Brillouin zone of $Mo_{0.91}W_{0.09}Te_2$. The $A$, $B$ and $A'$, $B'$ pairs have been identified as excitonic transitions with the $A$-$B$ splitting arising from spin-orbit interactions [49,76]. As for other TMD monolayers, the $A$ and $B$ peaks are assigned to excitonic peaks associated with the lowest direct optical transition at the $K$-point [239-241]. The $C$ and $D$ features have been attributed to regions of parallel bands near the $\Gamma$ point of the Brillouin zone of bulk $MoTe_2$ [242] and to similar parallel bands in monolayers of other TMDs [237,243].

We now compare the PL and reflection contrast response of $Mo_{0.91}W_{0.09}Te_2$ for different thicknesses. Figure 4.5b shows that the reflection contrast increases and the *A* exciton redshifts with increasing thickness. The PL spectra in Figure 4.5a show that the peak position also redshifts; however, the rate of the redshift of the PL peak is faster than that of the *A* exciton and the intensity of the PL peak decreases as opposed to that of the *A* exciton. We report the position of the *A* exciton and the PL peak position as a function of thickness in Figure 4.5c. The *A* exciton redshifts by 33 meV to 1.067 eV from 1L to 2L and continues shifting gradually with increasing thickness. However, the PL peaks redshift more than the *A* exciton peaks; the two peaks are separated by 5 meV for 1L, but by 45 meV for 4L.

We attribute this large difference in the shift between the absorption and emission features to the emergence of an indirect transition at lower energies than the *A* exciton with increasing thickness, as observed in other semiconducting TMDs [244,245]. We expect the indirect band gap to contribute to PL, but not significantly to the absorption spectrum. We thus conclude that 1L $Mo_{0.91}W_{0.09}Te_2$ exhibits a direct band gap, unlike the crystals thicker than 2L, in accordance with the behavior of its $MoTe_2$ counterpart. The PL intensity of the 1L crystal is about three orders of magnitude greater than that of the bulk, due to the direct optical gap transition of the former. Even though the PL intensity is significantly weaker for 2L than it is for 1L, since the PL peak and the *A* exciton are separated by only 10 meV, the assignment of the 2L material as indirect gap is unclear. However, the 20 meV increase in the width of the PL and *A* exciton peaks of 2L as compared to 1L strongly indicates the presence of a scattering channel for the *A* exciton in the 2L. We also note that there have been different opinions on the nature of the 2L $MoTe_2$ band gap, both at room [62,203] and low temperatures [202].

The near-IR part of the 1L absorption spectrum is shown in greater detail in Figure 4.5d. We find that the *A* and B features are located at 1.10 eV and 1.38 eV, respectively. The corresponding features appear at similar energies of 1.10 eV and 1.35 eV, respectively, for 1L $MoTe_2$ [62]. We note that the direct gap, or *A* exciton, position in $Mo_{0.91}W_{0.09}Te_2$ is not very different from that of $MoTe_2$, which is compatible with the fact that for a given chalcogen (S, Se), the band gaps of Mo and W dichalcogenides are quite similar [220]. The *A*-*B* splitting for 1L is found to be 276 meV, which is slightly greater than the $MoTe_2$ value

of 250 meV [62]. We attribute this increase to the presence of W, since dichalcogenides of W have significantly higher $A$-$B$ splitting than those of Mo [220,246,247]. Thus, our PL and reflection measurements have revealed that 2H $Mo_{0.91}W_{0.09}Te_2$ is a semiconducting material like 2H $MoTe_2$.

## 4.4 Strain-Dependent Measurements of 1L $Mo_{0.91}W_{0.09}Te_2$ and $MoTe_2$

To gain further insight into the band structure of 1L $MoTe_2$ and $Mo_{0.91}W_{0.09}Te_2$, we perform strain-dependent PL measurements on these materials. After the exfoliation and transfer processes, as explained in Section 4.2.4, we pattern metal strips by electron beam (e-beam) lithography and deposit 10 nm Cr/30 nm Ag by e-beam evaporation onto the crystals to clamp them to the substrate, as shown in Figure 4.6a-b. We apply uniaxial in-plane tensile strain to a flexible substrate using a two-point bending apparatus. The strain, $\epsilon$, is calculated as $\epsilon = \tau/(2R)$, where $\tau$ = 250 μm is the thickness of the PEN and $R$ is the radius of curvature of the bent substrate, determined from photos taken at each strain level (Figure 4.6c). We use PEN or PETG substrates for the optical measurements on the bending platform with strain due to their high Young's moduli of ~5 GPa [248,249].

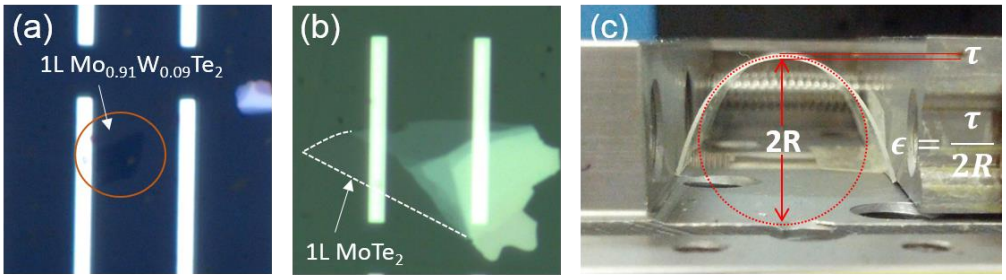


Figure 4.6: Optical image of (a) $Mo_{0.91}W_{0.09}Te_2$ and (b) $MoTe_2$ clamped to PEN with metal strips. (c) Two-point bending apparatus used for applying tensile strain. The strain is calculated from the formula shown, with the radius of curvature determined from the photo taken at each strain level.

Figure 4.7a-b shows the PL measurements of 1L $Mo_{0.91}W_{0.09}Te_2$ and $MoTe_2$ as a function of strain. As the strain increases, the PL peak redshifts, corresponding to a decrease in the band gap. For $Mo_{0.91}W_{0.09}Te_2$, the PL peak shifts from 1.09 eV at 0% strain to 1.02 eV at 2.3% strain or -30 meV/% strain. For $MoTe_2$, the PL peak shifts from 1.08 eV at 0% strain to 1.01 eV at 2.1% strain or -33 meV/% strain. The widths of the $Mo_{0.91}W_{0.09}Te_2$ and $MoTe_2$ PL peaks decrease from 63 meV and 59 meV, respectively, at

0% strain to minimum values of 49 meV and 42 meV, respectively, with strain. Figure 4.7c shows how the 1L $MoTe_2$ PL peak energy and spectral widths vary with strain.

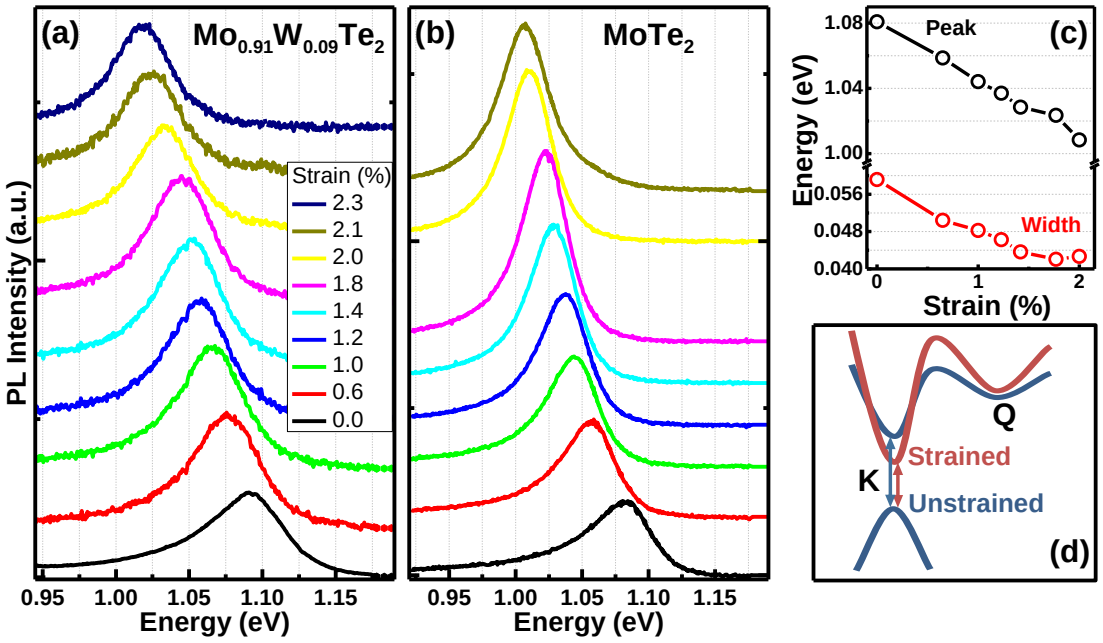


Figure 4.7: PL spectra of 1L (a) $Mo_{0.91}W_{0.09}Te_2$ and (b) $MoTe_2$ under different amounts of uniaxial tensile strain. All spectra are vertically offset for clarity. (c) The dependence of the peak energy and spectral width of 1L $MoTe_2$ on strain. (d) Schematic band structure of strained and unstrained 1L $MoTe_2$, showing changes in the energy separation between the minima of the $K$ and $Q$ valleys in the conduction band.

To account for the unexpected decrease of the width of the emission peak in the PL spectra with increasing strain for both materials, we can identify three possible factors: 1) the contribution to PL from trions is suppressed, 2) the material conforms better to the flexible substrate (after being transferred), reducing inhomogeneous broadening, or 3) exciton-phonon scattering is partially suppressed.

We first consider the suppression of trion emission due to strain. Trions are not expected to contribute much to absorption unless the sample is heavily doped [250,251]. However, trions can still contribute appreciably to PL since they are more stable even at room temperature due to their high binding energy of about 25 meV [204,205]. Therefore, if suppression of trion PL caused the reduction in the linewidth, we would not expect to see a parallel narrowing in the absorption feature with strain. However, our measurements show a similar decrease in the width of the absorption and PL features, thus ruling out this

mechanism. Figure 4.8 shows strain-dependent absorption and PL of 1L $Mo_{0.91}W_{0.09}Te_2$ and Figure 4.9 shows the extracted peak energy and linewidths of the absorption and PL spectra corresponding to Figure 4.8.

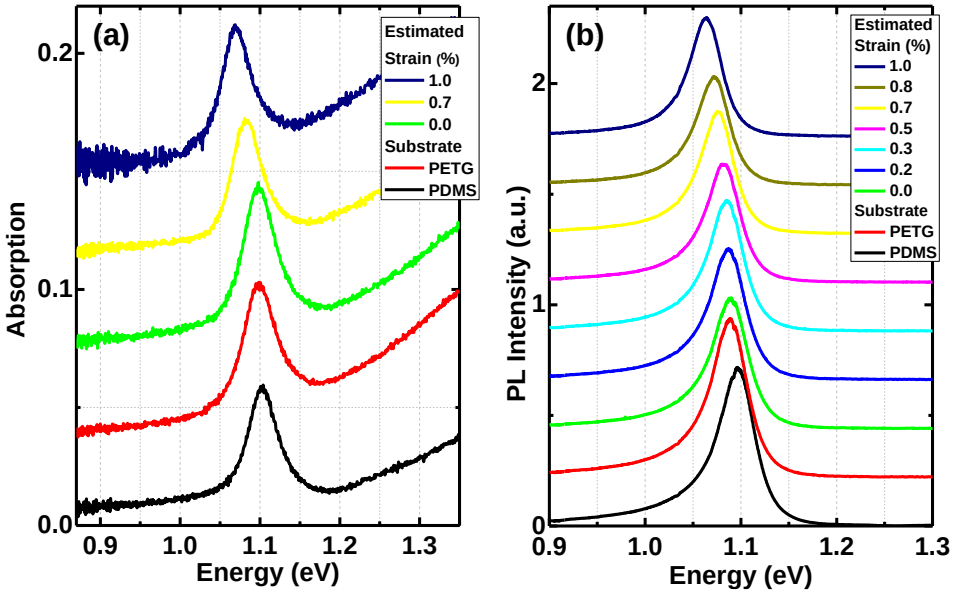


Figure 4.8: Strain-dependent (a) absorption and (b) PL measurements of 1L $Mo_{0.91}W_{0.09}Te_2$ on PDMS (as-exfoliated, before transferring onto PETG), on PETG (after transfer) and with increasing strain. The spectra are vertically offset. Intensities of the measurements on PDMS were adjusted to match the PETG due to their different refractive indices which result in different electric field enhancement on their surfaces.

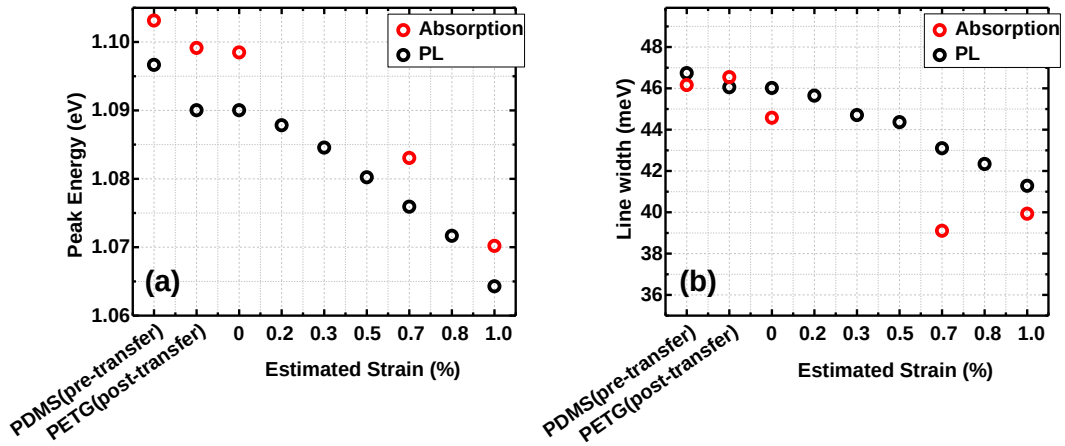


Figure 4.9: (a) Peak energy and (b) line widths of absorption and PL spectra corresponding to Figure 4.8.

Second, we consider the possibility that the material conforms better to the substrate under strain, leading to a reduction of inhomogeneous broadening. We first observe that the width of the emission feature of strained 1Ls drops to a value as low as 42 meV (Figure 4.7c), which is less than that of any as-exfoliated samples (for which the width is around 47-50 meV) [62,203]. Further, similar measurements on 1L $WSe_2$ by Schmidt *et al.* have demonstrated that the strain-induced narrowing of the spectral widths is reversible upon the release of strain [252]. This observation suggests that the elimination of inhomogeneities alone cannot account for line narrowing in their case, as the inhomogeneities are not expected to recover fully when the strain is released. Hence, we do not expect this mechanism to explain our observations.

Third, we consider the effect of strain on the exciton-phonon coupling. As we know from the current and earlier studies, 1Ls of both materials have direct optical gaps [62,202,203,253]. However, the 1L has an indirect transition at a slightly higher energy than that of the $A$ exciton, which is known from band structure calculations and from extrapolating the energy of the indirect gap as compared to that of 2L and thicker crystals [62,202,203,253]. Moreover, the energy separation between the minima of indirect $Q$ (also known as $T$) [254,255] and direct $K$ valleys, $\Delta E_{QK}$, in the conduction band will increase with uniaxial (as well as biaxial) strain in similar material systems [207,208,256-258]. This is illustrated in Figure 4.7d, which shows a schematic band structure of strained and unstrained 1L $MoTe_2$. However, scattering of an electron from the $K$ to $Q$ valley requires the absorption of a phonon. This becomes less likely with increasing $\Delta E_{QK}$. Therefore, we infer from our results that a weakening in the exciton-phonon intervalley scattering is mainly responsible for the decrease in the spectral linewidths.

Figure 4.9b shows that the spectral linewidths at 0.0% and 1.0% strain are about $\Gamma(\epsilon = 0.0\%)$ = 47 meV and $\Gamma(\epsilon = 1.0\%)$ = 41 meV, respectively. The change in linewidth is then $\Delta\Gamma$ = 6 meV. If we express the total linewidth, $\Gamma$, as follows:

$$\Gamma = \Gamma_{rad} + \Gamma_{K-Q} + \Gamma_{K-K} \quad (6)$$

where $\Gamma_{rad}$, $\Gamma_{K-Q}$ and $\Gamma_{K-K}$ are contributions to the linewidth broadening due to the radiative decay, exciton-phonon intervalley scattering from $K$ to $Q$ valley, and intravalley scattering within the $K$ valley, respectively [219,259]. Assuming $\Gamma_{rad}$ and $\Gamma_{K-K}$ change

only insignificantly with 1% strain, we conclude that $\Gamma_{K-\mathrm{Q}}$ is larger than about 6 meV [260]. Therefore, an upper limit on the lifetime of the exciton-phonon scattering from $K$ to $Q$ of 1L $MoTe_2$ and $Mo_{0.91}W_{0.09}Te_2$, $\tau_{K-\mathrm{Q}}$, can be estimated as follows:

$$\tau_{K-Q} = \frac{\hbar}{\Gamma_{K-Q}} \lesssim 110\ fs \tag{7}$$

The ability to suppress phonon absorption indicates that $Q$ and $K$ states are within a few times the phonon energy and the highest energy phonon to mediate such scattering [the $LO(E')$ mode] is about 30 meV [221,254,261]. Thus, we predict that $\Delta E_{QK}$ of the unstrained 1Ls is not much larger than 30 meV. We expect the linewidth narrowing effect via tensile strain to be smaller (larger) for $MoS_2$ ($WSe_2$ and $WS_2$), for which $\Delta E_{QK}$ is predicted to be larger (smaller) than that in $MoTe_2$ [254,261].

Here we note an advantage of a strain-dependent study over a temperature-dependent one. Strain, like temperature, can modify the band structure, but in the former case without significantly affecting the population of phonons. We also note that it is typically assumed that the relative energy of different valleys is not affected by temperature. This is not always correct as lowering the temperature has a similar effect to biaxial compressive strain [262]. Therefore, tuning the bands of nearly direct or indirect gap semiconductors via strain will provide more insight about the band structure and can help interpret the temperature-dependent studies on the spectral linewidths of TMDs [204,252,259,263].

Finally, we would like to consider the implications of weaker exciton-phonon scattering for electron transport. There have been calculations of the enhancement of transport properties in group VI TMDs due to the change in the relative energies of $K$ and $Q$ valleys in the conduction band under tensile strain, leading to a reduction in electron-phonon scattering [207,264]. We propose that this effect should be larger for $MoTe_2$ than $MoS_2$, as the former has a smaller value for $\Delta E_{QK}$. A similar phenomenon has been exploited to enhance the electron mobility of silicon transistors, where the intervalley energy separation increases with tensile strain, leading to reduced intervalley electron-phonon scattering [265,266].

## 4.5 Comparison of Electrical Transport of $Mo_{0.91}W_{0.09}Te_2$ and $MoTe_2$

We have also performed preliminary electron transport measurements of few-layer (3-12 nm) $MoTe_2$ and $Mo_{0.91}W_{0.09}Te_2$ transistors to compare their electrical properties. All devices have channel lengths of ~1 μm, Au source/drain contacts, 90 nm $SiO_2$/Si ($p^{++}$) back gates, and 20 nm aluminum oxide ($AlO_x$) capping layers (see Figure 4.10a for a schematic of the devices). Figure 4.10b-c shows comparisons of their drain current ($I_D$) vs. gate voltage ($V_G$) transfer curves. Without accounting for contact resistance, the estimated field-effect mobilities of the $MoTe_2$ transistors are $\mu_{FE}$ ~32 $cm^2/(Vs)$ and ~26 $cm^2/(Vs)$, and for $Mo_{0.91}W_{0.09}Te_2$ transistors $\mu_{FE}$ ~24 $cm^2/(Vs)$ and ~20 $cm^2/(Vs)$. The $MoTe_2$ transistors tend to have higher maximum drive currents at $V_G$ = 30 V, despite slightly higher threshold voltages (see Figure 4.10b-c). However, given differences in thickness and variability in contact resistance (well-known with TMDC transistors) [51], it is difficult to determine whether $Mo_{0.91}W_{0.09}Te_2$ has poorer transport properties compared to $MoTe_2$; such sample-to-sample variation can be seen even among nominally "identical" TMDC transistors. Further measurements must be performed on $Mo_{1-x}W_xTe_2$ devices with multiple channel lengths, contact metals, and compositions to draw more definitive conclusions and to exclude any differences stemming from device-to-device variation.

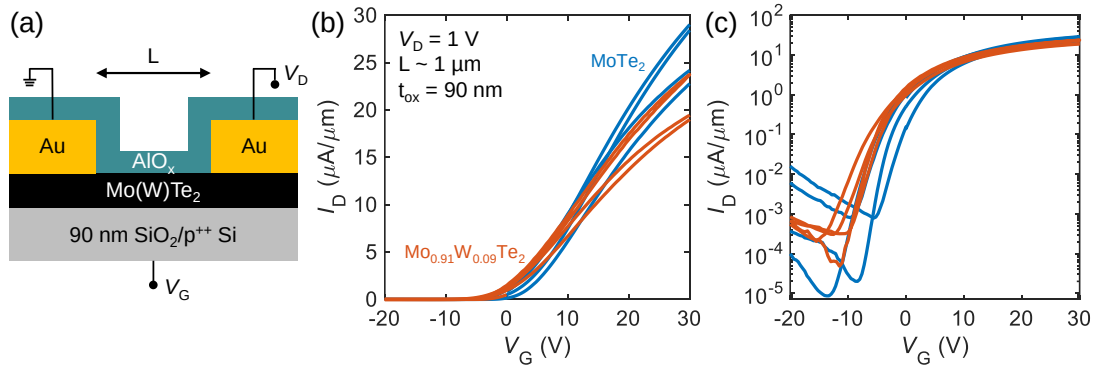


Figure 4.10: (a) Device cross-section diagram. (b) Linear and (c) log scale plots showing measured drain current ($I_D$) vs. gate voltage ($V_G$) transfer curves of two few-layer $Mo_{0.91}W_{0.09}Te_2$ (red) and two few-layer $MoTe_2$ (blue) transistors with channel lengths of ~1 μm. The double curves show the forward and backward $I_D$-$V_G$ sweeps.

## 4.6 Conclusion

In summary, we have characterized single crystal 2H $Mo_{0.91}W_{0.09}Te_2$ down to monolayer thickness with photoluminescence, absorption, and Raman spectroscopy. We

have determined that atomically thin 2H $Mo_{0.91}W_{0.09}Te_2$ is a semiconductor with similar optical properties to $MoTe_2$; the monolayer possesses a direct optical band gap at 1.10 eV, and the thicker layers become indirect. The presence of W in the alloy alters the band structure, as observed by absorption measurements, and can be studied further by Raman spectroscopy, particularly using resonant excitation [267]. Given that this alloy is closest in W-content to the 2H to 1T' phase transition [215], it may be a promising material for phase-change memory applications. We have manipulated the band structure of monolayer $MoTe_2$ and $Mo_{0.91}W_{0.09}Te_2$ via tensile strain up to 2.3% and have lowered the optical band gap of these materials to near 1 eV. We have thus extended the optical range of group VI TMD monolayers further into the near-infrared (NIR) region. We have also observed that the relative energy separation between valleys changes with strain, and that exciton-phonon intervalley scattering can also be manipulated in this fashion. We attribute the reduced spectral linewidth of the $A$ exciton under tensile strain to a decrease in the rate of exciton-phonon scattering. This suggests a corresponding decrease in the electron-phonon scattering rate and a potential improvement in the electrical transport properties in these materials with tensile strain.

# Chapter 5

# Strain Engineering of 1L $MoS_2$ Transistors

## 5.1 Introduction

Transition metal dichalcogenides (TMDs) have gained interest for electronic and optoelectronic devices due to their atomically thin nature and pristine interfaces that lack dangling bonds [38]. Molybdenum disulfide ($MoS_2$) is particularly promising because of its high-quality monolayer (1L) film growth [53], stability [52], and good n-type electrical performance due to Fermi level pinning near the conduction band [50,51]. However, the electrical properties, including drive current, mobility, and contact resistance, of $MoS_2$ and other TMD-based devices must be improved for them to compete with existing technologies based on silicon. Many techniques have been implemented to improve the electrical properties of TMD-based transistors such as contact engineering [50,51,94] and channel doping [54,84-86], and strain engineering has been proposed as another method to improve performance.

Strain engineering has been used to improve the current and mobility in silicon metal oxide semiconductor field-effect transistors (Si MOSFETs) since the 90 nm technology node [12-14]. In Si FETs, uniaxial compressive strain to pMOS transistors is realized through selective growth of silicon germanium (SiGe) at the source and drain regions, while nMOS transistors achieve uniaxial tensile strain via nitride encapsulation layers [13,14]. Reduced electron effective mass and scattering due to band splitting in the conduction band, and reduced hole effective mass due to band warping in the valence band lead to enhanced mobility with strain [13,14,268]. Experimental and theoretical studies have shown that strain can also modify the band structure and phonon dispersion of TMDs [77,87,89,106,107,257,258,269-276]. Strain engineering is promising for TMDs because they are extremely sensitive to external perturbations and can withstand much higher strains than bulk materials, suggesting their suitability for applications in flexible electronics [78,103].

In particular, tensile strain has been predicted to improve the electrical properties of $MoS_2$ transistors. Tensile strain results in changes to the band structure, affecting the band gap, energy minima and separation between valleys, and carrier effective masses, which can lead to improved mobility and drive current [258,269,271,272]. However, most studies to date have focused on optical measurements such as photoluminescence and Raman spectroscopy of $MoS_2$ with strain, reporting changes in optical band gap and phonon mode energies [77,270,274,277-279]. Some studies have also shown measurements of two-terminal devices based on $MoS_2$ as a function of strain, utilizing the piezoresistive property of $MoS_2$ for strain sensing applications [106-110]. Few studies have experimentally demonstrated electrical measurements of $MoS_2$ transistors as a function of strain [257,273,280,281], and none have reported improvements in mobility due to strain in 1L $MoS_2$.

In this work, we study the effect of uniaxial tensile strain on the electrical performance of 1L $MoS_2$ transistors fabricated on flexible substrates. We use Raman spectroscopy to verify the amount of applied strain, and photoluminescence (PL) spectroscopy to measure the change in the optical band gap of $MoS_2$. We demonstrate an improvement in field-effect mobility ($\mu_{FE}$) and drain current ($I_D$) up to 2x with ~0.7% applied strain, representing the largest improvement in electrical performance for a TMD using strain to date. Finally, we show that these transistors could be useful as strain sensors because they have voltage-dependent gauge factors up to 200, larger than most conventional strain sensors based on bulk materials and most 2D-based strain sensors.

## 5.2 Device Fabrication and $MoS_2$ Transfer Process

### 5.2.1 Fabrication of 1L $MoS_2$ Transistors

We fabricate transistors with local back-gates on polyethylene naphthalate (PEN), a flexible and transparent plastic substrate. The steps described for fabricating our $MoS_2$ transistors are depicted in Figure 5.1, with schematics included for each step in the process. First, we define Cu (28 nm)/Au (5 nm) back-gates by optical lithography and deposit them via electron beam (e-beam) evaporation. Then, we deposit ~20 nm aluminum oxide ($Al_2O_3$) as the gate dielectric by atomic layer deposition (ALD) using a Savannah S200 from Cambridge Nanotech with trimethyl alumina (TMA) and $H_2O$ as precursors, for 200 cycles.

The temperature of the chamber during deposition is 130 °C due to the thermal limitation of our substrates.

Next, we transfer 1L molybdenum disulfide ($MoS_2$), grown by chemical vapor deposition (CVD) on $SiO_2$/Si substrates [53], onto the $Al_2O_3$ using a polymer-assisted transfer process [102] (see Section 5.2.2 for details on the transfer process). Au (55 nm) contacts are then defined and e-beam evaporated to form the source and drain of the transistors. We also define and evaporate Ti (3 nm)/Cu (30 nm)/Au (5 nm) pads connected to the Au contacts for device probing. Finally, the $MoS_2$ is patterned and etched into rectangles to form the channels using a gentle $O_2$ plasma in a Drytek2 chamber at 150 mtorr with 100 sccm $O_2$ at a power of 50 W for 45 seconds. Figure 5.2a-b shows a schematic and top-down optical image of one of the $MoS_2$ transistors with staggered geometry (i.e. gate under the channel and source and drain contacts above the channel). The triangles observed in the optical image of Figure 5.2b are bilayer (2L) $MoS_2$ regions [53]. The transparency of the sample is evident in Figure 5.2c, where the green color in the white box corresponds to the transferred $MoS_2$ film.

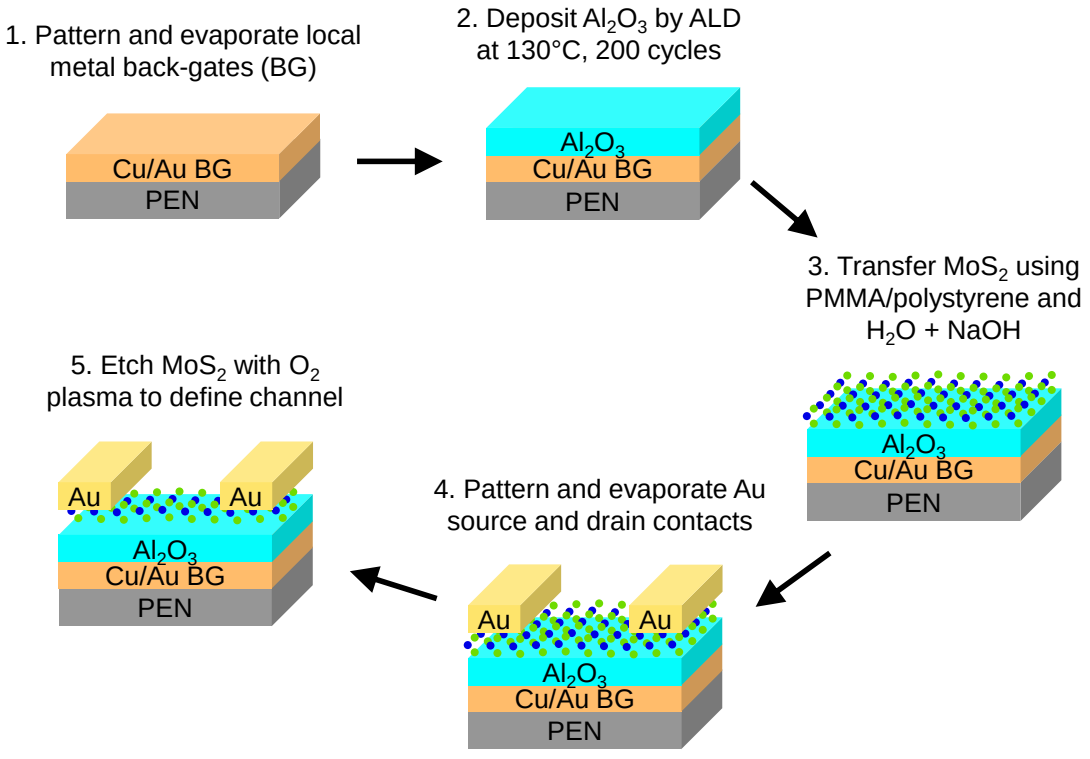


Figure 5.1: Summary of steps used to fabricate $MoS_2$ transistors on flexible substrates.

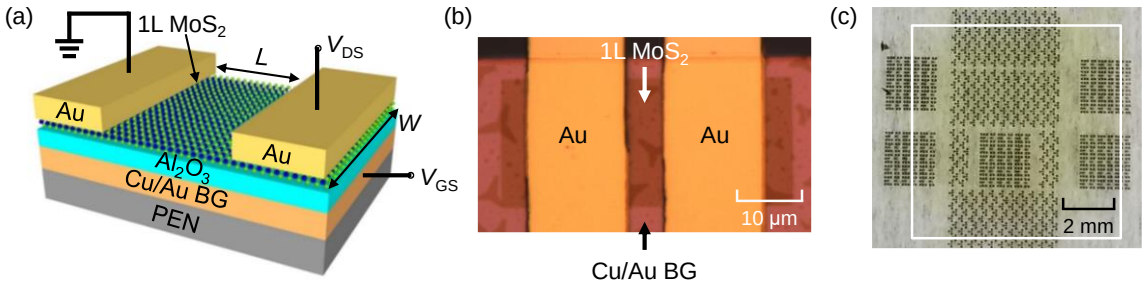


Figure 5.2: (a) Schematic of local back-gated (BG) monolayer (1L) $MoS_2$ transistor on a polyethylene naphthalate (PEN) flexible substrate, with Au source/drain contacts and an $Al_2O_3$ gate dielectric. (b) Top-view optical image of 1L $MoS_2$ device with a length ($L$) of 8 μm and width ($W$) of 20 μm. (c) Picture of sample (on a cleanroom wipe) taken after fabrication was completed, with the green color within the white box corresponding to the transferred $MoS_2$ film.

### 5.2.2 $MoS_2$ Transfer Process

We describe the steps used to transfer $MoS_2$ grown by CVD onto polyethylene naphthalate (PEN) substrates as follows.

1. Place thin strips of tape (Nitto Denko RevAlpha series thermal release tape or Kapton) on all four edges of sample with $MoS_2$ grown by CVD on $SiO_2$/Si substrate.
2. Spin-coat 2% PMMA at 2500 rpm for 1 minute and bake for 45 seconds at 135 °C.
3. Spin-coat polystyrene (PS) dissolved in toluene (PS/toluene 3 g/20 mL) at 2000 rpm for 1 minute, and then bake for 5 minutes at 85 °C.
4. Remove tape very carefully from edges of sample.
5. Place $MoS_2$ sample with polymer support layers in a beaker of water. Agitate sample in water to cause delamination of $MoS_2$/polymer stack from growth substrate. Use tweezers to poke edges of the polymer stack to initiate delamination from substrate.
6. If $MoS_2$/polymer stack does not delaminate in water, place sample in a beaker of 1M NaOH for a few minutes to etch $SiO_2$ and promote delamination. After the $MoS_2$/polymer stack begins to delaminate from the substrate, return the sample to a fresh beaker of water. Return to step 5 until the entire sample has delaminated from the substrate.
7. After $MoS_2$/polymer stack has delaminated from the growth substrate, it will float on the water. Use the PEN (or another target substrate) to pick up the floating sample.

8. Carefully blow a $N_2$ gun perpendicular to the sample to remove water trapped between the $MoS_2$ and new substrate.
9. Place the sample on a hot plate at 55 °C for 5 minutes, then increase the temperature to 85 °C and heat the sample for 5 minutes, and finally increase the temperature to 135 °C. This gradual increase in temperature is to minimize damage (e.g. bubbles and holes) to the 1L after the transfer. When the temperature reaches 135 °C, remove the sample from the hot plate.
10. Place the transferred $MoS_2$ sample in toluene for 12 hours to dissolve the polymers. Rinse the sample in acetone and IPA after removing it from toluene.

## 5.3 Optical Measurements of 1L $MoS_2$ with Strain

### 5.3.1 Raman Spectroscopy of Devices

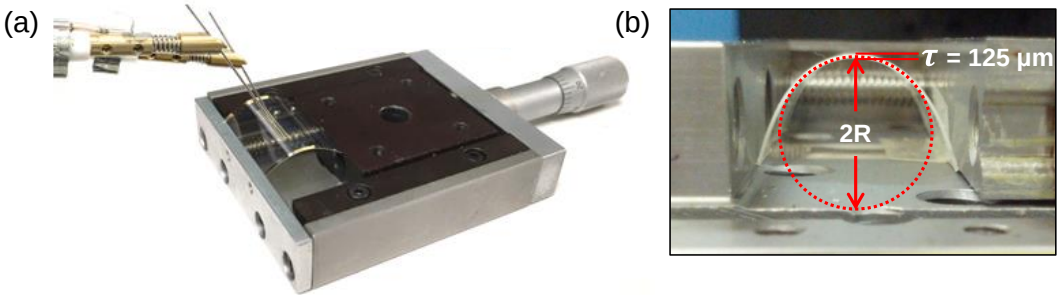


Figure 5.3: (a) Two-point bending apparatus for applying tensile strain to the flexible substrates, illustrating the probes used for electrical measurements. (b) Image of bent substrate which is used to calculate amount of applied strain $\varepsilon = \tau/(2R)$, where $\tau$ is the thickness of the substrate and $R$ is the radius of curvature of the bent substrate.

We apply strain to our $MoS_2$ transistors using a two-point bending apparatus and by controlling the distance between the two ends of the substrate, as shown in Figure 5.3a. The equation used to estimate strain ($\varepsilon$) is $\varepsilon = \tau/(2R)$, where $\tau$ is the thickness of the PEN substrate (125 μm) and $R$ is the radius of curvature of the bent substrate (see Figure 5.3b) [282]. The amount of strain applied to the $MoS_2$ is confirmed via Raman spectroscopy. The E' peak ($E^1_{2g}$ for bulk) at ~384 $cm^{-1}$ corresponds to an in-plane vibrational mode, and the $A_1$' ($A_{1g}$ for bulk) peak at ~403 $cm^{-1}$ corresponds to an out-of-plane vibrational mode [283,284]. Tensile strain increases the bond lengths and weakens the bonds, leading to a softening of the phonon modes and thus a redshift in the corresponding Raman peak

[77,87,276,282]. The peak shift of the E' mode is much larger than that of the $A_1$' mode, because in-plane strain affects the in-plane more than the out-of-plane Raman modes [77,106,270,274]. We are unable to conclude if the $MoS_2$ after device fabrication initially has built-in tensile or compressive strain from the growth and transfer processes, because $Al_2O_3$ and Au are both known to cause peak shifts in the Raman and PL spectra of $MoS_2$ [285-287].

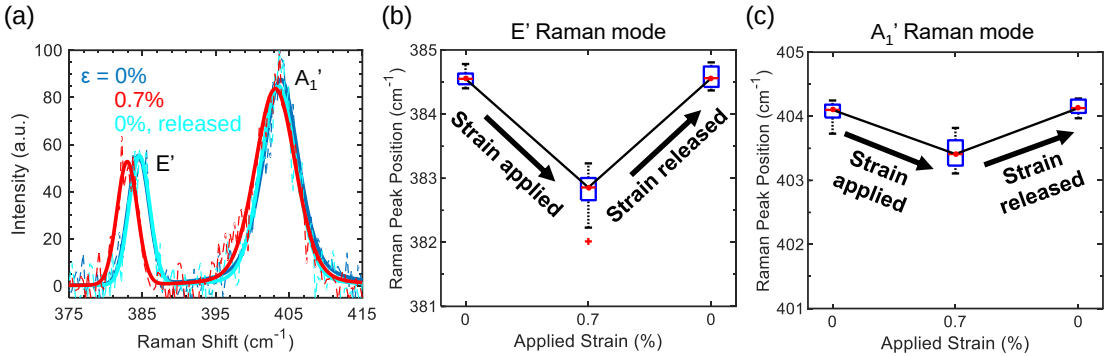


Figure 5.4: (a) Raman spectra of the device from Figure 5.2b at different levels of strain. The E' Raman peak redshifts with strain and returns to its initial position upon release of strain. Box plots showing (b) E' and (c) $A_1$' Raman peak positions of 10 devices. The figures include data averaged from ~5 spots across the channels of all devices and show Raman peak positions before applying strain, with 0.7% strain, and after the strain returns to 0%.

Figure 5.4a shows the Raman spectra of the $MoS_2$ device from Figure 5.2b without applied strain (blue) and with ~0.7% tensile strain (red). We perform Raman measurements on four locations across the channel of the device but only include one representative spectrum at each strain level here for clarity. The data are fit to a superposition of Lorentzian and Gaussian peaks. The E' peak clearly redshifts with ~0.7% applied tensile strain. The positions of the E' peaks without and with applied strain are 384.6 ± 0.3 $cm^{-1}$ and 383.0 ± 0.2 $cm^{-1}$, respectively. This corresponds to a peak shift of ~2.3 ± 0.2 $cm^{-1}$/% strain, which is comparable to that of other studies [106,270,288]. The cyan curve, representing the measurement after strain is released, matches very well with the initial 0% (blue) curve. As expected, the peak shift in the $A_1$' Raman peak is much lower (1.0 ± 0.3 $cm^{-1}$/% strain) than that of the E' peak. This shift may be partially due to altered substrate interactions rather than purely a direct strain effect on the out-of-plane bonds [285].

Figure 5.4b-c illustrates the E' and $A_1$' peak position data for 10 devices. The data are presented as box plots for 0%, 0.7%, and back to 0% strain. For each device, we averaged the Raman peak positions over ~5 spots in the channel region. The average E' peak position across all 10 devices after device fabrication, with 0.7% strain, and after the strain is released is ~384.6 ± 0.1 $cm^{-1}$, ~382.8 ± 0.4 $cm^{-1}$, and ~384.6 ± 0.2 $cm^{-1}$, respectively. We note that some studies report peak splitting of the degenerate E' Raman mode with tensile strain due to breaking the symmetry of the crystal [77,274]. Our samples did not exhibit such behavior in the Raman spectra, likely because the $MoS_2$ did not experience large enough strains.

### 5.3.2 Photoluminescence (PL) Spectroscopy of Devices

We also perform photoluminescence (PL) spectroscopy as a function of strain on our $MoS_2$ devices. Figure 5.5a displays the PL spectra of the $MoS_2$ device from Figure 5.2b at 0% (blue), 0.4% (magenta), 0.6% (red), and back to 0% strain (cyan). The experimental data and fits to the data using Lorentzian distributions are included in the plot. The A exciton peak observed at ~1.8 eV arises due to the lowest energy transition at the *K*-point in the conduction and valence bands [49,76]. The weaker peak at ~2 eV is due to the B exciton, which arises from spin-orbit splitting in the valence band [49,76]. Figure 5.5b displays a schematic band diagram of 1L $MoS_2$ with the A and B transitions. As expected, the A exciton, which corresponds to the energy of the optical band gap of $MoS_2$, redshifts with strain because of a decrease in the optical band gap (see Figure 5.5a). This reduction in band gap results from increased interlayer atomic distance, which changes the superposition of atomic orbitals and the energy states [78,87,275,289]. The A exciton peak positions at 0%, 0.4%, 0.6%, and back to 0% strain are 1.810 ± 0.006 eV, 1.790 ± 0.004 eV, 1.772 ± 0.004 eV, and 1.811 ± 0.005 eV, respectively. Therefore, the peak shift of the A exciton peak is ~63 ± 10 meV/% strain for this device. This is similar to that of other experimental studies demonstrating PL of $MoS_2$ with strain [77-79].

Figure 5.5c shows the position of the A exciton peak at 0%, 0.4%, 0.6%, and back to 0% strain (cyan box plot). Each box plot represents data from 7 transistors, and for each transistor we averaged the peak position over 3 spots in the channel region. The average A exciton peak position across all devices at 0% strain, 0.4% strain, 0.6% strain, and back to

0% strain is 1.813 ± 0.004 eV, 1.793 ± 0.005 eV, 1.773 ± 0.005 eV, and 1.814 ± 0.005 eV, respectively.

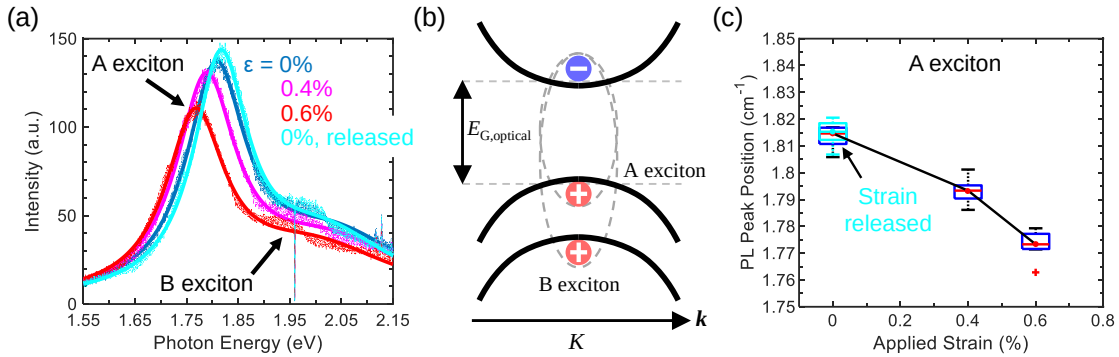


Figure 5.5: (a) Photoluminescence (PL) spectra of the device from Figure 5.2b at different levels of strain. The A exciton peak redshifts with strain and returns to its initial position upon release of strain. The line at ~1.96 eV is due to the Raman filter in the system. (b) Schematic band diagram of 1L $MoS_2$ showing the optical band gap ($E_{G,optical}$) and the A and B excitons. (c) Box plots showing the A exciton peak position from PL measurements as a function of strain, including after the strain is released (cyan box plot). Each box plot includes data from 3 spots across the channels of 7 devices.

## 5.4 Electrical Performance of 1L $MoS_2$ Transistors with Strain

### 5.4.1 $I_D$-$V_{GS}$ and $I_D$-$V_{DS}$ Measurements

In addition to optical measurements, we perform electrical measurements of our devices as a function of strain. Our set-up enables direct probing of our samples under strain (see Figure 5.3a) in a vacuum probe station with pressure ~$2 \times 10^{-5}$ torr. We perform electrical measurements with a Keithley 4200-SCS using Keithley Interactive Test Environment (KITE) software. Figure 5.6a shows drain current vs. gate voltage ($I_D$-$V_{GS}$) measurements of the $MoS_2$ transistor shown in Figure 5.2b ($W$ = 20 μm, $L$ = 8 μm) under different levels of applied strain. The blue, purple, yellow, and red curves in Figure 5.6a illustrate the forward voltage sweeps of the $I_D$-$V_{GS}$ measurement of the device with 0%, 0.4%, 0.6%, and 0.7% applied strain, respectively. The solid lines correspond to data plotted on a log scale (left y-axis), and the dashed lines correspond to the same data plotted on a linear scale (right y-axis). The on-state current increases for each successive measurement and then returns to the initial (unstrained) level upon release of the strain (cyan curve in Figure 5.6a). Thus, strain does not have a permanent effect on the device characteristics. The reverse voltage sweeps of all measurements are removed for clarity

here but displayed in Figure 5.7. The difference between the forward and reverse voltage sweep measurements points to hysteresis in the device, likely arising from electrostatic screening by $H_2O$ and $O_2$ adsorbates trapped at the $MoS_2$-$Al_2O_3$ interface during the transfer process [173]. The gate current remains low (<1.2 nA) across all $V_{GS}$ and strain levels, indicating that there is not much leakage current through the gate dielectric (see Figure 5.7).

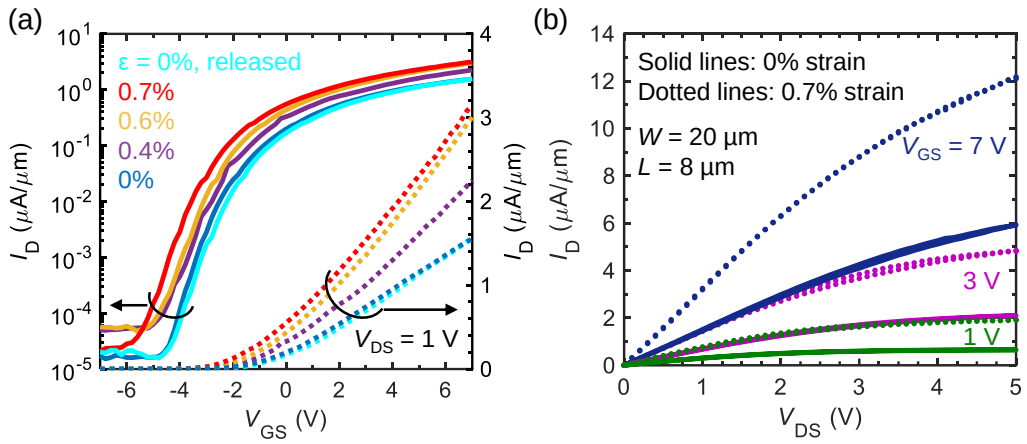


Figure 5.6: (a) Transfer characteristics ($I_D$-$V_{GS}$) of the device from Figure 5.2b at $V_{DS}$ = 1 V and different levels of applied tensile strain. (b) Output voltage characteristics ($I_D$-$V_{DS}$) of the device from Figure 5.2b at 0% (solid) and 0.7% (dotted) applied tensile strain, for $V_{GS}$ between 1 V and 7 V.

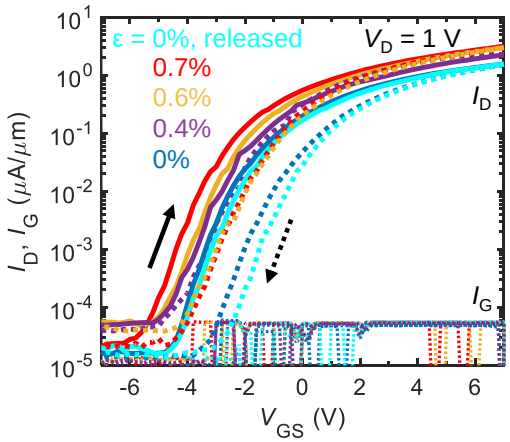


Figure 5.7: $I_D$-$V_{GS}$ curves showing forward (solid lines) and backward (dashed lines) sweeps at different levels of strain. The gate current ($I_G$) at different levels of strain is also depicted by the dotted lines.

The drain current vs. drain voltage ($I_D$-$V_{DS}$) measurements of the device at 0% (solid lines) and 0.7% strain (dotted lines) are displayed in Figure 5.6b at $V_{GS}$ = 1 V (green curve),

$V_{GS}$ = 3 V (magenta curve), and $V_{GS}$ = 5 V (blue curve). These plots include forward and backward voltage sweeps with no observable hysteresis, which again suggests that the traps are located at the $MoS_2$-$Al_2O_3$ interface and are mainly affected by sweeping $V_{GS}$. As before, we observe an increase in $I_D$ with strain for the same $V_{DS}$ and $V_{GS}$. At $V_{GS}$ = 7 V and $V_{DS}$ = 5 V, the current $I_D$ doubles from ~6 μA/μm to ~12 μA/μm at 0.7% strain.

### 5.4.2 Field-effect Mobility ($\mu_{FE}$) and Drive Current ($I_D$) Improvements

We also perform strain-dependent electrical measurements of 7 other transistors with lengths $L$ = 2 μm to 15 μm on the same sample. We extract the field-effect mobility ($\mu_{FE}$) from the $I_D$-$V_{GS}$ curves, calculated as $\mu_{FE} = \frac{dI_D}{dV_{GS}} \frac{L}{WC_{ox}V_{DS}}$. We note that the threshold voltage ($V_T$) changes with strain (see Figure 5.6a), suggesting that the carrier density is changing because of the decreasing band gap [106,290]. To account for shifts in $V_T$, we extract $\mu_{FE}$ at the same carrier density $n$ ~ 1.1×10$^{13}$ cm$^{-2}$, where $n = \frac{C_{ox}}{q}(V_{GS} - V_T - \frac{V_{DS}}{2})$. We estimate $V_T$ using the linear extrapolation method, which uses the voltage intercept of a line fit to the $I_D$-$V_{GS}$ curve near the maximum transconductance $g_m = \frac{\partial I_D}{\partial V_{GS}}$ [291].

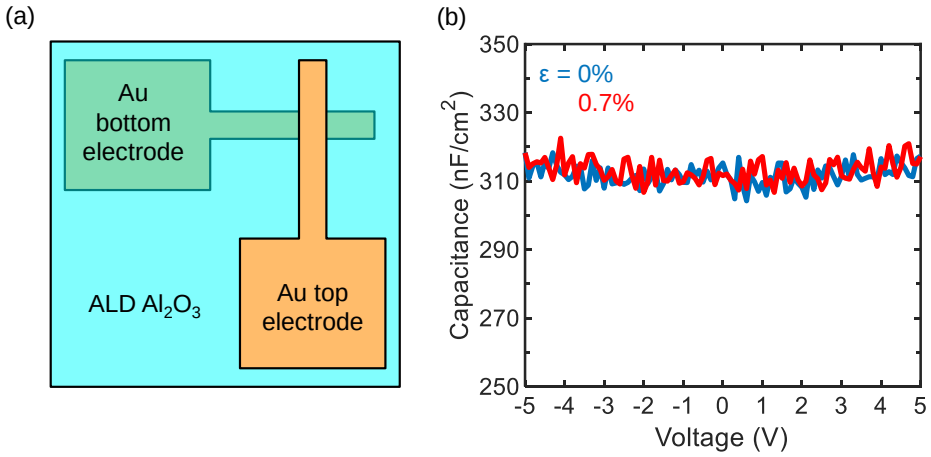


Figure 5.8: (a) Schematic of Au-$Al_2O_3$-Au structure for capacitance-voltage (C-V) measurements. (b) C-V measurements of an Au-$Al_2O_3$-Au device with and without strain. The capacitance is normalized by the area of the top and bottom Au electrode overlap.

$C_{ox}$ is the capacitance of the $Al_2O_3$ gate dielectric, calculated from capacitance-voltage (C-V) measurements of Au-$Al_2O_3$-Au structures (see Figure 5.8a) on the same sample as the $MoS_2$ transistors. We verify that the capacitance does not change with strain, as shown

in Figure 5.8b. We measure a capacitance of ~310 nF/cm$^2$, which we use in our calculation of $\mu_{FE}$. Using ellipsometry, we estimate an $Al_2O_3$ thickness $t_{ox}$ ~ 20 nm. We plot the relative dielectric constant $\epsilon_r$ for different electrode areas, as displayed in Figure 5.9a. For large electrode areas, $\epsilon_r$ converges to ~7 for our deposited $Al_2O_3$, based on the equation $C_{ox} = \frac{\epsilon_r \epsilon_o}{t_{ox}}$, where $C_{ox}$ is normalized by the area of the Au electrode overlap and $\epsilon_o$ = 8.85×10$^{-14}$ F/cm. The AC frequency and voltage bias during the measurements are 20 kHz and 30 mV, respectively. We measure the breakdown field of the gate dielectric, as shown in Figure 5.9b, and ensure that our applied electric field across the $Al_2O_3$ is kept below ~0.6 V/nm.

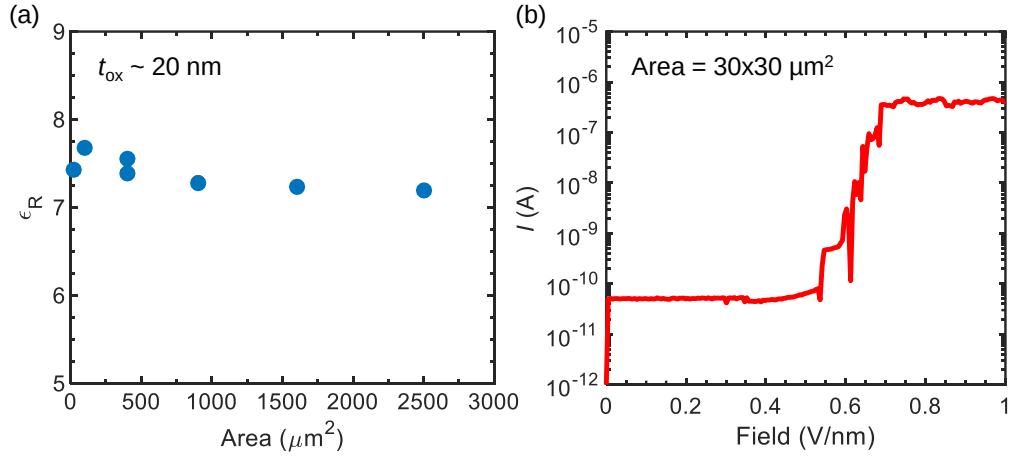


Figure 5.9: (a) Plot of relative dielectric constant ($\epsilon_R$) as a function of area of the Au electrode overlap. (b) Current vs. field for a 30 × 30 μm$^2$ Au electrode area, showing a breakdown field of ~0.6 V/nm.

The $\mu_{FE}$ for the initial, 0% strain measurement extracted from the $I_D$-$V_{GS}$ curves in Figure 5.6a is ~5.3 cm$^2$V$^{-1}$s$^{-1}$, and the $\mu_{FE}$ at 0.7% strain is ~10.8 cm$^2$V$^{-1}$s$^{-1}$. Therefore, we achieve a ~2x improvement in $\mu_{FE}$ at 0.7% strain for this device. We extract $\mu_{FE}$ at the same carrier density ($n$ ~ 1.1 × 10$^{13}$ cm$^{-2}$) and $I_D$ at the same voltages ($V_{GS}$ = 7 V, $V_{DS}$ = 1 V) and plot the data across all devices. Figure 5.10a-b shows $\mu_{FE}$ and $I_D$ normalized to their initial values, with the data from all devices represented by box plots. The average improvement in $\mu_{FE}$ at 0.7% strain is 1.85 ± 0.23, and the average improvement in $I_D$ at 0.7% strain is 1.76 ± 0.18.

Figure 5.11a-b shows absolute values of $\mu_{FE}$ and $I_D$ as a function of strain, with each color corresponding to a different device. As before, all values of $\mu_{FE}$ are extracted at the same carrier density $n$ ~ 1.1×10$^{13}$ cm$^{-2}$ and $V_{DS}$ = 1 V, and all values of $I_D$ are extracted at

$V_{GS}$ = 7 V and $V_{DS}$ = 1 V. The points on the right side of each plot show $\mu_{FE}$ and $I_D$ after the strain returns to 0%. We note that the initial unstrained mobilities are lower than some other $MoS_2$ studies [51,53], which we attribute to growth-to-growth variation and degradation of the $MoS_2$ after transfer to the flexible substrates. We also perform strain-dependent electrical measurements on a different set of 1L $MoS_2$ transistors with higher initial mobilities, which will be discussed in Section 5.4.3.

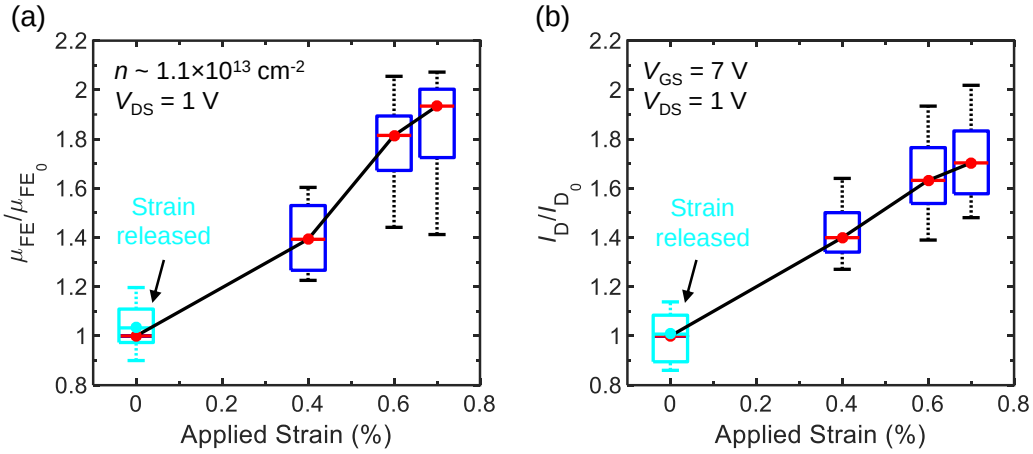


Figure 5.10: (a) Field-effect mobility ($\mu_{FE}$) and (b) drain current ($I_D$) normalized to the initial (unstrained) values for 8 devices as a function of applied strain, with the box plots showing the median value across devices (red points), first and third quartiles (blue box), and maximum and minimum points (top and bottom lines, respectively). $\mu_{FE}$ is extracted at a carrier density $n \sim 1.1\times10^{13}$ cm$^{-2}$. $I_D$ is extracted at an applied voltage of $V_{GS}$ = 7 V and $V_{DS}$ = 1 V. The cyan box plots correspond to the measurements after strain is released.

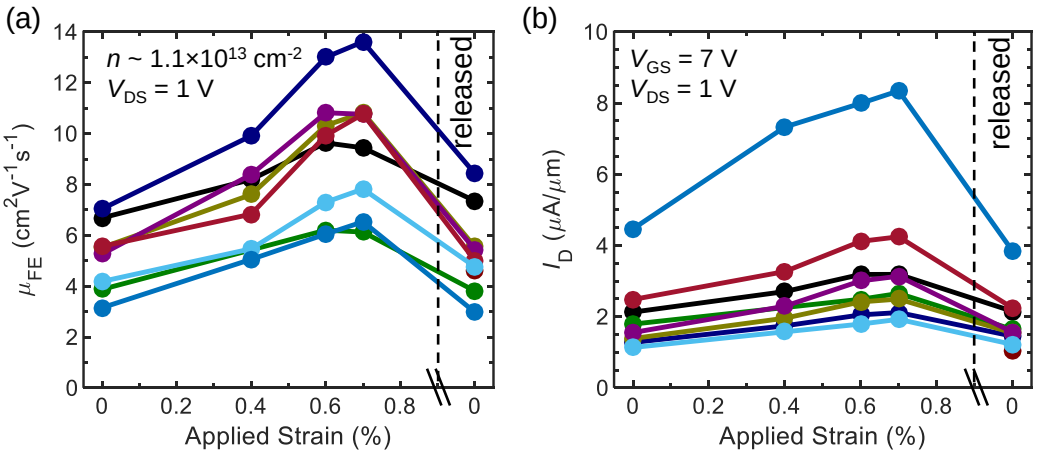


Figure 5.11: (a) Mobility ($\mu_{FE}$) and (b) drain current ($I_D$) for 8 different devices at 0%, 0.4%, 0.6%, 0.7%, and back to 0% strain.

We plot normalized $\mu_{FE}$ and $I_D$ at 0.7% strain as a function of length down to 2 μm (see Figure 5.12a-b), with no clear trend observed. This suggests that the current enhancements are intrinsic to the $MoS_2$ and not related to contact resistance effects. We expect a similar improvement in mobility and current for short channel transistors, though contact resistance may play a larger role at shorter channel lengths. Further studies with shorter channel ($L$ < 1 μm) transistors are needed to determine the effect of strain on short-channel devices. We also extract $\mu_{FE}$ at a lower carrier density ($n$ ~ 4.8×10$^{12}$ cm$^{-2}$) to determine if $n$ has an effect on the improvement in the electrical performance. The absolute and normalized $\mu_{FE}$ at lower $n$ have slightly lower values but the overall trends are the same as at higher $n$ (see Figure 5.13).

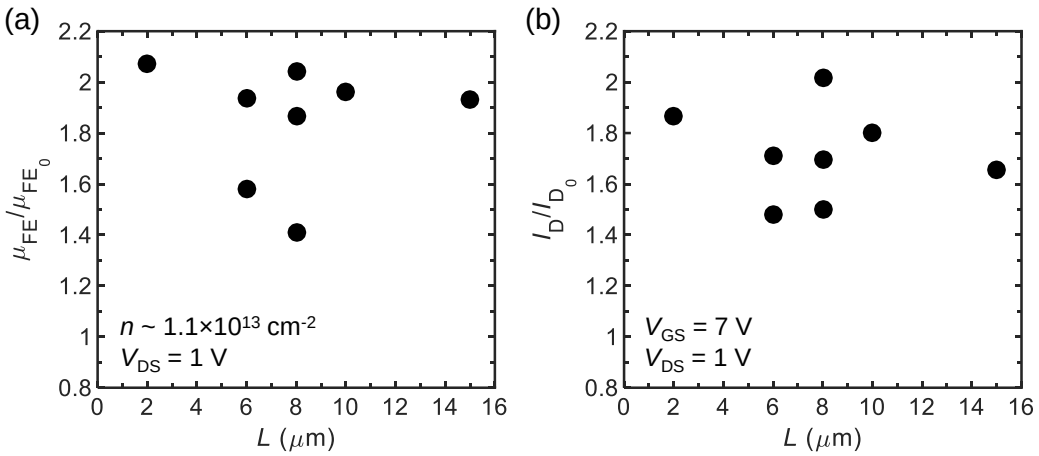


Figure 5.12: (a) Normalized $\mu_{FE}$ and (b) normalized $I_D$ at 0.7% strain as a function of channel length.

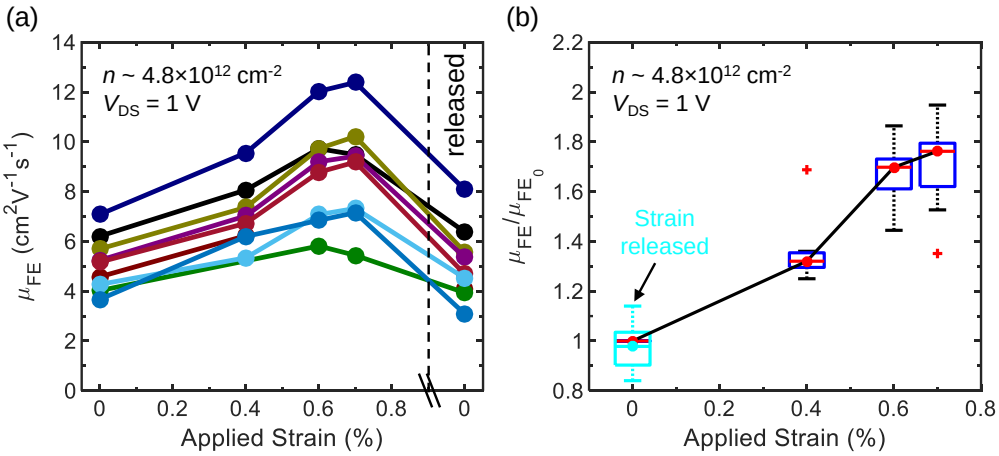


Figure 5.13: (a) Mobility ($\mu_{FE}$) and (b) normalized mobility ($\mu_{FE}$) for 8 different devices at 0%, 0.4%, 0.6%, 0.7%, and back to 0% strain at a lower carrier density $n$ ~ 4.8×10$^{12}$ cm$^{-2}$.

### 5.4.3 Degradation of Devices at Higher Levels of Strain

Figure 5.11a-b illustrates an improvement in $\mu_{FE}$ and $I_D$ across all devices at 0.4% and 0.6% strain, with some devices achieving an increase up to 2x. At 0.7% strain, we observe additional improvements for most of the devices, but some of the devices degrade slightly at this higher level of strain. For measurements of other samples in which the amount of strain exceeds 0.7%, we observe a degradation in electrical performance of all devices. Figure 5.14a depicts this decrease in mobility at 0.8% strain during the 1st measurement. When the strain returns to 0%, the mobility decreases further. However, the 2nd measurement (Figure 5.14b) shows an increase in mobility when strain is again applied to the devices. These results demonstrate that there is an initial "break-in" of the device when the strain exceeds 0.7%, corresponding to a degradation in performance. During subsequent measurements, we observe an increase in mobility with strain.

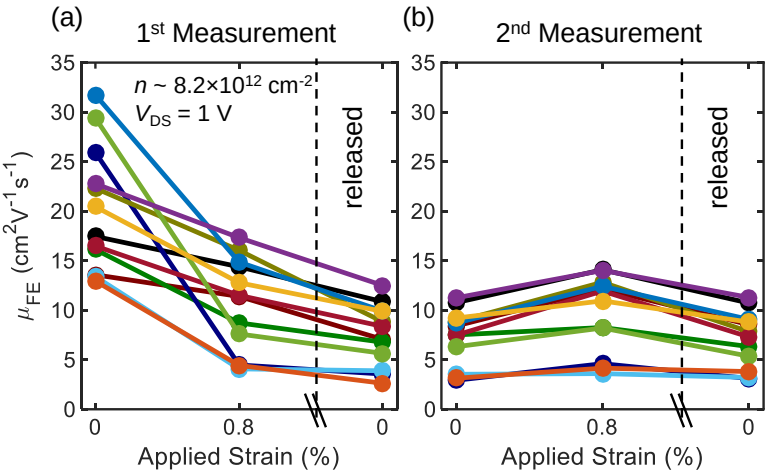


Figure 5.14: Field-effect mobility as a function of strain for devices on a different sample. Each curve corresponds to a different device. (a) First measurement of devices at 0%, 0.8%, and back to 0% strain, showing a degradation in mobility. (b) Second measurement after device "break-in" at 0%, 0.8%, and back to 0% strain, this time showing an improvement in mobility at 0.8% strain.

Figure 5.15a-b shows the same trends in current at higher strain, i.e. an initial decrease in current with strain during the first measurement and subsequently an increase in current with strain during the second measurement. Once the strain is released the second time, the current and mobility return to the same levels as before the second measurement. We would like to point out that the device measurements displayed in Figure 5.14 and Figure 5.15 have higher initial unstrained mobilities and drive currents than the device measurements

shown in Figure 5.11, but we were unable to further improve the mobility with strain because of device degradation.

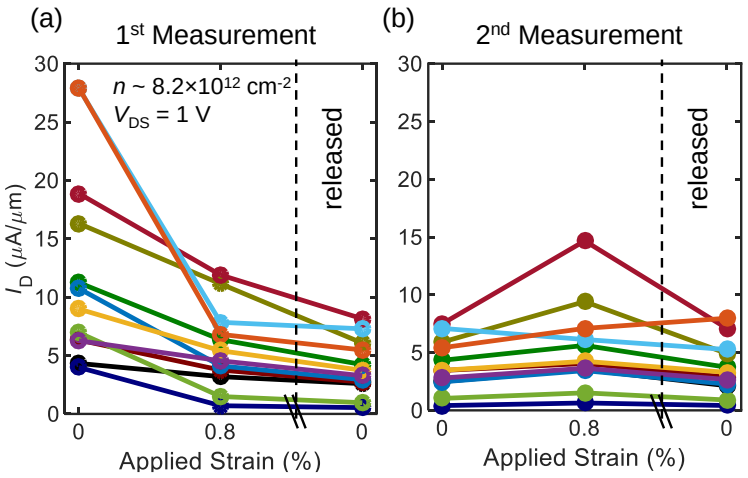


Figure 5.15: $I_D$ as a function of strain for the same devices in Figure 5.14. Each color corresponds to a different device. (a) First measurement of devices at 0%, 0.8%, and back to 0% strain, showing a degradation in current. (b) Second measurement after device "break-in" at 0%, 0.8%, and back to 0% strain, this time showing an improvement in current at 0.8% strain.

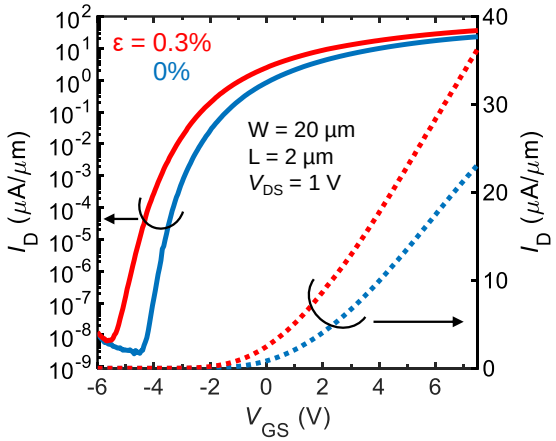


Figure 5.16: $I_D$-$V_{GS}$ measurements at 0% and 0.3% strain for a transistor with $W = 20$ μm and $L = 2$ μm on a different sample. The mobility increases from ~25 $cm^2V^{-1}s^{-1}$ at 0% strain to ~34 $cm^2V^{-1}s^{-1}$ at 0.3% strain at $n \sim 7\times10^{12}$ $cm^{-2}$.

We also perform strain-dependent electrical measurements on another set of 1L $MoS_2$ transistors with higher initial mobilities (~15 $cm^2V^{-1}s^{-1}$ to 35 $cm^2V^{-1}s^{-1}$), and transfer characteristics from one of these transistors are included in Figure 5.16. The mobility and current of these devices improve with ~0.3% strain, but we were unable to continue improving the devices due to degradation of the devices at higher levels of strain. The

mobility of the device in Figure 5.16 increases from ~25 $cm^2V^{-1}s^{-1}$ at 0% strain to ~34 $cm^2V^{-1}s^{-1}$ at 0.3% strain at $n \sim 7\times10^{12}$ $cm^{-2}$.

We attribute the degradation in electrical performance at higher strains to cracking in the metal or worsened adhesion of the contact metal to the $MoS_2$. The gate leakage current remains the same when the drain current decreases at higher strain levels, so it is unlikely that the gate dielectric contributes to the device degradation. We also do not expect this degradation to result from "slippage" of the $MoS_2$ along the substrate at higher strain, because we observe the expected shift in the E' Raman peak at such levels of strain (see Figure 5.17 for Raman spectra at 0% and 0.8 % strain of a device whose measurements are shown in Figure 5.14 and Figure 5.15). Alternate oxides like $HfO_2$, which has a lower Young's modulus than $Al_2O_3$, or metals that are more ductile might enable higher strains without resulting in cracking or delamination of materials in the device stack [257,292].

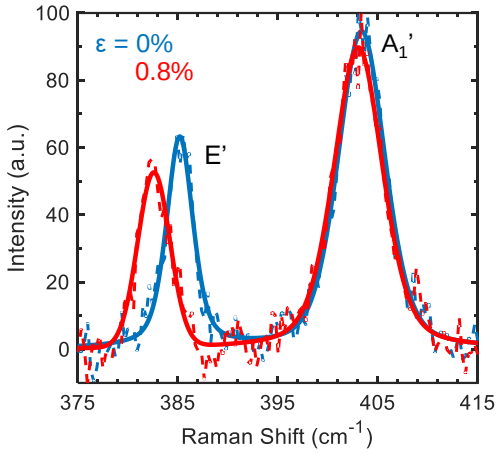


Figure 5.17: Raman spectra at 0% and 0.8% for one of the devices that degraded at 0.8% strain. The redshift in the E' peak shows that the $MoS_2$ is still strained even after initial device degradation and does not slip against the substrate.

### 5.4.4 Changes in Band Structure with Strain

The improvements in current and mobility of our devices result from changes in the band structure with strain. The optical band gap of 1L $MoS_2$ at the *K*-point decreases with tensile strain, depicted by a shift in the A exciton peak in Figure 5.5a. The exciton binding energy is not expected to vary significantly with strain [258,260], so we expect a decrease in the electronic band gap similar to that of the optical band gap. The second lowest valley in the conduction band occurs at the *Q*-point (halfway between the *Γ*- and *K*-points), and

the energy separation between the *Q* and *K*-points ($\Delta E_{QK}$) is predicted to be ~50-200 meV for unstrained 1L $MoS_2$ [88,269,271,293,294]. We note that the calculated $\Delta E_{QK}$ varies widely in the literature and depends on factors like screening environment, and the experimental value might be lower than what theory predicts. Interactions between electrons and phonons in the *K* and *Q* valleys leads to intervalley scattering when $\Delta E_{QK}$ is small [88,269,294]. When tensile strain is applied to $MoS_2$, the energy separation between the *K*- and *Q*-points ($\Delta E_{QK}$) increases (see Figure 5.18), resulting in less intervalley scattering [88,269,271,294]. Intervalley scattering is known to degrade field-effect mobility, so a decrease in intervalley scattering should lead to improved mobility. Because 2L $MoS_2$ has a smaller $\Delta E_{QK}$ than 1L $MoS_2$ [293], we expect an even larger mobility improvement with strain for 2L $MoS_2$.

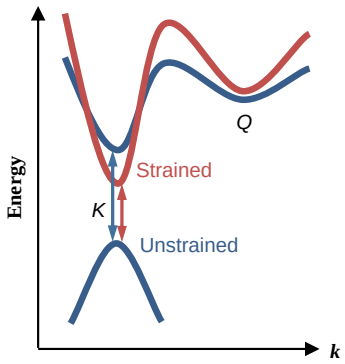


Figure 5.18: Schematic band structure of strained and unstrained 1L $MoS_2$, showing an increase in the energy separation between the minima of the *K* and *Q* valleys in the conduction band for strained $MoS_2$.

Tensile strain is also expected to change the curvatures of the valleys in the conduction band, leading to decreased effective mass of electrons [240,271,295]. This is similar to the reduced effective mass of electrons with strain in silicon nMOS transistors, which leads to increased mobility [13,268]. Applying tensile strain to transistors has also been shown to lower the Schottky barrier heights at the metal-semiconductor junctions at the source and drain contacts [89,106,273,296,297]. This may be due to a reduction in the band gap of the material or change in carrier density and can result in more efficient injection of electrons and lower contact resistance. However, because our devices have relatively long channels and the improvements in $\mu_{FE}$ and $I_D$ do not depend on channel length (see Figure 5.12), we expect the contribution of contact resistance to total resistance to be relatively small

[51,55]. Thus, we believe that the electrical performance improvements are mostly related to the electronic transport in the $MoS_2$ channel (i.e. decrease in band gap, effective mass, intervalley scattering), and contact effects play a minor role.

Our results are a promising proof-of-concept of strain-induced performance enhancements in 2D-based transistors, but future studies will aim to develop methods to induce strain in transistors during fabrication, such as through tensile encapsulation layers [298,299] or lattice-mismatched substrates [300], as has been demonstrated in silicon FETs [12-14]. This would have the additional advantage of inducing biaxial strain in the 2D material, which is expected to have a larger effect on the electrical properties than uniaxial strain [269,276].

## 5.5 $MoS_2$ Transistors for Strain Sensors

The large change in resistance of $MoS_2$ transistors with strain indicates that these devices could be useful for strain sensors. The figure of merit used to characterize strain sensors is the gauge factor (GF), which is defined as $\Delta R/R_0/\Delta\varepsilon$, where $\Delta R$ is the change in resistance between 0% strain and strain $\varepsilon$, and $R_0$ is the initial resistance at 0% strain [301]. Metals are often used in commercial strain gauges due to their ease of fabrication, but they typically have GF < 50 [302]. Semiconductors are promising as strain sensors since they have much larger GF. Silicon strain sensors have GF ~ 30-50 for polycrystalline silicon (poly-Si) [303,304] and up to 200 for single-crystal silicon (c-Si) [305]. 2D materials like $MoS_2$ and other TMDs are predicted to have large GFs because, similar to silicon and germanium, they are piezoresistive. In addition, they can withstand much higher strains than conventional bulk materials, making them especially attractive for flexible electronics [103].

Figure 5.19a shows the resistance ($R = V_{DS}/I_D$) vs. $V_{GS}$ curves for the device in Figure 5.2b at 0%, 0.4%, 0.6%, and 0.7% applied strain. Figure 5.19b illustrates $\Delta R/R_0$ extracted for each level of strain with respect to the 0% strain curve in Figure 5.19a, at $V_{GS}$ = -4.5 V, 0 V, 3 V, and 7 V. We find the largest change in resistance at $V_{GS}$ = -4.5 V, which corresponds to the subthreshold region of the transistor. Fitting a line to the $\Delta R/R_0$ curve for $V_{GS}$ = -4.5 V yields an average GF of ~150 across all levels of strain. Figure 5.19c shows the calculated GF as a function of $V_{GS}$ for each different strain level in Figure 5.19a.

We observe a peak in GF at all strain levels near $V_{GS}$ = -4.5 V, with the maximum GF reaching 200 for 0.4% strain. Figure 5.19d compares our best GF values to those found in literature for $MoS_2$, in addition to other 2D materials, silicon, and metals. We note that this plot only includes GF values calculated as $\Delta R/R_0/\Delta\varepsilon$. Some studies calculate GF as $\Delta I/I_0/\Delta\varepsilon$, which artificially results in much larger GF values. We find that our GF for 1L CVD-grown $MoS_2$ is higher than the best GFs for 1L and 3L exfoliated $MoS_2$ [107], CVD-grown $MoS_2$ [108-110], other 2D materials [306], polycrystalline silicon [303,304], and metals [302]. Comparable and slightly higher GFs have been demonstrated for 2L exfoliated $MoS_2$ [106,107] and bulk crystalline Si [305,307]. However, large area, 1L CVD-grown $MoS_2$ is more promising and easier to integrate than exfoliated $MoS_2$ or bulk Si for large-area flexible and transparent sensor systems.

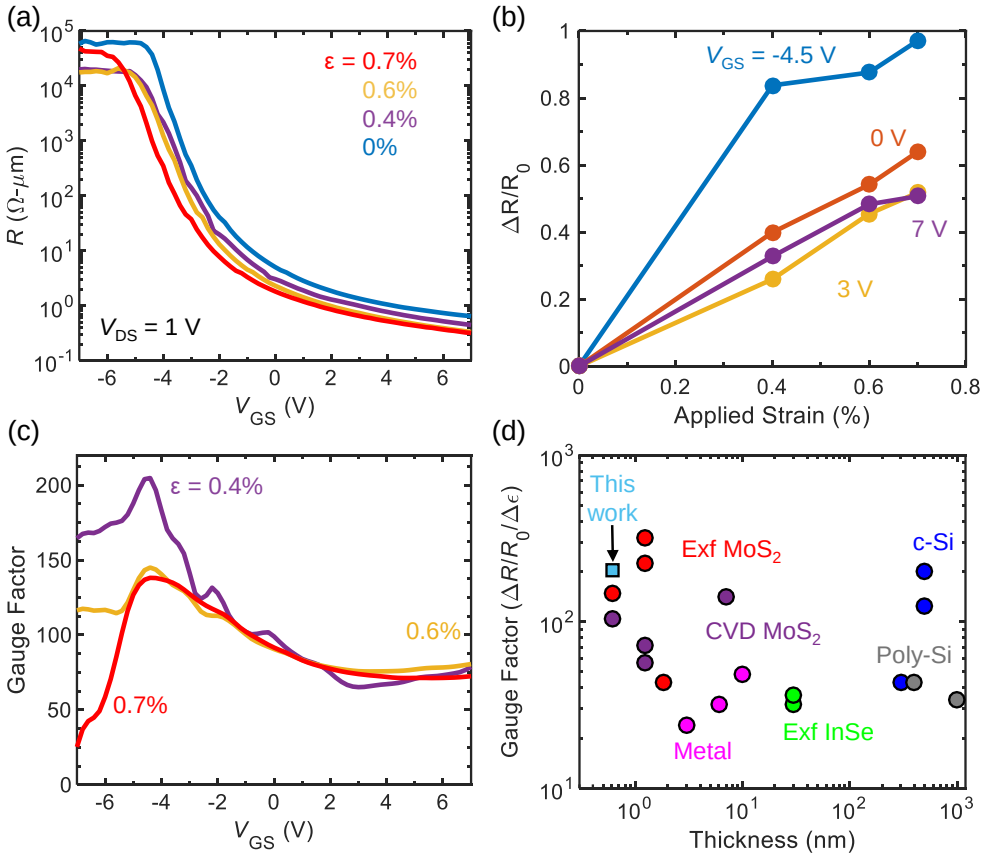


Figure 5.19: (a) Resistance ($R$) vs. $V_{GS}$ curves of the device in Figure 5.2b at $V_{DS}$ = 1 V at different levels of applied strain (ε). (b) $\Delta R/R_0$ vs. strain at different gate voltages for the curves in (a). (c) Gauge factor (defined here as $\Delta R/R_0/\Delta\varepsilon$) vs. $V_{GS}$ for the different levels of strain. (d) Plot of gauge factor vs. thickness for various materials found in literature, including CVD-grown $MoS_2$, exfoliated $MoS_2$, exfoliated InSe, polycrystalline Si, crystalline Si, and various metals.

## 5.6 Conclusion

In summary, we studied the dependence of the electrical performance of CVD-grown 1L $MoS_2$ transistors on tensile strain. Shifts in the Raman spectra confirmed the amount of strain we applied to the $MoS_2$, and shifts in the PL spectra quantified the decrease in the band gap with strain. We demonstrated a continuous increase in mobility and current in the $MoS_2$ transistors up to 2x and showed that the devices recovered their initial characteristics when the strain was released. We attribute these improvements in electrical properties to changes in the band structure, including decrease in band gap, electron-phonon intervalley scattering, and effective mass of electrons. We also showed that $MoS_2$ transistors are useful for strain sensors and achieve gauge factors up to 200, which is among the highest values reported in literature for a sub-1 nm thick film. Using $MoS_2$ transistors as strain sensors could enable flexible and transparent sensor systems for strain mapping. These results achieve the largest mobility and on-state current enhancements to $MoS_2$ transistors using strain to date, suggesting that strain engineering might play an important role for integrated 2D electronics.

# Chapter 6

# Conclusions and Future Work

## 6.1 Conclusions

This thesis presented a detailed study of devices based on molybdenum disulfide and molybdenum ditelluride. Through electrical, optical, thermal, and strain-dependent characterization, I studied the fundamental properties of these TMDs and improved our understanding of TMD-based transistors and memory. First, I explored resistive memory based on $MoTe_2$, a relatively underexplored TMD. I demonstrated bipolar switching in these devices and showed that the forming process is thermally-activated, based on temperature-dependent measurements. Using scanning thermal microscopy, I observed localized heating in our devices, which were the first direct observations of localized heating and switching in 2D-based memory. I discovered that the switching ultimately resulted in Au migration between electrodes due to Joule heating, but initial forming likely resulted from Te migration or vacancy generation within the $MoTe_2$. These results provide insight into the thermal aspects of switching in TMD-based memory and suggest that this thermal measurement technique can be useful for studying novel memory devices. Such a thermal analysis is especially important for 3D chips where thermal crosstalk is of concern.

Next, we performed electrical measurements of $MoS_2$ transistors with different growth methods, thicknesses, and gate dielectrics and at different temperatures to study hysteresis and charge trapping, which lead to inaccurate analysis of the electrical properties. We developed a simple technique which utilizes pulsed voltages applied to the gate with pulse widths ranging from 1 μs to 500 ms to reduce hysteresis in the $I_D$-$V_{GS}$ curves of $MoS_2$ transistors. These results suggest that most charge traps have time constants longer than 1 ms in these devices. We demonstrated a reduction in charge trap density to $<1.4\times10^{10}$ $cm^{-2}$ for a pulse width of 500 μs across devices with $SiO_2$ gate dielectrics. We also showed that hysteresis-free measurements using pulsed measurements enable a more accurate extraction of field-effect mobility than DC measurements, which can give errors up to 50%.

Lastly, we used a tunneling front model to estimate the depths of active charge traps in our gate oxides. While we aim to fabricate transistors without any charge trapping or hysteresis, our technique allows for extraction of the "true" threshold voltage and mobility of emerging devices based on novel materials that suffer from charge trapping.

Then, we employed Raman, photoluminescence (PL), and absorption spectroscopy to study the properties of $Mo_{0.91}W_{0.09}Te_2$, a semiconducting alloy of $MoTe_2$ with similar optical properties. The slight differences in the Raman peak positions and A-B spitting in the valence band measured with PL result from the presence of W atoms, which are heavier than Mo atoms. We determined that 1L $Mo_{0.91}W_{0.09}Te_2$ is also a direct gap semiconductor, as evidenced by its strong PL peak corresponding to the energy of the A exciton. For the first time, we applied strain to 1L $Mo_{0.91}W_{0.09}Te_2$ and 1L $MoTe_2$ to tune the band structure of these materials and measured a decrease in the optical band gap. We also observed a decrease in the linewidth of the PL and absorption peaks, which we attributed to decreased exciton-phonon intervalley scattering due to the larger separation of the *K* and *Q* valleys of the conduction band with tensile strain. These results provided insight into the properties of $Mo_{0.91}W_{0.09}Te_2$ and motivated further studies on the dependence of the electrical properties of TMD-based transistors on strain.

Lastly, I used strain engineering to enhance the electrical properties of $MoS_2$ transistors. Raman and PL spectroscopy were performed to verify the amount of strain applied to the $MoS_2$ and measure the decrease in optical band gap, respectively. I demonstrated an improvement in field-effect mobility and drive current in $MoS_2$ transistors up to 2x with applied uniaxial tensile strain and showed that the effects are reversible when the strain is released. The large change in resistance with strain, in addition to the transparency and flexibility of $MoS_2$, suggests that these devices could be useful for strain sensing applications. I measured gauge factors up to 200, which is among the highest values for atomically thin 2D materials. These results are encouraging because although 1L TMDs have potential for highly scaled transistors, their electrical properties must be improved to compete with existing technologies. This is the first study showing improvements to the electrical performance of 1L TMD transistors with strain and suggests that strain may play a significant role in 2D electronics, as it has for silicon.

Overall, this body of work provides an extensive study of TMDs for logic, memory, and flexible electronics applications. In the next section, I will describe important areas of research that need to be explored for these materials to be adopted by industry.

## 6.2 Future Work

This work, in addition to many other studies, shows that TMD-based devices are very promising for next-generation electronics, but there are many aspects of the fabrication and performance of these devices that must be improved to bring them closer to commercial use. In terms of fabrication challenges, high-quality and wafer-scale growth are needed for nearly any application. Many applications also require low temperature growth or integration of 2D materials using transfer techniques. Establishing methods for wafer-scale, wrinkle-free transfers has been demonstrated in some studies but will need to be fully automated for use in industrial applications. Other issues that can arise during fabrication of 2D-based devices are poor adhesion of 2D materials to the growth or target substrates. In addition, materials such as gate dielectrics often have poor adhesion to the surface of 2D materials due to the weak van der Waals forces and lack of dangling bonds.

2D materials have gained interest for niche applications in flexible electronics, including sensors and displays. The results in Chapter 5 showed that $MoS_2$ transistors have larger gauge factors than many conventional strain gauges and thus can be useful for strain sensors. Due to their transparency, flexibility, good electrical performance, and low fabrication temperatures, TMDs have also been investigated for flexible displays [308]. TMDs may be integrated into devices for these kind of niche applications more easily than state-of-the-art technology, which has more stringent requirements for the quality of materials and electrical performance of devices.

Further studies of TMD-based memory are needed to determine whether these materials are practical for emerging memory devices and can compete with storage-class memory such as RRAM and CBRAM based on transition metal oxides, which have been studied for many more years. Measurements of endurance, reliability, and retention will be important to fully evaluate their performance. In addition, different materials and thicknesses need to be explored to find the optimal combination for the best performance. Apart from TMD-based RRAM and CBRAM, TMDs can also be integrated into phase

change memory (PCM) as heat confinement layers [95,96] or dynamic random access memory (DRAM) as the access transistor to reduce power consumption [90,92,93].

Electrical properties such as mobility, current, and contact resistance of TMD transistors need to be improved for these transistors to be integrated into logic chips. While $MoS_2$ is the most studied TMD and has good n-type performance, other 2D materials such as $WS_2$ are predicted to have higher mobilities and can also act as both n-type and p-type transistors [254,309,310], which is useful for complementary transistor technology. Channel doping by charge transfer from sub-stoichiometric oxides or chemicals is an example of a method to improve the mobility and contact resistance [54,84-86], and selective doping in the contact regions while leaving the channel region intact may also prove to be a promising technique. Substitutional doping of large area growths is another possible approach to improve mobility and contact resistance but has yet to be successfully applied to 2D materials using large scale growth techniques. In addition, encapsulating the TMD transistor with a high-quality material such as hexagonal boron nitride or high-*k* dielectrics deposited by atomic layer deposition can improve the dielectric environment and reduce charge trapping, thereby improving device performance [169].

Strain engineering is also a useful tool to improve the electrical performance of TMD-based transistors, and the studies described here may serve as a useful starting point for further investigations. Chapter 5 showed that applying strain to devices by bending flexible substrates proved to be a nice proof-of-concept method to study the effects of different levels of strain on the electrical properties of transistors, but development of methods to induce strain during fabrication of transistors is necessary moving forward. Established methods of applying strain in silicon technology can be adapted for TMD-based devices. For example, growth of TMDs on substrates with different lattice constants or thermal coefficients of expansion, or encapsulation of TMDs with stress-inducing nitride or metal layers may result in built-in strain in the TMDs [298-300,311], leading to improved electrical performance of transistors. In addition, other TMDs besides $MoS_2$ may experience larger enhancements in electrical performance with strain and therefore must be explored.

Looking to the future, 2D materials are unlikely to entirely replace Si but are promising candidates for 3D heterogeneous integration of logic and memory on Si-based chips. There

are many individual challenges facing memory and transistors as discussed above, in addition to challenges with integrating 2D-based logic and memory on a single 3D chip. However, with combined effort from the research communities in industry and academia, these challenges can be overcome and 2D materials can be integrated with state-of-the-art technology to enable continued improvements in computing performance.

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