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A Double-Sided Stack Low-Inductance Wire-Bondless SiC Power Module with a Ceramic Interposer

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A Double-Sided Stack Low-Inductance Wire-Bondless SiC Power Module with a Ceramic Interposer

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Abstract

The objective of this dissertation research is to develop a novel three-dimensional (3-D) wire bondless power module package for silicon carbide (SiC) power devices to achieve a low parasitic inductance and an improved thermal performance. A half-bridge module consisting of 900-V SiC MOSFETs is realized to minimize stray parasitic inductance as well as to provide both vertical and horizontal cooling paths to maximize heat dissipation. The proposed 3-D power module package was designed, simulated, fabricated and tested. In this module, low temperature co-fired ceramic (LTCC) substrate with vias is utilized as an interposer of which both top and bottom sides are used as die attachment surfaces, the SiC MOSFET bare dies are flip-chip attached on the LTCC interposer using nickel-plated copper balls, high horizontally thermal conductive material is integrated into the LTCC interposer to improve its thermal dissipation capability. Hence, the LTCC interposer provides both electrical and thermal routing and the nickel-plated copper balls replace bond wires in conventional planar power module as the electrical interconnections for the SiC power devices. On the other side, direct bond copper (DBC) substrate are used at both top and bottom sides of the 3-D module to achieve electrical path for SiC devices and double-sided cooling. As a result, 3D power routing is achieved to reduce stray inductance, and both vertical and lateral paths are utilized to spread heat generated by the power devices in this compact module architecture.

Electrical simulation was performed to extract the parasitic inductances in the 3-D package and compared to other reported module packages. Low loop parasitic inductance of 4.5nH at a frequency of 1MHz is achieved after optimization. Thermal and thermo-mechanical simulations were also conducted to evaluate the thermal performance and mechanical stress of the proposed module structure.

The fabrication process flow of the 3-D wire bondless module is developed and presented. The fabricated half-bridge module was evaluated experimentally by double-pulse test and thermal cycling test. Significant reduction in voltage overshoot and ringing was observed during the double-pulse test, and the module shows no degradation after thermal cycling test.

To push the double-sided wire-bondless module to higher voltage application, a 3.3-kV SiC double-sided wire-bondless common source module was designed, fabricated, and tested. Electric field simulations were performed considering the associated challenge of increased electric field strength in the higher-voltage wire-bondless module. High voltage blocking test was added to evaluate the high voltage operation capability as well.

Acknowledgements

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I also want to pay my most humble tribute to Dr. Michael D. Glover and Clint Hardee, although no longer with us. The training and help I have received from them made my dissertation research proceed smoothly.

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List of Published Papers

Chapter 4 consists of a published IEEE paper with the following citation:
S. Huang, Z. Xu, F. Yu and S. S. Ang, "Impact of nano-diamond composites on low-temperature co-fired ceramic interposer for wide bandgap power electronic module packages," 2016 *IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Fayetteville, AR, 2016, pp. 314-318, doi: 10.1109/WiPDA.2016.7799959.

Chapter 5 consists of a published IEEE paper with the following citation:
S. Huang and S. S. Ang, "Investigations of low temperature co-fired ceramic heat spreading interposer for the thermal management of three-dimensional packages," 2018 *34th Thermal Measurement, Modeling & Management Symposium (SEMI-THERM)*, San Jose, CA, 2018, pp. 8-12, doi: 10.1109/SEMI-THERM.2018.8357346.

Chapter 1 Introduction

1.1 Background and Motivation

Power electronics is a study to control and converse electric power, and the conversion is performed with semiconductor switching devices including diodes and power transistors such as MOSFET in power electronic modules. An average of 12 billion kilowatts power is generated every hour all over the world, and about 20% of this energy is wasted during the power conversion process due to low conversion efficiency. Therefore, highly efficient power electronic module is one of the most important parts in power conversion systems. The modern power electronics systems have been rapidly developed for decades based on silicon (Si) devices, however, the Si power devices are approaching its material theoretical limits. Meanwhile, silicon carbide (SiC) electronic device technology has made big progress [1]. The properties of SiC material including larger bandwidth, higher electrical breakdown field, and higher thermal conductivity allow SiC power semiconductor devices to achieve higher breakdown voltage and lower on-state resistance, higher operation temperature, as well as higher switching speed with lower switching loss and higher switching frequency compared to traditional Si devices [2]. Besides semiconductor devices, power module packaging technologies also play an important role in improving conversion efficiency of power electronic module by affecting its electrical, thermal and mechanical performance.

The commercial SiC MOSFETs are commonly developed with high voltage rating above 650 V, high current rating up to around 200 A, and high power capability. Besides, SiC can withstand higher temperature due to its wide band gap and has a 3.5 times better thermal conductivity than Si, which means promising high temperature operation at high voltage and power levels [3]. Right

now, most SiC power modules existing in the market follow the conventional packaging structure and method of Si power modules, in which bonding wires are interconnection for bare semiconductor dies mounted on one planar substrate, mostly direct bond copper (DBC), as shown in Fig. 1.1. The conventional power module packaging is easy to fabricate with low cost thanks to the well-developed production process. However, the electrical and thermal advantages of SiC power devices are limited by this structure [4]. For example, the bonding wires bring in large parasitic inductances and resistances which result in large voltage overshoot and ringing at high frequency, leading to significant device switching losses and electromagnetic interference (EMI) noises [2]. Besides, wire bond lift-off due to temperature development within the bonding wires is one of the most common and important failure modes in power electronics modules [5]. Another critical challenge of packaging is the thermal and thermal-mechanical management in the power module. The SiC power devices have high voltage drop when conducting current during short switching time, these result in significant power dissipation in the power module which needs to be removed in time through packaging. The coefficient of thermal expansion (CTE) mismatch between materials used in the power modules could cause thermo-mechanical stress issue hence potential failure such as surface degradation in SiC device bonding pads and crack in die or substrate, ultimately the power devices are failed [6]. As a result, the advantages of SiC like high switching speed, low switching loss and high operation temperature can’t be fully fulfilled, new packaging architectures are necessary demand to break through the bottleneck for SiC device applications.

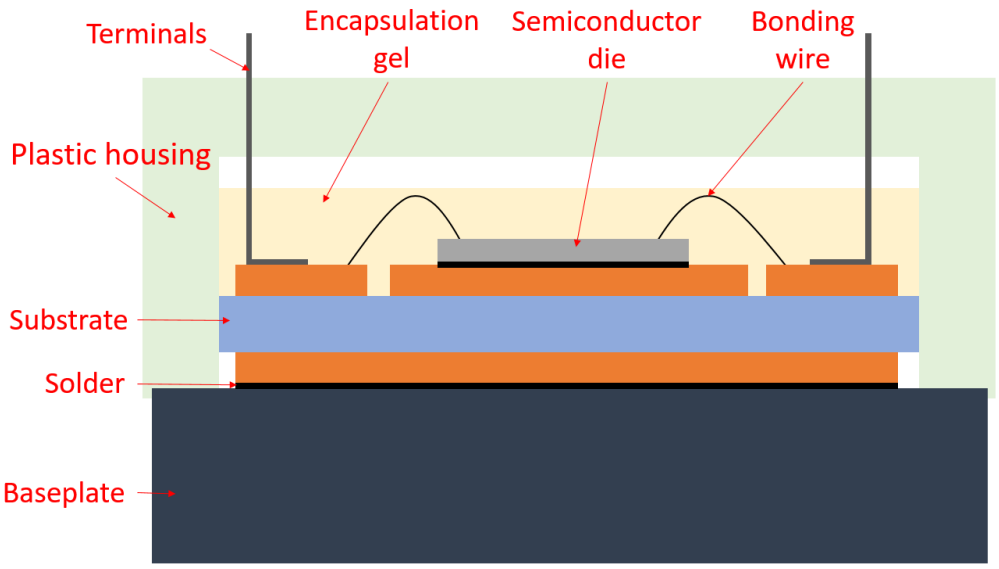


Fig. 1. 1 A conventional wire bonding power module packaging structure.

To meet the demand of high-performance power electronics in application such as automotive product, the development of power electronics packaging targets at increasing power density, minimizing parasitic parameter, reducing footprint and cost while maintaining good reliability. The Electrical and Electronics Technical Team Roadmap for electric drive vehicle published by U.S Department of Energy in October 2017 proposed a target of power density for the high-voltage power electronics is shown in Table 1.1 [7]. A compact layout such as double-sided stack package helps increase power density, but it brings challenges to thermal management and reliability, because the smaller package limits heat dissipation, and the high temperature will affect the reliability of interconnection and interface. Besides, there is higher requirement on the precision during module fabrication due to the compact layout. Meanwhile, along with the replacement of Si with SiC devices which operate at a higher switching frequency, the parasitic inductance of the

module package needs to be minimized to reduce oscillation and overshoot during switching and thus reduce the switching loss [8].

Table 1. 1 Technical Targets for High Voltage Power Electronics [7]

Power Electronics Targets			
Year	2020	2025	Change
Power Density (kW/L)	13.4	100	87% volume reduction

Motived by such trends, a double-sided low-inductance wire-bondless power module with ceramic interposer for 900-V SiC MOSFETs and a double-sided wire-bondless power module for 3.3-kV SiC MOSFETs have been designed and fabricated in this dissertation research. Both modules achieve small footprint due to the stack wire bondless structure, the size of the 900-V module is 28 mm x 50.5 mm x 5.32 mm, and the size of the 3.3-kV module is 35.8 mm x 61.7 mm x 5.7 mm, the power density of the power module is 23.0 kW/L and 50.6 kW/L, respectively. To improve the thermal management efficiency, double-sided cooling is utilized, besides, how the integration of high thermal conductivity materials affect the thermal performance of the LTCC interposer is investigated. Effects are also made to address the challenge of high requirement on the precision during module fabrication, such as solder mask for alignment, fixtures for module assembly, and silver sintering to avoid interface material overflow. Moreover, in order to minimize the parasitic inductance of the package, vertical power loop is achieved with LTCC interposer and copper ball interconnection in the 900-V power module, and the metal post in the 3.3-kV power module. The parasitic inductance of 4.5 nH and 5.1 nH in power loop are achieved in the two power modules, respectively.

1.2 Review of SiC Power Module Packaging Technologies

Although conventional wire bonding packaging is mostly used in commercially available power modules for SiC devices, such as low voltage (<1200 V) 62 mm and medium-voltage (3.3 – 6.5 kV) XHP^{TM} 3 industry standard packages, as shown in Fig. 1.2, there are lots of research conducted in the last decade on novel packaging structures to address the limitations of standard packages on high speed switching and high temperature operation. Some of the recent advanced packaging technologies are introduced below.

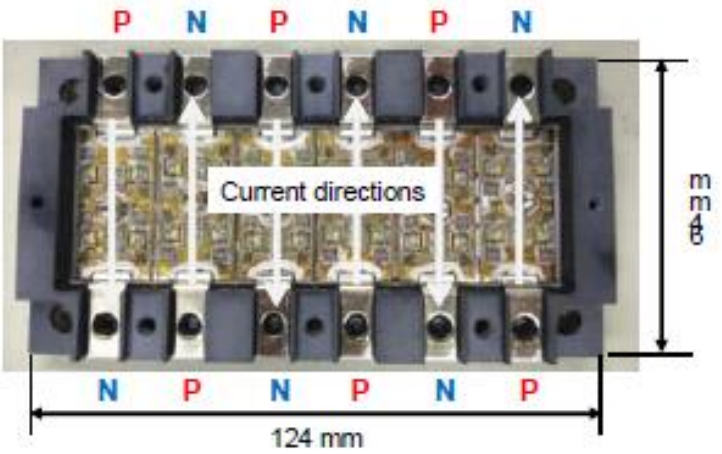
(a) (b)

Fig. 1. 2 (a) A 62mm standard package, and (b) a XHP^{TM} 3 standard package.

1.2.1 Improved Wire Bonding Packages

Commercially available SiC power module using standard wire bonding packages could bring high parasitic loop inductance (> 15 nH). Considering the high switching speed of SiC device, the large parasitic inductance will cause high voltage spike and oscillation on switch devices, as well as high loss [9]. With the help of advanced packaging structures, ultra-low parasitic inductance can be achieved, hence the high frequency switching operation can be achieved with high efficiency. Some of the novel packaging methods utilize and optimize existing wire bonding technologies,

such as developing an antiparallel phase leg unit configuration to resolve the issue of the mutual inductance among the paralleled phase leg units, which leads to ultra-low parasitic inductance of 3.8nH [10], as shown in Fig. 1.3 (a); or utilizing multi-layer hybrid substrates (DBC + PCB) which allows the power loop current to go vertically between substrates and creates current commutation between them, hence greatly reduces the power loop inductance to several nH [11], as shown in Fig. 1.3 (b).



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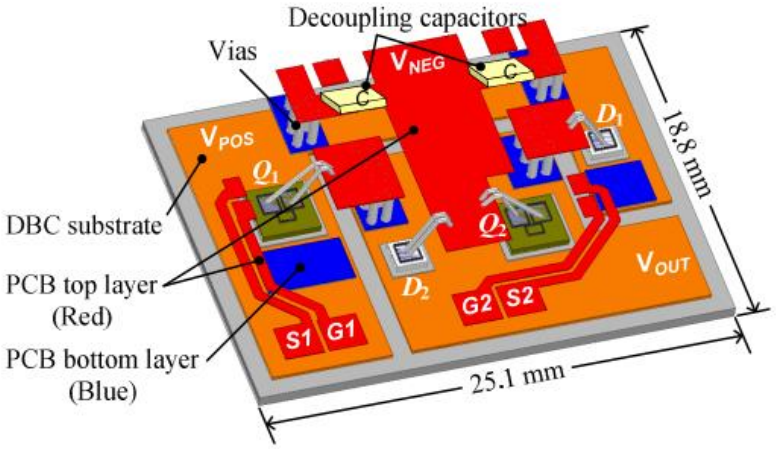


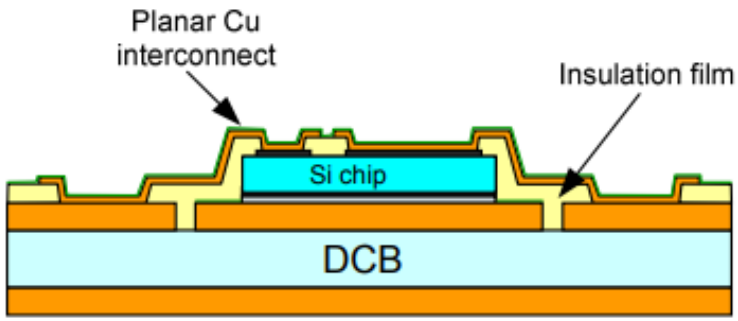
(b)

Fig. 1. 3 Improved wire bonding packages [10] [11].

1.2.2 Novel Wire Bondless Packages

Other attempts are made to achieve wire-bondless structure and 3D integration, considering the reliability issue related to wire bond fatigue [12] and the potential big performance improvement coming with 3D technology. Lots of interconnection methods to replace bonding wires have been researched, the examples include the planar interconnect technology using thick Cu for

interconnection on a high-reliable insulating film on top side of power semiconductor dies, which can reduce the stray inductance by 50% (about 5 nH) due to the reduction in the loop area for current [13], as shown in Fig. 1.4 (a); and the SkiN technology with a flex printed circuit board sintered on top of power dies for interconnection, which can reduce the loop inductance to be less than 5 nH because of the reduced loop height [14], as shown in Fig. 1.4 (b).



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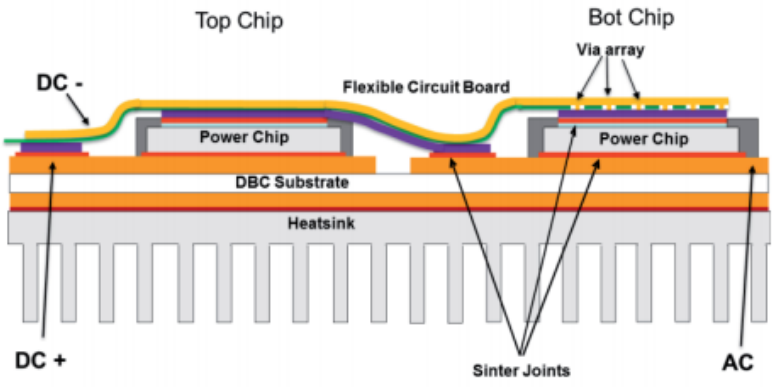


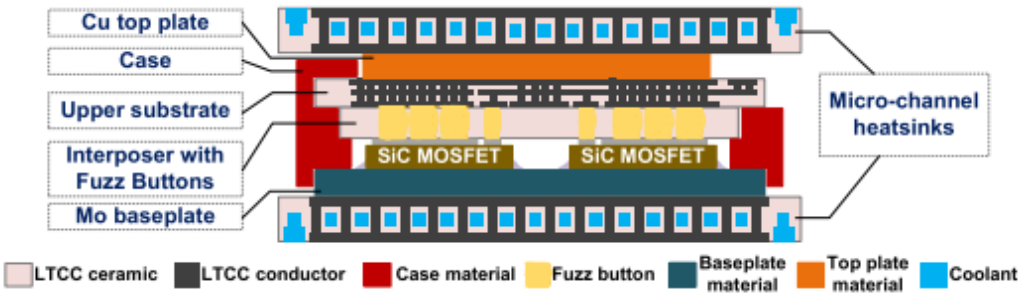
(b)

Fig. 1. 4 Novel wire bondless packages [13] [14].

1.2.3 Double-sided Packages

SiC power devices can operate at high temperature and achieve high power density, which means the SiC power module packages can have high power dissipation during operation and need

advanced thermal management system. Double-sided packages with substrates on both top and bottom of the power module allow the heat to dissipate from both top and bottom sides of the power devices, besides, the increased contact area on top side of the die compared to wire bonding structure allows more uniform temperature distribution of the package, hence reduce the maximum junction temperature of power devices and the thermal resistance [15]. Examples include the press-pack package [16], as shown in Fig. 1.4 (a), and 3D planar-bond-all package [17], as shown in Fig. 1.4 (b).



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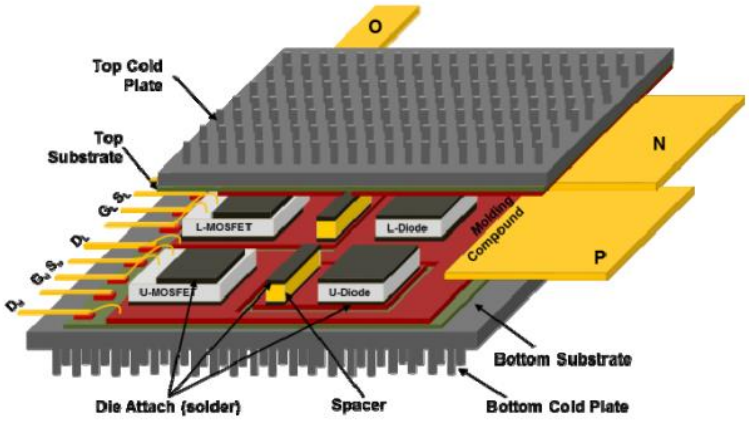

(b)

Fig. 1. 5 Double-sided packages [16] [17].

Based on the literature review, the trend of SiC module packaging is: optimized layout, advanced interconnection technologies, and efficient cooling system for high performance and high reliability [18].

A comparison of some SiC module packages utilizing state-of-the-art approaches is presented in Table 1.2. The proposed module designs in this dissertation research are comparable with or better than most of the state-of-the-art approaches regarding electrical and thermal performance, but there are also some challenges and trade-offs regarding reliability and manufacturing complexity, these concerns are discussed in the dissertation by thermos-mechanical simulation, thermal-cycling test, and fabrication process.

Table 1. 2 Comparison of the state-of-the-art power module packages

Organization	Interconnection	Power loop inductance (nH)	Cooling method	Power density (kW/L)
VT [11]	wire bonding	3.8	Single-sided	not given
VT [19]	wire bonding	8.0	Single-sided	7.80
TH Rosenheim [13]	planar copper	5.5	Single-sided	not given
RWTH Aachen [20]	copper ribbon	4.8	integrated micro-channel	70.9
ORNL [17]	copper-molly post	1.7	Double-sided	not given
Denso [21]	laminated busbar	10.6	Double-sided	100

1.3 Objectives of Dissertation

The objective of this dissertation research is to develop a working and reliable multiple chip integrated wire-bondless stacked power electronic module, which is electrically tested to specification, compare to simulations, and utilizes both vertical and lateral paths for cooling, to

achieve a low parasitic inductance SiC power module with advanced cooling. Low temperature co-fired ceramics (LTCC), a multilayer ceramic substrate, will be used as interposer in the module. A half-bridge module with parallel SiC devices will be defined in the packaging structure using multi-chip vertical stacking. An all-sided heat management system is proposed to solve thermal issues in this architecture. To achieve the objective, following works will be accomplished:

a) Investigate and utilize materials having high in-plane thermal conductivity in order to remove heat near bare die power devices horizontally along the long edges of module.

b) Development of a novel, multi-stage assembly process to achieve component placement in at least five stacked layers.

c) Design and optimize the double-sided stack module with LTCC interposer, the wire-less interconnection will be achieved by copper balls, conductive through vias and traces in/on the LTCC interposer.

d) One half bridge module with four SiC MOSFETs integrated will be fabricated, every two of which will be paralleled to compose a switching position allowing high current. The performance of the module will be evaluated by simulations and experiments.

Moreover, a medium-voltage (3.3-kV) wire bondless package for a SiC MOSFET based dual common source module is achieved, the objective of the package design is to solve the problems including partial discharge at triple point, high voltage isolation and thermal management associated with medium-to-high voltage power modules. The simulation, module fabrication, and tests are performed for the proposed package design.

1.4 Organization of Dissertation

This dissertation is organized as follows:

Chapter 2 introduces the design of a 900-V double-sided stack wire-bondless SiC power module with LTCC interposer, the electrical, thermal, and thermo-mechanical simulation results for the proposed module design are presented. Next, the fabrication and characterization of the proposed module are performed in Chapter 3. In Chapter 4 and 5, investigation of thermal materials with high thermal conductivity are conducted, including nano-diamond, graphene, and pyrolytic graphite sheet (PGS), in order to improve the thermal performance of the LTCC interposer. The application methods and thermal test results of the candidate materials mentioned above are presented. In Chapter 6, another double-sided wire-bondless package design for a medium-voltage (3.3-kV) SiC power module is introduced, as well as the simulation and test results. Finally, Chapter 7 concludes the work in the dissertation and proposes possible future work for continued research.

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Chapter 2 Design of a 900-V Double-Sided Stack Wire-Bondless SiC Power Module with LTCC Interposer

One of the most import goals of the new power module packaging design is to ensure the performance of the SiC power devices. For example, the high switching speed enables the SiC device to work at high switching frequencies up to several MHz with low switching losses. This makes the mitigation of parasitic parameters become a critical performance parameter, because a higher di/dt causes a larger voltage overshoot and ringing [1] with a similar parasitic inductance. Another outstanding property of the SiC device is its capability to operate at high junction temperatures up to 500℃ [2], which requires packaging materials to be able work reliably at these high temperatures and to have a similar coefficient-of-thermal-expansion (CTE) matching that of the SiC power devices. In this chapter, the detailed design of the proposed stack wire-bondless power module with LTCC interposer and double-sided cooling is presented, as well as the simulation results, including parasitic inductance extraction and thermo-mechanical simulation.

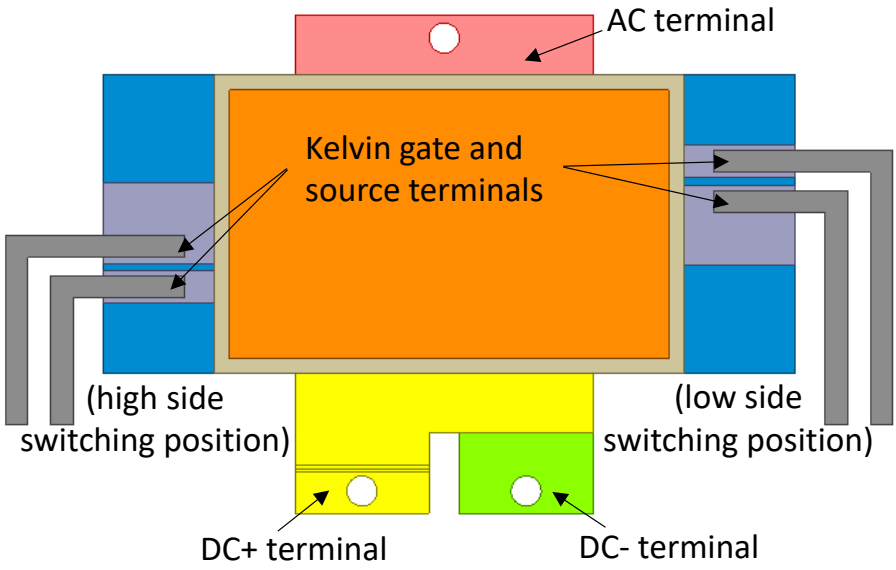
2.1 Design of a Stack Wire-Bondless Half-Bridge Power Module

Fig. 2.1 (a) and (b) show the top view and side view of the stack wire bondless power module, respectively. As can be seen, a half bridge module is defined, with two SiC MOSFETs bare dies in parallel in each switching position. The MOSFETs are from CREE (Part No. CPM3-0900-0010A) with a fast intrinsic body diode and low reverse recovery, which eliminates the need for external anti-parallel diodes [3]. The MOSFET bare dies are flip-chip bonded onto a LTCC multilayer interposer, which provides both electrical and thermal routings in the power module. Nickel (Ni)-plated copper (Cu) balls are used for flip-chip bonding to achieve the interconnections between SiC devices and LTCC substrate, the Cu ball is selected because of its high electrical and

thermal conductivity compared with traditional solder ball. The power module consists of two direct bond copper (DBC) substrates at top and bottom, which act as die attachment substrates and also provide vertical double-sided cooling. As a result, the gate and source pads on top of the MOSFET bare die are routed through Cu balls and conductive traces on LTCC interposer to the outer terminals, while the drain pad at back of the bare die is soldered to the DBC substrates on which power terminals are attached on. Besides, the MOSFET attached on one side of the LTCC interposer is face to face connected to the MOSFET at the other side by conductive through vias in the LTCC interposer, forming a parallel pair in the high side or low side switching position of the half bridge module.

Fig. 2.1 (c) shows the exploded view of the stack module as well as the current loops. As can be seen, the current flows from DC+ terminals to the DC- terminal through the MOSFETs at high side switching position and the intrinsic body diodes of the MOSFETs at low side. On the other hand, there is a return current loop through the MOSFETs at low side switching position and the intrinsic body diodes of the MOSFETs at high side. As a result, the opposing forward and return current partially cancel which helps reduce the power loop inductance because the DC+ and DC- tracks are close on top of each other [1][4].

The copper sheet made DC+ and DC- terminals are on one side of the module, while the AC terminal is on the opposite side. This allows for easy direct bus bar connection and facilitates the double-sided cooling by inserting the module into a slot with cooling plates on both sides [5], as shown in Fig. 2.2.



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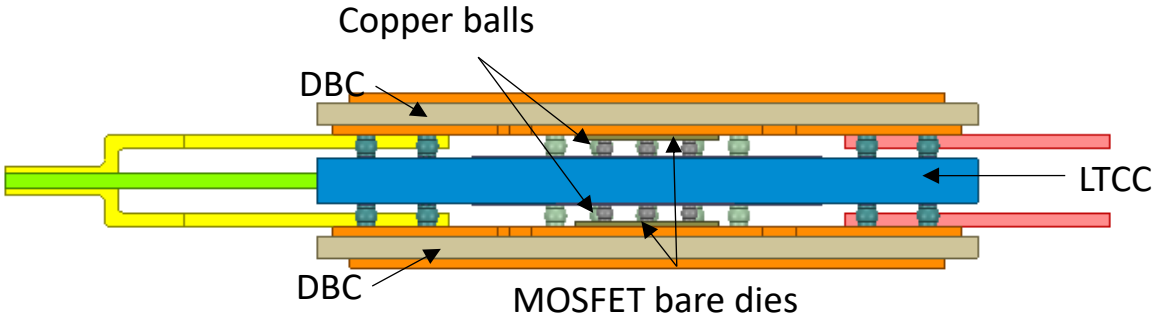
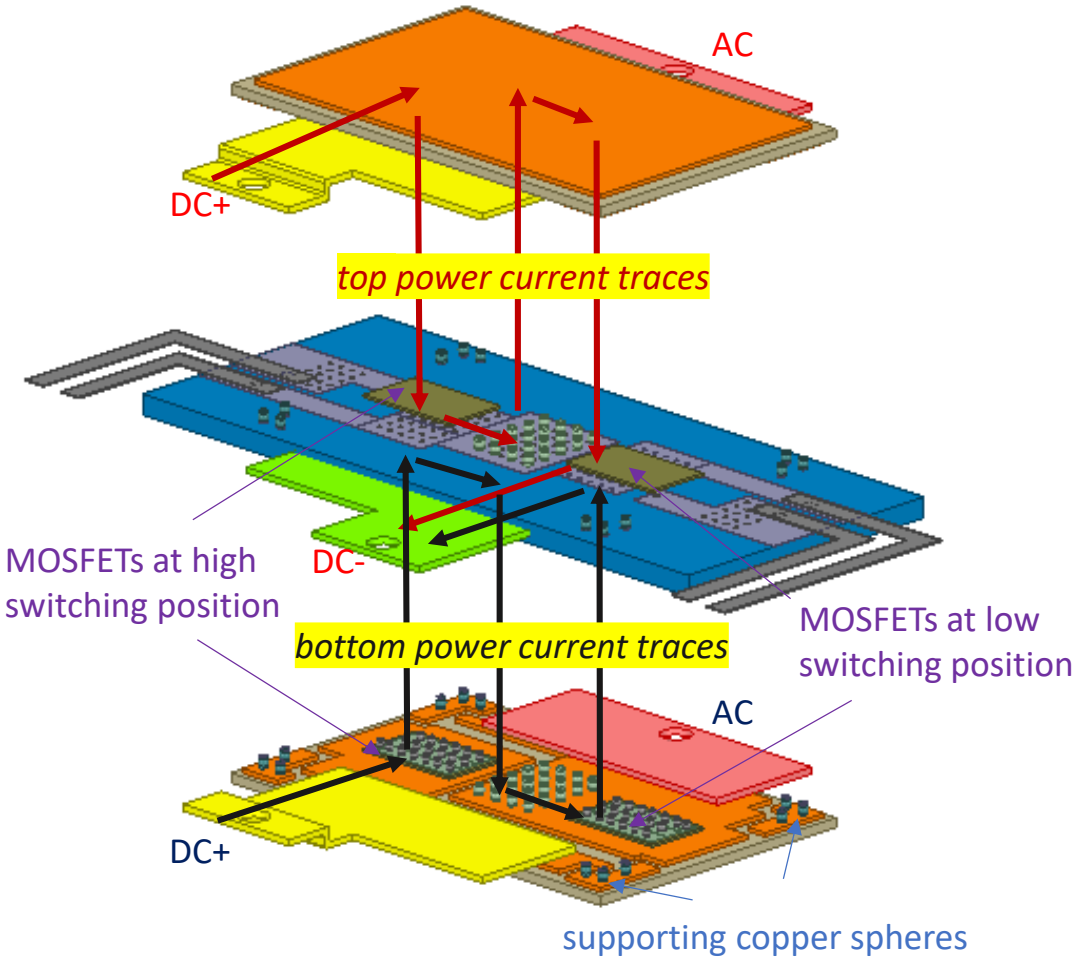


(b)

Fig. 2. 1 (a) Top view, (b) Side view, and (c) Exploded view & current loops of the double-sided stack power module structure.



(c)

Fig. 2. 1 Cont. (a) Top view, (b) Side view, and (c) Exploded view & current loops of the double-sided stack power module structure.

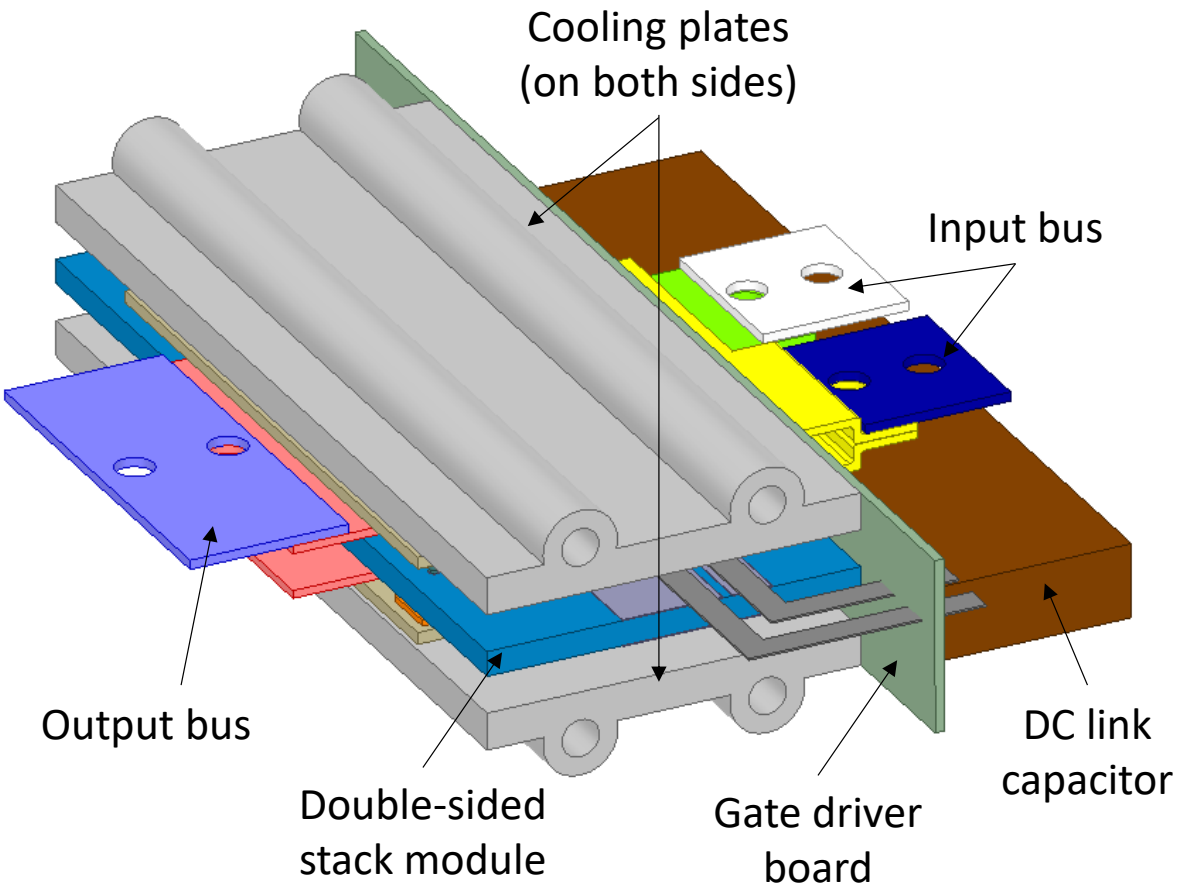


Fig. 2. 2 A double-sided cooling concept for the stack module.

2.2 Design of LTCC Interposer

LTCC interposer is multilayer structure providing electrical paths in the power module. DuPont™ GreenTape™ 9K7 is used to prepare the LTCC interposer, the GreenTape™ 9K7 system provides a complete co-fireable system with gold or silver components having excellent low loss at high frequency [5]. There are six layers in the designed LTCC interposer, as shown in Fig. 2.3. The first and sixth layer (L1 and L6) has solderable silver paste printed on it to form gate and source pads for the SiC MOSFET bare dies to flip-chip attached on, through vias filled with conductive silver paste in the six layers (L1~L6) forms interconnection between layers hence connection between

gate and source pads on L1 and L6, as a result, the devices attached on the top and bottom surfaces of the LTCC interposer are connected in parallel. The first three layers (L1~L3) hold a cut out for the DC- terminal, which is soldered on the solderable pad on the fourth layer (L4).

In order to fabricate the multilayer LTCC interposer, each layer of green tape is punched to form vias, then printed or filled with silver pastes, after that, the layers are laminated together in order to form the multilayer structure. The detailed fabrication process will be introduced in Chapter 3.

Nowadays, silicon and glass have been developed and utilized as interposers because of their advantage of high I/O density and the good thermal performance with through-package vias (TPVs). However, silicon interposer has high electrical loss, and glass interposer has very low thermal conductivity of 0.8 – 1.0 W/(m*K), moreover, only TPVs can be built within both of them to enhance their performance. On the other hand, LTCC multilayer structure can accommodate complex interconnection both externally and embedded within the interposer, which allow for design flexibility for both electrical and thermal power routes in the power module.

Despite LTCC can achieve both horizontal and vertical electrical interconnections, it has a limitation on thermal performance. The thermal conductivity of the LTCC green tape is 4.6 W/(m*K), which is much lower than DBC substrate. To overcome the thermal management issue with LTCC, thermal vias filled with high thermally conductive materials are a primary option to remove the heat generated from the power devices. Meanwhile, to improve the heat dissipation in the horizontal direction of LTCC, materials with high in-plane thermal conductivity can be integrated into the LTCC interposer. Some candidate materials and their impact will be discussed in Chapter 4 and 5.

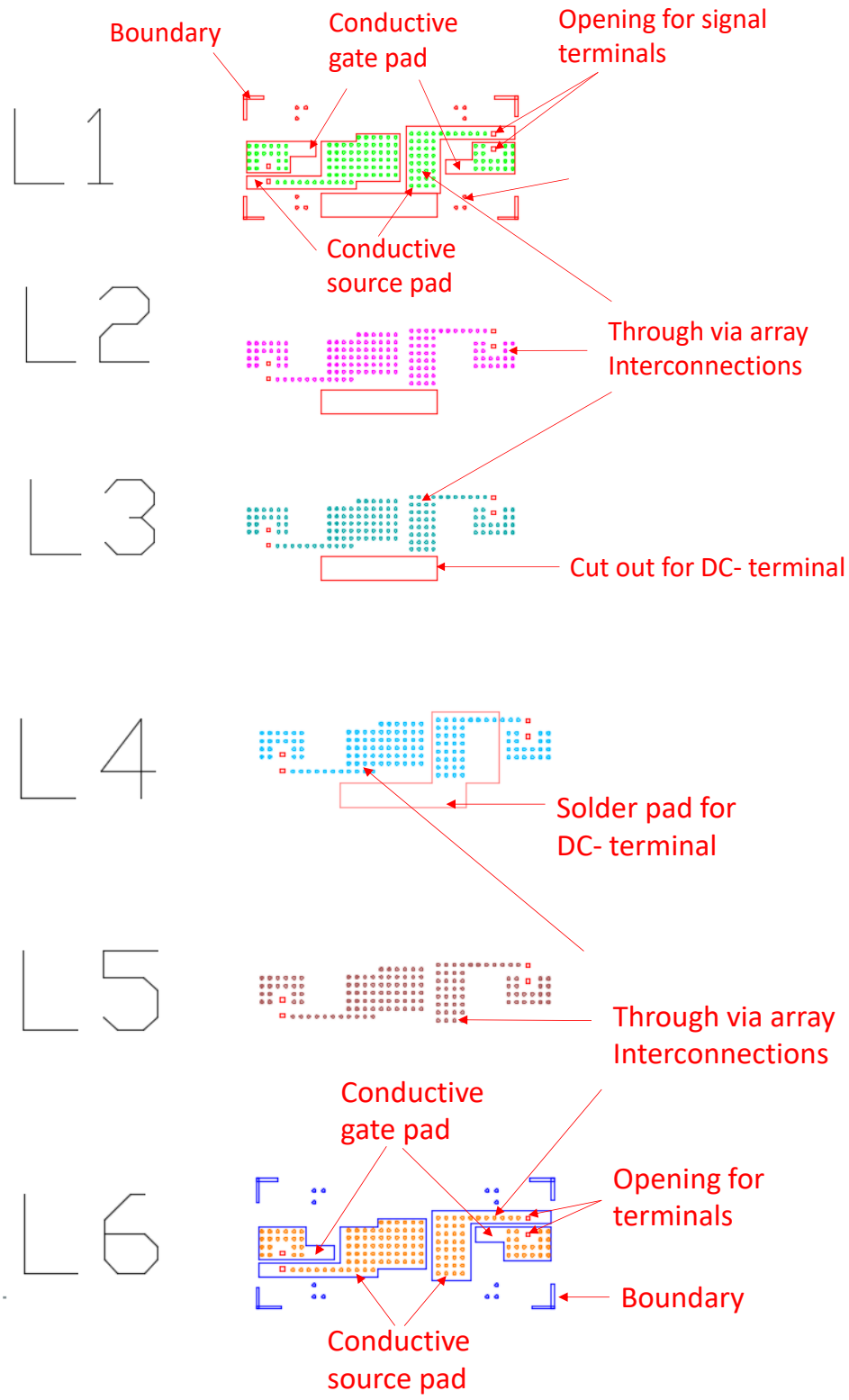
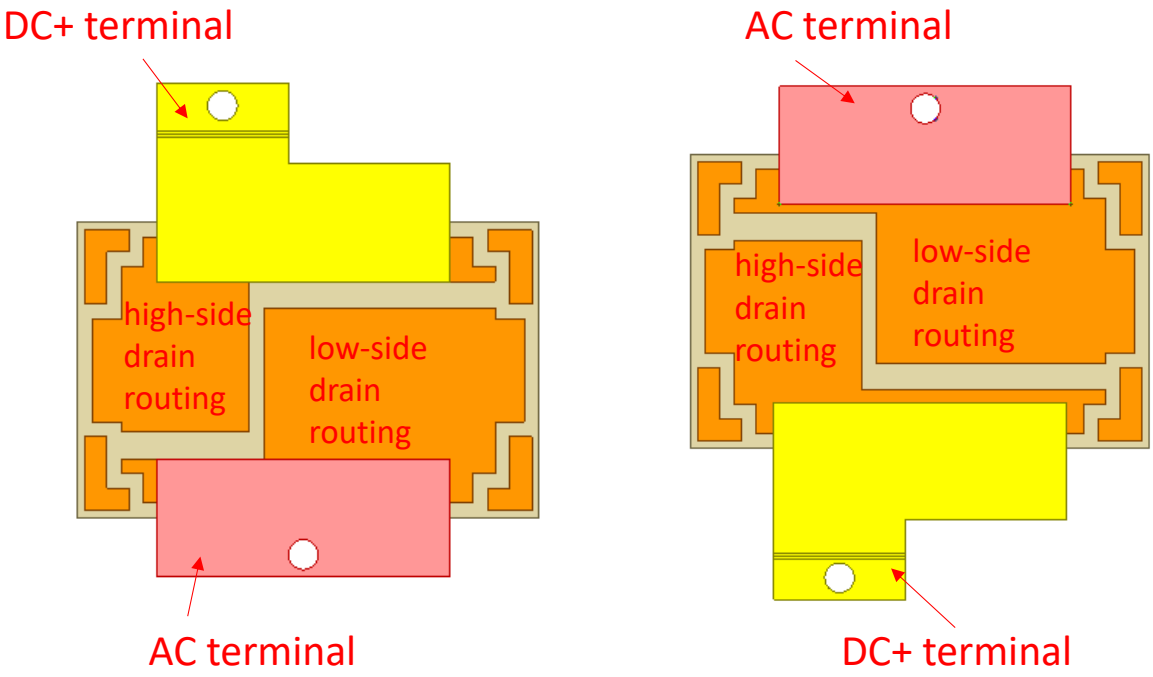


Fig. 2. 3 Six layers in the designed LTCC interposer.

2.3 Design of DBC Substrates

The DBC substrates on top and bottom of the power module provide drain routing of the SiC MOSFETs, as well as thermal spreader for the module. The designs of top and bottom DBC substrates with terminals soldered on them are shown in Fig. 2.4 (a) and (b), respectively.



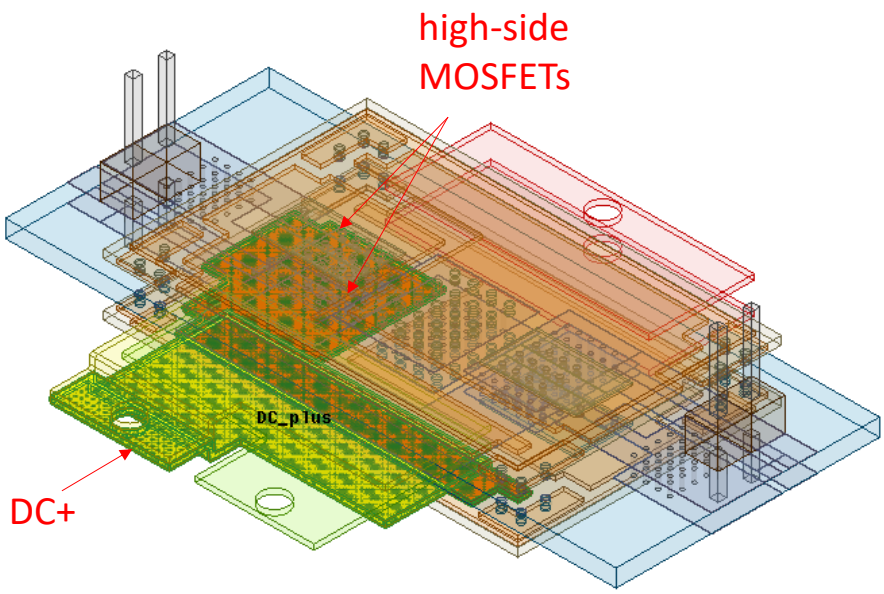
(a) (b)

Fig. 2. 4 (a) Top and (b) bottom DBC substrate design with DC+ and AC terminals.

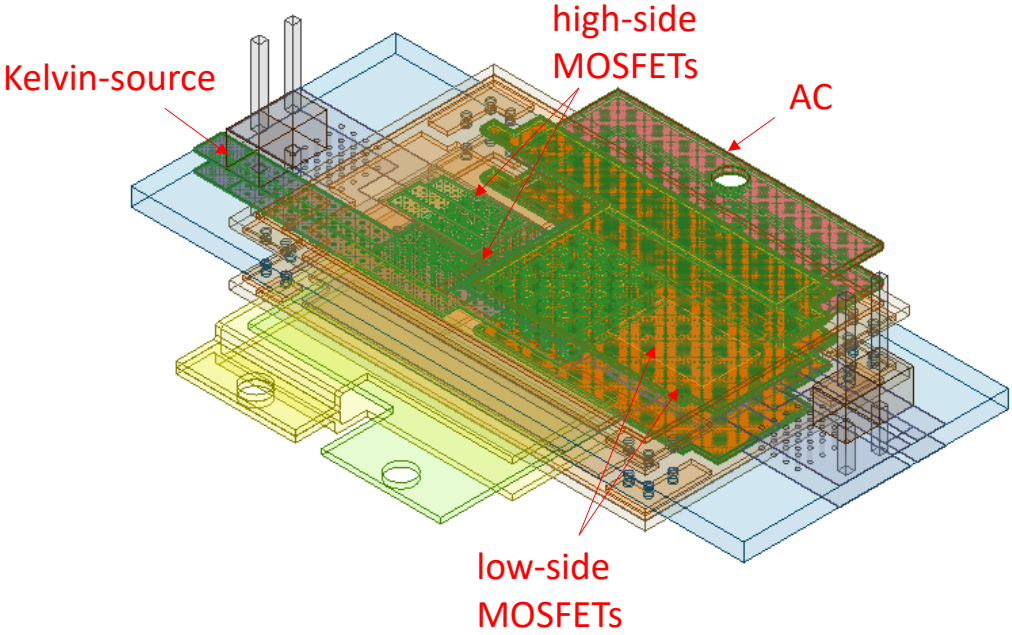
2.4 Parasitic Inductance Extraction

As mentioned earlier, the stray parasitic inductance induced by the power module packaging plays an important role on the switching performance and power losses of the SiC devices when operating at high switching frequency. In order to investigate the parasitic inductance, Ansys Q3D Extractor was used to simulate and extract the parasitic inductances within the proposed wire-bondless module, based on the simulation results, the module packaging design can be optimized

to minimize the stray parasitic inductance [6]. Fig. 2.5 shows the conducting nets assigned for the parasitic inductance extraction. Fig. 2.5 (a) shows the DC+ net, which is assigned to extract the parasitic inductance from DC+ terminals through DBC copper traces to the drain pads of the MOSFETs at high-side switching position. The common net is shown in Fig. 2.5 (b), it represents the parasitic inductance path from the AC terminal to the source pads of the high-side MOSFETs through DBC copper traces, copper balls and LTCC conductive traces, as well as to the drain pads of the low-side MOSFETs through DBC copper traces. The DC- net as shown in Fig. 4.5 (c) corresponds to the parasitic inductance path between DC- terminal and source pads of the MOSFETs at low-side switching position through LTCC solder pads, conductive through vias, and copper balls, the Kelvin source loop inductance from Kelvin source pin through LTCC conductive traces and copper ball interconnection to source of the low-side MOSFETs is also shown in this net. The Kelvin-connected source pin is used as a reference potential for the gate driving voltage, which can eliminate the effects of large voltage drop in power loop and reduce the switching losses due to the negative feedback caused by the parasitic inductance in the power source terminal [7]. Fig. 4.5 (d) shows the Kelvin gate net for the low-side devices between the Kelvin gate pin and the gate pads. Fig. 4.6 shows the model of the parasitic inductance for the proposed double-sided stack half-bridge module with two MOSFETs in parallel in each switching position. As shown in the model, the power loop inductance includes the DC+ inductance (L-HD) in DC+ net, the common inductance (L-HS and L-LD) in common net, and the DC- inductance (L-LS) in DC- net. While the gate loop inductance consists of L-HG / L-LG in Kelvin gate net and L-HS / L-LS in common net / DC- net for MOSFETs at high-side and low-side switching positions, respectively.

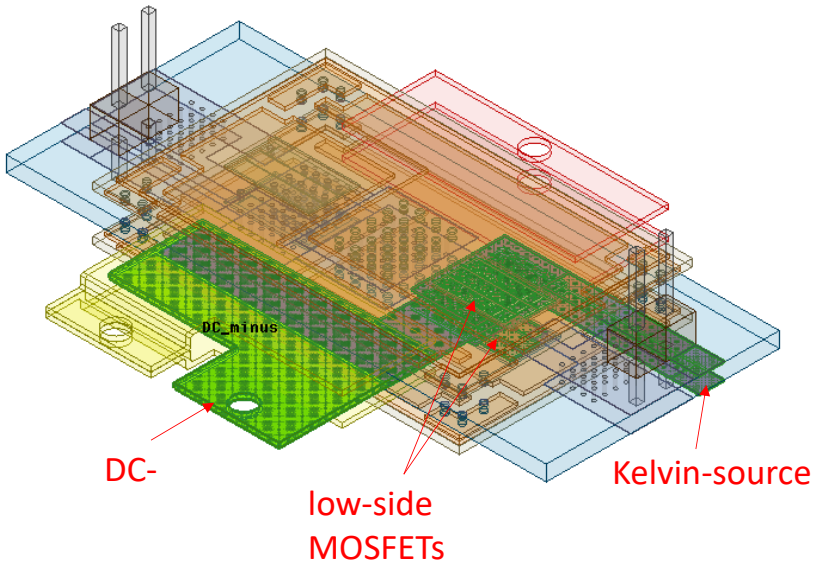


(a)

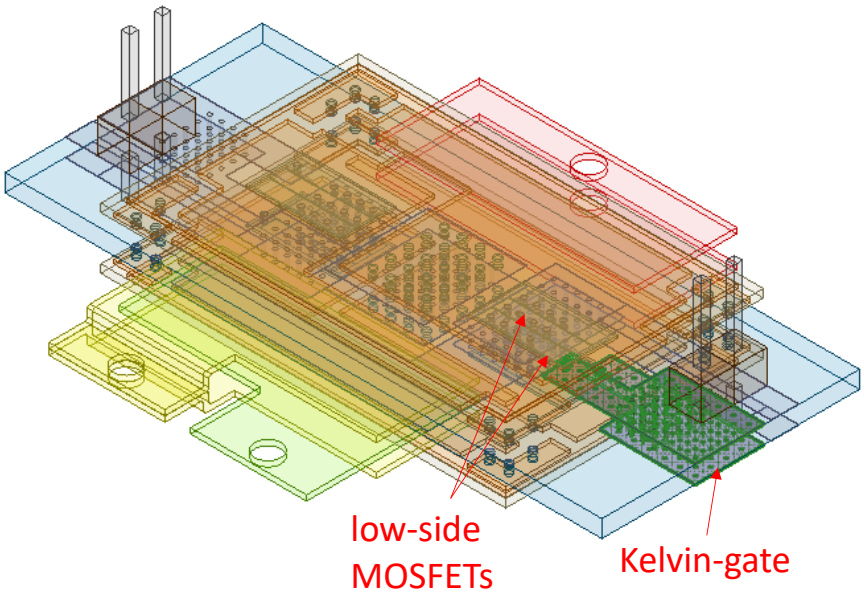


(b)

Fig. 2. 5 (a) DC+ net, (b) common net, (c) DC- net, and (d) kelvin gate net assigned for parasitic inductance extraction in the proposed wire-bondless module package.



(c)



(d)

Fig. 2. 5 Cont. (a) DC+ net, (b) common net, (c) DC- net, and (d) kelvin gate net assigned for parasitic inductance extraction in the proposed wire-bondless module package.

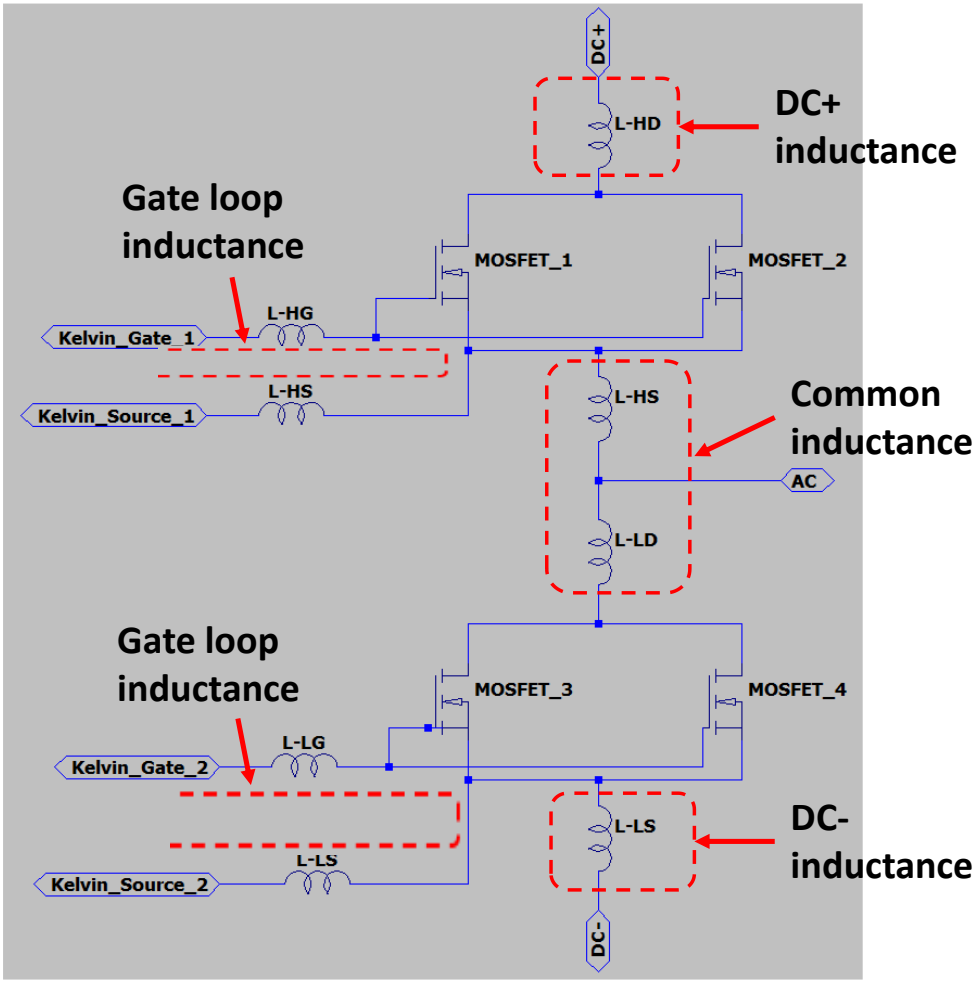


Fig. 2. 6 Model of the parasitic inductance of the proposed half-bridge module package.

The simulated frequency-dependent parasitic inductance results for the proposed wire-bondless half-bridge module are shown in Fig. 2.7. As can be seen, the gate loop inductance is about 4.8 nH at 1MHz, the low gate loop inductance can help reduce the ringing in the gate voltage. The critical stray inductance between DC+ and DC- terminals which affects ringing and overshoot in the power loop can be calculated using the equation below:

$$L_{power-loop} = L_1 + L_2 + L_3 + 2 \times (M_{12} + M_{23} + M_{13}) \quad (4.1)$$

Where L_1 is the DC+ inductance, L_2 is the common inductance, L_3 is the DC- inductance, and M_{xy} is the mutual inductance between L_x and L_y [8]. As a result, the simulated power loop inductance can be estimated, as shown in Fig. 2.8, to be about 4.5 nH at 1MHz, which is 40% lower compared to a commercial low inductance (7.5 nH) SiC wire-bondless half-bridge module also using double-sided cooling and current cancellation strategy [9].

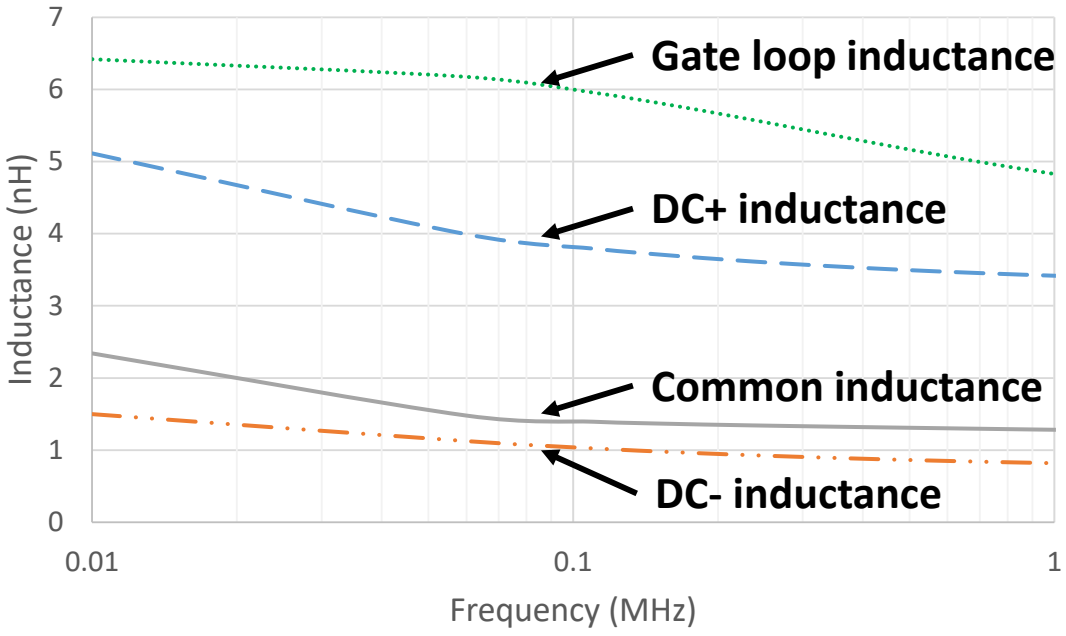


Fig. 2. 7 simulated frequency-dependent parasitic inductance by Ansys Q3D.

In order to validate the simulation results of parasitic inductance for the power module, a Bode 100 impedance analyzer was used to measure the parasitic inductance using a mechanical module with a continuous path between the DC+ and DC- terminals, since this method can only measure the parasitic inductance in conductive paths. The measured results are shown in Fig. 2.8 to compare with the simulated values. As shown, the simulation indicates reasonable agreement with the measurement at high frequency.

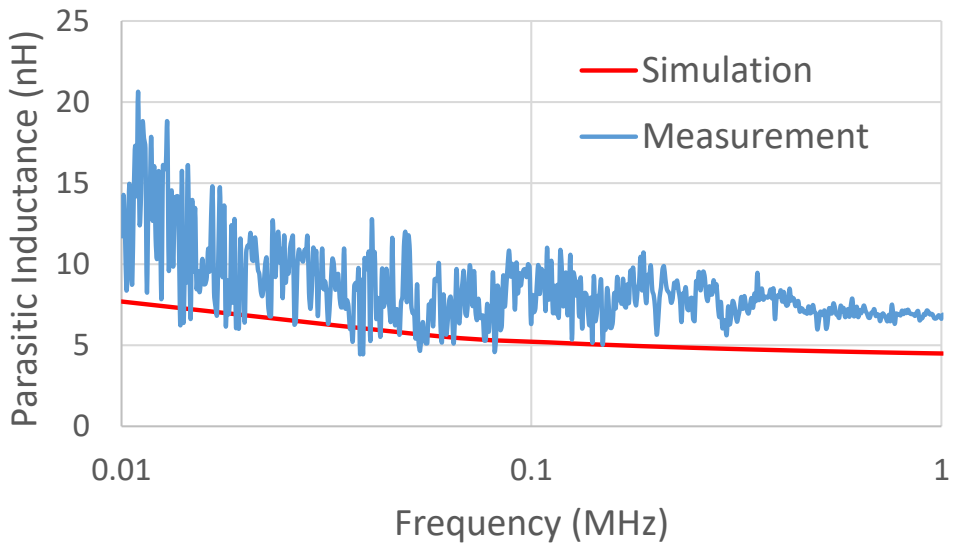


Fig. 2. 8 Simulated and measured power loop inductance between the DC+ and DC- terminals.

2.5 Thermo-mechanical Simulation

The double-sided stack power module consists of several components of different materials that have different coefficients of thermal expansion (CTEs). When current flows through the SiC devices, heat is generated and distributed in the module, developing a temperature gradient. Hence, during operation, the power module frequently subjects to temperature changes, the thermo-mechanical stress resulting from CTE mismatch between different materials can cause defects such as power device cracks, DBC substrate delamination, and bonding wire shifts, which affect the function and reliability of the power module [10] [11]. In this section, the thermo-mechanical simulations were performed to investigate the thermos-mechanical stress of the power modules of different structure and using different materials.

Ansys Workbench was used to perform the thermos-mechanical simulations, the material properties of the components in the power module are shown in Table 2.1. For comparison, three cases were studied. The first case is the proposed double-sided module package with Cu-AlN-Cu

DBC substrates, the second case is the same double-sided structure but with Cu-Al_2O_3-Cu DBC substrates, and the third case is single-sided power module with Cu-AlN-Cu DBC substrates.

Table 2. 1 Material properties of the components in the power module

Component	SiC die	Copper	AlN	Al_2O_3	SAC305 solder	LTCC
CTE (ppm/°C)	4.0	18	4.5	8.4	23.5	4.4
Density (g/cm^3)	3.1	8.3	3.26	3.89	7.4	3.1
Young's modulus (GPa)	410	110	344	370	51	145
Thermal conductivity (W/m*K)	120	401	170	35	59	4.6
Poisson's ratio	0.14	0.34	0.24	0.22	0.3	0.25

Due to the symmetry structure, only half of the module for the first case was used for simulation in order to reduce the computation time, as shown in Fig. 2.9. Thermal simulation was performed first, the power dissipation of each device is defined to be 56.25 W, the heat transfer coefficient on DBCs at both sides of the module is set to be 3000 W/(m^2K), and the ambient temperature is assumed to be 25 ℃. Fine mesh in interface layers of the model was applied to get a more accurate result. The thermal simulation result is shown in Fig. 2.10, the maximum device junction temperature is 85.6 ℃. The simulated temperature distribution in the model was then imported for thermos-mechanical simulation, the results are shown in Fig. 2.11, include the Von-Mises stress distribution shown in Fig. 2.11 (a) and the deformation shown in Fig. 2.11 (b) of the model. As can be seen, the maximum stress is 283 MPa, which is located on the copper ball sandwiched between SiC die and LTCC interposer, as shown in Fig. 2.12. This is due to the CTE mismatch between copper ball and SiC die, as well as between copper ball and LTCC interposer. The maximum deformation of 4.94 μm is located at the AlN DBC interface, as shown in Fig. 2.13,

which is because of the large CTE difference and the large contact area between the copper layer and AlN layer of the DBC substrate.

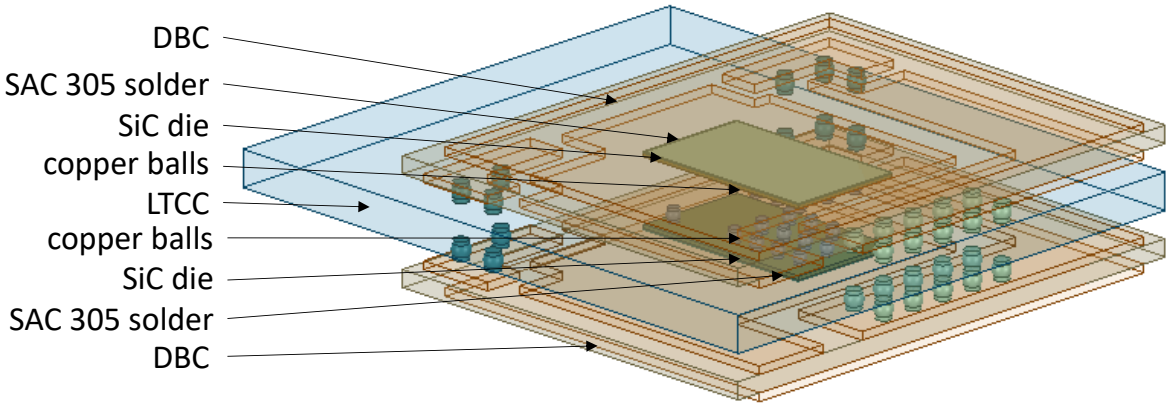


Fig. 2. 9 Thermo-mechanical simulation model of the proposed double-sided stack module.

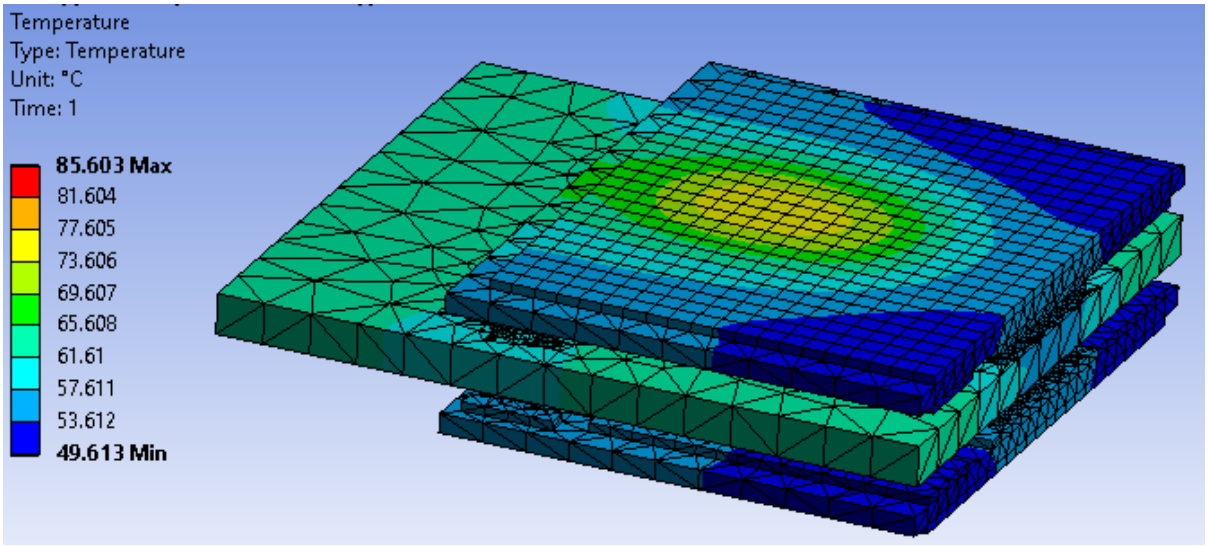
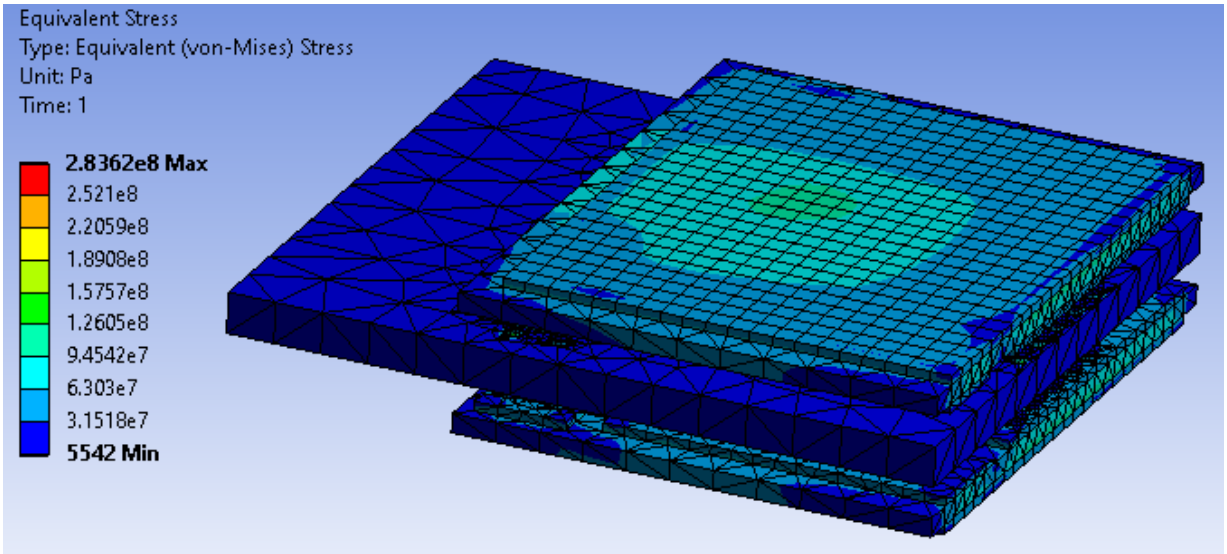
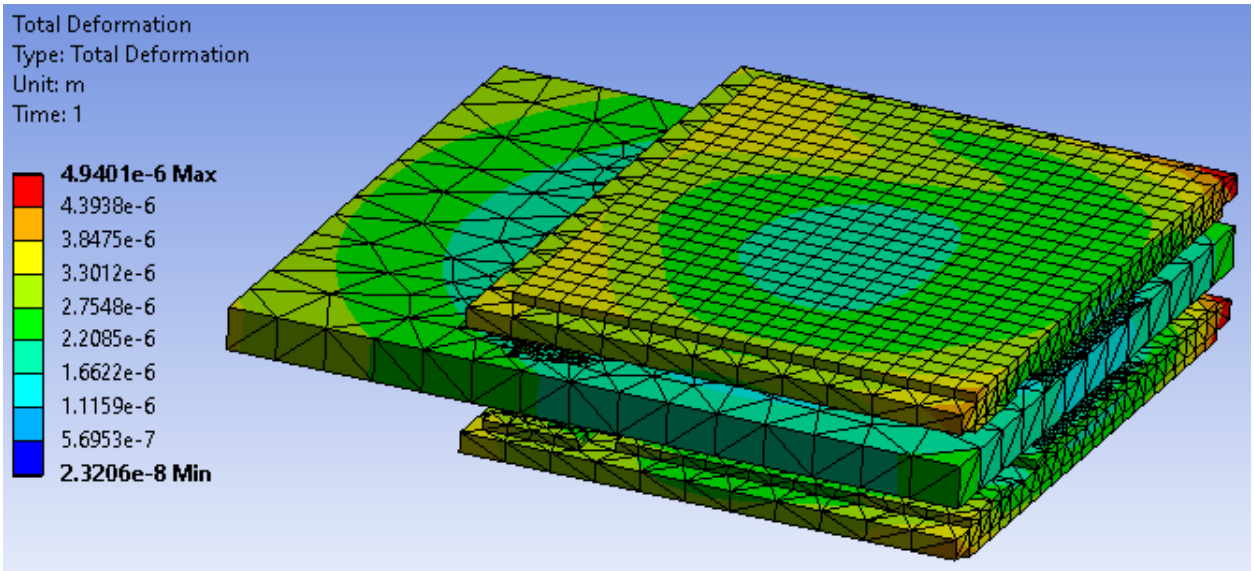


Fig. 2. 10 Temperature distribution of the double-sided stack module with AlN DBC.



(a)



(b)

Fig. 2. 11 (a) Von-Mises stress distribution, and (b) deformation of the double-sided stack module with AlN DBC.

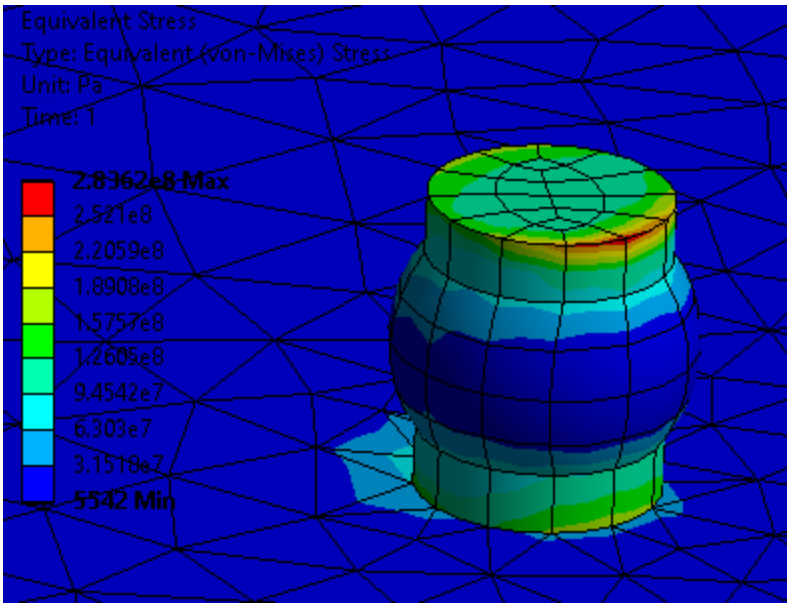


Fig. 2. 12 The Cu ball between SiC die and LTCC interposer having maximum Von-Mises stress in first case.

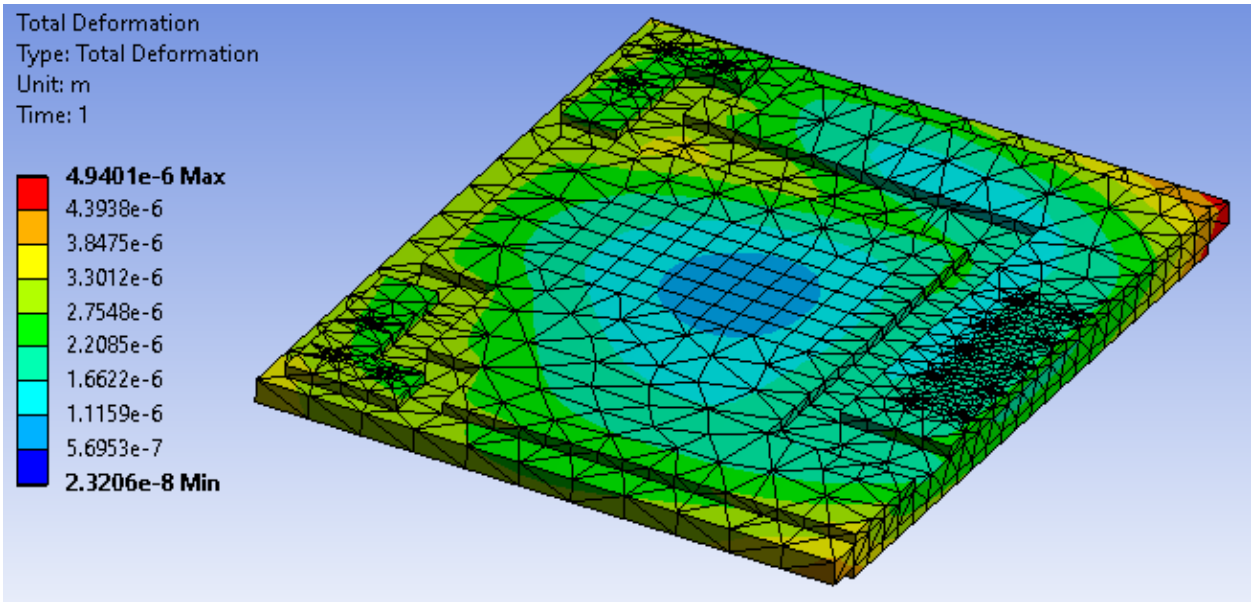
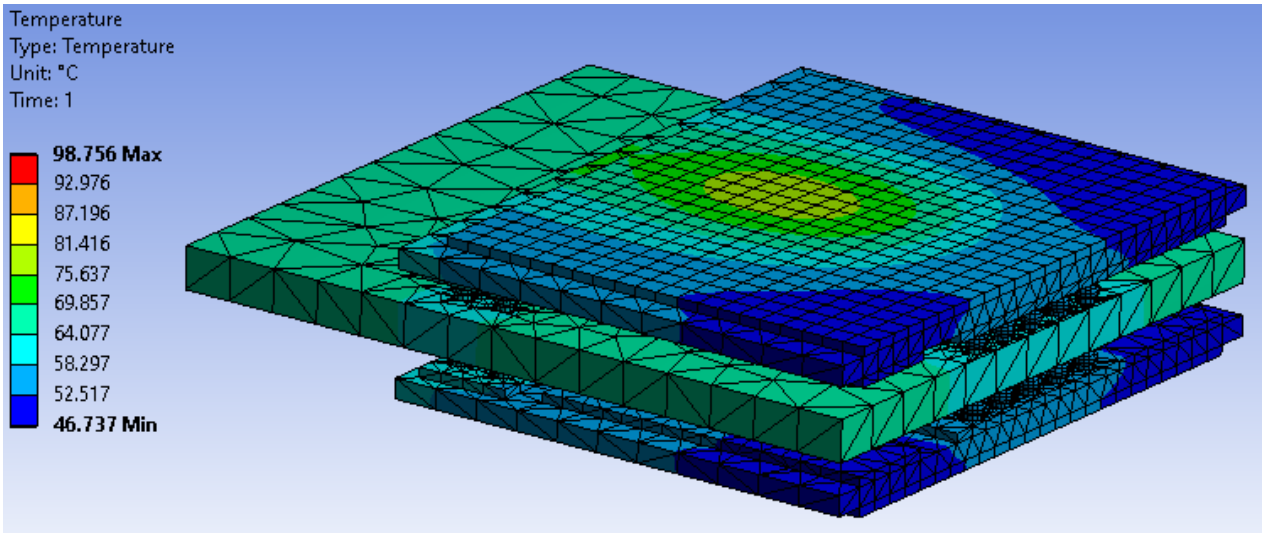


Fig. 2. 13 The AlN of DBC substrate having maximum deformation in first case.

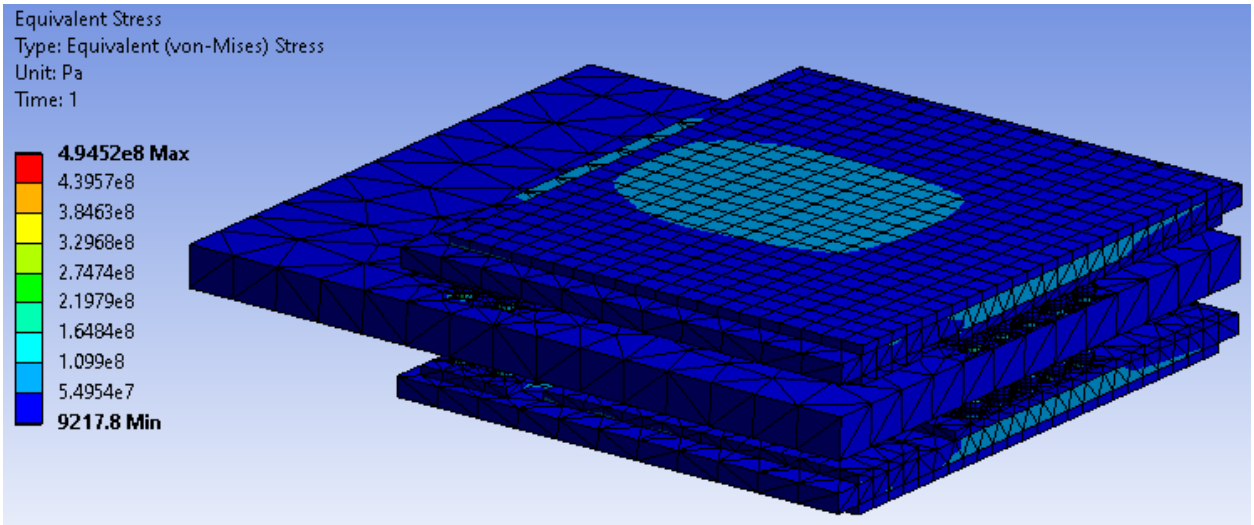
Similarly, the thermos-mechanical simulations were performed for the other two cases. The simulation results for the double-sided structure with Al_2O_3 DBC substrates are shown in Fig. 2.14,

and Fig. 2.15 shows the simulation results of the single-sided model with AlN DBC substrates. Table 2.2 lists the simulation results of the three cases for comparison. As shown, the double-sided model has lower Von-Mises stress and deformation compared to single-sided model using the same materials, which is because the maximum junction temperature in the double-sided model is 37.3 ℃ lower than that of single-sided model benefiting from the double-sided cooling. On the other hand, the use of AlN DBC in double-sided model reduces the Von-Mises stress and deformation due to closer CTE of AlN to SiC. The lower thermal loading stress and deformation help reduce delamination and crack failures in power modules.

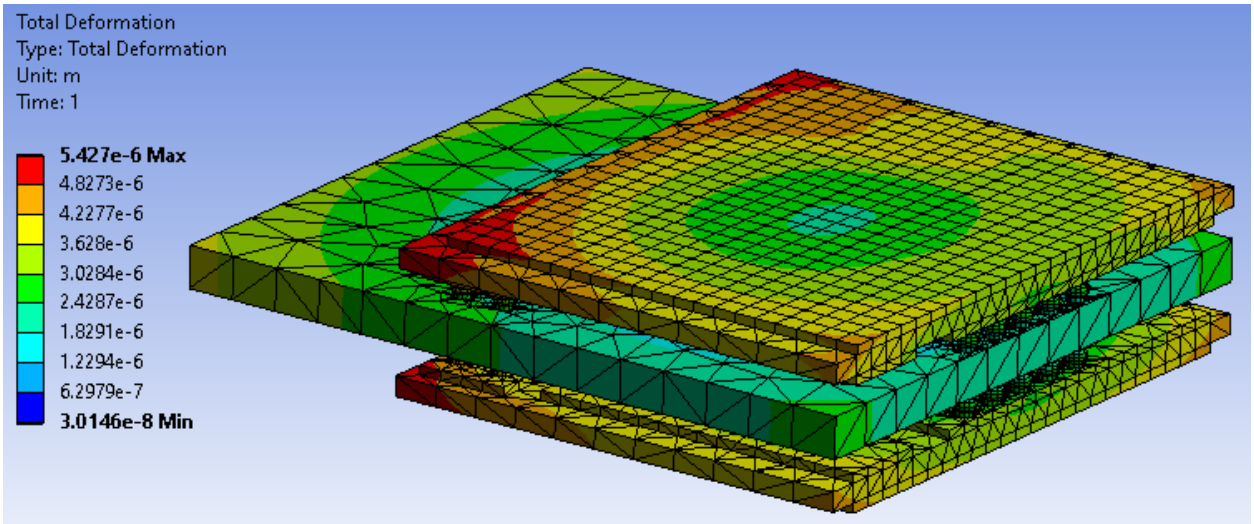


(a)

Fig. 2. 14 (a) Temperature distribution, (b) Von-Mises stress distribution, and (c) deformation of the double-sided stack module with Al_2O_3 DBC.

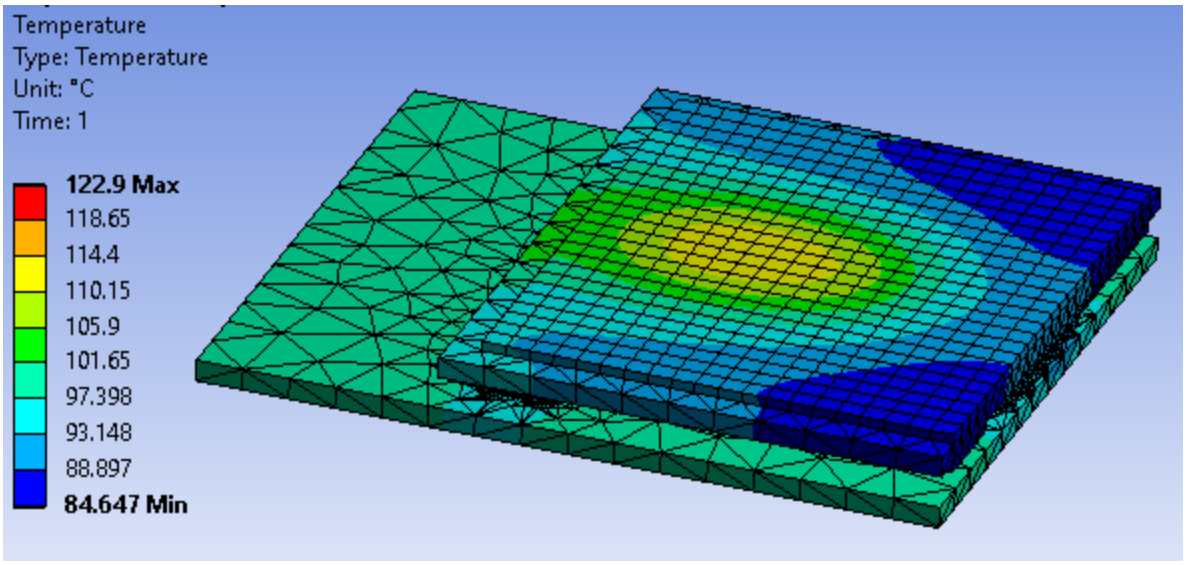


(b)

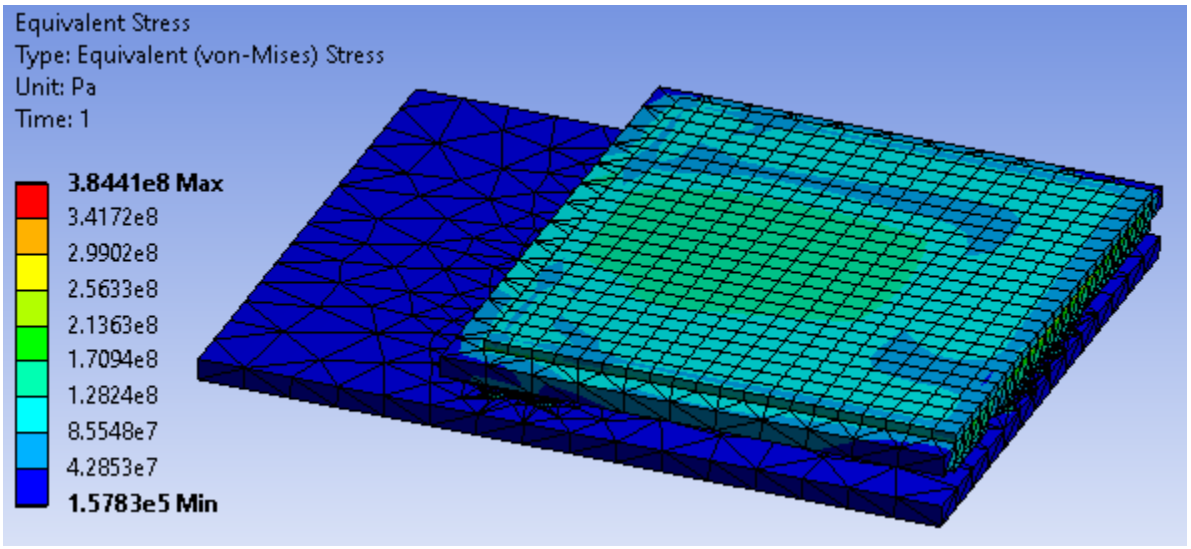


(c)

Fig. 2. 14 Cont. (a) Temperature distribution, (b) Von-Mises stress distribution, and (c) deformation of the double-sided stack module with Al_2O_3 DBC.

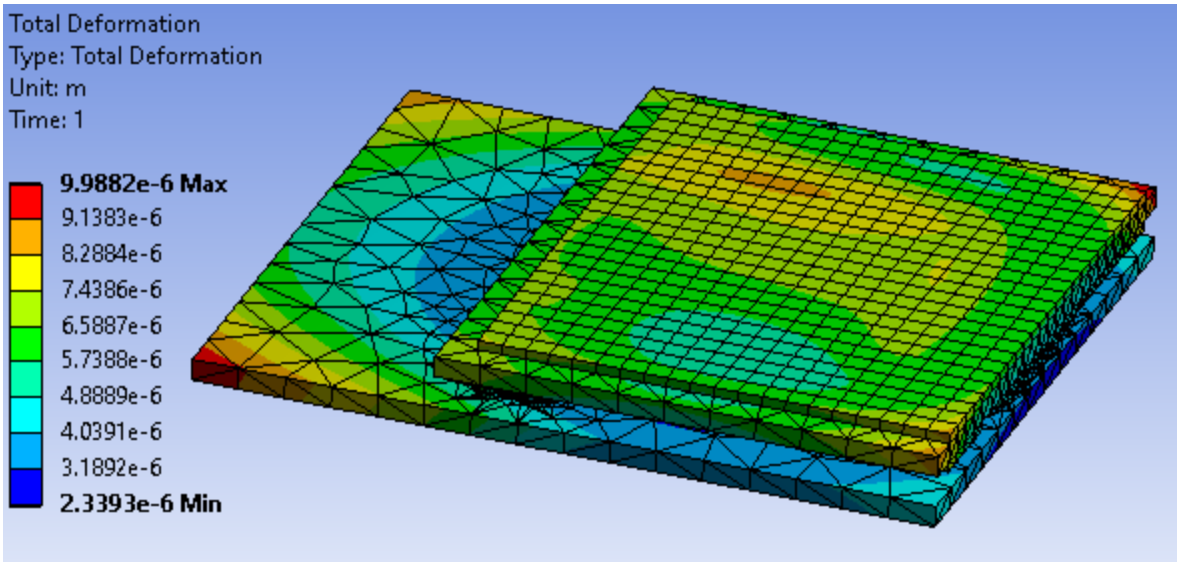


(a)



(b)

Fig. 2. 15 (a) Temperature distribution, (b) Von-Mises stress distribution, and (c) deformation of the single-sided module with AlN DBC.



(c)

Fig. 2. 15 Cont. (a) Temperature distribution, (b) Von-Mises stress distribution, and (c) deformation of the single-sided module with AlN DBC.

Table 2. 2 Thermo-mechanical simulation results comparison

Model	maximum device temperature (℃)	maximum Von-Mises stress (MPa)	maximum deformation (μm)
Double-sided, AlN DBC	85.6	283	4.94
Double-sided, Al_2O_3 DBC	98.7	494	5.42
Single-sided, AlN DBC	122.9	384	9.98

2.6 Chapter Summary

In this chapter, the detailed design of the double-sided stack wire bondless half-bridge module is presented, including the design of LTCC multilayer interposer and DBC substrates. The anti-

parallel current cancellation technique which helps reduce inductance is discussed. The electrical and thermos-mechanical simulations of the proposed power module package are then introduced. The simulated loop inductance of the wire bondless module is less than 5 nH at frequency higher than 1MHz, and the measurement verifies the simulation results. Thermo-mechanical simulation results show the double-sided structure has lower thermo-mechanical stress and deformation compared to single-sided structure, and using materials with matching CTEs help further reduce the thermal loading stress and deformation in the power module, hence lower the risk of delamination and crack.

To improve the thermal performance of LTCC interposer hence the better thermal management in the power module, high thermally conductive materials are investigated in Chapter 4 and 5 to integrate with LTCC.

2.7 References

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Chapter 3 Fabrication and Characterization of a 900-V Double-Sided Stack Wire-Bondless SiC Power Module with LTCC Interposer

In this chapter, the detailed fabrication process of the proposed double-sided stack wire-bondless module is introduced. As part of the dissertation research, a reliable fabrication process development was carried out and optimized in order to build the proposed module. After the fabrication, the electrical and reliability performance characterization were performed and will be discussed in this chapter as well.

3.1 Fabrication of the Proposed Power Module Package

A prototype of the proposed double-sided stack wire-bondless half-bridge module was fabricated, the main steps for the module fabrication include:

I. Bare die pads re-metallization

II. LTCC interposer fabrication

III. DBC substrate fabrication

IV. Flip-chip die attachment and module assembly

The detailed processing steps are described in the following sections.

3.1.1 Die Top Pads Re-metallization

The commercially available SiC MOSFETs from CREE have aluminum (Al) metalized pads on top for gate and source electrodes which are designed for conventional Al wire bonding [1]. However, in the proposed wire-bondless module package, flip-chip bonding is used for die attachment. As such, these Al top pads need to be re-metalized for direct solder attachment with

the nickel (Ni)-plated copper (Cu) balls. Electroless nickel plating is an option for re-metallization, the process is self-patterning which works only on Al surface, thus no additional masking is required and the complexity of the process is reduced. After that, a dry film solder mask is applied onto the re-metalized bare dies and UV patterned to create openings for the Cu balls placement on devices. The Ni-plated Cu balls are covered with solder paste and bonded on the top pads of bare die through a solder reflow process. The process flow is shown in Fig. 3.1.

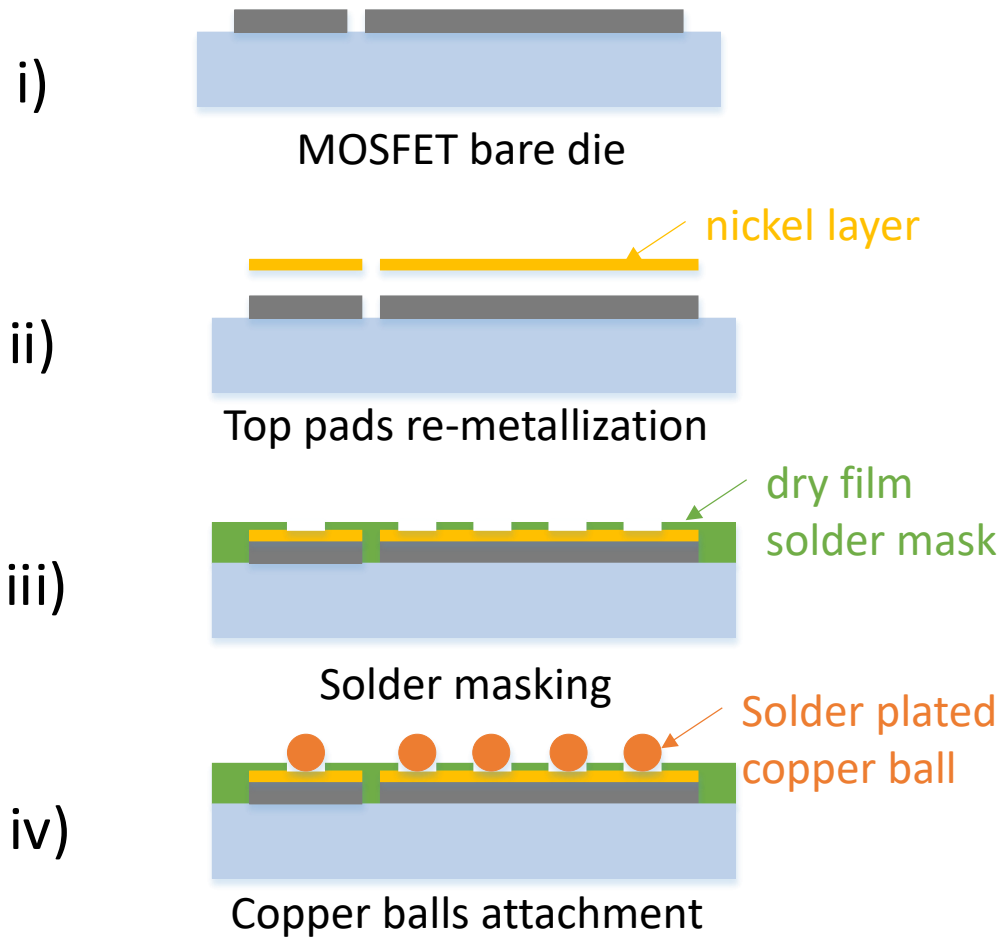


Fig. 3. 1 MOSFET bare die top pads re-metallization process.

The bare die was attached onto a small alumina substrate with double-sided Kapton tape, next, the sample was placed in a plastic holder, as shown in Fig. 3.2, and then placed in a series of electroless plating baths for Ni deposition, as shown in Fig. 3.3. The bare die was cleaned in alkaline soak cleaner first, and then placed in Desmut solution to remove the naturally-occurring oxidation layer of Al surface for a good adhesion with the deposited metal layers [2]. Next, aluminum etchant was used to micro-etch Al, followed by immediate immersion in zincate solution to form a thin and uniform zincate layer for subsequent nickel plating. 50% nitric acid (HNO_3) can be used to rinse and strip the zinc when necessary. At last, the device was put in the electroless nickel plating bath for a bridge-free deposit of nickel [3]. After the metallization, the Kapton tape was gently removed, and the plated bare die was thoroughly cleaned using isopropyl alcohol (IPA) and dried in oven to remove any organic residues. Fig. 3.4 shows the bare dies before and after the electroless Ni plating.

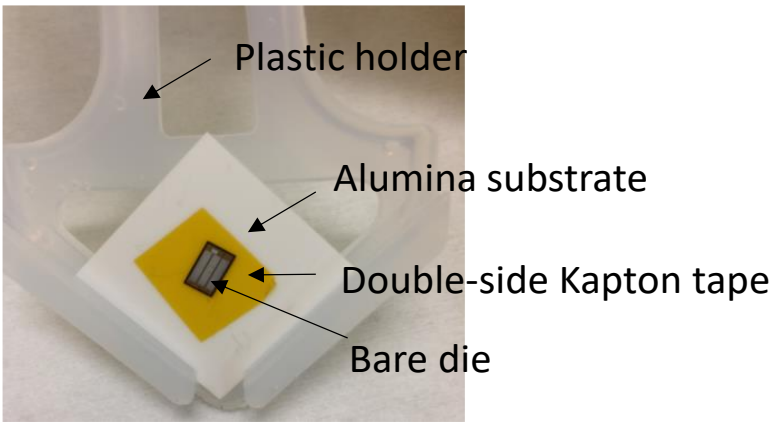


Fig. 3. 2 MOSFET bare die prepared for electroless nickel plating.

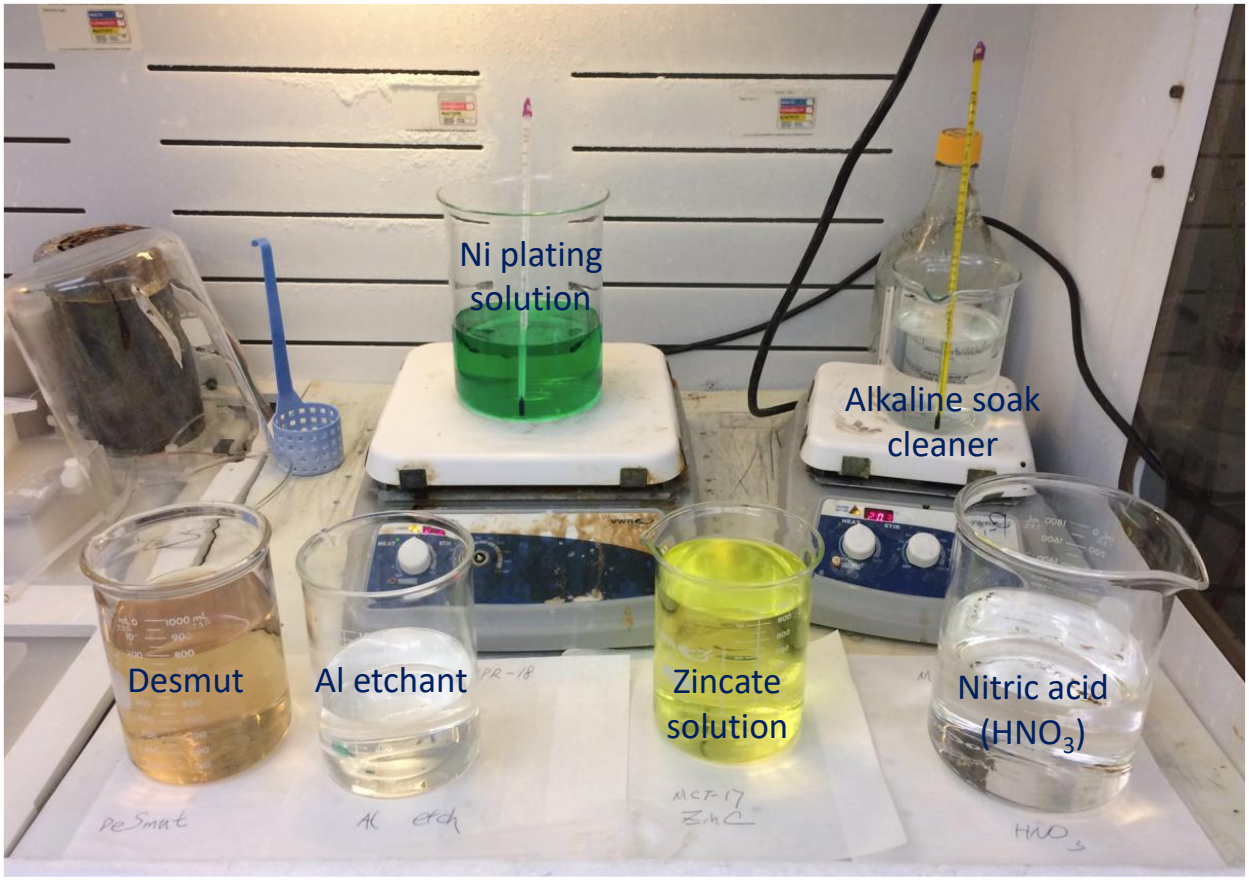


Fig. 3. 3 Solutions for electroless nickel plating.

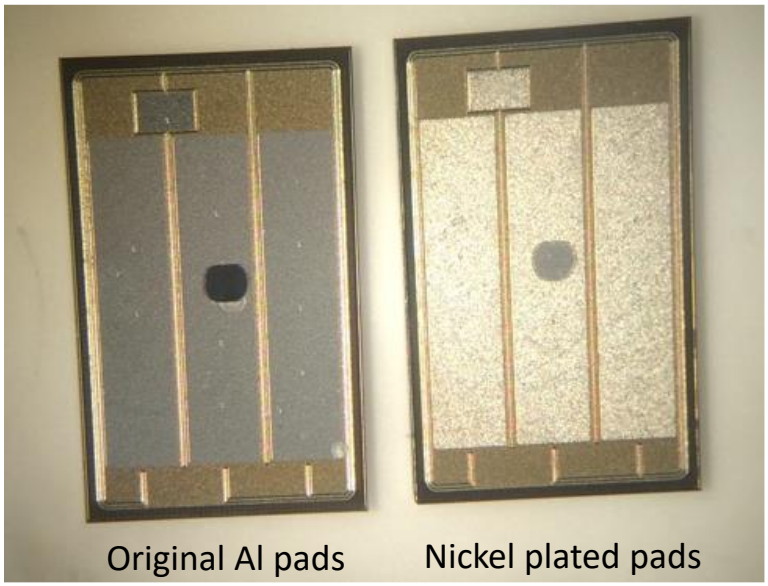


Fig. 3. 4 MOSFET bare dies before and after electroless nickel plating.

After Ni plating, the bare die was covered with a dry film solder mask, as shown in Fig. 3.5. The solder mask was UV-exposed and developed following the vendor's instruction to form pattern for copper ball array and good adhesion on the bare dies, as shown in Fig. 3.6.

Fig. 3. 5 MOSFET bare dies covered with dry film solder mask.

Fig. 3. 6 MOSFET bare dies with patterned solder mask attached on.

Copper ball attachment was the next step, solder paste was first stenciled printed into the circular open area on gate and source pads, and Cu balls with diameter of 0.508 mm were placed on to the wet solder paste by hand for gate and source connections. The assembly was then reflowed in a Sikama reflow oven to bond the copper balls securely to the pads of device. Fig. 3.7 shows the bare dies with copper balls attached on them, which are ready for flip-chip bonding.

Fig. 3. 7 MOSFET bare dies with copper balls attached on.

3.1.2 LTCC Interposer Fabrication

The LTCC interposer is a multilayer structure which allows the integration of electrical and thermal routes. The fabrication of LTCC interposer starts with DuPont™ 9K7 green tape being preconditioned in oven at 80 ℃ for 10 minutes. After preconditioning, a punch machine was used to create 20-mil-diameter through vias and cavities based on the design mentioned earlier in Chapter 4. The next step is to fill the through vias manually using a soft squeegee with a conductive co-fired silver (Ag) via fill composition, the DuPont LL601, which is compatible with the 9k7 LTCC tape. To facilitate flip-chip bonding, a co-fired solderable silver/palladium (Ag/Pd)

composition, the DuPont LL617, was printed on the top and bottom surfaces of the two external layers of the LTCC interposer using a screen printer. While green tapes of the internal layers with electrical paths besides through vias were screen printed with the DuPont LL612, a co-fired Ag conductor. Some of the prepared LTCC green tapes are shown in Fig 5.8, including a surface layer (L1) and an internal layer (L4).

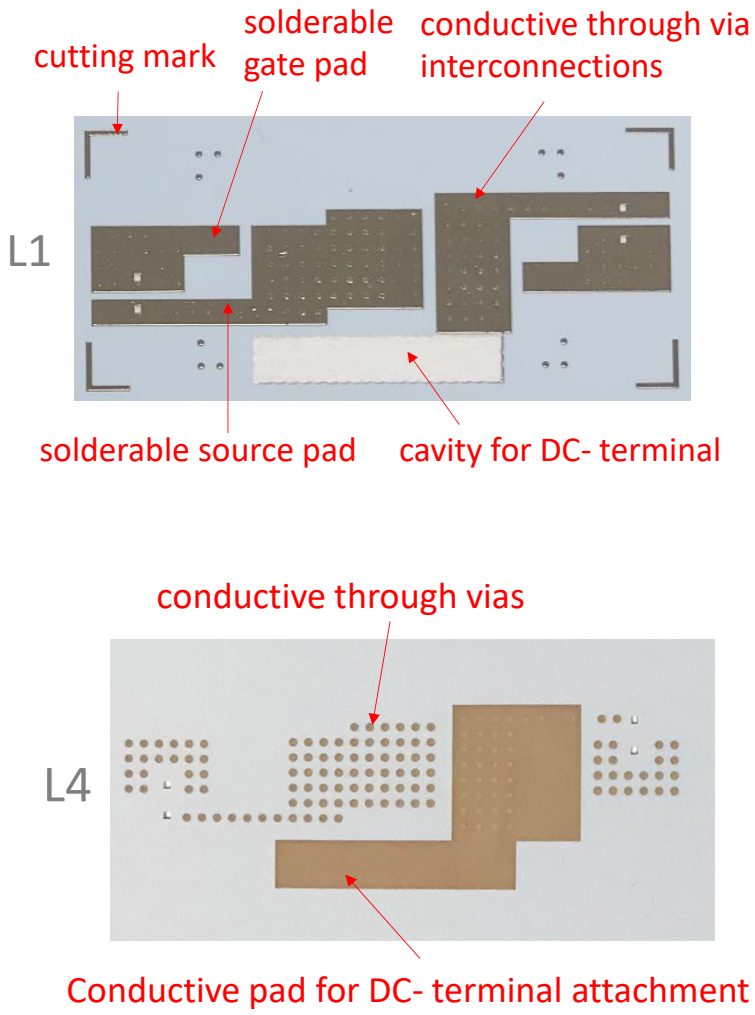
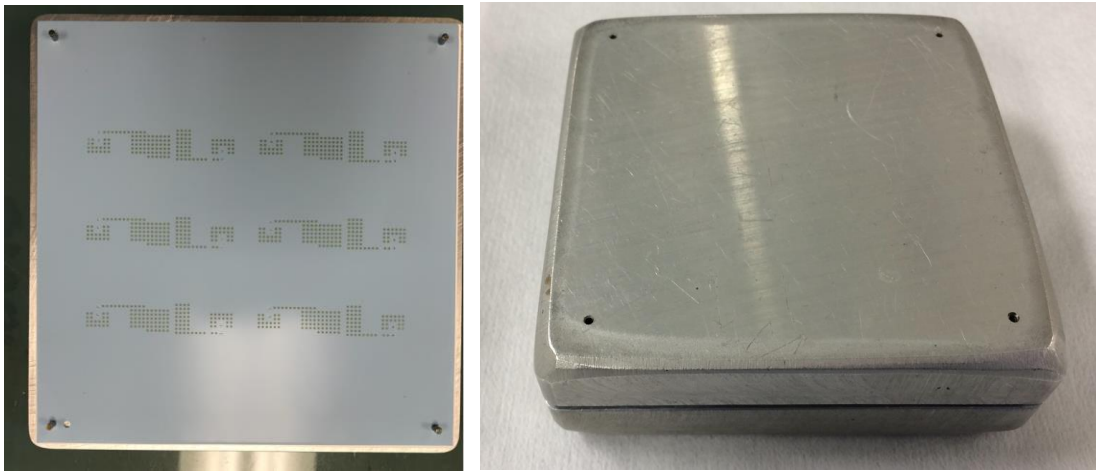


Fig. 3. 8 Prepared LTCC green tapes.

The prepared LTCC green tapes were stacked in order and sandwiched between two thick Al pads, the assembly was then wrapped with latex and vacuum sealed in three aluminum foil bags, as shown in Fig. 3.9.



(a) (b)

(c)

Fig. 3. 9 (a) Stacked LTCC green tapes on Al pad, (b) LTCC green tapes sandwiched between Al pads, and (c) vacuum sealed LTCC green tape assembly.

The isostatic lamination method was applied on the sealed assembly, which was placed in a 65 ℃ water bath for 10 minutes with a pressure of 3000 psi. The equipment used for lamination is shown in Fig. 3.10.

Fig. 3. 10 Isostatic laminator system.

The laminated tapes are then diced on a 70 ℃ hot plate along the printed cutting mark, followed by a co-fire process in a static furnace to form a solid ceramic substrate with a final thickness of 1.34 mm after shrinkage. A recommended co-fire profile from DuPont as shown in Fig. 3.11 was applied [4]. The profile lasts 26.5 hours with peak temperature of 850 ℃. The fired LTCC substrate is shown in Fig. 3.12.

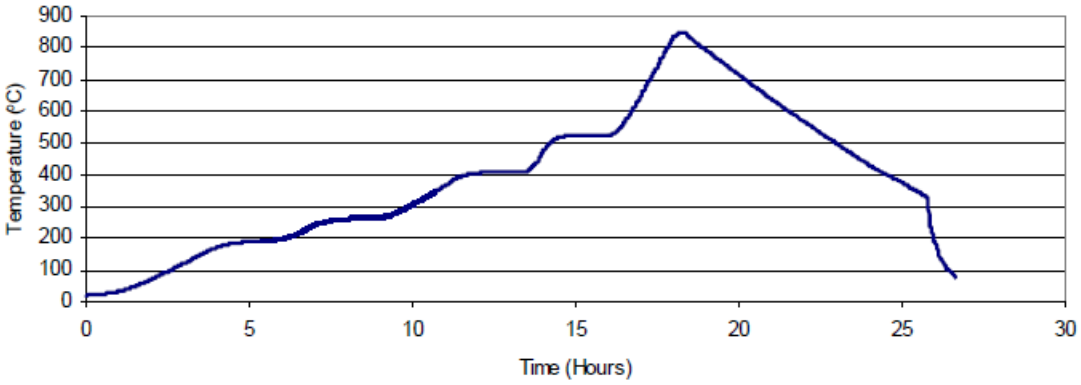


Fig. 3. 11 Co-fire profile for the 9k7 LTCC green tapes [4].

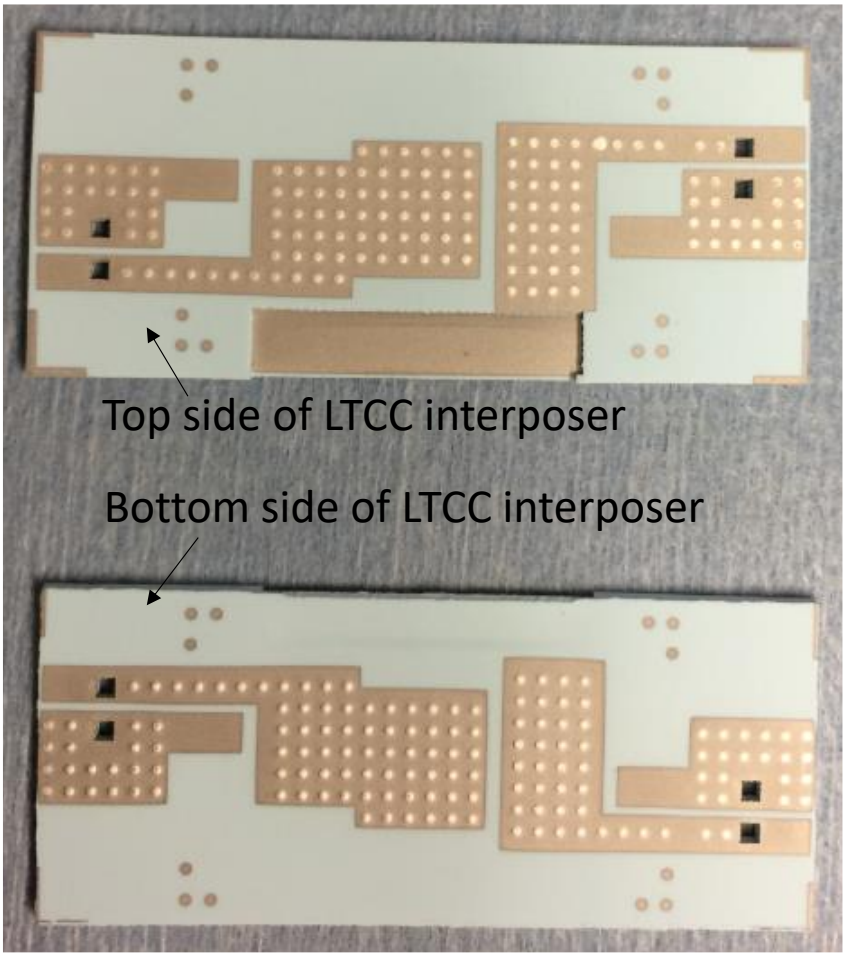


Fig. 3. 12 Fabricated LTCC substrate after co-fire.

Like the MOSFET bare dies, a solder mask was attached onto the top and bottom surfaces of LTCC interposer, followed by copper balls and DC- terminal soldering, as shown in Fig 5.13. These Cu balls have a diameter of 0.692 mm, which is larger than the Cu balls soldered on devices, the diameter of the latter is 0.508 mm. The height different between the two kinds of Cu balls is the thickness of device. As such, the bigger Cu balls create electrical connections between LTCC interposer and DBC substrates, hence the connection between the source pads of the MOSFETs at high-switching position on LTCC interposer and the drain pads of the MOSFETs at low-switching position on DBC substrate. Besides, the source pads of the MOSFETs at low-switching position is electrically connected to the DC- terminal though the filled conductive vias and the printed conductor in the internal layers of the LTCC interposer. The prepared LTCC interposer is shown in Fig. 3.14.

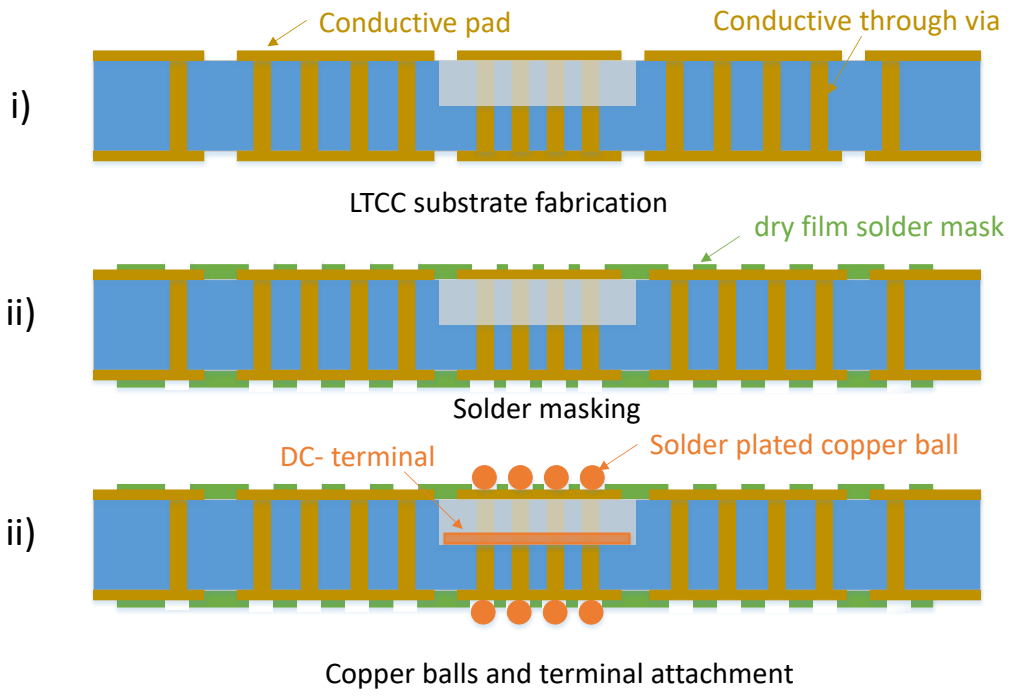


Fig. 3. 13 LTCC interposer preparation process.

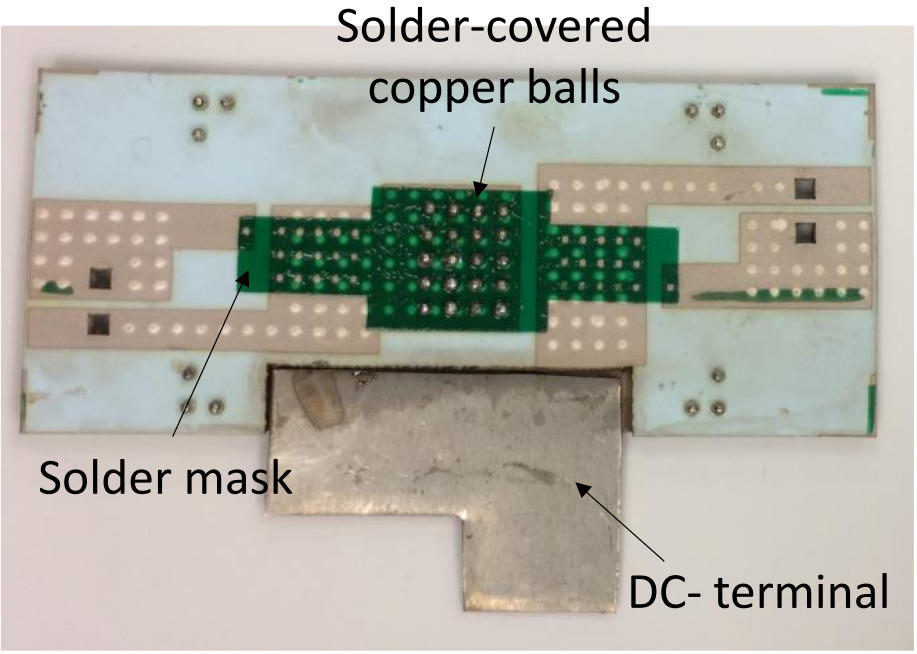


Fig. 3. 14 Prepared LTCC interposer.

3.1.3 DBC Substrate Preparation

The direct bonded copper (DBC) substrate is made of two Cu sheets bonded on alumina or aluminum nitride. DBC has the advantage of high thermal conductivity and high current capacity, making it widely used in power electronic products. In the proposed module, DBC substrate with 12-mil Cu was used. The DBC was first plated with 4 μm nickel to provide good bonding surface and prevent oxidation. Then, a layer of photoresist dry film was adhered to the DBC using a laminator. After that, a photolithography mask representing the layout of DBC design was placed on DBC, followed by an UV light exposure. The photoresist dry film on DBC substrate was then developed to create the desired pattern, and the DBC substrate was put on a transfer belt in a Chemcut machine to etch away the exposed copper by ferric chloride (FeCl3) etchant solution. After etching, the DBC substrate was diced to the designed size using a diamond dicing saw. The

fabricated DBC substrates for the proposed module are shown in Fig. 3.15. The DC+ and AC terminals are then attached onto the two DBC substrates using solder paste, as shown in Fig. 3.16.

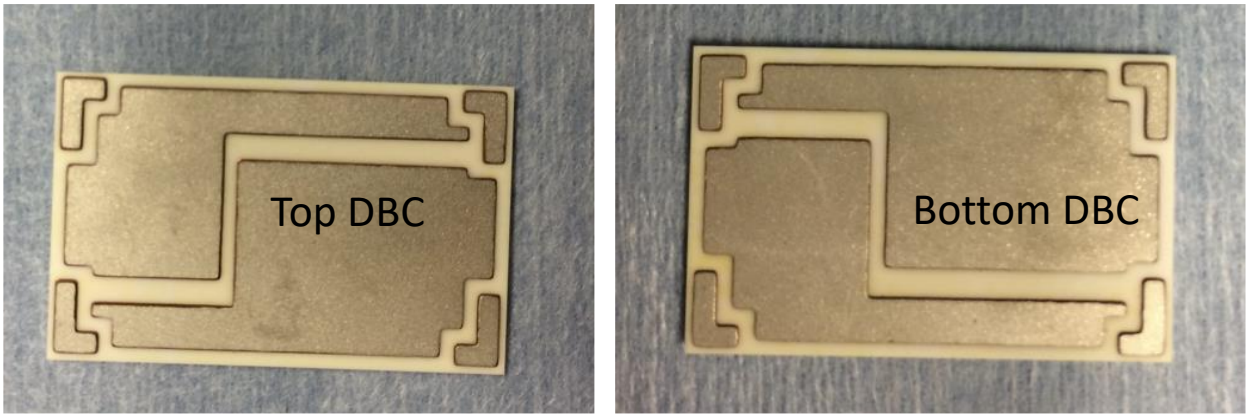


Fig. 3. 15 Fabricated DBC substrates.

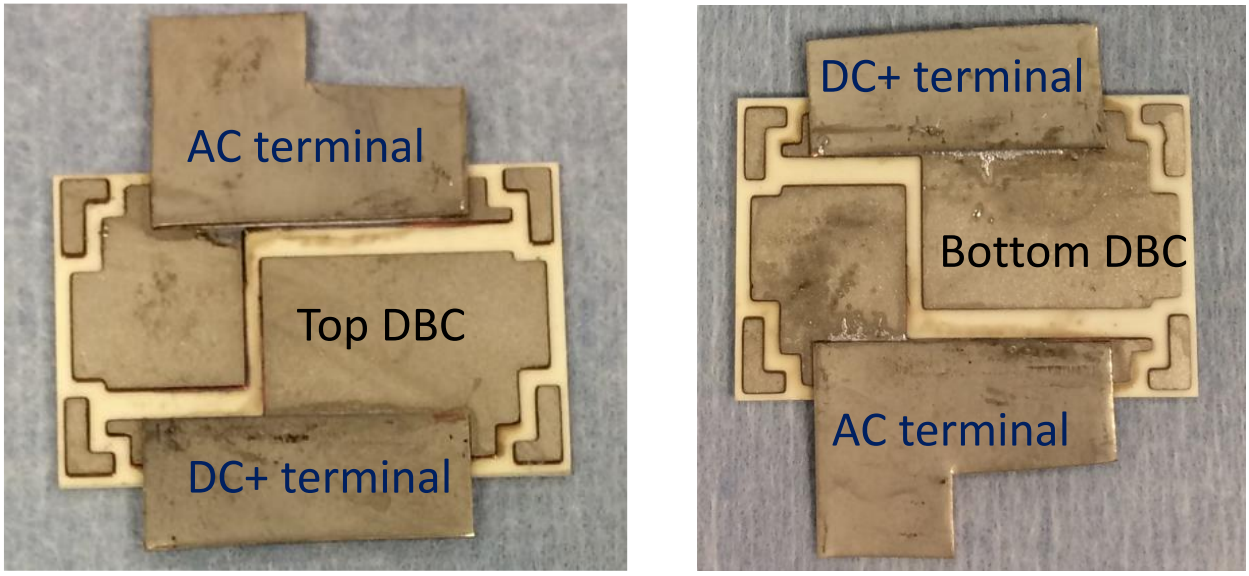


Fig. 3. 16 DBC substrates with power terminals soldered on.

3.1.4 Flip-chip Die Attachment and Module Assembly

After all the necessary components were prepared, the proposed stacked module was assembly, the process is shown in Fig. 3.17.

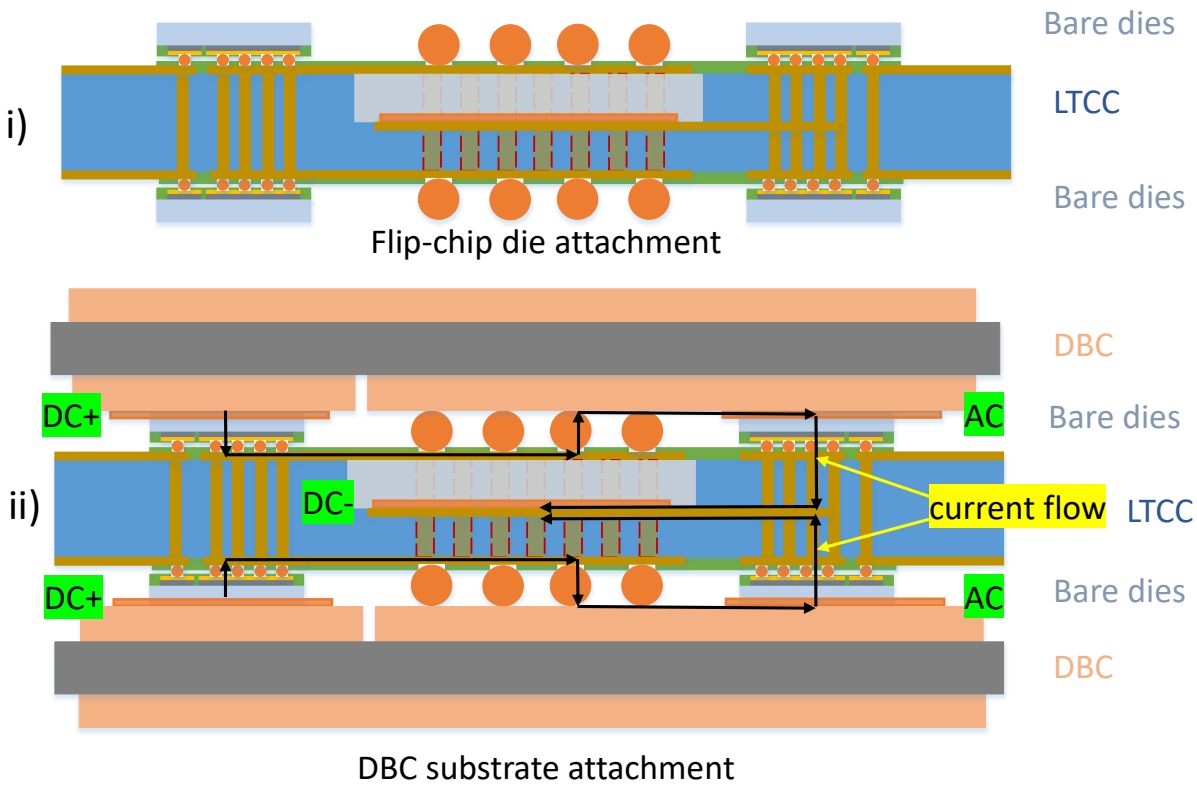


Fig. 3. 17 Module assembly process.

First step is flip-chip die attachment. The openings of the solder mask on LTCC were printed with a solder flux, the Cu balls attached bare dies were then flipped, aligned, and placed to the LTCC interposer surface using the Finetech Fineplacer flip-chip bonder, as shown in Figure. 5.18. The reflow process was followed to achieve conductive joints between Cu balls and metalized layer of LTCC interposer. A set of graphite fixture with cavities for SiC dies was used to keep the dies in position during reflow, as shown in the Fig. 3.19. The LTCC was sandwiched between two graphite fixtures within the cavity, the SiC bare dies were attached on LTCC through the opening of the fixture which also keeps them in position. The two fixtures aligned with the help of screw at four corners. The lid gave pressure for the SiC dies attachment on top of LTCC, the support at bottom prevented the SiC dies from moving. As a result, electrical connections were created

between the top gate and source electrodes of MOSFETs and the conductive traces on LTCC interposer.

The next step is to assembly the stack module. The SAC305 solder paste was printed on the backside of SiC devices. The LTCC interposer with dies attached was then sandwiched between the top and bottom DBCs with the help of a graphite alignment fixture shown in Fig. 3.20. A reflow process was followed in reflow oven, and the connection between the back drain electrodes of MOSFETs and the copper traces on DBC substrates were achieved. A fabricated double-sided stack wire-bondless power module is shown in Fig. 3.21, the Kelvin gate and source pins can be soldered on the LTCC interposer at last.

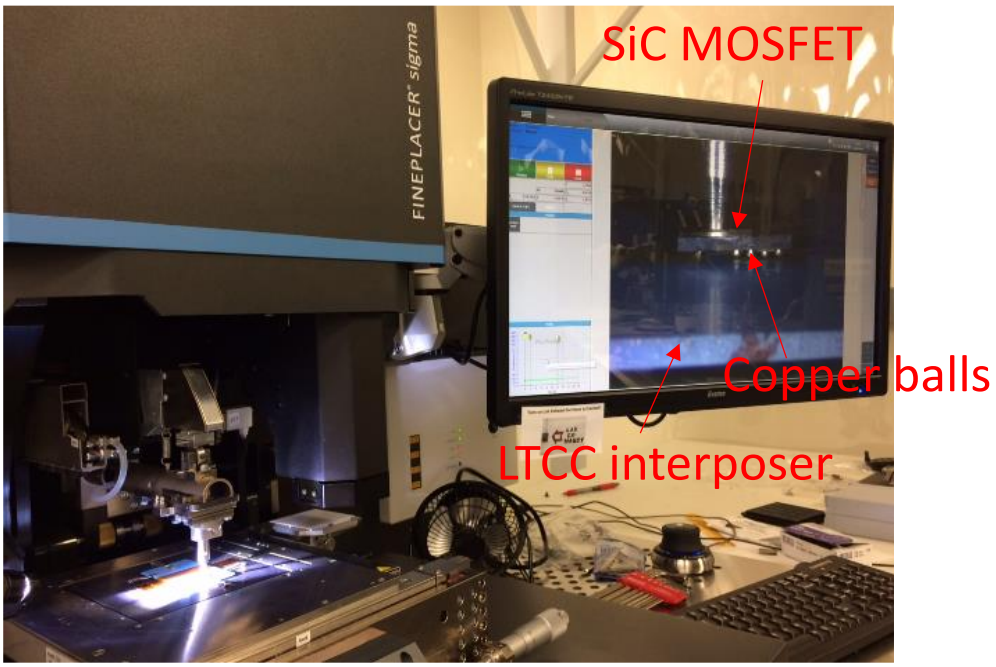


Fig. 3. 18 Flip-chip bonding process using the Finetech flip-chip bonder.

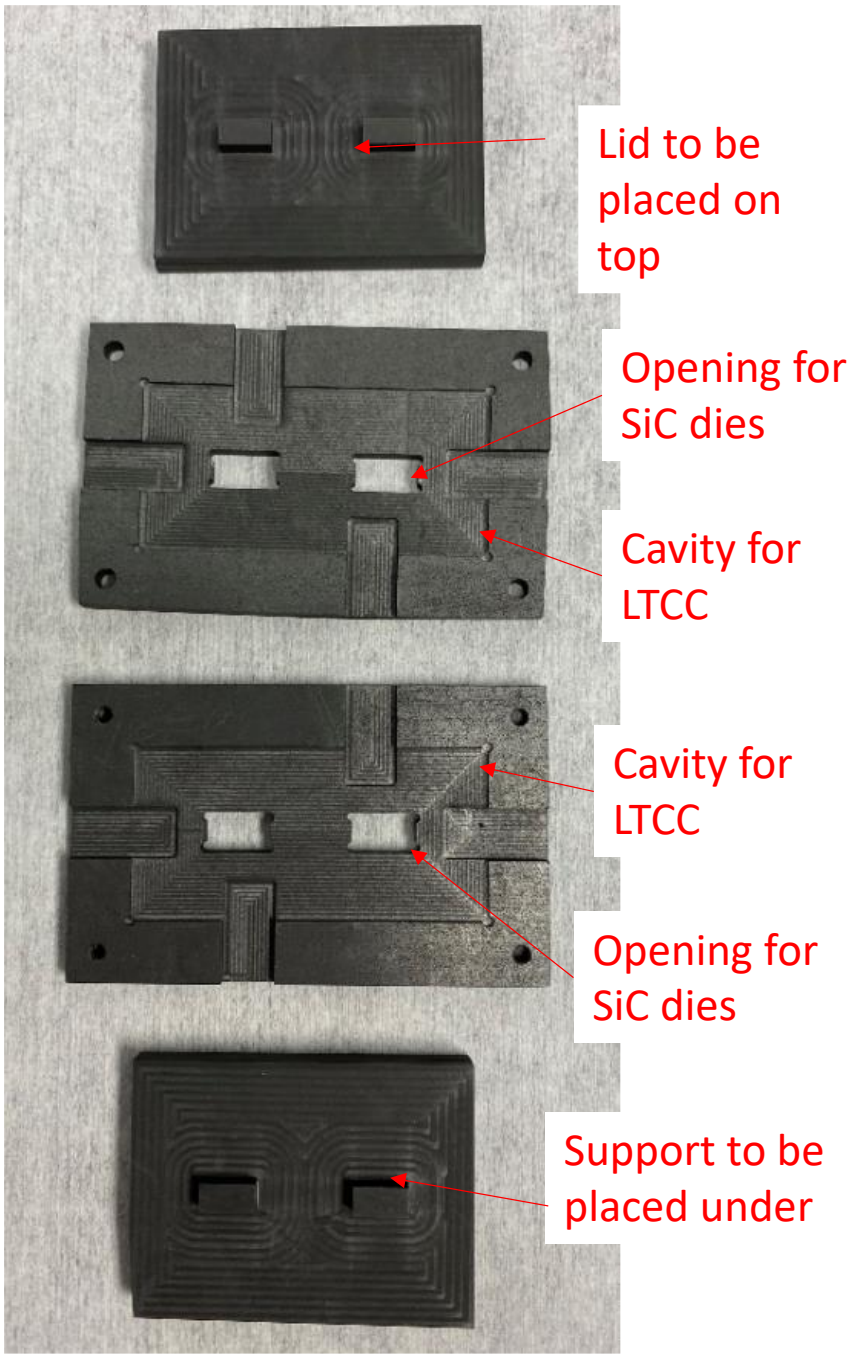


Fig. 3. 19 Graphite fixture set for flip-chip bonding in reflow oven.

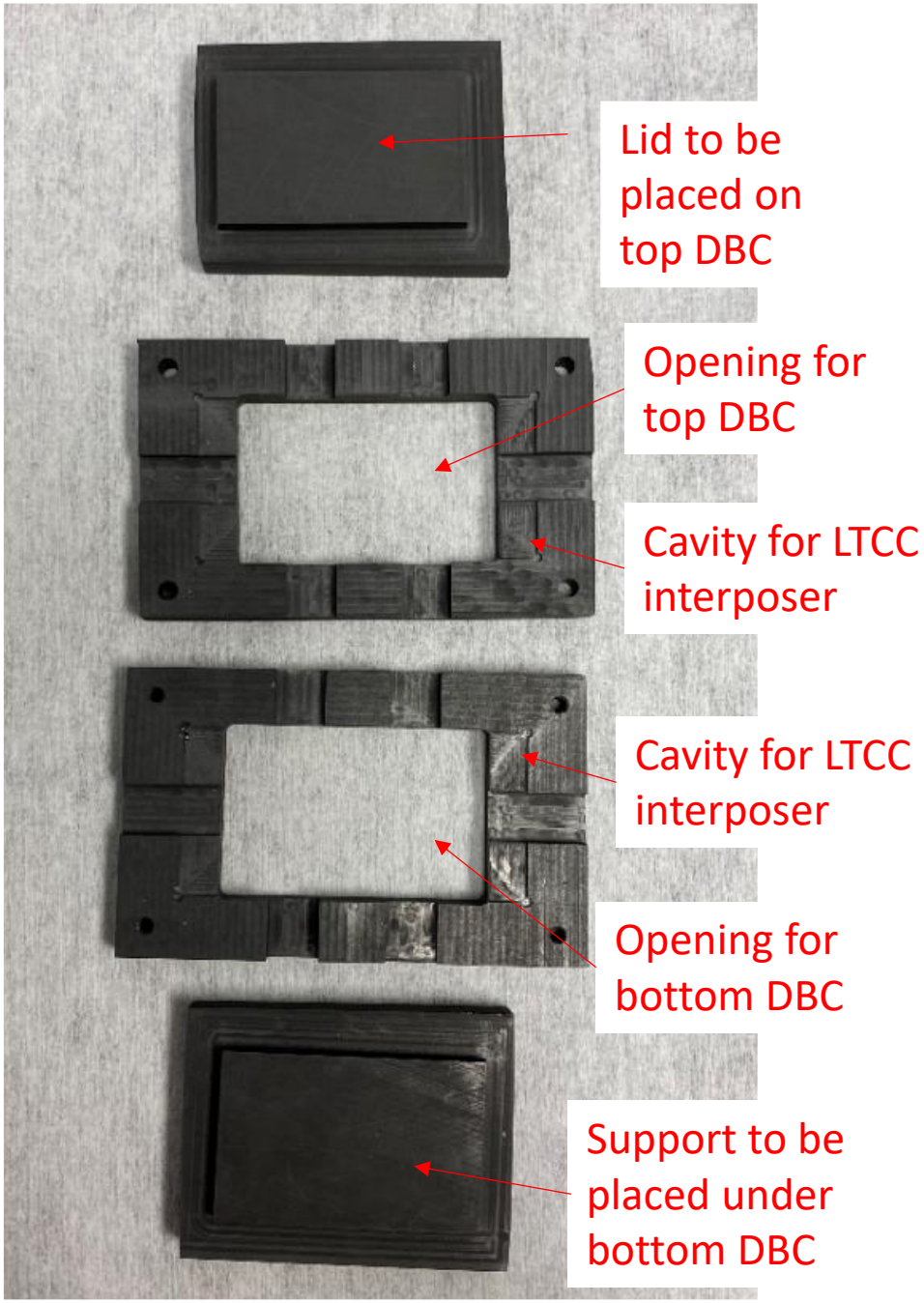


Fig. 3. 20 Graphite fixture set for module assembly in reflow oven.

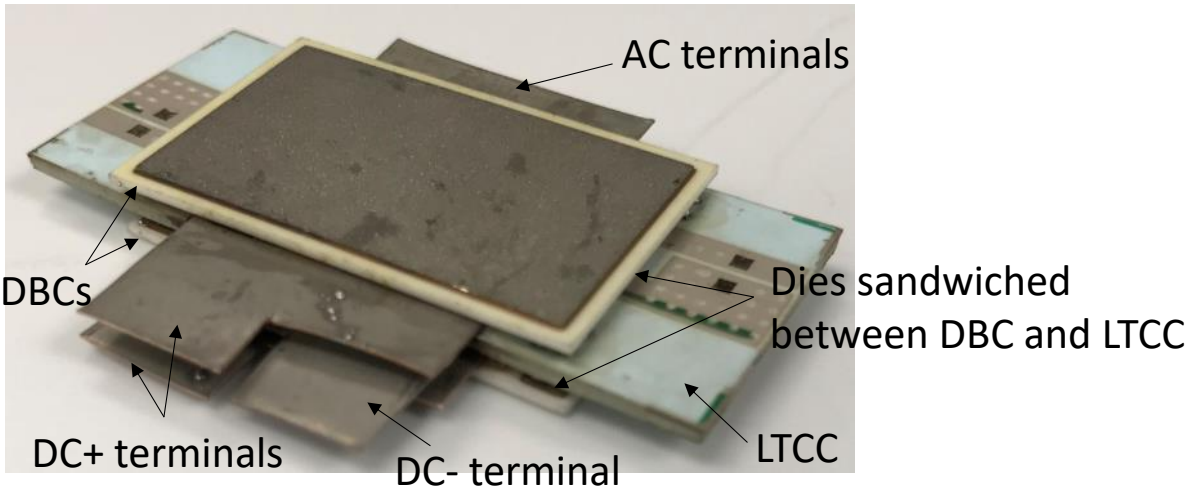


Fig. 3. 21 A fabricated double-sided stack wire-bondless module prototype.

3.2 Experimental Characterization of the Fabricated Power Module

After the fabrication of the proposed power module, experimental tests were conducted on the fabricated prototype to evaluate its performance, including electrical and reliability tests.

3.2.1 Static Characteristics

A source measure unit (SMU) was used to measure the drain-source leakage current of both switching positions of the half-bridge module in order to verify the electrical connection of the fabricated module and investigate the package influence on the leakage current. The drain-source leakage current is given by a p-n junction diode in reverse direction, the ideal leakage current is independent from the applied voltage, however, in practice, an additional current is added to the ideal saturation current, resulting in increased leakage current when higher reverse voltage is applied. Reasons for this additional current are: (1) surface leakage and inversion layers, (2) body defects, and (3) generation and recombination [5]. The drain-source leakage currents of both switching positions as a function of drain-source voltage are shown in Fig. 3.22, the leakage currents have a specified maximum voltage of 700 V with a safety margin up to approximately

825 V when avalanche occurs. That's why the leakage current spikes at 825 V. However, the drain-source leakage currents are 4.1 μA and 14.2 μA at 900 V, respectively, for the high-side and low-side switching position, which are still less than the maximum value (100 μA) as provided in the device datasheet.

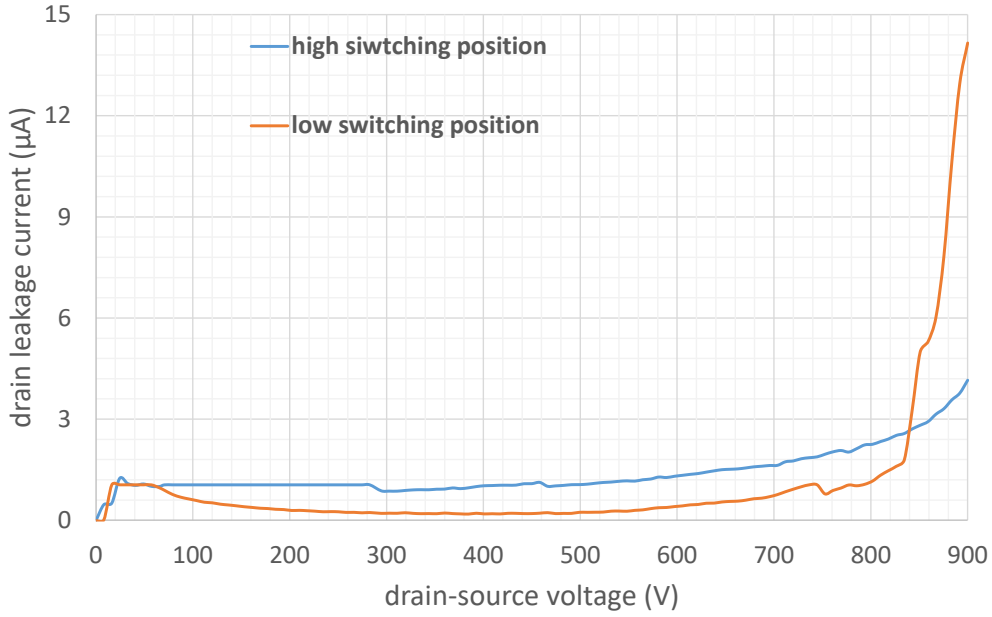


Fig. 3. 22 Drain-source leakage current measurement results.

3.2.2 Switching Test

Double-pulse test is performed to characterize the switching performance of the fabricated wire-bondless power module. A double-pulse test schematic for low-side MOSFETs of the half-bridge module is shown in Fig. 3.23. In the double-pulse test, the 1st pulse turns on the MOSFETs at low-side switching position and establishes current in the load inductor. Turn-off of the 1st pulse creates current in the body diode of the MOSFETs at high-side switching position, the load current almost keeps constant during turn-off period because of the high load inductance and short turn-off interval. The 2nd turn-on pulse leads to reverse recovery of the body diode hence current overshoot

in the low-side MOSFETs under test. The 2nd turn-off results in drain-source voltage overshoot, and the voltage spike is related to the parasitic inductance of the power loop.

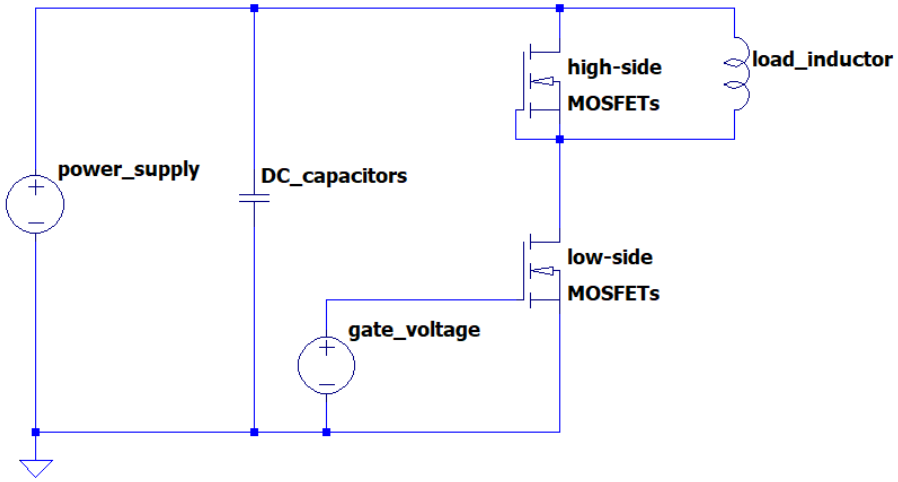


Fig. 3. 23 A double-pulse test schematic.

The test set-up is shown in Fig. 3.24. A power supply provided 15V DC voltage to the gate driver board, and a function generator provided the double pulse signal to the gate of the MOSFETs at low-switching position through the gate driver. DC capacitors on the test fixture were used to decouple the DC bus connection stray inductance. The high voltage source supplied DC bus voltage for the power module, a current transformer with a toroid magnetic core was used to monitor the current in power loop, the switching waveforms of drain-source voltage (V_{ds}) and drain current (I_d) of the low-side MOSFETs were captured using an oscilloscope, which are shown in Fig. 3.25. As can be seen from the switching waveforms, the fall and rise times of the V_{ds} are 69 ns and 78 ns, respectively. The drain-source voltage overshoot at turn-off due to power loop parasitic inductance is about 5%. The small oscillation of these waveforms during switching transients indicates the low-inductance behavior of this double-sided stack module.

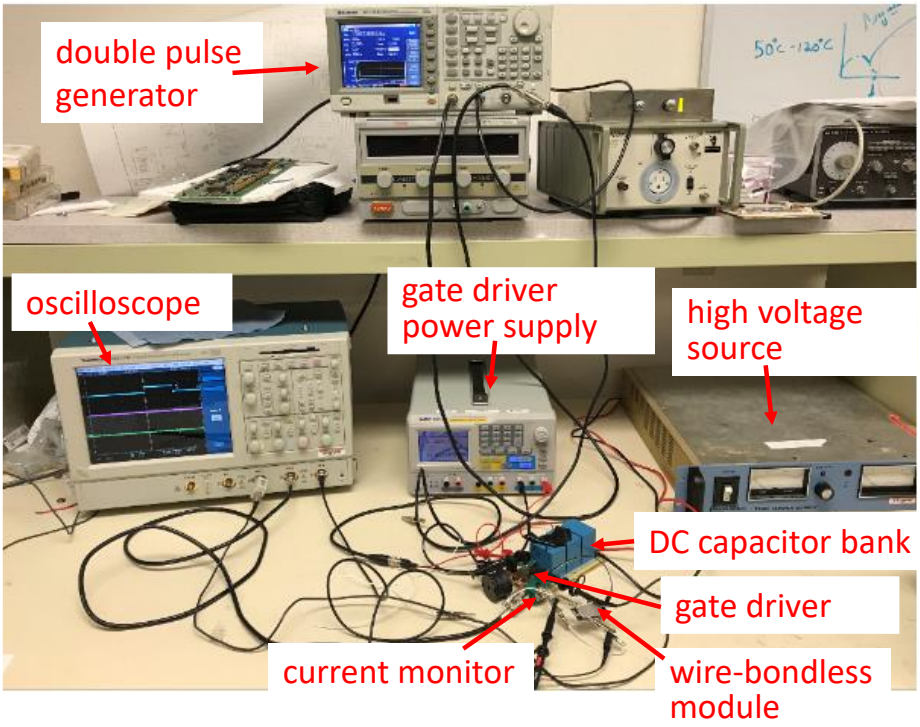
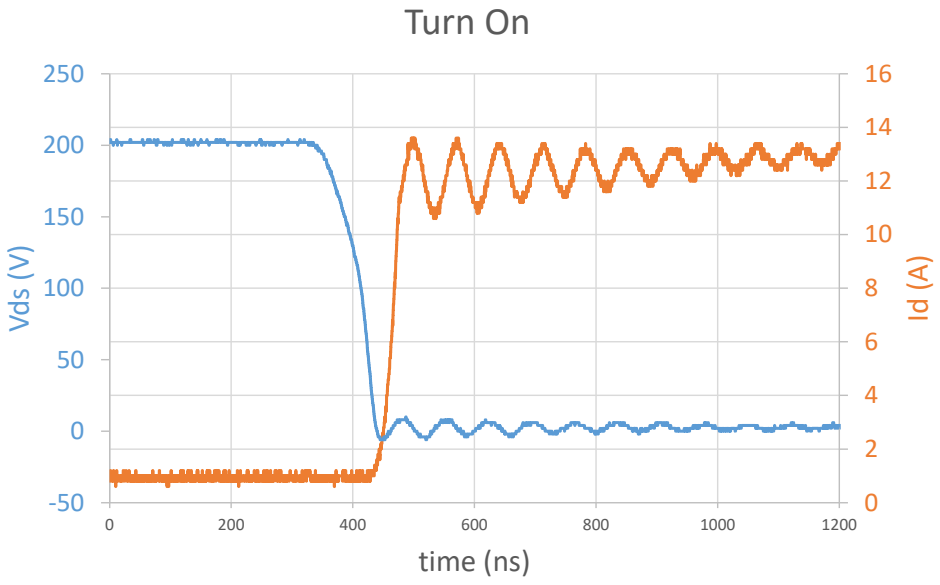
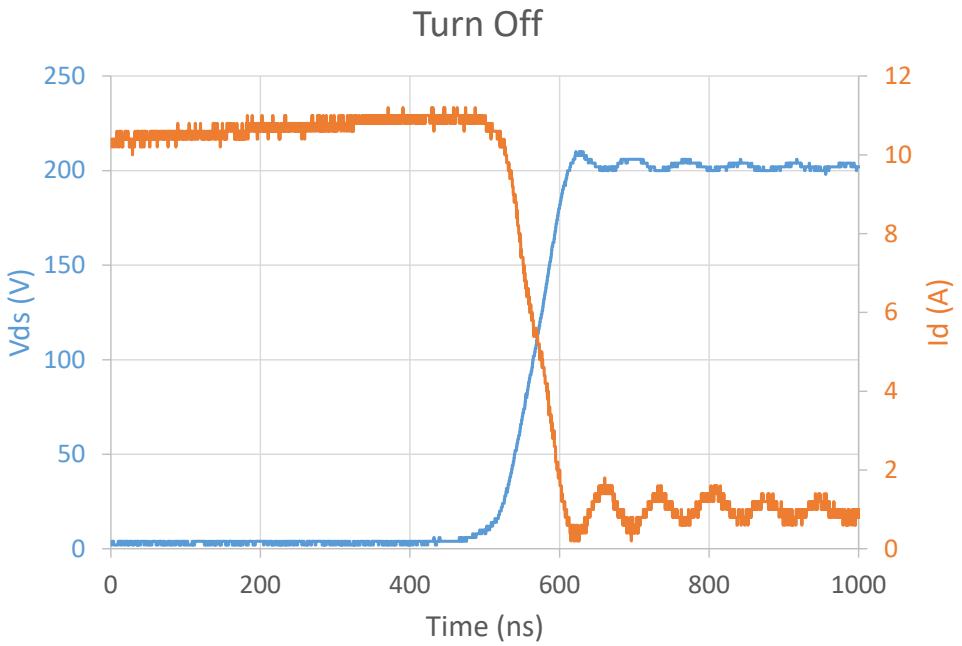


Fig. 3. 24 Double-pulse test setup.



(a)

Fig. 3. 25 Switching waveforms of V_{ds} and I_d at (a) turn on, and (b) turn off.



(b)

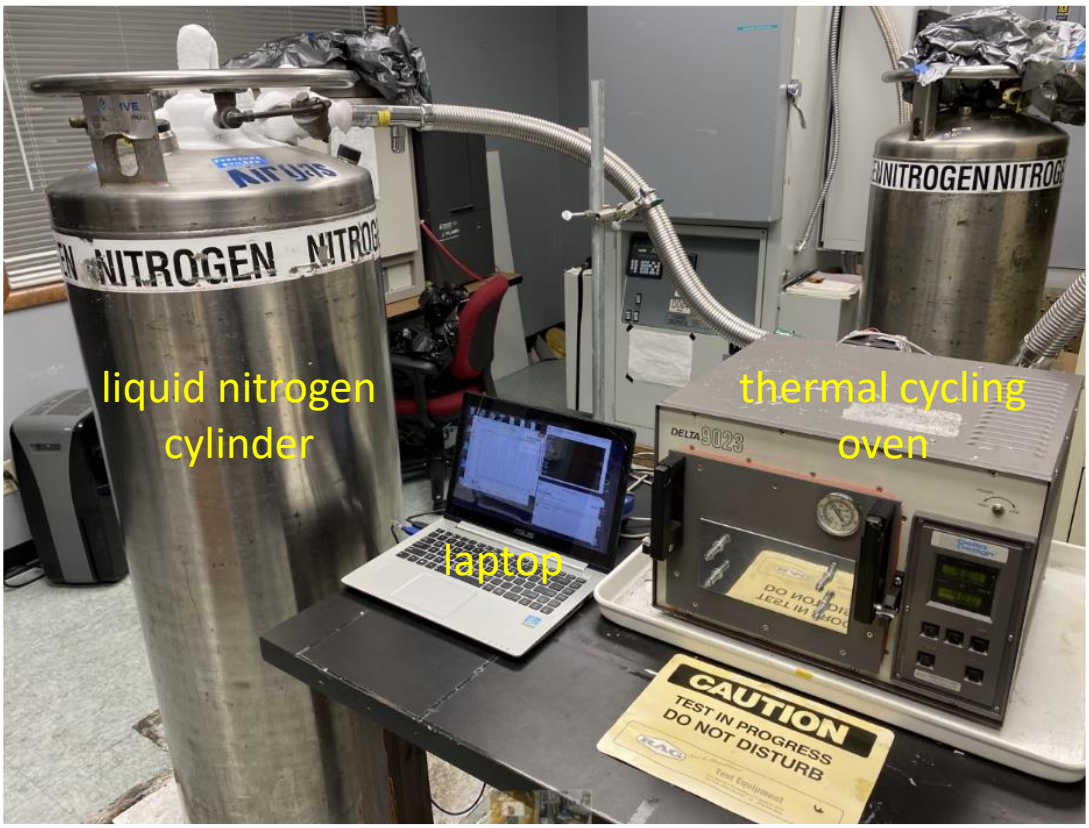
Fig. 3. 25 Cont. Switching waveforms of V_{ds} and I_d at (a) turn on, and (b) turn off.

3.2.3 Thermal Cycling Test

Considering that the CTE difference of materials in the fabricated stack wire-bondless power module can result in large thermal stress on the interface layers when temperature in the module changes, a thermal cycling test was performed to validate the reliability of the fabricated module.

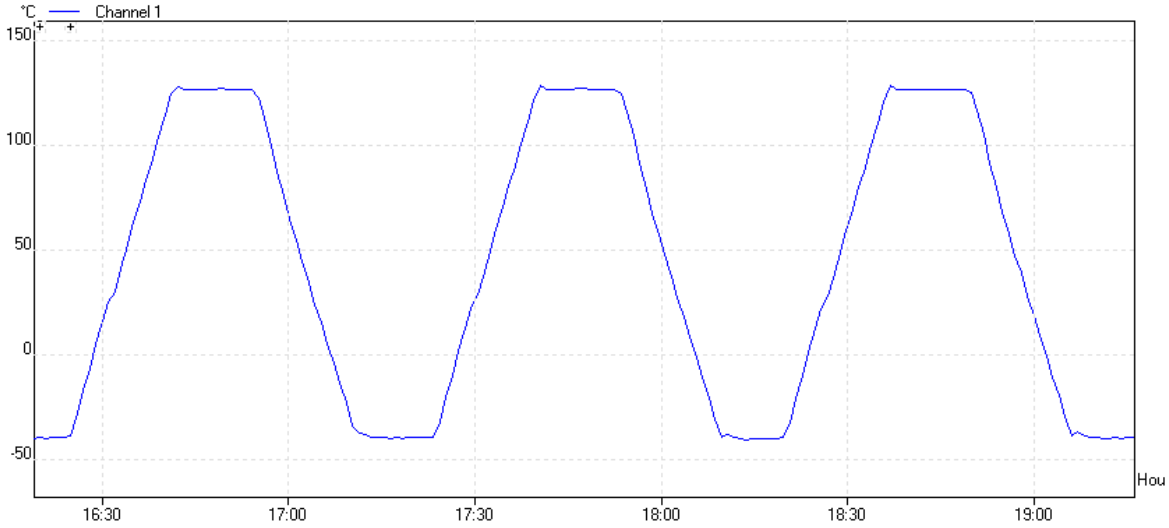
The test conditions is chosen to be -40℃ to 125℃ based on JEDEC Standard of temperature cycling, which is used to determine the reliability of components and interconnects to withstand mechanical stresses induced by alternating high and low temperature extremes [6]. The thermal cycling test setup is shown in Fig. 3.26 (a), the test temperature profile was loaded through a software in the laptop connected to the thermal cycling oven, and liquid nitrogen was used for rapid cooling. The power module under test was placed inside the oven, and a thermocouple was

attached on the module using Kapton tape to monitor the actual temperature of power module, the measured actual temperature by thermocouple is shown in Fig. 3.26 (b). 50 cycles were carried out, after the thermal cycling test, the power module was taken out of the chamber to check any shorting or delamination. Leakage current was measured and compared with the results before thermal cycling test, as shown in Fig. 3.27. The comparison indicate that the power module passed the 50-cycle thermal cycling test without degradation, besides, no crack or delamination was observed.



(a)

Fig. 3. 26 (a) Thermal cycling test setup, (b) measured thermal cycling temperature profile.



(b)

Fig. 3. 26 Cont. (a) Thermal cycling test setup, (b) measured thermal cycling temperature profile.

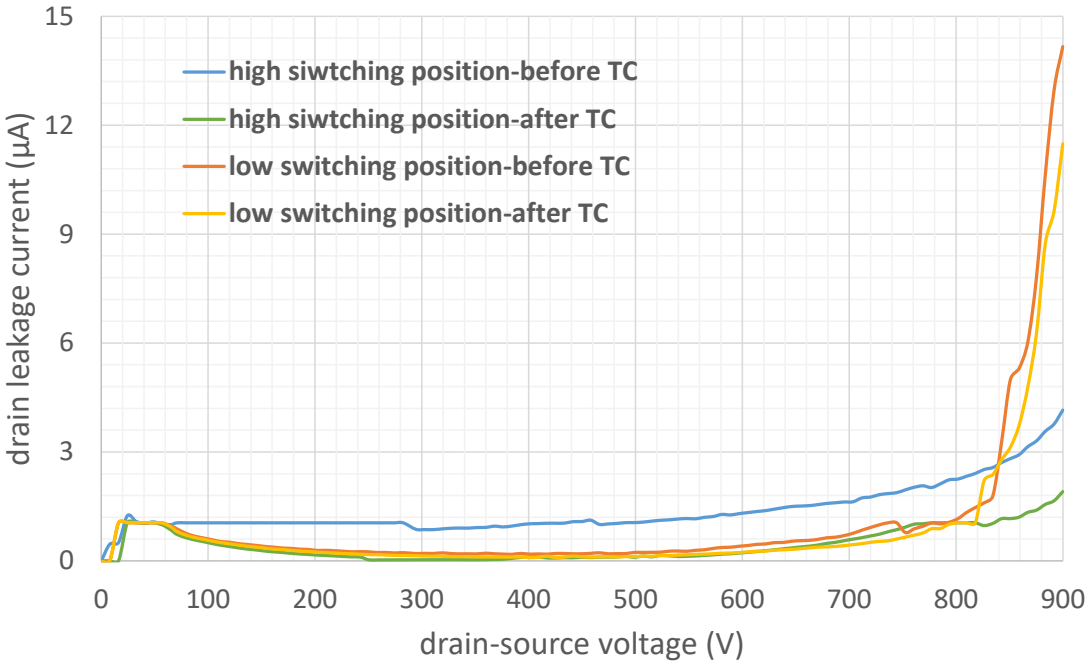


Fig. 3. 27 Leakage current measurement results before and after thermal cycling (TC) test.

3.3 Chapter Summary

This chapter introduces the developed processes to fabricate the proposed double-sided stack wire-bondless module, as well as the electrical and reliability tests to evaluate the performance of fabricated module. The major fabrication steps such as device re-metallization, LTCC interposer and DBC substrates preparation, and flip-chip die attachment are described in detail. Several modules were successfully fabricated following the processes. Next, experimental evaluation of the fabricated module was discussed. The switching test shows a significant reduction in drain source voltage overshoot and ringing, and the reliability of the module was verified by thermal cycling test.

3.4 References

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Chapter 4 Impact of Nano-diamond Composites on the Thermal Performance of LTCC Interposer

Chapter 2 consists of a published IEEE paper with the following citation:

S. Huang, Z. Xu, F. Yu and S. S. Ang, "Impact of nano-diamond composites on low-temperature co-fired ceramic interposer for wide bandgap power electronic module packages," 2016 *IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Fayetteville, AR, 2016, pp. 314-318, doi: 10.1109/WiPDA.2016.7799959.

Impact of Nano-diamond Composites on Low-Temperature Co-fired Ceramic Interposer for Wide Bandgap Power Electronic Module Packages

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Abstract— A 2.5D package with interposer is proposed for wide bandgap (WBG) power modules. Low temperature co-fired ceramic (LTCC) is used for the interposer because its coefficient of thermal expansion (CTE) is closely matched to those of WBG devices as well as its flexibility to have complex structures and through-hole vias built on it. Furthermore, its thermal performance can be enhanced through the addition of through-hole thermal vias. Nano-composite of nano-diamond and silver paste was used as via filled materials in these LTCC interposers. It was found that such interposers with bigger trench vias yielded smaller thermal impedance values while those with circular vias yielded larger thermal impedance values. Scanning acoustic

microscopy (SAM) revealed large number of voids in samples with circular vias. As such, besides via filled materials, interposer pattern design, and via dimensions are also crucial in these interposers. Thermal simulations were performed for these interposers and different thermal materials were used and compared.

Keywords—Nano-diamond; LTCC interposer; Wide bandgap power module; Thermal analysis.

4.1 Introduction

Silicon carbide (SiC) and gallium nitride (GaN) power devices are increasingly desired for high power density electronic modules for their performance advantages over those of their silicon counterparts. New packaging architecture, such as the 2.5-dimensional (2.5D) package with interposer as shown in Fig. 1, is proposed for a high density compact wide bandgap (WBG) power module. Multiple WBG chips are soldered on direct bonded copper (DBC) side by side with a low temperature co-fired ceramic (LTCC) interposer mounted on top of chips. The main advantages of such stacked package include enhanced interconnect density and reduced interconnect length, addressing miniaturization, modularity, performance and cost [1-2]. Work has already been performed to show that the stacked wire bondless power modules demonstrate significantly reduced parasitic inductances and minimized electromagnetic interference effects compared to those of coplanar modules [3]. However, for higher power density 2.5D and 3D modules, as the number of chips increases, and because of their smaller footprints, heat density is significantly increased in the modules, which makes it a key issue to remove heat more efficiently to avoid hot spots within the modules that can greatly affect both thermo-mechanical reliability and electrical performance of modules. Hence, for high density power electronic modules, it is essential to take both the electrical

and thermal considerations into account during the design phase, otherwise, the WBG device lifetime can be decreased drastically because of large thermal stresses and resultant mechanical stresses [4].

Silicon and glass interposer technology is being developed because of many advantages including high I/O density, and there are various works reporting their thermal characteristics with through-package vias (TPVs) [5]. However, silicon interposer is limited to wafer size and high electrical loss, while glass interposer has a much lower thermal conductivity of 0.8-1.0 W/(m*K). Besides, only vertical TPVs can be built within the silicon and glass interposers to enhance their performance.

In this paper, LTCC is proposed as an interposer in high-density power modules based on both SiC and GaN. First, the LTCC green tape has a CTE that closely matches that of SiC and GaN. The CTE values of DuPont 9k7 and 951 LTCC green tapes are 4.4 ppm/°C and 5.8 ppm/°C, separately, and the CTEs of SiC and GaN are 4.0 ppm/°C and 5.6 ppm/°C. CTE mismatch among different layers will cause warpage or delamination, leading to reliability issues [4]. Second, the LTCC substrate can accommodate complex interconnect and cavity structures both externally and embedded within the substrate [6], which allows coordinated integration of both electrical and thermal power routes in power modules, as shown in Fig. 4.1. Specifically, horizontal surface channels and through-hole vias can be incorporated in these LTCC interposers, where high thermal conductivity materials can be applied to improve heat removal. As such, various LTCC interposer designs and applicable thermal management materials are investigated. In addition to the specific LTCC via pastes, nano diamond (ND) particles are used to form nano-composites due to their high thermal conductivity, chemical stability, and large external surface to maximize interactions with

the matrix [7]. The effect of the nano-diamond composites in different LTCC interposer structures is studied.

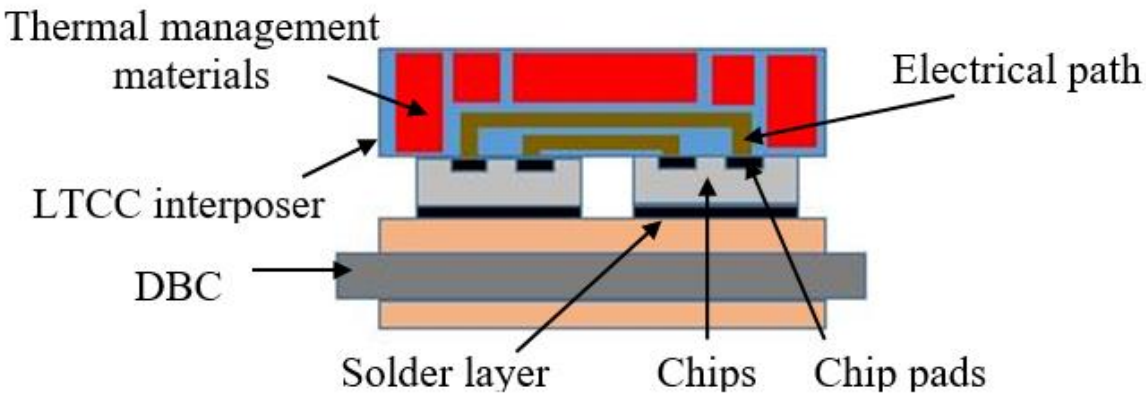


Fig. 4. 1 2.5D package with interposer.

4.2 Experimental

4.2.1 Materials

DuPont 9k7 LTCC green tape was chosen to build the interposer. A LL601 silver (Ag) paste was chosen as the co-fired via-filled matrix material. The via paste is specially formulated to fully fill the via hole and match the shrinkage of the tape [8]. Nano-diamond particles having 4~5 nm primary particle size was chosen as the nano fillers.

4.2.2 Nano-dimond Composites Preparations

Nano-diamond particles were dried overnight in vacuum at 60°C at first. Then, the nanoparticles were added into LL601 silver paste thinner 9450 at a ratio of 0.026g ND: 2ml thinner. The composites were mixed by a vortex mixer at 3000 RPM for 30 minutes to form nano-diamond dispersion. Next, the mixture was put into ultrasonic bath for 20 minutes to maximize dispersion of

nanoparticles. The final composites were prepared by mixing the nano-diamond dispersion with the LL601 silver paste.

4.2.3 LTCC Interposer Substrate Fabrication

An array of 12 and 20 mil circle and trench through-vias were designed as shown in Figs. 4.2 and 4.3. Individual LTCC green tape layers were prepared by punching vias on them according to designs. Then, either LL601 silver paste or its nano-diamond composites were filled into the through vias by printing. Repeat this process for six individual green sheets, collate and stack them using a precision tooling fixture and laminate at 3000 psi. The laminate went through co-fire following specific temperature profile at 850°C to form solid ceramic. Subsequently, DuPont 6277 silver/palladium (Ag/Pd) paste was printed on both surfaces of the LTCC structure for post fire operation to achieve a suitable interface for the attachment of a heat source during following test. The fabricated LTCC test specimens are shown in Fig. 4.4.

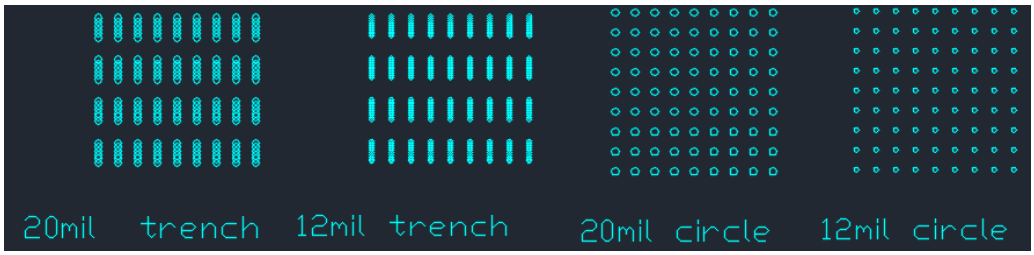


Fig. 4. 2 Top view of LTCC thermal vias designs.

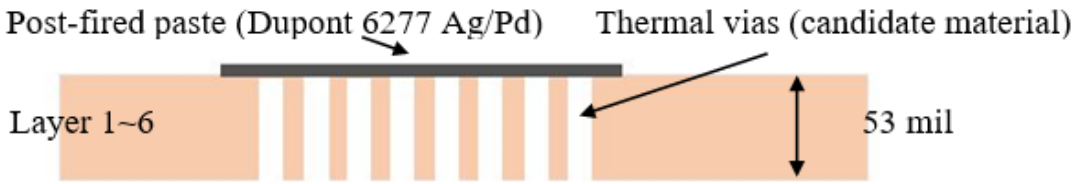


Fig. 4. 3 Cross-section view of LTCC thermal vias designs.

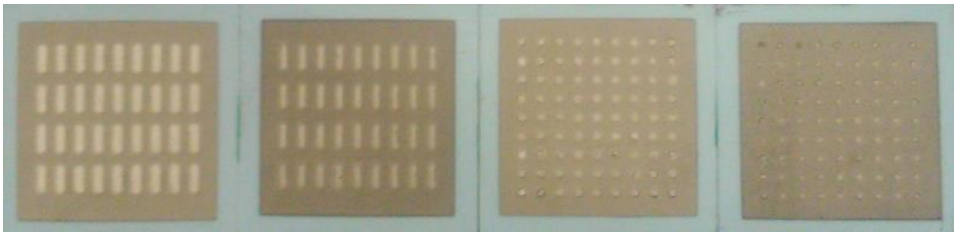


Fig. 4. 4 Fabricated LTCC test specimens.

4.2.4 Thermal Impedance Measurement

The thermal impedance measurement for LTCC interposer samples is based on the ASTM D5470-06 standard steady-state test method [9]. This standard method is established on an ideal heat conduction between two parallel surfaces separated by the studied specimen of uniform thickness. One of the two parallel surface is in contact with a heater which produce uniform heat flow propagation to surfaces, while the other one contacts a cooler to remove the heat flow. Therefore, the temperature difference creates a thermal gradient across the test specimen. Assuming no lateral heat spread, the heat flow goes through the test specimen and interfaces uniformly without heat loss.

The thermal impedance θ is defined by (4.1)

$$\theta = A * \Delta T / Q \qquad (4.1)$$

where A is the area of contact interface of test specimen perpendicular to the heat flow, Q is the average heat flow through specimen, and ΔT is the temperature difference across the specimen. The thermal impedance represents both the studied specimen and its interaction with surfaces. It is the sum of the specimen resistance and contact resistance [10].

Figs. 4.5 and 4.6 show the schematic and the experimental setup used to measure the thermal impedance. Different thermal material filled LTCC specimens were sandwiched between the surfaces of two copper blocks, each copper block has 15.85 x 15.85mm surfaces, which are the same as the contact surfaces of LTCC test specimens, and a height of 35 mm. A heater was placed on the top of one copper block, and the heater temperature was controlled at 80°C by a temperature controller. The bottom of the other copper block was cooled by a water chiller whose temperature was kept at 10 °C**.**

Four T-type thermocouples were inserted into four holes in copper blocks to record the temperatures (T_1, T_2, T_3 and T_4 in Fig. 4.5), two in each block. The distance d_1 or d_4 between two thermocouples in the same block is 25mm, and the distance d_2 or d_3 between thermocouple and the copper block surface is 5mm. Temperatures were recorded when the temperature variation was within ±0.5°C in a 5-minute period. The system was thermally insulated by wrapping with glass fiber.

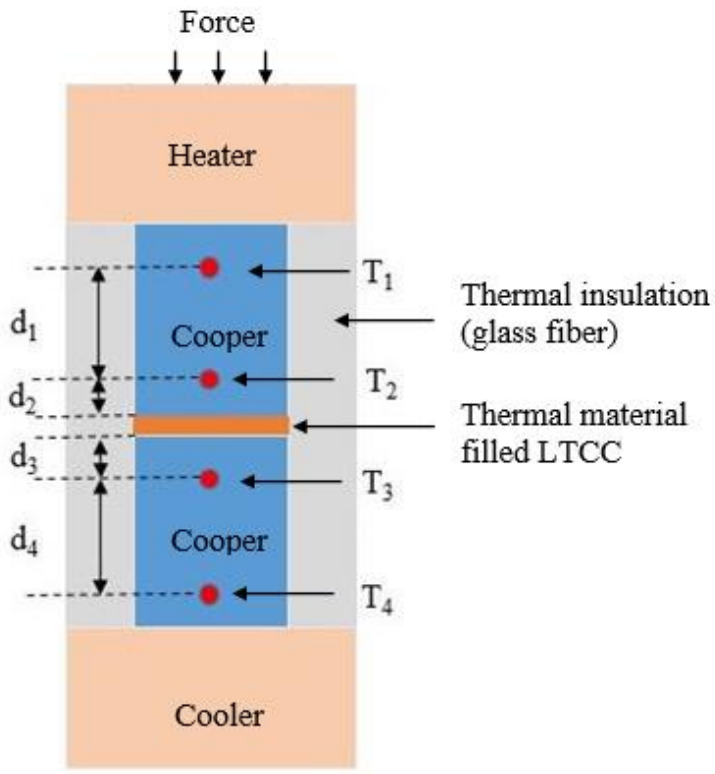


Fig. 4. 5 Schematic of thermal impedance test method.

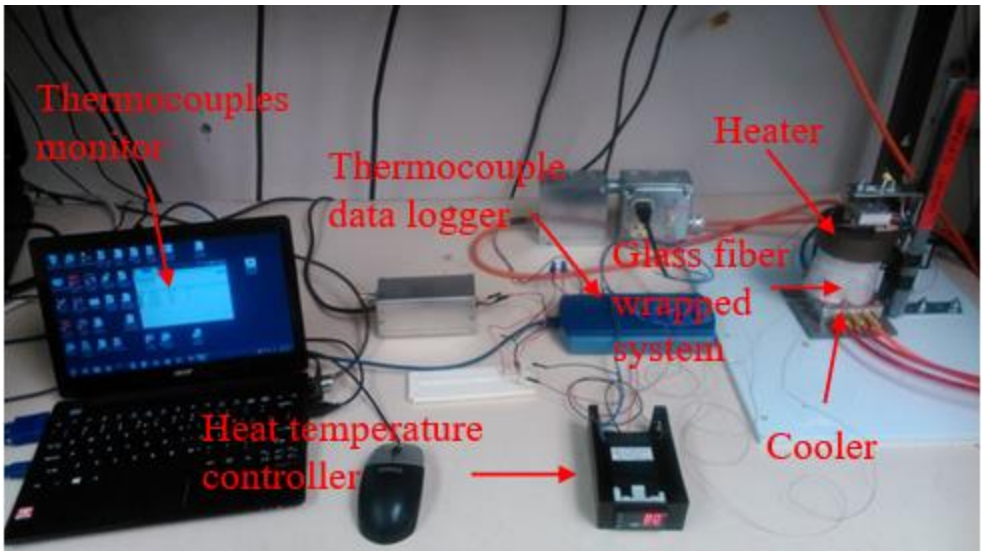


Fig. 4. 6 Experimental set-up for thermal impedance measurement system.

According to the ASTM D5470-06, the heat flow in copper blocks is determined by (4.2) and (4.3)

$$Q_{12} = \lambda_{cu} * A * (T_1 — T_2) / d_1 \qquad (4.2)$$

$$Q_{34} = \lambda_{cu} * A * (T_3 — T_4) / d_4 \qquad (4.3)$$

where λcu is the thermal conductivity of copper, A is the area of 15.85 x 15.85mm surfaces. The average heat flow through the specimen under test is given by (4.4)

$$Q = (Q_{12} + Q_{34}) / 2 \qquad (4.4)$$

The temperatures at the top and bottom surfaces of the LTCC test specimen are given by (4.5) and (4.6)

$$T_{top} = T_2 — d_2 * (T_1 — T_2) / d_1 \qquad (4.5)$$

$$T_{bottom} = T_3 + d_3 * (T_3 — T_4) / d_4 \qquad (4.6)$$

The thermal impedance is then determined by (4.1), where $\Delta T = T_{top} — T_{bottom}$ in this case.

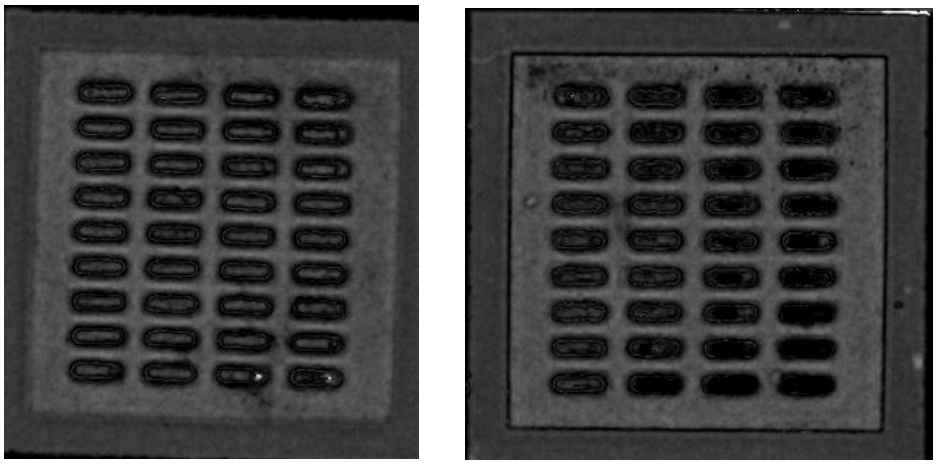
4.3 Results and Discussion

The thermal impedance values measured for different LTCC interposer specimens are listed in Table 4.1. The results reveal that for LTCC samples with circular vias, their thermal impedances increased by 30-40% when nano-diamond-silver composite via filled material was used, while for samples with trench vias, their thermal impedances decreased by 15-25%. Specifically, bigger trench vias yielded smaller thermal impedance values.

Scanning acoustic microscopy (SAM) inspection was performed for the LTCC specimens to examine the paste inside vias. Fig. 4.7 and Fig. 4.8 show the acoustic images of different LTCC interposer samples. As can be seen from Figs. 4.7(a) and (b), the paste inside trench vias is quite uniform with no obvious voids for either sample with different via filled materials within the resolution of the SAM. Fig. 4.8(a) shows that there are no obvious voids observed in circular vias filled with silver paste. However, as shown in Fig. 4.8(b), large number of voids, which are shown as circular shaped white features, is revealed within circular vias of the LTCC interposer filled with nano-diamond-silver paste. The possible cause of the voids could be the change in thermo-mechanical behavior of nano-diamond-silver composites. As mentioned earlier, the co-fired via fill LL601 silver paste is specially formulated to be shrinkage-matched for the DuPont 9k7 LTCC tape, which means the silver paste is able to fully fill vias even after firing. However, introducing nanoparticles into matrix materials changes the viscosity and other mechanical properties of the composite [11], which degrades the thermo-mechanical performance of nano-diamond-silver composites and affects the adhesion of paste to LTCC tapes during firing.

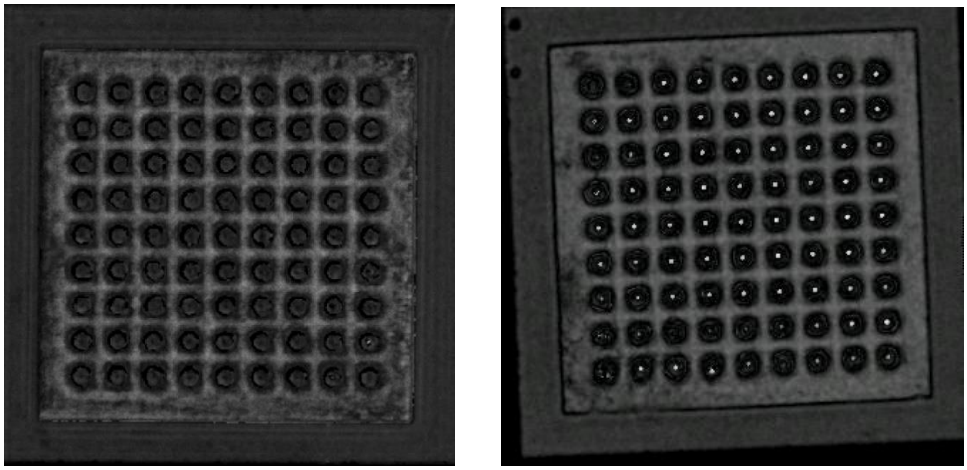
Table 4. 1 Thermal impedance measurement results

Sample	**θ (°C * cm^2/W)**
Ag (12 mil circle)	7.10
Ag + ND (12 mil circle)	9.96
Ag (20 mil circle)	6.99
Ag + ND (20 mil circle)	9.59
Ag (12 mil trench)	8.87
Ag + ND (12 mil trench)	7.01
Ag (20 mil trench)	6.35
Ag + ND (20 mil trench)	5.63



(a) (b)

Fig. 4. 7 SAM images of test specimens (a) 20 mil circle vias filled with silver paste, (b) 20 mil circle vias filled with nano-diamond-silver paste.



(a) (b)

Fig. 4. 8 SAM images of test specimens (a) 20 mil circle vias filled with silver paste, (b) 20 mil circle vias filled with nano-diamond-silver paste.

Simplified two-device packages were simulated to study the effect of different LTCC interposers on their thermal performance. Two power packaging structures with and without an interposer were studied as shown in Figs. 4.9 and 4.10. As can be seen from Fig. 4.9, two SiC devices are attached on DBC, while from Fig. 4.10, an interposer is added on top of the devices. The thermal simulations

were conducted using Solidworks based on experimental results obtained for the interposer. In the simulation, the bulk ambient temperature was set to be 25°C, the two SiC devices dissipated heat in the packages with a total power of 20 W, and the heat convection coefficient h of the surrounding atmosphere was set to be in the range of 200 to 400 W/(m^2*K) as listed in Table 4.2. The measured thermal impedance values were used as the inputs for the thermal simulation to obtain the temperature distributions in the package and the maximum junction temperature T_{Jmax} in devices as shown in Fig. 4.11, Fig. 4.12 and Fig. 4.13, respectively. As can be seen from Table 4.2, in the case of surrounding heat transfer coefficient at 200 W/(m^2*K), the maximum junction temperature of the package with a LTCC interposer consisting of 20-mil nano-diamond-silver paste filled trench vias (lowest thermal impedance) is 34.7°C and 15.1°C lower than those packages without an interposer and with a glass interposer, respectively. The lower the environmental heat transfer coefficient, the more effective the nano-diamond-silver composites filled LTCC interposer is to reduce the maximum junction temperature.

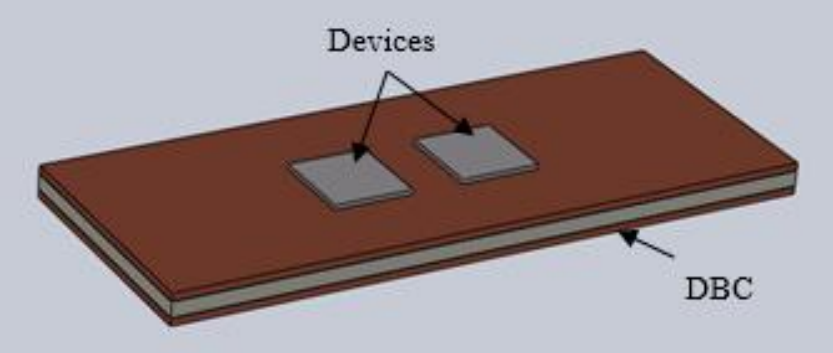


Fig. 4. 9 Silumated two-device package without an interposer.

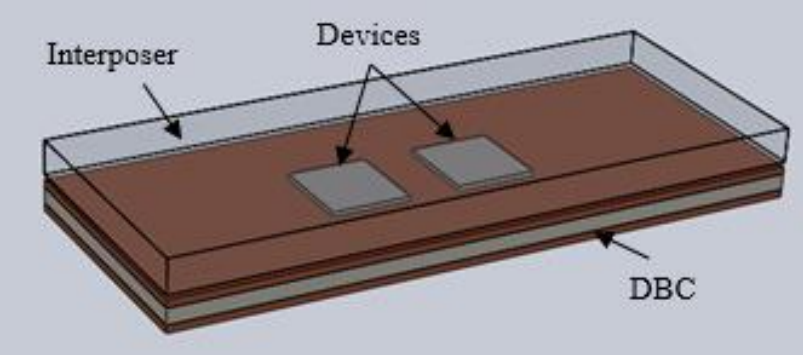


Fig. 4. 10 Silumated two-device package with an interposer.

Table 4. 2 Solidworks thermal simulation results

T_{Jmax} (°C) =		convection coefficient h (W/(m^2*K))			
Case		200	250	300	400
No interposer		202.7	170.0	148.2	120.8
Glass interposer		183.1	155.7	137.1	113.4
LTCC interposer	highest thermal impedance	176.2	150.5	133.0	110.5
	lowest thermal impedance	168.0	144.2	127.0	106.8

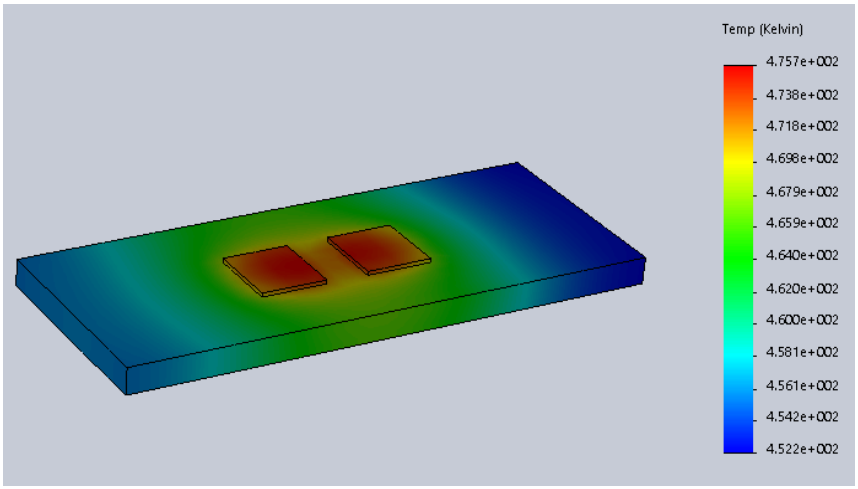


Fig. 4. 11 Temperature distributions in the package without an interposer.

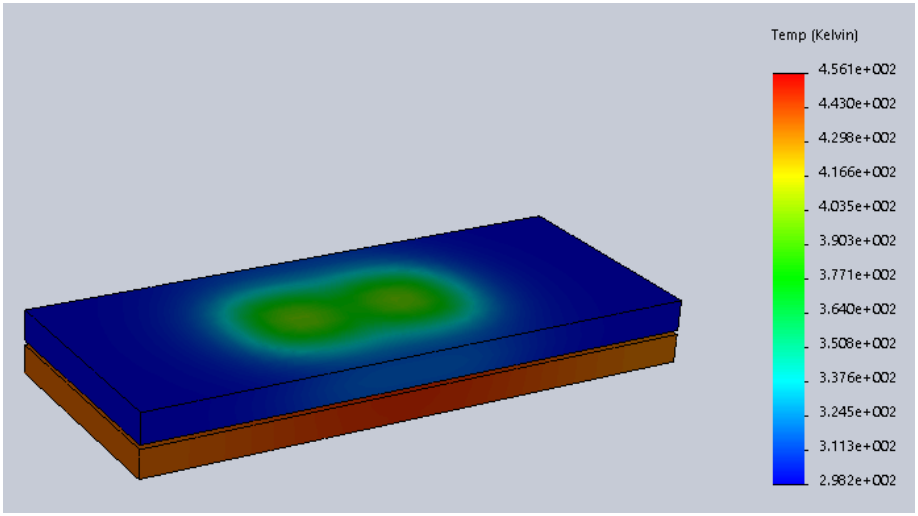


Fig. 4. 12 Temperature distributions in the package with a glass interposer.

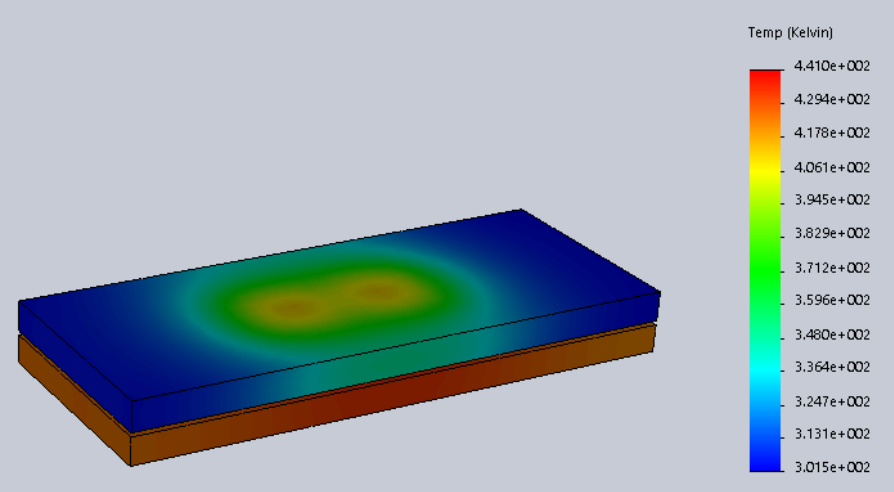


Fig. 4. 13 Temperature distributions in the package with a LTCC interposer filled with nano-diamond-silver paste in 20 mil trench vias.

4.4 Conclusion

This paper proposes a LTCC interposer in 2.5D package for wide bandgap power modules. LTCC is chosen because of its advantages over traditional silicon and glass interposers, especially for modules based on SiC and GaN devices, one of which is its ability to utilize high thermal conductivity materials to enhance its thermal performance in compact power modules. The impact of nano-diamond composites on the LTCC interposer is investigated due to the high thermal conductivity property of nano-diamond. LTCC interposers with different via structures and different via filling materials were fabricated, and their thermal impedance values were measured. It was found that the addition of nano-diamond particles to LTCC co-fired silver paste resulted in an improvement in thermal performance when the composites were used in trench vias by reducing the system thermal impedance of LTCC interposers. In addition, thermal simulation showed that LTCC interposer with nano-diamond composites filled trench vias helped to reduce the junction temperature in power modules. However, the thermal behavior of nano-diamond composites was more affected by the degradation in mechanical properties when used in circle vias, large number

of voids was observed in the circle vias. Future work will be on finding a suitable fraction of nano-diamond in composites to yield an increased mechanical and thermal performance of the nano composites.

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Chapter 5 Investigations of Graphene and Pyrolytic Graphite Sheet (PGS) to Improve the Thermal Performance of LTCC Interposer

Chapter 3 consists of a published IEEE paper with the following citation:

S. Huang and S. S. Ang, "Investigations of low temperature co-fired ceramic heat spreading interposer for the thermal management of three-dimensional packages," 2018 *34th Thermal Measurement, Modeling & Management Symposium (SEMI-THERM)*, San Jose, CA, 2018, pp. 8-12, doi: 10.1109/SEMI-THERM.2018.8357346.

Investigations of low temperature co-fired ceramic heat spreading interposer for the thermal management of three-dimensional packages

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Abstract

The heat density in three-dimensional (3D) power module packages is significantly increased because of the stacked structure and the small footprints of devices, making thermal management a key issue to maintain the performance of these power modules. This paper proposes a low temperature co-fired ceramic (LTCC) heat spreading interposer as a novel cooling solution for 3D packages, and investigates the effects of various high thermally conductive materials on the thermal performance of the interposer, including graphene and pyrolytic graphite sheet (PGS). A two-chip face-to-face stacked configuration was used as the model for analysis and thermal

simulations. Steady state temperature tests were performed on the LTCC interposers of different structures and integrated with different thermal spreading materials, and their thermal performance were compared.

Keywords

Three-dimensional (3D) package, Low temperature co-fired ceramic (LTCC) interposer, thermal management.

5.1 Introduction

The power density of current mobile electrified systems is expected to increase significantly in order to achieve economic and environmental benefits. As a result, new power electronic module packaging architecture, such as the three-dimensional (3D) package, has gained more and more attention for its enhanced system performance. In a 3D package, multiple chips are stacked vertically with an interposer between them to achieve higher electrical interconnect density and short interconnect length [1]. Many researches have been carried out to demonstrate the low inductance advantage of wire bondless 3D packaging of semiconductor devices, which can mitigate the problems of ringing, overshoots and EMI emissions [2]. On the other hand, the heat density in the 3D packages is much higher than the conventional 2D packages due to the higher circuit density and closer distances between chips. To guarantee the electrical performance and improve the thermo-mechanical reliability of the 3D modules, it becomes a key issue to dissipate heat near devices more efficiently to avoid hot spots.

Conventional cooling methods for a 3D package utilize direct bond copper (DBC) substrates at both top and bottom of the power module as double-sided cooling. Heat is removed from both the

top and bottom DBCs. However, additional cooling solutions are needed when the double-side cooling is not sufficient for the high heat density situations. Other than introducing liquid cooling integrated within the 3D package, in which situation mechanical components such as pumps and valves are needed, high thermally conductive material can be used to conduct heat near the power devices horizontally to the outer ambient [3].

Silicon and glass interposers have been reported because of their capability to achieve high I/O density, and the possibility to improve their thermal characteristics by through-package vias (TPVs) [4]. However, silicon interposer has the disadvantage of high electrical loss, while the thermal conductivity of glass interposer is as low as 0.8-1.0 W/(m*K). Besides, only vertical TPVs can be built and utilized within the silicon and glass interposers, which limits the design of interconnect distribution and the usage of long horizontal edge of interposers [5].

In this paper, we propose the low temperature co-fired ceramic (LTCC) as an interposer used in 3D module packages. First, compared to silicon and glass whose coefficient of thermal expansion (CTE) is 2.6 ppm/℃ and 54 ppm/℃, respectively, LTCC tape has a CTE of 4.4 ppm/℃ [6], which is close to the CTE of silicon carbide (SiC), 4.0 ppm/℃. Matching CTE values improve the reliability of module by reducing the risk of warpage or delamination between layers [7]. Second, LTCC substrate can accommodate complex interconnect and cavity structures, which allows coordinated integration of both electrical and thermal power routes for heterogeneous 3D power module structures, hence the LTCC interposer can offer cooling ability without degrading the electrical performance of 3D module. Besides, its low loss characteristics make it suitable for high frequency applications up to 100GHz. Last but not least, LTCC can be used as substrate to integrate materials such as graphene and pyrolytic graphite sheet (PGS), which have high thermal

conductivity and small volume, making them potential solid-state thermal conduits within the LTCC tape to aide spreading of heat away from hot spots within the module.

As various materials are proposed, it is important to evaluate their effects for thermal management. The study herein performs the thermal analysis of LTCC interposer test coupons with different candidate materials using simulation and temperature measurement tests, their thermal performance is compared and discussed.

5.2 Method

To study and measure the thermal performance of LTCC interposers with different thermally conductive materials, a two-chip face-to-face stacked configuration was used for analysis as shown in Fig. 5.1. In this 3D module, two chips are placed on two opposite sides of LTCC interposer and connected by through via arrays in the LTCC interposer. DBC substrates are attached on the other side of each chip to dissipate the heat generated by chips as double-sided cooling. The two power chips of size 3.10 mm x 3.36 mm dissipating a total 20W power are considered in this structured.

When LTCC heat spreading interposer is integrated, the maximum junction temperature of devices decreases as shown in Fig. 5.2. As the thermal conductivity of a LTCC interposer increases to 100 W/(m*K), the maximum device temperature reduces from 115℃, when no interposer is presented, to 87℃. Hence, in order to reduce the chip temperature, higher thermally conductive interposer is desired. To achieve that, high thermally conductive materials are integrated within the LTCC interposer.

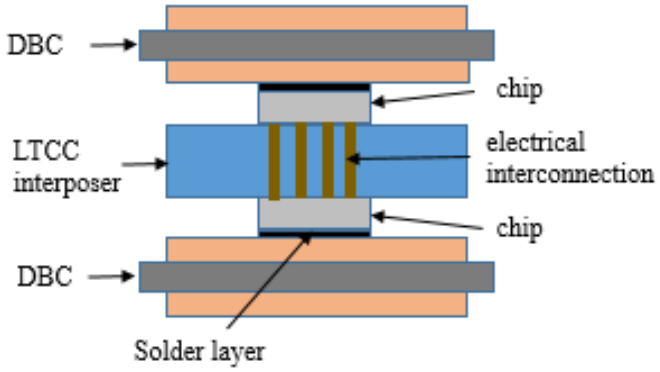


Fig. 5. 1 3D package model used for analysis.

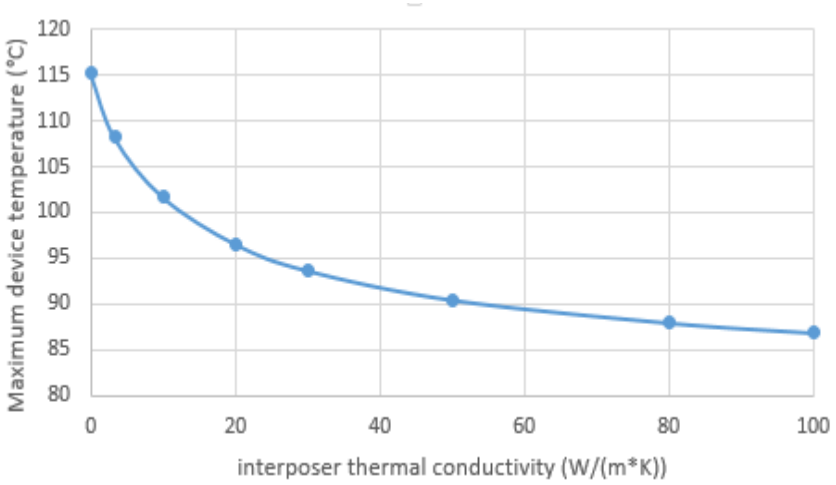


Fig. 5. 2 Temperature versus thermal conductivity for the LTCC heat spreading interposer.

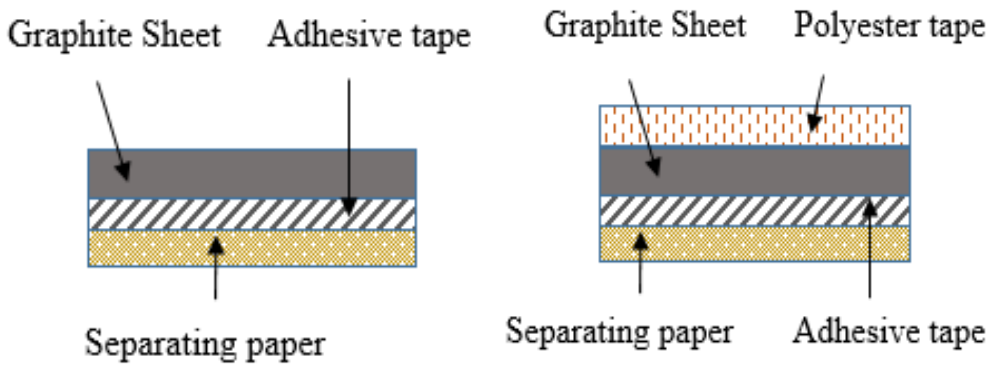
5.2.1 Thermal Spreading Material Preparations

Graphene nano-powder and pyrolytic graphite sheet (PGS) were chosen to form thermal conduits within the LTCC interposer because of their high thermal conductivities.

The graphene nano-powder of 5-30 nm average flake thickness was dispersed in ethyl acetate by a mixer at 2500 RPM for 30 minutes, followed by an ultrasonic bath for 10 minutes to maximize the dispersion. Then the dispersed graphene nano-powder was mixed with silver (Ag) paste matrix

to improve the thermal conductivity as its in-plane thermal conductivity is much higher than the cross-plane thermal conductivity, so that the heat can flow to sides of the power module along the longest thermal path as compared to thermal paths to the top and bottom.

PGS from Panasonic is a graphite polymer film with an in-plane thermal conductivity ranging from 700 to 1950 W/(m*K), which can diffuse the heat generated by heat sources horizontally through it in the power package. Two different types of PGS, A-M and A-DM, were used. Both sheets have similar 10 μm thickness and same in-plane thermal conductivity of 1950 W/(m*K). However, the A-M type has only 10 μm adhesion tape on one side, while the A-DM type has an additional 10 μm polyester insulation tape on the other side. The cross-section view of the two PGSs is shown in Fig. 5.3 [8].



(a) (b)

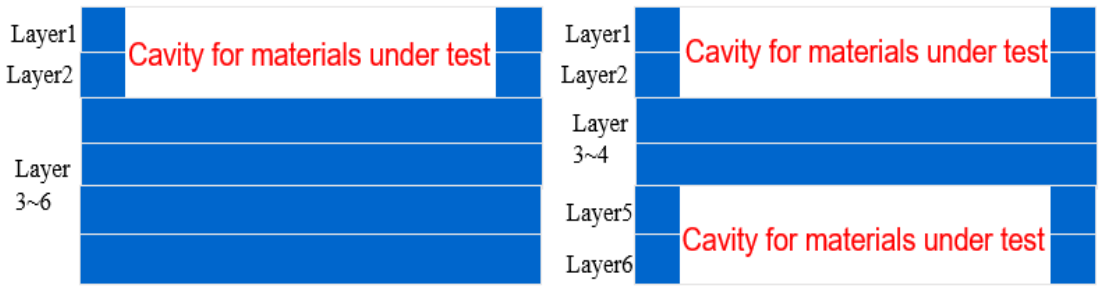
Fig. 5. 3 (a) A-M type PGS (b) A-DM type PGS.

5.2.2 LTCC Interposer Substrate Fabrication

Considering the material properties, two different LTCC interposer structures were designed, one is with surface channels where material under test is filled in, and the other one is with material attached on interposer surfaces.

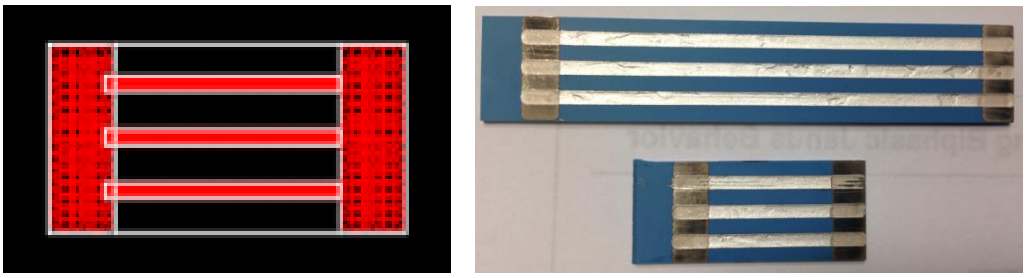
In the case of graphene nano-powder and sliver paste composite, both one-side and double-sided surface channels with two different lengths (30 mm and 77.5 mm) are designed and fabricated within LTCC substrates, as shown in Figs. 5.4 and 5.5. Cavity was punched on some LTCC green tapes, and then they were stacked with blank LTCC tapes according to designs shown in Figure 5.4. For the one-side channel, LTCC co-fired silver paste is filled onto the top two layers of LTCC tape. As for the double-sided channels, besides LTCC interposer sample with channels filled with only co-fired silver paste was prepared, sample with LTCC co-fired silver paste embedded in the 2nd and 5th layers, and then graphene and sliver composite filled in the top 1st and bottom 6th layers after LTCC tape firing, was also fabricated. Graphene-sliver mixture was filled in the post-fire process, since graphene decomposes at around 400℃, while LTCC firing can go as high as 850℃ in order to transfer the soft green tapes to solid ceramic.

As for the case of PGS, they were attached on both top and bottom surfaces of LTCC interposers of 77.5 mm in length using its adhesion tape. The fabricated sample is shown in Fig. 5.6.



(a) (b)

Fig. 5. 4 Cross section view of (a) one-sided surface channel and (b) double-sided surface channels within LTCC interposer.



(a) (b)

Fig. 5. 5 (a) Top view of LTCC surface channels; (b) Fabricated LTCC interposer samples with surface channels filled.

Fig. 5. 6 Fabricated LTCC interposer sample with PGS attached on surfaces.

5.2.3 Steady State Temperature Tests

To test the thermal performance of different LTCC interposer samples, temperature measurement method as shown in Fig. 5.7 is used. Tests were conducted with the LTCC interposer samples placed horizontally and exposed to ambient air, a 3~5cm wide distance was kept between test coupons if more than one was under test at the same time. Two power film resistors were placed face to face on both top and bottom surfaces of the LTCC interposer, acting as power device heat sources dissipating same and constant power during test. T-type thermocouples connected to a data logger were placed between each resistor and interposer to measure and record the device temperatures. Equilibrium was assumed when the temperature variation was within ±0.1°C/min,

and the device temperatures at both top and bottom were recorded when stable. The experimental setup is shown in Fig. 5.8.

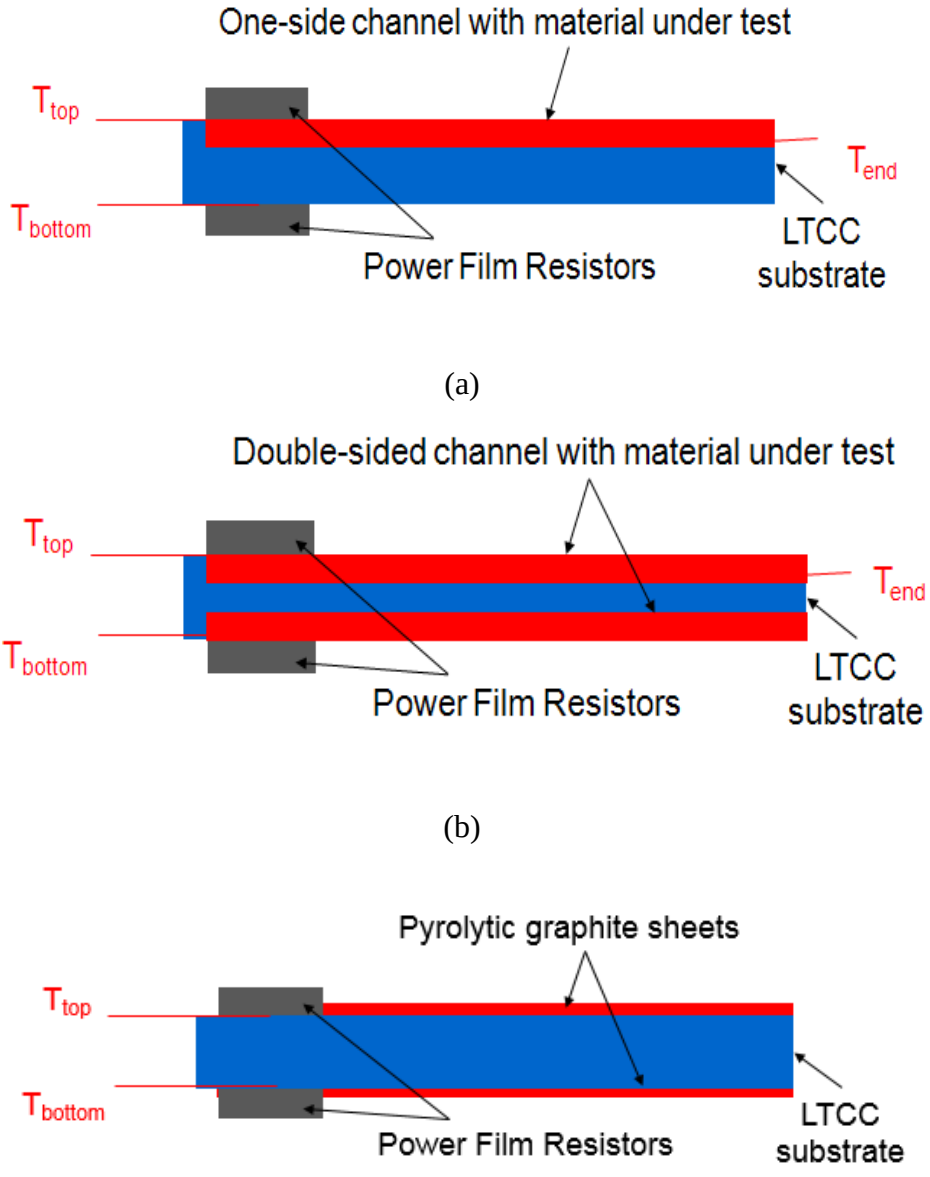
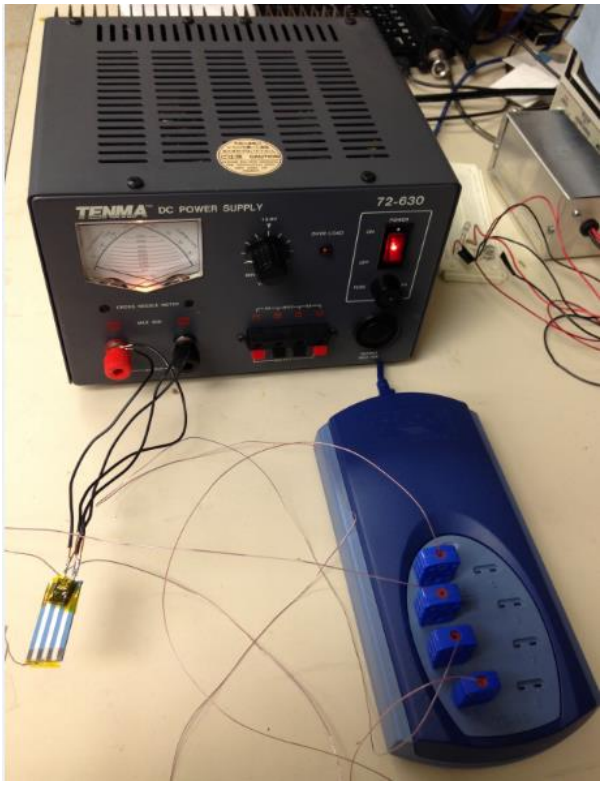
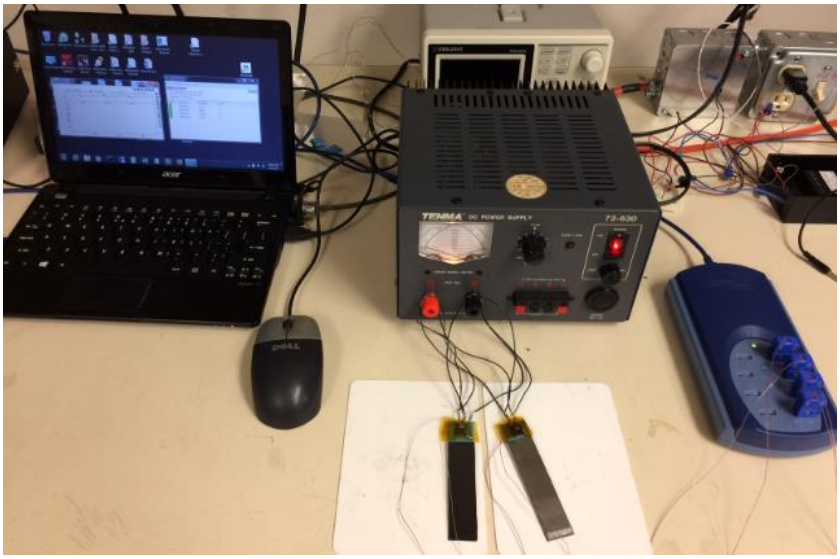


Fig. 5. 7 Temperature measurement method for LTCC interposer with (a) one-side surface channel (b) double-sided surface channels (c) surface attachedTemperature measurement method for LTCC interposer with (a) one-side surface channel (b) double-sided surface channels (c) surface attached.



(a)



(b)

Fig. 5. 8 Experimental set-up for temperature measurement on samples of (a) one LTCC interposer with surface channel (b) two LTCC interposers with different types of PGS.

5.3 Results and Discussion

Table 5.1 shows the test results for the LTCC interposers in which thermal conduit channels of different lengths and with different materials filled into, including silver (Ag) paste only and the mixture of graphene and silver paste. Maximum temperatures at both power film resistors, which acted as the heat sources, attached on top and bottom surfaces of LTCC interposer after steady state were recorded.

Table 5. 1 Device temperature measurement results for LTCC interposer with surface channels

Test Sample			**T_{top} (℃)**	**T_{bottom} (℃)**
30mm	No channel	Blank tape	97.5	91.5
	One-side channel	Ag	82.7	86.6
	Double-sided channels	Ag	81.5	79.3
		mixture	76.8	71.8
77.5mm	No channel	Blank tape	94.2	83.2
	One-side channel	Ag	82.8	85.9
	Double-sided channels	Ag	80.9	72.2
		mixture	68.5	64.3

As can be seen from Table 5.1, for similar lengths, when the same silver paste is used, the interposer with double-sided thermal conduit channels shows a better thermal performance with lower device temperatures. As can be seen, the addition of graphene nano-powder further improves the thermal performance of the LTCC interposer. The maximum temperature drop compared to LTCC interposer without thermal conductive channels happens when graphene and silver paste

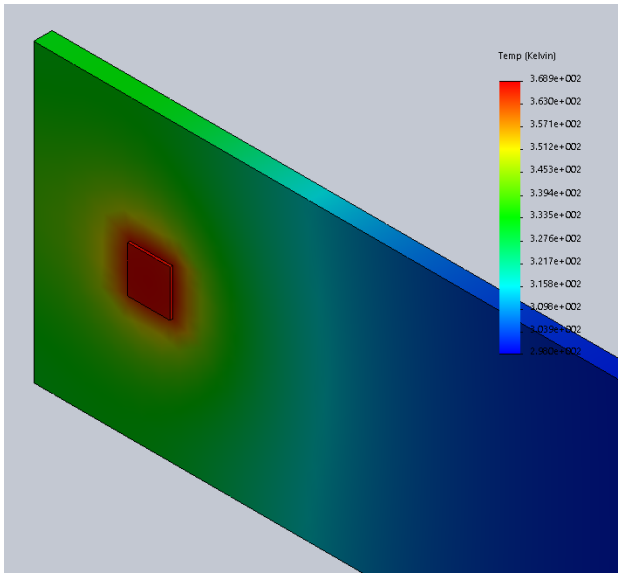
mixture is filled in the double-sided channels, and the values are 20.7℃ and 25.7℃, respectively for the 30mm and 77.5mm channels.

Table 5.2 shows the test results when PGS was attached onto LTCC interposer surfaces. It demonstrates that the PGS enhances the thermal performance of LTCC substrate and reduces the device temperature by 9.3~13.8°C, similar to the thermal simulation results shown in Fig. 5.9, where the addition of PGS to LTCC interposer helps reduce the maximum junction temperature in the power module from 95.7°C to 83.8°C, a 11.9°C temperature drop. Notice that the bottom device temperature is lower than that of top device because ceramic substrate underneath test coupons helped release the heat from the bottom during experiment, as shown in Fig. 5.8(b). While in the thermal simulation, only air convection is considered.

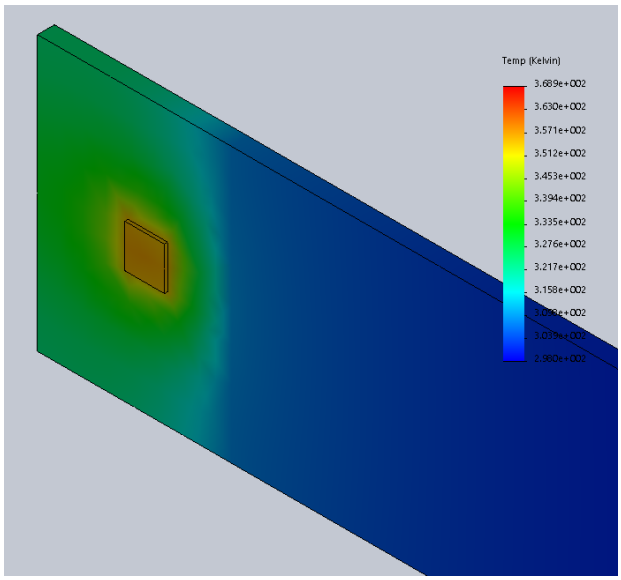
Between the two types of PGS, the A-M type without polyester insulation tape performs better than the A-DM type with a further 4.5~5.4°C reduction in device temperatures. On the other hand, when layer up the A-M type PGS, the thermal conductivity of LTCC interposer is reduced and the device temperatures increase. This could result from the adhesion tape on the top layer of PGS acting as an insulation and blocks the heat transfer.

Table 5. 2 Device temperature measurement results for LTCC interposer with PGS attached

Test Sample	**T_{top} (℃)**	**T_{bottom} (℃)**
Blank LTCC substrate	94.2	83.2
A-M type PGS	80.5	69.4
A-DM type PGS	85.9	73.9
Double layered A-M type PGS	85.4	80.4



(a)



(b)

Fig. 5. 9 Thermal simulation results for (a) blank LTCC interposer and (b) LTCC interposer with PGS attached on surfaces.

5.4 Conclusion

This paper proposes LTCC interposer integrated with high thermally conductive materials as thermal management for 3D power electronic module packages. LTCC is chosen as substrate for

interposer because it is able to provide a high density, high reliability, high performance and low-cost interconnect package. The thermal performance of LTCC interposers with graphene nano-powder and pyrolytic graphite sheets is investigated by the steady state temperature test. Both materials help reducing device temperature in a 3D package when they are applied to LTCC interposer. Specifically, the mixture of graphene nano-powder and sliver paste results in bigger improvement in thermal performance than PGS, but it has high requirement of dispersion uniformity since the nanoparticles are prone to agglomeration. The PGS is easy to use, stable and affordable, making it a potential heat spreader on LTCC interposer.

5.5 Acknowledgments

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5.6 References

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Chapter 6 Design and Validation of a 3.3-kV Double-sided Wire-Bondless SiC Power Module

6.1 Introduction

Silicon carbide (SiC) power devices have demonstrated their advantages of performance including higher efficiency, compact size, reduced system cost, and high-frequency and high-temperature applications, when compared to silicon (Si) power devices, which have been the dominating choice for power electronics applications for decades but exhibits several limitations regarding blocking voltage, switching frequency, and operation temperature [1] [2]. These properties enable SiC power devices to be used for high power density and high efficiency power electronics applications. Right now, SiC power device technology has been developed fast towards medium to high voltage, e.g., 3.3 - 15kV [3]. Several manufacturers such as CREE and Microchip have successfully released 3.3 kV SiC MOSFETs with superior performance compared to Si IGBTs.

However, the conventional low-voltage power module packaging technologies are not good enough for high-voltage application because of the accompanying issues such as electric field mitigation at triple point (DBC metal, DBC ceramic and encapsulant) which leads to partial discharge and consequent breakdown, high voltage isolation, creepage and clearance distances, high-speed switching, and heat flux removal.

The objective of this work is to develop an advanced packaging design for the 3.3-kV SiC MOSFETs. The proposed package enables the SiC MOSFETs to switch high voltages in tens of nano-seconds with small voltage spike and oscillation, the size of the module is kept compact to achieve high power density, and potential double sided cooling helps maximize heat removal from the power devices. A dual common source MOSFET power module was achieved. The approaches

include double-sided wire-bondless packaging design, molybdenum (Mo) post interconnection, and two-step passivation were applied. The detailed design of the wire-bondless common source module package for 3.3-kV SiC MOSFETs is presented, as well as the fabrication process and electrical test results.

6.2 Design of a 3.3-kV Wire-bondless SiC-MOSFET Based Common Source Module

This section presents the design of a wire-bondless medium-voltage power module package for 3.3-kV SiC devices. The 3.3-kV, 40-mΩ, 50-A SiC MOSFETs from CREE are selected. As mentioned earlier, there are several challenges for medium-to-high voltage power module package, one of the biggest issue is that the electrical field strength in the module is increased, and if the electric field strength exceeds the dielectric breakdown strength of the insulating materials, partial discharge or breakdown may happen and damage the insulating materials, such as encapsulation material and ceramic substrate [4]. The other common challenges include thermo-mechanical stress due to more interfaces and larger contact areas in a wire-bondless module, the need of a good cooling system since the MOSFET has high power dissipation, and the sensitivity to parasitic inductances for the high-speed switching application in order to minimize voltage overshoot and ringing during switching transience.

6.2.1 Overview of the Module Design

The double-sided stack wire-bondless module package introduced in Chapter 2 and 3 has several advantages including small size, low parasitic inductance, and improved thermal management system. In order to move forward to higher voltage module package, metal post interconnection is proposed [5], the cross-section view of a typical structure is shown in Fig. 6.1. The metal posts provide shorter interconnects so that lower parasitic inductance, and electrical isolation between

top and bottom DBC substrates, as well as reduce the electric field concentration in the power module [6] [7]. By changing the height of the metal posts, higher blocking voltage of the module can be achieved.

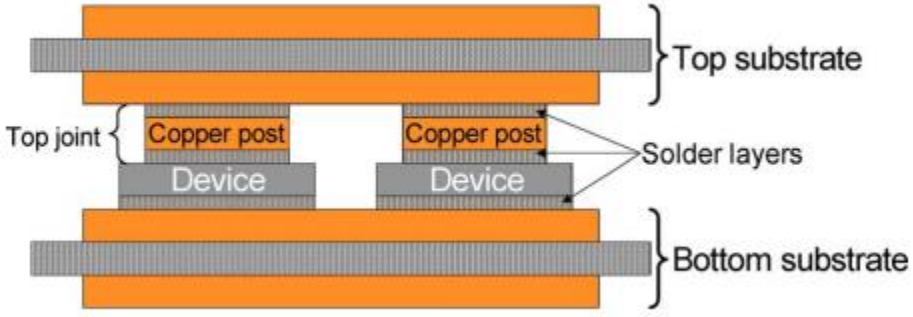
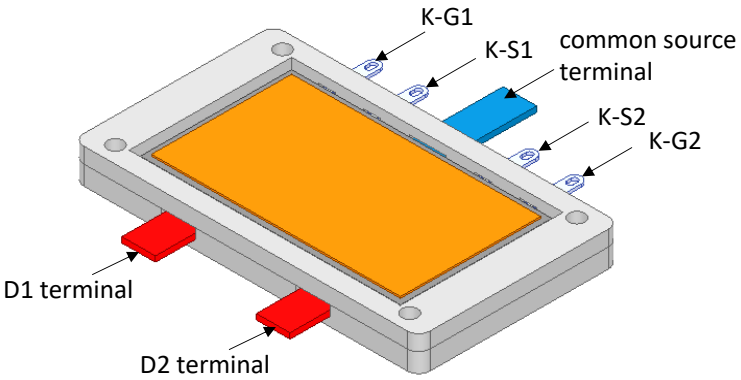


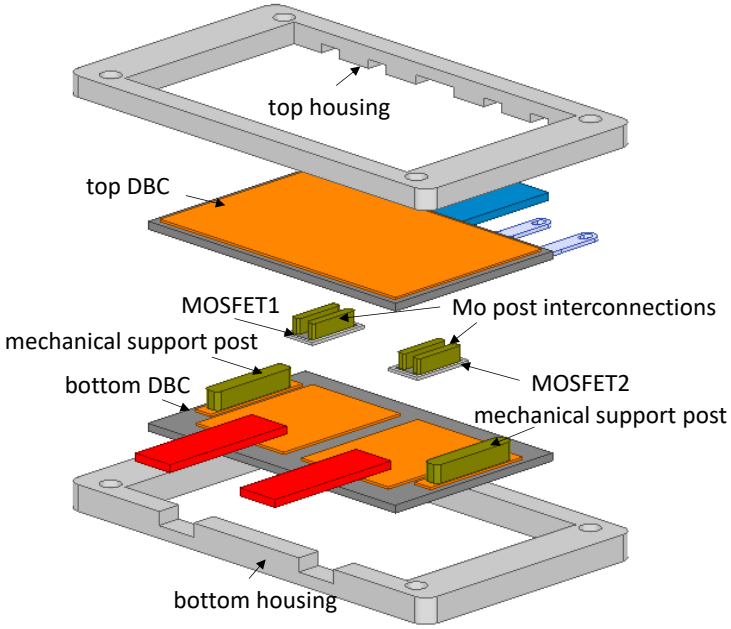
Fig. 6. 1 A wire-bondless module using Cu posts for interconnection [6].

As a result, a wire-bondless module package as shown in Fig. 6.2 (a) is proposed for a due common source module, the exploded view is shown in Fig. 6.2 (b), and the schematic of which is shown in Fig. 6.2 (c). The due common source module has two 3.3-kV SiC MOSFETs with common source, which can be used for applications such as three-phase rectifiers, switched-mode and resonant-mode power supplies, and uninterruptible power supplies. The proposed module package has symmetrical design and sandwich structure, molybdenum (Mo) posts are used to achieve wire-bondless interconnection for devices. This compact structure allows for increased power density and reduced parasitic inductance, hence improved dynamic performance [8]. Two DBC substrates are used, one at bottom for die attachment, and the other one at top for electrical connection. Besides interconnection for the bare dies, Mo posts of different height are used as standoffs that provide mechanical support and reduce the electric field strength in the module. Mo is selected

due to its close coefficient of thermal expansion (CTE) to SiC, which is 4.8 ppm/°C to 4.0 ppm/°C, so the thermos-mechanical stress at the interface between Mo post and SiC die can be lowered.

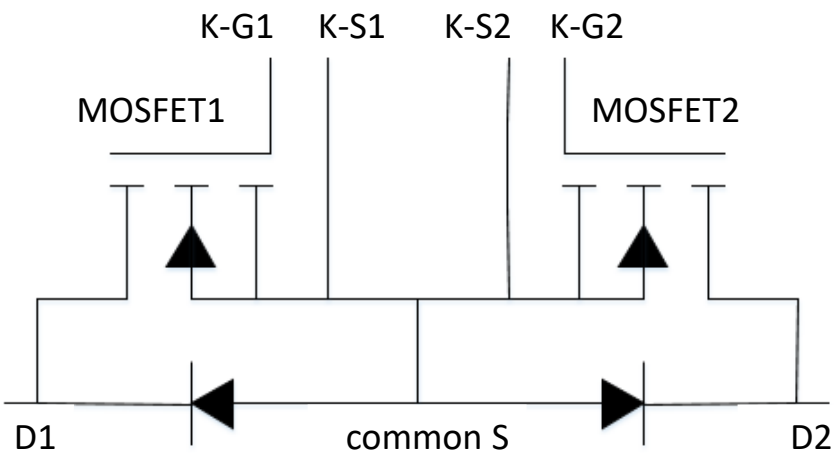


(a)



(b)

Fig. 6. 2 (a) A proposed wire-bondless module package for 3.3-kV SiC MOSFETs, (b) the exploded view of the module, and (c) the schematic of a due common source module.



(c)

Fig. 6. 2 Cont. (a) A proposed wire-bondless module package for 3.3-kV SiC MOSFETs, (b) the exploded view of the module, and (c) the schematic of a due common source module.

The size of the proposed module is 27 mm x 46.4 mm x 5.7 mm without the housing, and the maximum power dissipation of each MOSFET is 319 W, which gives a power density of 89.3 kW/L. And the size turns to 35.8 mm x 61.7 mm x 5.7 mm when the housing is included, which gives a power density of 50.6 kW/L. For reference, the power density of Wolfspeed's 3.3-kV module in XHP^{TM} 3 package is 0.98 kW/L when two MOSFETs are included.

The design of the module consists of several parts, two critical considerations are the DBC substrate design and the Mo post selection, because they will greatly affect the electric field distribution in this medium-voltage module and the thermos-mechanical stress in this sandwich structure. The details of the design is discussed in the following sections.

6.2.2 Electric Field Simulation

In a high-voltage and high-density power module, the electric field increases accordingly. If this electric field exceeds the breakdown strength of the substrate ceramic or encapsulation material, partial discharge will occur at triple point, as shown in Fig. 4, where the electric field concentrates [9]. Repetitive partial discharge can eventually lead to module failure, such as breakthrough in the ceramic substrate.

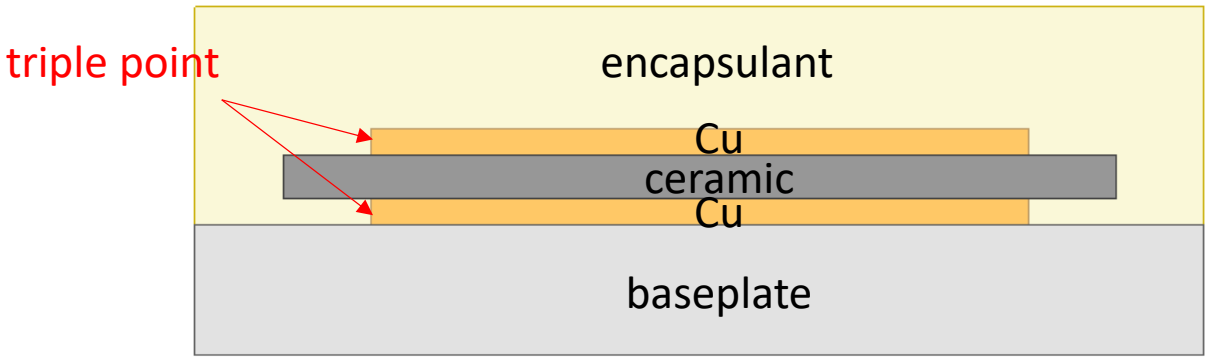


Fig. 6. 3 Triple point in a power module.

In order to reduce the electric field for higher voltage in power modules, the DBC substrate design needs to be optimized. As can be seen from Fig. 6.4, there are three paths where breakthrough can happen, therein, path A depends on the ceramic thickness and material dielectric strength, besides these, path B and C additionally depend on the encapsulation and DBC substrate layout geometry [10]. Researches in [11] also indicated that the stacking DBC substrates can reduce the peak electric fields. Therefore, in this section, the electric field simulations are introduced for different materials and DBC layout designs, and the results are discussed.

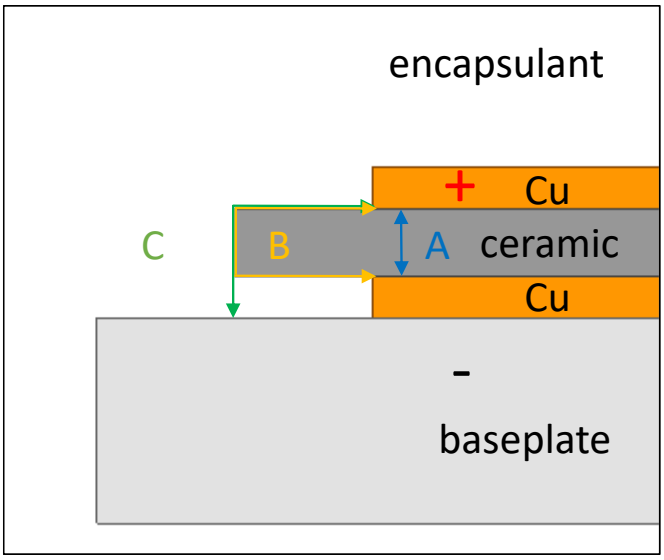


Fig. 6. 4 High voltage isolation of ceramic substrates [10].

Fig. 6.5 shows the simulation model of the DBC substrate, the potential of one top Cu pad is set to be 3.3 kV, representing the drain of one MOSFET which is consistently at the positive potential, the potential of the other top Cu pad is set to be 0 V, representing the worst case that the other MOSFET is conducting. The bottom Cu layer is grounded (0 V). The thickness of ceramic (t) and the distance between Cu layer edge and ceramic edge (d_{top} for top and d_{bottom} for bottom Cu layer, respectively) are varied.

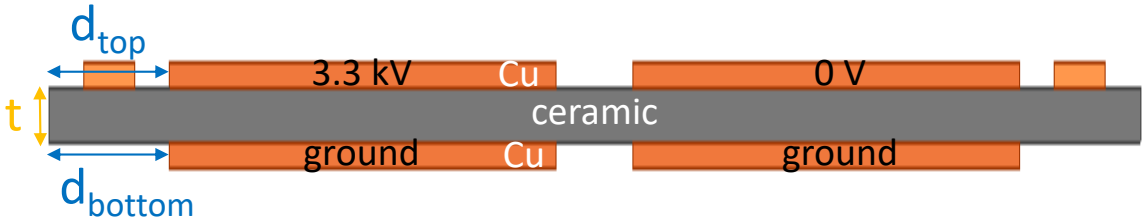


Fig. 6. 5 Electric field simulation model.

Fig. 6.6 shows the simulated 2-D electric field distribution for Al_2O_3 and AlN DBC substrates of the same layout design and thickness (1mm). The maximum electric field strength at triple point is 4.29 kV/mm for Al_2O_3 DBC, and 4.24 kV/mm for AlN DBC. This is predictable because the AlN has slightly higher dielectric strength (17 kV/mm) than the Al2O3 (14.6 kV/mm).

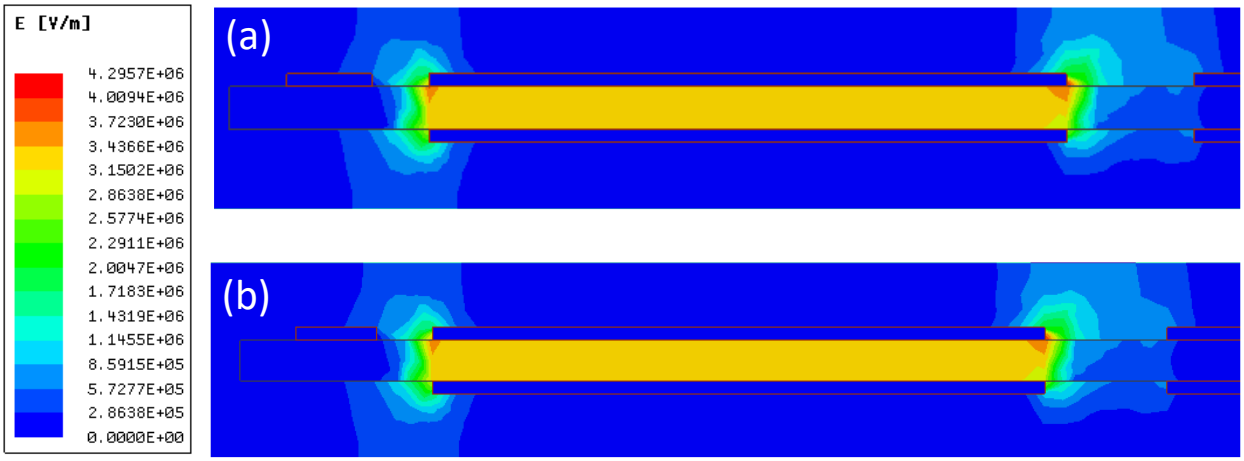


Fig. 6. 6 Electric field simulation results for 1-mm-thick (a) Al_2O_3 and (b) AlN DBC substrates.

Fig. 6.7 shows the simulation results for AlN DBC substrates of the same layout design but different thickness (t). Two different thickness, 0.635 mm and 1 mm based on the availability of commercial DBC substrates, were simulated. The maximum electric field strength is 6.20 kV/mm for 0.635-mm-thick AlN DBC, and 4.24 kV/mm for 1-mm-thick AlN DBC. Therefore, thicker ceramic helps reduce the electric field strength in the module.

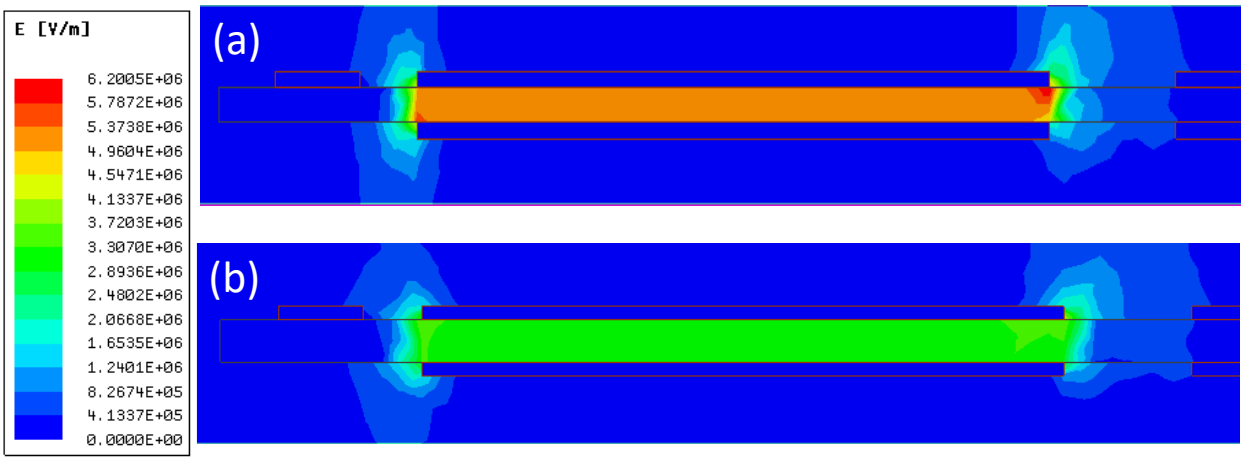


Fig. 6. 7 Electric field simulation results for (a) 0.635-mm-thick and (b) 1-mm-thick AlN DBC substrates.

Fig. 6.8 shows the simulation results for 1-mm-thick AlN DBC substrates with different offset, $d_{offset} = d_{top} - d_{bottom}$, where d_{top} and d_{bottom} are the distances between Cu layer edge and ceramic edge as defined earlier. d_{offset} is set to be 3.35 mm, 0 mm, and – 3.35 mm, and the simulated maximum electric field strength is 5.02 kV/mm, 4.24 kV/mm, and 4.23 kV/mm. Therefore, thicker ceramic helps reduce the electric field strength in the module. The offset value of 0 mm results in about 15% lower maximum electric field strength compared to the offset value of 3.35 mm, but there isn't much improvement when keep reducing the offset value. Considering the smaller bottom Cu area will limit the heat spreading, the offset value of 0 mm, which means the top and bottom Cu layers align, will be further investigated. Fig. 6.9 shows the difference when the bottom Cu of DBC substrate is either one whole piece or two separated pieces aligning with the top Cu. The one whole piece of bottom Cu results in a maximum electric field of 5.09 kV/mm, which is 20% higher than 4.24 kV/mm of the other case.

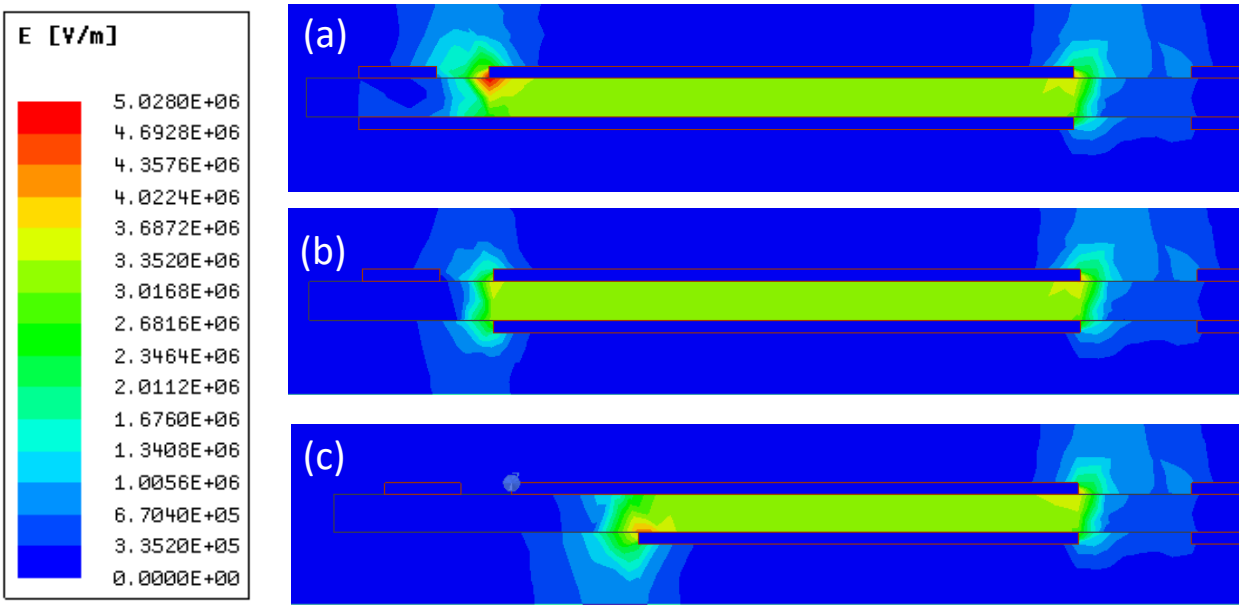


Fig. 6. 8 Electric field simulation results for 1-mm-thick AlN DBC substrates with top and bottom metallization layer edge offset of (a) 3.35 mm, (b) 0 mm, and (c) -3.35 mm.

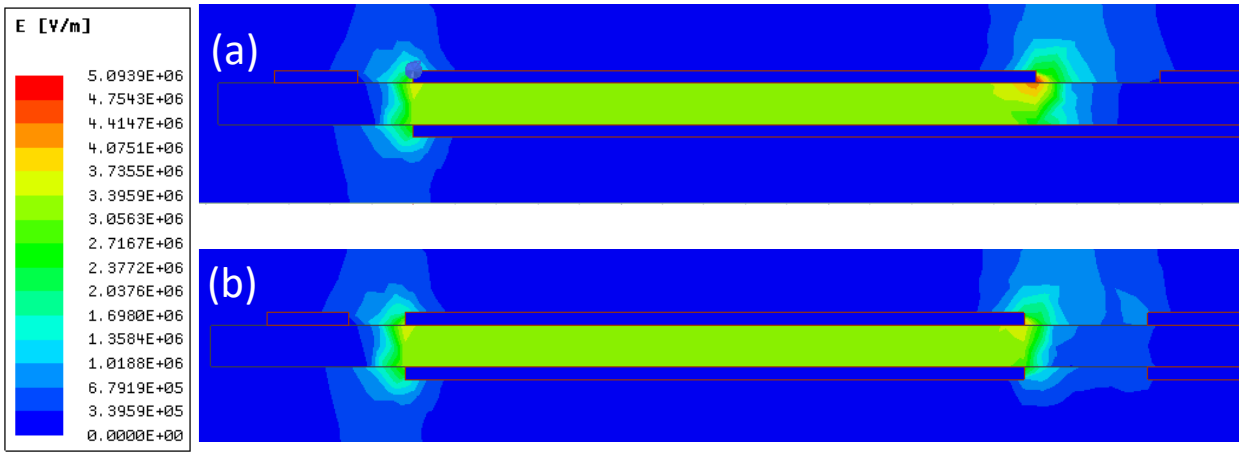


Fig. 6. 9 Electric field simulation results for 1-mm-thick AlN DBC substrates with (a) one whole piece of Cu pad and (b) two separated Cu pads at bottom.

The electric field simulation results of single and stacked AlN DBC substrates of the same layout design are showed in Fig. 6.10. The maximum electric field strength of one layer of 1-mm-thick

AlN DBC is 4.24 kV/mm, while the value of two layers of stacked 0.635-mm-thick AlN DBC is 4.06 kV/mm. As can be seen from Fig. 6.10, stacking DBC substrates help reduce the electric field strength both at the triple points and the ceramic.

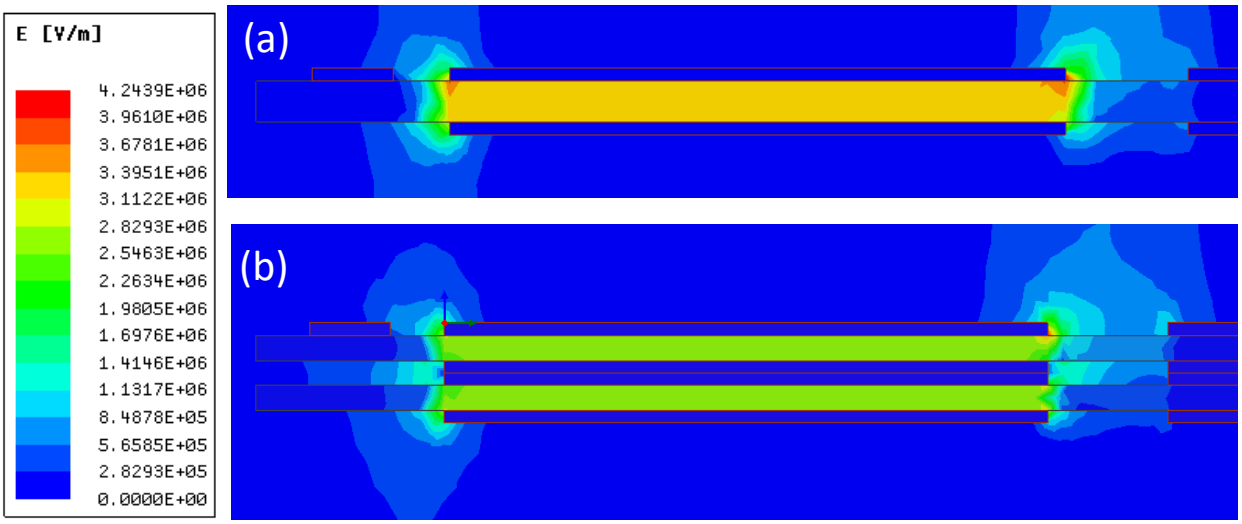


Fig. 6. 10 Electric field simulation results for (a) single 1-mm-thick and (b) two stacked 0.635-mm-thick AlN DBC substrates.

Different top Cu layer layout designs were also simulated. As can be seen from Fig. 6.11, d_1 is defined as the distance between the ceramic edge and the edge of Cu trace for Mo post standoff to be attached, while d_2 is defined as the distance between the Cu traces for Mo post standoff and for device to be attached, respectively. The simulation results are listed in Table 6.1, when both d_1 and d_2 are 1 mm, the peak electric field strength is relatively lower.

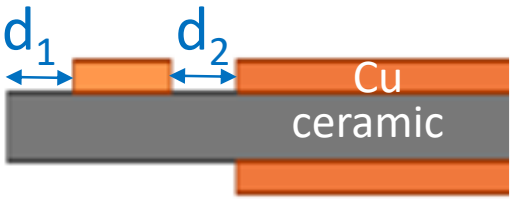


Fig. 6. 11 Electric field simulation model for different top Cu layout.

Table 6. 3 Simulated maximum electric field strength of different top Cu layout

d_1 (mm)	d_2 (mm)	maximum electric field strength (kV/mm)
1	1	4.16
1	2	4.40
2	1	4.40
2	2	4.34

Besides DBC substrate design, the Mo post height is another factor that influences the electric field distribution within the module. The posts help reduce the electric field and improve the voltage isolation in the power module. The electric field distribution was simulated for different height of Mo post, as shown in Fig. 6.12, the electric field strength at triple point reduces from 4.29 kV/mm to 4.15 kV/mm when increasing the Mo post height from 1.6 mm to 2 mm.

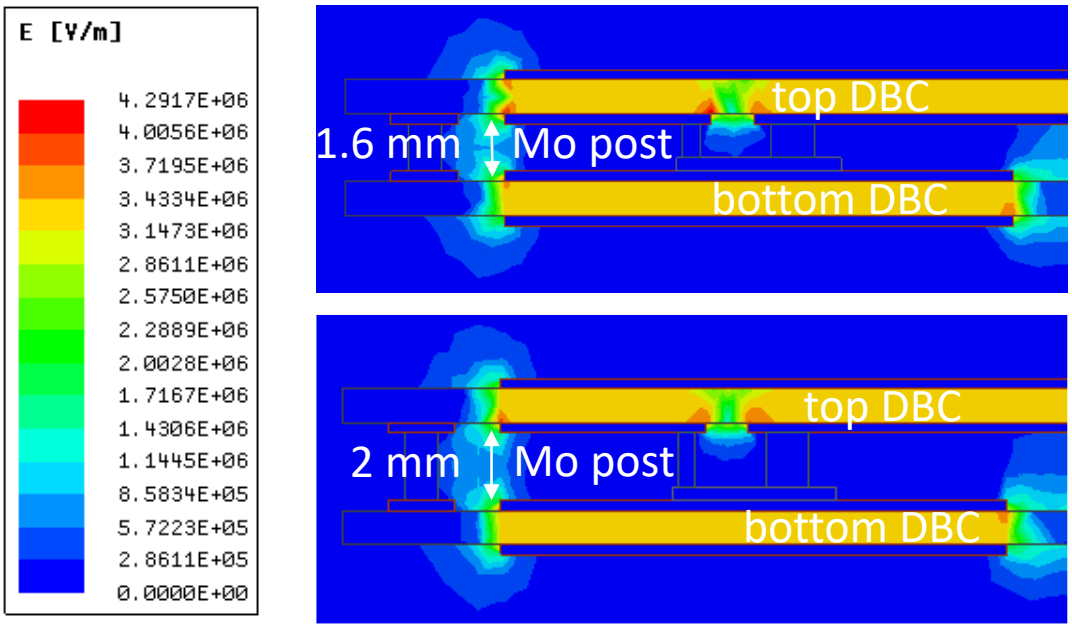


Fig. 6. 12 Electric field simulation results for (a) 1.6-mm-tall and (b) 2-mm-tall Mo post.

In conclusion, single 1-mm-thick AlN DBC substrate and two 0.635-mm-thick stacked AlN DBC substrates, with two separated Cu pads aligning with the top Cu pads, are optimal designs for DBC substrate in the proposed power module structure. The distance between edges of Cu pad with positive potential and ceramics, as well as the metal post height, have impact on the electric field distribution and the maximum electric field strength at triple points in the power module too.

6.2.3 Thermo-mechanical Stress Analysis

In the proposed wire-bondless module, the SiC bare dies are sandwiched between two DBC substrates, and Mo posts are placed on SiC top pads to replace bonding wires for interconnection. The thermo-mechanical stresses caused by the CTE mismatch of contacting materials would be more severe. Several factors will affect the thermos-mechanical stress distribution and values,

including metal post size and DBC design. The detailed simulation results and discussion are presented in this section.

First of all, the size of the post that is to be attached on top pads of the MOSFET is determined by the pad size, as shown in Fig. 6.13. The source post should be made as large as possible within the bounds of the original pads to achieve high current, low parasitic inductance, and good mechanical stability, while keeping a sufficient distance from the gate pad in case of shorting. On the other hand, the gate pad has a relatively small size of 0.5 mm x 0.8 mm, hence two possible posts can be designed for the attachment on gad pad. First is to use a post of the same or smaller size of gate pad, in this case, the gate pad needs to be re-metallized for metal post attachment, but there is high requirement on the accuracy when attaching the post due to the small gap between gate and source pads (0.05 mm). The second method is to enlarge the gate pad by depositing a layer of insulation material around the gate pad, and then metal deposition, by doing so, a post of bigger size than gate pad can be attached.

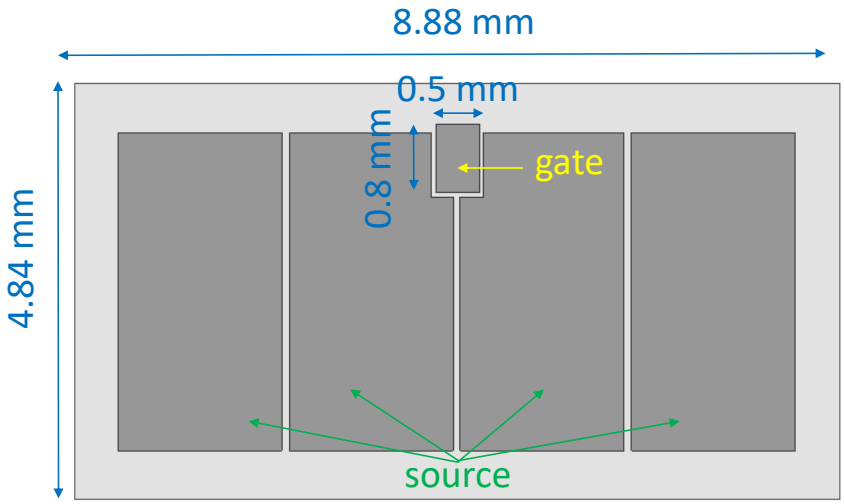
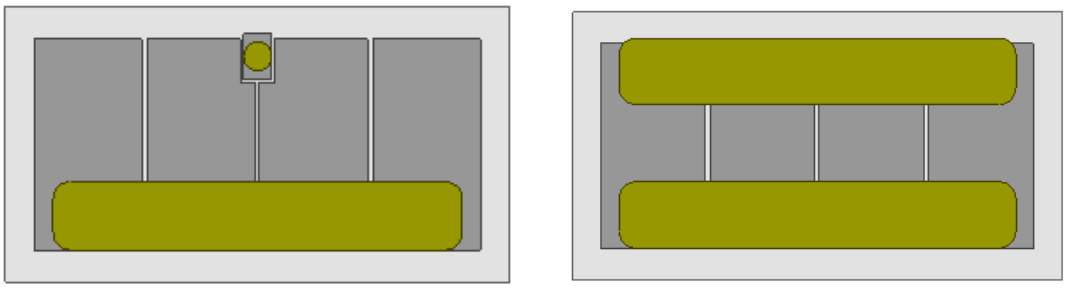


Fig. 6. 13 Top view of the 3.3kV MOSFET bare die.

The thermos-mechanical simulations were performed using ANSYS workbench for different post designs shown in Fig. 6.14. In Fig. 6.14 (a), the gate post has the diameter of 0.5 mm, and the source post size is 1.2 mm x 7.2 mm. In Fig. 6.14 (b), the gate post is enlarged and the gate post size is the same as source post. The proposed module design as shown earlier in Fig. 6.2 was used as simulation model, the power dissipation of each MOSFET is set to be 200 W, the heat transfer coefficient on DBCs at both sides of the module is defined to be 5000 W/(m^2K), and the ambient temperature is assumed to be room temperature 25 ℃. The simulation results are listed in Table 6.2 and shown in Fig. 6.15 and Fig. 6.16. As can be seen, the big gate post can help improve the heat dissipation from the bare dies and reduce the device temperature, the overall module stress and the thermo-mechanical stress on devices are also lower, and so is the maximum deformation. The maximum thermos-mechanical stress in the module is located at the die attached Cu pad of bottom DBC as shown in Fig. 6.16 (c), while the maximum deformation is at the top DBC Cu trace.

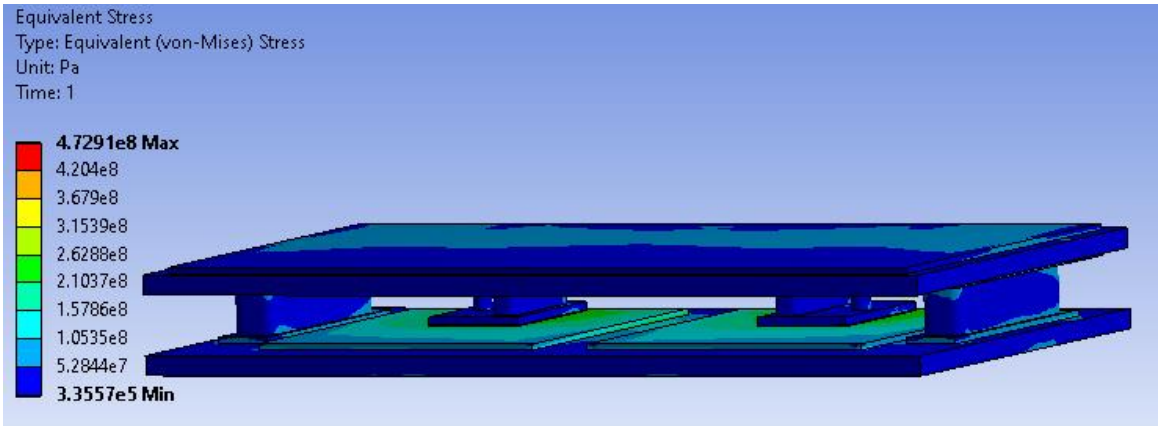


(a) (b)

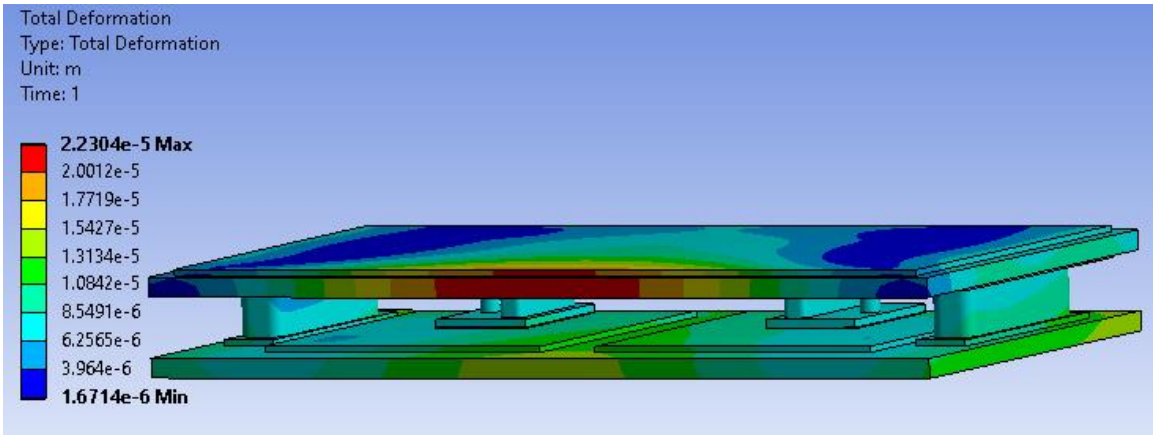
Fig. 6. 14 MOSFET bare die with (a) small gate post attached on original pate pad, and (b) big gate post attached on enlarged gate pad.

Table 6. 2 Thermo-mechanical simulation results for different gate post design

Model	maximum device temperature (°C)	maximum Von-Mises stress in module (MPa)	maximum Von-Mises stress on device (MPa)	maximum deformation (μm)
Small gate post	168.4	472.9	273.1	22.3
Big gate post	152.5	430.3	205.3	20.3

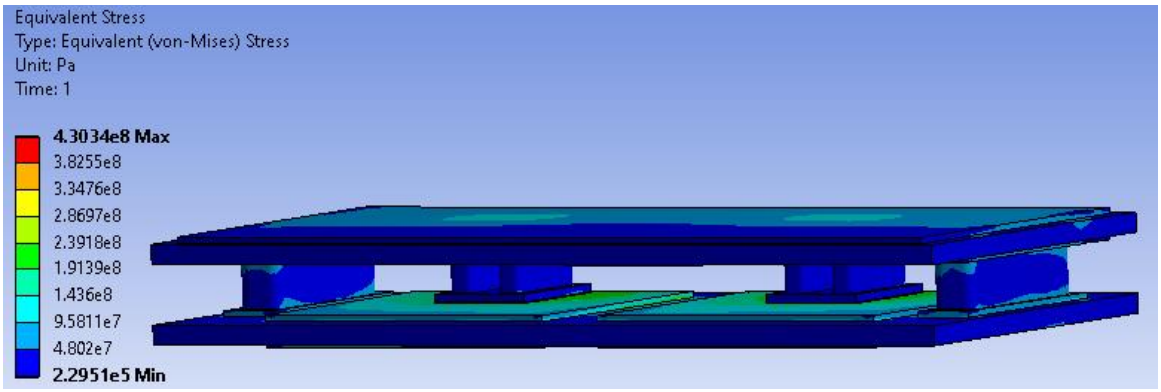


(a)

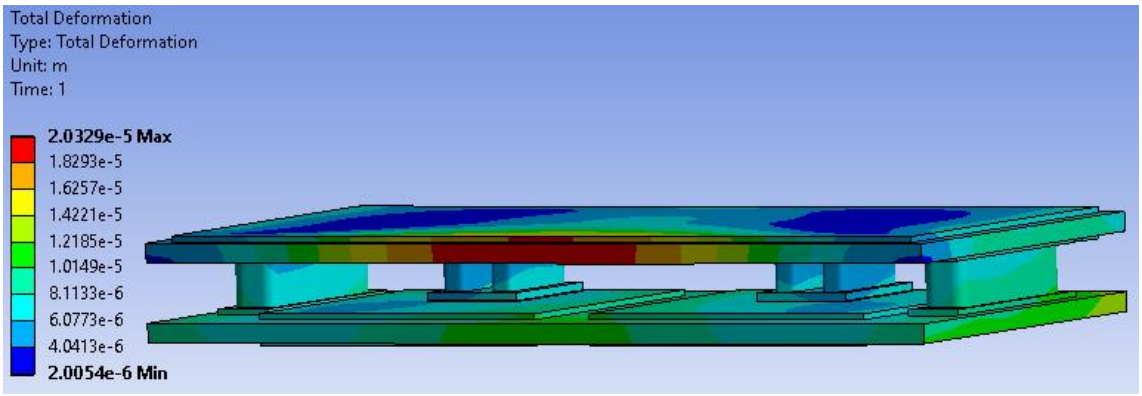


(b)

Fig.6. 15 (a) Von-Mises stress distribution, and (b) deformation of the proposed double-sided wire-bondless module with small gate post attached.

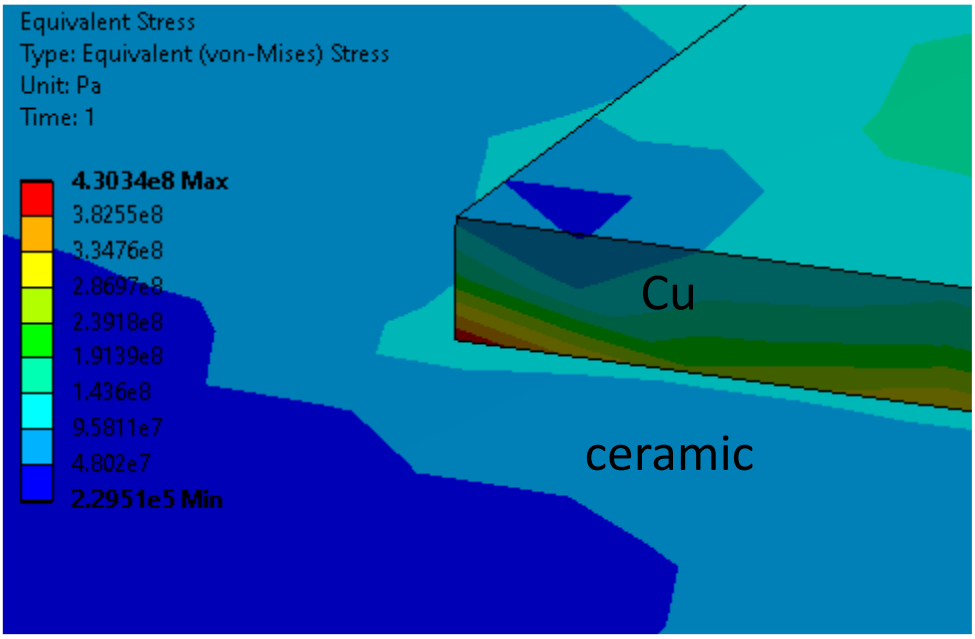


(a)



(b)

Fig.6. 16 (a) Von-Mises stress distribution, (b) deformation, and (c) maximum Von-Mises stress location of the proposed double-sided wire-bondless module with big gate post attached.



(c)

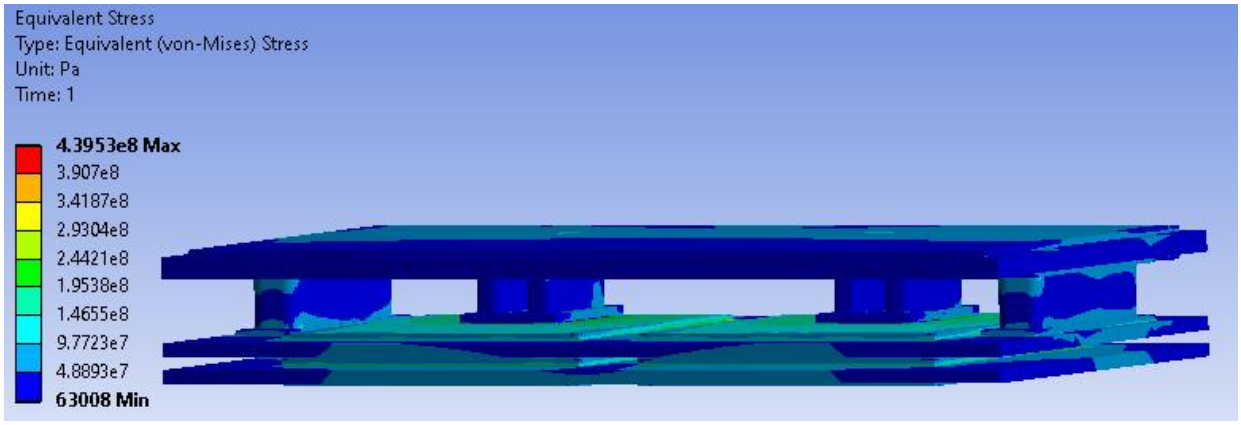
Fig.6. 16 Cont. (a) Von-Mises stress distribution, (b) deformation, and (c) maximum Von-Mises stress location of the proposed double-sided wire-bondless module with big gate post attached.

In the last section, both single 1-mm-thick AlN DBC substrate and two 0.635-mm-thick stacked AlN DBC substrates are selected to be optimal designs for bottom DBC substrate in the proposed power module structure from the aspect of electric field reduction. To help select the best substrate design, the thermos-mechanical stress simulations were performed for these two case, and the results are listed in Table 6.3. Fig. 6.16 shows the simulation results when single DBC is used in the proposed module, which Fig. 6.17 shows the simulation results for stacked DBC. As shown in Table 6.3, the power module with stacked DBC substrates has slightly lower device temperature,

but the maximum stress and deformation is higher, especially the thermos-mechanical stress on devices, as shown in Fig. 6.17 (c).

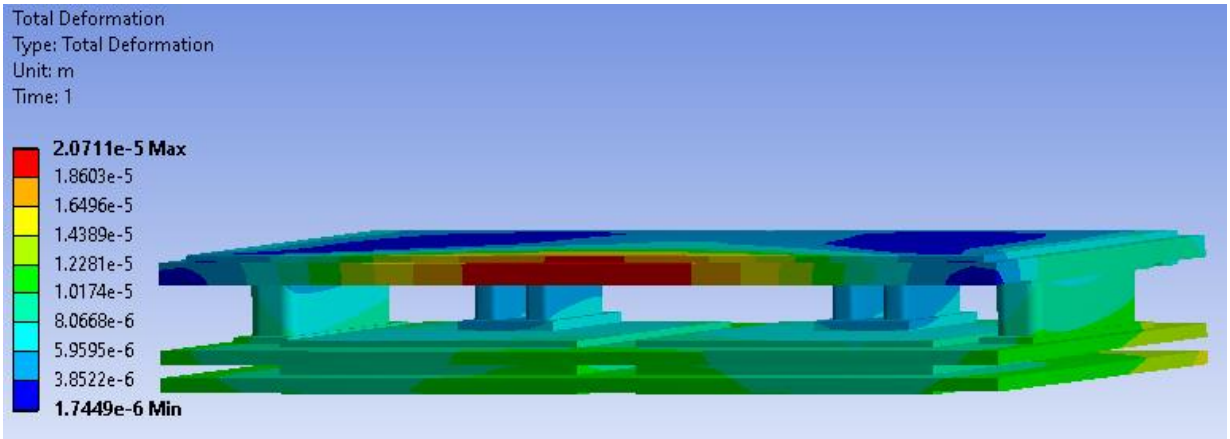
Table 6. 3 Thermo-mechanical simulation results for different bottom DBC substrate design

Model	maximum device temperature (°C)	maximum Von-Mises stress in module (MPa)	maximum Von-Mises stress on device (MPa)	maximum deformation (μm)
single DBC	152.5	430.3	205.3	20.3
Stacked DBC	149.4	439.5	267.7	20.7

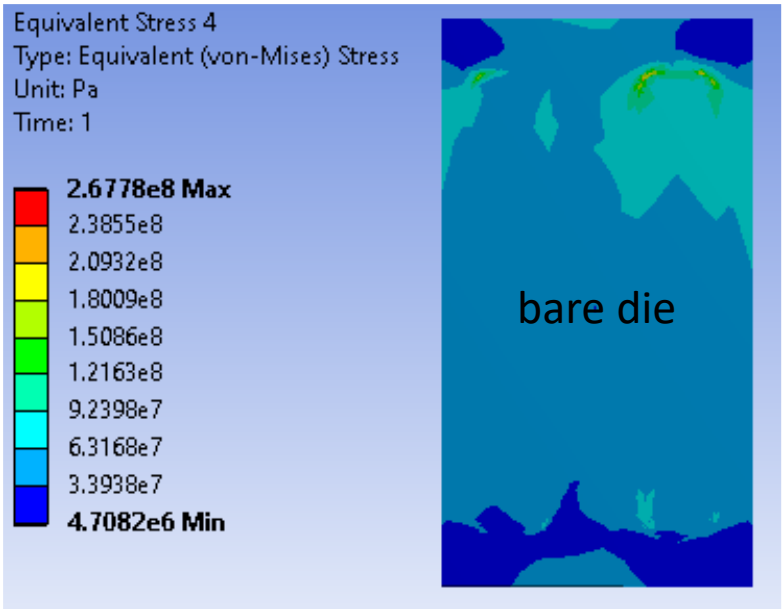


(a)

Fig.6. 17 (a) Von-Mises stress distribution, (b) deformation, and (c) maximum Von-Mises stress on device of the proposed double-sided wire-bondless module with two stacked DBC substrates.



(b)



(c)

Fig.6. 17 Cont. (a) Von-Mises stress distribution, (b) deformation, and (c) maximum Von-Mises stress on device of the proposed double-sided wire-bondless module with two stacked DBC substrates.

In Fig. 6.11, d_1 is defined as the distance between the ceramic edge and the edge of Cu trace for Mo post standoff to be attached, while d_2 is defined as the distance between the Cu traces for Mo post standoff and for device to be attached, respectively. Different Cu layout designs with different d_1 and d_2 values influent the electric field distribution, thermo-mechanical simulation were also performed for different layout designs, and the results are listed in Table 6.4. The maximum device temperature doesn't change much with d_1 and d_2. Increasing d_2 will increase the deformation, while increasing d_1 help reduce the overall thermo-mechanical stress in the module. When both d_1 and d_2 are 2 mm, the maximum stress on devices is the lowest.

Table 6. 4 Thermo-mechanical simulation results for different Cu layout designs

d_1 (mm)	d_2 (mm)	maximum device temperature (℃)	maximum Von-Mises stress in module (MPa)	maximum Von-Mises stress on device (MPa)	maximum deformation (μm)
1	1	159.3	443.9	191.8	21.9
1	2	159.2	456.2	182.3	23.3
2	1	158.0	356.3	231.5	21.7
2	2	158.1	365.9	157.5	23.1

Summarizing both the electric field and thermos-mechanical simulations, for the proposed double-sided wire-bondless power module, single 1-mm-thick AlN DBC is selected as bottom DBC substrate due to the lower electric field strength and lower thermal stress on devices, distance between ceramic edge and Cu pad, as well as distance between Cu pads are set to be 2 mm because of the relatively low peak electric field strength and low thermos-mechanical stress on bare dies. Mo post height is chosen to be 2mm, and big gate post on enlarged gate pad will be used within the module.

6.3 Module Fabrication Process

The fabrication process of the double-sided wire-bondless module is shown in Fig. 6.18. The 3.3-kV MOSFET bare dies were re-metallized, including enlarging gate pad. Metal posts were then attached on the top pads of the bare dies using nano-silver (Ag) sintering process, which was also used for die attachment because of the advantage of low voiding, high thermal and electrical conductivity, and less liquidity compared to solder [12]. Two-step encapsulation was used including polyimide (PI) and silicone to improve the blocking voltage capability. The detailed fabrication process will be discussed in the following sections.

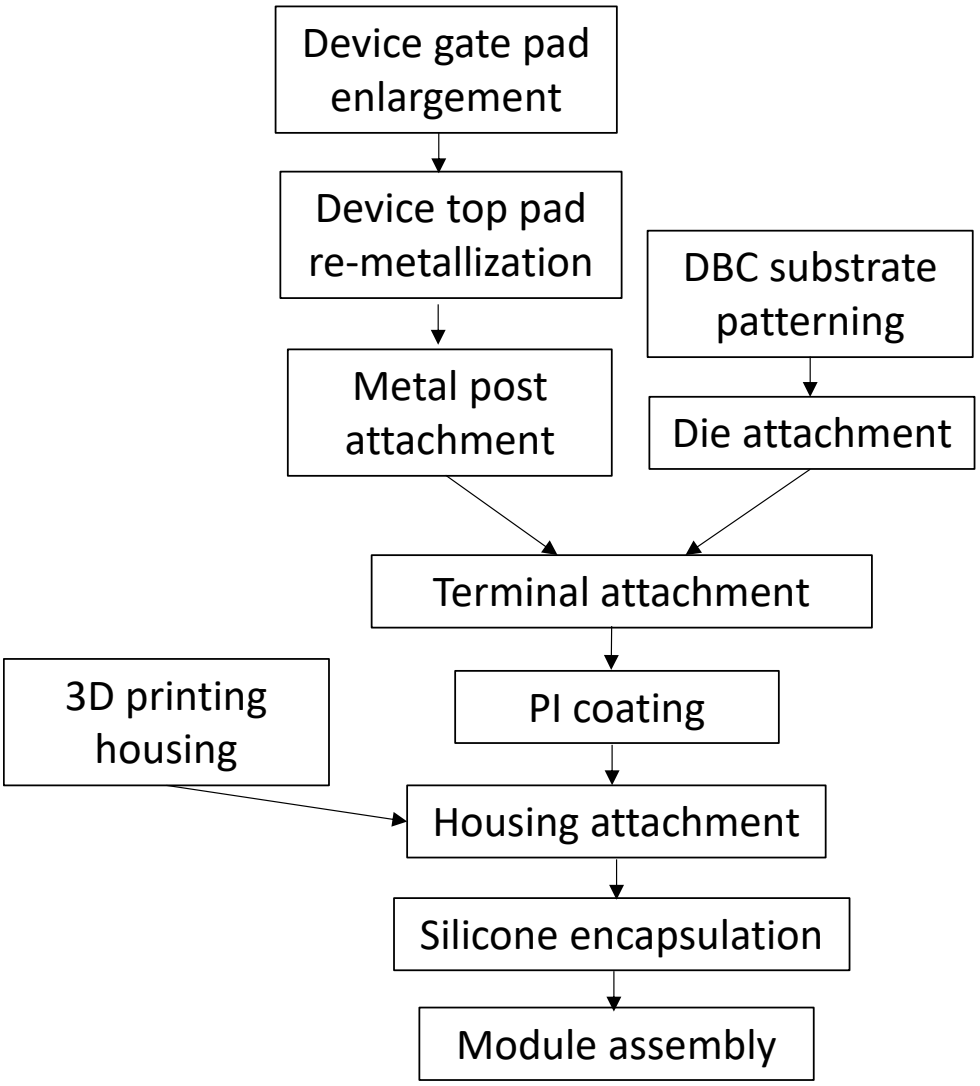


Fig.6. 18 Fabrication process for the proposed 3.3-kV double-sided wire-bondless power module.

6.3.1 SiC Die Top Pads Metallization

The first step to process the top pads of the 3.3-kV SiC MOSFET bare die is to enlarge its gate pad. As shown in Fig. 6.19, a 300 nm thick silicon dioxide (SiO_2) layer was sputtered around the gate pad, since the gate-source voltage of the device is less than 25 V, 300-nm-thick SiO_2 is enough for insulation. Next, 100-nm-thick titanium (Ti), 200-nm-thick nickel (Ni), and 700-nm-thick silver (Ag) were deposited in order using an E-beam evaporator onto the gate pad and the SiO_2

covered area, as such, the gate pad were enlarged from 0.5 mm x 0.8 mm to be the Ti-Ni-Ag covered area of 1.45 mm x 7.5mm.

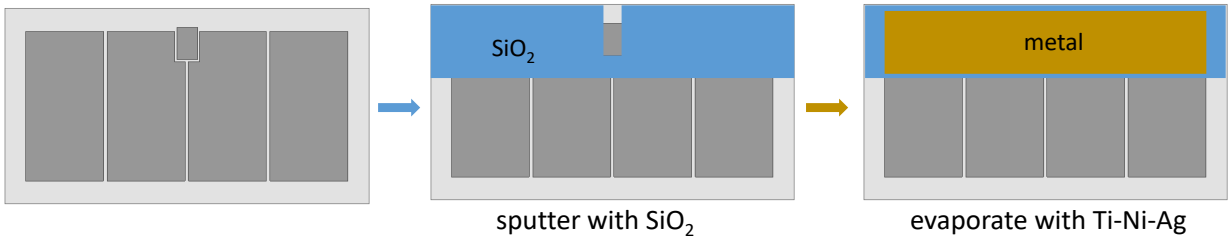


Fig.6. 19 Device gate pad enlargement process.

A fixture as shown in Fig. 6.20 was used as chip carrier for the sputtering and E-beam evaporation. The mask for SiO_2 deposition covered the gate pad and partial source pads, the other mask for Ti-Ni-Ag deposition was used to re-metalize the enlarged gate and source pads for Ag sintering. The Ti layer was deposited first as an adhesion layer on the aluminum (Al) pads, Ni acted as a solder diffusion barrier, and the Ag was deposited at last to improve the bonding strength for sintering.

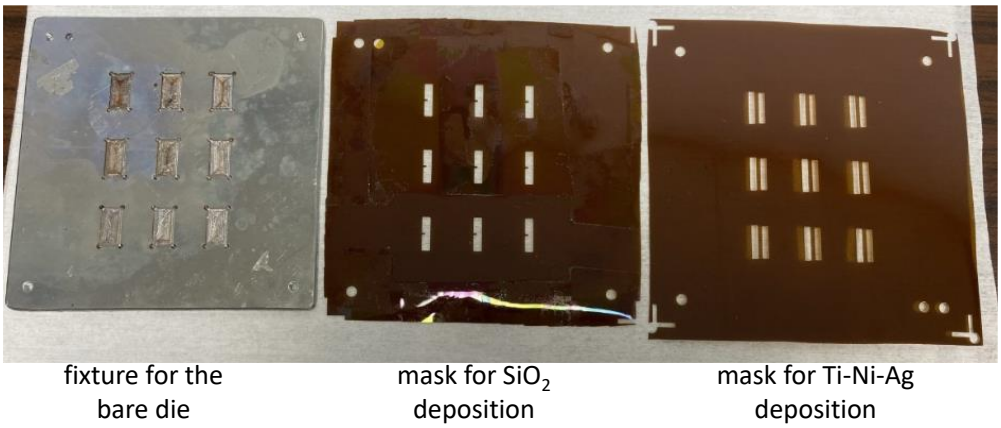


Fig.6. 20 Fixture and masks for device top pads metallization.

Fig. 6.21 shows the devices with SiO_2 layer deposited. Fig. 6.22 shows the E-beam evaporator and the crucibles containing metals for device re-metallization.

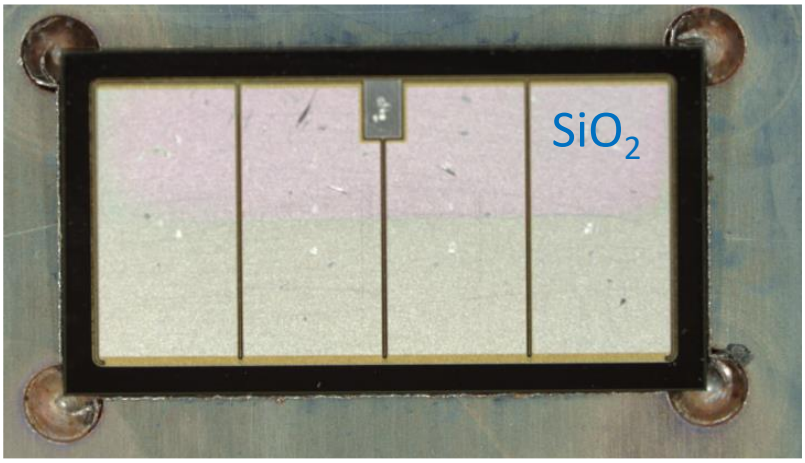
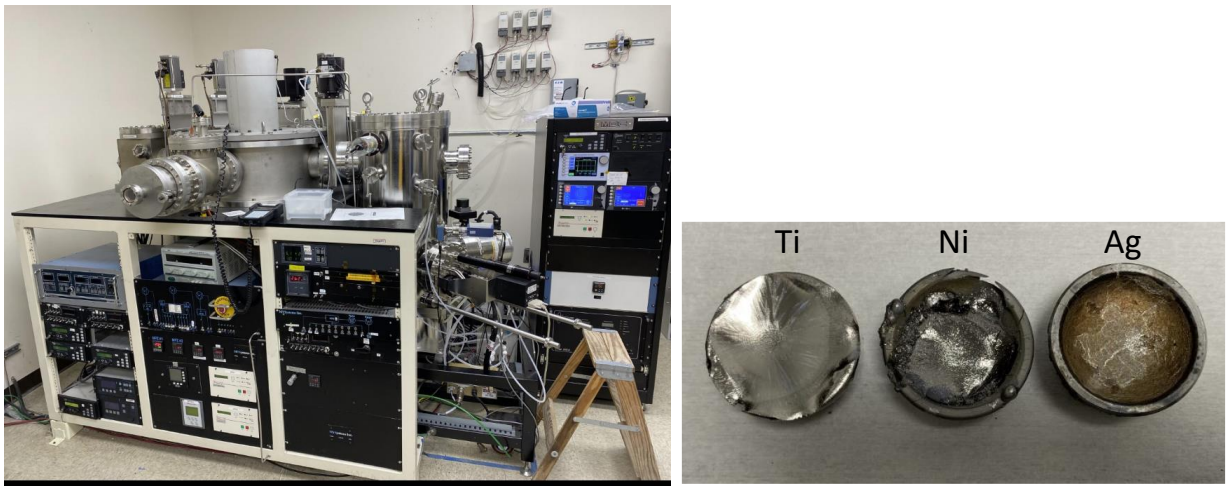


Fig.6. 21 3.3-kV MOSFET bare die with SiO_2 layer deposited.

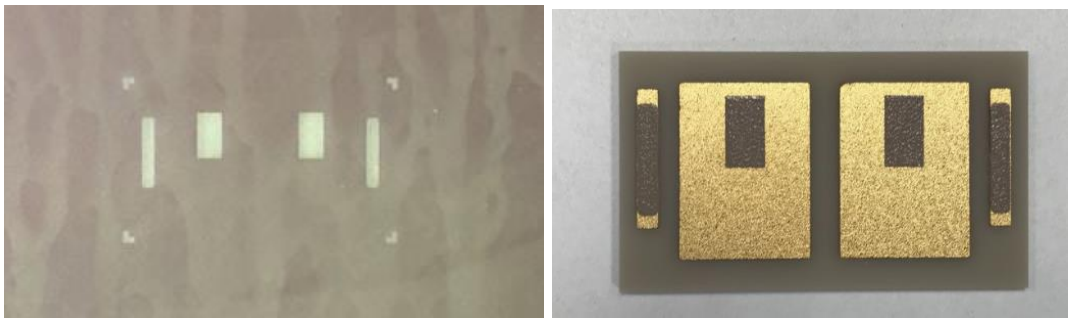


(a) (b)

Fig.6. 22 (a) E-beam evaporator, and (b) crucibles carrying metals for E-beam evaporation.

6.3.2 Die and Post Attachment

Pressure-less sintering was used to attach the metal posts to bare dies and DBC substrate, as well as to attach dies to DBC substrate. A screen printing mask as shown in Fig. 6.23 (a) was used to print the nano-silver sintering paste onto the DBC, as shown in Fig. 6.23 (b). A fixture was used to hold the dies in position during sintering process, as shown in Fig. 6.23 (c), and the DBC substrate after die and post silver sintering attachment and power terminal soldering attachment is shown in Fig. 6.23 (d).



(a) (b)

(c) (d)

Fig.6. 23 (a) Screen printing mask, (b) DBC substrate with nano-Ag sintering paste printed on, (c) fixture for die attachment, and (d) dies, posts, and terminals attached DBC substrates.

Kyocera's pressure-less silver sintering paste was used for post and die attachment, the paste has thermal conductivity higher than 200 W/(m*K), good interface reliability and low-temperature sintering capability [13]. The silver sintering paste was cured in air at 200 ℃ for 90 minutes. The scanning acoustic microscope (SAM) examination image of the sintered die attachment layer shows low voiding and uniform thickness, as shown in Fig. 6.24.

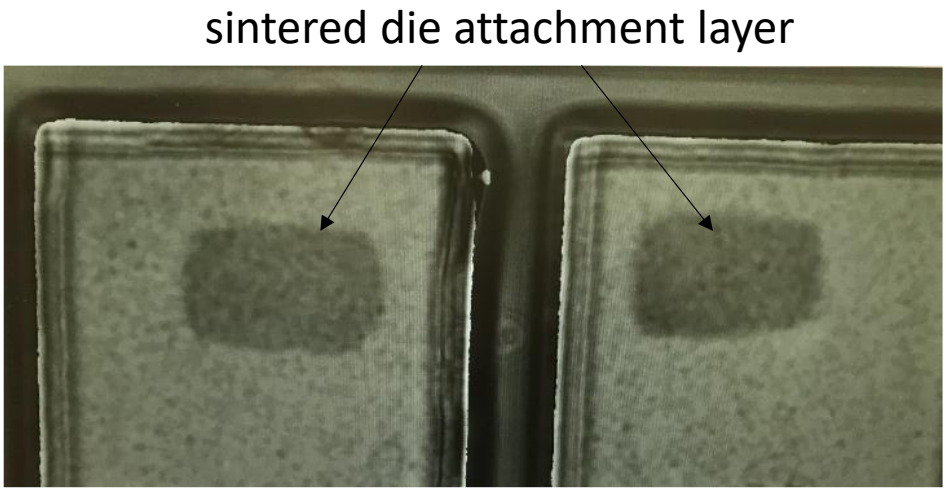


Fig.6. 24 SAM examination image of the sintered die attachment layer.

6.3.3 Two-step Encapsulation

A two-step encapsulation is proposed for the high voltage wire-bondless module. A high-voltage passivation material, polyimide (PI) from HD MicroSystems with a dielectric breakdown strength higher than 200 kV/mm [14], was first spin coated onto the die and post attached DBC substrate, as shown in Fig. 6.25. The PI was spin coated at 2000 rpm for 30 seconds, then soft baked at 130 ℃ on a hot plate for 90 seconds. The coated DBC substrate was heated at 200 ℃ for 40 minutes to fully cure the PI.

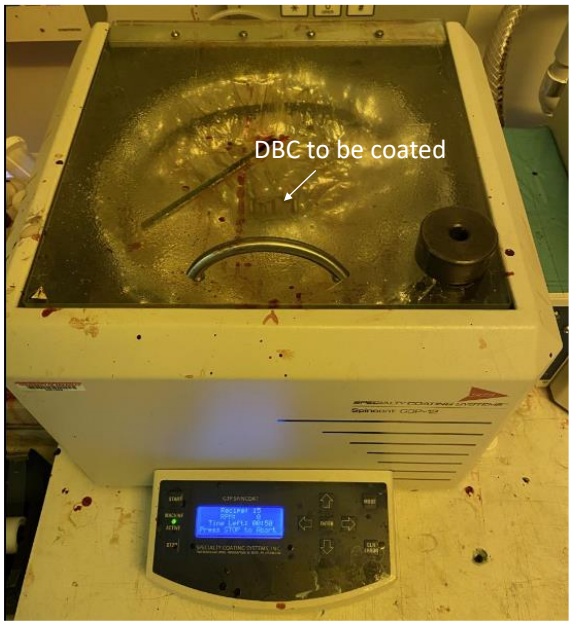


Fig.6. 25 PI coating on die attached DBC substrate using a spin coater.

High temperature resin which can stand up to 289 ℃ from Formlabs was used to 3-D print the designed housing, as shown in Fig. 6.26. The bottom housing was attached with the DBC substrate, silicone elastomer was then used as the second step to encapsulate the PI coated substrate.

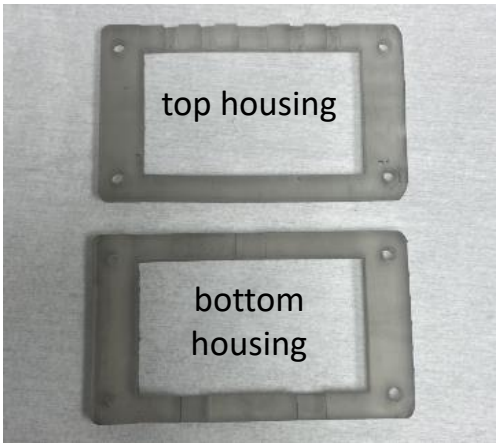


Fig.6. 26 3-D printed high temperature housing.

6.3.4 Module Assembly

The top DBC substrate was attached to the metal posts using SAC305 solder paste. Solder paste was selected because it can create a thicker bondline to accommodate the height difference of posts [8]. The SAC305 solder paste was printed onto the metal posts, and the top DBC was flipped and attached onto the posts using a set of fixtures shown in Fig. 6.27 for alignment with the bottom DBC. The assembly was put into reflow oven to form the bonding, the assembled module is shown in Fig. 6.28.

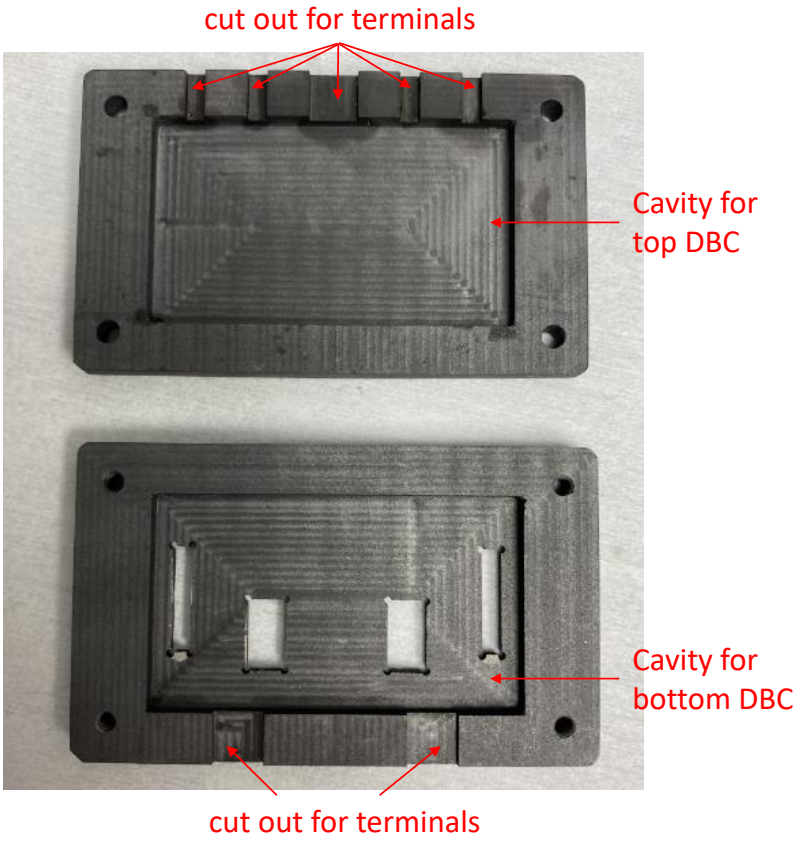


Fig.6. 27 Fixtures for module assembly.

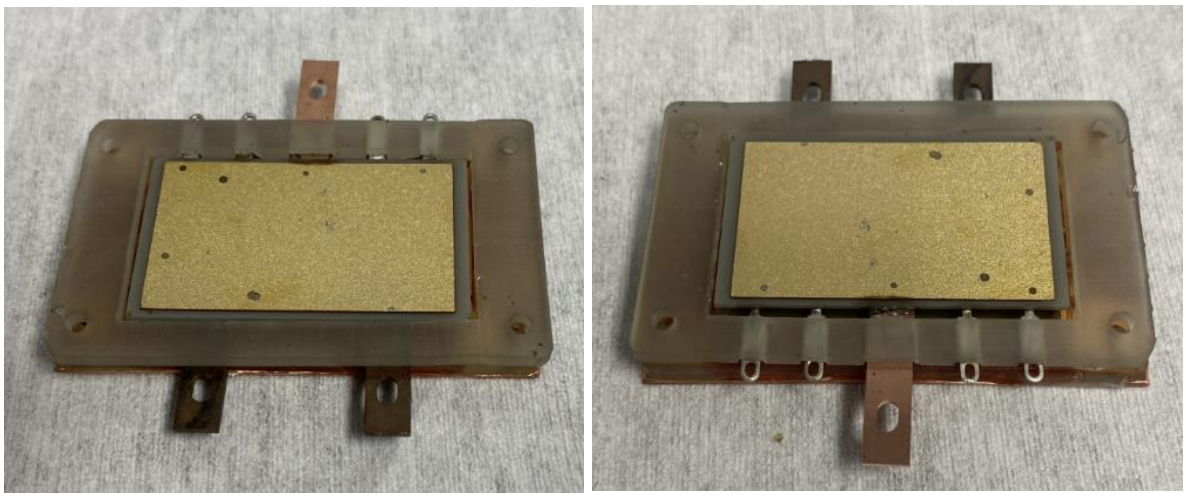


Fig.6. 28 Fabricated 3.3-kV double-sided wire-bondless power module.

6.4 Wire-bonding Module Fabrication

To compare the switching performances of the wire-bondless module to those of a wire-bonding counterpart, a wire-bonded module was fabricated using the same 3.3-kV MOSFETs, as shown in Fig. 6.29.

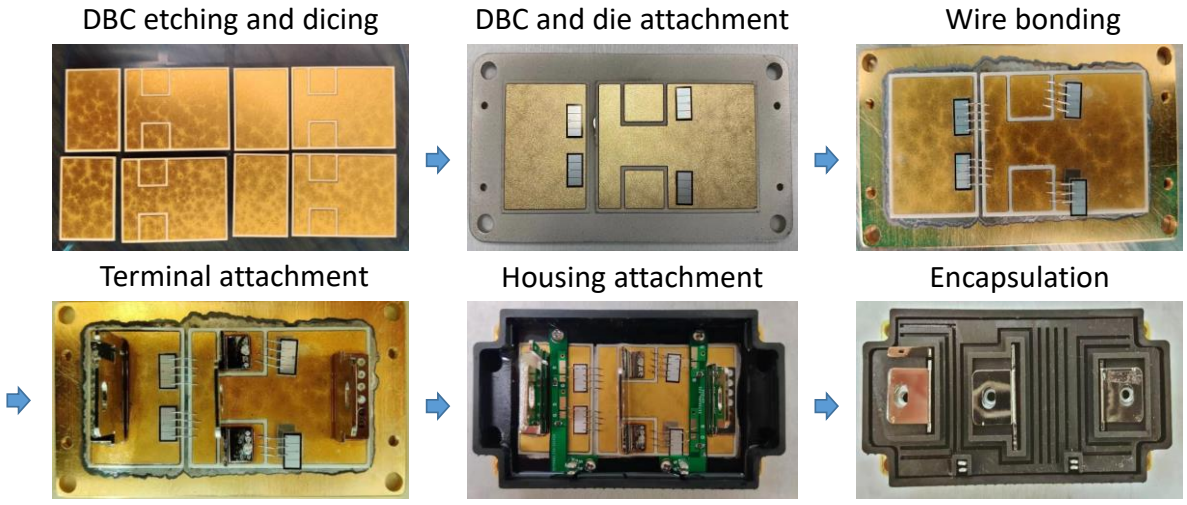


Fig.6. 29 Fabrication process of a 3.3-kV wire-bonding power module.

6.5 Module Testing

After fabrication of the 3.3-kV double-sided wire-bondless module, experimental tests were conducted to evaluate the performance, the detailed tests and results are presented in this section.

6.5.1 Leakage Current Test

Gate-source and drain-source leakage currents of both MOSFETs were measured with a source measure unit (SMU) to verify the electrical connection and to investigate the package influence. The measurement results of gate-source leakage current (I_{gss}) are shown in Fig. 6.30 together with the results of bare dies before fabrication. One die has increased I_{gss} of 13 nA when V_{gs} is 20 V, but is still much less than the maximum value (0.5 μA) as provided in the device datasheet. Fig. 6.31 shows the drain-source leakage current (I_{dss}) measurement results, ignoring the noise peak from the equipment at the beginning, the I_{dss} keeps at low value up to 1 kV.

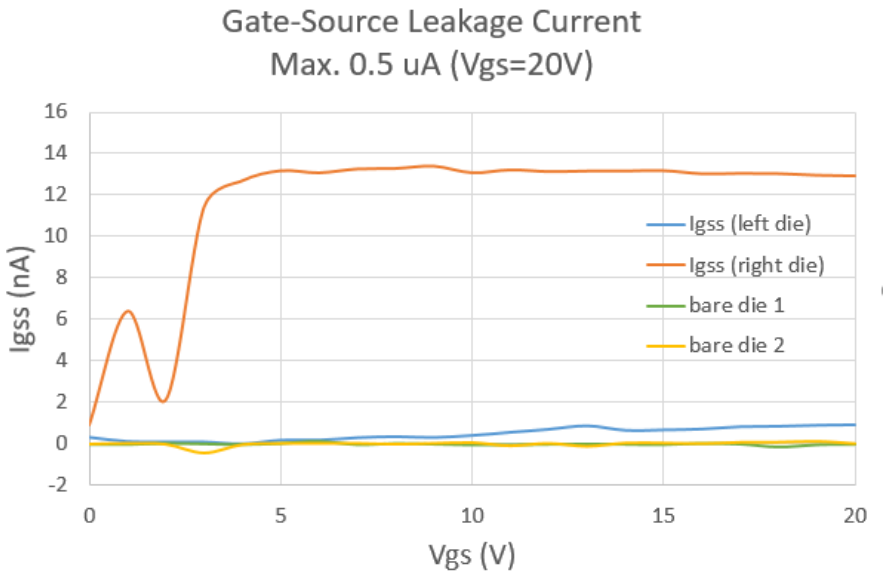


Fig.6. 30 Measured gate-source leakage currents of the fabricated 3.3-kV power module.

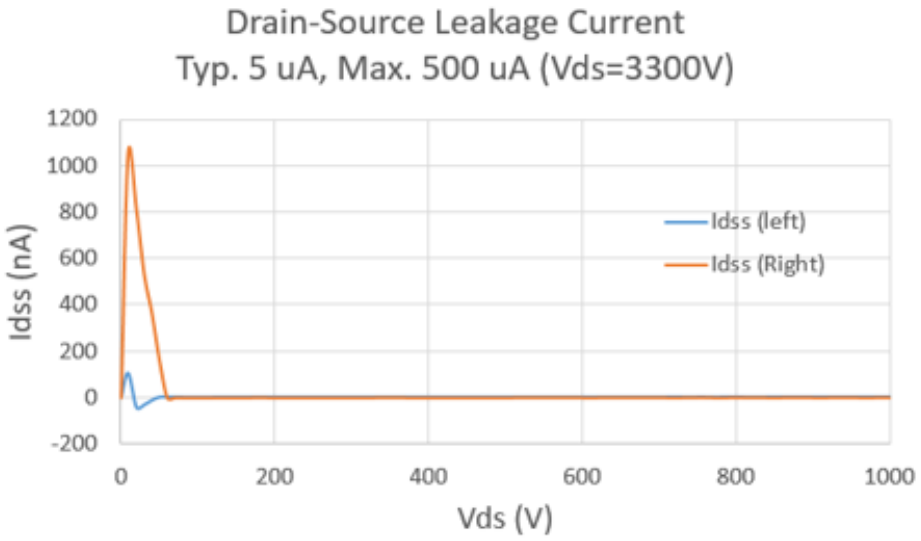


Fig.6. 31 Measured drain-source leakage currents of the fabricated 3.3-kV power module.

6.5.2 High Voltage Dielectric Test

High voltage dielectric test was conducted to verify the packaging capability for high voltage operation. The test setup is shown in Fig. 6.32. High voltage was applied to the DC+ and common source terminals of the power module when V_{gs} is 0, the current through the module was recorded, and the test results are shown in Table 6.5. As can be seen, the current keeps low until 3 kV, when the current increased to 3.14 μA. This is because avalanche happens when the drain-source voltage approaching the maximum blocking voltage of the MOSFET. Considering the maximum value of I_{dss} is 500 μA at 3.3 kV according to the datasheet, the fabricated power module is supposed to be operate normally within the blocking voltage.

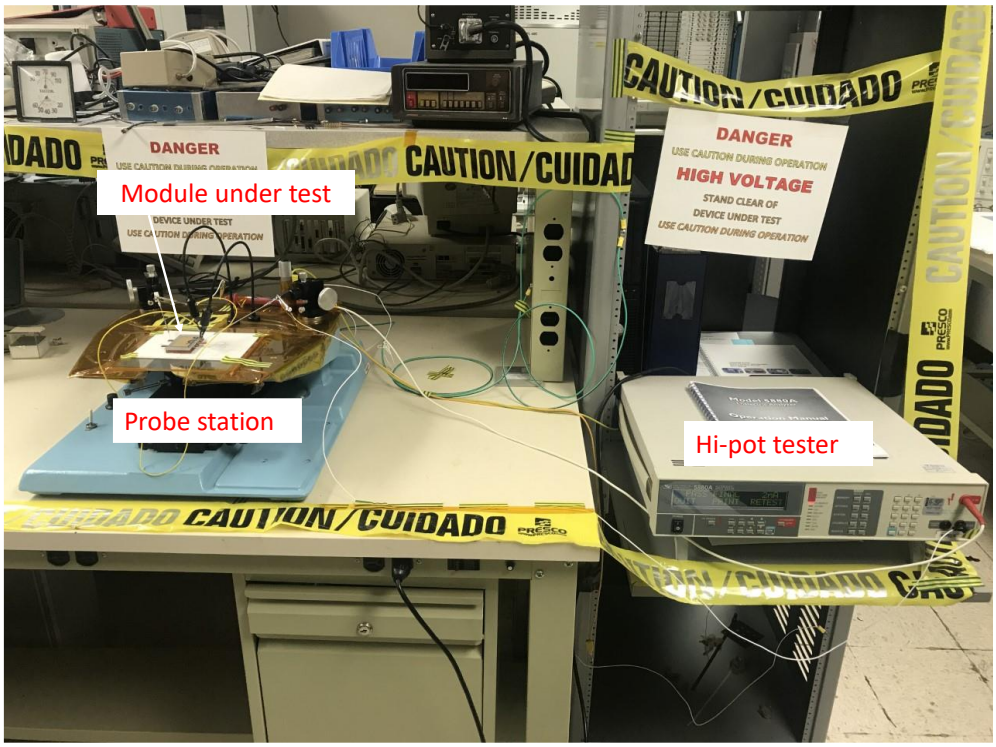


Fig.6. 32 High voltage dielectric test setup for the fabricated 3.3-kV wire-bondless module.

Table 6. 5 DC voltage dielectric test results for the fabricated module

DC V_{ds} (V_{gs}=0 V)	Current
100 V	2 nA
500 V	2 nA
1000 V	2 nA
1500 V	2 nA
2000 V	2 nA
2500 V	2 nA
3000 V	3.14 μA

To evaluate the high voltage blocking capability of two-step encapsulation, samples with different encapsulation method were prepared and tested. DBC substrates with only silicone encapsulated,

one layer of PI coated then silicone encapsulated, and two layers of PI coated then silicone encapsulated were prepared, as shown in Fig. 6.33. One layer of PI was measured to be 11 μm ~ 13 μm thick, the thickness of two layers of PI is 17 μm ~ 20 μm, and the silicone thickness is about 1 mm. The high voltage was applied to the standoff soldered on the top Cu pad of DBC substrate, while the Cu at bottom of DBC substrate was grounded. The voltage increased at the rate of 100 V/s until the breakdown happened in the sample through ceramic or between metal pads. The breakdown voltage (BDV) test results for both DC and AC voltages are listed in Table 6.6. As can be seen from the table, the addition of PI can help improve the breakdown voltage of the DBC substrate.

DBC substrates with silicone encapsulated but different top Cu layout designs were also tested the breakdown strength, and the BDV measurement results are shown in Table 6.7.

However, how the two-step encapsulation or DBC layout design affect the partial discharge inception voltage (PDIV) can't be demonstrated by the breakdown test, because partial discharge can occur when there is μm size cavity in solid insulation material [15]. Further tests to measure the PDIV of different DBC substrate samples needs to be conducted in the future.

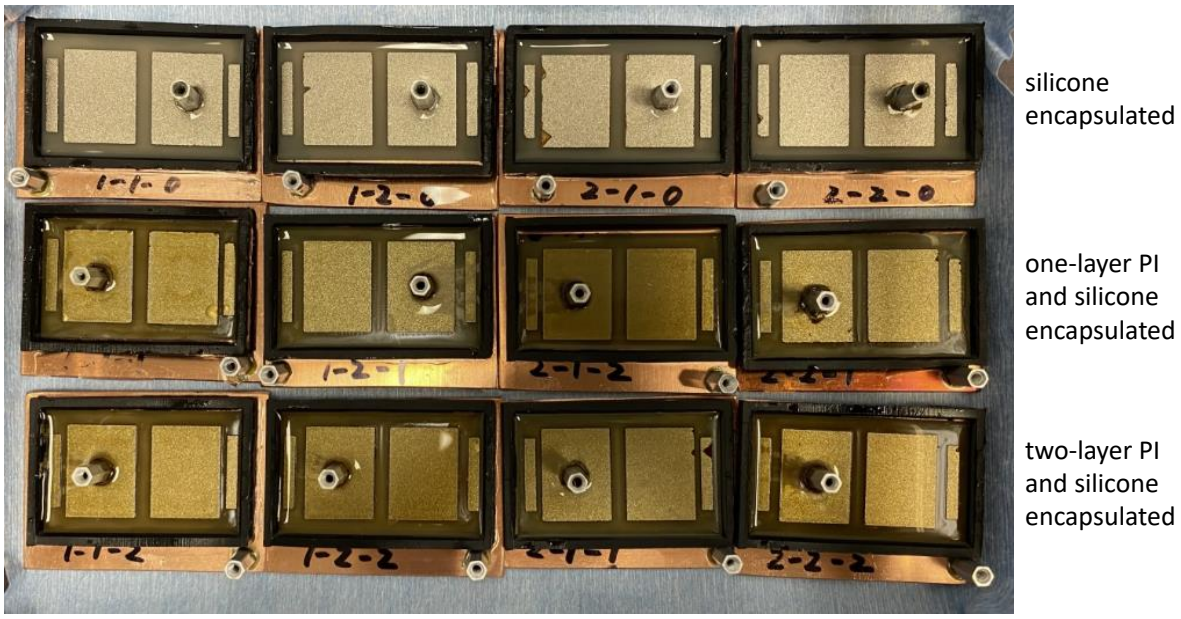


Fig.6. 33 Samples with different encapsulant for high voltage breakdown test.

Table 6. 6 High voltage breakdown test results for samples with different encapsulant

sample	DC breakdown voltage (V)	50 Hz AC breakdown voltage (V)
silicone	6256	3928
one-layer PI and silicone	7000	4065
two-layer PI and silicone	> 7000	4138

Table 6. 7 High voltage breakdown test results for samples with different Cu layout design

d_1 (mm)	d_2 (mm)	DC breakdown voltage (V)	50 Hz AC breakdown voltage (V)
1	1	6388	4082
1	2	6507	4386
2	1	6434	4309
2	2	6517	4676

6.5.3 Switching Test

Double-pulse test is performed to characterize the switching performance of the fabricated power module. The double-pulse test setup is shown in Fig. 6.34. 24 V was provided to the gate driver board by power supply, and double pulse signal was provided by the function generator to the gate of MOSFET under test through the gate driver. Drain-source voltage applied on the MOSFET was provided by the high voltage source. The switching waveforms of gate-source voltage (V_{gs}), drain-source voltage (V_{ds}) and drain current (I_d) of the two MOSFETs were captured using an oscilloscope, which are shown in Fig. 6.35. Both MOSFETs can switch properly. The switching waveforms of the wire-bonding module are shown in Fig. 6. 36.

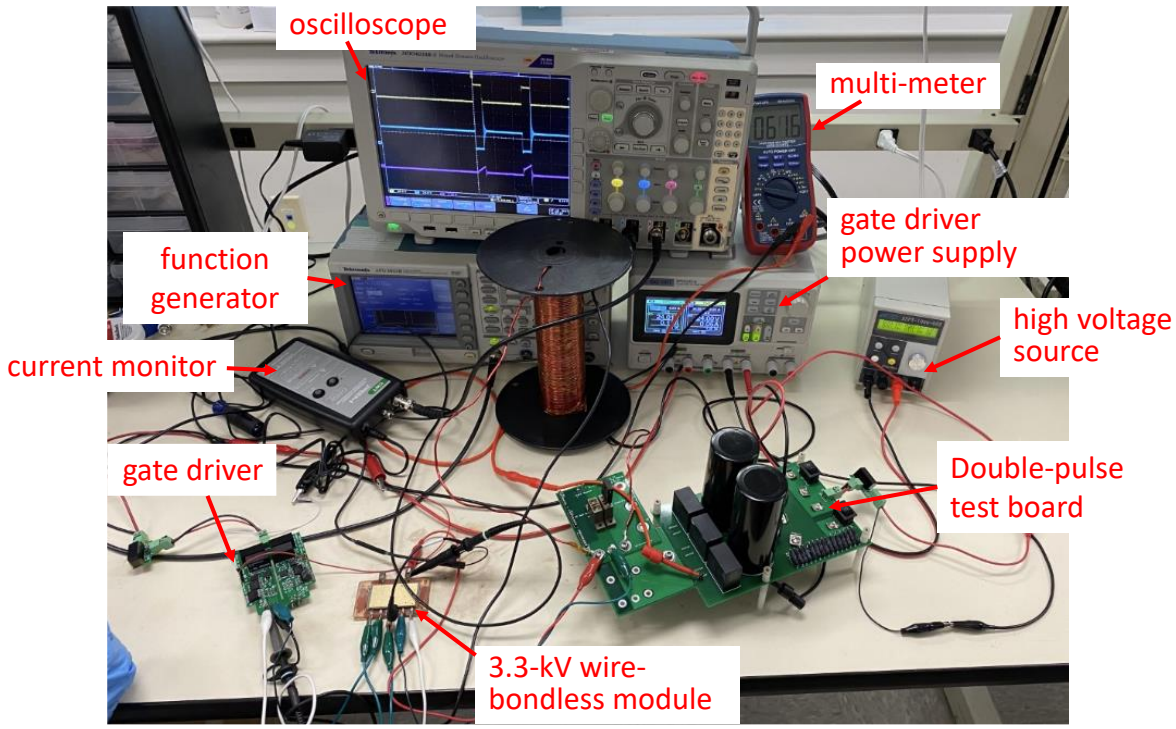


Fig.6. 34 Double-pulse test setup for the fabricated 3.3-kV wire-bondless module.

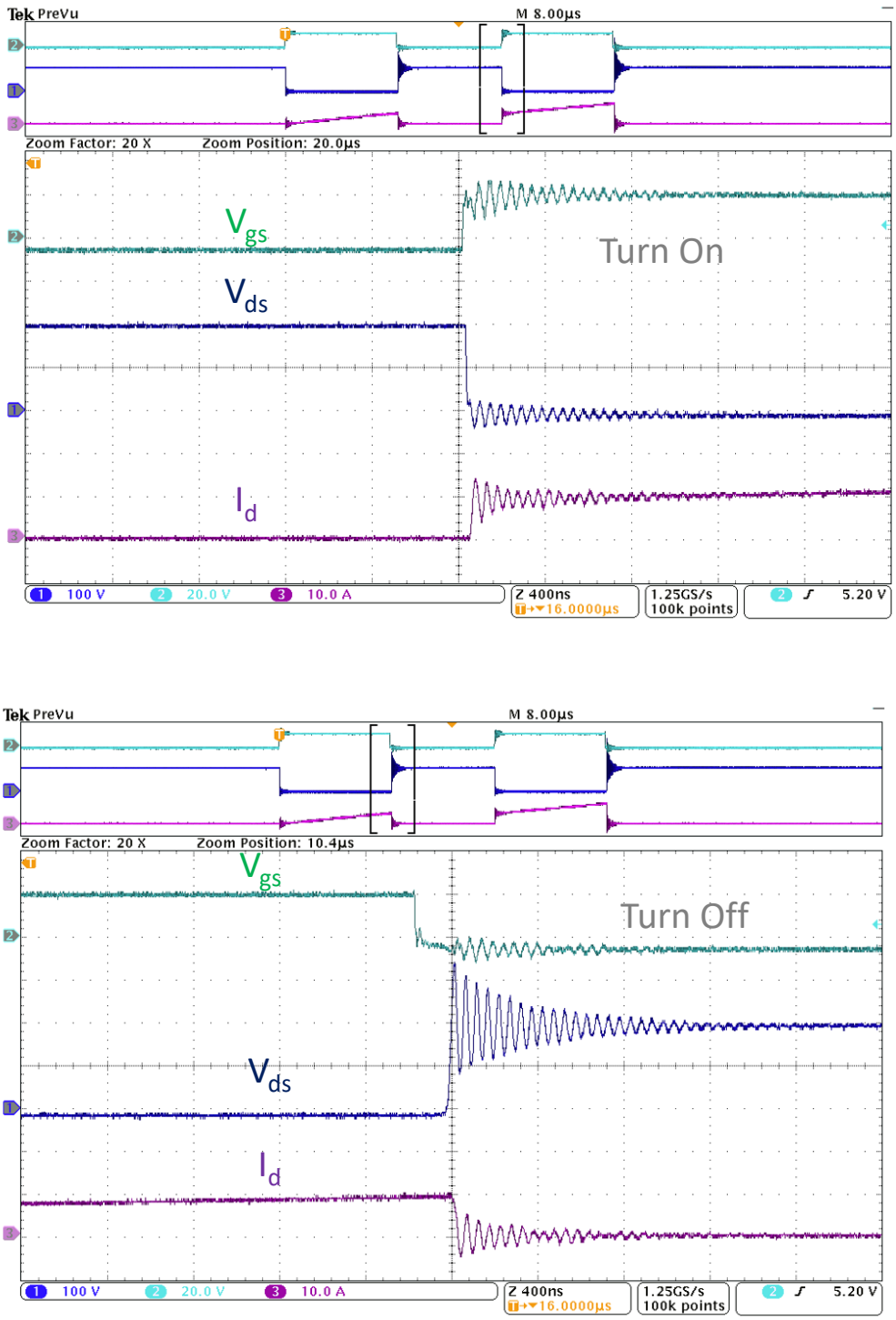


Fig.6. 35 Double-pulse test results for the fabricated 3.3-kV wire-bondless module.

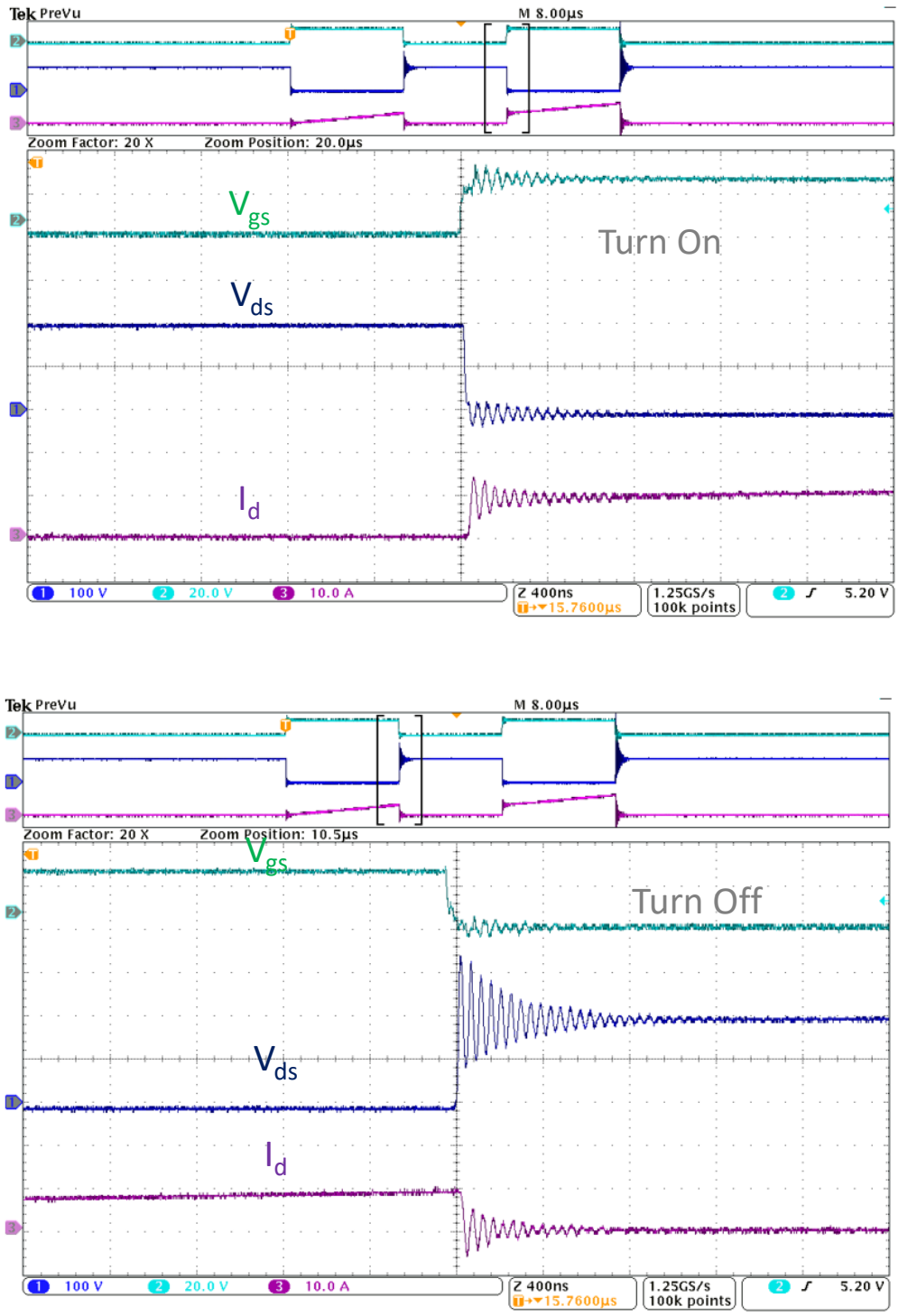


Fig.6. 36 Double-pulse test results for the fabricated 3.3-kV wire-bonding module.

6.6 Chapter Summary

This chapter introduces the detailed design, fabrication processes, and experimental tests for the proposed 3.3-kV double-sided wire-bondless module. For the higher-voltage module, electric field reduction in the proposed compact module package need to be specifically considered to ensure the module can operate at higher voltage. Thus, the electric field simulations were performed, together with the thermos-mechanical simulations, optimal design for the module package was selected. The major fabrication steps such as device re-metallization including gate pad enlargement, silver sintering process, and two-step encapsulation are described in detail. Several modules were successfully fabricated following the processes. At last, experimental evaluation of the fabricated module was conducted. The leakage current test and switching test verified the functionality of the module, and the dielectric test confirmed the module can operate at high voltage.

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Chapter 7 Conclusion and Future Work

7.1 Conclusion

This dissertation discussed the design, fabrication, and characterization of two SiC double-sided wire-bondless modules, one is a stack module with LTCC interposer, and the other one is a higher-voltage (3.3-kV) module with metal posts for interconnection.

As part of the dissertation research, materials with high in-plane thermal conductivity was investigated. Thermal materials including nano-diamond, graphene, and pyrolytic graphite sheet (PGS) were studied regarding their capability to integrate within the LTCC interposer and thermal performance. After experimental tests, the PGS is considered as a good candidate as heat spreader for LTCC interposer because of its good thermal performance, ease to use and apply, and stability.

A double-sided stack wire-bondless half-bridge power module with LTCC interposer for SiC MOSFETs was proposed, electrical and thermos-mechanical simulations were used to optimize the module package design. Multiplayer LTCC interposer was introduced into the module as device flip-chip attachment substrate to achieve both horizontal and vertical electrical paths, as a result, power loop current can be partially cancelled and the critical power loop inductance can be reduced. A simulated loop inductance of 4.8 nH was achieved at 1 MHz, which helps improve the switching performance of the power module.

Power module prototype of the proposed design was fabricated. To achieve wire bondless interconnection, SiC device re-metallization, copper ball attachment, and flip-chip bondless were developed. The leakage current test, double-pulse test, and thermal cycling test were performed on the fabricated module to evaluate the performance of the power module. The test results exhibited low voltage ringing and overshoot, and good reliability.

The other module package was proposed based on the research of double-sided wire-bondless power module for higher voltage application. 3.3-kV SiC MOSFETs were used in this module. Electric field reduction and thermo-mechanical reliability were both considered and simulated to help select the optimal module package design. Module prototype was also fabricated, different re-metallization process for device pads was performed using sputtering and E-beam evaporation, Mo posts were used for better thermos-mechanical stability, silver sintering process was used for die attachment instead of solder reflow due to its low voiding and high interface reliability, and a two-step encapsulation using additional high-voltage passivation material was applied for the power module fabrication. Experimental tests showed the capability to operate at high voltage for the fabricated power module.

7.2 Future Work

To further test the reliability of the fabricated modules, longer-term thermal cycling test and power cycling test should be performed. Comparison of the switching performance between the proposed double-sided module and commercial double-sided module of the close working range should also be made. The nano-silver sintering paste is a promising die attachment material with superior electrical and thermal conductivity, as well as reliability compared to solder pastes. However, its bonding quality highly depends on the sintering process. Pressure-less and pressure-assisted sintering are recommended to performed and compared.

The electrical insulation capability of two-step encapsulation should be investigated and characterized by the partial discharge inception voltage (PDIV) test, how PI passivation layer will affect the PDIV should be studied, as well as how the thickness of PI layer will affect.

For the 3.3-kV wire-bondless module, double-pulse test at higher voltage above 2 kV should be performed to study the high voltage switching waveforms of the module.

An appropriate cooling system designed for the proposed modules is worth investigating to improve the thermal management efficiency for the compact module packages. Ultimately, more power module prototypes should be fabricated and used to create a high-density, medium-voltage power converter. A systematic study could also be done to better understand the performance of the proposed power module.

List of published and submitted work

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1. S. Huang and Z. Chen, "A SiC Double-Sided Stacked Wire-Bondless Power Module for High-Frequency Power Electronic Applications," in *Third Quarter 2021 Journal of Microelectronics and Electronic Packaging*.

2. P. Sun, X. Cui, S. Huang, P. Lai, Z. Zhao and Z. Chen, "LTCC Based Current Sensor for Silicon Carbide Power Module Integration," in *IEEE Transactions on Power Electronics (Early Access)*.

3. J. Ke, S. Huang, Z. Yuan, Z. Zhao, X. Cui, S. S. Ang and Z. Chen, "Investigation of Low-Profile, High-Performance 62-mm SiC Power Module Package," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2020.

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