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Towards High Efficiency and High Power Density Converter: System Level Design, Modulation, and Active EMI Filters

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Towards High Efficiency and High Power Density Converter:
System Level Design, Modulation, and Active EMI Filters

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Abstract

Power converter exposes strong challenges to its efficiency, power density and reliability. For the grid-connected inverter application, three-level (3-L) T-type neutral-point-clamped (TNPC) inverters has higher efficiency and lower total harmonic distortion (THD) compared to two-level inverter. Hybrid switch concept combines the benefit of both silicon carbide (SiC) MOSFET and Si IGBT. By applying hybrid switch structure in 3-L T-type inverter, the total power density of 3-L TNPC inverter will be higher while the cost will be lower than that of all-SiC 3-L T-type inverter. The hybrid switch based 3-L TNPC inverter also imposes challenge to its modulation and control, a propoer modulation and control shceme need to be chosen to enable better inverter performance in terms of efficiency, neutral point balancing and electromagnetic interference (EMI). Morever, to shrink the EMI filter size for the power converter, an active EMI filter (AEF) structure is proposed. The proposed AEF provides superior performance than any of the conventional passive EMI filter and the existing AEFs. In this work, the system level design and testing of a 30 kW grid-connected 3-L T-type inverter with hybrid switch structure is discussed. Then, an improved space vector modulation (SVM) has been proposed, which enables neutral-point balancing (NPB) control in the proposed hybrid-switch-based TNPC inverters with loss and common-mode voltage reduction. Finally, the design, modelling, and testing of the proposed AEF is demonstrated.

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I would like to thank Dr.Fang Luo for offering me the chance to fulfill my master's degree under his supervision. I'm grateful for the training and advice he has provided to me as a graduate student.

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Dedication

   This work is dedicated to my parents (names are not included for privacy) for supporting me through childhood to adult. I am also thankful to my future wife for not being present in my life till now, so I could dedicated on research.

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Chapter 2 is made up of this paper

2. H. Peng et al., "Improved space vector modulation for neutral-point balancing control in hybrid-switch-based T-type neutral-point-clamped inverters with loss and common-mode voltage reduction," in CPSS Transactions on Power Electronics and Applications, vol. 4, no. 4, pp. 328-338, Dec. 2019.
doi: 10.24295/CPSSTPEA.2019.00031.
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3. H. Peng, B.Narayanasamy, Z.Yuan, A. Imran and F. Luo, "Selective Digital Active EMI filtering using Resonant Controller", submitted for review in *IEEE Transactions on Power Electronics*, **Under review**
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1   Introduction

The power converter is heading towards higher power density, higher efficiency while having high reliability. Power converters are indispensable in automotive, aerospace, renewable energy applications as the motor drive inverter or grid-connected inverter. In data-centers and cloud infrastructure, rectifier and DC-DC converters are an essential part of the power supply. Within those applications, high power density, high efficiency, reliability are critical factors in the power architecture design.

Within the inverter topology, 3-L topology gradually draws attention from academia and industry (automotive, aerospace, renewable energy applications) due to its superior performance than the conventional two-level (2-L) topology. For the same device and configuration, 3-L topology provides higher efficiency, lower THD, and smaller passive filter size. Detailed system-level modeling and prototype building are available in the literature. The primary design issues for the 3-L inverter include but not limited to semiconductor selection, DC-link capacitor selection, output and input filter design, and hardware design.

Among wide bandgap (WBG) semiconductor devices, two materials suitable for power electronic applications are SiC MOSFET and GaN devices. However, the die size is still a bottleneck for WBG devices, which limited its application in high power applications. The benefits and challenges in paralleling WBG devices are available in the literature. The cost will increase dramatically if WBG devices are used in parallel. In order to overcome the higher cost, some literature proposes using the hybrid-switch structure. In the hybrid-switch structure, the principle is to parallel Si IGBT with SiC MOSFET for higher current rating applications to ensure low cost. However, the gate driver and the modulation strategy of such paralleling devices are complicated. Furthermore, in mixed switch combinations, the key idea for mixed switch combinations is to re-

place the Si IGBT with SiC MOSFET only in some switch positions within the topology, which enables the benefit of high efficiency, lower cost, and simple structure.

Furthermore, the combination of 3-L topology with mixed switch structure, features high efficiency, low cost, and simple structure. However, this structure has not been thoroughly investigated in 3 phase application yet. Within the 3 phase application, the main challenges will be system-level optimization and control and modulation. In this study, the system-level optimization is first introduced and follows the control and modulation of the proposed topology.

Lastly, when power electronics products are sold in the market, the converter or inverter itself needs to pass specific conducted emission standards. For solving electromagnetic interference (EMI) issues within the converter or inverter, EMI filter is introduced. Conventionally, the EMI filter occupies around 30 % of system volume while it becomes a bottleneck for the converter to gain higher power density. Thus, active EMI filter (AEF) are used for reducing the filter size. There are feedforward and feedback types of AEFs. For most of the offshore AEFs, the attenuation was limited 24 dB. In this study, a resonant controller-based voltage sensing current cancellation (VSCC) active EMI filter is pushing the attenuation 45 dB, which is 21 dB higher than the offshore AEFs.

This work is to solve the current issues within 3-L TNPC topology with hybrid-switch structure and active EMI filter. In Chapter 2, a system-level modeling, design, and testing of 3-L TNPC topology with hybrid switch structure is carried out. In Chapter 3, the modulation and control of 3-L TNPC topology with hybrid-switch structure is introduced. The active EMI filter is discussed, and resonant-controller based VSCC active EMI filter is introduced in Chapter 4. Finally, Chapter 5 gives the conclusion and future work.

2 Practical Design and Evaluation of a High Efficiency 30-kVA Grid Connected PV Inverter with Hybrid Switch Structure

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Simon S. Ang, and Haider Ghazi Mhiesan

2.1 Abstract

Photovoltaic (PV) grid-connected inverter exposes strong challenges to its efficiency, power density and reliability. This paper presents the design and test of a 30 kVA grid-connected inverter. The designed inverter achieved peak efficiency of 99.3% and a specific power of 2 kW/L by using a hybrid switch based three-level (3-L) T-type neutral point clamped (TNPC) topology. The hardware prototype presents excellent dynamic current and thermal distribution.

2.2 Introduction

Photovoltaic sources are a promising and emission free renewable energy source [1], and grid connected inverters are one of the main units within the PV grid connected system. With the growth of wide bandgap (WBG) devices [2] such as SiC MOSFETs and GaN high-electron-mobility transistors (HEMT), grid-connected inverters realize benefits of smaller size, lower weight, and lower loss. Hybrid switch based converters [3–5] have merits of low conduction loss as well as low cost.

Two-level (2-L) inverters, 3-L neutral-point-clamped (NPC) inverters, and 3-L TNPC inverters are three typical inverter topologies for grid-connected application and will be compared in this paper. a 3-L TNPC with hybrid switch structure is then chosen for its superior performance
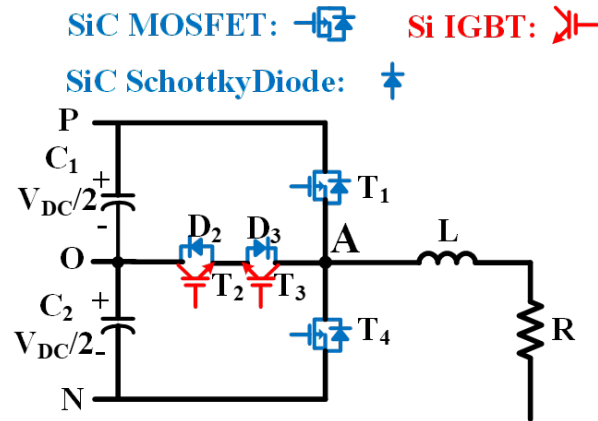
Fig. 2.1: A hybrid switch based TNPC structure[4]

under high switching frequency scenarios. A 3 phase TNPC with hybrid switch structure is then built and tested. Dynamic current sharing between devices [6] is ensured by adopting switching cell method. Continuous test is performed under full power rating for efficiency and thermal evaluation.

2.3   System Level Design and Optimization

Fig. 2.2 shows the grid connected inverter which is to be designed. The design targets are shown in Table 2.1. There are 4 major elements in the inverter system, they are semiconductors (Si IGBTs or SiC MOSFETs), the DC-link capacitor, the output filter, and cooling components. In order to optimize the inverter system's performance, system level modeling need to be carried out in terms of the weight, cost, and loss of the main elements. However, the controller system, sensors, and gate drivers are ignored in the modeling part since they are similar for different designs. The design flowchart is shown in Fig. 2.3, which will be extensively discussed in this section.

TABLE 2.1: Design targets for 3 phase inverter

Output power P_{out}	30 kVA	DC-link voltage V_{DC}	800 V
Ouput line-to-line voltage $V_{LL,rms}$	460 V	Grid frequency f_0	60 Hz
Power factor pf	0.8 to 1	Efficiency η	99%
Switching frequency f_{sw}	70kHz	Modulation techniques	SPWM
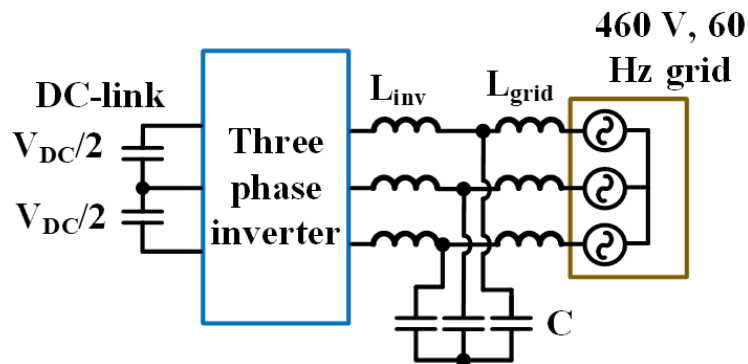
Fig. 2.2: Three phase grid connected inverter
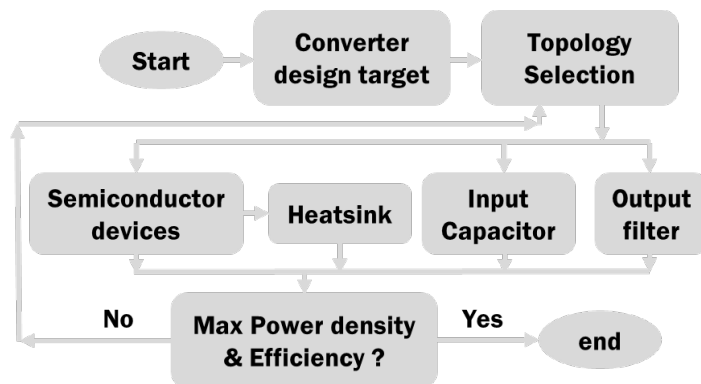
Fig. 2.3: Design methodology

2.3.1 Inverter Topology and Semiconductor Stage Evaluation

In this section, four topologies are evaluated: 2-L 3 phase inverter using all-SiC MOSFET, 3-L 3 phase NPC inverter using SiC MOSFET and SiC schottky diode, 3-L 3 phase TNPC inverter using all-SiC MOSFET, and hybrid switch based 3-L 3 phase TNPC inverter. Schematic of those three topologies are shown in Fig. 2.4a to Fig. 2.4d, respectively.

[5] presented that for the high power factor application, clamping leg devices of the 3-L TNPC inverter will be mainly soft switching. For 3-L TNPC inverter, assuming the switching state 1, 0, and -1 represent the phase leg output being clamped to the input positive rail, the input middle point, and the input negative rail respectively. The switching loss table of 3-L TNPC can be given as Table 2.2. When the power factor target of the inverter is high enough, the switching loss of clamping leg is negligible. The hybrid switch based 3-L TNPC structure, which is shown in Fig. 2.4d, utilizes Si IGBT and SiC Schottky diode as clamping leg switches and SiC MOSFET for half-bridge switch positions. With SPWM, the clamping switches are soft-switching under the unity power factor, and thus, the utilization of Si IGBTs does not increase the switching loss. Therefore, the total semiconductor cost of this hybrid switch based 3-L TNPC is lower than that of the all-SiC 3-L TNPC inverter. While the cost is low, the efficiency is higher than that of the all-SiC 3-L TNPC inverter.

TABLE 2.2: Switching loss table for 3-L TNPC inverter

Switching action	1 to 0 and 0 to 1	-1 to 0 and 0 to -1
Switching loss ($I_{ph} > 0$)	$E_{T1,\,off,\,on} = E_{Mos,\,off,\,on}$ $E_{T3,\,on,\,off} = 0$	$E_{T2,\,on,\,off} = E_{Mos/IGBT,\,on,\,off}$ $E_{T4,\,off,\,on} = 0$
Switching loss ($I_{ph} < 0$)	$E_{T3,\,on,\,off} = E_{Mos/IGBT,\,on,\,off}$ $E_{T1,\,off,\,on} = 0$	$E_{T4,\,off,\,on} = E_{Mos,\,off,\,on}$ $E_{T2,\,on,\,off} = 0$

To evaluate the performance of four topology candidates mentioned above, On company's semiconductor devices are chosen, detailed devices' parameters are shown in Table 3.6. Conduc-
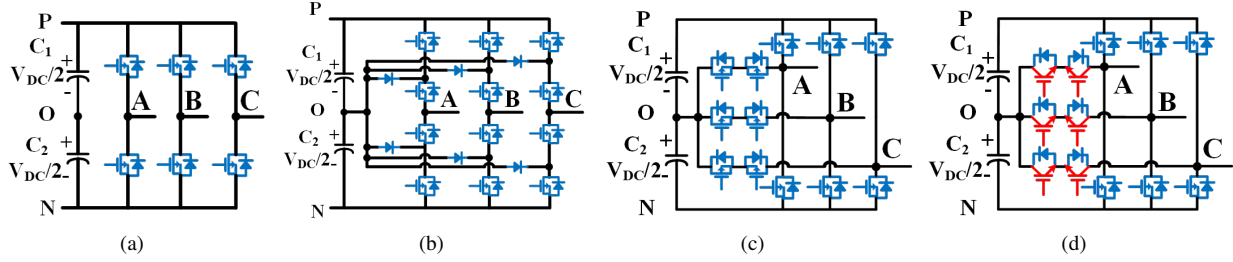
Fig. 2.4: Evaluated converter topologies: (a) 2-L 3 phase inverter (b) 3-L 3 phase NPC inverter (c) 3-L 3 phase TNPC inverter (d) 3-L 3 phase TNPC inverter with hybrid switch structure

tion and switching characteristics of those devices can be extracted from the datasheet. To achieve target efficiency (99%) at rated power level (30 kw), 6 SiC MOSFETs, 3 SiC diodes, and 2 Si IGBTs are used in parallel for each switch position.

TABLE 2.3: Power semiconductors used in the evaluation

	Voltage	Current	Typical switching loss	Cost p.u.(Mouser)
SiC MOSFET @ On-Semi NTHL080N120SC1	1200 V	31 A	$E_{on} = 258\ \mu J$, $E_{off} = 52\ \mu J$ @800 V, 20 A, $R_g = 4.7\ \Omega$	7.64 $
SiC Diode @ On-Semi FFSH2065A-D	650 V	20 A	$E_{sw} \approx 0$ (Very low reverse recovery loss)	5.91 $
Si IGBT @ On-Semi FGH40T65SH	650 V	40 A	$E_{on} = 1390\ \mu J$, $E_{off} = 541\ \mu J$ @400 V, 40 A, $R_g = 6\ \Omega$	2.51 $

The power losses of semiconductor devices depend on the voltage/current waveforms and control methodologies. For simplicity, the SPWM modulation is utilized, and the output current waveform is assumed to be idealized sinusoidal function. Based on [6–8], the loss information of different topologies can be calculated as Table 2.5, the parameter which is used in the calculation is shown in Table 2.4.

The semiconductor stage efficiency for each topology is shown in Fig. 2.5. The cost of 2-L, 3-L NPC, 3-L TPC, and 3-L TNPC with hybrid switch combination are 275.04 $, 656.46 $, 550.08 $, and 411.54 $, respectively. 3-L NPC topology has lowest efficiency due to its largest conduction loss. At high switching frequency scenario, 2-L inverter's efficiency drops rapidly due to its high commutation voltage. For 70 kHz switching frequency application, 3-L TNPC has

TABLE 2.4: Parameter used in the loss calculation

Parameter	Definition
f_0	Grid frequency
w	Grid angular frequency
$P_{cond,MOS}$	Conduction loss of MOSFET
$P_{cond,diode}$	Conduction loss of diode
$P_{cond,IGBT}$	Conduction loss of IGBT
$P_{sw,MOS}$	Switching loss of MOSFET
$P_{sw,IGBT}$	Switching loss of IGBT
φ	Power dactor angle
$I_{PK} = \frac{\sqrt{6}P_{out}}{3V_{LL,rms}}$	Peak phase current
$i(k) = I_{pk} \cdot sin(\frac{k \cdot f_0}{f_{sw}} \cdot 2\pi - \varphi)$	Transient current
M	Modulation index
$R_{MOS,on}$	Conduction resistance of MOSFET
$V_{fw,diode}$	Forward voltage drop of diode
R_{diode}	Conduction resistance of diode
$V_{fw,IGBT}$	Forward voltage drop of IGBT
R_{IGBT}	Conduction resistance of IGBT
$E_{MOS,on}(v,i)$	Switching on energy of MOSFET
$E_{MOS,off}(v,i)$	Switching off energy of MOSFET
$E_{IGBT,on}(v,i)$	Switching on energy of IGBT
$E_{IGBT,off}(v,i)$	Switching off energy of IGBT

highest efficiency among all topologies. Morever, for the unity power factor scenario, efficiency of 3-L TNPC inverter with hybrid switch combination is comparable with that of all-SiC 3-L TNPC inverter. While the efficiency comparable, the cost of 3-L TNPC inverter with hybrid switch combination is much lower than that of all-SiC 3-L TNPC inverter. Thus, 3-L TNPC inverter with hybrid switch combination topology is chosen for semiconductor stage.

2.3.2 LCL filter Design

The basic LCL structure can be found in Fig. 2.2. L_{inv}, C_{out}, and L_{grid} donate the inverter side inductor, capacitor, and grid side inductor, respectively. The value selection of L_{inv} depends on the current ripple limitation of inverter output stage. The capacitor will add to the reactive power for the inverter system, normally the reactive power consumed by capacitor is limited to $2 \sim 5\%$

TABLE 2.5: Loss calculation for different topologies (single phase)

Topology	Conduction loss
2-L inverter	$P_{cond,MOS} = \frac{1}{\pi}\int_0^\pi i^2(k)R_{MOS,on}\, dwt$ (2.1)
3-L NPC inverter	$P_{cond,MOS} = \frac{1}{\pi}\int_0^\pi i^2(k)\cdot R_{MOS,on}\cdot(1+M\lvert sin(wt)\rvert)\, dwt$ (2.2) $P_{cond,diode} = \frac{1}{\pi}\int_0^\pi (1-M\lvert sin(wt)\rvert)\cdot(\lvert i(k)\rvert V_{fw,diode}+i^2(k)\cdot R_{diode})\, dwt$ (2.3)
3-L TNPC inverter	$P_{cond} = \frac{1}{\pi}\int_0^\pi i^2(k)R_{MOS,on}\cdot(2-M\lvert sin(wt)\rvert)\, dwt$ (2.4)
3-L TNPC inverter with hybrid switch structure	$P_{cond,MOS} = \frac{1}{\pi}\int_0^\pi i^2(k)\cdot R_{MOS,on}\cdot M\lvert sin(wt)\rvert)\, dwt$ (2.5) $P_{cond,diode} = \frac{1}{\pi}\int_0^\pi (1-M\lvert sin(wt)\rvert)\cdot(\lvert i(k)\rvert\cdot V_{fw,diode}+i^2(k)\cdot R_{diode})\, dwt$ (2.6) $P_{cond,IGBT} = \frac{1}{\pi}\int_0^\pi (1-M\lvert sin(wt)\rvert)\cdot(\lvert i(k)\rvert\cdot V_{fw,IGBT}+i^2(k)\cdot R_{IGBT})\, dwt$ (2.7)
Topology	**Switching loss**
2-L inverter	$P_{sw,MOS} = 2f_0\cdot\sum_{k=\frac{0\cdot f_{sw}}{2\pi\cdot f_0}}^{k=\frac{\pi\cdot f_{sw}}{2\pi\cdot f_0}}(E_{MOS,on}(V_{DC},\lvert i(k)\rvert)+E_{MOS,off}(V_{DC},\lvert i(k)\rvert))$ (2.8)
3-L NPC inverter	$P_{sw,MOS} = 2f_0\cdot\sum_{k=\frac{0\cdot f_{sw}}{2\pi\cdot f_0}}^{k=\frac{\pi\cdot f_{sw}}{2\pi\cdot f_0}}(E_{MOS,on}(\frac{V_{DC}}{2},\lvert i(k)\rvert)+E_{MOS,off}(\frac{V_{DC}}{2},\lvert i(k)\rvert))$ (2.9)
3-L TNPC inverter	$P_{sw,MOS} = 2f_0\cdot\sum_{k=\frac{0\cdot f_{sw}}{2\pi\cdot f_0}}^{k=\frac{\pi\cdot f_{sw}}{2\pi\cdot f_0}}(E_{MOS,on}(\frac{V_{DC}}{2},\lvert i(k)\rvert)+E_{MOS,off}(\frac{V_{DC}}{2},\lvert i(k)\rvert))$ (2.10)
3-L TNPC inverter with hybrid switch structure	$P_{sw,MOS} = 2f_0\cdot\sum_{k=\frac{\varphi\cdot f_{sw}}{2\pi\cdot f_0}}^{k=\frac{\pi\cdot f_{sw}}{2\pi\cdot f_0}}(E_{MOS,on}(\frac{V_{DC}}{2},\lvert i(k)\rvert)+E_{MOS,off}(\frac{V_{DC}}{2},\lvert i(k)\rvert))$ (2.11) $P_{sw,IGBT} = 2f_0\cdot\sum_{k=\frac{0\cdot f_{sw}}{2\pi\cdot f_0}}^{k=\frac{\varphi\cdot f_{sw}}{2\pi\cdot f_0}}(E_{IGBT,on}(\frac{V_{DC}}{2},\lvert i(k)\rvert)+E_{IGBT,off}(\frac{V_{DC}}{2},\lvert i(k)\rvert))$ (2.12)

of converter's power level. Then, L_{grid} need to be designed according to IEEE 1547 and IEEE 519 standard for harmonics of grid-tied inverter.

According to [9], the expression for calculating the minimum value for L_{inv} can be found in (2.13). Since the output sinusoidal peak current is around $I_{PK} = 53.2A$, the peak current ripple can be set to 40% of peak sinusoidal current. Thus, the calculated minimum inductance value for
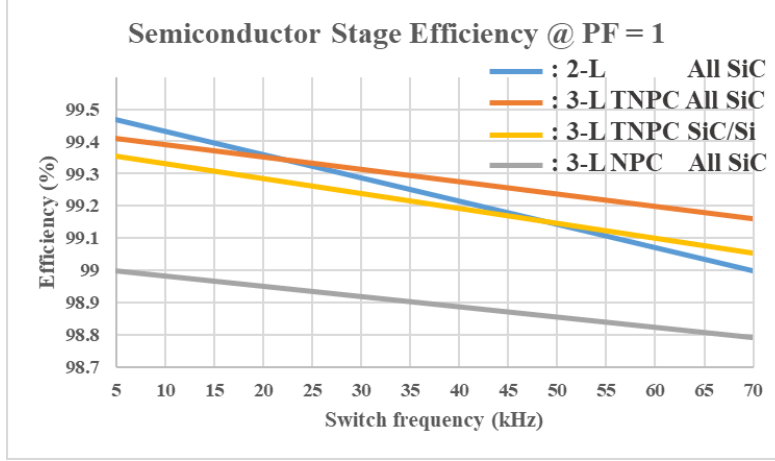
Fig. 2.5: Semiconductor stage efficiency comparison

L_{inv} is around $90\mu H$, which will be used for physical design of the inductor. According to (2.13), the maximum capacitance value C_{out} is $7.5\mu H$ in order to limit the reactive power. Finally, $5\mu H$ MKP386M550125YT4 film capacitor from Vishay is chosen.

$$\Delta I_{max} \approx \frac{V_{DC}T_{sw}}{6L_{inv}}, \; L_{inv} \approx 90\mu H \qquad (2.13)$$

$$Q_c \approx 3wV_{ph,rms}^2 C_{out} < 0.02P_{out}, \; C_{out} < 7.5\mu H \qquad (2.14)$$

Based on the designed value of L_{inv} and C_{out}, the value of grid side inductor L_{grid} can be designed according to IEEE 1547 and IEEE 519 grid-tied inverter harmonics requirement. The IEEE 1547 and IEEE 519 grid-tied inverter harmonics requirement is shown in Table 2.6. The phase voltage is a PWM waveform. The filter need to attenuate phase voltage noise to obtain the output phase current waveform which meet the standard. The required attenuation can be expressed as (2.15).

TABLE 2.6: IEEE 1547 and IEEE 519 grid-tied inverter harmonics requirement

Harmonic order	$< 11^{th}$	$11 - 17^{th}$	$17 - 23^{th}$	$23 - 35^{th}$	$> 35^{th}$	THD
Limit (% of fundamental current)	$< 4\%$	$< 2\%$	$< 1.5\%$	$< 0.6\%$	$< 0.3\%$	$< 5\%$

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$$G_{grid}(s) = \frac{I_{g,spec}(s)}{V_{inv,SPWM}(s)} \tag{2.15}$$

Morever, the attenuation (output current to input voltage) of LCL filter is expressed in (2.16). The attenuation spectrum of LCL filter need to be lower than the spectrum of required attenuation $G_{grid}(s)$. The LCL filter attenuation is plotted based on different value of L_{grid}, and the comparison between LCL filter attenuation and the required attenuation is shown in Fig. 2.6a. Since the switch frequency is as high as 70 kHz, the LCL filter attenuation is much lower than the grid code requirement in the high frequency range. For the low frequency range, which is shown in Fig. 2.6b, it can be observed that L_{grid} inductance need to be higher than 50 μH. Finally, $L_{grid} = 100\ \mu H$ is chosen for the grid side inductor.

$$G_{LCL}(s) = \frac{I_g(s)}{V_{inv}(s)} = \frac{1}{L_{inv}L_{grid}C_{out}s^3 + (L_{inv} + L_{grid})s} < G_{grid}(s) \tag{2.16}$$
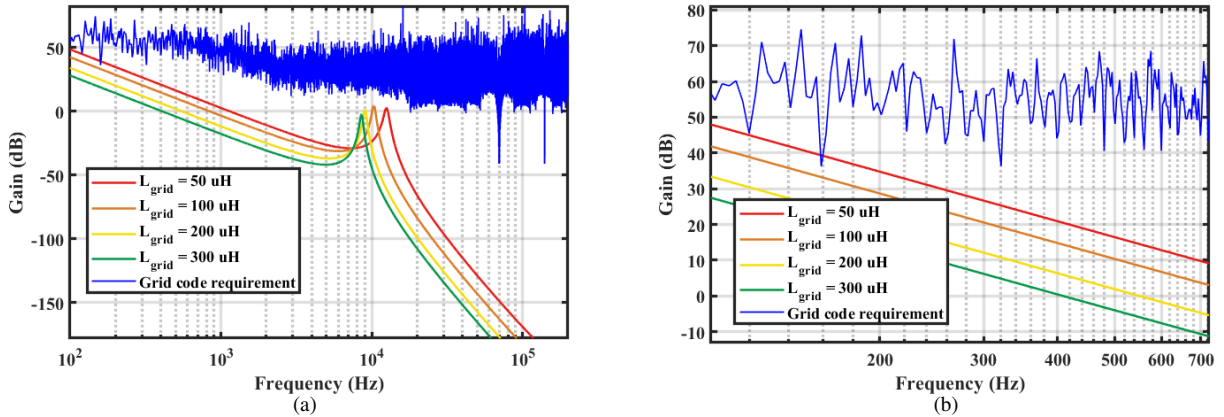
Fig. 2.6: LCL filter design in frequency domain: (a) attenuation of LCL filter comparing to required attenuation (b) zoom in of low frequency range

The final LCL filter value are: $L_{inv} = 90\ \mu H$, $L_{grid} = 100\ \mu H$, and $C_{out} = 5\ \mu H$. Normally the resonant frequency of the LCL filter f_{res} need to be higher than 10 times of the grid frequency,

and lower than half of the switching frequency. The resonance frequency f_{res} of the LCL filter is given by (2.17). Furthermore, the voltage drop on the filter inductor can be found in (2.18), which is much lower than the phase voltage. The LCL filter value design meets most of the design criteria mentioned in the reported literatures.

$$10 f_0 < f_{res} = \frac{1}{2\pi} \sqrt{\frac{L_{inv} + L_{grid}}{L_{inv} L_{grid} C_{out}}} = 10.34 \ kHz < 0.5 f_{sw} \tag{2.17}$$

$$V_{L,rms} = 2\pi f_0 (L_{inv} + (L_{grid}) \cdot I_{rms} \approx 2.7 \ V << V_{ph,rms} = 265.6 \ V \tag{2.18}$$

The area product A_p design method, which is expressed in (2.19), is used for inductor design. K_0 is the filling factor for the inductor window area, which is normally set at 0.3 to 0.4 with insulation and support consideration. J is the winding current density, which is normally set as 3.5 A/mm^2 under natural air cooling conditions. To further reduce the skin effect in high switching frequency application, Litz wire (22 AWG with 45 strand, 6 AWG-equivalent) is selected for inductor winding. B_m is the maximum flux density in the inductor core, which is chosen based on core material specification. A_e and A_w donates the inductor's core cross sectional area and window area, respectively. Magnetic powder core [10] is selected for core design. For inverter side inductor L_{inv}, MPP 60 μ core with 62 cm outer diameter is chosen, and 22 turns of windings are implemented. For the grid side inductor L_{grid}, high flux 125 μ core with 62 cm outer diameter is chosen, and 18 turns of windings are implemented.

$$A_p = A_e A_w > \frac{L I_{rms} I_{max}}{K_0 J B_m} \tag{2.19}$$

2.3.3 DC-link capacitor

The DC-link capacitor volume occupies a large portion of the inverter system's volume. In this study, 3 major factors are taken into consideration for the DC-link capacitor selection: DC-link voltage ripple, neutral point voltage ripple, and capacitor's current rating.

For 3-L inverter, assuming two capacitors C_1 and C_2 are in parallel to provide neutral point. The total DC-link capacitance is given by $C_{DC-link} = 0.5C_1 = 0.5C_2$. [8] showed that the ripple voltage on the DC-link can be obtained by (2.20). The required DC-link capacitor $C_{DC-link}$ to keep the DC-link voltage ripple ΔV_{dc} within 0.5% of total DC-link voltage V_{dc} can be obtained as 24.3 μF, and then $C_1 = C_2 = 48.6\mu F$.

$$\Delta V_{dc} = \frac{V_{ph,rms}I_{ph,rms}}{2\pi f_{sw}V_{DC}C_{DC-link}}(\sqrt{3} - \frac{\pi}{3}) < 0.5\%V_{dc} \tag{2.20}$$

However, for 3-L inverter, the neutral point voltage V_{np} will also have variation due to the neutral point current. In order to limit the neutral point voltage variation, neutral point balancing (NPB) control need to be implemented. [11] proposed a NPB control strategy using zero sequence injection. Furthermore, [12] gave the analytical relationship between neutral point voltage variation ΔV_{np} and the circuit parameters under the zero sequence injection NPB control frame, and the expression is given by (2.21). C_{np} is the total neutral point capacitance, which satisfies $C_{np} = 2C_1 = 2C_2$. $k(M, cos(\varphi))$ is a parameter associate with worst case power factor and modulation index. For the system parameters in the paper ($cos(\varphi) = 0.8 - 1$ and $M \approx 0.94$), $k(M, cos(\varphi))$ is approximately 0.1. To limit the neutral point voltage ripple ΔV_{np} to be within 2% of the DC-link voltage V_{DC}, the neutral point capacitance C_{np} can be calculated as $C_{np} = 651\mu F$. To leave some design margin, C_{np} is finally designed as $C_{np} = 840\mu F$, and then $C_1 = C_2 = 420\mu F$.

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$$\Delta V_{np} = \frac{V_{DC}I_{LL,rms}}{2C_{np}wV_{LL,rms}} \cdot k(M, cos(\varphi)) < 2\%V_{DC} \tag{2.21}$$

The DC-link capacitor suffers both fundamental frequency harmonics current and switching frequency harmonics current. [13] gave the expression of DC-link capacitor's current, which can be found in (2.22)-(2.24). With the system parameter discussed in the paper, the RMS current of the DC-link capacitor $I_{cap,rms}$ can be calculated as 19 A.

$$I_{avg} = \frac{3}{4}I_{PK}Mcos(\varphi) \tag{2.22}$$

$$I_{rms} = \sqrt{\frac{3I_{PK}^2M(\sqrt{3} + \frac{2}{\sqrt{3}}cos(2\varphi))}{4\pi}} \tag{2.23}$$

$$I_{cap,rms} = \sqrt{I_{rms}^2 - I_{avg}^2} \tag{2.24}$$

In summary, the final DC-link capacitor $C_{DC-link}$ is set to be $210\mu F$, which is composed of two capacitor $C_1 = C_2 = 420\mu F$ in parallel. For each of the C_1 and C_2, 14 of 30 μF, 800 V DCP4L053007HD2KSSD film capacitors from WIMA are chosen.

2.4 Hardware Development and Experiment

The final architecture is shown in Fig. 2.7a, on T_1 and T_4 there are six SiC MOSFETs in parallel. And for T_2 and T_3 position, there are two IGBTs in parallel. For D_2 and D_3 position, there are three SiC Schottky diodes in parallel. The exact position of devices on hardware is shown in Fig. 2.7b. Entire 3-phase 3-L inverter prototype with heatsink is shown in Fig. 2.7c.
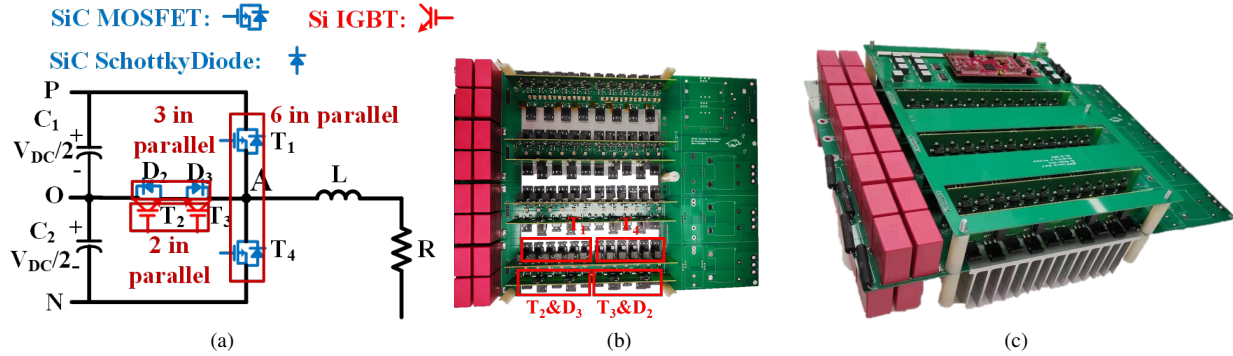
Fig. 2.7: Hardware prototype for 3 phase 3-L inverter with hybrid switch structure: (a) Structure of 3-L TNPC phase leg (b) Top view of prototype (c) 3-phase 3-L TNPC inverter

First, the double pulse test (DPT) for evaluating the current sharing and switching performance is conducted under 800 V DC voltage, 60A load current condition. DPT result for T_4 is shown Fig. 2.9, where dynamic current sharing is excellent for both turn on and turn off transient.
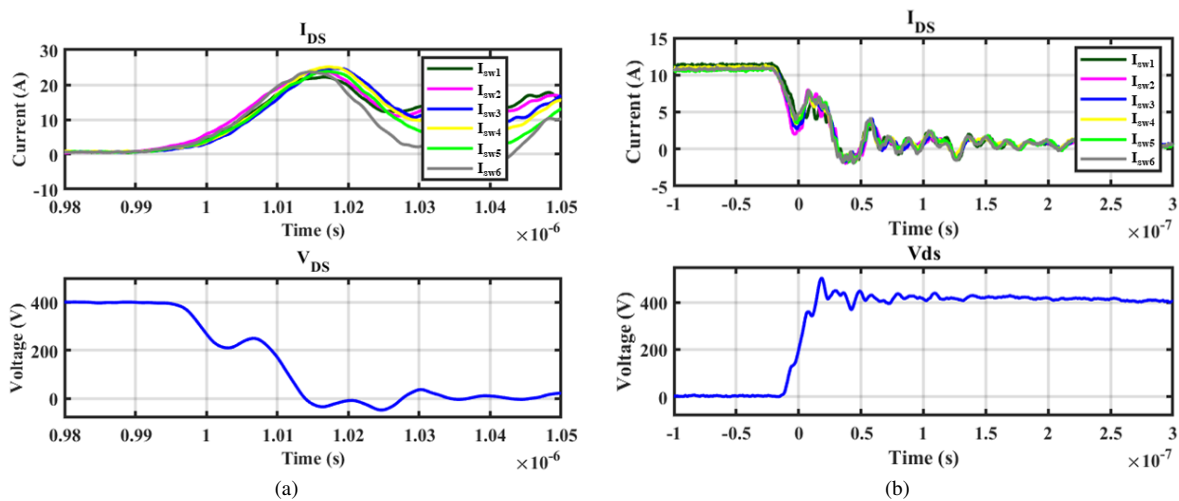
Fig. 2.8: DPT test waveform for T_4 device: (a) Turn on transient of T_4 position (b) Turn off transient of T_4 position

A 3-phase test is conducted under a full power rating (30 kVA) in laboratory. The DC-link voltage is set at 800 V. The fundamental frequency is set to 2 kHz and the power factor (pf) under test is 0.3 due to the equipment limitation. The switching frequency is set to 70 kHz. The test setup is shown in Fig. 2.9a, and the line-to-line voltage, phase current waveform is shown in Fig. 2.9b.
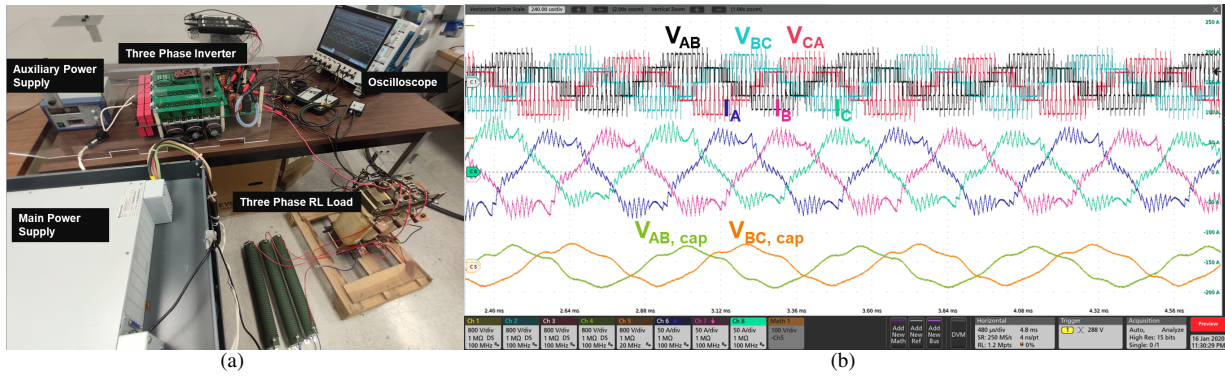
Fig. 2.9: Continuous test for 3 phase 3-L TNPC prototype: (a) Test setup for 3 phase testing (b) Testing waveform
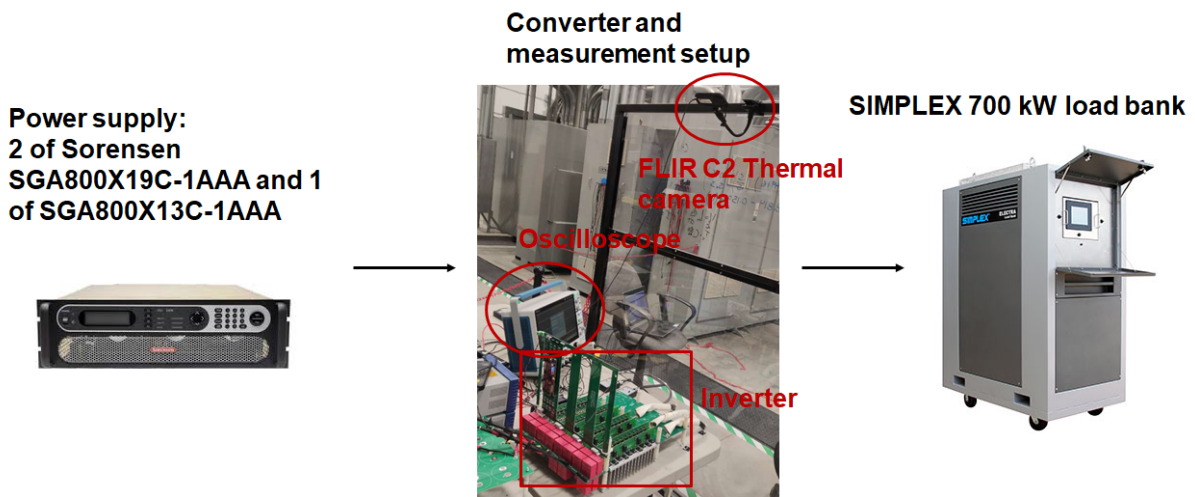
Fig. 2.10: Resistive load testing setup

The power testing of the inverter is also conducted under 30 kW resistive load. The basic test setup is shown in Fig. 2.10. And the schematic can be find in Fig. 2.11a. The testing waveform for the inverter under rated voltage and power is shown in Fig. 2.11b. As it can be seen from the figure, the input voltage is set to be 800 V, and the output line-line voltage is 460 V, while the output current is set to be 52 A.

The thermal information is also captured during the testing after 20 minutes burning. As it's shown in the Fig. 2.12b, the higher temperature of the entire prototype is only around 40 degree C, which might be due to the inaccuracy of the thermal camera. Taking inaccuracy of the thermal
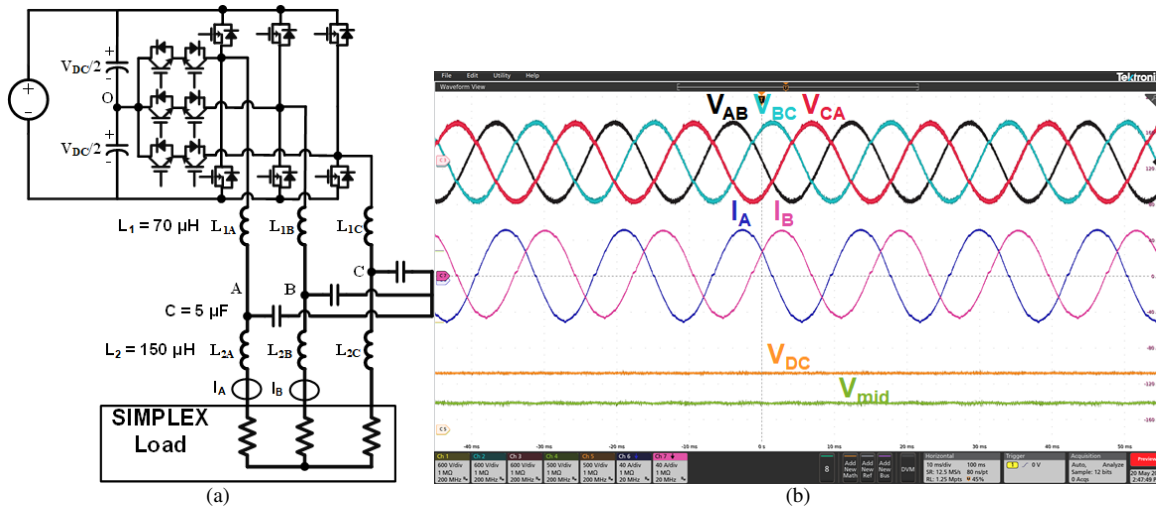
Fig. 2.11: Resistive load testing: (a) Resistive load testing schematic (b) Resistive load testing waveform

camera into account, the converter is still running at a safe temperature range (case temperature lower than 80 degree C). The thermal image result validate that the thermal design of the prototype has enough margin, which can ensure the inverter will still be safe operating even under heavy load.

The efficiency of the entire inverter system is also measured from the test setup, which is shown in Fig. 2.13a. The input and output power are both obtained from oscilloscope and Yokogawa WT1600 power analyzer. After comparison of both data, an accurate efficiency curve is drawn in Fig. 2.13b. As it can be seen from the figure, the highest efficiency of the inverter is around 99.26 %. At rated power (30 kW), the efficiency of the entire inverter is around 99.07 %.

2.5   Conclusion

Based on efficiency, cost, and weight comparison for different topology options, a 3-phase 3-L TNPC with hybrid switch combination is selected. The hardware prototype is then built and test. DPT shows good current sharing performance between paralleled devices. Three-phase test-

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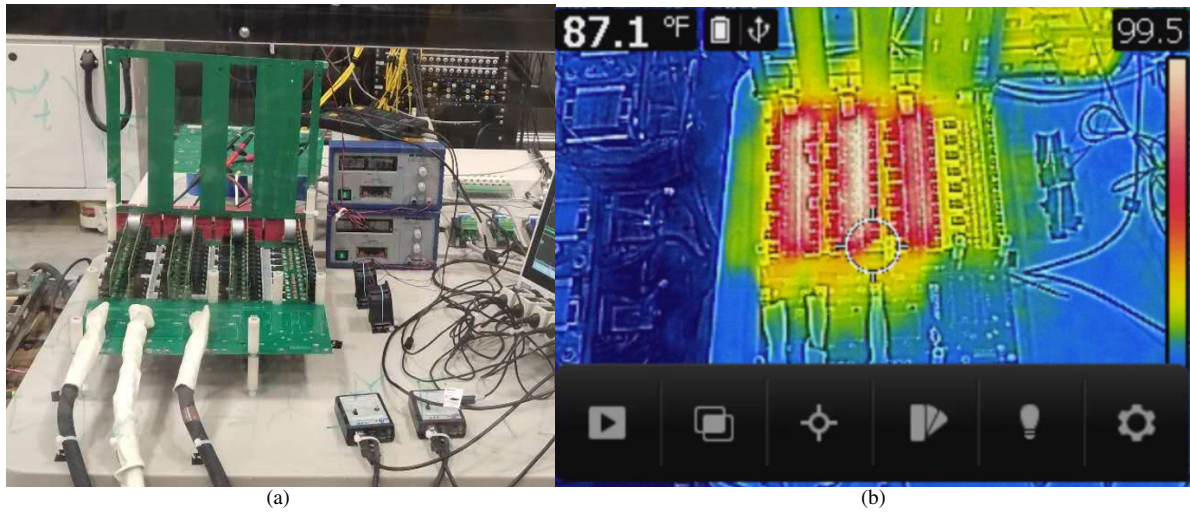
Fig. 2.12: Thermal image of the resistive load test: (a) original test setup (b) thermal image
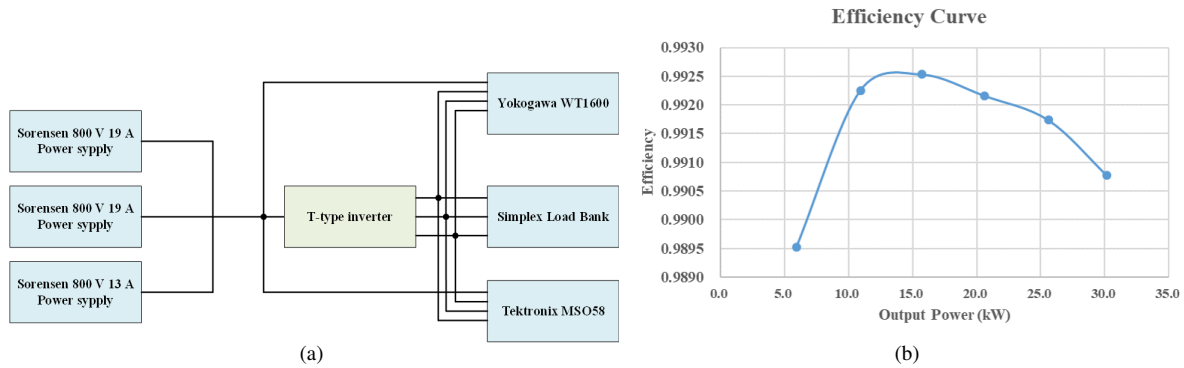
Fig. 2.13: Efficiency measurement of the inverter: (a) Efficiency measurement setup (b) Efficiency measured

ing under full power rating is carried out. The thermal measurement as well as the efficiency measurement are conducted, which validate the inverter system design.

2.6 Bibliography

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3 Space Vector Modulation for Neutral-Point Balancing Control in Hybrid-Switch-Based T-type Neutral-Point-Clamped Inverters With Loss and Common-Mode Voltage Reduction

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Amol Deshpande, Asif Imran Emon, Fang Luo, and Cai Chen

3.1 Abstract

This paper compares different space vector modulation (SVM) strategies for neutral-point voltage balancing (NPVB) control in three-level (3-L) T-type neutral-point-clamped (TNPC) inverters, and proposes an improved SVM trimmed for NPVB control in hybrid-switch-based 3-L TNPC inverter with the features of loss and common-mode voltage (CMV) reduction. The proposed SVM strategy uses a new principle of small vector selection and vector sequence, and thus, it can balance the neutral point (NP) potential and achieve soft-switching of clamping leg simultaneously. The paper includes detailed analysis for circuit commutation mode, loss breakdown, and common-mode voltage patterns under different operation conditions. The circuit simulations and experiments are carried out in the last part of this paper to validate the proposed SVM strategy.

3.2 Introduction

Three-level T-type neutral-point-clamped (3-L TNPC) inverter has higher efficiency and lower total harmonic distortion (THD) compared to two-level inverter, and it has become popular in high-speed motor drives and all-electric aircraft applications[1–5]. Emerging silicon carbide (SiC) MOSFET has lower losses and high switching speed compared to Si IGBT and enables higher efficiency and power density in power converters[6–11]. SiC MOSFET is becoming a

major competitor and replacement for Si IGBT in power electronics systems.
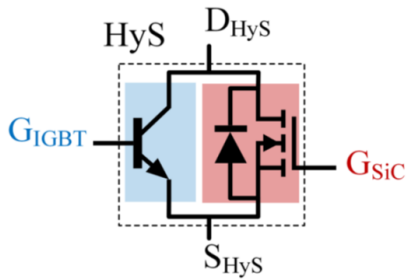
Fig. 3.1: Structure of the hybrid switch

TABLE 3.1: Current dependent operation of the hybrid-switch-based inverter [12]

Conditions:	SiC MOSFET voltage drop is lower than Si IGBT threshold	Load current is within SOA of SiC MOSFET	Load current exceed SOA of SiC MOSFET
Operations:	Only SiC MOSFET is turned on	Hybrid switch operation	Only IGBT is turned on
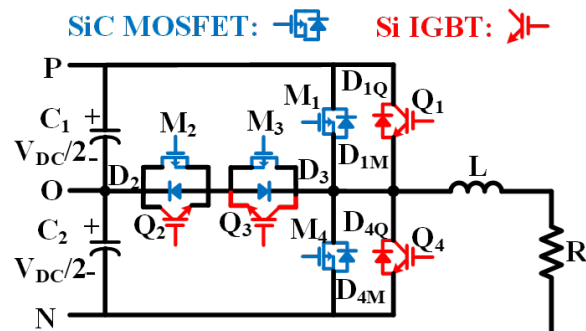
Fig. 3.2: T-type inverter with hybrid switch structure 1 [13]

However, the state-of-the-art die size limit and the high cost of SiC MOSFET are the bottlenecks for its high-current commercial applications. Therefore, [13] proposed a hybrid switch concept, as shown in Fig. 3.1. By adjusting the switching sequence of the two switches, the T-type inverter with the hybrid switch (hybrid structure 1) [14–16], which is shown in Fig. 3.2, can have low switching loss from SiC MOSFET switching, and low conduction loss from IGBT conduction. However, due to the long discharging time of the carriers inside the IGBT, the Si-SiC hybrid switch operation mode have a minimum duty cycle limitation [17], which deteriorates the output

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total harmonic distortion performance. Furthermore, the hybrid-switch-based 3-L TNPC increases the system complexity in terms of the gate driver and power loop design [18–20]. Because of more paralleled semiconductors, more gate drivers and more gating signals are required. [12] mentioned that the Si-SiC hybrid switch structure should ensure the safe operation area (SOA) of the SiC MOSFET. Table 3.1 illustrates the current dependent operation in [12].
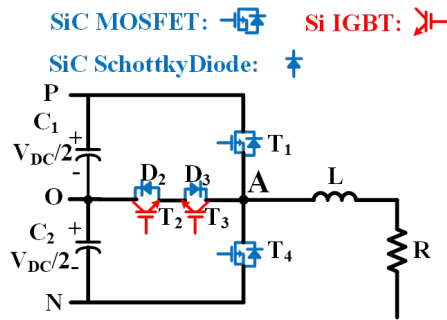
Fig. 3.3: T-type inverter with hybrid switch structure 2 [21]

To reduce the system complexity as well as improve the output THD performance, M_1, M_4, Q_2, Q_3, D_2 and D_3 in hybrid structure 1 are selected to operate, and the new structure is shown in Fig. 3.3 [21]. The hybrid structure 2 utilizes Si IGBT and SiC Schottky diode as clamping leg switches and SiC MOSFET for half-bridge switch positions. With SPWM, the clamping switches are soft-switching under the unity power factor, and thus, the utilization of Si IGBTs does not increase the switching loss. Therefore, the total semiconductor cost of this hybrid switch combination 3-L TNPC is lower than that of the all-SiC 3-L TNPC inverter. While the cost is low, the efficiency is higher than that of the all-SiC 3-L TNPC inverter.

Although hybrid structure 2 possesses the merits of low complexity and high efficiency, it has not been fully validated in the 3-phase 3-L TNPC system yet. One of the main challenges is to design a proper space vector modulation (SVM) scheme, which needs to consider the soft switching feature of the clamping leg, neutral point balancing (NPB) [22–25], and the common-

mode voltage (CMV) performance. This paper provides a criterion to choose the appropriate SVM for T-type inverter with hybrid structure 2 under different conditions. Firstly, this paper obtains the switching energy of T-type inverter with hybrid structure 2 by experimental double pulse test (DPT) result, then 3 different SVM schemes are discussed in terms of switching loss, NPB, and output CMV voltage performance.

The organization of the paper is as follows. Section II summarizes the soft-switching conditions for 3-L TNPC with hybrid structure 2, then loss analysis, neutral point balancing capability and common-mode noise voltage comparison of 3 different SVM schemes are discussed. In Section III, a 20 kVA hardware is built, the DPT is firstly performed to obtain exact switching loss, followed by the analysis and comparison of semiconductor loss breakdown, EMI spectrum, and neutral point voltage ripple for three SVMs. Section IV presents the conclusion of the preferred modulation scheme.

3.3 Analysis of Different Modulation on Hybrid Switch Based 3-Phase 3-L TNPC

For switching loss reduction [21] and NPB [22–25] in 3 phase 3-L TNPC inverter with hybrid switch combination, SVM 1 with NPB [23], SVM 2 with NPB [24], and improved SVM 2 with NPB are compared, and 1_{st} sector of the space vector modulation hexagon is given as an example. The nearest three space vector (NTSV) [26] and discontinuous pulse width modulation (DPWM) [27] are adopted to track the reference vector and further reduce the switching loss.

In this chapter, switching loss and soft-switching condition of clamping leg is discussed first in 3-L TNPC with the hybrid switch combination. Then three different SVM schemes are compared in terms of switching losses, neutral point balancing capability, and CMV performance, which gives guidance for hardware design and PWM modulation choice.
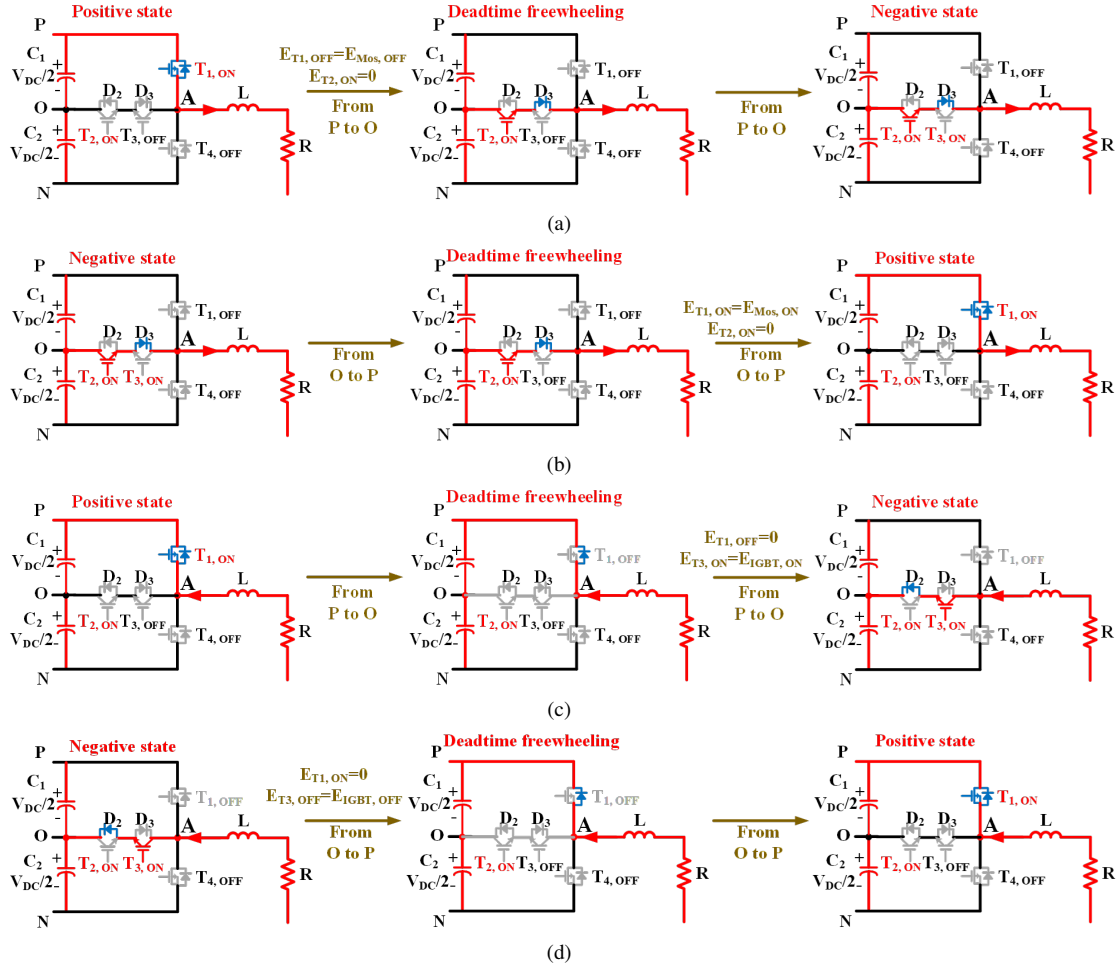
Fig. 3.4: Different switching transitions when the phase output is positive or neutral: (a) Switch transition 1 (Positive phase current) (b) Switch transition 2 (Positive phase current) (c) Switch transition 3 (Negative phase current) (d) Switch transition 4 (Negative phase current)

3.3.1 Preferred Switch Pairs in Terms of Switching Loss Reduction

Since switching loss of Si IGBT is much higher than SiC MOSFET, hard switching of Si IGBT on clamping leg in 3-L TNPC inverter with hybrid switch combination should be avoided or minimized. As shown in Fig. 3.4(a), when the phase current is positive, and the phase output voltage is transitioning from positive to neutral, T_1 is hard switching off, and then T_2 and D_3 are soft switched on. From Fig. 3.4(b) we can know that when phase current is positive, and the phase output voltage is transiting from neutral to positive, clamping leg devices are soft switched off,

Space vector	V_1	V_2	V_3	V_4
CMV	$-1/3V_{dc}$	$-1/6V_{dc}$	0	$1/6V_{dc}$
Space vector	V_5	V_6	V_7	V_8
CMV	$1/3V_{dc}$	$-1/6V_{dc}$	$1/6V_{dc}$	0

TABLE 3.2: CMV of space vectors

and T_1 is hard switched on. Moreover, when the phase current is negative, and phase output is transitioning from positive to neutral or from neutral to positive, T_3 is hard switched on and hard switched off.

In summary, when phase current is positive, switch pair 1 and 0 is preferred since the clamping leg is soft-switching, as shown in Fig. 3.4(a) and Fig. 3.4(b). Switch pair 0 and -1 should be avoided since clamping leg switch T_2 is hard switching. Symmetrically when phase current is negative, switch pair 0 and -1 is preferred to obtain the soft-switching character of clamping leg, and switch pair 1 and 0 should be avoided or minimized to reduce the switching loss of Si IGBT, as shown in Fig. 3.4(c) and Fig. 3.4(d). Based on the aforementioned analysis, different SVMs can be compared in terms of switching loss, more detailed information will be given in the later section.

3.3.2 Common Mode Voltage of 3L TNPC Inverter

Assuming that only heatsink is grounded, the equivalent model of 3 phase 3-L TNPC [28–33] is drawn in Fig. 3.5, with the consideration of all the semiconductor's junction to heatsink and output to ground capacitance. Also, a simplified model is given in Fig. 3.6, which indicates that the CMV noise can be modeled through (3.1).

$$V_{CM} = (V_{AN} + V_{BN} + V_{CN})/3 \tag{3.1}$$
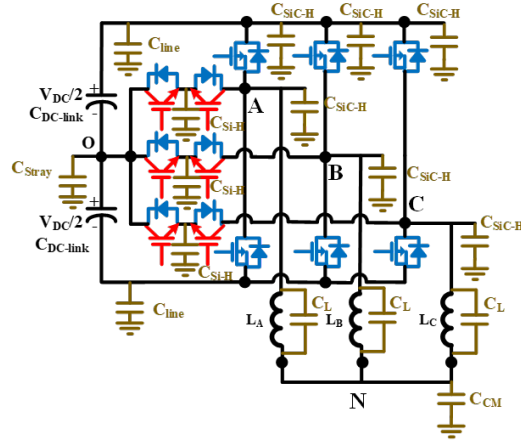
Fig. 3.5: Three-phase 3-L TNPC model with the parasitic capacitor

C_{Si-H}/C_{SiC-H}: pF range C_{line}: pF range
C_L: pF range C_{Stray}: pF range
C_{CM}: nF range $C_{DC-link}$: μF to
                          mF range
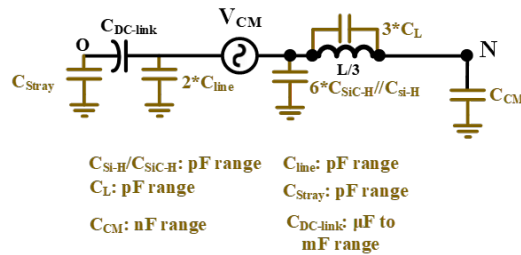
Fig. 3.6: Three-phase 3-L TNPC CMV path

Space vectors in sector 1 of the modulation hexagon, which are shown in Fig. 3.7, are given as an example for CMV calculation. As shown in Table 3.2, small vector V_1 and V_5 have the largest CMV, while zero vector V_8 and medium vector V_3 do not contribute to CMV.

3.3.3 Switching Loss Reduction, NPB, and CM Voltage Analysis for Different SVM Schemes

Firstly, space vectors of sector 1 are marked out in Fig. 3.7 and small vectors' influence on neutral point potential are stated in Table 3.3. For simplicity, the region 3 and 2 are analyzed and compared for three kinds of SVM schemes, choices of small vectors and alignment in the region 1 and 4 are similar to the region 3 and 2. From Table 3.2 it is known that small vectors V_2 and V_4

TABLE 3.3: Small vector's influence on NP potential

Small Vector Angle	Discharge NP	Charge NP
0°	V_4	V_1
60°	V_5	V_2

have lower CM voltage than V_1 and V_5. Less small vectors like V_2 and V_4 are chosen, smaller CM voltage the SVM schemes can get.

1: Connected to positive rail
0: Connected to clamping leg
-1: Connected to negative rail
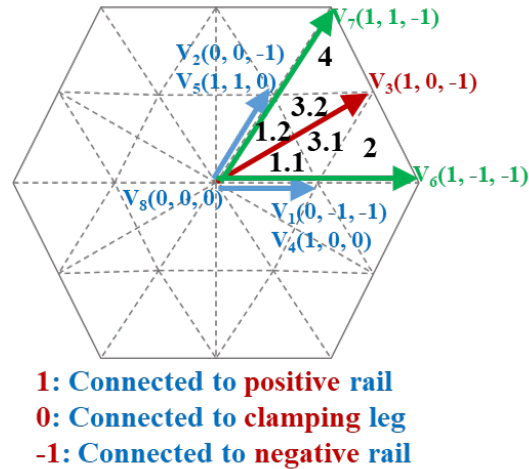
Fig. 3.7: Three-phase three-level space vector hexagon

The region 3 of Sector 1

The space vector choice and alignment for SVM 1, SVM 2, and improved SVM 2 are shown in Table 3.4. For SVM 1 scheme, both of the small vectors V_1, V_2, V_4, and V_5 are used for balancing the neutral point potential, and B phase switching state changes between 1 and 0 plus 0 and -1. Since SVM 1 does not consider the B phase current direction, B phase has hard switching operations on the clamping leg. For SVM 2 scheme, the region 3 is divided into the region 3.1 and the region 3.2 according to B phase voltage polarity. In the region 3.1, only V_1 and V_4 small vectors are used for balancing the neutral point potential. In the region 3.2, only V_2 and V_5 small vectors are used for balancing the neutral point potential. B phase clamping leg is always soft-switching under unity PF. Improved SVM 2 scheme is proposed to reduce the switching loss under the wider power factor range. When the B phase current is negative, V_1 and V_4 small vectors are used for balancing the neutral point potential. V_2 and V_5 small vectors are used when the B phase current is

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TABLE 3.4: Space Vector Choice and Alignment in Sector 3

The region 3 of Sector 1	Discharge NP	Charge NP
SVM 1	V_3-V_2-V_1-V_2-V_3	V_3-V_4-V_5-V_4-V_3
SVM 2 & 0°-30°	V_1-V_2-V_3-V_2-V_1	V_2-V_3-V_4-V_3-V_2
SVM 2 & 30°-60°	V_4-V_3-V_2-V_3-V_4	V_5-V_4-V_3-V_4-V_5
Improved SVM 2 & $I_b < 0$	V_1-V_2-V_3-V_2-V_1	V_2-V_3-V_4-V_3-V_2
Improved SVM 2 & $I_b > 0$	V_4-V_3-V_2-V_3-V_4	V_5-V_4-V_3-V_4-V_5

TABLE 3.5: Space Vector Choice and Alignment in Sector 2

The region 2 of Sector 1	Discharge NP	Charge NP
SVM 1	V_1-V_6-V_3-V_6-V_1	V_6-V_3-V_4-V_3-V_6
SVM 2	V_1-V_6-V_3-V_6-V_1	V_6-V_3-V_4-V_3-V_6
Improved SVM 2	V_1-V_6-V_3-V_6-V_1	V_6-V_3-V_4-V_3-V_6

positive. Improved SVM 2 scheme is basically the same as SVM 2 scheme under the unity power factor, and since it considers the phase current direction for choosing the small vector, and thus, it has lower losses on clamping leg under the non-unity power factor case.

The region 2 of Sector 1

For region 2, modulation strategies of SVM 1, SVM 2, and improved SVM 2 are the same, which are shown in Table 3.5. V_1 and V_4 are chosen to discharge and charge the neutral point voltage, and alignments are V_6-V_3-V_4-V_3-V_6 and V_1-V_6-V_3-V_6-V_1 when the neutral point voltage is lower and higher than half of the DC-link voltage. Soft switching can be achieved on the clamping leg of B phase under the unity power factor.

Summary of Different SVM Schemes

In general, the improved SVM 2 scheme has the lowest switching loss on clamping leg. Moreover, under the non-unity power factor condition, SVM 1 has better neutral point balancing

Switching Energy Information for SiC MOSFETs

Condition:
$V_{GS} = -4V/+15V$
$V_{DD} = 400$ V

Switching Energy Information for Si IGBT

Condition:
$V_{GE} = -4V/+15V$
$V_{DD} = 400$ V

(a) Switching energy information for SiC MOSFET position

(b) Switching energy information for Si IGBT position
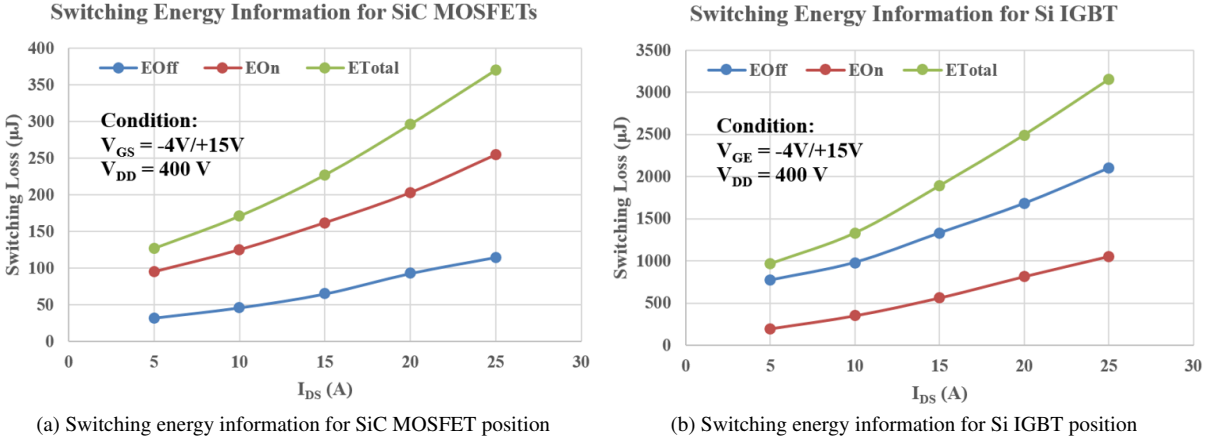
Fig. 3.8: Switching loss information for SiC MOSFET position and Si IGBT position

ability than SVM 2 and improved SVM 2. According to Table 3.2, V1 and V5 have the highest CM voltage. Since SVM 2 and improved SVM 2 exclude V_1 or V_5 for reducing the switching loss, and SVM 1 employs both of the V_1 and V_5 for NPB, SVM 2 and improved SVM 2 have relatively lower CMV than that of SVM 1.

3.4   Experimental Test and Loss Breakdown

A 6 kVA 3-phase 3-L TNPC prototype is built to evaluate the efficiency and CM voltage noise spectrum with different SVM, upper and lower DC-link capacitors are 150 μF each. As shown in Table 3.6, we have chosen 1200 V/ 30 A SiC MOSFET, C3M0075120K from Wolfspeed, and 600 V/ 30 A Si-IGBT IKZ50N65EH5 from ROHM, and FFSH1665A SiC Schottky diode, for experiment validation. Top leg and bottom leg switches are rated for 1.2 kV, and DC-link voltage is set to be 800 V to remain some safety margin. Output RMS voltage is set to 208 V to meet one of the grid standards. Switching frequency is set to be 70 kHz to reduce the passive components' volume. The prototype is composed of three 2-kVA single-phase 3-L TNPC, as shown in Fig.3.9.

30
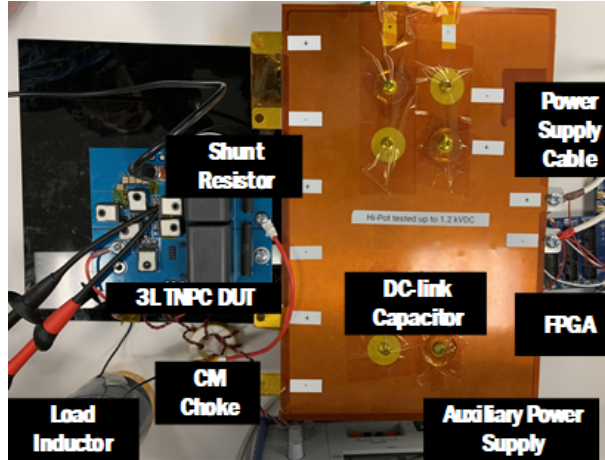
Fig. 3.9: Test setup of DPT

TABLE 3.6: Device Parameters

	Voltage (V)	Current (A)
SiC MOSFET (Wolfspeed-C3M0075120K)	1200	30
Si IGBT (ROHM-RGCL60TS60D)	600	30
SiC Shottky diode (Wolfspeed-C3M0075120K)	650	23

Switching Energy Evaluation of the Three-Level Inverter

Switching energy calculation based on the devices' voltage and devices' current waveform is comprehensively evaluated in [34–36]. DPT is firstly performed to obtain the switching transitions of both SiC MOSFET and IGBT devices. As mentioned in [37], switching energy in 3-L phase leg is different from 2L half-bridge due to the device's junction capacitance, so the double pulse test in this paper is performed based on the single-phase 3-L TNPC platform. In this way, loss analysis using switching energy data from the double pulse test on the 3-L TNPC platform gives more accurate results. The accurate switching energy information for SiC MOSFETs and Si IGBT switch is shown in Fig. 3.8.

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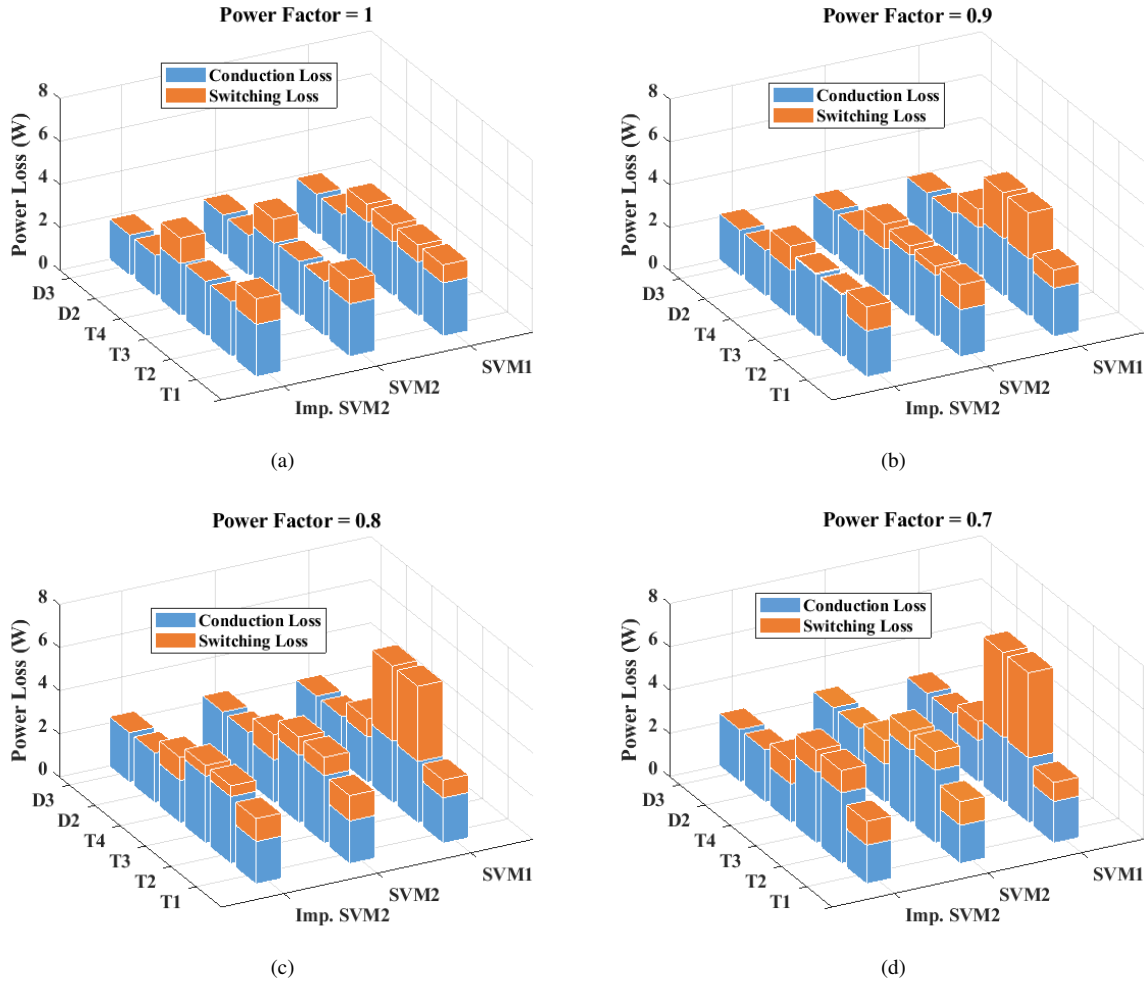
Fig. 3.10: Loss breakdown of semiconductor devices at different power factors: (a) Loss breakdown when PF=1 (b) Loss breakdown when PF=0.9 (c) Loss breakdown when PF=0.8 (d) Loss breakdown when PF=0.7

Semiconductor Loss Breakdown and EMI Performance Evaluation

Switching energy from DPT and device conduction performance in the component datasheet are used, and a detailed semiconductor loss breakdown can be obtained in simulation. While the total power level is 6 kVA, and the switching frequency is 70 kHz.

For the near unity PF case, the loss breakdown for different modulation schemes is listed in Fig. 3.10(a), and total semiconductor loss using SVM 1, SVM 2, and improved SVM 2 are respectively 17.1 W, 16 W, and 16 W. As shown in the diagram, under the unity power factor case,

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total loss of the SVM 2 and the improved SVM 2 are 6.4% lower than using SVM 1. All of the

SVMs have the same neutral point voltage ripple, which is around 2 V due to the hysteresis control

algorithm at half of the switching frequency and switching actions at switching frequency.

However, for PF=0.8 (lead or leg) case, loss breakdown for different modulation schemes

are listed in Fig. 3.10(c), and total semiconductor loss using SVM 1, SVM 2 and improved SVM

2 are respectively 22.7 W, 18.9 W, and 17.9 W. It can be seen that by adopting SVM 1, clamping

leg devices have excessive switching loss. In this condition. SVM2 and improved SVM 2 have

respectively 4.2 times and 5.3 times lower clamping leg devices' switching loss than that of SVM

1. Neutral point ripple voltage using SVM 1, SVM 2, and improved SVM2 are respectively 2.3 V,

8.5 V, and 15 V.

The difference of SVM schemes is the switching transitions and soft-switching conditions

of the clamping leg switches under different conditions, the average duty ratio for each switch does

not change a lot for different SVM schemes. So even the conduction loss of different modulations

have some difference, this difference in conduction loss is not as much as in switching loss, and

it's not obvious in the figures.
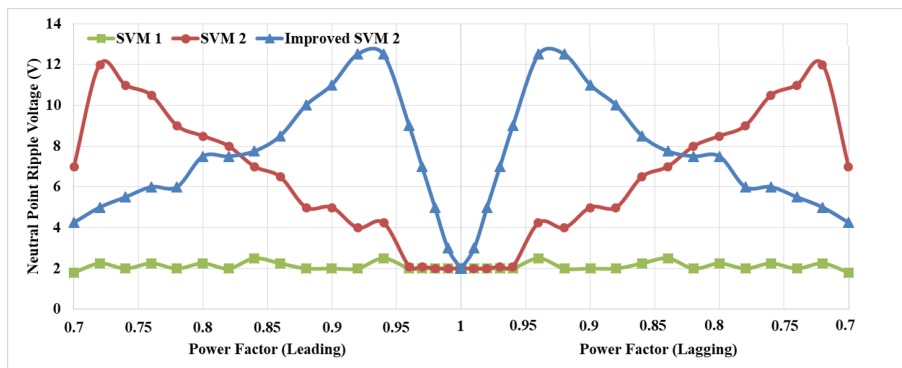
Fig. 3.11: Neutral point ripple voltage

In summary, with the power factor decreasing from 1 to 0.7, SVM 1 has a much higher loss

on clamping leg devices than SVM 2 and improved SVM 2, which may result in device overheat
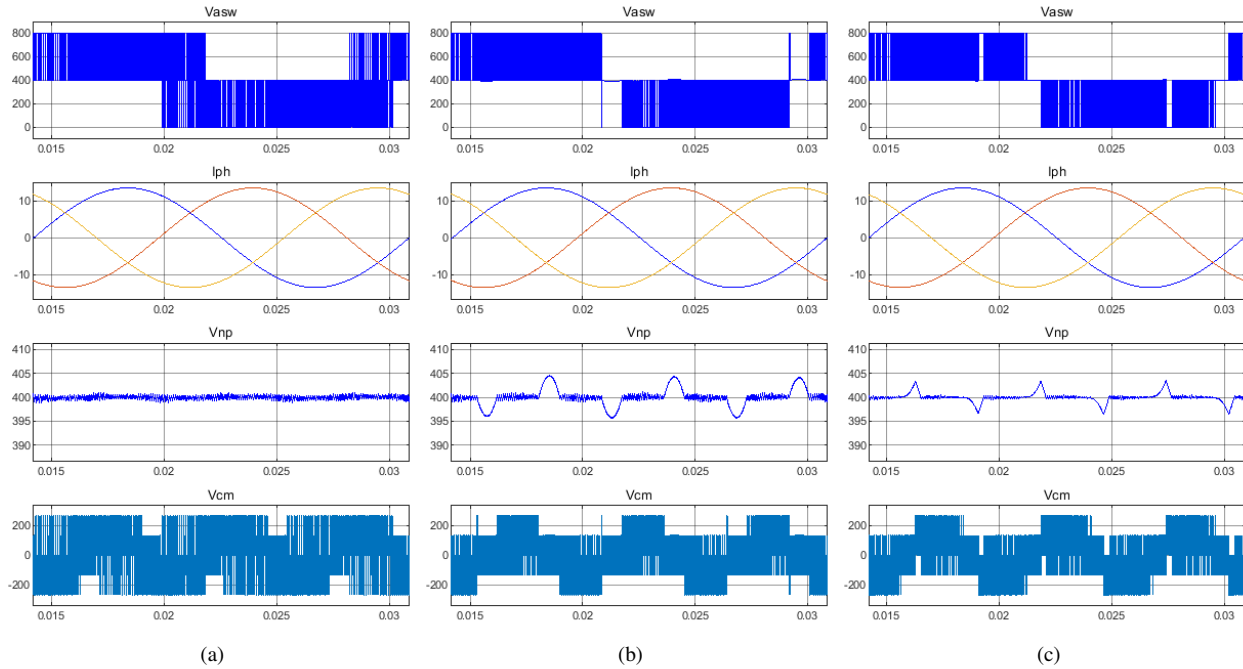
Fig. 3.12: Phase leg output voltage, phase current, NP voltage, and CM voltage waveform when PF=0.8: (a) Waveform for the SVM 1 (b) Waveform for the SVM 2 (c) Waveform for improved SVM 2

issue. And it can be seen in 3.10 that under different power factor cases, SVM 2 and improved SVM 2 have more equal loss distribution among switching devices, so SVM 2 and improved 2 are preferred in terms of semiconductor loss reduction and the semiconductor loss distribution point of view.

The neutral point voltage ripple versus power factor relationship is shown in Fig. 3.11. We can know that when the power factor is in the region of 0.85 to 1 (lead or lag), the SVM 1 and improved SVM 2 have higher neutral point voltage than SVM 2. When the power factor is high enough, SVM 2 also has as good clamping leg loss reduction capability as improved SVM 2. So when the power factor is between 0.85 and 1, it is better to use the SVM 2 modulation scheme for both clamping leg loss reduction as well as NPB purpose.

When the power factor is in the region of 0.7 to 0.85 (lead or lag), the SVM 1 still possesses

the best NPB capability, and in the meantime, the improved SVM 2 has better NPB performance than the SVM 2. Moreover, when the power factor is relatively lower, improved SVM 2 has better clamping leg loss reduction capability than the SVM 2. When the power factor is between 0.85 and 1, the improved SVM 2 serves better for both clamping leg loss reduction and NPB purpose.
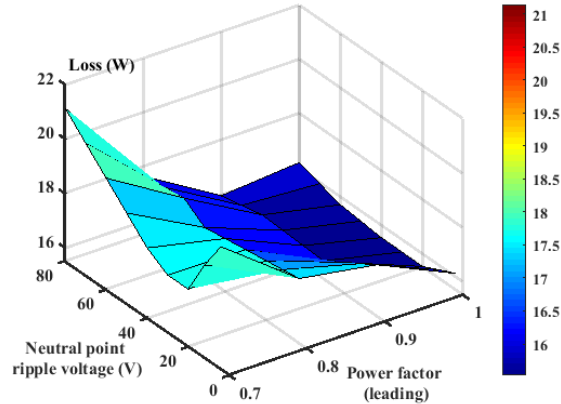
Fig. 3.13: Trade-off between NPB and loss performance for improved SVM 2

As shown in Fig. 3.13, comparison is made for evaluating the trade-off between NPB and loss performance using the improved SVM 2. Hysteresis width for neutral point balancing algorithm is controlled for obtaining different neutral point voltage ripple. It can be seen from Fig. 3.13 that, when neutral point ripple is increasing within a certain range, the total loss is decreasing due to less number of changing space vector alignment actions. However, when neutral point voltage ripple increases, the commutation voltage of the device is higher due to the unbalanced neutral point potential, which deteriorates the loss performance. It is recommended that the hysteresis width should be kept within 30 V for a neutral point balancing control algorithm.

MATLAB simulation has been conducted to compare EMI performance of different SVM schemes. In this simulation, V_{asw} represents the output phase voltage switching waveform, I_{ph} represents the phase current, V_{np} is the NP voltage, and V_{cm} shows the common-mode voltage. As
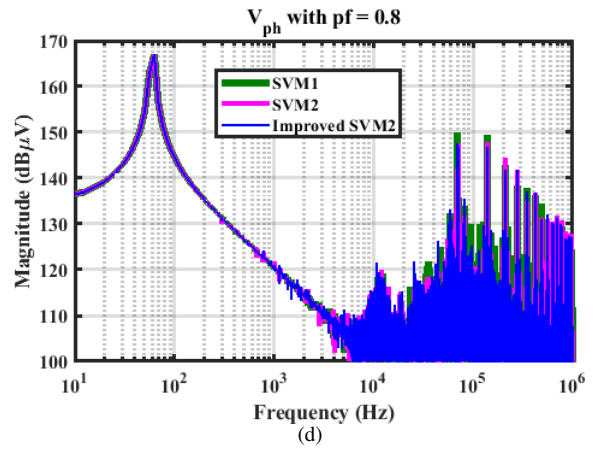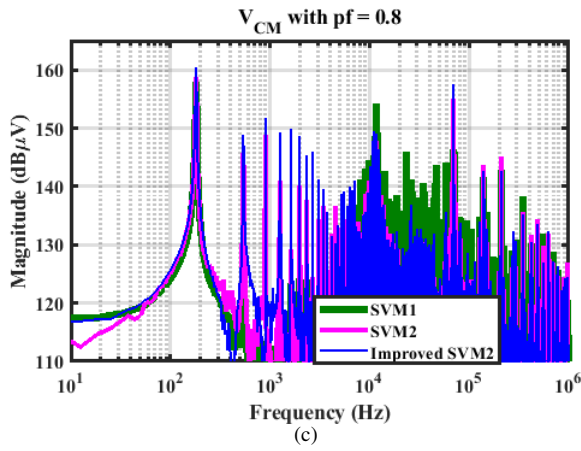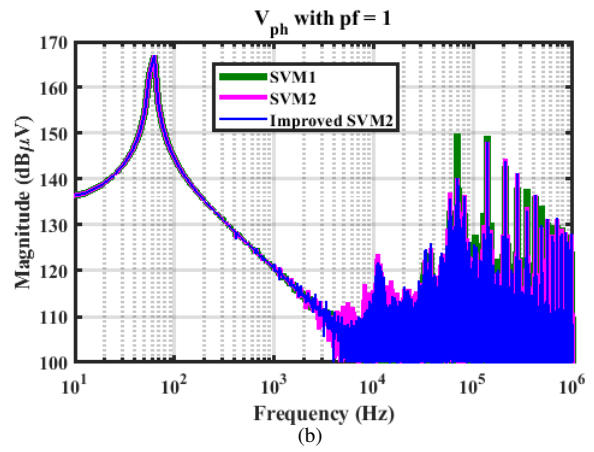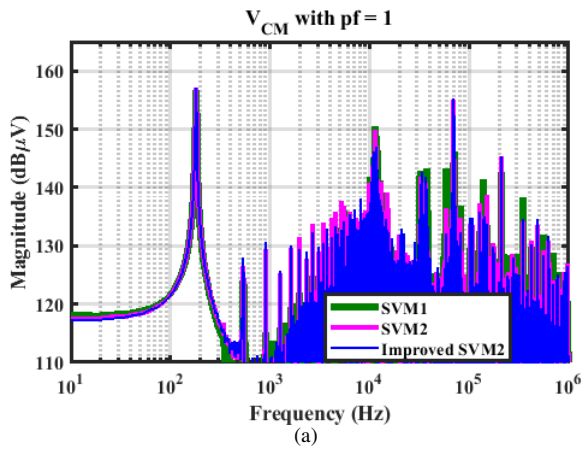
Fig. 3.14: CMV and phase voltage spectrum at different power factors: (a) CMV when PF=1 (b) Phase voltage spectrum when PF=1 (c) CMV when PF=0.8 (d) Phase voltage spectrum when PF=0.8

shown in Fig. 3.12, when PF=0.8, SVM 1 has a higher CM voltage ripple than SVM 2, and improved SVM 2. Under PF=1 and PF=0.8 case, CM voltage and phase leg output voltage spectrum are shown in Fig. 3.14. As shown in Fig. 3.14(a) and Fig. 3.14(c), from 10 kHz to 100kHz range which is of great significance in EMI filter design, SVM 2 and improved 2 have lower CM noise than SVM 1, especially at relatively low power factor case. It is shown in Fig. 3.14(b) and Fig. 3.14(d), since SVM 2, and improved SVM 2 have higher neutral point unbalanced voltage under non-unity power factor, their phase leg voltage has slightly larger harmonics (300 Hz, 420 Hz, etc.) than SVM 1. In terms of common-mode filter and output filter design, SVM 2 and improved SVM 2 are preferred due to their lower common-mode voltage harmonics as well as comparable phase output voltage spectrum.

In summary, SVM 2 and improved SVM 2 have better performance regarding semiconductor loss and common-mode voltage reduction than SVM 1, but SVM 1 has the best neutral point balancing capability. When the power factor is between 0.85 and 1, SVM 2 is adopted for better overall performance, and when the power factor is between 0.7 to 0.85, improved SVM 2 can be utilized for its' overall better loss reduction as well as neutral point balancing performance.

3.5   Conclusion

In this paper, semiconductor losses of different commutation loops in hybrid switch combination TNPC are analyzed and compared. Based on different switching losses of commutation loops, SVM 1 and SVM 2 themes are utilized and compared in this topology comprehensively in terms of their influences on switching loss, NPB and EMI spectrum, and then improved SVM 2 is proposed to further push the converter to higher efficiency at relatively low power factor.

Comparing to SVM 1, SVM 2 and improved SVM 2 schemes have better loss performance

and CM noise performance, while improved SVM 2 scheme has the lowest power loss and lowest CM noise. As for neutral point balancing capability, SVM 1 is better than SVM 2 and improved SVM 2 under non-unity power factor, and their neutral point balancing capabilities are the same under the unity power factor.

Hybrid-switch-based 3 phase 3-L TNPC is comprehensively studied in this paper, and it gives guidance for hybrid switch topology design consideration and the choice of SVM strategy.

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4   Selective Digital Active EMI filtering using Resonant Controller

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Rongxuan Zhang, and Fang Luo

4.1   Abstract

Conventional passive EMI filters are bulky and occupy up to **30**% of converter volume and weight. Active EMI filters are a critical technology that enables a reduction in the size of passive components. The performance of active EMI filters (AEF) with feedback control for volume reduction is limited by relatively low-gain on the feedback loop to ensure stability. A novel digital active EMI filter (DAEF) with the resonant controller, which provides ultra high-gain at frequencies of interest, is demonstrated for DM noise attenuation in this paper. The filter consists of a noise sensing circuit, the resonant controller built in the Field Programmable Gate Array (FPGA), and the noise injection circuit. The experimental test results show that the proposed EMI filter has **45 dB** more attenuation at **150 kHz** than the conventional passive EMI filter, which is also the highest attenuation reported in the DAEF literatures.

4.2   Introduction

Power converters generate conducted EMI noise due to the switching action of the power semiconductor devices [1–3]. Conventionally, a second-order passive EMI filter using an inductor and capacitor, is utilized to mitigate this noise. These passive filters tend to be bulky and could occupy up to 30% of the system volume. Active EMI filters (AEF) could be used to reduce the volume of the passive components. The AEF provides attenuation up to a few Mega Hz, and a smaller passive filter is used to provide high-frequency attenuation. The AEF, along with the

passive filters, is referred to as hybrid EMI filters (HEFs). The AEFs can be classified based on the methodology of control, the active circuits, noise sensing, and noise cancellation mechanisms [4]. Previously, AEFs using feedforward[4], feedback[5–7], and a combination of both control techniques [7] have been demonstrated. Also, AEFs utilizing different voltage or current sensing and cancellation have been demonstrated [8–12]. All these implementations use analog ICs along with passive components for the active circuits, and the performance of single-stage AEFs is limited due to the stability. Recently, DAEFs [13–16] that use DSP/FPGAs in addition to the analog circuitry have been demonstrated. This paper proposes a new control algorithm for single-stage DAEF, which demonstrates higher attenuation than any other previous works in the literature.
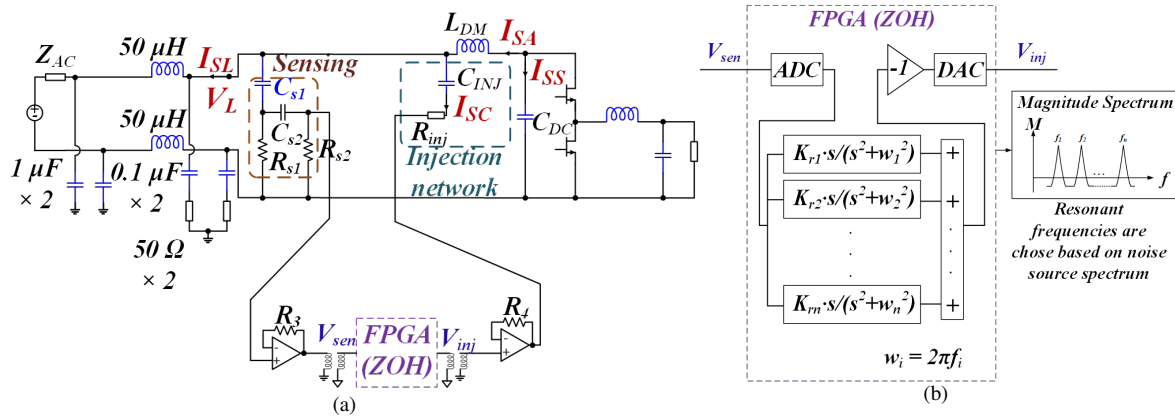
Fig. 4.1: Proposed digital active EMI filter with the resonant controller: (a) Digital active EMI filter based on VSCC topology (b) Resonant controller built in FPGA

A typical implementation of a voltage-sensing current-cancellation (VSCC) digital active EMI filter (DAEF) is shown in Fig. 4.1aa. It comprises of the noise sensing high-pass filter (HPF), the Analog-to-Digital Converter (ADC), the DSP/FPGA, the Digital-to-Analog Converter (DAC), the active circuit, the main passives, and the compensation circuitry. The DSP/FPGA will not be present in an analog-only implementation. The main limitation to the performance of any AEF with feedback compensation is stability. The stability is mainly influenced by the

phase shift introduced by the noise-sensing stage [6] and the noise-processing stage. Particularly, in converters with ac voltage, a second-order high-pass filter is required to separate the sensed noise from the fundamental voltage or current signal. This results in reduced attenuation of the AEF and additional compensation network. Some compensation networks require high-voltage capacitors, thus reducing the volumetric benefits of using an active EMI filter. This limitation is applicable to both analog and digital AEF. In [17] showed how the processing delay in digital AEF affects the attenuation. In [16], it was shown that the previous switching cycle noise could be used to compensate for noise in the next switching cycle to avoid the delay. However, attenuation of only $24\,dB$ could be achieved in the process. This paper proposes an improved digital active EMI filter that uses the resonant controller which achieves improved attenuation without increasing the volume overhead from additional high-voltage components.

The proportional resonant (PR) controller [18, 19] has been widely used in grid-connected inverters, which provides superior performance than the conventional proportional-integral (PI) controller in tracking sinusoidal signals. Ideally, the resonant part of the PR controller provides infinite gain at the frequency of interest, while providing no gain or phase shift at other frequencies. Thus, the resonant controller will be perfectly suitable for the VSCC DAEF application. CISPR 22 [20] class B conducted noise limits, defines EMI test frequency range from $150\,kHz$ to $30\,MHz$. If the resonant controller is to be implemented in the DAEF system, the resonant frequency should be set to be a few $100s$ of kHz, while digital controller discretization frequency should be at least a few $10s$ of MHz for fulfilling the sampling requirement. Therefore, a FPGA instead of a DSP is used for control. The structure of the resonant controller is shown in Fig. 4.1b, multiple resonant controllers are used in parallel at different frequencies for canceling EMI noise at different frequencies.

The contributions of this work are as follows. A novel digital AEF that implements VSCC

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topology using the resonant controller is proposed. The stability analysis of the proposed imple-

mentation is carried out. The discretization and modeling of the resonant controller based VSCC

AEF are demonstrated, and the design methodology for proposed implementation is laid out. By

utilizing the resonant controller in the FPGA, the proposed AEF achieves an attenuation of $46\,dB$

at around $150\,kHz$, which is $25\,dB$ higher than the conventional single-stage active EMI filter. This

is the highest reported attenuation in the literature using single-stage digital or analog AEF.

The organization of the work is as follows. Section II describes the topology that is used

in the implementation. Section III involves the theoretical modeling of proposed VSCC with the

resonant controller. Section IV describes the design example for the proposed concept, and fre-

quency domain measurements using the vector network analyzer (VNA) is performed to verify

the modeling. Section V describes the experimental test setup and discusses the small-signal and

converter test results. Section VI presents the conclusion.

4.3 Active EMI filter Topology and System Level Modeling

Different AEF topologies use either current or voltage sensing and compensation. The

AEF topologies that utilize current-sensing or voltage compensation, current transformers (CTs)

or voltage-injection transformers are needed for implementation. For DM noise, CTs and voltage-

injection transformers can be bulky when the line current is high. Therefore, AEF topologies that

do not have transformers are preferred. The voltage-sense current-cancellation topology requires

high voltage capacitors and other low voltage circuitry for noise sensing and cancellation. In

summary, VSCC topology will maximize the volume reduction for AEFs, and will be used in

this paper. Previously, feedback control based voltage-sense current-cancellation topology was

demonstrated in [6]. However, the attenuation of only $12\,dB$ at around $150\,kHz$ is obtained. This
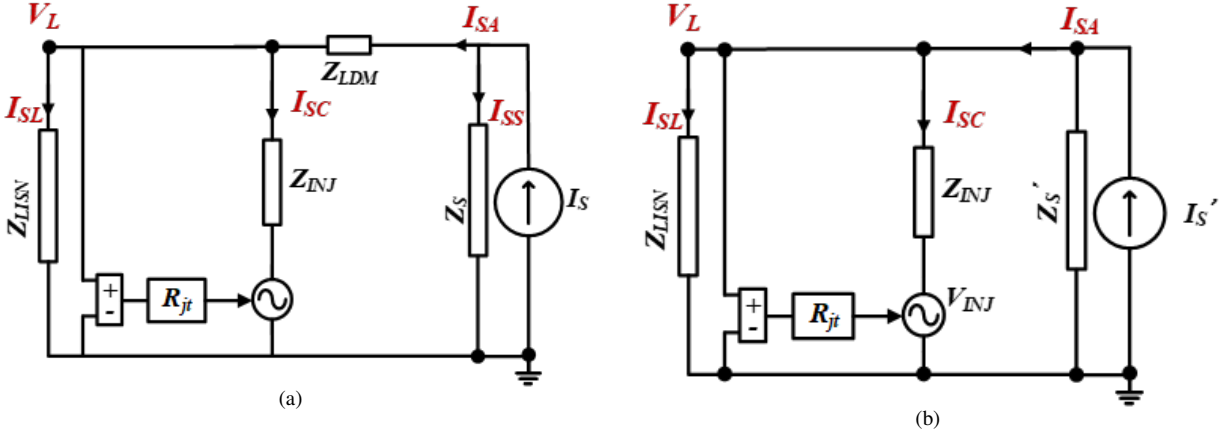
Fig. 4.2: VSCC AEF topology: (a) Simplified VSCC AEF topology (b) Equivalent circuit of VSCC AEF topology

paper utilizes the resonant controller built in FPGA for the feedback loop of the VSCC AEF and achieves $46\,dB$ attenuation at around $150\,kHz$ and is the highest attenuation in reported literatures.

The VSCC AEF topology is shown in Fig. 4.1, and the simplified version of VSCC topology is shown in Fig. 4.2a, where the feedback loop is collapsed into a transfer function R_{jt}. Through Norton and Thevenin's equivalent circuit transformation, the equivalent circuit can be obtained as Fig. 4.2b. I_S is the noise source current, and I'_S represents equivalent noise source current considering the current sharing between the differential-mode noise source impedance (Z_S) and impedance of DM inductor Z_{DM}. The new equivalent noise source (I'_S) and noise source impedance (Z'_S) is given by (4.1) and (4.2), respectively. The AEF cancellation current and noise current on the LISN are represented by I_{SC} and I_{SL}, respectively. The noise voltage on the LISN is represented by V_L.

$$I'_S = \frac{Z_S}{Z_S + Z_{DM}} I_S \tag{4.1}$$
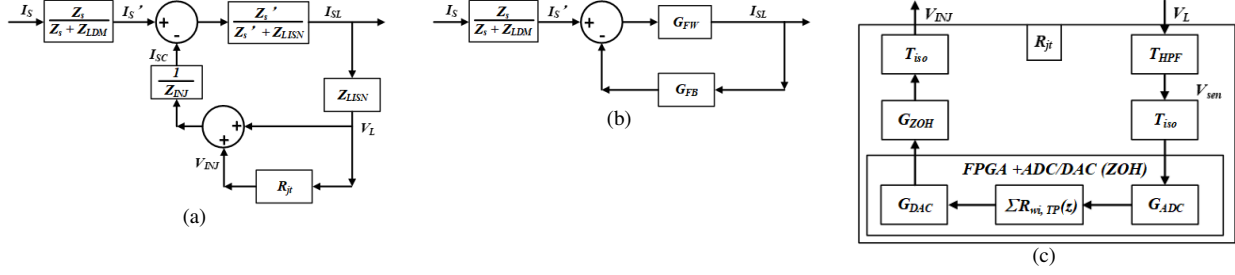
$$Z'_S = Z_S + Z_{DM} \tag{4.2}$$

Fig. 4.3: Block diagram of the VSCC DAEF system: (a) System block diagram (Sensing and FPGA processing stage are collapsed into R_{jt}) (b) Equivalent system block diagram (c) Sensing and FPGA processing stage block diagram

According to Fig. 4.1 and Fig. 4.2b, the block diagram of the VSCC AEF system is shown in Fig. 4.3a. The equivalent system block diagrams is shown in Fig. 4.3b, where $G_{FW}(s)$ and $G_{FB}(s)$ donate the transfer function of the forward and backward loop. Sensing and FPGA processing are collapsed into R_{jt}. The open-loop current gain G_{FW} without the DAEF (R_{js} is disconnected) is given by (4.3). The feedback loop transfer function is given by (4.4). Close-loop current gain G_{CL} with active EMI filter is given by (4.5). The insertion gain G_{IS}, which is defined as the ratio of current flowing through Z_{LISN} with and without active EMI filter, can be derived as (4.6). The open-loop gain is given by (4.7), which will be used for to define the stability margin.

$$G_{FW} = \frac{I_{SL}}{I'_S} = \frac{Z'_S \cdot Z_{INJ}}{Z_{INJ} \cdot (Z'_S + Z_{LISN}) + Z_{LISN} \cdot Z'_S} \tag{4.3}$$

$$G_{FB} = \frac{I_{SC}}{I_{SL}} = R_{js} \frac{Z_{LISN}}{Z_{INJ}} \tag{4.4}$$

$$G_{CL} = \frac{I_{SL}}{I'_S} = \frac{G_{FW}}{1 + G_{FW} \cdot G_{FB}} \tag{4.5}$$

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$$G_{IS} = \frac{G_{FW}}{G_{CL}} = \frac{1}{1 + G_{FW} \cdot G_{FB}} \tag{4.6}$$

$$T_{LG} = G_{FW} \cdot G_{FB} \tag{4.7}$$

The sensing and FPGA processing transfer function R_{jt} is shown In Fig. 4.3c. T_{HPF} denotes the transfer function of the high pass filter, T_{iso} denotes the RF transformer transfer function, G_{ADC} and G_{DAC} denotes the transfer function of ADC sampling stage, $R_{wi,Tp}(z)$ denotes the transfer function of the digitized resonant controller, G_{ZOH} denotes the transfer function of transformation between continuous and discrete domain. Within FPGA, resonant controllers are built in parallel with each other, and the transfer function of R_{js} is given by (4.8). The resonant controller provides high gain at frequencies that match the noise source spectrum. This enables the DAEF to provide high attenuation to the EMI noise at those frequencies. However, the delay introduced by ADC/DAC and the phase introduced by the resonant controller will give rise to the stability issues in the feedback loop.

$$R_{js} = T_{HPF} \cdot T_{iso}^2 \cdot G_{ADC} \cdot G_{DAC} \cdot \sum_{w_i=w_1}^{w_i=w_n} R_{wi,TP}(z) \tag{4.8}$$

4.4 Detailed Modeling of Digital Resonant Controller and Circuit Elements

This section will discuss discretization methods of the resonant controller and detailed modeling of each circuit elements within the VSCC DAEF system, which will provide a guideline for the component value design.

4.4.1 Discretization Methods of Resonant Controller

In [19] showed the influence of different discretization methods on the performance of the resonant controller. Continuous domain expression of the resonant controller is given by (4.9). Forward Euler, zero-order-hold, and the Tustin with prewarping discretization expressions for the resonant controller are given in (4.10), (4.11), and (4.12), respectively. w_i denotes the resonant frequency, and T_s denotes the digization step.

$$R_{wi}(s) = \frac{K_r s}{s^2 + w_i^2} \tag{4.9}$$

$$R_{wi,FE}(z) = \frac{K_r T_s \cdot (z^{-1} - z^{-2})}{1 - 2z^{-1} + z^{-2}(1 + w_i^2 T_s^2)} \tag{4.10}$$

$$R_{wi,ZOH}(z) = \frac{K_r sin(w_i T_s)/w_i \cdot (z^{-1} - z^{-2})}{1 - 2z^{-1} cos(w_i T_s) + z^{-2}} \tag{4.11}$$

$$R_{wi,TP}(z) = \frac{K_r sin(w_i T_s)/(2w_i) \cdot (1 - z^{-2})}{1 - 2z^{-1} cos(w_i T_s) + z^{-2}} \tag{4.12}$$

A comparison of different discretization methods is given in Fig. 4.4, where Ts is $10\,ns$ (corresponding to the sample rate of the FPGA), and the resonant frequency is $150\,kHz$. Within a small frequency range, the gain and phase of the resonant controller with continuous domain function, zero-order-hold, and the Tustin with prewarping discretization are matching well, all of which provide very high gain at the resonant frequency. However, the resonant controller with the forward Euler discretization method has minimal gain at the resonant frequency and is therefore
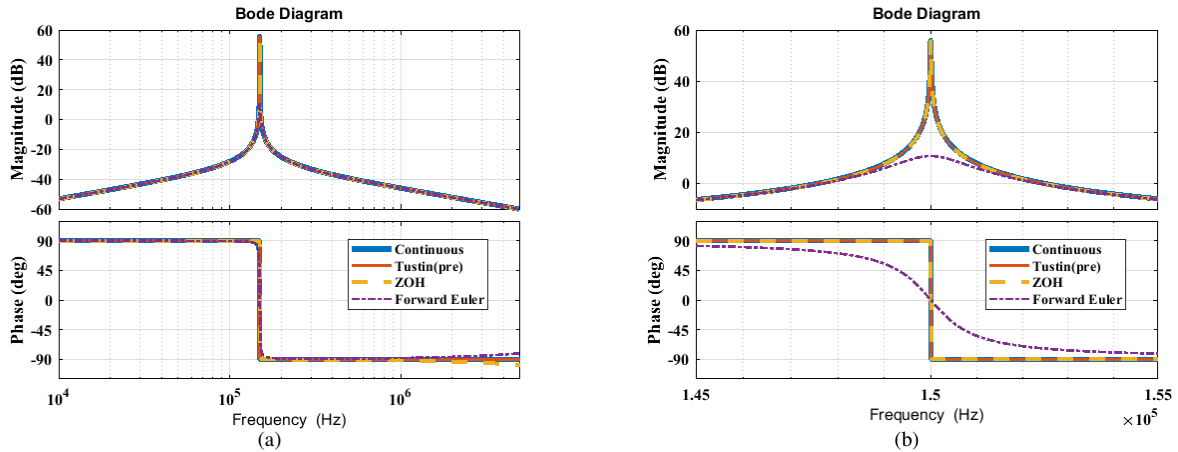
Fig. 4.4: Gain and phase comparison of different discretization methods: (a) Comparison within 10 kHz to 10 MHz (b) Comparison within 145 kHz to 155 kHz

not preferred in the real application. At higher frequencies, the resonant controller with zero-order-hold discretization methods has an undesired phase shift. Whereas, the resonant controller with the Tustin with prewarping discretization method matches better with continuous domain expression at all frequencies. Thus, the resonant controller using the Tustin with prewarping discretization method is chosen for the digital active EMI filter.

4.4.2   Gain Selection for Resonant Controller

As discussed above, the resonant controller using the Tustin with prewarping discretization methods matches pretty well with the continuous domain expression. The continuous domain expression will be used in this section to discuss the factors that affect the performance of the resonant controller.

The selection of gain at different resonant frequencies is dependant on the clock accuracy for pulse width modulation (PWM), the accuracy of the resonant controller itself within the FPGA, and the fundamental frequency of output current if the noise source is an inverter. Assuming the resonant frequency of the resonant controller is w_i, and the frequency variation caused by the PWM

clock accuracy or calculation accuracy is Δw_i (either positive or negative). The amplitude of the resonant controller at $w = w_i + \Delta w_i$ frequency is given by (4.13). The lower limit of gain value selection is given by (4.14), where dB_{rsd} denotes the desired amplitude residue of the resonant controller at $w = w_i + \Delta w_i$ frequency. The higher limit of gain value is given by (4.15), which limits the bandwidth of resonance within $w_i - 0.05w_i$ to $w_i + 0.05w_i$. This is essential to ensure that the resonant controller will not create stability issues when multiple resonant controllers are used in parallel.

$$|R_s(w_i + \Delta w_i)| = \left| \frac{K_{r,i}}{-2\Delta w_i + \frac{\Delta w_i^2}{w_i + \Delta w_i}} \right| \tag{4.13}$$

$$|R_s(w_i + \Delta w_i)| > 10^{\frac{dB_{rsd}}{20}} \tag{4.14}$$

$$|R_s(w_i \pm 0.05w_i)| \approx \frac{10K_{r,i}}{w_i} < 2 \tag{4.15}$$

4.4.3 Modeling of The High Pass Filter

The converter that uses this filter could be fed from ac or dc supply. Either way, the noise-sensing stage has to sufficiently attenuate any $60\,Hz$ ac voltage and its harmonics, and the high-frequency currents due to rectifier operation or any other converters connected to the same node. Otherwise, any low-frequency harmonics can easily saturate the output of the active circuits. Ideally, the output of the high pass filter should only include the switching frequency and its harmonics in the desired EMI frequency range ($150\,kHz$ to $30\,MHz$). The design of the sensing network requires careful consideration to ensure that it:

1. has the desired performance throughout the entire frequency range and

2. it does not add too much to the volume of the filter

It is not possible to get high attenuation at $60\,Hz$ with a 1st order high pass filter. Therefore a 2nd order high pass filter is used as the sensing network. The capacitor C_{s1} needs to be rated for the input voltage and needs to be safety rated (X1Y1 rated). The other components C_{s2}, R_{s1} and R_{s2} are low voltage and low power components. The capacitor C_{s2} is a 50 V rated X7R surface mount capacitor. The transfer function of the filter is given by (4.16) $\sim$ (4.18). The output of the high pass filter is buffered (op-amp configured as a voltage follower) and fed to ADC. The selected op-amp is unity-gain stable with a gain-bandwidth of about $500\,MHz$. Therefore, the output of the buffer could be assumed to be the same as that of the high pass filter.

$$T_{HPF} = \frac{s^2}{s^2 + k_1 s + k_2} \tag{4.16}$$

$$k_1 = \left(\frac{1}{C_{s1}R_{s1}} + \frac{1}{C_{s1}R_{s2}} + \frac{1}{C_{s2}R_{s2}} \right) \tag{4.17}$$

$$k_2 = \frac{1}{C_{s1}C_{s2}R_{s1}R_{s2}} \tag{4.18}$$

4.4.4 modeling of the ADC and DAC Sampling System

According to [21], the RF transformer used in the sampling system for matching the impedance on termination, the transfer function can be modeled as (4.19). The characteristic of the RF transformer is simply a bandpass filter, which has the first corner frequency w_1 at around $20\,kHz$ and the second corner frequency w_2 at around $200\,MHz$.

$$T_{iso} = \frac{1}{(1 + w_1/s) \cdot (1 + s/w_2)} \tag{4.19}$$

[22] presented the model of the discrete sampling system, the transfer function of transformation between continuous and discrete domain is given in (4.20), where T_s represents the digitization step.

$$G_{ZOH} = \frac{1 - e^{-sT_s}}{sT_s} \tag{4.20}$$

The ADC and DAC models are given in (4.21) and (4.22), where m and n denote the bit width of ADC and DAC, V_{ADC} and V_{DAC} denote the range of ADC and DAC, n_{ADC} and n_{DAC} donate the clock latency of ADC/DACs. For most of the off-the-shelf ADC/DACs, there is clock latency around 5 to 15 clock cycles.

$$G_{ADC} = \frac{2^m}{V_{ADC}} \cdot z^{-n_{ADC}} \tag{4.21}$$

$$G_{DAC} = \frac{V_{DAC}}{2^n} \cdot z^{-n_{DAC}} \tag{4.22}$$

4.5 Design Example of the Proposed Concept and VNA Measurement for Stability Analysis

In this section, the AEF system's parameters for the design example will be given or derived based on previous chapters, and then, the open-loop gain and close loop gain modeling and VNA measurement will be conducted.

The noise source is a DC-DC converter, the output filter components' parameters are

$L = 70 \ \mu H$ and $C = 5 \ \mu F$. The switching frequency of the DC-DC converter is $50 \, kHz$, and it realizes 12 to $5V$ conversion. The inductance value of the DM inductor is $L_{DM} = 131 \ \mu H$, and the capacitance value of the DM capacitor is $C_{INJ} = 470 \ nF$.

The gain for the resonant controller ($K_{r,i}$) is selected based on (4.13) $\sim$ (4.15). For example, for a DC-DC converter, which switching frequency is $50 \ kHz$, and resonant controller at $150 \, kHz$ is to be designed for DAEF. Assuming the $150 \, kHz$ noise will have $\pm 300Hz$ variation. Furthermore, $30 \, dB$ amplitude residue (dB_{rsd}) at $150kHz \pm 300 \ Hz$ is to be ensured. According to (4.14), the lower limit of the gain K_i can be calculated as $1.9 \cdot 10^4$. According to (4.15), the higher limit of K_i can be calculated as $3 \cdot 10^4$. So the value of the resonant controller's gain K_i should satisfy $1.9 \cdot 10^4 < K_i < 3 \cdot 10^4$.

For the second order high pass filter, the components' values are: $C_{s1} = 4.7 \ nF$, $C_{s2} = 10 \ nF$, $R_{s1} = 3.3 \ k\Omega$ and $R_{s2} = 3.3 \ k\Omega$. According to (4.16) $\sim$ (4.18), two corner frequencies of the high pass filter can be calculated as $700 \, Hz$ and $7 \, kHz$. The attenuation of $60 \, Hz$ signal is around $35 \, dB$, which will make sure that the line frequency voltage variation will not saturate the ADC sampling.

The proposed concept is implemented using Intel Cyclone IV FPGA in a Terasic DE2-115 demo board, and the operating frequency is set to $100 \, MHz$, so the discretization time step is $T_s = 10 \, ns$. In the configuration, the ADC AD9254 [23] has around 4 ns of propagation delay and 12 cycles of clock latency. Since the ADC is using the same clock as that of the FPGA, the propagation delay can be ignored, and totally 13 cycles of clock latency exist in ADC sampling. The same concept can be applied to DAC DAC5672 [24] model. In equation (4.21) and (4.22), the n_{ADC} and n_{DAC} values can be acquired as (4.23).

$$n_{ADC} = 14, \quad n_{DAC} = 5 \qquad (4.23)$$

Based on $(4.3) \sim (4.8)$, the loop gain of the proposed configuration of AEF without the resonant controller can be expressed as (4.24). The first round of loop gain and phase measurement should be done by replacing the resonant controller with unity gain transfer function, which is described as (4.7). The loop gain measured from the circuit under test as well as loop gain calculated from modeling are shown in Fig. 4.5. From $70\,kHz$ to $20\,MHz$, the model matches pretty well with the measurement, the discrepancy of the low-frequency and high-frequency gain/phase might be caused by the inaccuracy of the model of the RF transformer.

$$T_{LG,w/o\,res} = G_{FW} \cdot \frac{Z_{LISN}}{Z_{INJ}} \cdot T_{HPF} \cdot T_{iso}^2 \cdot G_{ADC} \cdot G_{DAC} \qquad (4.24)$$
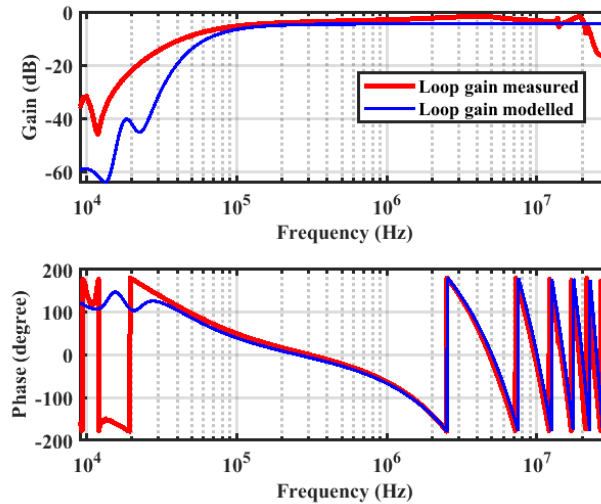

Fig. 4.5: Loop gain without resonant controller

In order to understand each part of the circuit's effects on stability, the bode plot of each function is shown in Fig. 4.6. As shown in the figure, in the frequency range of 9 kHz to 300 kHz,

the $G_{FW}Z_{LISN}/Z_{INJ}$ transfer function and high pass filter T_{HPF} transfer function is providing gain attenuation and phase lead. In the high-frequency range (above $300\,kHz$), the gain of each transfer function will be maintaining stable, but the G_{ADC} and G_{DAC} will have tremendous phase lag due to the clock latency.
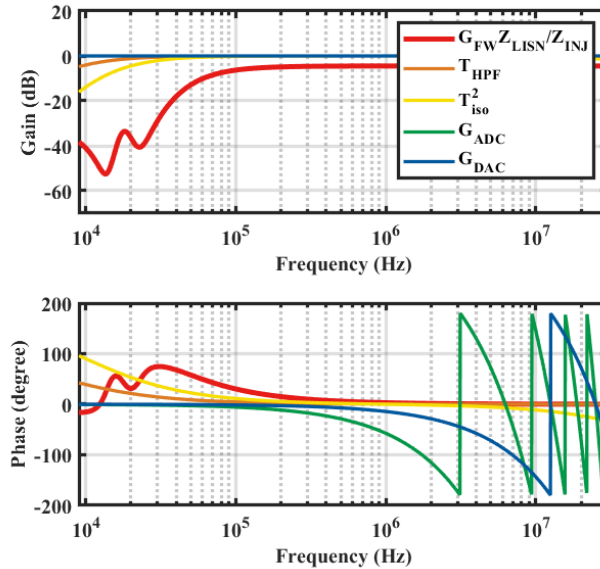

Fig. 4.6: The bode plot of each transfer function.

Gain and phase of the loop gain without the PR controller is of great significance in determining where the digital PR controller can be implemented. As shown in Fig. 4.4b, the resonant controller will introduce 90° lead/lag. In order to make sure that the entire loop gain with the resonant controller implemented is stable, the original phase of the loop gain without PR controller should be within ±90°. Otherwise, phase compensation should be implemented together with the resonant controller. As shown in Fig. 4.4b, to remain 25° phase margin, $65\,kHz$ to $950\,kHz$ frequency range is available for implementing the resonant controller without any phase compensation.

Assuming the noise source is a converter/inverter operating at $50\,kHz$ switching frequency,

then the noise source will contain $k_i \cdot 50\,kHz$ noise and its harmonics. CISPR 22 defined the conducted emission limit from $150\,kHz$ to $30\,MHz$, so the resonant controller's frequencies are selected as $i \cdot 50kHz$ where i ranges from 3 to 19. Gain selection for the resonant controller is done by using (4.14) and (4.15). After carefully designing the resonant frequencies and gains, the loop gain incorporating resonant controller is obtained in Fig. 4.7. As it can be seen from the loop gain measurement, the phase margin at the highest frequency is exactly $25°$, which matches well with previous analysis.
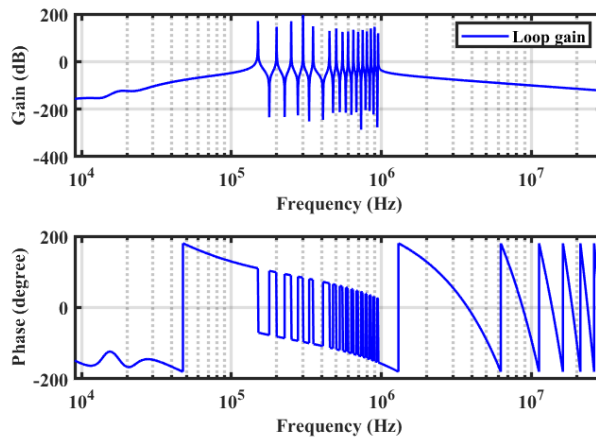

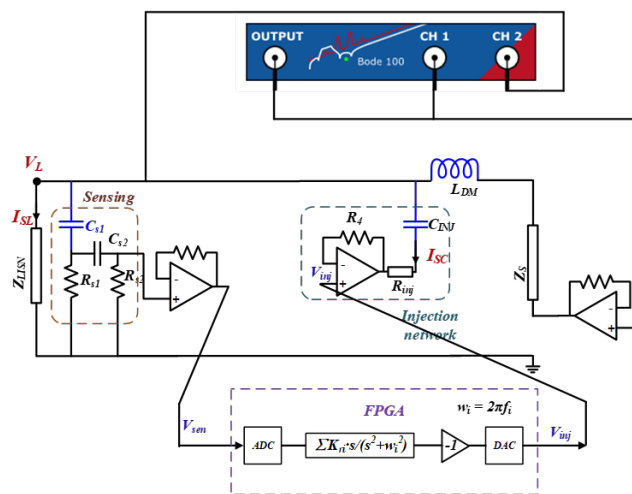**Fig. 4.7**: Loop gain with the resonant controller

Fig. 4.8: Insertion loss measurement setup

The insertion loss measurement is carried out using a VNA (Bode-100) is shown in Fig.
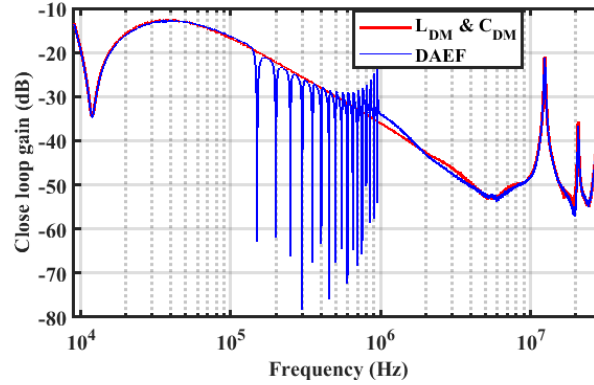
**Fig. 4.9**: Insertion loss measurement of DAEF implementation

4.8, and the measurement result is shown in Fig. 4.9. The figure shows that the insertion loss at $150\,kHz$ is enhanced by about $45\,dB$ using the resonant controller. The insertion loss is high at harmonics of $50\,kHz$ (n = 3, 4, ..., 19).
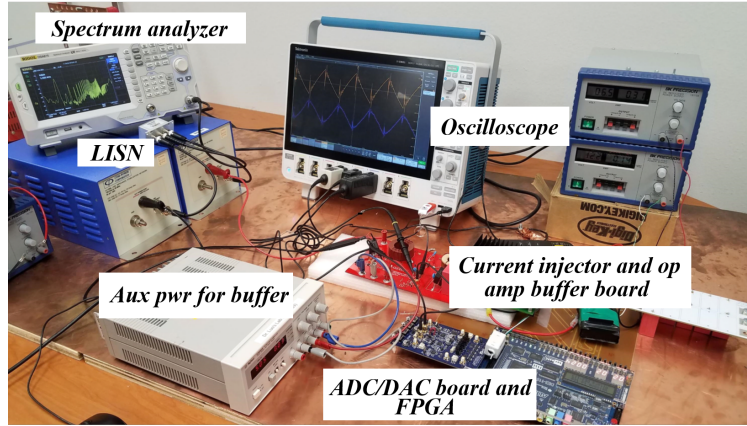
4.6 Experimental Results

The filter discussed above is implemented in the experiment. The proposed resonant controller is implemented in the FPGA (Intel Cyclone IV FPGA in a Terasic DE2-115 demo board along with a Terasic AD/DA daughter card with a sample rate of $100\,MHz$). Apart from the filter, the noise is measured at the LISN using an EMI receiver.

4.6.1 Small-Signal EMI Test

In the small-signal measurement, a function generator along with a buffer is used as the noise source, and D = 0.5 and D = 0.3 are implemented and tested. The EMI receiver measurement is shown in Fig. 4.11a and the attenuation at $150\,kHz$ with the active EMI filter is about $45\,dB$, which is the highest attenuation reported in any active EMI filter literature, both analog and digital active EMI filters. As for D = 0.3 condition, harmonics of $50\,kHz$ (n = 3, 4, ..., 19) is attenuated
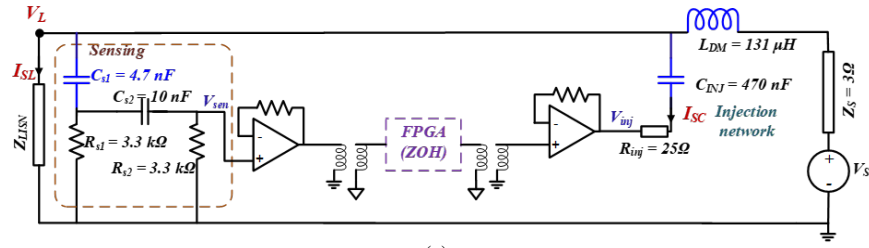
Fig. 4.10: Experiment setup: (a) Equivalent circuit for experiment setup (b) Picture for experiment setup

down to noise floor as well.

4.6.2 Converter EMI Test Results

In the converter EMI test, the noise source is a buck converter which converts voltage from $12\,V$ to $5\,V$, and the switching frequency is $50\,kHz$, the output current is $1\,A$. As shown in Fig. 4.12, the EMI noise at $150\,kHz$ is attenuated $37\,dB$ by using AEF, and all the other harmonics between $150\,kHz$ to $950\,kHz$ are attenuated to the noise floor. The performance of the proposed DAEF is the best among all reported literature.

Conclusion

The performance of conventional digital active EMI filters is limited by the delay introduced by the ADC/DAC. The best attenuation reported in the literature is $24\,dB$ at $150\,kHz$. This
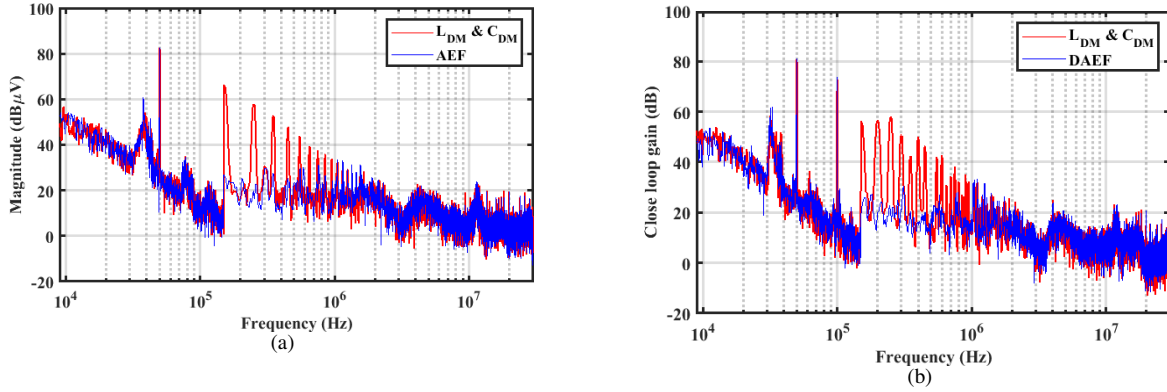
(a)

(b)

Fig. 4.11: Small-signal test of proposed DAEF under different noise source condition: (a) Test under D = 0.5 condition (b) Test under D = 0.3 condition
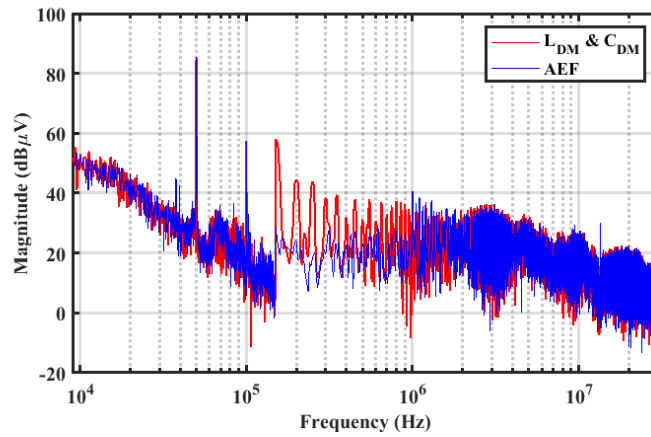

Fig. 4.12: Converter EMI test result

paper proposes a new method to combine the resonant controller along with the digital active EMI filter to improve the attenuation by another $20\,dB$. Design and modeling of the proposed DAEF are discussed, small-signal experimental results, as well as converter test results, have confirmed the validity of the proposed method.

4.7 Acknowledgment

4.8 Bibliography

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5   Conclusion and Future Work

Based on the work mentioned above, the major challenges of the 3 phase 3-L TNPC system building and control have been identified. However, for the system level design, the switching loop optimization and the current sharing strategy have not been discussed. The modulation technology, which introduced in Chapter 2, has not been implemented into hardware prototype yet. For the active EMI filter, the proposed configuration has not been implemented into inverter topology, and a proportional part may also need to be included for better bandwidth. The following are the needs for future work and research:

1. Extend the system-level optimization to power stage hardware design as well as the device paralleling design. A thermal solution for the hardware also needs to be investigated.

2. The proposed modulation and control technology needs to be implemented to hardware for better evaluation and understanding.

3. The active EMI filter needs to be implemented into inverter topology, and proportional part needs to be introduced.

4. Active EMI filter can be integrated into higher power level converter, further information for OPAMP selection, high power design needs to be discussed,

A   List of published and submitted work

1. H. Peng, Z. Yuan, B. Narayanasamy, X. Zhao, A. Deshpande and F. Luo, "Comprehensive Analysis of Three-phase Three-level T-type Neutral-Point-Clamped Inverter with Hybrid Switch Combination," *2019 IEEE 10th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Xi'an, China, 2019, pp. 816-821. doi: 10.1109/PEDG.2019.8807618

2. H. Peng et al., "Improved space vector modulation for neutral-point balancing control in hybrid-switch-based T-type neutral-point-clamped inverters with loss and common-mode voltage reduction," in *CPSS Transactions on Power Electronics and Applications*, vol. 4, no. 4, pp. 328-338, Dec. 2019, doi: 10.24295/CPSSTPEA.2019.00031.

3. H. Peng, B.Narayanasamy, Z.Yuan, A. Imran and F. Luo, "Selective Digital Active EMI filtering using Resonant Controller", submitted for review in *IEEE Transactions on Power Electronics*, **Under review**

4. H. Peng et al., "Practical Design and Evaluation of a High Efficiency 30-kVA Grid Connected PV Inverter with Hybrid Switch Structure", accepted for publication in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*

5. Z. Yuan et al., "Design and Evaluation of Laminated Busbar for Three-Level T-Type NPC Power Electronics Building Block With Enhanced Dynamic Current Sharing," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 395-406, March 2020, doi: 10.1109/JESTPE.2019.2947488.

6. B. Narayanasamy, H. Peng, A. Imran and F. Luo, "Modeling and Analysis of a Differential-Mode Active EMI Filter with an Analog Twin-circuit," accepted for publication in *IEEE Transactions on Electromagnetic Compatibility*.

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