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An 8-Bit Analog-to-Digital Converter for Battery Operated Wireless Sensor Nodes

Marvin Wayne Suggs Jr.
University of Arkansas, Fayetteville

An 8-Bit Analog-to-Digital Converter for Battery Operated Wireless Sensor Nodes

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Marvin Wayne Suggs Jr.
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_____
H. Alan Mantooth, Ph.D.
Thesis Director

_____   _____
Zhong Chen, Ph.D.   Jeff Dix, Ph.D.
Committee Member   Committee Member

Abstract

Wireless sensing networks (WSNs) collect analog information transduced into the form of a voltage or current. This data is typically converted into a digital representation of the value and transmitted wirelessly using various modulation techniques. As the available power and size is limited for wireless sensor nodes in many applications, a medium resolution Analog-to-Digital Converter (ADC) is proposed to convert a sensed voltage with moderate speeds to lower power consumption. Specifications also include a rail-to-rail input range and minimized errors associated with offset, gain, differential nonlinearity, and integral nonlinearity. To achieve these specifications, an 8-bit successive approximation register ADC is developed which has a conversion time of nine clock cycles. This ADC features a charge scaling array included to achieve minimized power consumption and area by reducing unit capacitance in the digital-to-analog converter. Furthermore, a latched comparator provides fast decisions utilizing positive feedback. The ADC was designed and simulated using Cadence Virtuoso with parasitic extraction over expected operating temperature range of $0 - 85°C$. The design was fabricated using TSMC's 65 nanometer RF GP process and tested on a printed circuit board to verify design specifications. The measured results for the device show an offset and gain error of +7 LSB and 31.1 LSB, respectively, and a DNL range of -0.9 LSB to +0.8 LSB and an INL range of approximately -4.6 LSB to +12 LSB. The INL is much improved in regard to the application of the temperature sensor. The INL for this region of interest is from -3.5 LSB to +2.8 LSB.

Dedication

  I would like to dedicate this thesis to my parents, Marvin and Wanda Suggs for your love and support throughout my time in school. You never fail to let me know that you love me and are there for me when needed. Thanks to my sisters, who are always encouraging and supporting me when needed.

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Chapter 1: INTRODUCTION

1.1 Thesis Structure

This thesis is divided into the following chapters. A brief description is given outlining the overview of the chapter.

- Chapter 1: Introduction – This chapter gives the motivation of this work and an introduction to the general concept of analog-to-digital conversion.

- Chapter 2: Background – This section gives the definition of key terms and gives outlook on a few ADC topologies.

- Chapter 3: Circuit Design and Simulation – The circuit design of the complete system and various sub-blocks are presented here along with their simulation results.

- Chapter 4: Testing and Characterization – This chapter covers the testing of the fabricated device along with the measured results.

- Chapter 5: Future Improvements - Suggestions for revisions in the circuit design to improve the device performance are given.

- Chapter 6: Conclusions– A summary of the fabricated device performance and learnings are given.

1.2 ADC Application

The intrinsic world we live in is indeed analog, as signals such as temperature, pressure, distance, voltage and numerous other parameters can be defined holistically. The human voice for instance is an analog wave and is radiated using an immeasurable number of steps between pitches and amplitude of the emitted sound. Even this sound wave captured by the best oscilloscopes on the market will only represent a finite sample of the true analog wave produced.

Wireless sensor nodes are a subset of Internet of Things (IOT) that can be applied to many new interesting applications. Sensors are data transducers that can be utilized in applications from measuring a temperature or pressure to detecting light or moisture. The ability to transfer this data wirelessly enables convenient access to information about the application of interest. In this particular application, we want to extract temperature data from inside a corn stalk and transmit this data wirelessly. To capture this data, an analog-to-digital converter is utilized to convert this data into a binary code that can be used with common modulation schemes to transmit the data to the end user.

Although analog signals reproduced by technology are not perfect, they can be represented by high resolution, discrete digital signals that allow us to get close. Digital signals are needed to be able to represent an infinite amount of data into a discrete form so that the devices that humans interface with, such as a computer or smartphone, can process this data. Also, to connect with the outside world, transducers are needed to convert physical phenomena such as pressure, temperature or light to an electrical signal and determine useful information. With this electrical signal, we can use analog-to-digital conversion techniques to represent transduced data in discrete bits that inherently include some error. Depending on the application, the resolution of this digital signal is determined by the quality of the signal needed to sufficiently capture the parameter being measured.

In the application associated with this thesis, temperature data will be transduced and converted to a digital signal able to be transmitted wirelessly for post-processing. This functionality supports the development of a wireless sensor node to be used for remote monitoring of parameters in crops for agricultural applications. As ambient temperature tends to be fairly slow changing, temperature sensor data transduced in the form of an analog voltage will vary slowly as

well. Furthermore, it is expected that only six or less temperature measurements will be taken throughout the day to feed machine learning algorithms that will eventually develop into predictive models concerning plant growth and productivity. With these models, producers will have information at their fingertips that will not only help reduce environmental stresses but also conserve resources.

Chapter 2: BACKGROUND

To familiarize the reader with the basic terms associated with analog-to-digital converters, some key terms will be reviewed.

Reference Voltage – The reference voltage are the values in terms of the amplitude of input voltages that the ADC can convert to a digital signal. For this converter, the minimum and maximum reference voltages are 0V to 1.8V, respectively.

Resolution – Defined as the minimum step size the converter can detect in the reference voltage, the resolution determines how well the discrete output codes represent the analog input signal. The resolution can be expressed in number of bits or by the minimum input voltage step size. For an N-bit converter, the theoretical minimum step size is defined as the reference voltage divided by 2^N.

Quantization Error – This error represents the inherent error in all converter topologies based on the finite resolution of analog-to-digital conversion. This error introduces noise to the sample signal due to the process of mapping an infinite number of input values to a finite number of output codes.

Offset Error – Expressed in LSB, the offset error is the difference in the ideal first transition voltage and the actual first transition voltage. This ideal transition is usually defined for ½ of the reference voltage for the least significant bit.

Full-Scale Error – Also commonly measured in LSB, the full-scale error is the difference in the actual and ideal full-scale transition value. For an 8-bit ADC, this corresponds to output code 255.

Gain Error – The gain error can be defined as the difference between the full-scale error and the offset error.

Differential Non-linearity (DNL) – The deviation in input values that map to adjacent digital output codes. Ideally, each digital code is 1 LSB wide.

Integral Non-linearity (INL) – The INL is the deviation of the mid-points of the quantization steps from the ideal transfer function.

For analog-to-digital conversion, there are several topologies to consider depending on the application. Tradeoffs between error, accuracy, speed, power consumption and design complexity need to be made in order to determine a suitable design that meets specifications most resourcefully. As accuracy increases, so does the number of bits, which may give a designer more incentive to choose a dual-slope converter over other topologies for a high resolution digital acoustic system. Where speed is of importance, flash ADCs are utilized for applications such as radar detection, electronic test equipment and optical communication. To give perspective on the right converter for this application, three topologies of converters are discussed here including flash, sigma-delta, and successive approximation converters.

Flash ADCs are typically used in high-speed applications; hence the name "flash". The ability to use high sampling speeds can be a significant figure of merit considering the application. Given a high frequency analog signal, flash ADCs have the ability to perform the conversion with only a short delay which gives it a significant speed advantage over some other topologies. To illustrate, an example of a typical 3-bit flash converter is shown in Figure 2.1 [1].
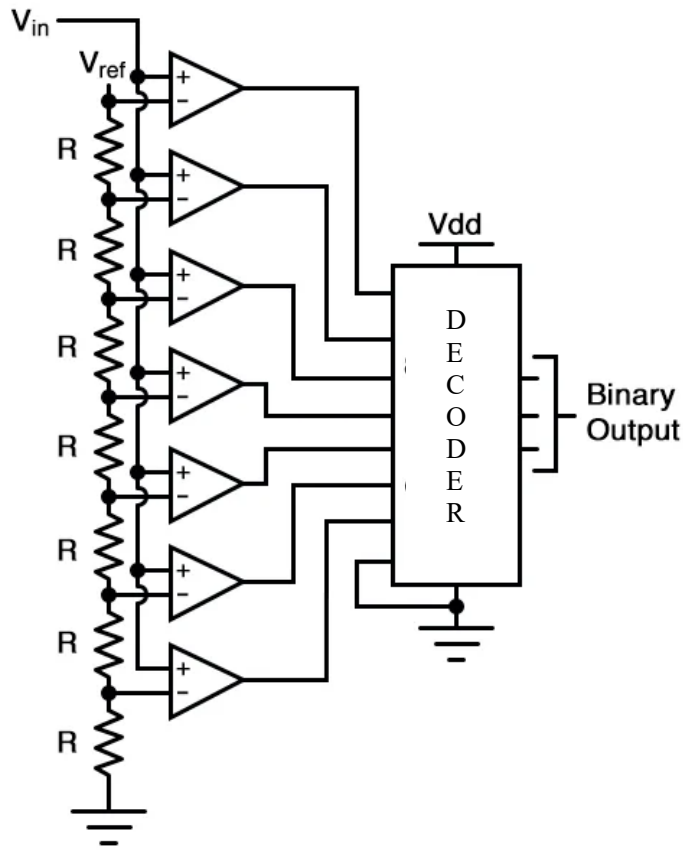
Figure 2.1. Flash ADC diagram [1]

In this example, a resistor string is used to divide the supply voltage into specified reference levels. These voltage references are then compared with the input signal using a comparator, which outputs a logic 1 if the positive terminal is at a higher potential than the negative terminal and conversely, outputs a logic 0 if the negative terminal is at a higher potential. For an N-bit flash ADC, (2N+1) comparators are needed to compare the reference voltage levels to the input signal. As the resolution increases, hence the number of bits, the number of comparators needed to perform the conversion increases by a factor of 2, which drives up power consumption and area. Due to this case, flash converters are mainly used for low to medium resolution applications. Efforts have been made in to lower the power consumption by reducing the number of comparators required to produce the digital output. In [2], a 4-bit flash ADC was designed and implemented

using a 1.8V supply voltage with a power consumption of 1.19mW. The 15 reference voltages are generated using voltage divider networks consisting of diode connected transistors instead of a resistor network. Only 4 comparators are used; a 2:1 mux, 4:1 mux, and 8:1 mux are employed with select lines that relay the proper reference voltage to the comparators for the conversion logic. The architecture of this 4-bit flash converter is shown in Figure 2.2.
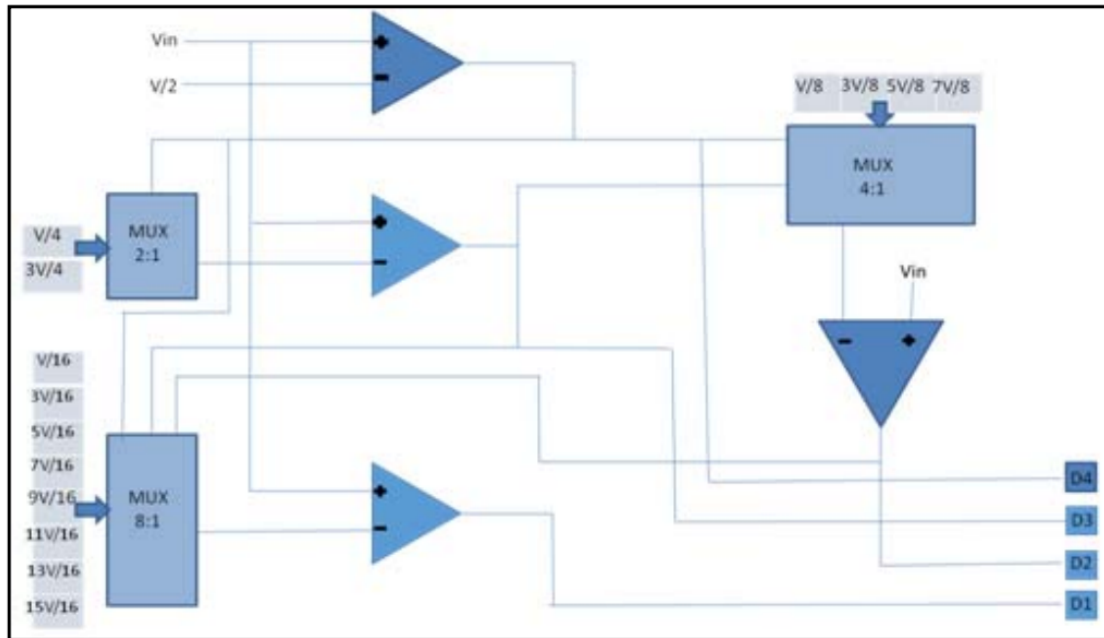
Figure 2.2. Flash ADC with reduced number of comparators [2]

As this method limits the number of comparators, the power consumption is reduced significantly however, N number of comparators are still needed for an N-bit design. Also, the voltage divider network and MUX size increases by a power of 2 per bit which will increase the circuit complexity for medium resolution converters.

Integrating ADCs are attractive for implementing high-resolution data conversion on slow-varying signals. An example is a dual-slope ADC that performs the conversion by integrating the input signal and a reference signal in two subsequent phases. A diagram of this ADC is shown in

Figure 2.3. The basic operation starts with the analog input V_A switched to the input of the integrator. Figure 2.4 shows the output of the integrating amplifier, V_S.
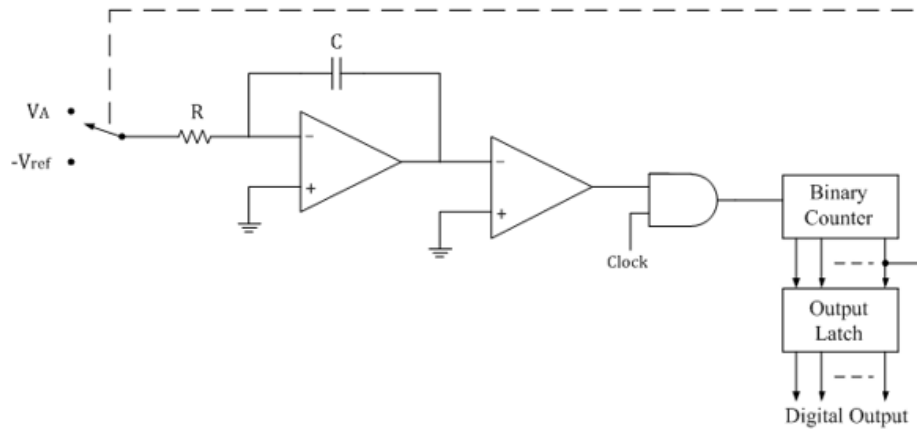
Figure 2.3. Dual-Slope ADC diagram [3]
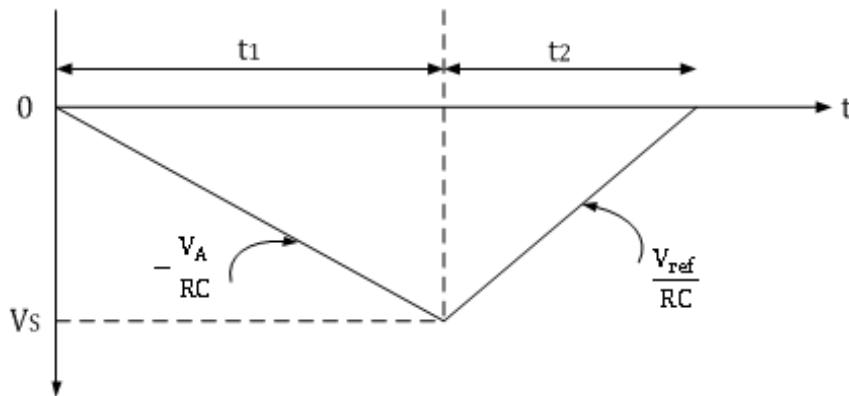
Figure 2.4. Dual-Slope waveform [3]

The output slope of the integrator is proportional to the slope of the magnitude of the sampled input voltage divided by the RC network in the negative feedback path. The comparator input goes high at the start of fixed time period t_1 while the AND gate toggles the binary counter on the rising edge of the clock. At the beginning of period t_2, the integrator input is switched to negative V_{ref} and the binary counter is reset to 0. The integration of negative V_{ref} yields a positive slope proportional to the magnitude of the reference voltage. The AND gate logic triggers the binary counter until the magnitude of the integration crosses the threshold, which is ground in this case.

The output binary counter gives the integration time t_2 that is a correlation between the sampled analog input voltage and the reference voltage. The output latch then provides the digital output corresponding to this time interval. These converters have a simple circuit implementation and occupy less silicon area than many ADCs. These converters are highly linear and low power consumption but have slower conversion times [4]. In [5], a 8-bit dual-slope type ADC built using Global Foundries' 130nm technology has been implemented for an RFID sensor node system. In this application, DC power is harvested from an on-chip antenna and eliminates the need for a battery. The ADC demonstrated an ultra-low dynamic power consumption of 44 micro-Watts for a sampling frequency of 15 kS/s. The design achieved a max DNL and INL of 0.6 LSB and 0.95 LSB, respectively, with an area of 0.06 mm^2. The design for the ADC is shown in Figure 2.5. The main subcomponents of the ADC include an amplifier-based integrator, a cross-coupled dynamic latching comparator, SR latch and a digital logic control module which controls the timing aspects of the dual-slope converter.
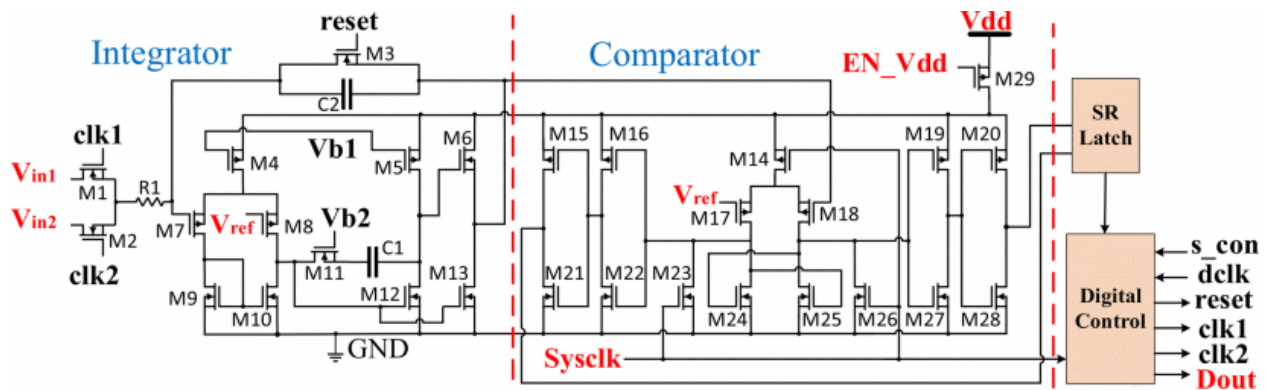
Figure 2.5. Dual-Slope ADC design [5]

This design saves power by duty cycling the ADC when not in use; Digital control signal, "En_Vdd", enables the supply voltage when in use. Compared to standard dual-slope ADCs, this design can save power by 51% [5]

SAR converters are used in low to medium resolution applications and allows for some speed to power consumption tradeoffs. The successive approximation algorithm uses a binary search technique allowing previously determined bits to compute the next best prediction and converge on a digital code most representative of the input voltage. This method is accomplished by use of several key circuits including a sample-and-hold circuit, shift register, SAR, Digital-to-Analog Converter (DAC) and a comparator. The general architecture of a SAR ADC is depicted in Figure 2.6 with the shift register included in the SAR block.
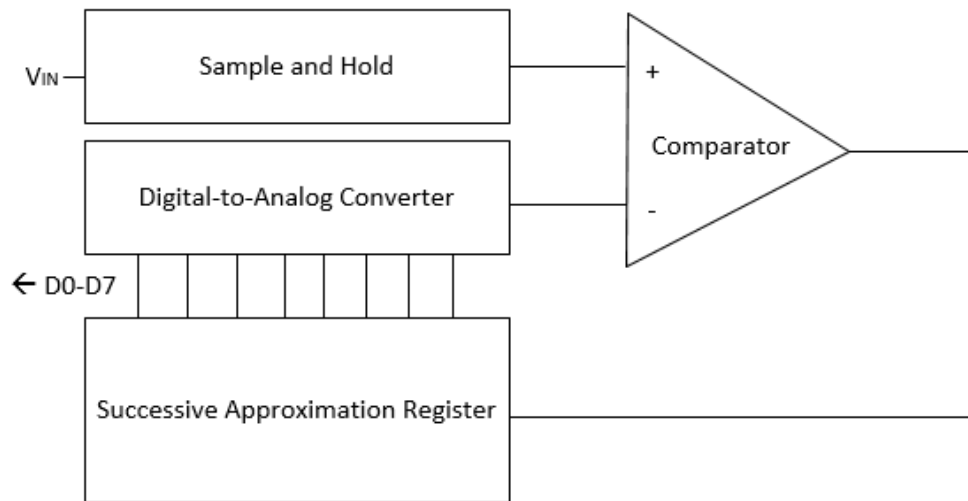
Figure 2.6. SAR ADC architecture

After initial sampling of the input voltage during the first clock cycle, this value is stored on a sampling capacitor and held for the remainder of the conversion time. The ring counter and SAR register operate to provide digital codes to a DAC that will give an output voltage representative of an initial binary guess. The output voltage of the DAC and sampled input voltage are delivered to a comparator that gives logical '0' or logical '1' feedback to set in the SAR based on the values of each input. The operation of the linear feedback shift register is shown in Figure 2.7.

	DAC outputs								C
0	o	o	o	o	o	o	o	o	X
1	1	o	o	o	o	o	o	o	a8
2	a8	1	o	o	o	o	o	o	a7
3	a8	a7	1	o	o	o	o	o	a6
4	a8	a7	a6	1	o	o	o	o	a5
5	a8	a7	a6	a5	1	o	o	o	a4
6	a8	a7	a6	a5	a4	1	o	o	a3
7	a8	a7	a6	a5	a4	a3	1	o	a2
8	a8	a7	a6	a5	a4	a3	a2	1	a1

Figure 2.7. Linear feedback shift register [6]

The SAR provides the next best prediction to the DAC for the remaining N-1 clock cycles allowing the SAR digital code to converge on an output best representative of the sampled input voltage. The conversion time equals (N+1) clock cycles, which infers an increase in the conversion time and power consumption as the resolution increases.

Efforts have been made in literature to increase the performance of the SAR ADC topology; mainly focused on power consumption and accuracy. To minimize the overall power consumption, a single-ended SAR ADC can be preferred over differential topologies [7]. An ultra-low power single-ended SAR ADC optimized for biosensor applications is proposed in [8]. The design features a novel DAC switching method that reduces the power consumption in the DAC

by 87.5% compared to conventional architectures. The architecture is shown in Figure 2.8.
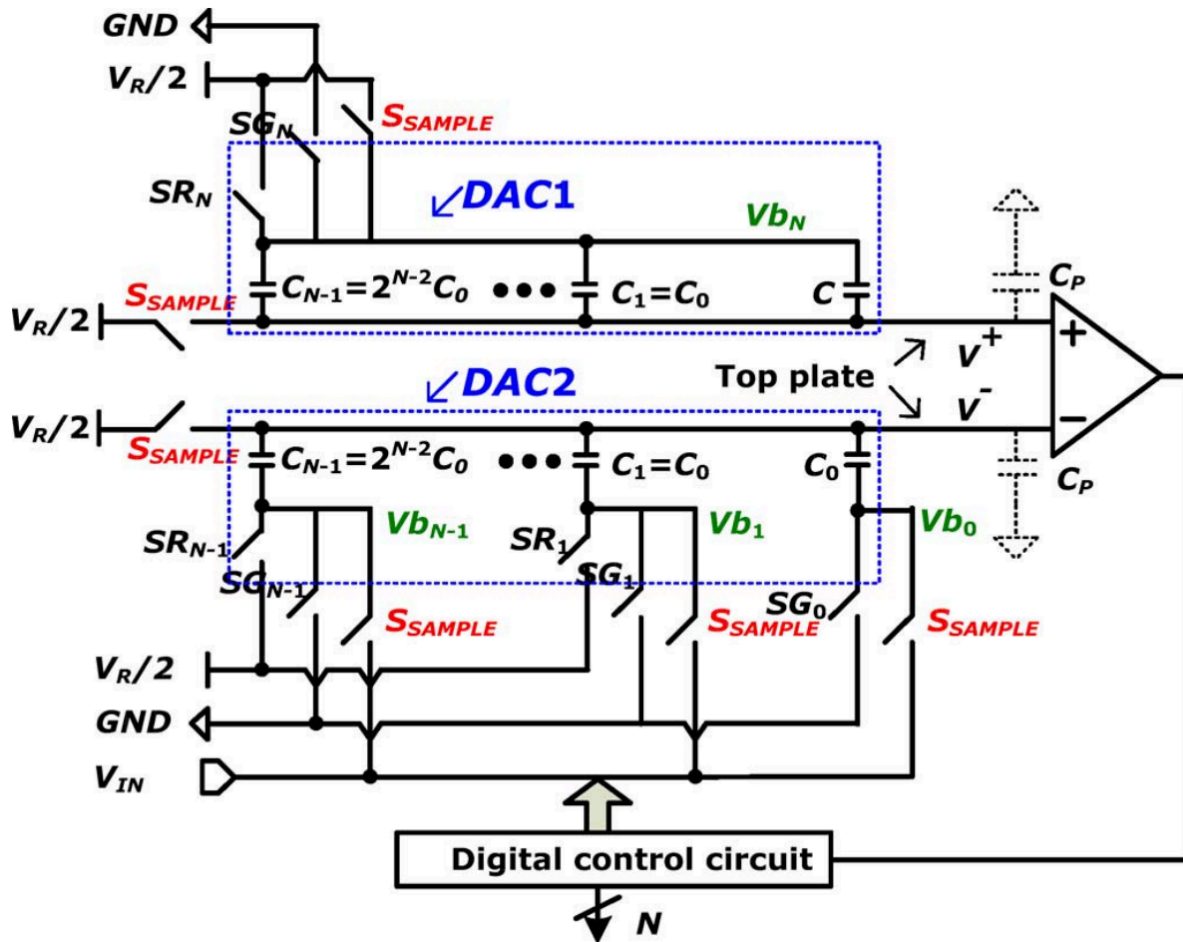
Figure 2.8. SAR ADC with novel DAC switching architecture [8]

In this design, the input signal is sampled on DAC2 while DAC1 is referenced to $V_R/2$. Subsequently, DAC1 is used to generate the MSB while DAC2 is handles the switching of the other N-1 reference levels. Utilizing $V_R/2$ as the reference voltage, this topology can digitize the full input range of 0 to V_R while reducing the power requirements. This work reported a power consumption of 16nW and 127nW for a sampling rate of 1kHz and 5kHz, respectively.

In [9], the authors reported nanowatt power consumption for a SAR ADC for an implantable sensor application. For a 60kS/s sample rate, the DNL and INL figures captured were

0.26 and 0.35 LSB, respectively. The design features a subthreshold comparator design where the bias current is described by Eq. (1) 1[10].

$$I_{DS} = \frac{W}{L} * \mu_{eff} * C_{OX} * Vt^2 * e^{\frac{V_{gs}-V_{TH}}{m*V_T}} * (1 - e^{\frac{-V_{DS}}{V_T}})$$ (1)

In this equation, μ_{eff} is the effective mobility, W and L refer to the width and length of the MOSFET, C_{OX} is the oxide capacitance, V_t is the thermal voltage, V_{gs} and V_{ds} are the gate-to-source and drain-to-source voltages respectively, and m is the body effect coefficient. The bias current through M5 is set between 50-1000nA depending on the supply voltage. The comparator design is shown in Figure 2.9.
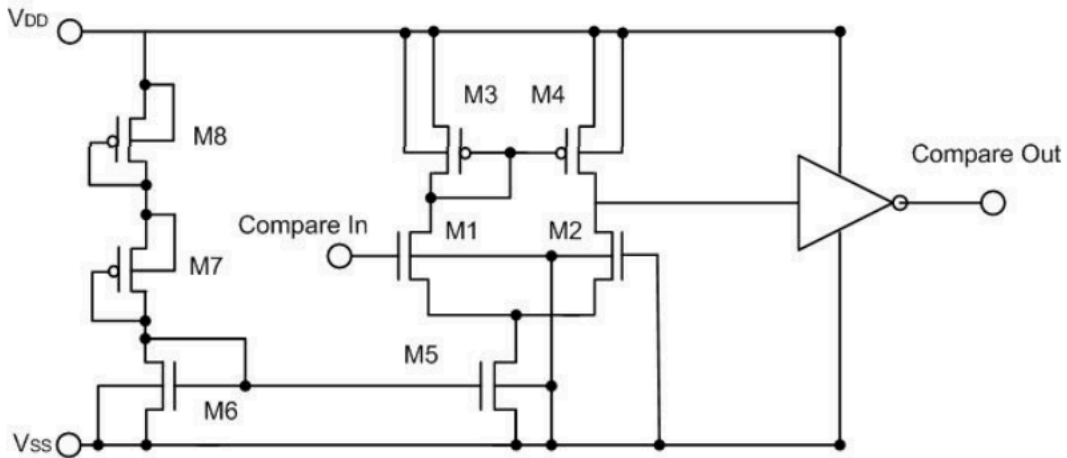
Figure 2.9. Subthreshold comparator design [9]

The amplifier gain is maximized around when the input is 0 V to compare negative and positive voltages. The output load for the amplifier is a CMOS inverter which determines the logic high and low for the comparator circuit. If the "compare in" signal is positive, the inverter output is logic 1, if the "compare in" signal is negative, the output is logic 0. As the topologies of the SAR ADCs are based on the same fundamental concepts, there are many ways to improve upon the design to optimize for speed and power consumption.

Chapter 3: DESIGN PROCESS AND SIMULATION

3.1 ADC Specifications

For this application, a SAR ADC topology was selected. As this design will eventually target a custom sensor for the corn plant, SAR ADCs give us good flexibility in design in terms of the resolution, speed and power consumption limitations. Sensor interface circuits such as this should be given specifications that give the end user the data of interest without limiting the sensor's capabilities beyond what the user needs. For this prototype, a Texas Instruments LMT85 analog temperature sensor is referenced that operates at a low 1.8 V supply voltage, has a wide temperature range functionality (-50° C to 150° C), low 5.4 µA quiescent current, and a push-pull output with 50 µA drive capability. The sensor output voltage range is fairly linear with a slight umbrella shape that can be reflected in the given parabolic equation:

$$Vo \; = \; 1324mV - \left[8.194\frac{mV}{°C}(T - 30° \; C)\right] - \left[0.00262\frac{mV}{°C2}(T - 30°C)\right]^2 \qquad (2)$$

where V_O is the analog output voltage in mV and T is the temperature with units of °C. Figure 3.1 shows the relationship between the temperature and output voltage for this device.
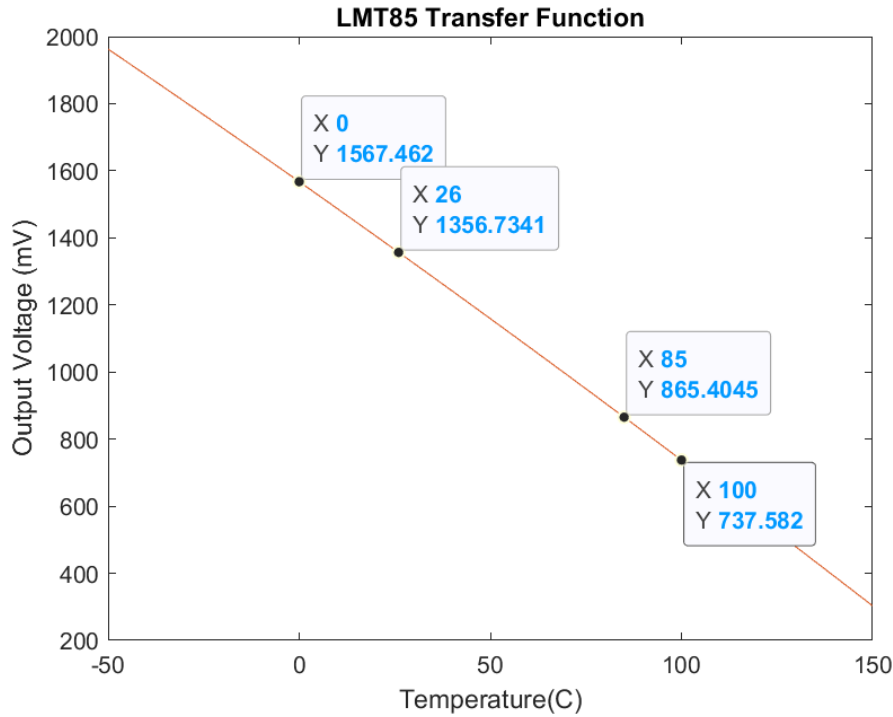
Figure 3.1. LMT85 transfer function

Eq. (2) and Figure 3.1 give an approximation of the transfer table as the accuracy of the equation degrades at the temperature range extremes. For this application, temperature measurements near the endpoints of this equation are unlikely and can be neglected. As such, we will define the usable range of our device from 0°C to 85°C which is slightly greater than the standard commercial temperature range (0°C to 70°C). As the output voltage range for the sensor (865.4mV – 1567.5mV) is a key specification for defining the input voltage range for the ADC, the minimum input voltage steps are also important for defining the LSB in terms of voltage. To capture this figure, the slope of the transfer function was used in Eq. (3) to capture the change in output voltage per degrees C.

$$Slope = \frac{(1567.462mV - 865.4045mV)}{(85°C - 0°C)} = 8.2595 \; mV/°C \tag{3}$$

The resultant slope was used as the minimum step change that should be detectable by the converter for a 1°C change in temperature.

In the TSMC 65 nanometer RF GP process design kit, 3.3V, 2.5V, 1.8V, and 1V devices are available to be utilized for the ADC design. Since the sensor circuitry can supplied by 1.8V and the expected output voltage range is less than 1.8 V for the application, a 1.8V supply voltage was chosen. This selection gives the designer the lowest supply voltage needed for the design, which minimizes power consumption and allows the battery supply (2.5V) to give adequate overhead in terms of supply voltage. To achieve a converter reference voltage of 1.8 V and sufficient resolution, it is determined that at least 8 bits are needed to provide the minimum step size defined by Eq. (4).

$$Resolution \ = \ 1.8 \, V \ / \ 2^{N} = \ 7.03125 \, mV \tag{4}$$

N is the number of bits; 8 in this case. Note that for the end user, the minimal temperature step size is given approximately by the slope of the transfer function divided by the resolution of the converter, which in this case is just less than 1°C. For increased sensitivity to temperature change, the resolution of the converter should be changed accordingly to detect the minimal voltage change measurable by the converter.

Interface circuitry for sensors vary in terms of speed and bandwidth due to the application. As only periodic temperature readings for this prototype are to be gathered for post-processing, specifications for speed and the correlated bandwidth can be relaxed to encourage a design with a lower power consumption. For a battery-operated wireless sensor node, the allotted power was determined from the capacity of the battery in fabrication by the department of biochemistry. Trial batteries provided approximately 77 milli-Watt-hours (mWh) of capacity at 2.27V. This available power will supply several circuits supporting the 433 MHz transmitter design that includes a Voltage Controlled Oscillator (VCO), Power Amplifier (PA), Low Dropout Linear Regulator

(LDO), Wake-Up-Receiver (WUR), and an ADC. Table 3.1 gives the power budget breakdown for the system level design.

Table 3.1. Power Budget Breakdown

Component	Estimated Power Consumption (1 Day)
VCO/PA	1.92 mJ
LDOs	0.12 mJ
ADC	0.27 μJ
Wake-Up Receiver (WUR)	216 mJ

As seen in Table 3.1, the power consumption by the sensor node is dominated by the WUR. As the ADC and transceiver circuitry will be cycled on when needed, the quiescent power draw will be limited to a maximum of 6 conversions per day, which corresponds to 45 nJ per conversion. The input voltage range is required to encompass the sensor's operating voltage however, the full input range available is used, which is 0 to 1.8 V. This allows some end-user flexibility; a wider voltage range can be used and it enables compatibility with more sensors.

Another key specification considered is the errors associated with the nonlinearity (DNL and INL) connected with the output transfer characteristics of the ADC. In this application, the range of voltages associated with one digital output code varies increasingly with rising DNL, which is undesirable. INL gives the deviation of the ideal measurement with the actual transfer characteristic and is essentially an integral of DNL measurements. This is also undesirable as it will require calibration techniques to correct for increased errors. For this ADC design, minimizing the DNL and INL is crucial to lowering the errors associated to the end application. Table 3.2 is given to summarize the list of specs for the ADC aforementioned in this discussion.

Table 3.2. ADC Design Specifications

Specification	Target
Resolution	8 bits
Power Consumption	< 45 nJ/conversion
Offset Error	minimum
Gain Error	minimum
DNL	minimum
INL	minimum
Input Range	0-1.8 V
Sampling Frequency	400 kS/s

3.2 SAR Algorithm

To implement the SAR algorithm, two individual blocks were created that are essential to the functionality of the SAR structure: the shift register and the successive approximation register. Both circuits are composed of D-Flip-Flops (DFFs), which include set and reset inputs. The transistor level structure for the DFF is shown below in Figure 3.2.
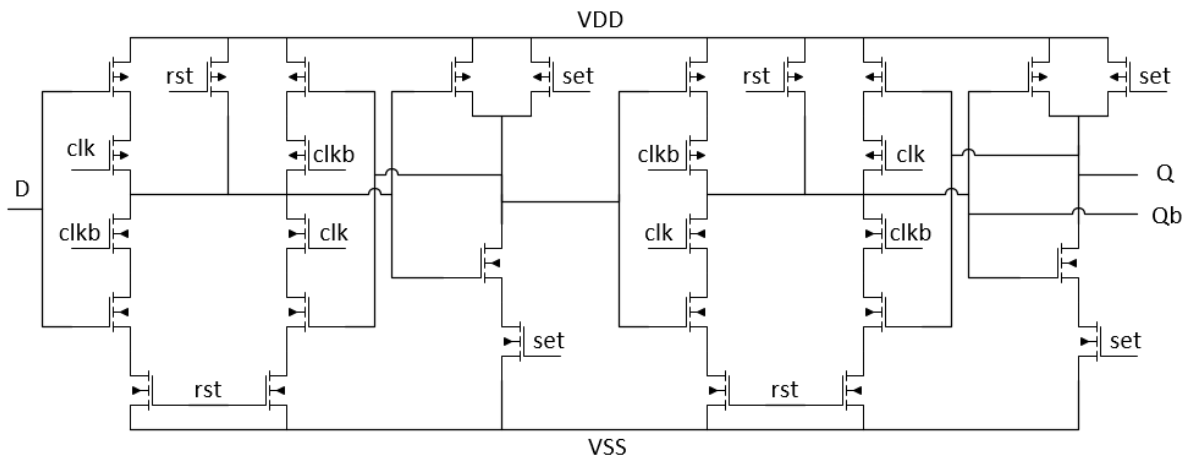
Figure 3.2. Asynchronous set-reset D-flip-flop

Inputs required are the complementary clock signals (clk and clkb), the input signal (D), set and reset (set and rst). Complementary outputs, Q and Qb, are needed to achieve the functionality of SAR register. Figure 3.3 shows the output of the DFF (Q) as its various inputs (D, clk, set, reset) are exercised.
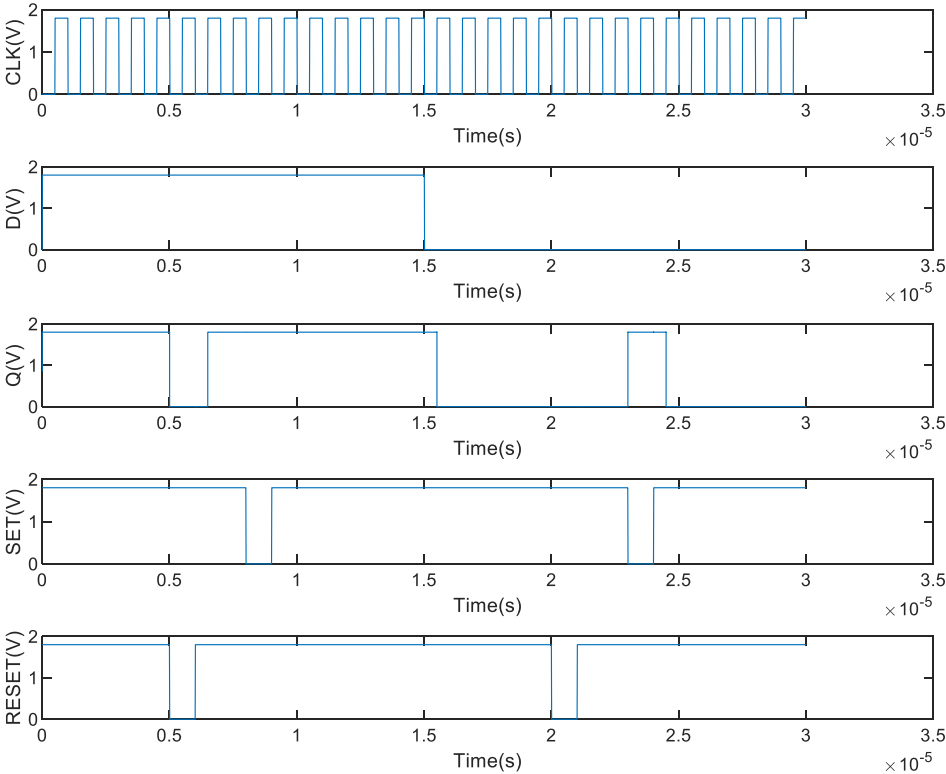
Figure 3.3. DFF operation

Some considerations must be taken in the design of the digital cells. For the shift register to operate correctly, one must ensure that the propagation delay and timing constraints are met to allow the signal to shift properly through the shift register. Propagation delay is the measure of the delay from the midpoint voltage of the rising edge of the clock to the midpoint voltage of the rising or falling output of the DFF. For the measurements, a clock with a rise time of 1 ns is used. The rising propagation delay is captured in Figure 3.4.
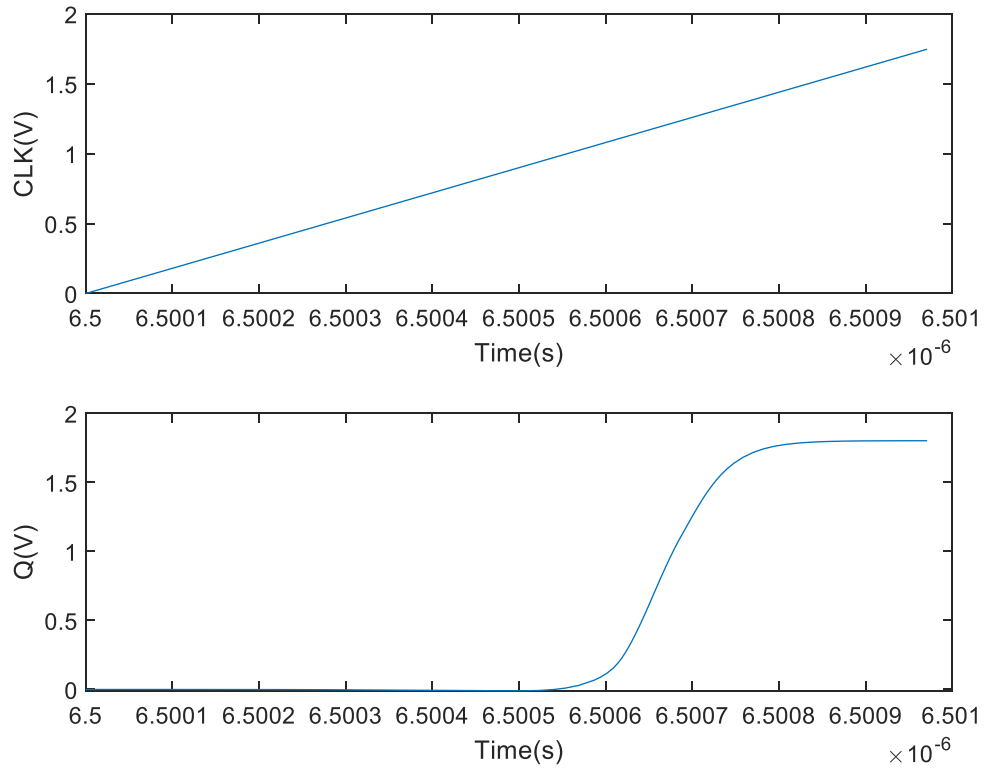
Figure 3.4. DFF rising propagation delay

The propagation delay was measured from the midscale voltage range of the two waveforms and found to be approximately 170 ps. The falling propagation delay time is shown in Figure 3.5 and was calculated to be approximately 235 ps.
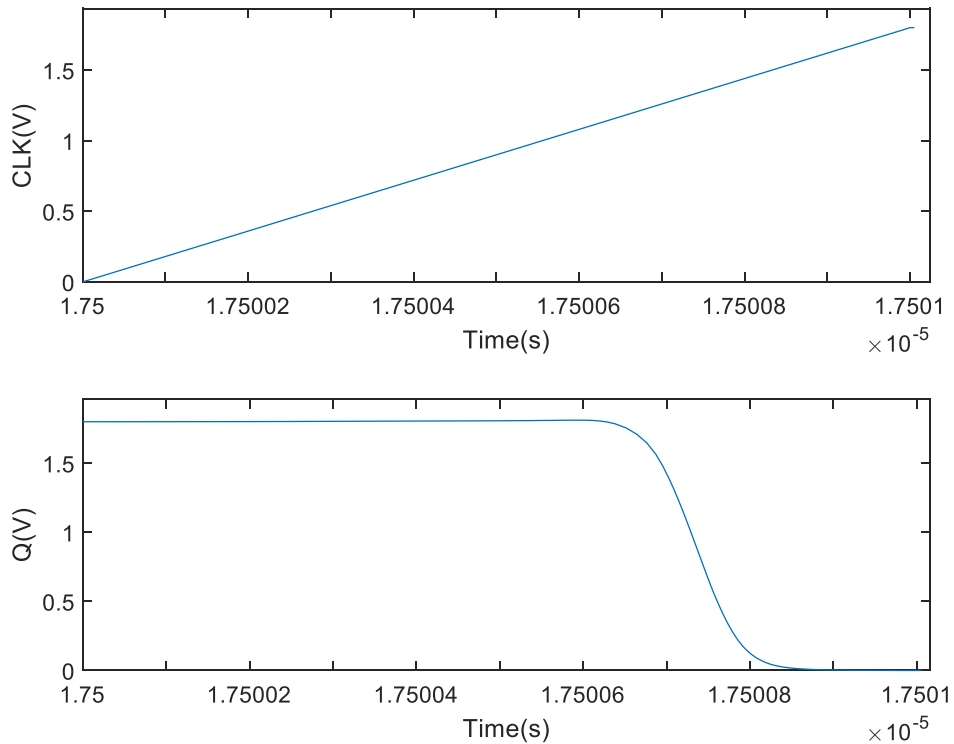
Figure 3.5. DFF falling propagation delay

The setup time is the time before the clock trigger edge where the data must be held at a stable state. The data should be stable long enough to prevent errors in latching the correct data. The hold time is the interval after the clock trigger edge where the data should be held stable to prevent errors. To ensure that this metastability does not occur in the shift register, the DFF outputs are buffered. These buffers add delay to ensure that DFF output is held long enough on the input of the subsequent DFF to allow the clock edge to latch the data present.

The shift register propagates a logic "1" through the DFFs on the rising edge of the clock. As each bit passes to the output "Q", the "Qb" pin sets the SAR register output to "1" by way of the asynchronous set pin, which is active low. On the next rising edge of the clock, the "Qb" pin releases the set signal of the associated SAR DFF and the COMP input signal is stored in the register. Note that the clock signal for the SAR registers are clocked by the output of the subsequent

DFFs. In the example in Figure 3.6 [6], the ring counter can be set asynchronously by the SET

function on D7 and is followed by an input logic "0" on the input pin D on the next rising edge of

the clock.
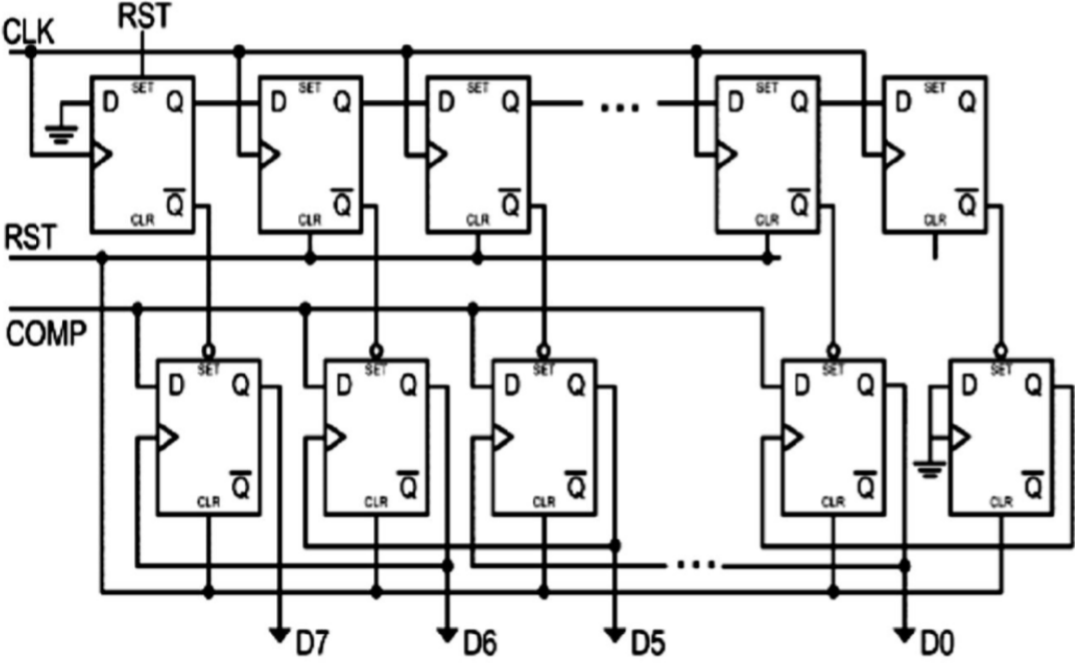
Figure 3.6. SAR register operation [6]

As the timing constraints are verified, the shift register and SAR register were verified in

simulation. Figure 3.7 shows an example simulation of the SAR register where the inputs (CLK,

START, COMP, and START) are exercised to verify its functionality. The outputs (D0-D7) are

monitored to verify the feedback logic (COMP) is stored correctly in each register.
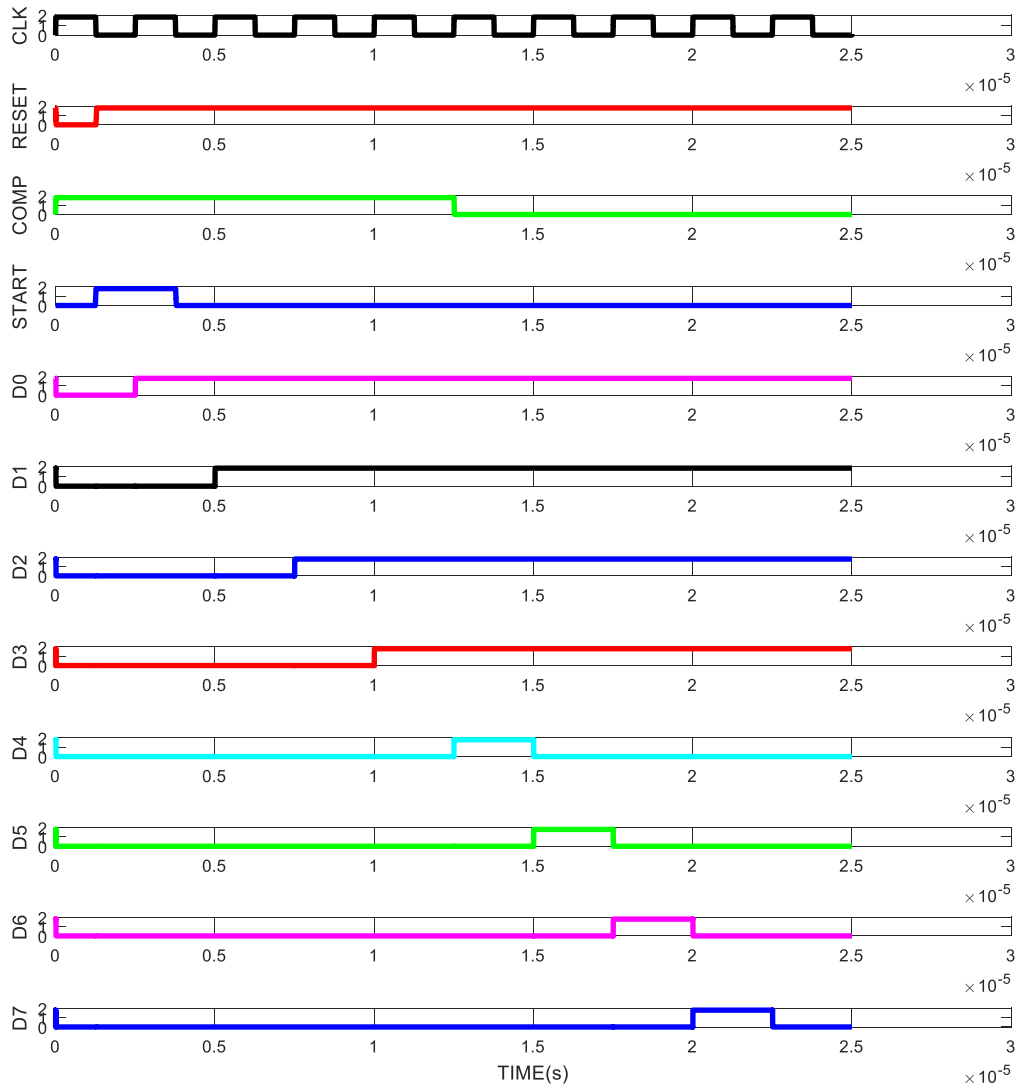
Figure 3.7. SAR register simulation

The bit stored in D3 is a result of the comparator signal transitioning low after the rising edge of the clock. As timing requirements are not met, D3 stores the previous value.

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3.3 Sample and Hold

For the operation of the SAR algorithm, there are two signals needed in order to determine the correct bits to be stored in the SAR register: the input voltage sample and the output voltage from the DAC. As the converter needs (N+1) clock cycles to perform the conversion, the input voltage cannot be allowed to change while the conversion is taking place. Sample and hold circuits allow the input voltage to be sampled and held until the conversion is completed. The basic components of a sample and hold circuit include a sampling switch and a holding capacitor. The sampling switch can vary in types depending on the amplitude of the signal being passed. Examples of sampling switches include an NMOS or PMOS pass transistor and transmission gates. The use of an NMOS or PMOS pass transistor can work for a range of input voltages; however, rail-to-rail operation cannot be achieved using these structures. For an NMOS or PMOS transistor to turn on, the gate to source voltage (V_{gs}) must be greater than the absolute value of the threshold voltage, $|V_t|$. As the input voltage trends toward the positive and negative rails, the NMOS and PMOS transistor channels turn off respectively when the threshold voltage is not satisfied. For a transmission gate, the complementary PMOS and NMOS are in parallel that allows the full range of input voltages to be stored on the holding capacitor. The size of the holding capacitor and pass transistors is another important parameter to consider. To ensure the accuracy of the sampling circuit within 0.5 LSB, the 3dB frequency of the circuit must satisfy the following Eq. (5) [11].

$$f3dB = \frac{1}{2\pi * Ron * Cs} > \frac{(N+1)ln2}{\pi} fs \qquad (5)$$

R_{on} is the on-resistance, C_s is the sampling capacitance and f_s is the sampling frequency. The RC time constant varies as a function of the series resistance and sample capacitance. The size of the sampling switches will determine the series resistance connected to the holding capacitor. For a 400 kHz sampling frequency, the 3dB frequency should be greater than approximately 800 kHz.

Increasing the sampling switch size lowers the series on resistance however, the effects of charge injection and clock feedthrough are increased due to parasitic capacitances, which can cause noise to be added to the sampled voltage. Charge injection occurs when the charges in the channel are forced into the circuit when the switch turns off. This charge can significantly affect the voltage stored on the holding capacitor if the sampling capacitor is small [12]. Clock feedthrough is also unwanted charge that is injected onto the data signal because of the coupling of the parasitic capacitances (C_{gd}) of the sampling switch. This phenomenon can also be minimized by using a larger holding capacitor and by using smaller device sizes [13]. Another factor to consider for the sample and hold function are the effects of voltage droop during the hold time. This voltage droop seen is due to the charge on the capacitor being discharged over time. For lower frequency operation, the hold time needed for N clock cycles is greater which means there will be a greater amount of leakage current during the conversion time. This droop can be minimized by increasing the capacitor size to a value where the leakage charge has minimal impact on the voltage stored on the capacitor [12]. Figure 3.8 shows the sample and hold circuit consisting of a transmission gate, sampling capacitor, and operational amplifier buffer driving a load capacitance, CL.
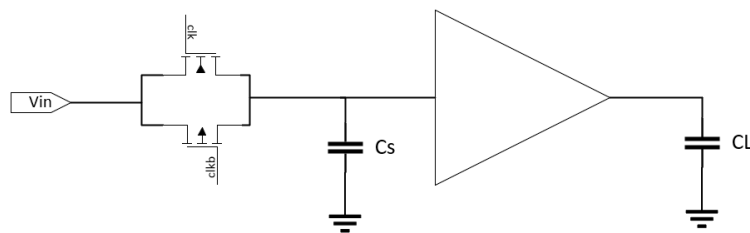
Figure 3.8. Sample and hold circuitry

To ensure the sample and hold circuit can be verified after fabrication, the circuit will need to be able to drive an oscilloscope that has a relatively large input load capacitance. If this load

capacitance (C_L) is connected directly to the sampling capacitor (C_s), the two capacitances will combine and increase the settling time significantly. Therefore, the use of an operational-amplifier buffer is needed to isolate the load capacitance from the sample and hold circuit without changing the performance significantly.

3.4 Digital-to-Analog Converter

The binary search algorithm is implemented by converting a digital signal into an analog voltage corresponding to the value of the bits provided. There are a few topologies to consider with each having their advantages, including the R-2R DAC and binary-weighted capacitive DAC. To minimize the static current dissipation, a binary-weighted capacitor charge-scaling array DAC was chosen that also lowers the size of the unit capacitance needed to implement the design compared to traditional binary weighted capacitive DACs. The split charge-scaling array DAC is shown in Figure 3.9.
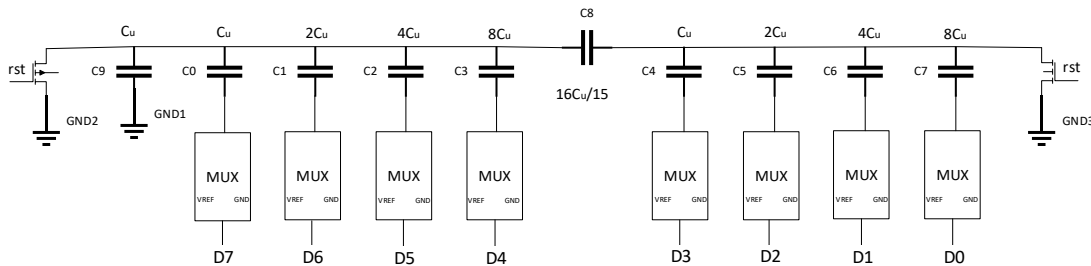
Figure 3.9. Charge-scaling array DAC

During the first clock cycle, the capacitor array is reset via NMOS transistors to allow any residual charge to be cleared from the array. During the subsequent clock periods, the reset switch is opened and the D0 bit is now switched to V_{ref} based off the successive approximation algorithm. An example of the operation of the charge scaling array is shown in Figure 3.10 where the MSB (D0) is equal to logic "1" [14].
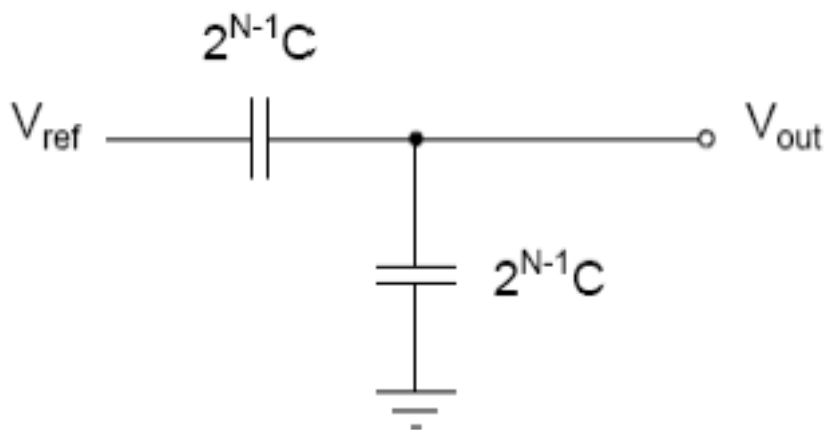
Figure 3.10. CSA equivalent circuit with MSB = 1 [14]

As the capacitances are equal, the resulting output voltage is $Vref/2$, which is the first guess of the SAR algorithm. From there, the remaining bits are switched in the DAC based on comparator feedback. These switches were implemented by using a Multiplexer (MUX). The MUX is made up of two transmission gates in parallel with complementary gate signals to pass. The sizing for the NMOS and PMOS structures is based on equalizing the channel on-resistance between the pair. This was implemented by choosing a width for the NMOS double the minimal sizing and using a parametric sweep to find the equivalent PMOS size. An input pulse signal with a very fast rise and fall time (1 ps) was given to determine the PMOS sizing with an equivalent output rise time compared to the falling time. In this simulation, the rising and falling times are taken for the MUX between 20% and 80% range of the transient edge with a 4pF load which is the MSB capacitor size. Figure 3.11 shows the output rising characteristic for the MUX with a rise time of 24.49 ns. Figure 3.12 shows the falling output characteristic for the MUX with a fall time of 24.78 ns. The rise and fall times are deemed appropriate for low to medium speed converters.
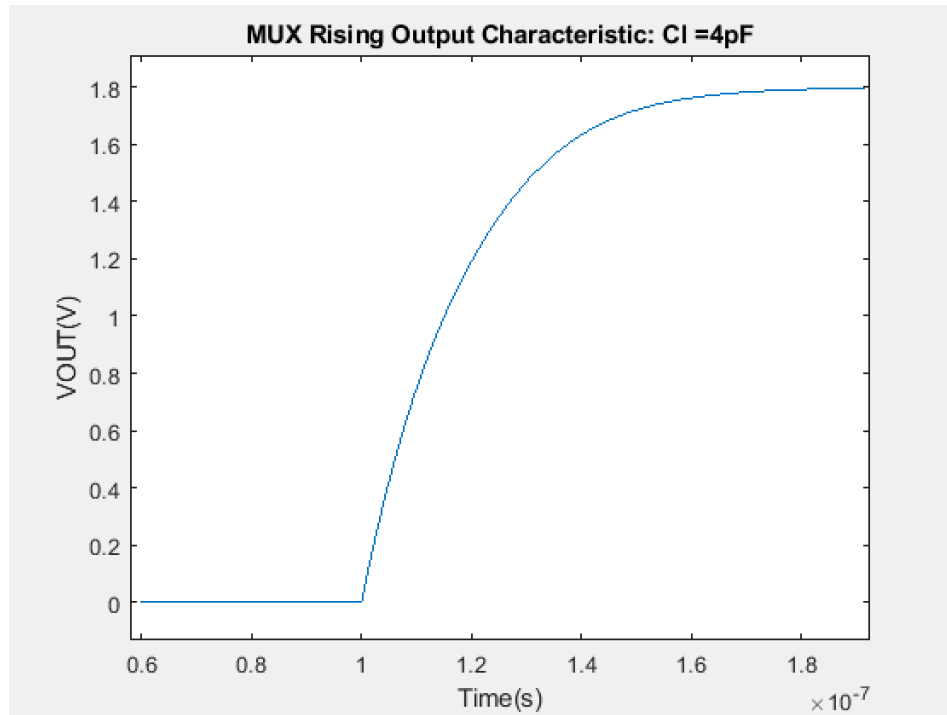
Figure 3.11. Output rising characteristic
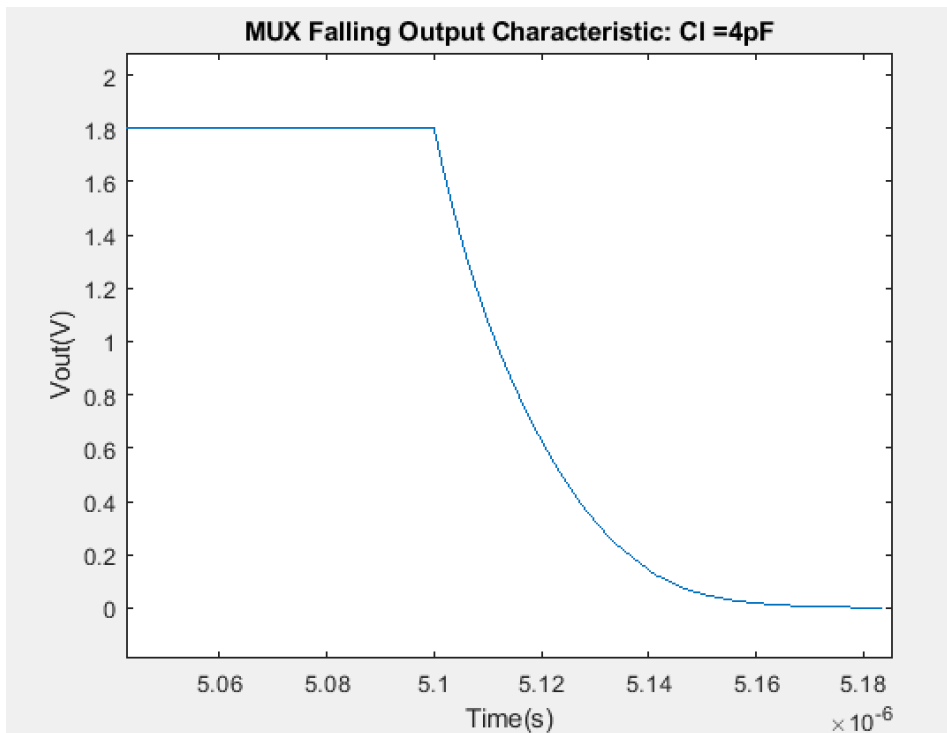
Figure 3.12. Output falling characteristic

The unit capacitance is chosen based on thermal noise and quantization noise and is limited to half of the least significant bit of the DAC in terms of voltage, as seen in Eq. (6) [15].

$$\sqrt{\frac{kT}{C} + \frac{LSB^2}{12}} \leq \frac{LSB}{2} \tag{6}$$

Eq. (6) can be rearranged to solve for C, the total capacitance of the DAC. Other factors to be considered are the parasitic capacitances, the capacitor array will see. As the unit capacitance decreases, the effects of parasitic capacitance dominate and cause offset errors to be added to the converted signal. The attenuation capacitor allows the equivalent MSB capacitance (D0-D3) to be scaled in size relative to the LSB capacitor array D4-D7. The value of the attenuation capacitor is set to 16/15 times the unit capacitance C_u (500fF) based on [14]. The output voltage V_O in terms of the 8 input bits (D0-D7) can be determined using Eq. (7).

$$Vo = V_{ref} \left[\frac{1}{15} \left(\left(D0 * 2^3 + D1 * 2^2 + D2 * 2^1 + D3 * 2^0 * \frac{15}{16} \right) + \frac{1}{2^8} \left(D4 * 2^3 + D5 * 2^2 + D6 * 2^1 + D7 * 2^0 \right) \right) \right] \tag{7}$$

In this equation, logic D0-D7 are the bits associated with the DAC capacitor array and V_{ref} is the reference voltage. From Eq. (7), it can be determined that the minimum and maximum output range of the DAC is approximately 0 V to 1.793 V, respectively. Figure 3.13 shows the output characteristic as a result of an input binary down counter from 255 to 0.
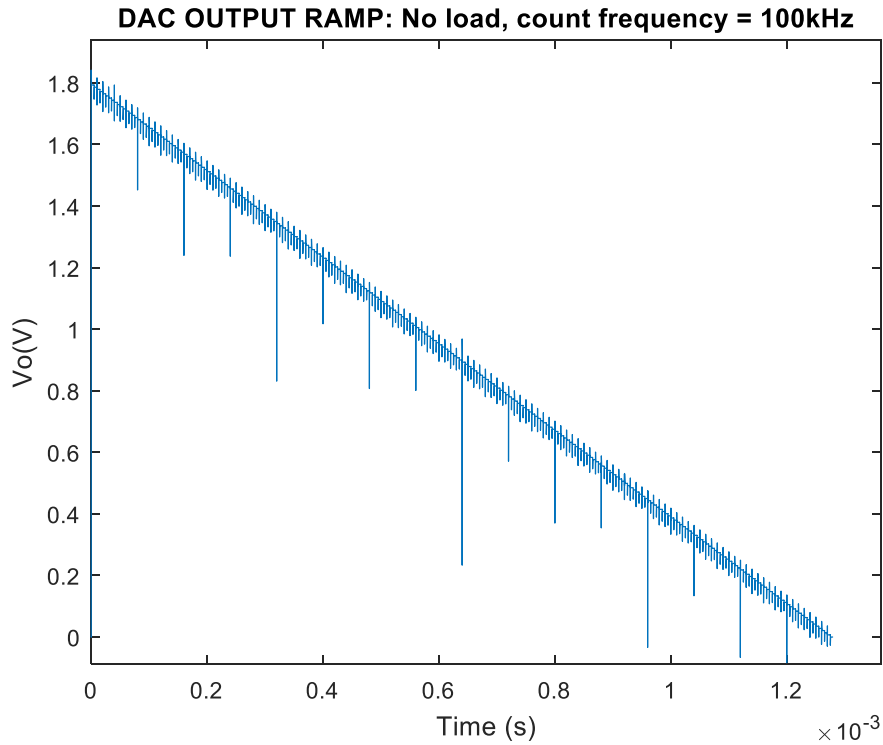
Figure 3.13. DAC response to ramp (unbuffered)

The offset and gain error of the DAC are nearly negligible as there is no load condition for this simulation. As the output of the DAC will be tested after fabrication, the output of the DAC will necessitate a buffer to drive an off-chip load capacitance. The op-amp previously discussed is used to isolate the capacitor array from the test equipment and comparator to prevent static errors being injected in the DAC transfer characteristic. The buffered output characteristic curve is a function of the 8-bit binary up counter and is shown in Figure 3.14.

DAC OUTPUT RAMP: CI=13pF, Count Frequency =100kHz
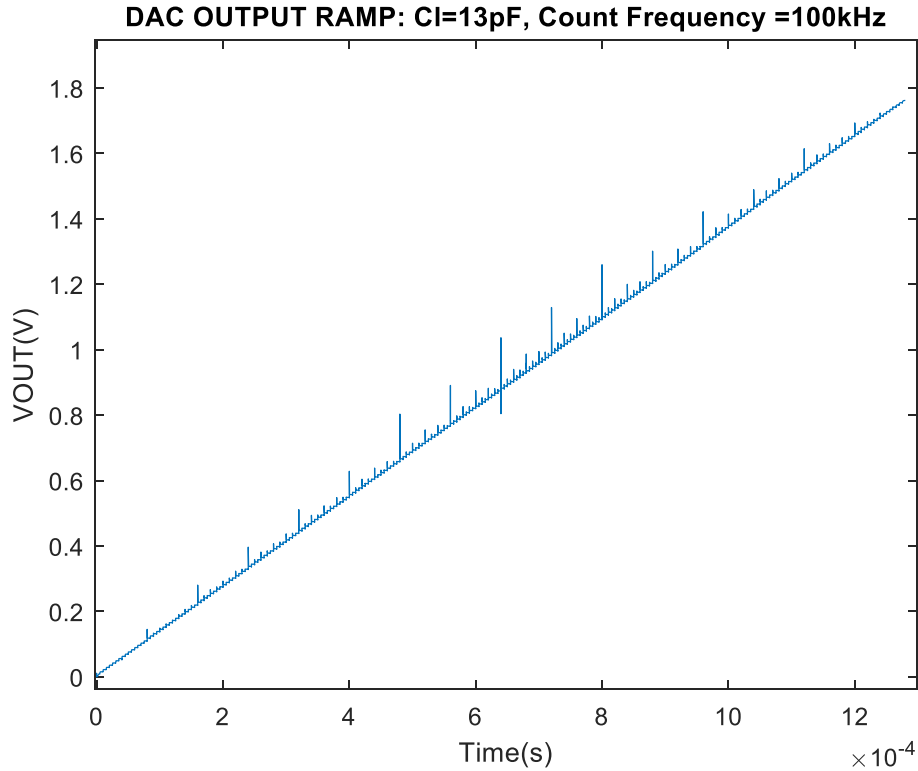
Figure 3.14. Buffered DAC response to ramp (rising)

The transient spikes are expected and are due to switching between bits in the DAC structure.

Minor offset and gain error are introduced due to the range limitations of the operational amplifier

buffer. Several key parameters are extracted from the DAC such as the DNL and INL. In theory,

the ideal values for DNL and INL are 0, which corresponds to a perfect transfer output

characteristic. This is difficult to achieve in practice. The DNL associated with the DAC are shown

in Figure 3.15.
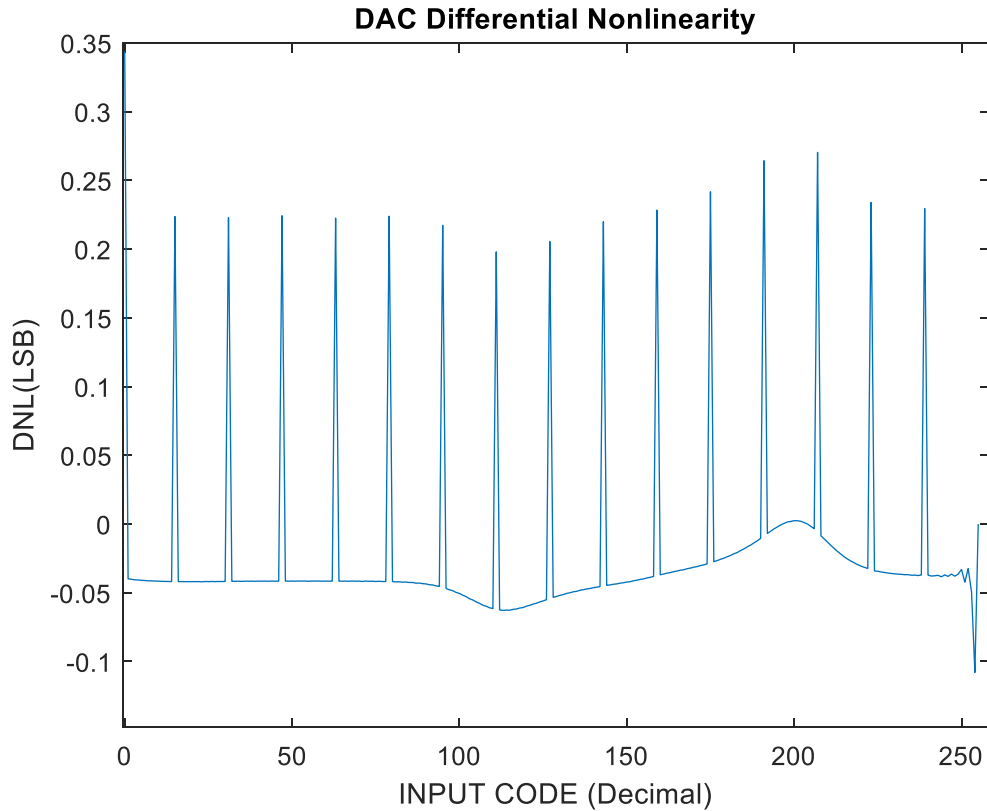
Figure 3.15. DAC differential nonlinearity

The maximum and minimum DNL associated with the DAC is approximately +0.34 LSB and -0.11 LSB, respectively. These results are on par with the reported maximum DNL for other conventional split-capacitor array DACs [16][17]The periodic spikes seen are due to some amount of parasitic capacitance associated with D3 in the capacitor array. The D3 bit is set 16 times in the DAC transfer characteristic at periodic input codes. Parasitic capacitances due to the layout have increased the voltage value of the individual bit in the capacitor array. This results in increased bit widths at periodic codes in the output characteristic. The spikes cause an approximately 0.25 LSB DNL in the output characteristic which corresponds to an almost 2mV spike in the DAC output characteristic. This kind of behavior in the DNL plot is also observed in [16] for an 8-bit split-charge array DAC. The INL associated with the DAC is shown in Figure 3.16.
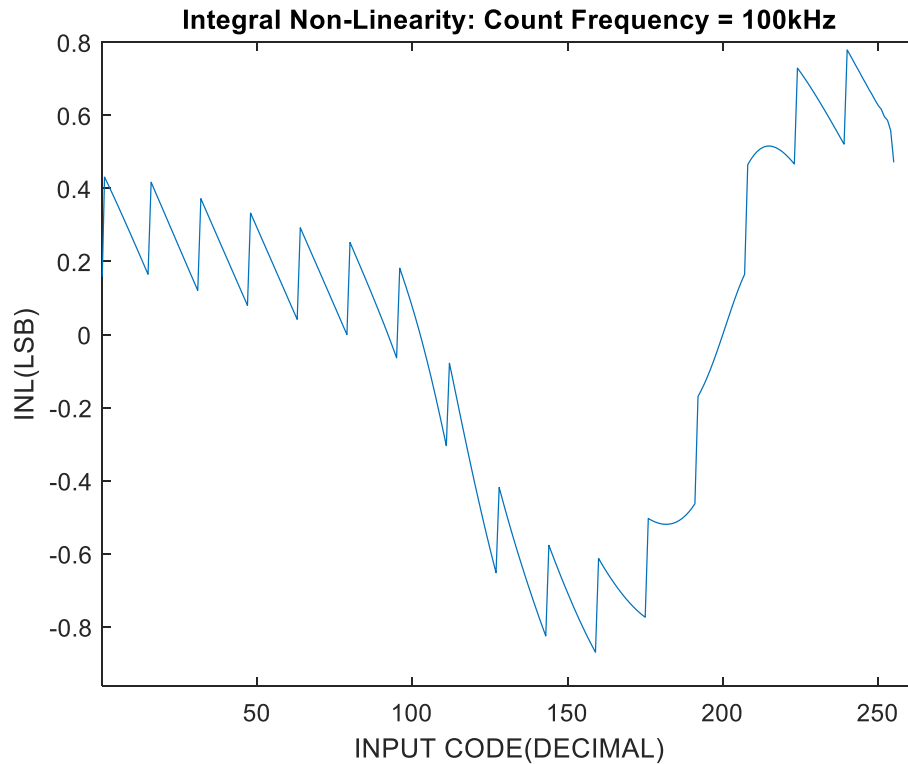
Figure 3.16. DAC integral non-linearity

The maximum and minimum INL associated with the DAC is +0.78 LSB and -0.87 LSB, respectively The INL figures are comparable with the reported maximum INL for other conventional split-capacitor array DACs [16][17]. The INL figures are attributed mainly to the parasitic capacitances created during layout of the DAC structure. For split-charge DACs, top plate parasitic capacitors add nonlinearity because the effect of the parasitic capacitances on the value of the DAC voltage is not constant for different input voltages [18]. As the figures are less than 1 LSB for the full transfer characteristic, this result is considered acceptable.

3.5 Operational Amplifier

For the operational amplifier design, there are several considerations regarding the specifications. The open loop gain, unity-gain bandwidth, phase margin and output drive need to be appropriate for use as a buffer. Open loop gain is defined as the ratio of the amplitude of the

33

output voltage to the input voltage often expressed in log scale, decibels. Although buffers are used in the unity-gain configuration, an acceptable open loop gain is necessary to allow the op-amp output to settle in the time requirement given by the speed of the converter. The open loop gain requirement (A_{ol}) can be shown by Eq. (8) [1]

$$Aol > 2^{N+1} \tag{8}$$

With the maximum error being defined by the half the LSB, the appropriate open loop gain specification is 55dB. The unity-gain bandwidth needed can also be calculated by using Eq. (9) [1].

$$F_{un} > F_{clk} * \frac{\ln(2^{N+1})}{\pi * \beta} \tag{9}$$

F_{un} is the unity gain frequency, F_{clk} is the sampling frequency, and ß is the feedback factor. This equation allows the unity-gain bandwidth to be designed using the settling time needed for the associated clock period. To ensure the design has some room for error, a F_{clk} corresponding to 1 MHz is used for this design calculation.

The output load, the buffer will be driving is also of importance. As there will be test points to verify the design, the buffer will need to drive the capacitance of a standard oscilloscope, which is approximately 13pF typically. If not properly designed, the amplifier's drive strength can limit the performance of the circuit by slowing the amplifier response time. The slew rate of an op-amp output stage for a capacitive load can be designed using the following equation [1]:

$$Slew\ Rate\ \frac{V}{us} = Io\ /\ C \tag{10}$$

C is the load capacitance and I_o is the output current. In this design, the slew rate requirement is set to the full-scale voltage divided by one half the clock period of the sampling frequency. The output current can be calculated and the output drive stage of the op-amp buffer can be appropriately designed. The output range is set to the minimum and maximum range of the sensor.

Finally, the phase margin needs to be considered to ensure stability of the op-amp in the closed-loop configuration. Standard design procedure allows for a minimum of 45° of phase margin with 60° considered as satisfactory. The phase margin can be measured using the op-amp Bode plot of DC gain vs frequency by taking the absolute value of the frequency difference between the unity-gain frequency and the frequency your phase crosses -180°. A summary of specifications is listed in Table 3.3.

Table 3.3. Summary of Specifications

Parameter	Specification
Open loop Gain (A_{ol})	55 dB
Unity gain Frequency (F_{un})	1 MHz
Phase Margin	60⁰
V_{OH}	1.567 V
V_{OL}	865 mV
Slew Rate	3.6 V/us

The implementation of the operational amplifier in Figure 3.17 began with the design of a commonly used 2-stage operational amplifier that consists of a five-transistor operational transconductance amplifier and a common source output drive stage. An equation-based design procedure was followed to design the op-amp with a desired gain, bandwidth and phase margin [19]. A compensation network was added between the stages to meet the phase margin requirements. As the input differential pair are NMOS type, the input common mode range will be limited to V_{th}-VDD.
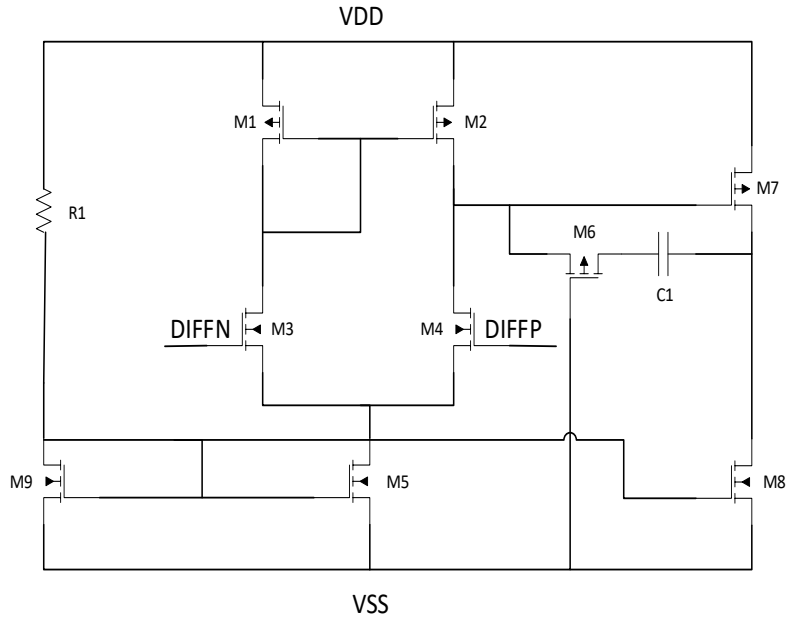
Figure 3.17. Two-stage op-amp with compensation

As the ADC will be designed for full ICMR operation, a rail-to-rail input stage is added to allow

this range of operation. A folded-cascode type amplifier with both an N-type and P-type input

differential pair allows for rail-to-rail operation [20]. This topology is shown in Figure 3.18.
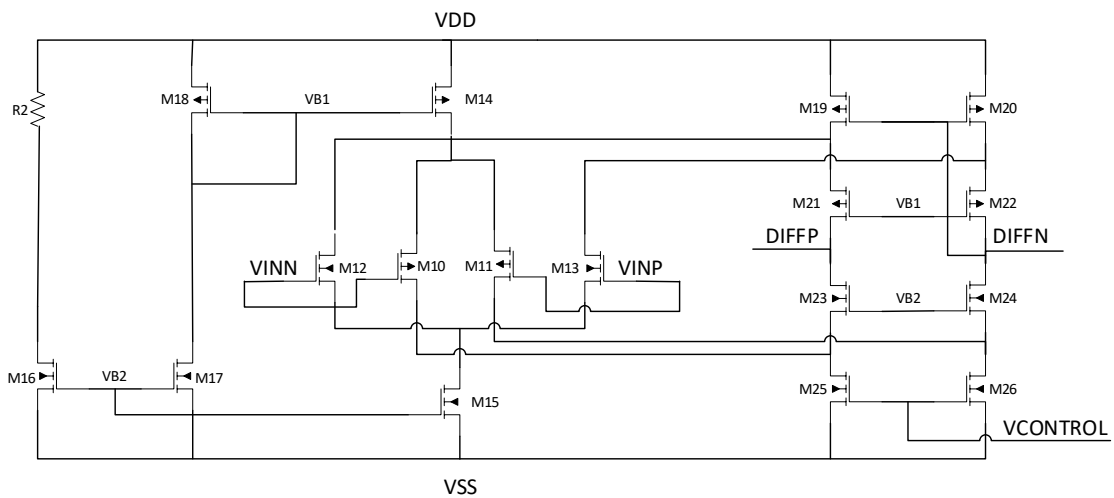
Figure 3.18. Wide swing folded cascode amplifier [20]

This additional stage necessitates the use of a common-mode feedback circuit to ensure the output

common mode of the amplifier remains within the input common-mode range of the subsequent

amplifier stage. A common mode feedback (CMFB) circuit was added to control the output common-mode voltage and to regulate it to a specified voltage that is normally midscale of the power supply rails. Figure 3.19 shows the schematic of the continuous-time CMFB circuit utilized in the design.
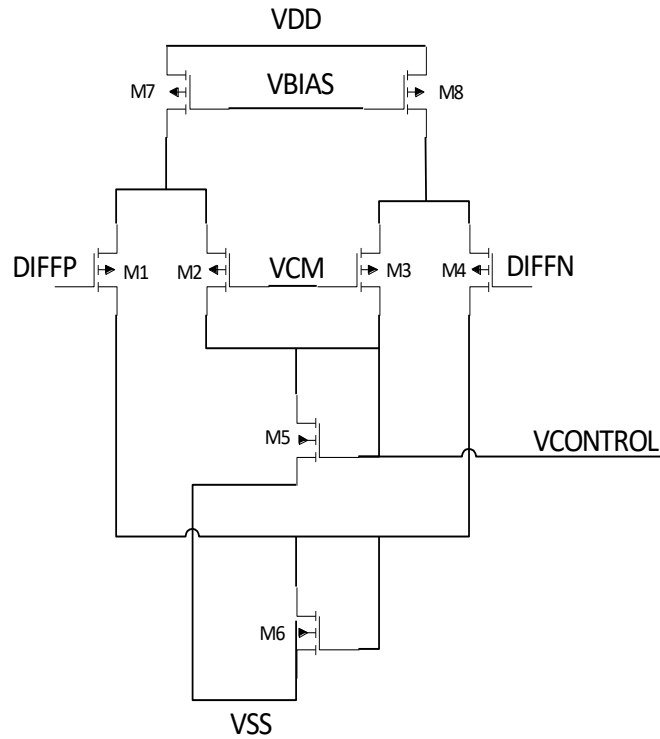
Figure 3.19. Common mode feedback [21]

Increasing common mode voltages causes the currents in both M2 and M3 to increase, which in turn, causes the voltage across M5 (VCONTROL) to increase. This voltage controls the n-channel current sources in the folded cascode which causes larger currents to pull down toward the negative rail bringing the common mode voltage back to its original value.

The simulation results of the operational amplifier in open loop configuration and for the transient response are shown in Figures 3.20 and 3.21, respectively.
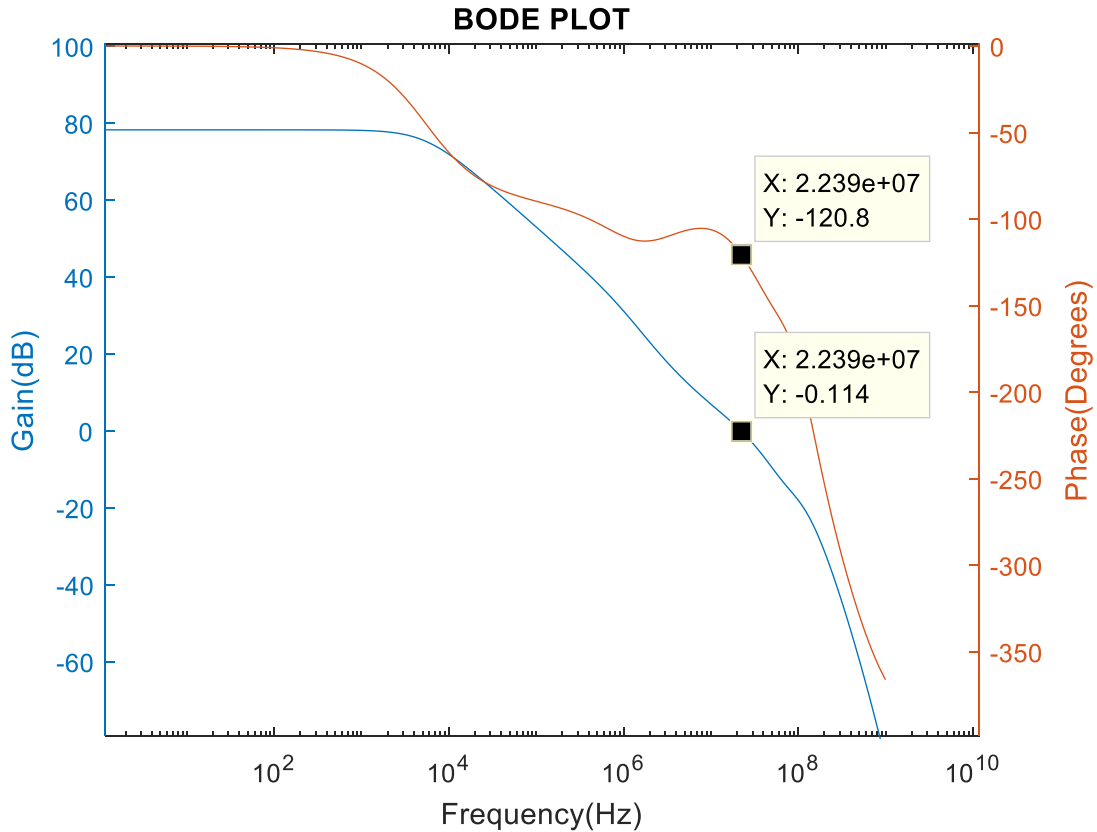
Figure 3.20. Op amp Bode plot

The open loop gain is approximately 78 dB, which meets the 55 dB specification. The simulated unity-gain crossover frequency is approximately 22.39 MHz, which corresponds to a phase of 120.8 degrees. The resultant phase margin is 59.2 degrees, which also satisfies the design specifications. The transient step response for the op-amp in the non-inverting configuration is shown in Figure 3.21.
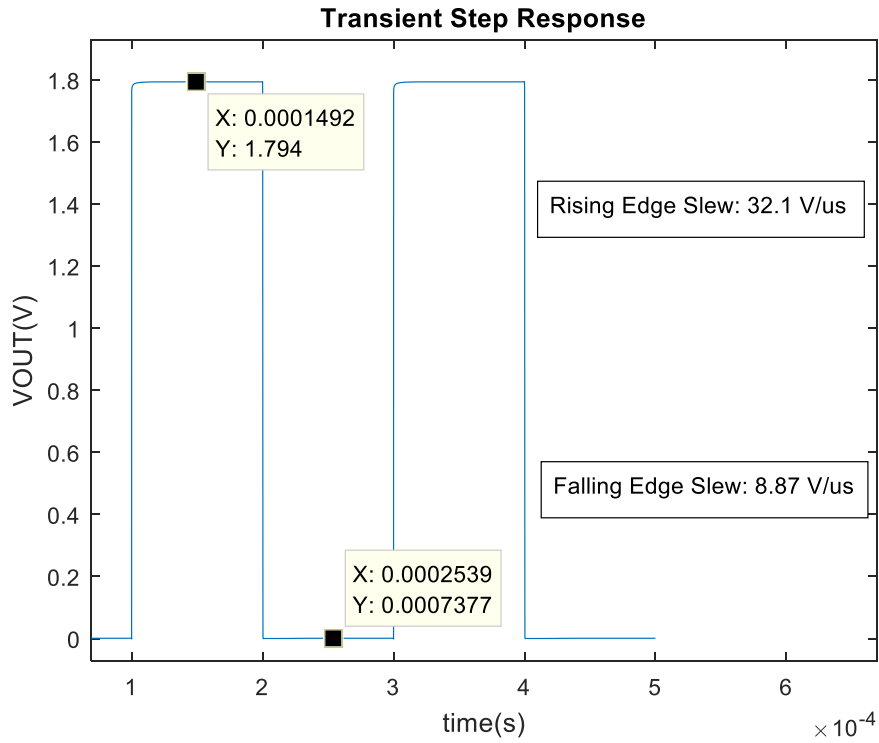
Figure 3.21. Transient step response

The transient response shows the response of a pulse signal on the non-inverting terminal of the op-amp in the unity-gain configuration. The input voltage signal given is a 0V to 1.8V pulse with a rise time of 1ps. The op-amp shows an output rise and fall time of 33.43ns and 121.3ns, respectively. Table 3.4 summarizes the simulated results for the list of specifications.

Table 3.4. Op-Amp Simulation Results

Parameter	Specification Value	Simulated Result
DC Gain *(Vcm=0.9V)*	55 dB	78.2 dB
Unity Gain Frequency	1 MHz	22.39 MHz
Phase Margin	60⁰	59.2°
Slew Rate	3.6 V/µs	8.87 V/µs
V_{OH}	1.567 V	1.794 V
V_{OL}	865 mV	700 µV
Quiescent Current	400 µA	227 µA

3.6 Comparator

The SAR takes input directly from the comparator that gives feedback on the relative values of the sampled input signal and the digital-to-analog converter. The sampled input signal is applied to the positive terminal while the DAC output is on the negative terminal. The comparator output provides the feedback for the SAR to allow the system to converge to the sampled input signal. The main specifications regarding the comparator are the resolution and speed. The resolution is defined as the minimal difference in terms of voltage the input terminals need in order for the comparator to amplify the difference. This specification can be derived by the LSB in terms of voltage the converter is designed to accommodate. Standard convention is to set the resolution to ½ the LSB of the converter, which in this design is approximately 3.5 mV. The gain specification is set by the necessary V/V gain needed to amplify the resolution of the comparator to the full-scale voltage. The gain needed is approximately 562 V/V, which is approximately 55 dB.

Several topologies of comparators can be implemented for this application. Operational amplifiers can be used as comparators in the open-loop configuration. Fast, discrete-time, dynamic comparators can also be utilized that can provide low to zero static power dissipation during the

active clock phase. In this design, a continuous time, latched comparator was utilized. The basic structure of the comparator centers on the latch, which is considered the decision-making part of the circuit. The latch can be modeled by back-to-back inverters that utilize positive feedback. The time constant of the latch should be considered as the speed of the decision circuit should be fast enough for the sampling frequency of the converter. Eq. (11) shows the time constant of the latch [21].

$$T_{ltch} = K \frac{L^2}{\mu_n V_{eff}}$$ (11)

K is a proportionality constant ranging from 0 to 1, L is the length, and V_{eff} is the effective voltage. By examining Eq. (11), the variables affecting the latch time constant can be recognized. As explained in [17], the latch time constant depends primarily on the technology; efforts should be made to maximize V_{eff} and minimize the capacitance connected output nodes of the latch. If the differential input to the latch is small, the latch time constant is also affected as seen in Eq. (12) [21].

$$T_{ltch} = K \frac{L^2}{\mu_n V_{eff}} \ln \left(\frac{\Delta V_{logic}}{\Delta V_0} \right)$$ (12)

In Eq. (12), ΔV_{logic} is the voltage needed for subsequent logic circuitry to safely differentiate the correct output value.

In this case, a buffer is needed to isolate the load capacitance from the latch and to convert the differential output to single-ended logic needed for the successive approximation register logic. If the load capacitance connected the differential latch outputs are not equal, an offset voltage will be seen on the output [22]. The buffer used in this design is a self-biased (n-flavor) input buffer. The latch inverter buffers were also added to further isolate the load capacitance from the latch and to increase the drive strength.

Due to the differences in the loading of the latch output nodes and the effects of process variation, the latch will practically have some offset. This offset results in one output decision to be favored over another by some amount of voltage, V_{OS}. This condition can degrade the resolution of the comparator by requiring a larger differential input to the latch for the correct decision to be achieved. To minimize the effects of the offset, a preamplifier is commonly utilized. As seen in Eq. (13), the preamplifier gain (A_v) amplifies the differential voltage to the latch which can then essentially null the effects seen by the latch offset voltage (V_{os}) [21].

$$V_{offset} = V_{off-preamp} + \frac{Vos}{Av} \tag{13}$$

The total offset of the comparator (V_{offset}) can be shown by Eq. (13) where $V_{off-preamp}$ is the preamplifier offset, V_{OS} is the latch offset, and A_v is the gain provided by the preamplifier.

Another consideration for CMOS latched comparators is kickback noise. Kickback noise is caused by large voltage variations in the internal nodes coupling to the input as depicted in Figure 3.22 [23].
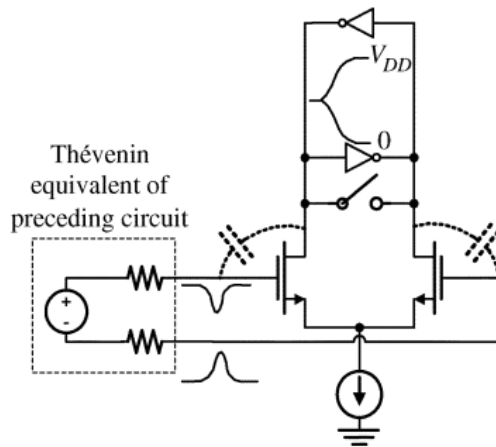
Figure 3.22. Kickback noise generation [23]

As the positive feedback mechanism creates a large dV/dt, the coupling capacitance C_{gd} creates a path for noise to disturb the preceding circuit. Several noise reduction techniques have been studied in [23] and the preamplifier implemented is shown in Figure 3.23. The design of the preamplifier was implemented using a complementary differential input pair where the difference currents are mirrored and added together at the input of the latch. With the current mirror acting as a buffer, the input branches are both insusceptible to the kickback noise from the latch output [24]. The complete comparator design is shown in Figure 3.23.
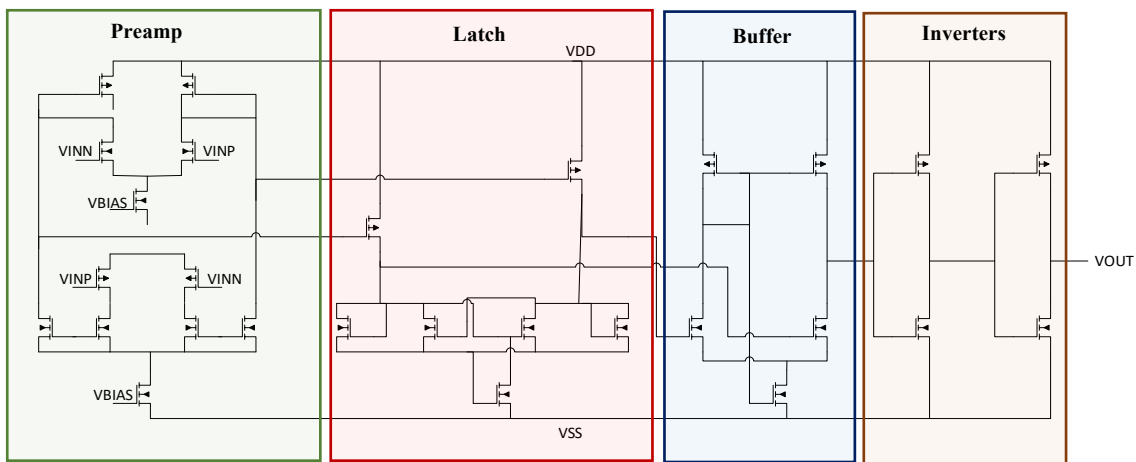
Figure 3.23. Comparator schematic

To characterize the comparator, the AC performance of the preamplifier was simulated to extract the gain and bandwidth figures. Figure 3.24 shows the Bode plot of the preamplifier circuit with a common mode voltage of 0.9 V from 1 Hz to 1 GHz.

PREAMPLIFIER AC CHARACTERISTICS: Vcm = 0.9 V

X 2.2909
Y 29.4009
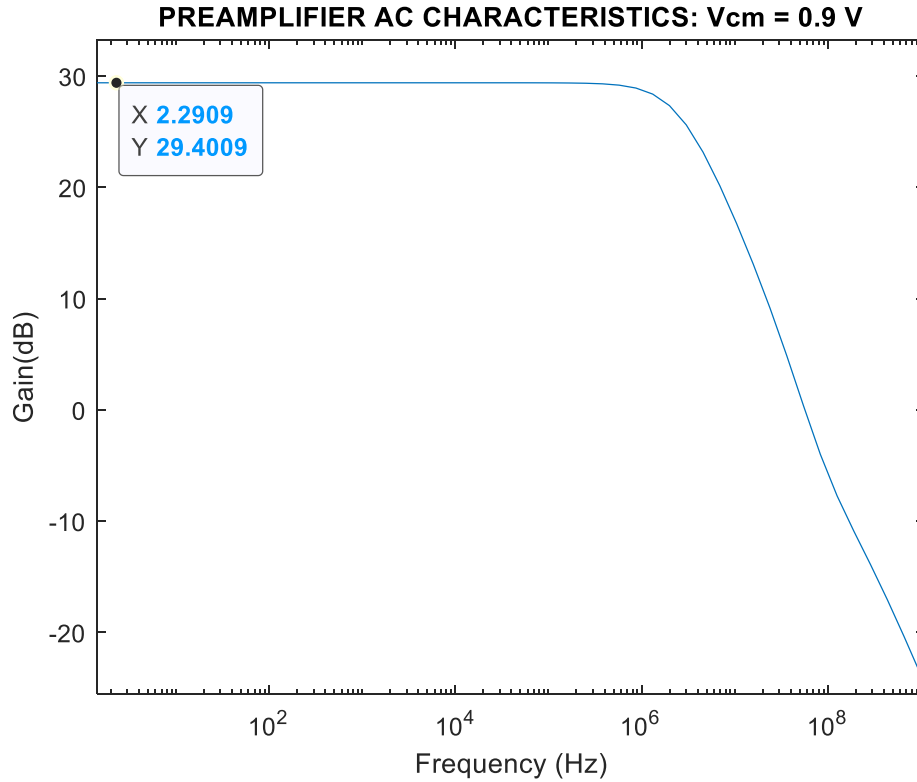
Figure 3.24. Preamplifier AC characteristics

The maximum gain and bandwidth were found to be 29.4 dB and approximately 2.5 MHz, respectively. At the minimum resolution (3.5mV), the amplifier provides sufficient gain to overcome a 100mV latch offset voltage, which is only expected to be on the order of 10mV to 20mV. To further characterize the comparator, the DC performance was simulated. The positive comparator input is swept from 0 to V_{dd} while the inverting terminal is stepped for each simulation in 100mV increments to show the comparators' wide input common mode range. Figure 3.25 shows the step response of the comparator output with V_{ref} at 0.9 V and the noninverting terminal swept from 0 to V_{dd}.
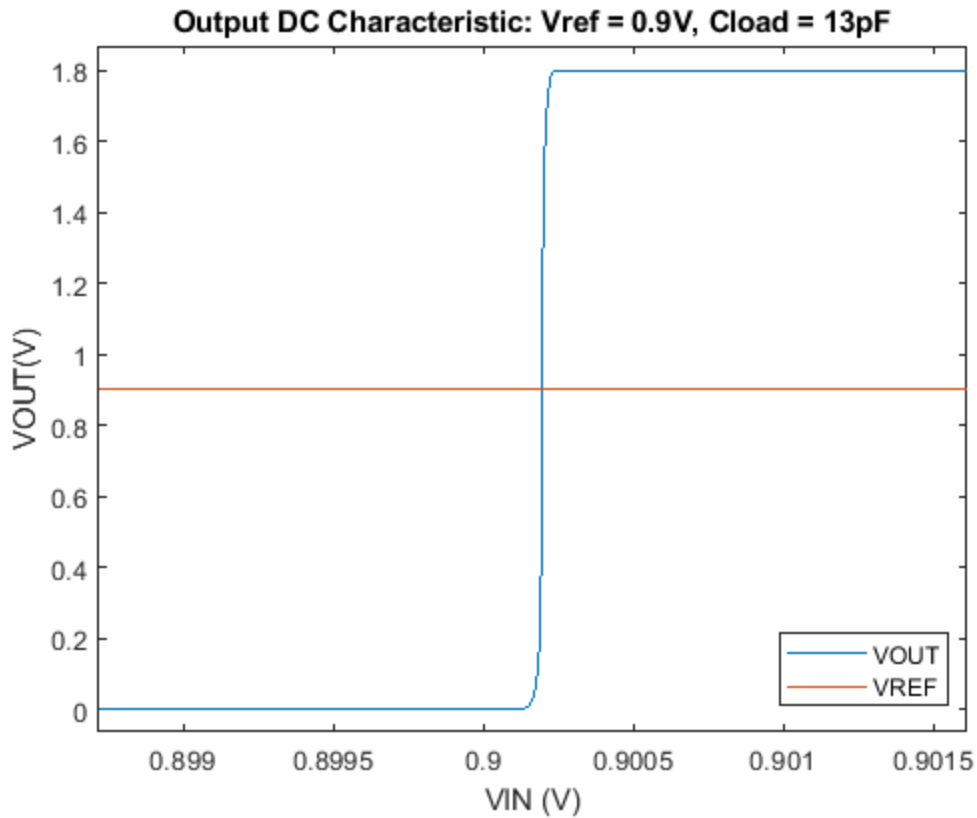
Figure 3.25. Comparator DC performance

The offset of the comparator is found to be 0.19mV, which meets the resolution requirement for this application (3.5mV). With the resultant output transfer curve, the gain of the comparator can be known by taking the derivative [1]. As the comparator design utilizes a latch with inherent positive feedback, the gain figure can be large. Figure 3.26 shows the derivative of the output transfer characteristic curve for the comparator.
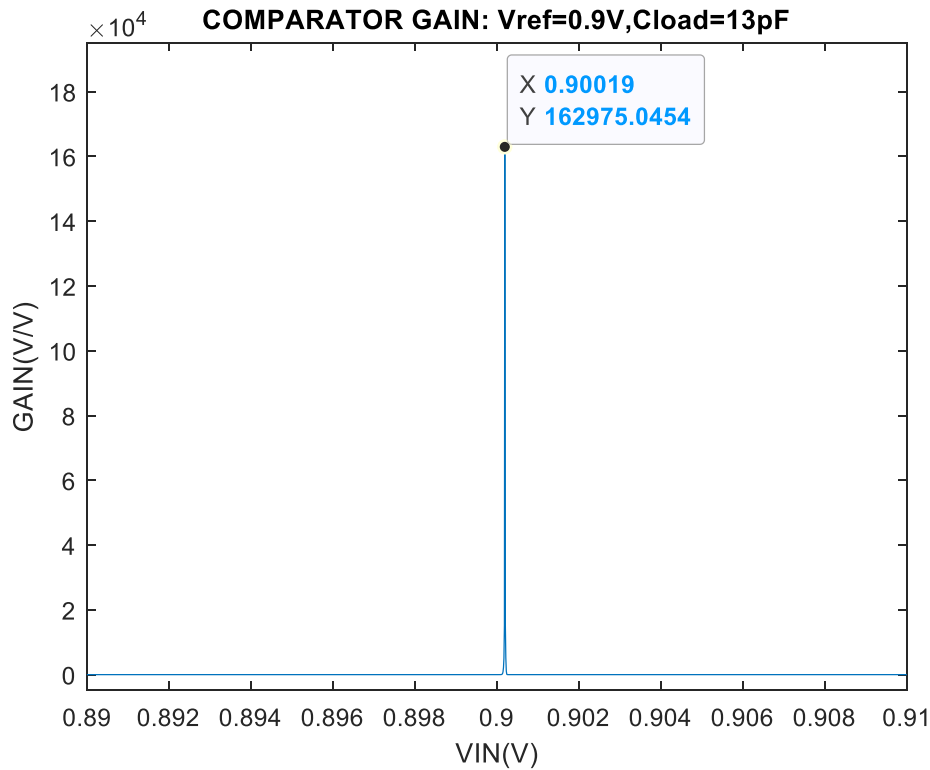
Figure 3.26. Comparator gain

The gain is shown to be approximately 162875 V/V with an offset voltage of 0.19 mV. Similarly, the transient response of the comparator is characterized by applying a pulse slightly higher than the reference voltage. In the transient response, one side of the differential amplifier is initially off and then turned on, requiring the internal nodes of the preamplifier to be charged over a wide voltage range. The propagation delay is also measured by applying a reference voltage on the negative terminal and a slightly greater voltage ($V_{ov} = 3.5mV$) on the positive input (VIN). Figure 3.27 shows the transient response of the comparator with the reference voltage at 0.9 V.
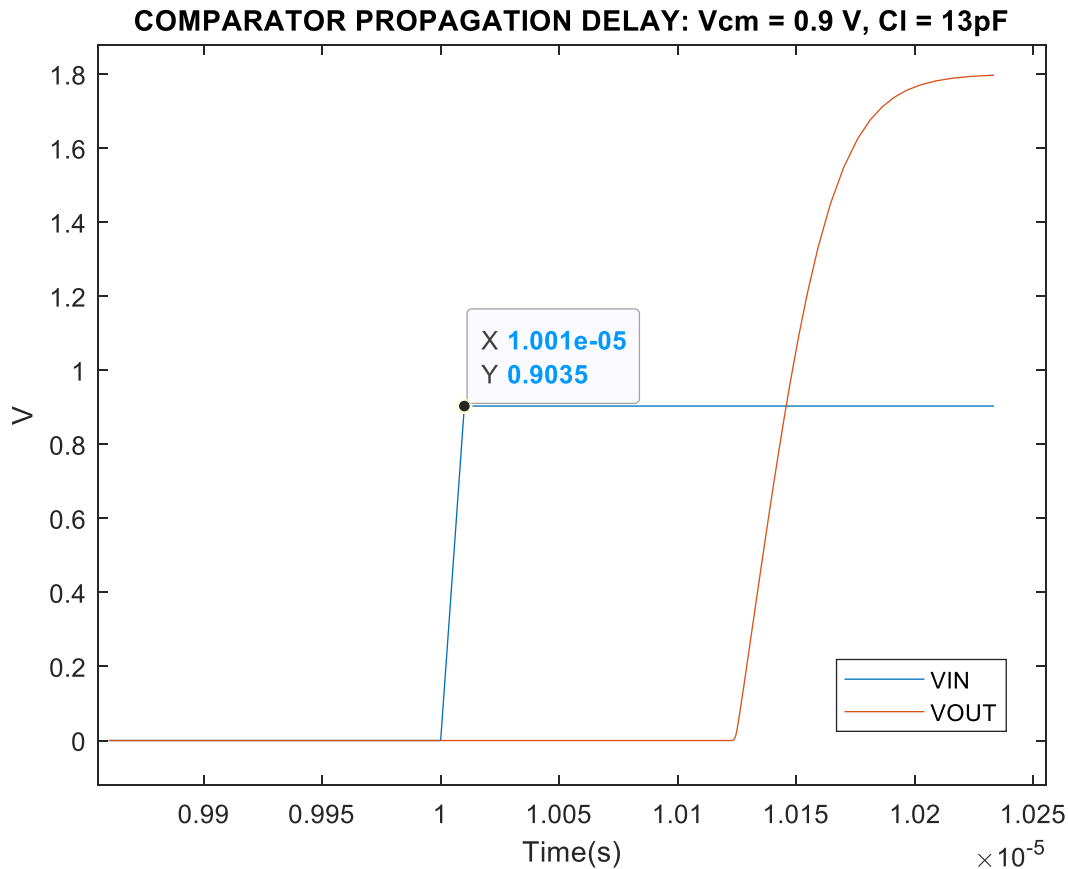
Figure 3.27. Comparator propagation delay

The propagation delay was measured from the instance the small overdrive voltage was applied until mid-scale (0.9 V) was reached on the output (VOUT). With a load capacitance of 13pF, the rising propagation delay was found to be 137 ns. Similarly, the falling propagation delay was 185 ns. The rise and fall times were 34 ns and 24 ns, respectively. As the comparator sensitivity and speed is affected by the overdrive voltage, this propagation delay can be reduced by increasing the gain and bandwidth of the preamplifier stage or by adding additional gain stages. The summary of results for the comparator are shown in Table 3.5. The results are acceptable as they meet the resolution and speed requirements required; approximately 3.5mV and 1.25 microseconds, respectively. The speed requirement corresponds to half the period of the sampling frequency.

Table 3.5. Summary of Simulated Comparator Parameters

Parameter	Specification	Simulated Value
Input Offset Voltage *(Vcm=0.9V)*	3.5 mV	0.19 mV
Propagation Delay Rising *(Vod=3mV,Vcm=0.9V)*	1.25 μs	137 ns
Propagation Delay Falling *(Vod=3mV,Vcm=0.9V)*	1.25 μs	185 ns
Rise time *(Cl=13pF)*	1.25 μs - P_{DR}	34 ns
Fall time *(Cl=13pF)*	1.25 μs - P_{DF}	25 ns
Quiescent Current	200 μA	102 μA

3.7 System Level Simulation

The system level simulation of the converter requires a variable input voltage source, clock signal, reset signal and a start signal. For the system level simulations, a 400 kHz clock signal along with a start and reset signal were applied to the circuit with rise and fall times of 10 nanoseconds. The input voltage is ramped from ground to VREF with a slow ramp signal adequate for linearity plots with a 0.1 LSB resolution. The input ramp signal is applied to "VIN" from ground to 1.8 V with a rise time (T_{vin}) calculated based on Eq. (14).

$$Tvin = 2^N * \frac{Cc}{Fs} * B \hspace{3cm} (14)$$

N is the number of bits while C_c is the number of clock cycles per conversion including the valid. F_s is the sampling frequency, and B is the number of bins per code (10). The output bit lines were imported into MATLAB and post-processed by combining them into an output string based on the respective valid end of conversion signal. The simulated transfer characteristic is shown in Figure 3.28 where the output code is shown as a function of the input voltage.
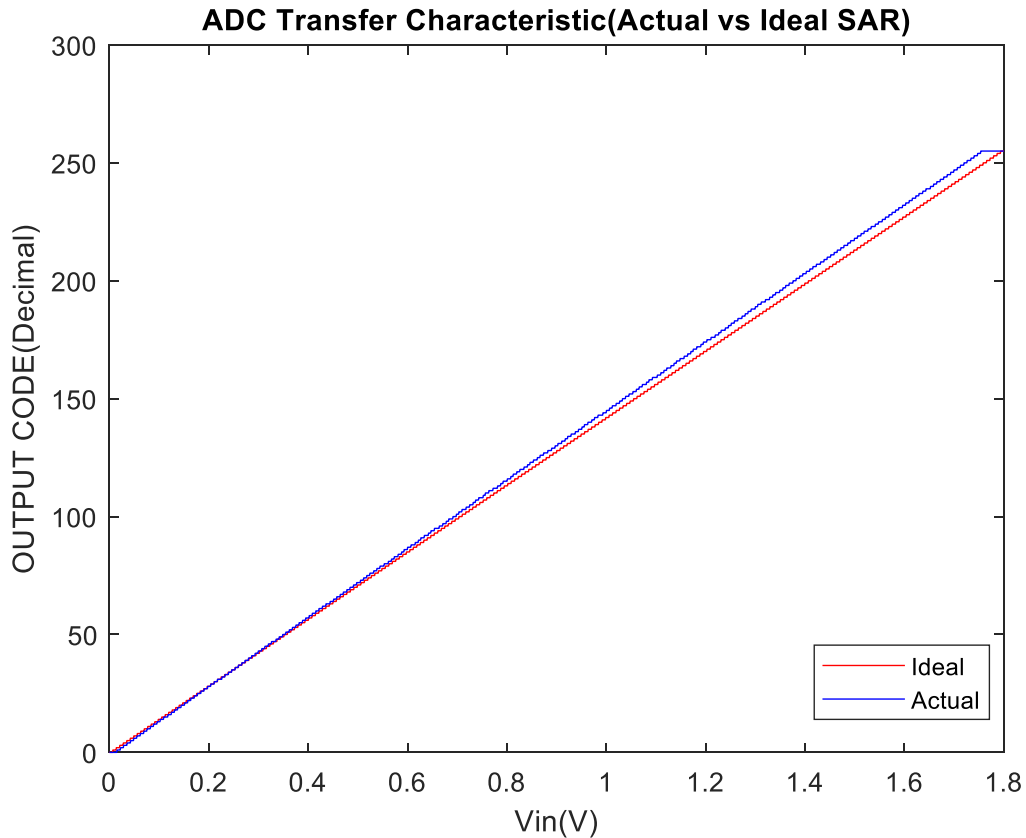
Figure 3.28. Simulated ADC transfer characteristic with ideal

The offset and gain error associated with the ADC transfer characteristic is -2.2 LSB and +8.2 LSB, respectively. These results are satisfactory as the offset and gain error are well outside the sensors' output range we are looking to digitize. With a large offset or gain error, the dynamic range of the sensor is limited and causes the ADC to saturate within the operating range of the sensor.

From the simulated ADC transfer characteristic, the DNL figures were established using MATLAB as well. The width of each output code from the transfer characteristic was measured and compared to the ideal width of the code, which in this case, is ten. Ten was selected to be able to get fair amount of resolution (0.1 LSB) and also keep simulation times reasonable. The DNL for the simulated transfer characteristic is shown in Figure 3.29.
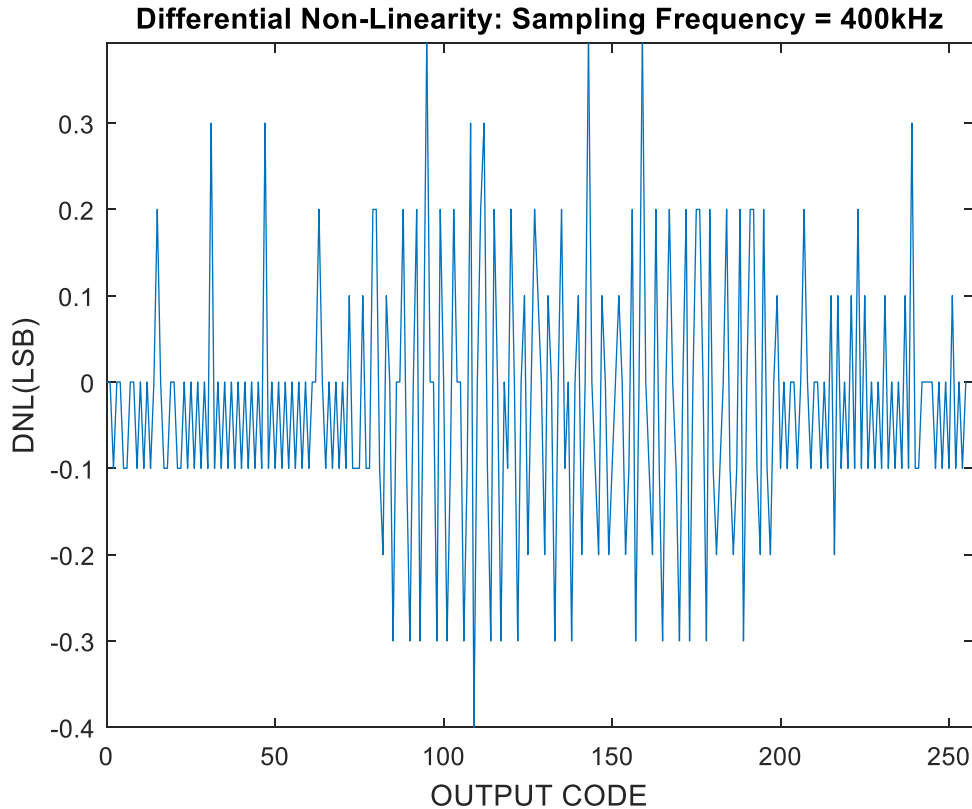
Figure 3.29. Simulated ADC DNL

The minimum and maximum DNL values is -0.4 LSB and 0.5 LSB, respectively. Ideal values for DNL would be zero for the full ADC range. It is seen the DAC has a major influence on the ADC transfer characteristic. As previously discussed, the periodic spikes are a result of parasitic capacitances related with the layout of the DAC capacitor array. Also, positive gain error results in an average DNL value of less than 0. These results are expected based on simulation results for the DAC transfer characteristic.

Figure 3.30 shows the simulation results corresponding the INL of the ADC transfer characteristic. The INL of the transfer characteristic is extracted by performing a sum of each individual DNL value from output code 0 to 255.
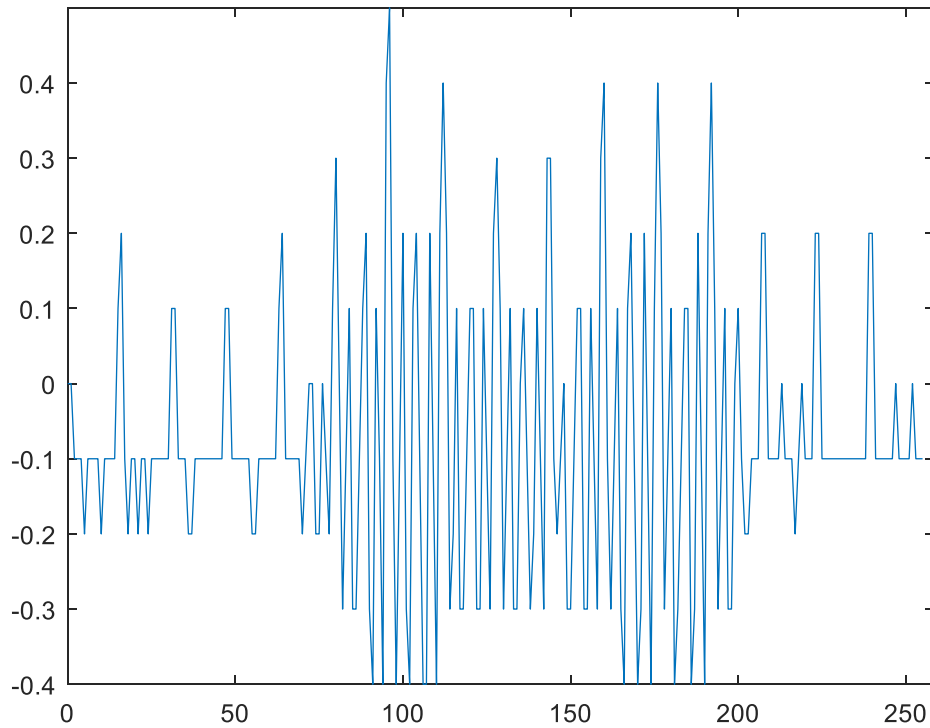
Figure 3.30. ADC INL

The minimum and maximum values for the INL is -0.4 LSB and +0.5 LSB, respectively. Also, the

ideal value for INL is 0. The DAC's capacitor array parasitics has the greatest influence on the

INL characteristic as well. These results are deemed acceptable as the DNL and INL results are

comparable with other published works such as in [25] and [26].

3.8 Layout

When implementing the SAR ADC with a capacitive array DAC, the accuracy can be

largely affected by the process variation in capacitors. According to [27] the major sources of error

in realizing capacitors is over-etching and oxide thickness gradients across the surface of the

microcircuit. The effects of over-etching generally dominate and can be minimized by realizing

larger values of capacitance using a parallel combination of smaller, unit-sized capacitors. Also,

by arranging the capacitors in a common centroid layout, oxide gradient changes affect all

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capacitors in the same way. For the DAC capacitor array, a modgen was created that allows patterning of the unit capacitances in a common centroid style layout. Both the MSB and LSB capacitor array were developed by using a modgen [28] and connected via the attenuation capacitor as depicted in the schematic in Figure 3.9. The complete ADC layout is shown in Figure 3.31.

Figure 3.31. Complete ADC layout

Chapter 4: TESTING AND CHARACTERIZATION

This chapter covers the testing of the fabricated device received from the foundry. The SAR ADC is tested on the system level along with the subcircuits comprising the SAR ADC. As there are many I/O pins and level shifters required for testing the ADC sy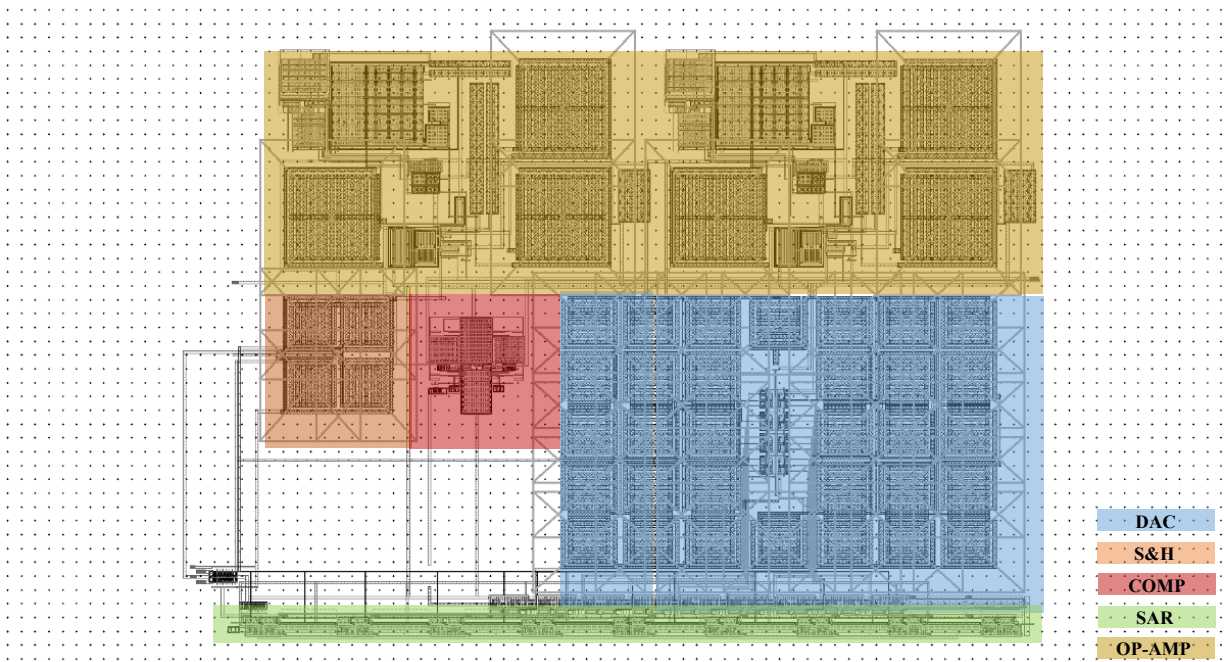stem design, a PCB was developed to extract the ADC transfer characteristic. The SAR algorithm and DAC were also tested on the PCB because of the high number of I/O pins and logic level translators needed for the testbench. The remaining subcomponents, the comparator design and sample-and-hold, were tested on the die level. With the ADC system level measurement and testing of the individual subcomponents, there will be insight to the performance of the ADC and the contributing factors. Section 4.1 covers the ADC system level testbench and measurement results. Sections 4.2 – 4.6 cover subcomponents of the ADC; the SAR, sample and hold, operational amplifier buffer, DAC and comparator.

4.1 ADC DC Characteristics Testbench and Measurements

To measure the fabricated ADC's static DC characteristics, a testbench was created utilizing a printed circuit board. The printed circuit board was created using Allegro PCB Designer to host the packaged die. Several testbenches were included in the PCB design for testing the various circuits related to the 433 MHz transmitter and power regulation. The packaged die and necessary IO pins were soldered onto a printed circuit board along with logic level translators to convert the 3.3 V logic from the FPGA to 1.8 V logic. The PCB design artwork and the fabricated PCB is shown in Figure 4.1. and 4.2, respectively.
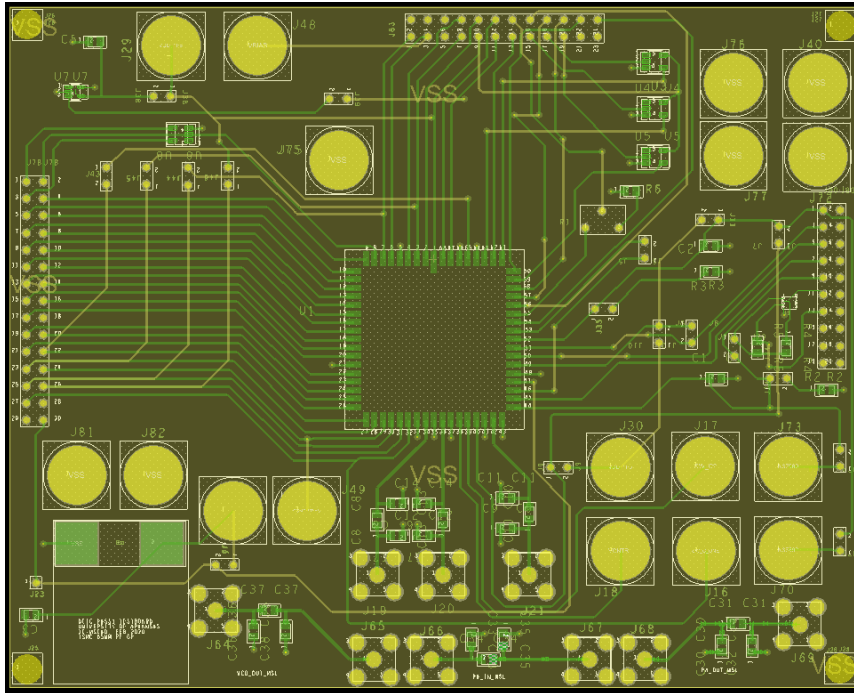
Figure 4.1. PCB test-board
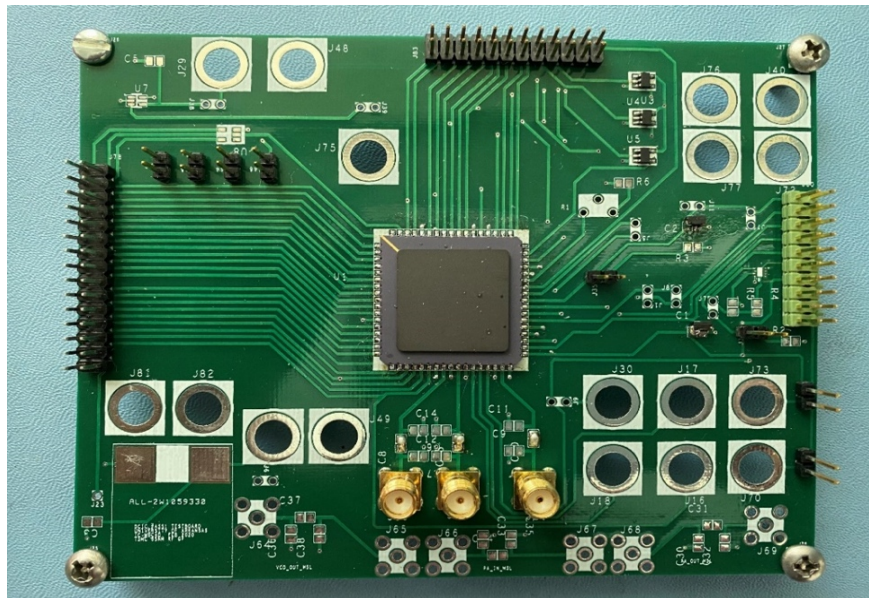
Figure 4.2. Populated PCB test-board

The equipment required for the ADC testbench includes a DC power supply, function generator, an Altera Cyclone II FPGA and a mixed signal oscilloscope. The ADC transfer characteristic is captured by applying a slow, increasing ramp function using the function generator

and providing the necessary control signals (CLK, RESET, START) via the FPGA. To capture the output, the oscilloscope is connected to the ADC output bits via the oscilloscope logic probes. After each cycle, the program checks for a valid signal (EOC) to detect any errors in completing any conversions during the process. If a valid signal is not present, the program flags an LED. Figure 4.3 shows the test setup for the ADC system level measurement, excluding the DC power supply.
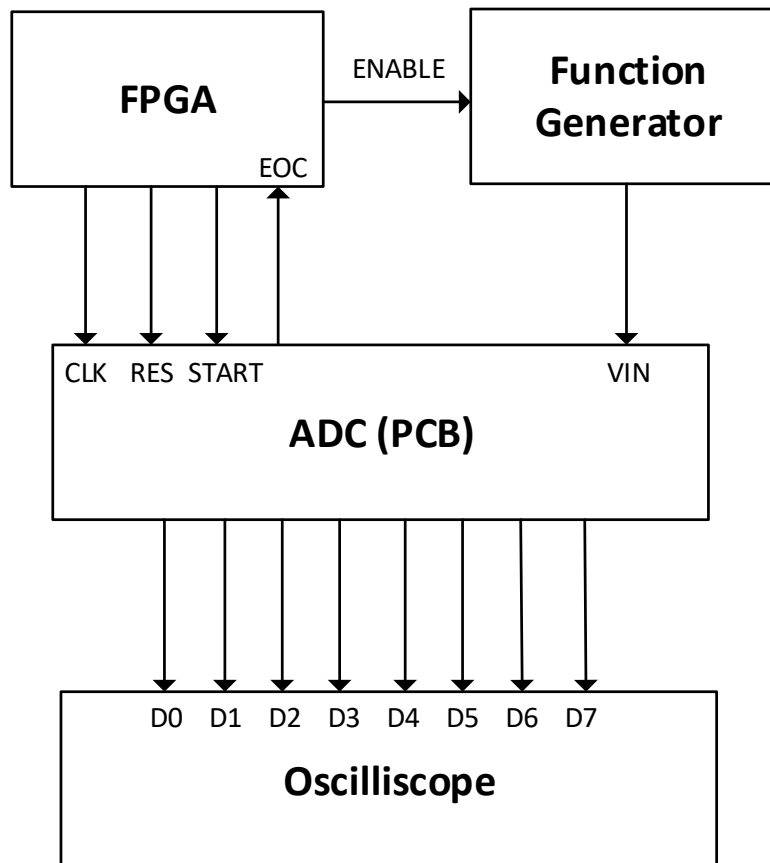
Figure 4.3. ADC testbench

The Altera FPGA was coded to provide the necessary control signals to properly operate the ADC. Using Quartus software, a module was developed in VHDL and subsequently simulated in ModelSim for verification. The bus clock signal was derived from the 50 MHz system clock and the appropriate reset, start and enable signals were programmed using the rising and falling

edges of the bus clock. At the beginning of each cycle, the ADC performs a reset to enable sampling and to clear any data stored in the DFFs during power on or during a previous conversion cycle. A start signal is provided to allow the conversion to begin on the rising edge of the next clock after assertion. Also, an enable signal is provided for the function generator to externally trigger the ramp signal. Figure 4.4 shows the FPGA control signals provided to the ADC for each conversion period.
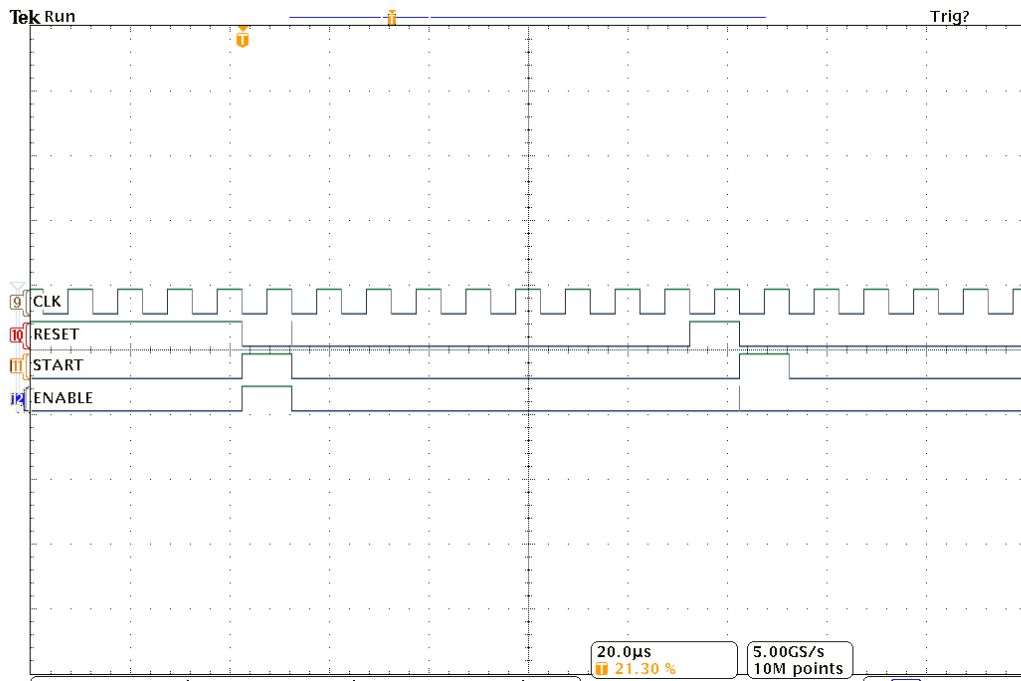
Figure 4.4. FPGA control signals

Along with the proper DC supply and bias voltages, the testbench shown previously in Figure 4.3 was implemented. The ADC transfer characteristic was captured by the digital logic probes of the oscilloscope and post-processed using MATLAB. At the end of each conversion period, each individual output code was extracted using the valid (EOC) signal and subsequently stored into an array. The output code as a function of the input voltage along with an ideal characteristic curve is shown in Figure 4.5.
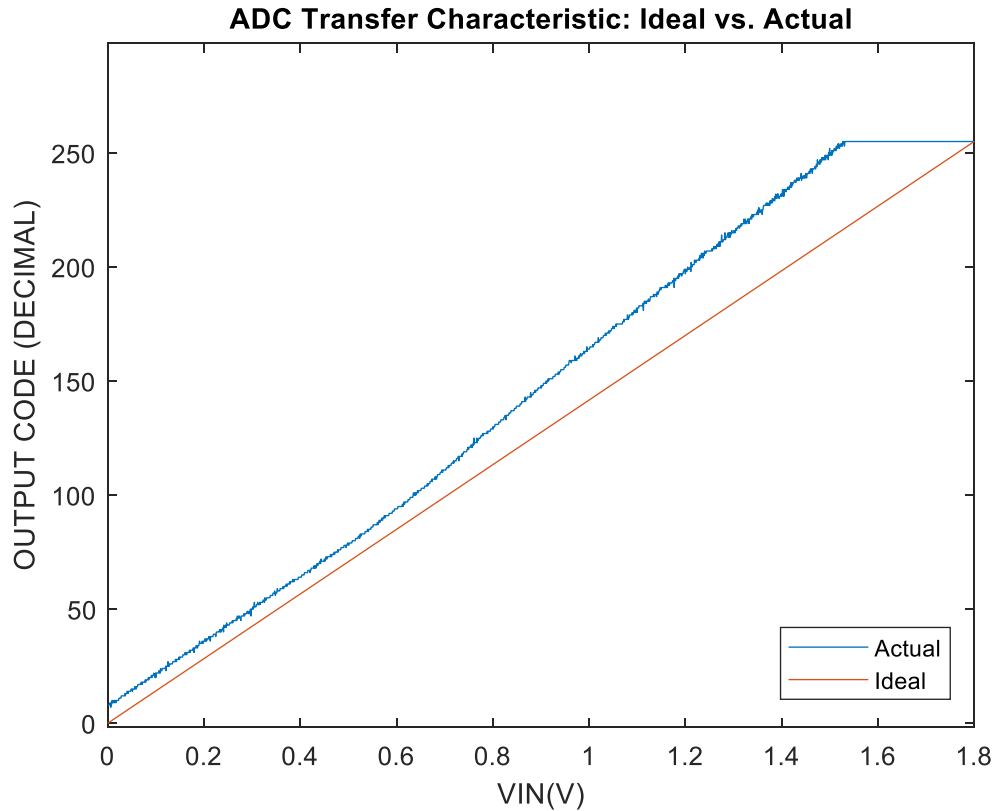
Figure 4.5. ADC transfer characteristic: ideal vs. actual

The actual measured transfer characteristic shows positive offset and gain error, +7.1 and +31.1 LSB, respectively. Observing the measured characteristic, there appears to be a fair amount of noise present which alludes the fact. Comparing the measured data with an ideal SAR ADC as shown in Figure 4.5, the measured data shows two distinct slopes which convey there is some degree of nonlinearity in transfer characteristic.

For the DNL of the transfer characteristic, the width, or the number of successive hits for each output code, was extracted from the transfer characteristic. The measured DNL is shown in Figure 4.6.
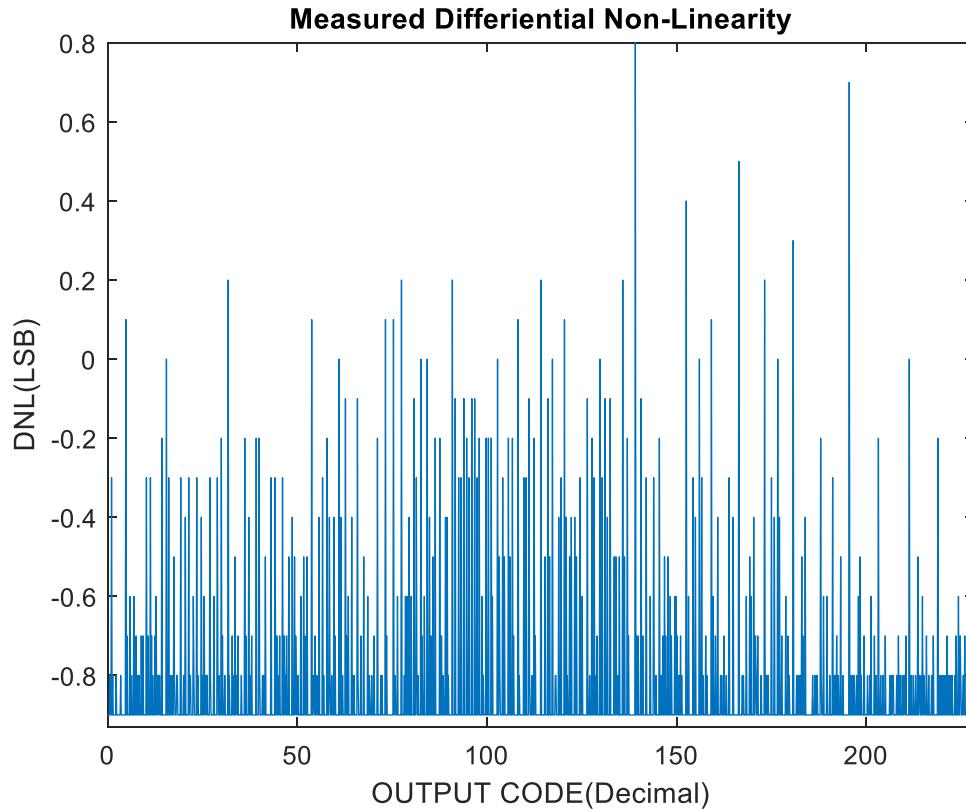
Figure 4.6. ADC DNL

The minimum and maximum values for the DNL is -0.9 and 0.8 LSB, respectively. The DNL shows significant noise present in the system that exceeds the threshold value of LSB/2. The DNL is affected by combined noise in the individual blocks of the ADC. The degraded DNL performance in this case is most likely attributed to random error in the sample and hold circuit or comparator sensitivity as the error from one cycle to the next varies greatly.

To extract the INL, the best fit method was used to calibrate the offset and gain error associated with the transfer characteristic. The best fit line for the measured data is shown in Figure 4.7. The measured data was subtracted by the best fit line to show the nonlinearity associated with the transfer characteristic.
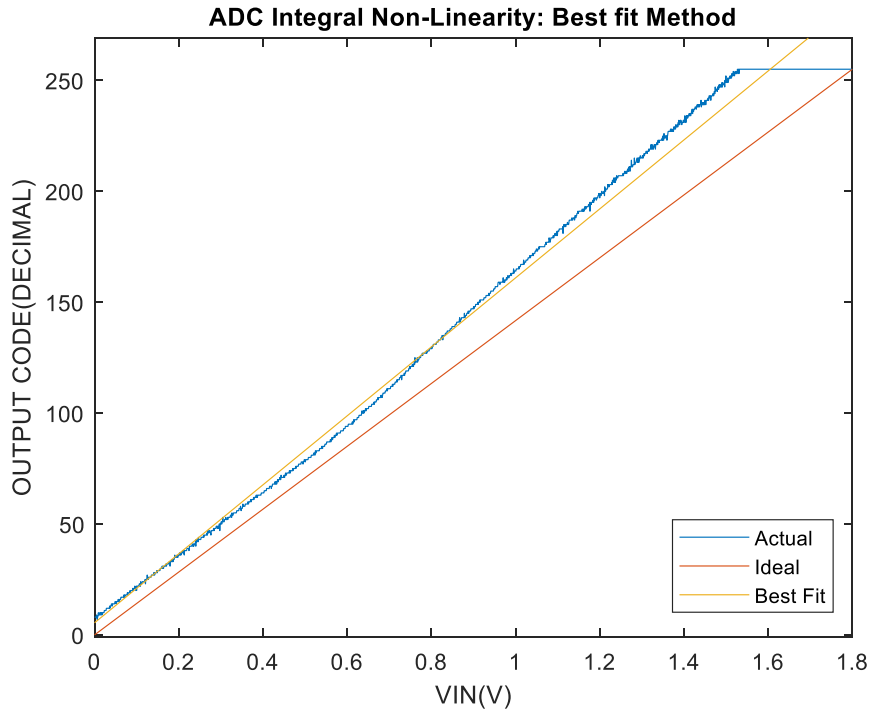
Figure 4.7. ADC transfer characteristic with best fit line

The measured data shown in Figure 4.8 shows an INL from -4.6 LSB to +12 LSB. From observation, a slope change near output code 85 is easily distinguishable. Since this slope transition is near the threshold voltage of the NFET, the nonlinearity of the ADC transfer characteristic could be largely affected by the complementary input stages of the op-amp and comparator circuits.
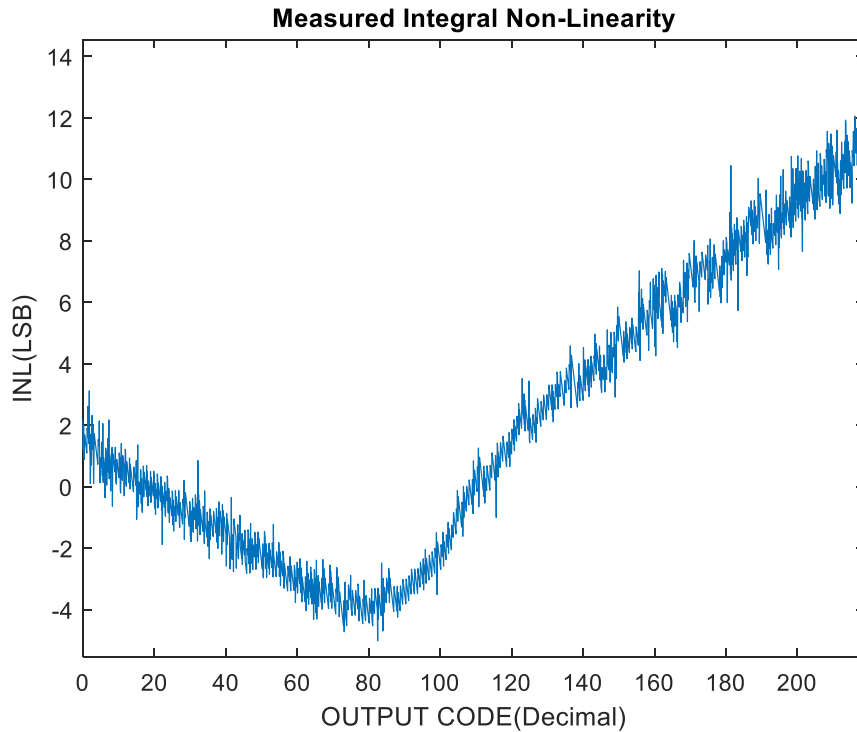
Figure 4.8. Measured integral non-linearity (best fit)

The measured results are compared to the simulation results in Table 4.1. The device's measured system level performance in regard to the DC static errors have increased significantly.

Table 4.1. Simulated vs. Measured ADC Specifications

Parameter	Simulated	Measured
Offset Error	-2.2 LSB	+7 LSB
Gain Error	+10.2 LSB	+31.1 LSB
DNL	-0.4 LSB, +0.5 LSB	-0.9 LSB, + 0.8 LSB
INL	-1.1 LSB, + 1.8 LSB	-4.6 LSB, +12 LSB
Power Consumption	21.4 nJ/conv	24.4 nJ/conv

It is worth noting that in regard to the application, the INL error figure will be reduced. The temperature sensor's operating range is limited from 0°C to 85°C which corresponds to an output voltage of 865mV to 1.567V. As the ADC will only digitize this voltage range, the transfer characteristic for this region of interest is shown in Figure 4.9.

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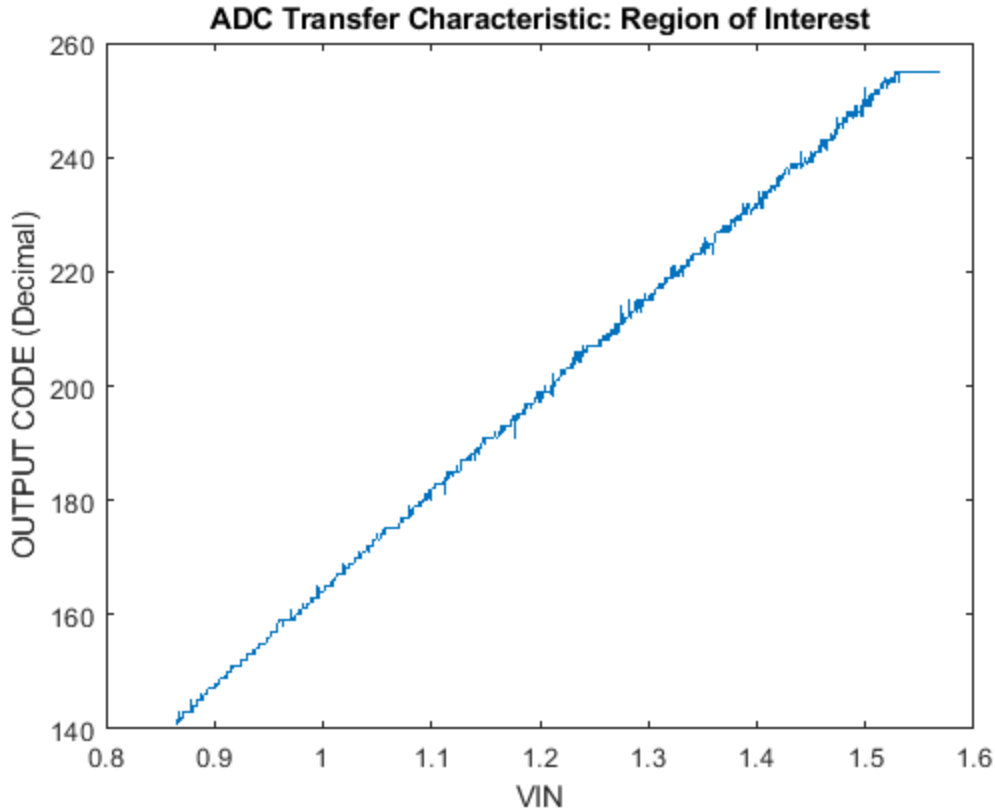
Figure 4.9. ADC transfer characteristic for region of interest

The magnitude of the DNL errors are still present however, the sensor's actual range will not see the nonlinear effects of the slope change as seen previously in Figure 4.8. In Figure 4.10, the INL figures are established using the best fit method for the region of interest. The INL minimum and maximum values are from -3.5 LSB to +2.8 LSB, respectively, which is much improved from the overall ADC INL characteristic. It is seen that the INL in the region of interest is much more a function of random noise than dynamic offset. In the following sections, testing of the subcomponents of the ADC should give insight to the performance of the ADC in regard to these DC errors.
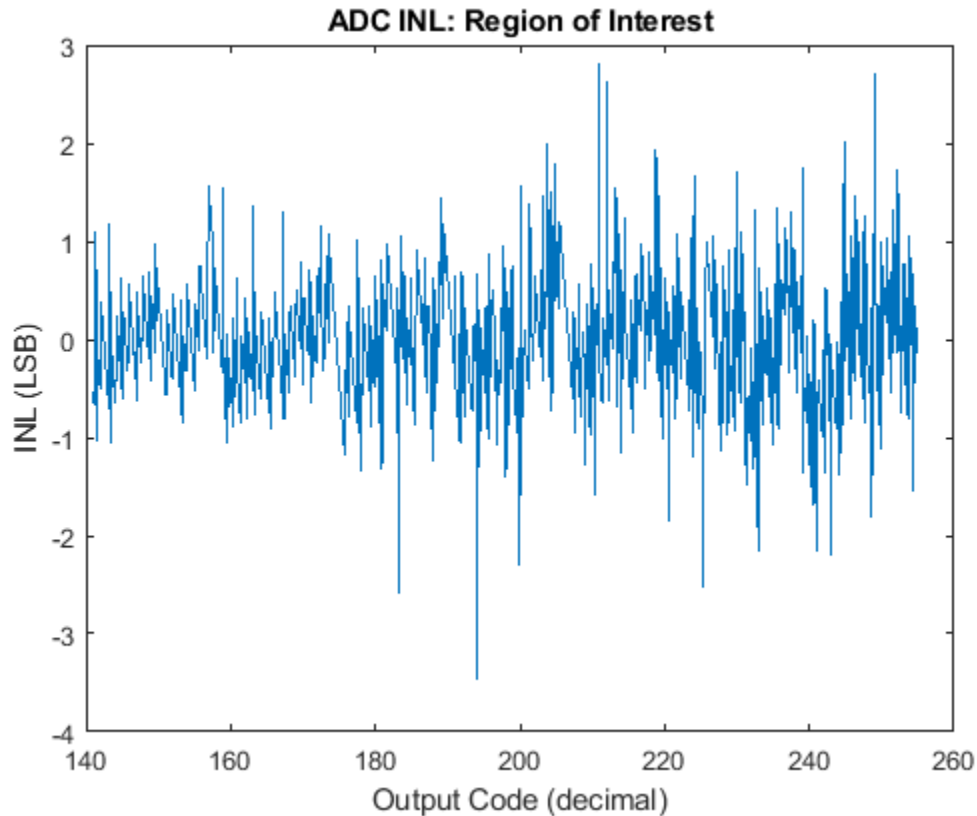
Figure 4.10. ADC INL characteristic for region of interest

4.2 Successive Approximation Register

The SAR algorithm is implemented by a shift register and registers that store feedback provided by a comparator. To test the proper operation of the SAR, a binary counter was constructed using the Altera Cyclone II FPGA. VHDL code was developed in Quartus software to cycle through all possible binary combinations able to be stored in the 8-bit SAR. This was implemented by generating a feedback signal (COMP-IN) that stores the binary combinations in the registers at the designated clock edges in the conversion cycle. Figure 4.11 shows how the register stores bits in binary order from "binary 0" to "binary 6" as given by the feedback signal "COMP-IN." The PCB and PCB I/Os were used to feed the DC supply voltage and connect the 8-bit output and relevant control signals to FPGA and digital probes of a mixed-signal oscilloscope. All possible outputs for the SAR from binary 0 to binary 255 were verified in MATLAB.
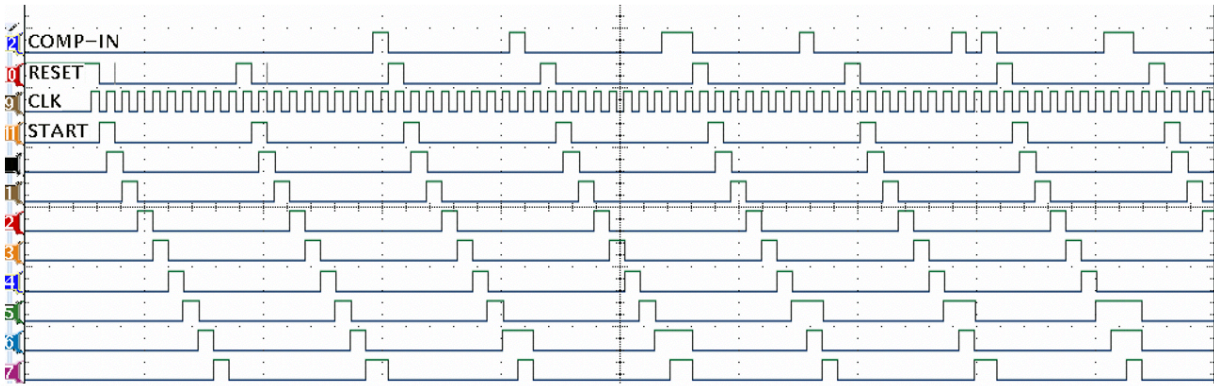
Figure 4.11. SAR operation

4.3 Operational Amplifier

The operational amplifiers are utilized in the unity gain configuration to provide a current source to drive off-chip load capacitance of the measurement equipment. Several key parameters were measured to give the performance of the fabricated device. The open loop gain was measured by applying a 900mV DC on the inverting terminal and sweeping the non-inverting terminal in 1mV increments using a function generator. After canceling the offset, it was determined that a 1mV increase in the input voltage caused the output voltage to saturate to the rail voltage of the op-amp. Given that minimum step size of the measurement equipment is 1mV, the open loop gain was estimated by Eq. (15) where dV_{out} is 1.8 V and dV_{in} is 1mV.

$$Av = 20 * log\,(dVout/dVin) \tag{15}$$

The open loop gain was calculated to be approximately 65 dB which meets the specification indicated in Chapter 3. Next, the unity gain frequency was determined for the op-amp. The limitations of the measurement equipment make building a Bode plot in the open loop configuration difficult. Because of this, the op-amp was arranged in the unity gain configuration where the frequency response was measured using a 1 V pk-pk sine wave with a 900 mV DC offset provided by a function generator. The output as a function of input frequency was measured from

approximately DC to 5MHz and is shown in Figure 4.12. The V_{out} was found to attenuate below 1 V at a frequency of 3.9 MHz.
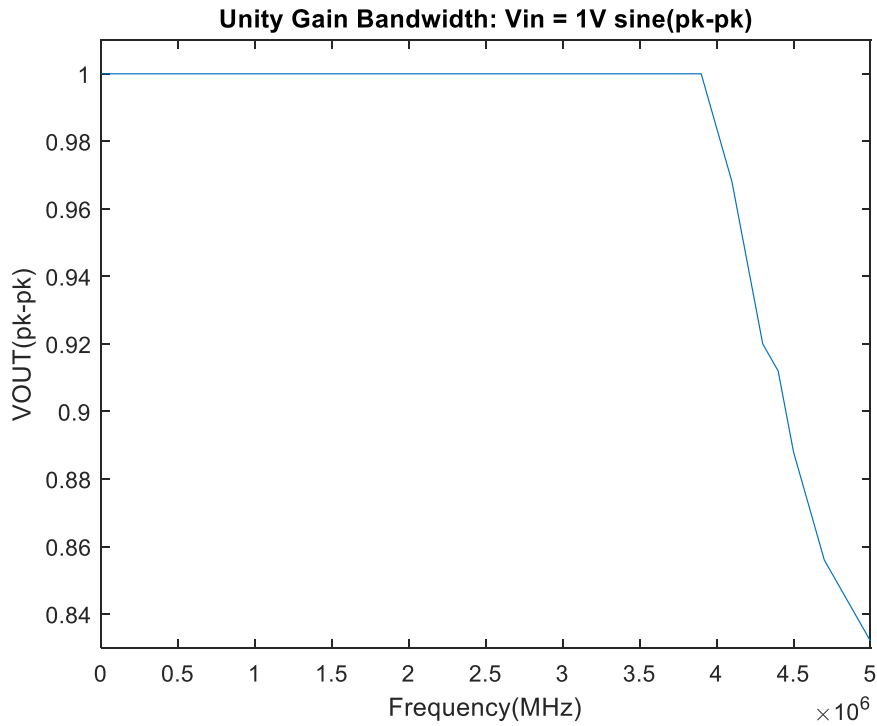
Figure 4.12. Measured unity gain frequency

As this circuit would be supplied by a non-ideal source such as an LDO, there can be power supply variations that cause unintended effects on the op-amp output voltage. The power supply rejection ratio (PSRR) performance shows the ability of the operational amplifier to reject power supply variations. The test setup is delineated in [29]. As the output stage includes a large value for Miller capacitance, the PSRR performance is degraded as the power supply can be coupled through the gate-to-source capacitance of the output stage. Figure 4.13 shows the PSRR performance measured with a supply voltage ripple of 200 mV and 900 mV common mode input voltage. Note that AC coupling is applied to remove the DC offset associated with the waveforms.
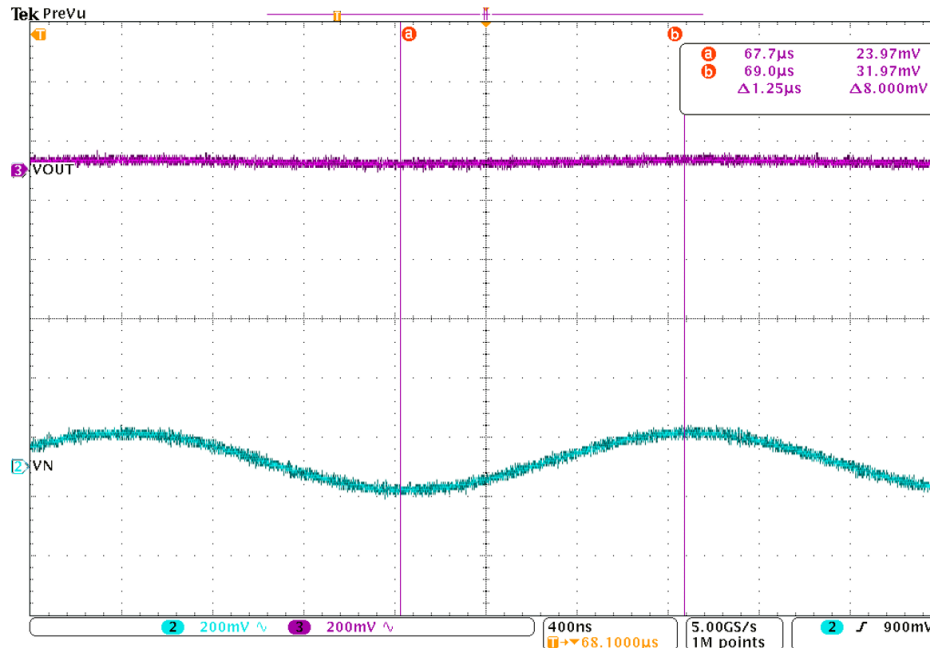
Figure 4.13. Measured PSRR

The PSRR is calculated to be 48.93dB. Table 4.2 summarizes the measured results for the op-amp buffer for each of the specifications. These results are acceptable with regard to its functionality as a buffer. With regard to the op-amp's influence on the ADC transfer characteristic, the input offset voltage has an adverse effect on the integral nonlinearity. As the op-amp's complementary inputs have random mismatch due to the fabrication process and the offset voltages corresponding to each input pair varies, nonlinear error is introduced in the characteristic.

Table 4.2. Summary of Measured OP-AMP Buffer Parameters

Specification	Spec Value	Simulated Values	Measured Value
DC Gain	55 dB	78.2 dB	65 dB
Unity-Gain Frequency	1 MHz	22.39 MHz	3.9 MHz
Slew Rate (Cl=13pF)	3.6 V/μs	8.87 V/μs	9.6 V/μs
V$_{OH}$	1.567 V	1.794 V	1.72 V
V$_{OL}$	865 mV	700 μV	44 mV
Quiescent Current (V$_{CM}$=0.9V)	400 μA	227 μA	286 μA

4.4 Sample and Hold

The sample and hold circuit was tested by verifying both the sample and hold phase of the sampling switch. A probe station, DC power supplies and function generator were used to test the bare die test structure. In the sampling phase of the switch, the output voltage should follow the input voltage as both transmission gate switches are closed. During the hold phase, the output voltage should no longer track the input signal and should remain fixed while the switch is opened. The sample and hold output as a function of the 100kHz sinusoidal input signal and 200kHz enable signal is shown in Figure 4.14. While the switch is enabled, V_{out} follows the input waveform with some clipping shown near the rails of the power supply. While the switch is disabled, V_{out} is remains constant as expected. One of the factors affecting the accuracy of the sample and hold is the error voltage held on the holding capacitor while the switch is being disabled. The sampled signal with the included error is compared with the DAC by means of the successive approximation algorithm.
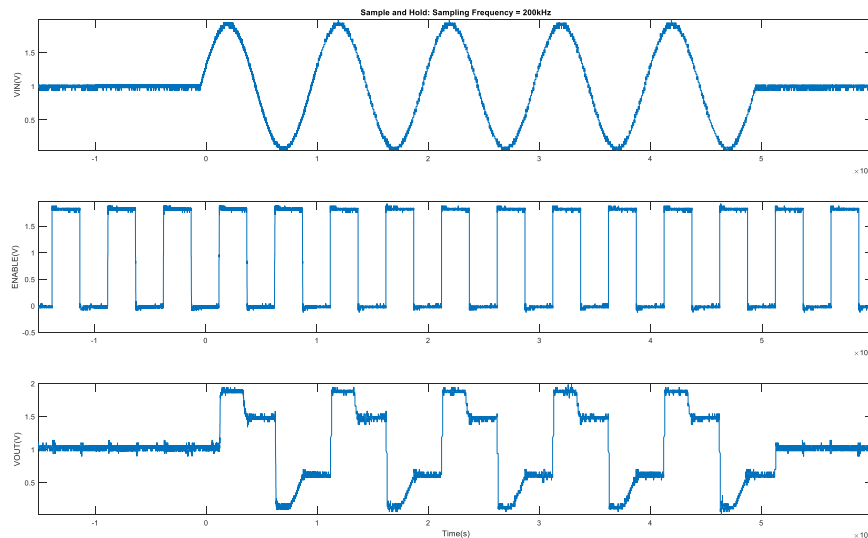
Figure 4.14. Sampling switch operation

The sample and hold circuit will operate with an input signal that is practically constant DC. In Figure 4.15, one ADC sample is shown along with the DAC and comparator feedback signals. One of the issues noticed in the transient response is the positive hold step that occurs at the beginning of every conversion cycle. This is undesirable as it causes the ADC to converge to an input signal with a random amount of error injected into the data path.
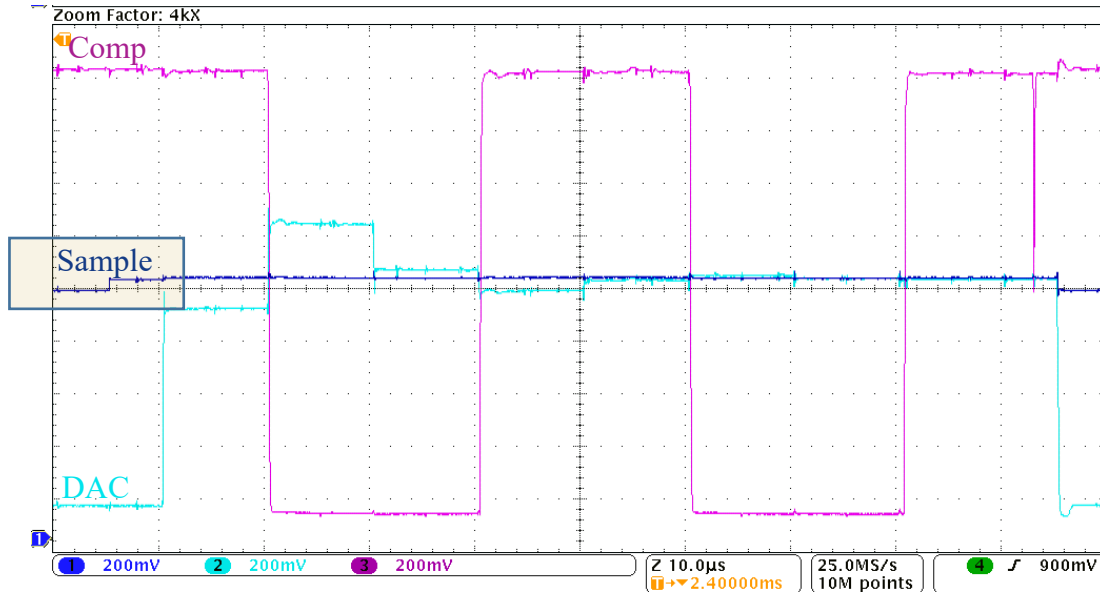
Figure 4.15. ADC successive approximation algorithm operation

This positive hold step is likely due to charge injection, clock-feedthrough, or a combination of the two. According to [12], the charge injection contributing to this error for a "symmetric" transmission gate sampling switch is discussed however, the same concepts do apply for an asymmetric TG. Although the complementary switched induce opposite charge charges when turning off, the input voltage dependency only allows complete cancellation of charges for one input voltage value [12]. Consequently, this phenomenon is adding non-linearity error in the sampling circuit. Clock feedthrough error through gate and gate-to-drain overlap capacitances are also believed to be coupling undesirable currents into the signal path. In [13], clock feedthrough charges in transmission gate switches are analyzed and models are created for the full conduction

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and half conduction periods during switch turn-off. The physical mechanisms described show that in the half conduction periods, where only one transistor is operating, account for most of the error. These operating periods are near the rails, which will consequently add nonlinearity to the ADC transfer characteristic, especially toward the extrema. Compensating the clock feedthrough error is possible by maximizing the amount the time drain current is flowing through the switch while turning off [13]. In testing, increasing the control signals' rise and fall times showed little to no improvement since internal buffers were included that drive the gates of the sampling switches.

4.5 Digital to Analog Converter

The DAC is a binary-weighted scaled charging array type. As process variation can cause mismatches in the sizes of the capacitors, this can be a major contributor in errors in the ADC's transfer function. The DAC is tested on the PCB using a DC power supply, FPGA and oscilloscope. As each bit corresponds to a weighted voltage value based on the output of the SAR register, the DAC transfer characteristic was seen by utilizing the shift register and manually controlling the feedback loop as what is demonstrated in Figure 4.11. This increasing binary ramp in the SAR provides input to the DAC for conversion to analog. The digital signal was swept from 8-bit binary "0" to 8-bit binary "255" to extract all possible values of the DAC. The resulting DAC waveform of Figure 4.16 shows the DAC output as a function of the input sequence of bits.
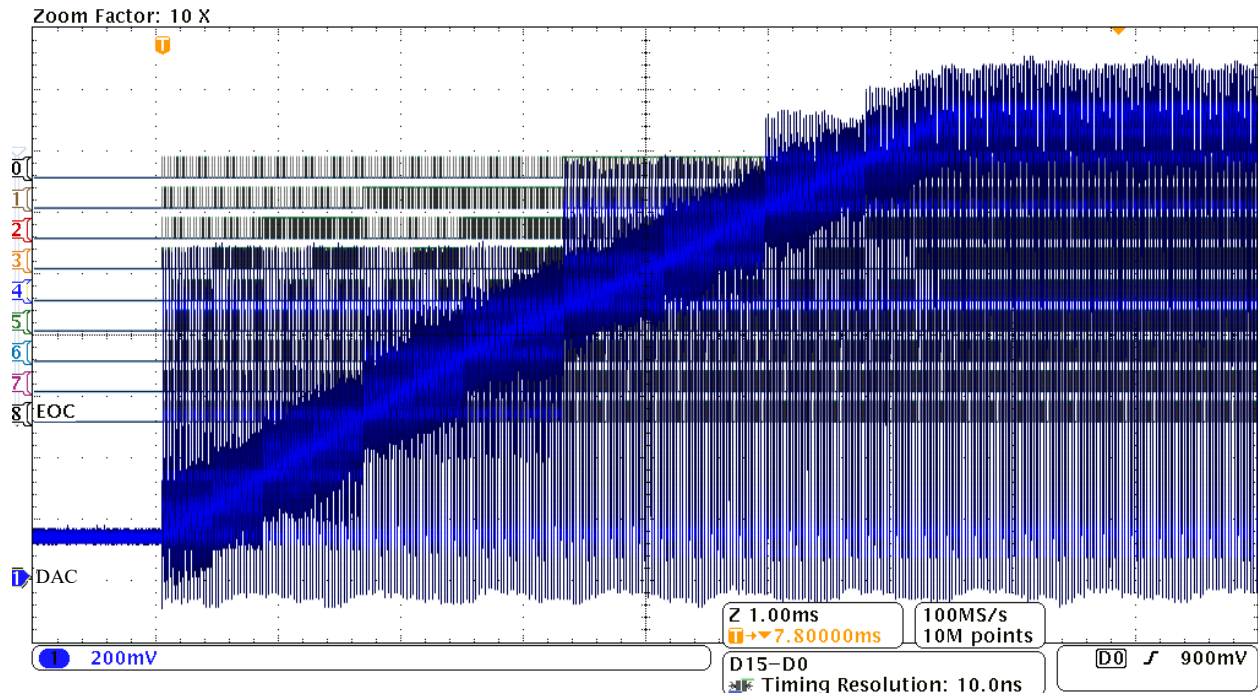
Figure 4.16. Transient DAC waveform

The "EOC" signal is used as a valid signal to indicate when the conversion is complete for each digital bit sequence from 8-bit binary 0 to binary 255. The resulting measured transfer characteristic in Figure 4.17 was extracted from the transient DAC waveform using the valid signal for all the corresponding digital input codes using MATLAB. For each input, binary 0 through binary 255, the value of the output voltage from the DAC was stored in a 1:256 array. The output voltage was then plotted against the input binary value converted to decimal. For an ideal split-charge DAC, the value of the output voltage can be calculated for each binary input by the following equation.

$$\left(D * \frac{VDD}{2^N}\right) \tag{16}$$

D represents the input binary code (in decimal) and N is the number of bits (8). This ideal transfer characteristic is included in Figure 4.17. The limited DAC range seen in the measured DAC transfer characteristic can show up as increased offset and gain error present in the ADC transfer characteristic assuming a perfect sample-and-hold.
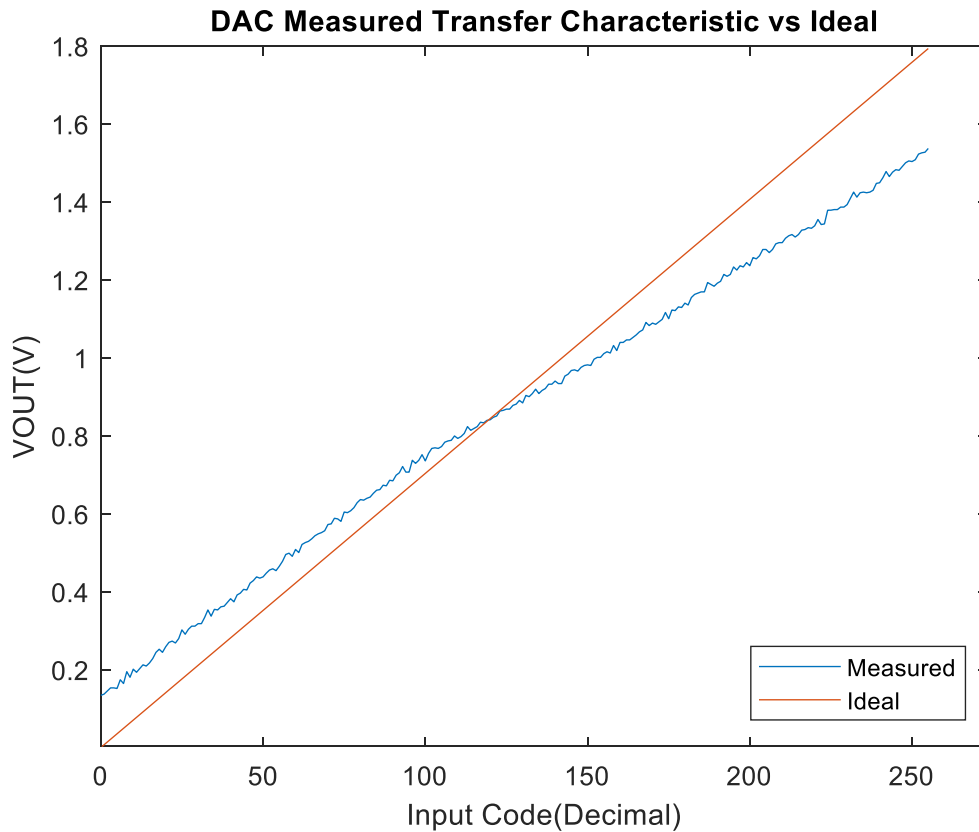
Figure 4.17. Measured DAC transfer characteristic vs ideal

Furthermore, the measured response shows a significant change in slope before midscale which relays there is nonlinearity in the DAC transfer characteristic. The measured transfer characteristic was further post-processed to determine the differential and integral nonlinearity. High levels of noise in the DAC is also shown by the increase in DNL as illustrated in Figure 4.18. For the DNL figures, the width of each binary step of the DAC output is compared the ideal LSB value.
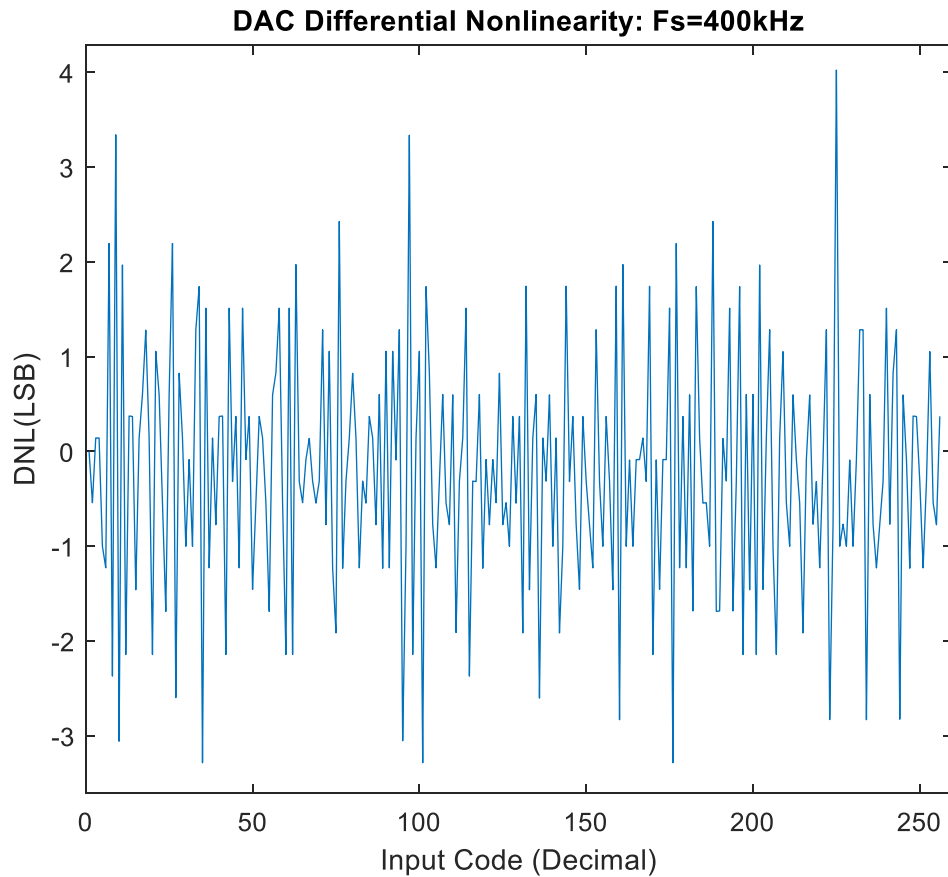
Figure 4.18. DAC differential nonlinearity

The measured DAC differential nonlinearity ranges from approximately -3.2 LSB to +4 LSB. It is expected that some of the DNL error is introduced by capacitor mismatch and some error is being contributed by the measurement equipment. To determine the integral non-linearity, the best fit approach was used to nullify the effects of offset and gain error in the transfer characteristic. The best fit line is shown in Figure 4.19. The measured transfer characteristic crosses the best line twice and shows two distinct slopes.
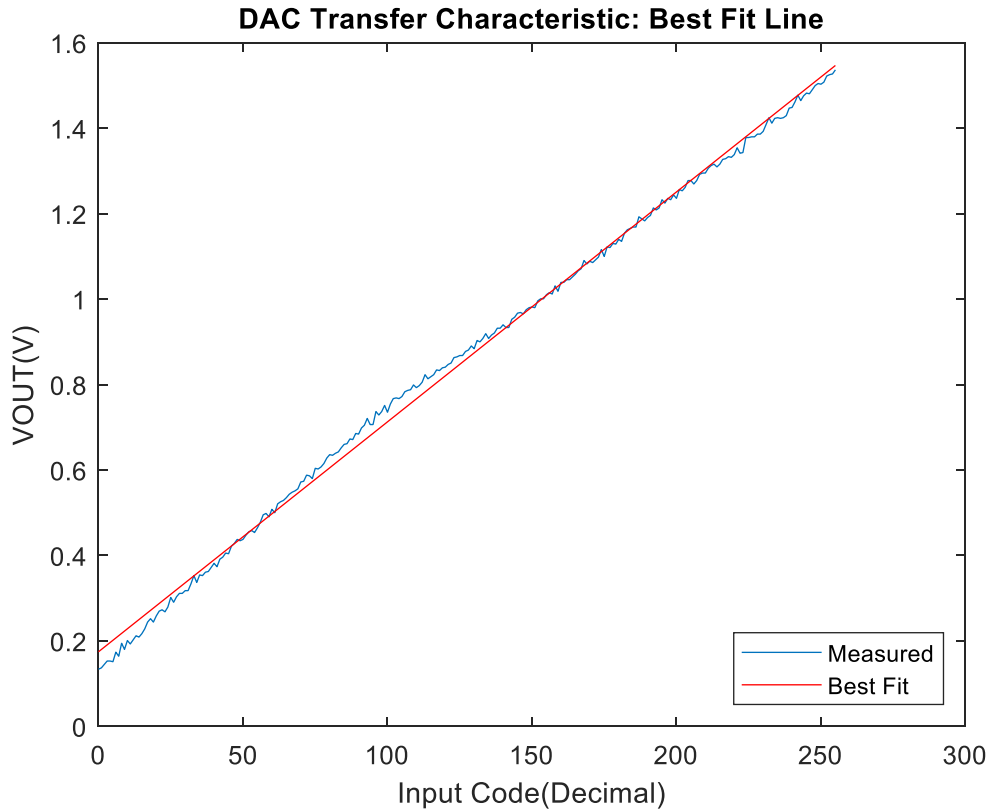
Figure 4.19. DAC transfer characteristic best fit line

Using the best fit line as a reference, the integral nonlinearity was calculated and shown in Figure 4.20. The minimum and maximum values for the INL of the DAC are -7.1 LSB and + 6.2 LSB. As the offset and gain error are canceled, it is seen that a slope change near code 90 occurs. This slope change is believed to due to the effects of switching between the complementary input pairs of the operational amplifier buffering the capacitive DAC output. Here it is likely that the offset voltage associated with the PFET differential pair is now dominated by the corresponding input offset voltage for the NFETs.
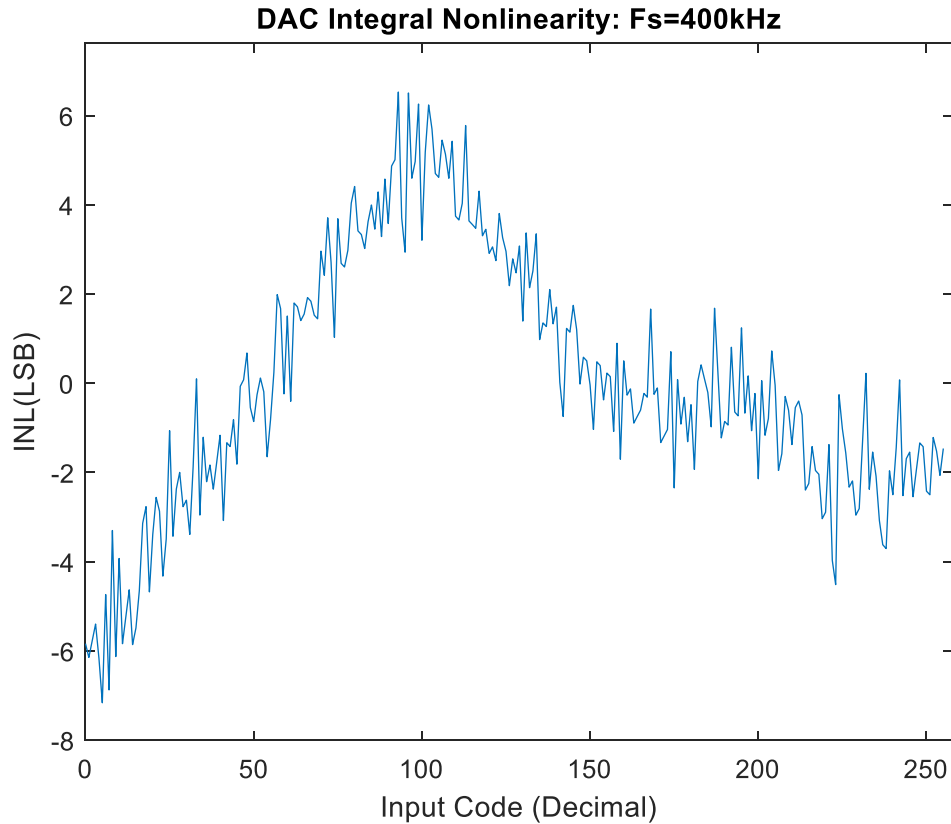
Figure 4.20. DAC INL using best fit method

The effects of the DAC transfer characteristic on the overall ADC characteristic are shown with the change in slope near output code 90. This negative change in slope in the DAC INL characteristic causes the ADC transfer characteristic to trend positive due to the successive approximation algorithm logic. One commonly known contributor to these errors is the input offset voltage due to transistor mismatch in the operational amplifiers. As these op-amps have complementary input pairs, this mismatch can affect both input pairs differently that can cause errors such as seen in Figure 4.20. Several techniques are discussed in [1] to calibrate out errors in INL and DNL and to trim offset errors associated with the operational amplifiers and comparators.

4.6 Comparator

The comparator performance was measured on the bare die with a Keithley source meter, function generator and an oscilloscope. The key parameters measured include the input offset voltage, sensitivity, and the propagation delay of the fabricated design. Input offset voltage is defined as the differential voltage necessary between the inputs of the comparator for the output to transition from one logic level to the other. The input offset voltage is caused by transistor mismatches in the design which can be minimized but not completely removed. To determine the offset, a mid-scale reference voltage (0.9 V) was given to the inverting terminal of the comparator while the non-inverting terminal is manually swept using a DC voltage.

For this design, the comparator requires a sensitivity of LSB/2, which in this case is approximately 3.5 mV (V_{min}). This sensitivity indicates the minimum voltage difference that can be detected between the input sample voltage and the DAC output voltage. Referencing Figure 4.21, the sensitivity was measured by applying a reference voltage $V_{ref,}$(light blue) on the inverting terminal and a pulse (dark blue) with an amplitude range from ground to 3 mV above V_{ref} on the non-inverting terminal. V_{out} (magenta) transitions from low to VDD/2 after a time delay of approximately 130 ns.
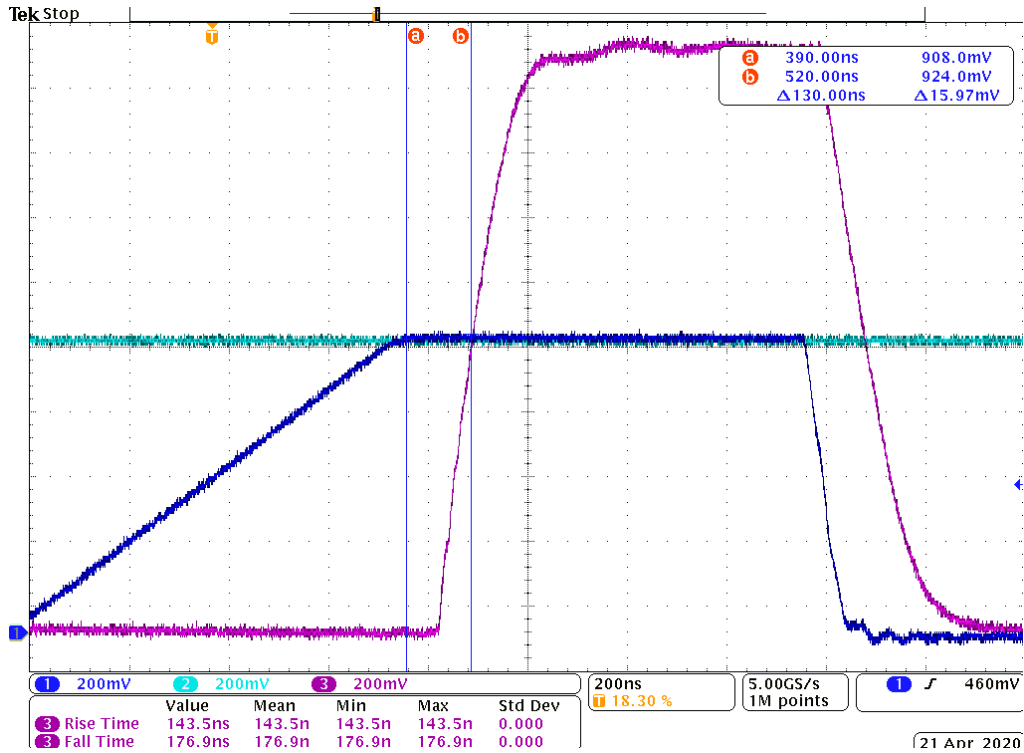
Figure 4.21. Comparator rising transient response

Referencing Figure 4.22, the falling transient response was captured by applying a reference voltage V_{ref},(light blue) on the inverting terminal and a falling pulse (dark blue) with an amplitude range from VDD to $V_{ref} - 3$ mV on the non-inverting terminal. The comparator output (magenta) transitions from VDD to VDD/2 with less than the minimal required resolution (V_{min}) and a delay time of approximately 396 ns. As the comparator testing shows that it can detect the minimum resolution required, the offset voltage dynamically varies for the full input common mode range. For an input common mode range from 0 to the threshold voltage of the NFET, the offset voltage for the PFETs dominate. Conversely, the NFET offset voltage increasingly dominates as the input common mode voltage trends toward the positive rail. As the offset voltages for the NFET and PFET are due to random mismatch, the magnitude and polarity of the offset will rarely match and affect nonlinearity.
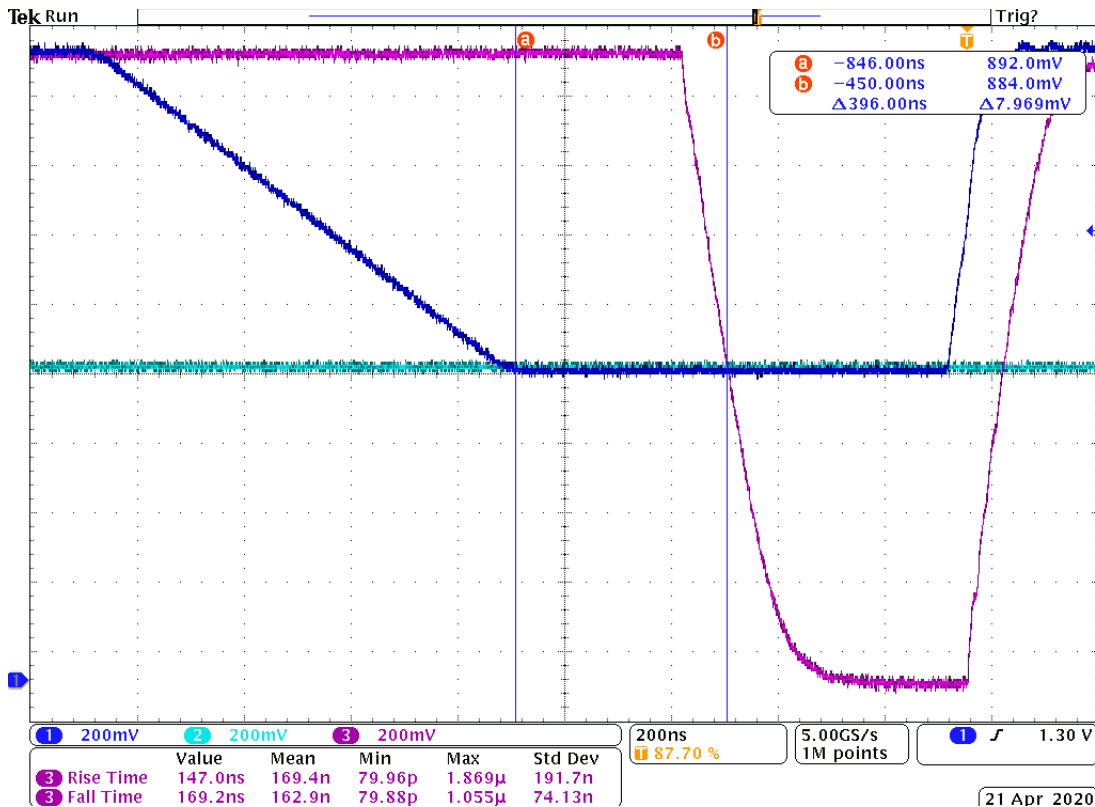
Figure 4.22. Comparator falling transient response

Table 4.3 summarizes the measure comparator parameter captured from the transient response characteristics. The results are acceptable as they meet the sensitivity requirements along with timing requirements derived from the sampling clock frequency. As the input offset voltage can change with the input common mode voltage, this will need to be addressed in future efforts.

Table 4.3. Summary of Measured Comparator Parameters

Specification	Spec Value	Simulated Values	Measured Value
Input Offset Voltage *(Vcm=0.9V)*	3.5 mV	0.19 mV	3 mV
Propagation Delay Rising (**P**_{DR}) *(Vod=3mV,Vcm=0.9V)*	1.25 μs	137 ns	130 ns
Propagation Delay Falling (**P**_{DF}) *(Vod=3mV,Vcm=0.9V)*	1.25 μs	185 ns	396 ns
Rise time *(Cl=13pF)*	1.25 μs - P$_{DR}$	34 ns	143.5 ns
Fall time *(Cl=13pF)*	1.25 μs - P$_{DF}$	25 ns	169.2 ns
Quiescent Current	200 μA	102 μA	83 μA

Chapter 5: FUTURE IMPROVEMENTS

Mitigating the effects of the increased errors associated with the subcomponents of the ADC would be the priority for a second pass of this design. A major contributor to DNL, INL and offset error in the ADC is the noise present in the sample and hold circuitry. The hold step is formed by the charge injection from the conducting channels during switch turnoff and clock feedthrough through the sampling switch gate capacitance. One strategy to help reduce this error would be to increase and also externally control the rise and fall times of the sampling switch gate signals. The increased time the channel charges will have to compensate can reduce the amount of error present on the sampling capacitor and lower the charges injected overall [13]. In this endeavor, a separate sample and hold circuit was built, however, including the sampling function in the DAC would be prioritized in future efforts. As transmission gate charges will only truly cancel for one value of V_{in} for the full ICMR, also increasing the sampling the capacitance would be a viable way of reducing the impact of sampling switch imperfections. By implementing this change, the sampling capacitance will be increased by a factor of 15 thus theoretically reducing the sampling error by the same extent. The F_{3dB} will suffer with this modification but should not degrade the sampling performance in this low-speed application. An example of this modification for a standard binary weighted array is shown in Figure 5.1[30]. After the reset phase, the analog input is stored on the bottom plates of the DAC capacitor array. During the conversion period, the SAR algorithm cycles through the bits in the same manner as previously discussed in Chapter 3. The DAC output voltage, now a function of the sampled input voltage, converges to the positive input terminal potential (VSS).
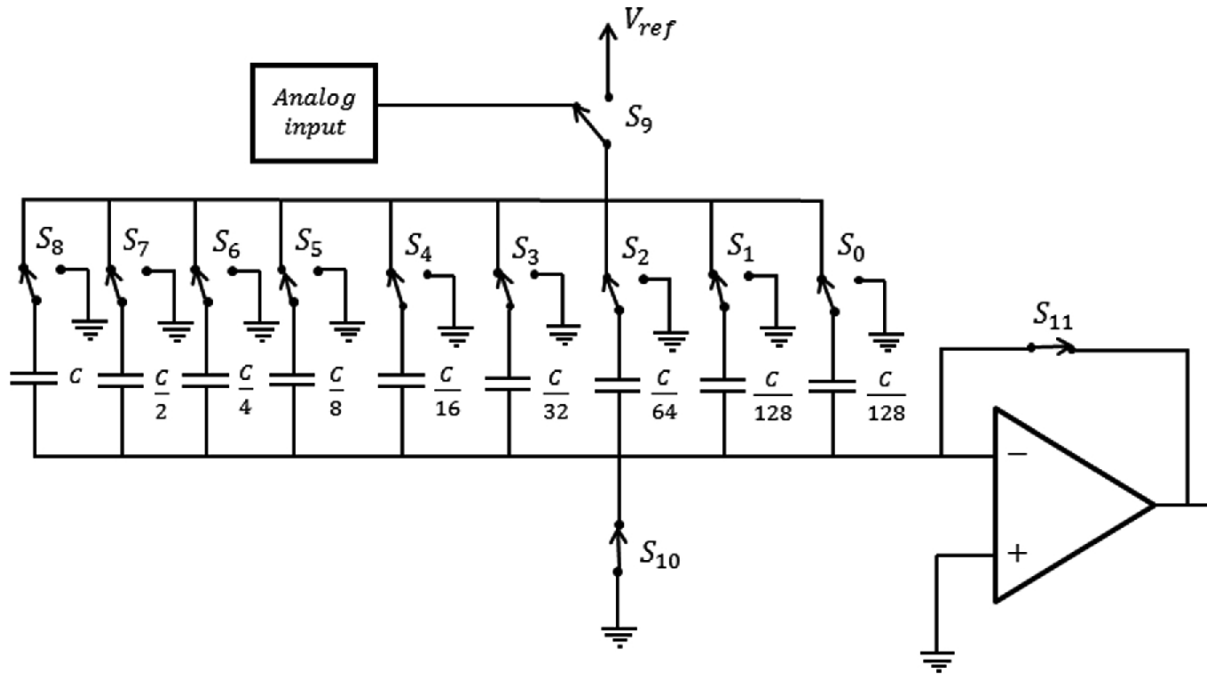
Figure 5.1. DAC capacitor array with sampling [30]

To implement this design, it is very important to be able to completely reset the DAC structure to get rid of previous cycle stray charges. Implementing the switch S_{10} will need some considerations due to the negative voltages held on the top plates of the capacitor array. During the conversion period, leakage current through the switch will cause nonlinearity in the transfer characteristic due to an increased V_{gs} in some operating conditions. This error will gradually increase for slower sampling rates. To mitigate this phenomenon, a switching architecture shown in Figure 5.2 can be utilized [31]. While "precharge" is logic 1, "control" is logic 0 and allows V_{TP} to be stored on the top plate of the capacitor (C). VDD is applied to the bottom plate of the capacitor. Next, "precharge" is switched to logic 0 and "control" goes to logic 1. This causes the voltage at the top plate of the capacitor array to be approximately negative V_{DD} which allows the M3 transistor to be connected to ground when the input voltage is sampled. During the conversion cycle, "control" and precharge" are at logic 0 to prevent charge loss from the capacitor array [32].
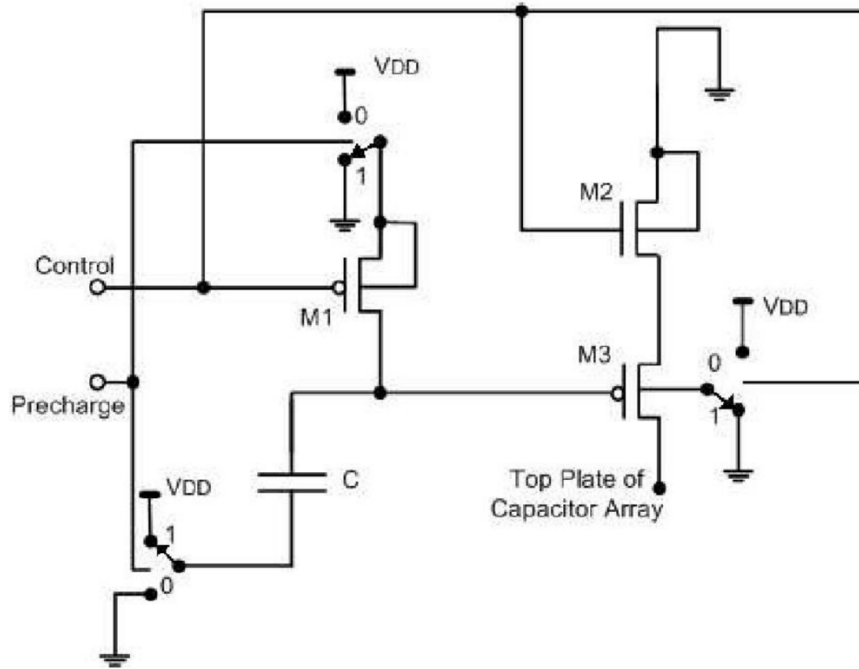
Figure 5.2. Reset switch design [31]

The comparator used in this effort is a latched based type, assisted by a preamplifier to minimize the impact of a potentially large latch offset voltage by providing enough differential gain to overcome the offset. One of the main issues still affecting the comparator performance is the input offset voltage of the preamplifier stage that can cause the output logic to reach the incorrect result. One of the more viable options for removing the effects of offset voltage is by switching to an op-amp based approach that nulls the offset voltage by way of an auxiliary input port. The auxiliary input port is used in many commercial devices today to accomplish this task. The method for trimming the offset is illustrated in Figure 5.3[1]. M1 and M2 are added to the structure to balance the differential currents supplied to the differential amplifier inputs. In Phase 1, when S1 is open and switches S2 and S3 are closed, the offset is calibrated by V_{out} and stored on C. The amplifier inputs are tied to the same potential and therefore the output (V_{out}) reflects the gate voltage necessary for M2 to balance the differential currents using negative feedback. During

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phase 2, switches S2 and S3 are open and S1 is closed. V_{out} in phase 2 reflects the comparison of the two input ports with a matched current flowing in the current mirror load; With this condition, the offset is eliminated. The offset will need to be measured once per conversion cycle and stored on an off-chip capacitance large enough to null the effects of leakage current and switching imperfections caused by S3.

(a)   (b)
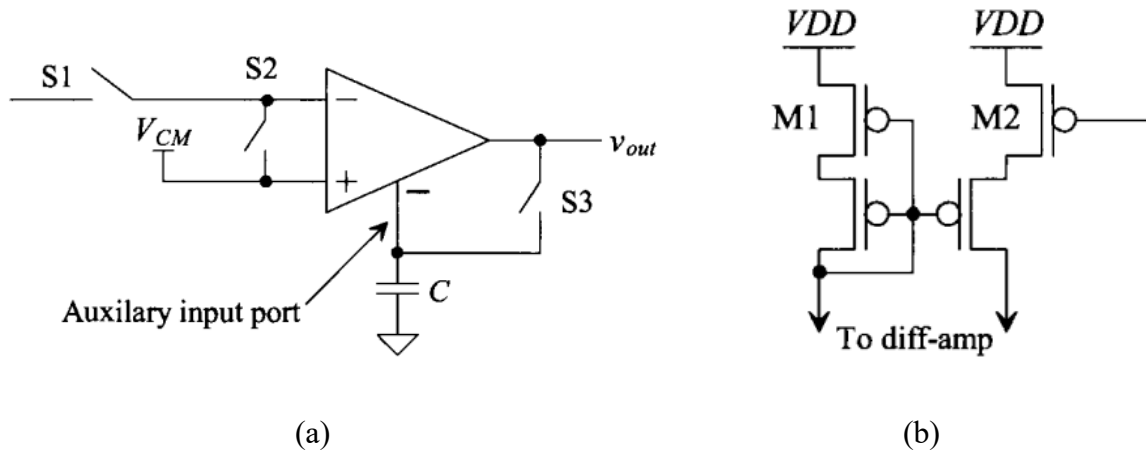
Figure 5.3. Auxiliary port [1] a) Op-amp configuration, b) Diff-amp modification

INL error in the DAC is mainly attributed to the operational amplifier performance near the rails. Ideally, the amplifier buffers the input signal linearly over the full range of input voltage within ½ LSB however, saturation, especially on the positive rail causes the error voltage to increase substantially. As the operation amplifiers were added mainly for driving large off-chip capacitance for testing, removing the buffers would lower the drive capability of the circuit but will not impact the performance of the DAC structure during operation. As a contingency, testing of individual circuits on the probe station would suffice using very low capacitance pico-probes. These probes require very little drive strength and should not dramatically impact the performance of the design for testing purposes. Yet, careful considerations should be taken in regard to switching imperfections to prevent noise from impacting the signal data path.

Chapter 6: CONCLUSION

This thesis covered the design, simulation, and measurement results of a 1.8V 8-bit SAR ADC fabricated in TSMC's 65 nm RF GP process. The SAR design included a separate sample and hold circuit, a split-charge scaled array DAC, latched based comparator with preamplifier, and SAR implemented using set-reset type D-flip-flops. The simulated results report an offset error and gain error of -2.2 LSB and +10.2 LSB respectively. The DNL was found to have a range of -0.4 LSB to +0.5 LSB and an INL with a range of -1.1 LSB and +1.8 LSB. After fabrication, a testbench was created to test the packaged die on a printed circuit board. An Altera Cyclone II FPGA and function generator were utilized to provide the necessary signals for the extraction of the offset and gain error as well as the linearity plots for the fabricated circuit. The offset and gain error were found to be +7 LSB and 31.1 LSB, respectively. Measured results for the full ADC transfer characteristic also show a DNL of -0.9 LSB to +0.8 LSB and an INL of approximately -4.6 LSB to +12 LSB. The INL is much improved in regard to the application of the temperature sensor; The INL for this region of interest is from -3.5 LSB to +2.8 LSB.

Charge injection and clock feedthough in the sampling circuit along with dynamic offset in the operational amplifier and comparator circuits contributed to high nonlinearity figures. Several items of improvement were presented to lower the noise and reduce the nonlinearity present in the transfer characteristic. Future improvements include calibration of the dynamic offset of the comparator along with a new DAC architecture that requires no separate sample and hold. With the new DAC architecture, it is expected that the charge injection and feedthrough errors will be significantly reduced, improving linearity figures for this design.

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