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Design and Evaluation of High Power, High Efficiency and High Power Density Motor Drives for More Electric Aircrafts

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Design and Evaluation of High Power, High Efficiency and High Power Density Motor Drives for More Electric Aircrafts

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by

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Abstract

More-electric aircraft (MEA) is an attractive concept as it can reduce carbon dioxide emission, relieve fossil-fuel consumption, improve the overall efficiency of aircraft, and reduce the operational costs. However, it poses substantial challenges in designing a high-performance motor drive system for such applications. In the report of Aircraft Technology Roadmap to 2050, the propulsion converter is required to be ultra-high efficiency, high power density, and high reliability. Though the wide band-gap devices, such as the Silicon-carbide based Metal Oxide Silicon Field Effect (SiC-MOSFET), shows better switching performance and improved high-temperature performance compared to the silicon counterparts, applying it to the MEA-related application is still challenging. The high switching speed of SiC-MOSFET reduces switching loss and enables the design of high-density converters. However, it poses intense challenges in limiting the stray inductance in the power stage. The fast switching behavior of SiC-MOSFET also challenges the design scalability by multi-chip parallel, which is essential in high-power-rating converters. Moreover, the partial discharge can happen at the lower voltage when the converter is operated at high altitude, low air-pressure conditions, which threatens the converter lifetime by the accelerated aging of the insulation system. This dissertation addresses these issues at the paper-design level, power-module level, and converter level, respectively. At the paper-design level, the proposed model-based design and optimization enables shoulder-by-shoulder performance comparison between different candidate topology and then generates optimal semiconductor design space for the selected topology. At the power-module level, this dissertation focuses on the development of an ultra-low inductance module by using a novel packaging structure that integrates the printed circuit board (PCB) with direct-bounding copper (DBC). The detailed power-loop optimization, thermal analysis, and fabrication guidance are discussed to demonstrate its performance and man-

ufacturability. At the converter level, this dissertation provides a comprehensive design strategy to improve the performance of the laminated busbar. In the design of the busbar conduction layer, this work analyzed the impacts of each stray inductance item and then proposed a novel double-side decoupled conduction-layer structure with minimized stray inductance and improved dynamic current sharing. In the design of the insulation system of the busbar, this dissertation investigates the design strategy to ensure the busbar is free of partial discharge without sacrificing the parasitic control. Through the dissertation, a single-phase 150 kVA converter, a three-phase 450 kVA converter, and a 1.2 kV, 300 A power module are designed, fabricated, and tested to demonstrate the proposed design strategies.

Acknowledgment

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I would like to thank the chair of my committee member, Dr. Roy McCann. He supported and helped me solve many administrative tasks and issues during Dr. Luo's transition to Stony Brook University. I would like to thank my committee members, Dr. Juan Carlos Balda, Dr. Zhong Chen, and Dr. David Huitink, for their time, support, and suggestions to improve my research works.

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Dedication

Dedicated to my dearest fiancée, Zhongjing Wang, and my beloved parents, Yingping Yuan and Ruyi Li.

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1. Z. Yuan et al., ”Design and Evaluation of A 150 kVA SiC MOSFET Based Three Level TNPC Phase-leg PEBB for Aircraft Motor Driving Application,” 2019 IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA, 2019, pp. 6569-6574. doi: 10.1109/ECCE.2019.8913071.
   Chapter 2 and is made up of this paper

2. Z. Yuan et al., ”Design and Evaluation of Laminated Busbar for Three-Level T-Type NPC Power Electronics Building Block With Enhanced Dynamic Current Sharing,” in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 395-406, March 2020, doi: 10.1109/JESTPE.2019.2947488.
   Chapter 3 is made up of this paper

3. Yuan, Zhao, et al. ”Insulation Design and Optimization of Laminated Busbar for More Electric Aircraft Motor Driver under High Altitude and Depressurized Environments.” AIAA Propulsion and Energy 2020 Forum. 2020.
   Chapter 4 is made up of this paper

4. Yuan, Zhao, et al. ”A 1.2 kV 400A SiC-MOSFET Based 3L-TNPC Power Module With Improved Hybrid Packaging Method for High-Density Applications,” 2021 Applied Power Electronics Conference, Phoenix, AZ, USA, 2021.
   Chapter 5 is made up of this paper

1 Introduction

1.1 Research Background

More-electric aircraft concepts can improve the efficiency of airplanes, reduce their carbon emissions and operating costs. While the high-performance power electronics converter is regarded as one of the critical enabling technologies for such concepts. The converters are designed to replace the conventional components powered by pneumatic or hydraulic power sources in the airplane. A recent announced Boeing 787 Dreamliner utilized an electrified no-bleed system for powering the control system of cabin environments, starting the engine and hydraulic pumps, and enabling deicing protection [1]. The updates result in the overall efficiency of Boeing 787 Dreamliner improved by about 3% [2]. Airbus A380 also significantly improved the usage of electric power, according to [3].

The development of a high-performance power electronics converter emphasizing high gravimetric power density, high efficiency, high reliability, and high-power rating is becoming essential. Under such an environment, the National Aeronautics and Space Administration (NASA) starts the investment in research of motor drive for electrified aircraft, with the goal of enabling the full-scaled electrified propulsion system on narrow-body aircraft by 2035 [4].

Motivated by such trends, the University of Arkansas has designed the first version of a more-electric motor drive, as reported in [5,6]. It utilizes the hybrid switch concept, which takes both advantages of low switching loss of silicon carbide (SiC) Metal Oxide Silicon Field Effect Transistor (MOSFET) and low conduction loss of silicon (Si) Insulated-gate Bipolar Transistor (IGBT). It is reported to achieve the 100 kVA power rating, an efficiency of over 99.0%, and a

power density of 27.7 kW/kg.

This dissertation is to provide the design of the second-generation motor drive, which is a higher power rating, higher efficiency, and higher power density. It is designed based on three-level t-type neutral-point clamped (3L-TNPC) topology. Design strategies such as model-based design for topology and power-switch selection, power loop optimization, insulation system optimization, signal sensing stage design are explained in detail in this dissertation.

1.2 Review of Motor Drive Prototypes for MEA Applications

Various prototypes for the more-electric motor drive are present during the past years. In 2018, Dr. Di Zhang, Dr. Jiangbiao He, and Dr. Di Pan from General Electric Global Research Center designed a one mega-watt motor drive for more-electric aircraft propulsion purposes [7,8]. The DC-link voltage is pushed to 2400 V to reduce the root-mean-square (RMS) current and reduce the weight of the cable. The three-level active neutral-point clamped converter is used as the topology to reduce the voltage stress of power semiconductors. The converter also utilizes the hybrid combination of Si IGBT and SiC MOSFET, ensuring good efficiency and reduced costs. The prototype has reached an efficiency of 99.0% and a power density of 12 kVA/kg.

The version II motor drive designed by Dr. Di Zhang, Dr. Jiangbiao He and Dr. Di Pan from General Electric Global Research Center was announced in 2019 [9,10]. Compared to the first version, version II further improves the performance of the converter by using better power semiconductors. Moreover, the layout of the converter is optimized to reduce the dimension and total weight of the converter. The passives are optimized as well, such as the dimensions and weights of output dv/dt filter as well as the EMI filters. Consequently, the efficiency is improved to 99.1%, and the power density is increased by1 kVA/kg.

Additionally, the University of Illinois at Urbana-Champaign Urban and the University of California Berkeley announced a gallium-nitride (GaN) high-electron-mobility transistor (HEMT) based nine-level flying capacitor converter for electric applications [11]. By utilizing the superior switching performance of GaN HEMT and increased output voltage levels, the better output total harmonic distortion (THD) can be achieved. It is claimed that a 200 kVA inverter can be built based on interleaving multiple of 6 kVA units [1].

Recently, the motor drive converter design under cryogenic condition is getting attention because the design further enables power rating and remarkably eliminates the weight of the cable. Accordingly, Dr. Ren Ren, Dr. Handong Gui, and Dr. Fred Wang from the Center for Ultra-wide-area Resilient Electric Energy Transmission Networks delivered a 1 MW converter design that operated at the cryogenic condition, as [12, 13]. It also utilizes a three-level active neutral-point-clamped topology, achieving an efficiency of 99.0%

1.3 Challenge and Research Objective

Though many works are done on design, prototyping, and evaluating the motor drive for more-electric aircraft, the challenges are still waiting to be solved.

1. Three-level converters have been demonstrated with higher efficiency and power density in the applications of more-electric aircraft. Nevertheless, the circuits suffer from high values of stray inductance in each current commutation loop, which overstresses the power switch and insulation system due to high switching-transient voltage.

2. Parallel power switches are necessary to achieve higher power ratings with reduced semiconductor loss. However, unequaled dynamic current sharing between parallel devices may result in diversified switching loss amount them, which increases the peak junction temperature of

the power switches.

3. During the operation of aircraft, the converter is working under low air-pressure conditions because of high altitude. Based on Paschen's law, the partial discharge could happen inside the converter, which significantly accelerates the aging of the insulation system, potentially causing insulation breakdown and reducing system reliability.

4. The overall performance of converters, such as efficiency and power density, is required to be further improved to meet NASA's 2025 roadmap. Breakthrough technologies should be discovered, such as novel packaging technologies and thermal management technologies.

This paper focuses on the hardware development of a 450 kVA motor drive. The dissertation comprehensively explained the design method and procedures. The objective of the design is to achieve even higher system efficiency and power density through an optimized power stage and an improved thermal management system. The design of the laminated busbar with enabling stray inductance minimization and partial-discharge free insulation are highlighted and will be explained in detail. A novel packaging method for three-level t-type neutral-point clamped converters will be introduced to improve system performance further.

1.4 Dissertation Outlines

In chapter 2, the converter design procedures are introduced in detail. The chapter starts with introducing the method of paper design by using the model-based optimization method. Furthermore, the procedures of practically building the converter from the paper design are present as well, such as the selection of optimal power switches and power modules, power stage design and optimization, and the design of signal sensing, conditioning circuits. In the end, the overall structure of 450 kVA motor drive is provided in chapter 2.

The design guidance of the conduction layer in the laminated busbar for a three-level t-type neutral-point-clamped converter is present in chapter 3. The step-by-step design guidance is proposed and explained in this chapter, with the targets of reducing busbar stray inductance, improving dynamic current sharing between parallel switches, and limiting the temperature rising on the busbar. Detailed experiments and simulations are carried out in this chapter to demonstrate the proposed design guidelines and evaluate the overall performance of the designed laminated busbar.

Chapter 4 provides the insulation design method for the laminated busbar in more aircraft applications. As mentioned previously, the partial discharge can happen at lower voltage during the high-altitude operation where air pressure is low. This phenomenon endangers converter lifetime and reliability. As the trend of higher voltage application, the partial discharge is becoming one of the primary challenges in aircraft propulsion converters. This chapter provides a comprehensive insulation design method to make sure the busbar is partial discharge free. This chapter also reveals the trade-off between busbar insulation margin and busbar stray inductance. Through quantitative modeling of the trade-off, the optimal insulation thickness can be chosen in this chapter to balance the insulation margin and busbar stray inductance.

Chapter 5 presents another aspect to improve motor drive performance: improve the performance of the power module. It is seen that power-module level redesign, modification, and improvements can significantly improve the overall performance of the motor drive. Because of additional design flexibility, the lower stray inductance can be achieved through the module layout. A novel power module structure is used in the packaging, which combines a printed circuit board (PCB) and a direct bounding copper (DBC). The new structure can help the converter reaching stray inductance as low as 2.47 nH. At the same time, the thermal performance can be improved as

well by enabling the direct solderability of coldplate. Such a method can eliminate the thermal interfacing material (TIM), remarkably reducing thermal resistance. A 1200 V, 300A power module for three-level t-type neutral-point-clamped topology is present in this part. The conclusion will be present at the end of the dissertation.

1.5 Bibliography

[1] M. Sinnett, 787 no-bleed systems: Saving fuel and enhancing operating efficiencies, Aero Quart., vol. 4, pp. 6–11, 2007.

[2] A. Nawawi et al., "Design and Demonstration of High Power Density Inverter for Aircraft Applications," in IEEE Transactions on Industry Applications, vol. 53, no. 2, pp. 1168-1176, March-April 2017, doi: 10.1109/TIA.2016.2623282.

[3] P. Wheeler and S. Bozhko, "The More Electric Aircraft: Technology and challenges.," in IEEE Electrification Magazine, vol. 2, no. 4, pp. 6-12, Dec. 2014, doi: 10.1109/MELE.2014.2360720.

[4] Jansen, Ralph, Cheryl Bowman, Amy Jankovsky, Rodger Dyson, and James Felder. "Overview of NASA electrified aircraft propulsion (EAP) research for large subsonic transports." In 53rd AIAA/SAE/ASEE Joint Propulsion Conference, p. 4701. 2017.

[5] A. Deshpande, Y. Chen, B. Narayanasamy, Z. Yuan, C. Chen and F. Luo, "Design of a High-Efficiency, High Specific-Power Three-Level T-Type Power Electronics Building Block for Aircraft Electric-Propulsion Drives," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 407-416, March 2020, doi: 10.1109/JESTPE.2019.2952367.

[6] Deshpande, Amol A., Yingzhuo Chen, Balaji Narayanasamy, Zhao Yuan, and Fang Luo. "Modular Three-level T-type Power Electronics Building Block for Aircraft Electric-Propulsion Drives." In AIAA Propulsion and Energy 2020 Forum, p. 3595. 2020.

[7] Zhang, D., et al. (2018). A Megawatt-Scale Medium-Voltage High Efficiency High Power Density "SiC+Si" Hybrid Three-Level ANPC Inverter for Aircraft Hybrid-Electric Propulsion Systems. 2018 IEEE Energy Conversion Congress and Exposition (ECCE).

[8] Zhang, D., et al. (2019). "A Megawatt-Scale Medium-Voltage High-Efficiency High Power Density "SiC+Si" Hybrid Three-Level ANPC Inverter for Aircraft Hybrid-Electric Propulsion Systems." IEEE Transactions on Industry Applications 55(6): 5971-5980.

[9] Zhang, D., et al. (2019). Development of A High-Power Density Megawatt-Scale Medium-Voltage Power Converter for Aircraft Hybrid-Electric Propulsion Systems. 2019 AIAA/IEEE Electric Aircraft Technologies Symposium (EATS).

[10] Zhang, D., et al. (2019). High Power Density Medium-Voltage Megawatt-Scale Power Converter for Aviation Hybrid-Electric Propulsion Applications. 2019 IEEE Energy Conversion Congress and Exposition (ECCE).

[11] Modeer, Tomas, Nathan Pallo, Thomas Foulkes, Christopher Barth, and Robert Pilawa-Podgurski. "Design of a GaN-based Interleaved 9-level Flying Capacitor Multilevel Inverter for Electric Aircraft Applications." IEEE Transactions on Power Electronics (2020).

[12] R. Chen et al., "A Cryogenically-Cooled MW Inverter for Electric Aircraft Propulsion," 2020 AIAA/IEEE Electric Aircraft Technologies Symposium (EATS), New Orleans, LA, USA, 2020, pp. 1-10.

[13] H. Gui et al., "Modeling of Multi-Loops Related Device Turn-On Overvoltage in 3L-ANPC Converters," 2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL), Toronto, ON, Canada, 2019, pp. 1-6, doi: 10.1109/COMPEL.2019.8769723.

2 Overview of Motor Drive Design for MEA Applications

Some content of this chapter comes from an accepted paper of IEEE ECCE 2019.

List of author's name, Yuan, Z., Deshpande, A., Narayanasamy, B., Peng, H., Emon, A.I., Whitt, R., Nafis, B.M., Luo, F. and Huitink,

2.1 Abstract

This chapter is to explain the procedures of designing motor drives for more-electric aircraft. The chapter stands from the system-level aspects and explicitly explains specifications of power motor and their design trade-offs. The design procedures are introduced to achieve the optimal-performance converter. It will start with the paper design, which compares different topology, switch combinations to choose the optimal design space. Then hardware design is carried out, including module selection and comparison, power stage design, and the design of signal sensing, conditioning, and control circuits. Accordingly, a high-performance three-phase 450-kVA motor drive for more electric aircraft application is designed as an example. It has been thoroughly evaluated through tests.

2.2 Model-based Design and Optimization

2.2.1 Overview of model-based design algorithm

To achieve high power density and high efficiency, the optimal paper design of the converter is necessary. Fig. 2.1 shows the components in the power stage of a motor drive, including power semiconductors, heatsink/coldplate, and the passives such as DC-link capacitors, output filters

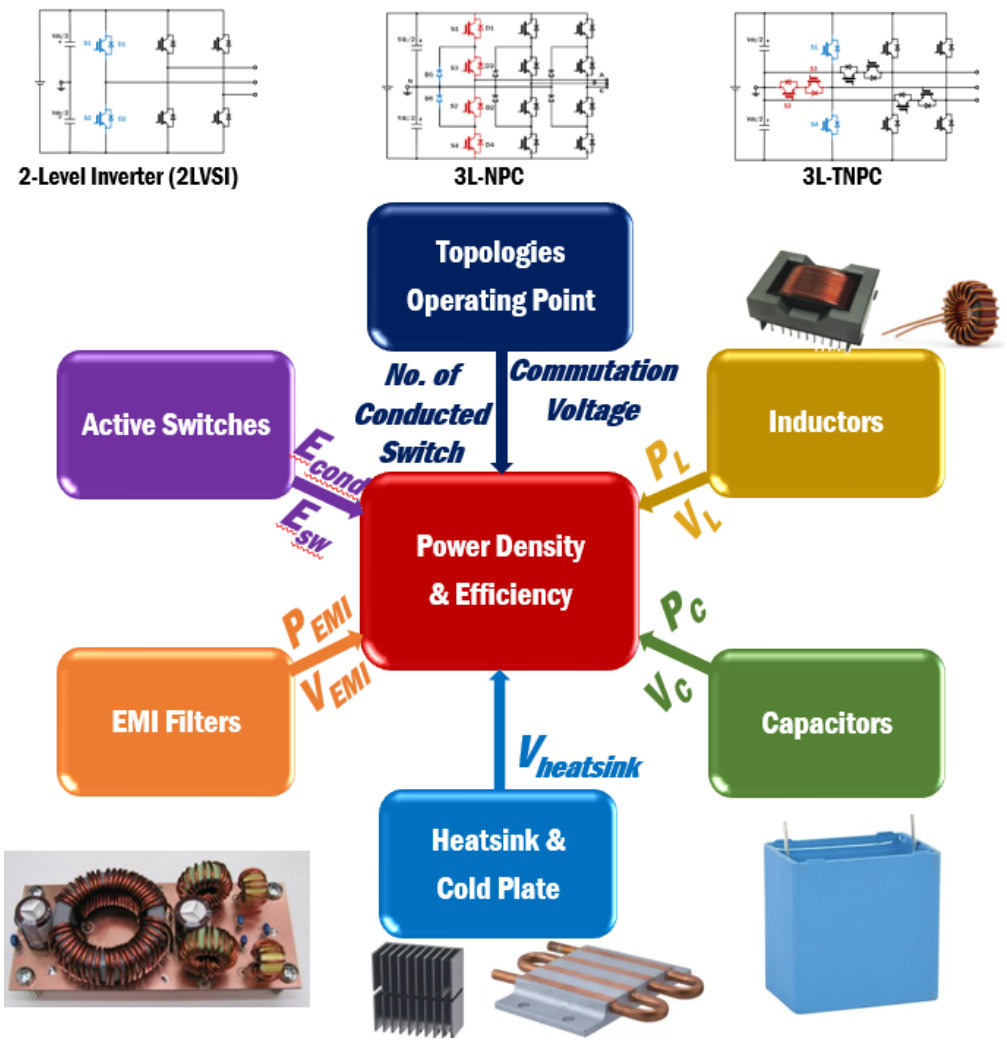


Fig. 2.1: Components in the power stage of motor drive.

and EMI filters. The weight, volume and loss of each the component will contribute to system efficiency and power density.

In such a system, the trade-off can be observed between power density and efficiency. For example, increasing the switching frequency can reduce the size and weight of output filter inductor, but it generates additional switching loss and makes the converter less efficient. Therefore, model-based optimization is required to optimize the converter from a system level.

The overview of model-based comparison can be summarized by Fig.2.2. The target of the

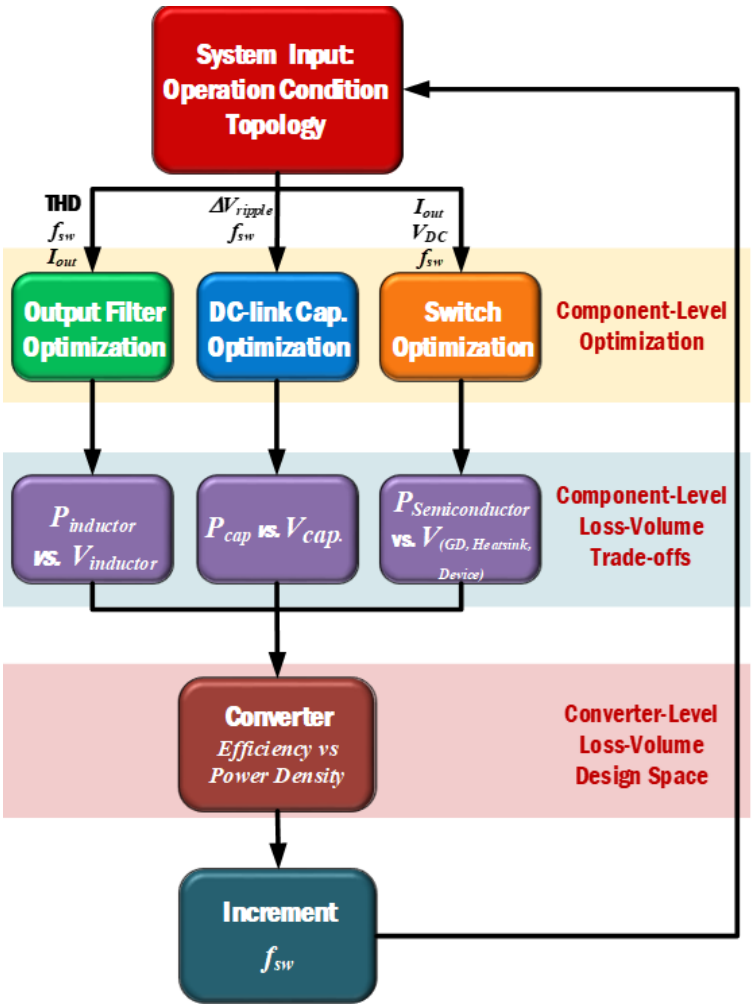


Fig. 2.2: Diagram of the model-based optimization.

model-based design is to obtain the Pareto curve between converter output efficiency and power density at various switching frequency, as shown in Fig.2.3 [1]. Thus, the model-based optimization allows designer to choose the optimal design space with satisfactory performance of both efficiency and power density.

As seen in Fig.2.2, there are five steps to perform model-based optimization. Step I is to define the parameters and requirements of the converter, such as topology, input voltage and output voltage, range of switching frequency, maximum allowed voltage ripple on the DC bus, and maximum allowed total-harmonic distortion (THD) at the output terminal.

Given the design parameters and requirements, step II is to perform the component-level optimization at given switching frequency. For example, perform the inductor optimization at given THD requirements [2], and perform switching-position level optimization to achieve the optimal number of parallel bare dies in each position [3]. The optimized loss-and-volume design space of each component is summarized in step III, and then combined to form the system-level design space in step IV. Step V is to perform the same procedure from step I to step IV by using the increased switching frequency. The output of the optimization is the Pareto curve, as shown in Fig.2.3.

2.2.2 Comparison of popular topology in motor drive systems

Model-based design and optimization is a powerful mathematical tool which can generate the optimized design space and enables design space selection based on converter performance. Nevertheless, understanding the physics behind the Pareto curve is necessary. This part is to discuss the advantages and disadvantages of three commonly used motor drive topologies, including two-level (2L) converters, three-level neutral-point-clamped converters (3L-NPC) and three-level t-type neutral-point-clamped converters (3L-TNPC), as shown in Fig. 2.4

For a fair comparison between topologies, the power semiconductors with the same packaging, and the same current ratings are used in the three topologies, which is summarized in Table 2.1. The efficiency of three topologies are calculated as Fig. 2.5. This loss calculation is based on the model for conduction loss and switching loss based on [4] and assuming converter is working at 1 kV DC-link voltage, and 150 kVA with a power factor of 0.95.

Based on the efficiency curve, it can be observed that,

1. At the lower switching frequency, the two-level converter has higher efficiency.

TABLE 2.1: The power semiconductors for topology comparison

Topology	Switch Model	Packaging Type	Voltage Rating and On-state Reisistance
2L Converter	Wolfspeed HT-3231 Two in parallel	Wolfspeed High-performance 62 mm Module	1.7 kV, 7.5 mΩ /2
3L-ANPC Converter	Wolfspeed HT-3231 Two in parallel	Wolfspeed High-performance 62 mm Module	1.2 kV, 2.5 mΩ
3L-TNPC Converter	Wolfspeed HT-3231 Two in parallel	Wolfspeed High-performance 62 mm Module	1.2 kV 2.5 mΩ and 1.7 kV 7.5 mΩ /2

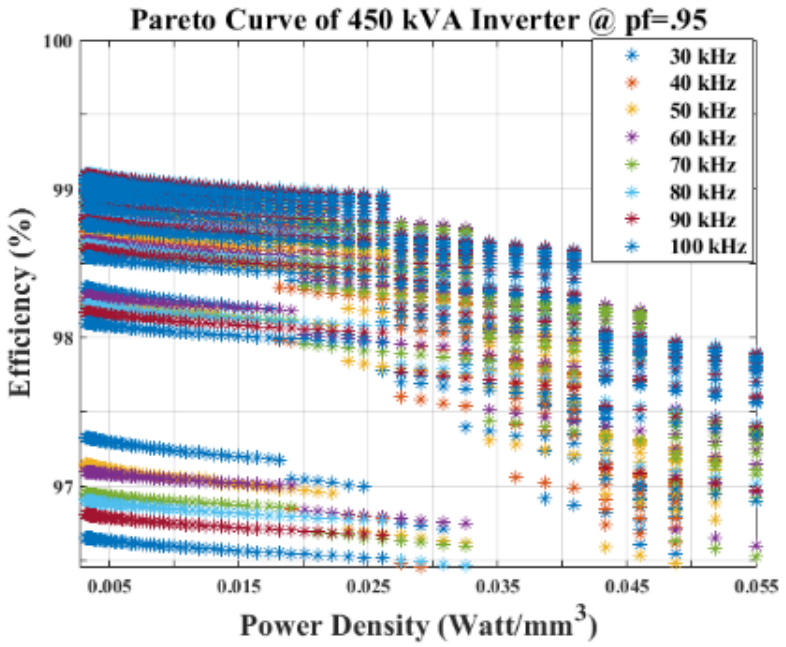


Fig. 2.3: The Pareto curve of designed 450 kVA motor drive [1].

2. As switching frequency is increasing, the efficiency of two-level converter drops faster than the three-level converter, which is the result of higher switching loss.

3. At high switching frequency, both three-level t-type neutral-point-clamped converter and three-level active neutral-point-clamped converter have the similar efficiency. However, the three-level t-type neutral-point-clamped converter has less switching count, which reduces semiconductor costs and improve power density.

Therefore, this dissertation utilizes the three-level t-type neutral-point-clamped converter as the topology for the hardware design.

2.2.3 Number of power module in parallel

Paralleling power modules is necessary for high power inverters in order to reduce the conduction loss and limit the junction temperature of each die. But the number of parallel modules at each switching position should be carefully decided to limit the system costs and complexity.

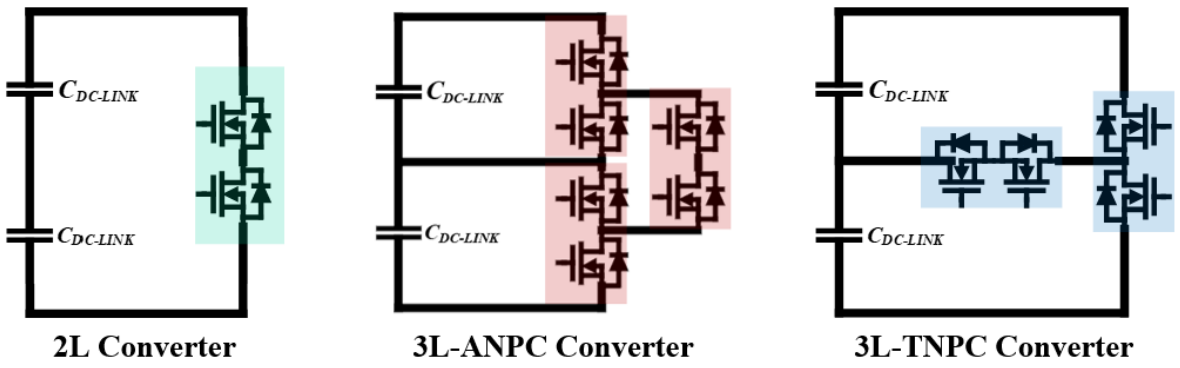


Fig. 2.4: The topology of two-level converter, 3L-ANPC converter and 3L-TNPC converter.

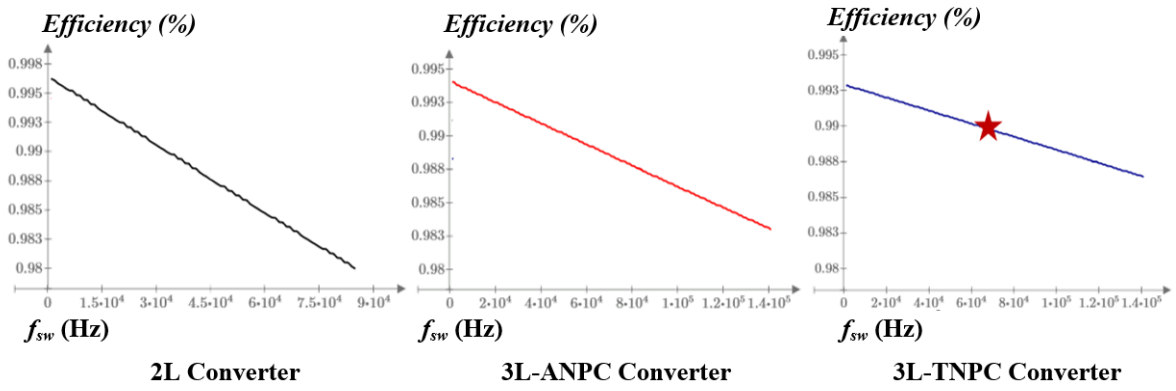


Fig. 2.5: Converter efficiency versus switching frequency for 2L converter, 3L-ANPC converter and 3L-TNPC converter by using the power semiconductors in Table 2.1.

Paralleling more switches at conduction-loss-concentrated switching positions can magnify the benefits.

To give an example, for 3-level t-type neutral-point-clamped converter, the semiconductor loss distribution is largely affected by power factor and modulation index. For motor driving applications with high power factor and high modulation index, the external half-bridge leg shown in Fig. 2.4 generates the majority of conduction loss, compared to the internal clamping leg. Thus more conduction loss can be reduced by paralleling modules at the external bridge.

To quantify the conclusion, the analysis of two scenarios are carried out and compared. Scenario (1) utilizes single Wolfspeed half-bridge (HB) module, HT-3231 as external leg and one

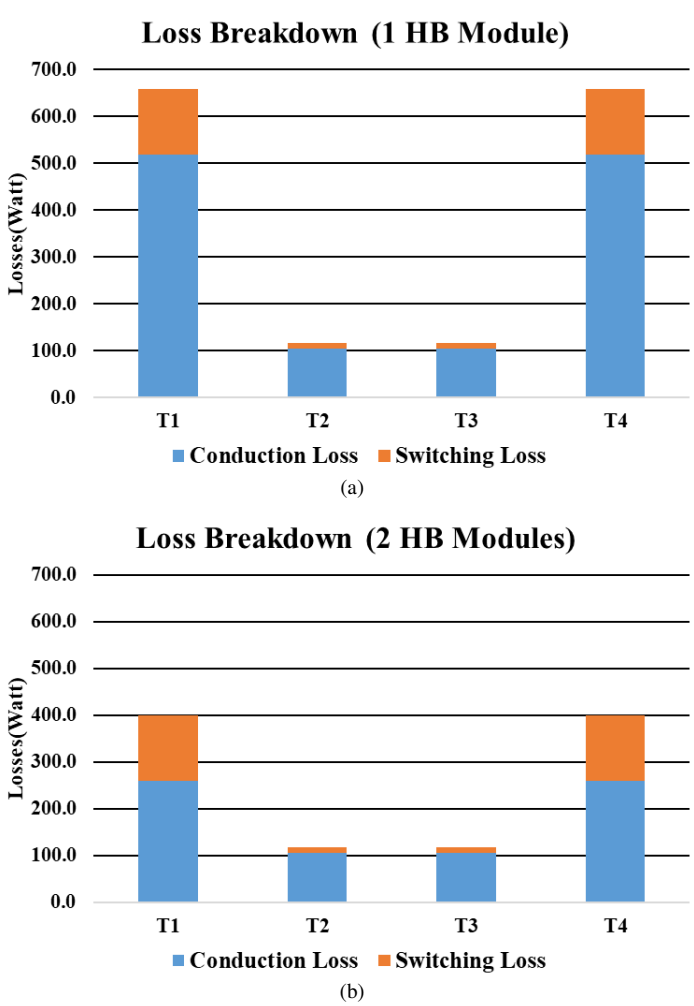


Fig. 2.6: The loss distribution of 3L-TNPC, under scenario (1) and (2), at $P_{out} = 150kW$ and $PF = 0.9$. (a)Loss breakdown based on one half-bridge module as external leg, and one common-source moulde as clamping leg, (b) loss breakdown based on two paralleled half-bridge module as the external leg, and one common-source module as clamping leg.

common-source (CS) module, HT-3220 as the internal clamping leg. While scenario (2) has two HB modules in parallel and keep the CS module the same.

For consistency, SPWM modulation is adopted in this paper for three-level t-type neutral-point-clamped converter. root-mean squared (RMS) current of T_1 and T_2 can be obtained through (2.1) and (2.2). Because of the symmetry of SPWM modulation, conduction loss on T_3, T_4 will be the same as that of T_2 and T_1 respectively. Then total conduction loss is given by (2.3). In the equations, r_{DS_HB} and r_{DS_CS} represent the on-state resistances of SiC MOSFETs in half-bridge

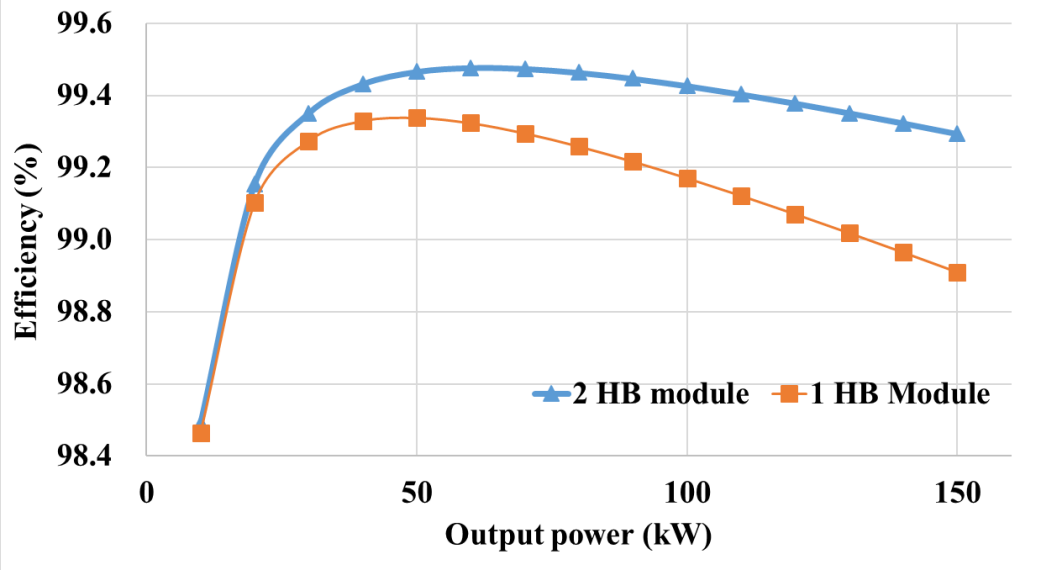


Fig. 2.7: The output efficiency at different load power

module and common-source module respectively.

$$I_{rms\_T1}(I_{pk},\varphi) = \sqrt{\frac{M \cdot I_{pk}^2}{3 \cdot \pi}(1+cos(\varphi)^2)} \tag{2.1}$$

$$I_{rms\_T2}(I_{pk},\varphi) = \sqrt{\frac{I_{pk}^2}{2} - \frac{2 \cdot M \cdot I_{pk}^2}{3 \cdot \pi}(1+cos(\varphi)^2)} \tag{2.2}$$

$$P_{cond\_total}(I_{pk},\varphi) = (I_{rms\_T1}(I_{pk},\varphi)^2 \cdot r_{DS\_HB} + I_{rms\_T2}(I_{pk},\varphi)^2 \cdot r_{DS\_CS}) \cdot 2 \tag{2.3}$$

Switching loss of T_1 and T_2 in one fundamental cycle are given by (2.4) and (2.4). Due to the symmetry, switching loss on T_3, T_4 will be the same as that of T_2, T_1 respectively. Total power of switching loss on semiconductor devices is given by (2.6).

$$E_{SW\_T2}(I_{pk},\varphi,f_{sw}) = \sum_{k=\frac{0 \cdot f_{sw}}{2\pi \cdot f_1}}^{k=\frac{(\varphi) \cdot f_{sw}}{2\pi \cdot f_1}} -(E_{T\_OFF\_CS} + \quad E_{T\_ON\_CS}) \cdot sin(\frac{k \cdot f_1}{f_{sw}} 2\pi - \varphi) \cdot \frac{I_{pk} \cdot \frac{V_{DC}}{2}}{I_{test\_CS} \cdot V_{test\_CS}} \tag{2.4}$$

$$E_{SW\_T1}(I_{pk},\varphi,f_{sw}) = \sum_{k=\frac{\varphi \cdot f_{sw}}{2\pi \cdot f_1}}^{k=\frac{(\pi) \cdot f_{sw}}{2\pi \cdot f_1}} (E_{T\_OFF\_HB} + \quad E_{T\_ON\_HB}) \cdot sin(\frac{k \cdot f_1}{f_{sw}} 2\pi - \varphi) \cdot \frac{I_{pk} \cdot \frac{V_{DC}}{2}}{I_{test\_HB} \cdot V_{test\_HB}} \tag{2.5}$$

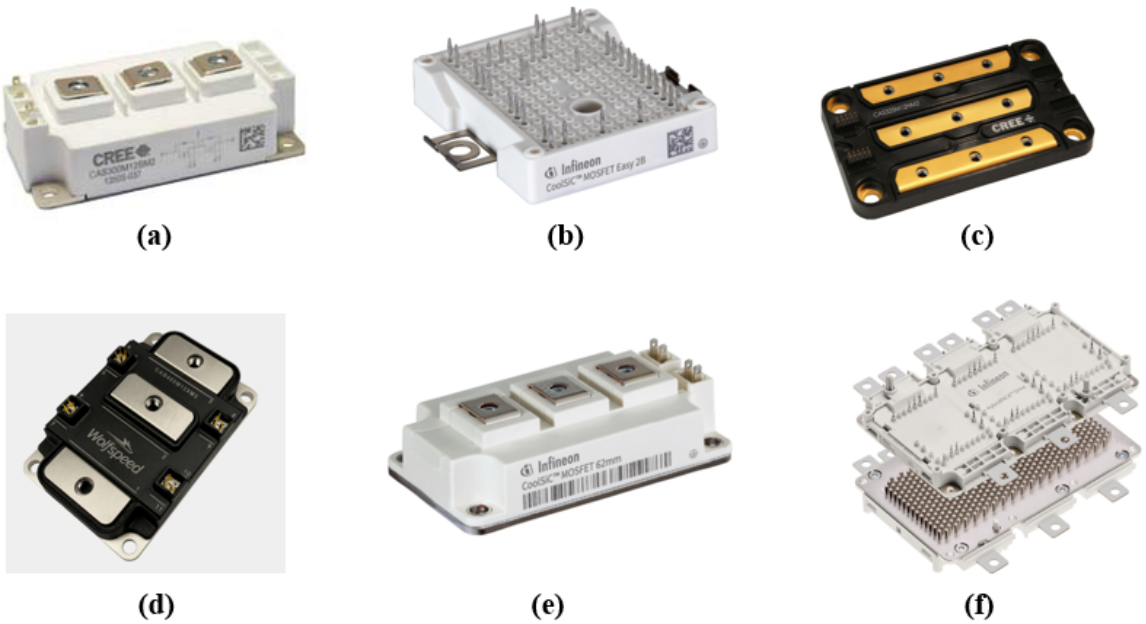


Fig. 2.8: The picture of commercially available power modules. (a) Wolfspeed 62-mm series [6], (b) Infineon Easy 2B series [10], (c) Wolfspeed high-performance 62 mm series [4], (d) Wolfspeed XM3 series [5], (e) Infineon CoolMOS 62 mm series [8], (f) Infineon HybridPack Drive series [9].

$$P_{SW\_Total}(I_{pk},\varphi,f_{sw}) = (E_{SW\_T1}(I_{pk},\varphi,f_{sw}) + E_{SW\_T2}(I_{pk},\varphi,f_{sw})) \cdot 2 \cdot f_1 \tag{2.6}$$

At 150-kW per-phase output power, switching frequency of 30-kHz and a power factor of 0.9 lagging. The loss distribution and output efficiency of both scenario (1) and (2) are performed and compared, as shown in Fig. 2.6, and Fig. 2.7. Because the high power factor and modulation index, the majority loss are concentrated in the external legs in scenario (1), namely, T1 and T4. The design in scenario (1) is practically unfeasible due to around 1-kW heat dissipation load of half-bridge module.

By paralleling one more half-bridge module in scenario (2), the conduction loss can be effectively cut by a half. As a result, more-equalized loss distribution is achieved among switching positions. The peak efficiency and full-load output efficiency can be improved to 99.45% and 99.30% respectively as shown in Fig. 2.7, it is seen that Wolfspeed High-performance 62 mm

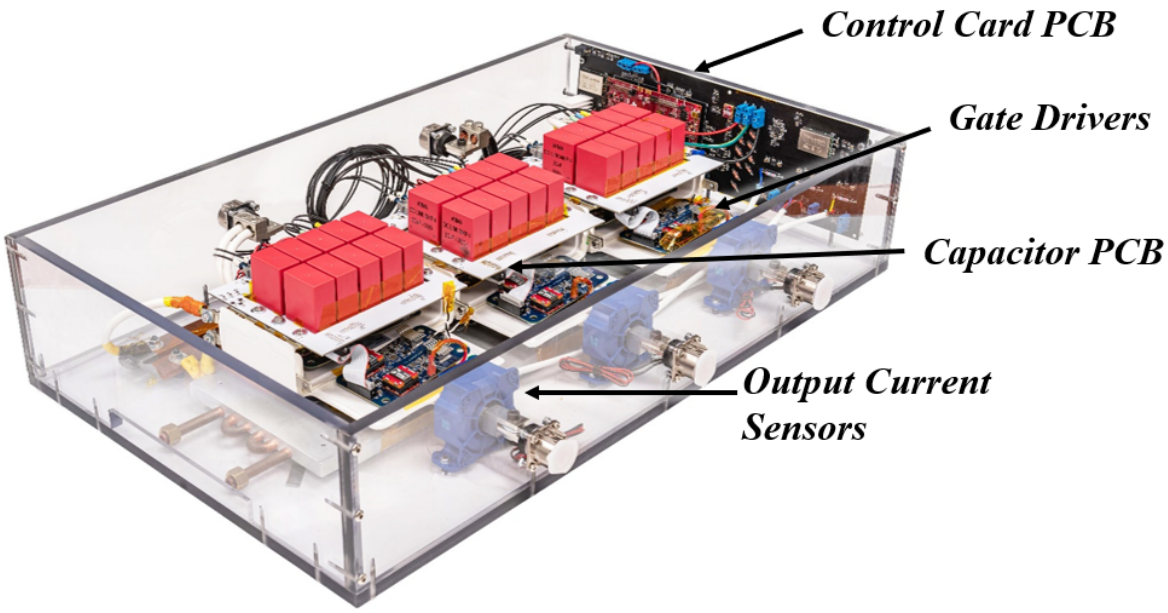


Fig. 2.9: Designed 450 kVA motor drive with auxiliary circuits noted.

series is better performance because of the lower stray inductance, the lower on-state resistance and the lower weight. Therefore, it is selected for the converter hardware design.

2.3 Module Comparison and Selection

Silicon carbide (SiC) based Metal Oxide Silicon Field Effect Transistor (MOSFET) shares advantages such as high switching speed compared to its silicon counterparts. The higher switching speed can significantly reduce the switching loss and enables high power-density converter design based on high switching-frequency operation. However, the advantage of SiC-based MOSFET cannot be fully exploit because of the parasitic in the circuits. For example, the high current slew rate (di/dt) feature makes the SiC-MOSFET more sensitive to the stray inductance in the circuit. According to the [4], the stray inductance in power loop can cause the voltage overshoot and severe ringing issues across the three terminals of SiC MOSFETs at both turn-on switching transient and turn-off switching transient. Therefore, the SiC MOSFET power module requires to have as less

TABLE 2.2: Comparison of commercially available SiC-MOSFET power modules

Manufacture and Model Number	Voltage rating and R_{DSon}	Stray Inductance	Junction-to-case Thermal resistance	Weight
Wolfspeed CAB760M12HM3	1200V 1.33 mΩ	4.9 nH	0.068 $^oC/W$	179 g
Wolfspeed CAB450M12XM3	1200V 2.6 mΩ	6.7 nH	0.11 $^oC/W$	175 g
Wolfspeed AB400M12BM3	1200V 3.25 mΩ	10.2 nH	0.13 $^oC/W$	300 g
Rohm BSM600D12P3G001	1200V 3.0 mΩ	10.0 nH	0.08 $^oC/W$	-
Infineon FF2MR12KM1	1200V 2.13 mΩ	20.0 nH	0.083 $^oC/W$	340 g
Infineon FS03MR12A6MA1B	1200V 2.85 mΩ	$<$10 nH	-	-
Infineon FF6MR12W2M1P_B11	1200V 2.85 mΩ	8.0 nH	0.266 $^oC/W$	39 g

stray inductance as possible.

Besides, the on-state resistance is one of the most important parameters on the datasheet of power modules. It means the resistance between the drain terminal and the source terminal of power modules when the modules is turned on. The on-state resistance can be abbreviated as $R_{DS,ON}$. Because the conductional loss is linearly related to the on-state resistance, this parameter is required to be as low as possible to improve the efficiency of the converter.

Moreover, the junction-to-case thermal resistance (R_{j-c}) of a power module is defined

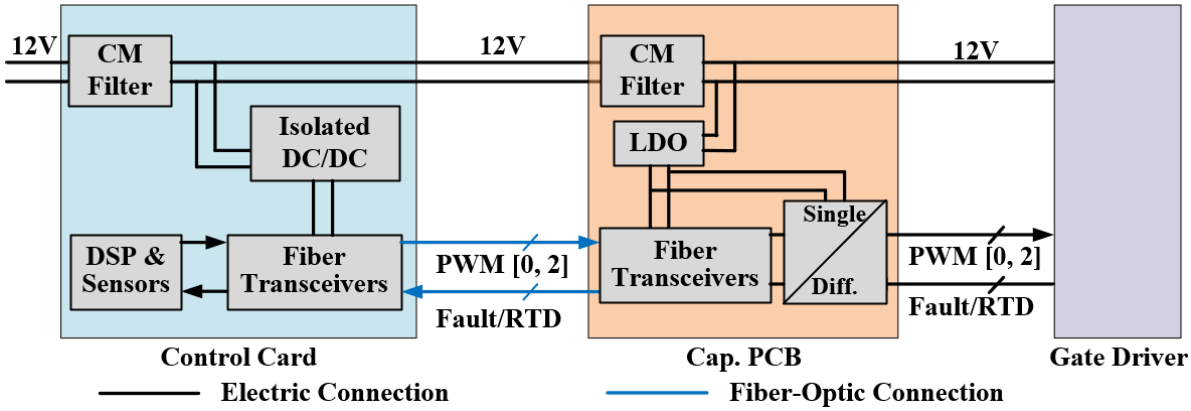


Fig. 2.10: The diagram of auxiliary power supply structure in 450 kVA motor drive.

as the temperature difference between the semiconductor junction and its case when there is 1-watt loss generated by the semiconductor. Thus, the unit of junction-to-case thermal resistance is $^{o}C/W$. It is used to count the thermal conductivity of the module. The junction-to-case thermal resistance is one of the most important parameters of power module as well, because it decides the current rating of the power module. For SiC MOSFET devices, the maximum allowable junction temperature is 175 ^{o}C, thus the current is limited by the loss generated in the module and the case temperature of the power module. Additionally, the on-state resistance of SiC-MOSFET is a positive temperature coefficient, which means the positive feedback loop exists: the higher junction temperature will raise the on-state resistance of SiC-MOSFET, which generates more loss and pushes the junction temperature even higher. This positive feedback loop potentially the challenges the thermal management system of power converter. Thus, selecting a module with a lower junction-to-case thermal resistance is necessary. Last but not the least, the weight of power module contributes to the weight of power converters. Therefore, the power module is preferred the lower weight for high power-density converters.

Given the three important parameters for power module selection, such as module stray

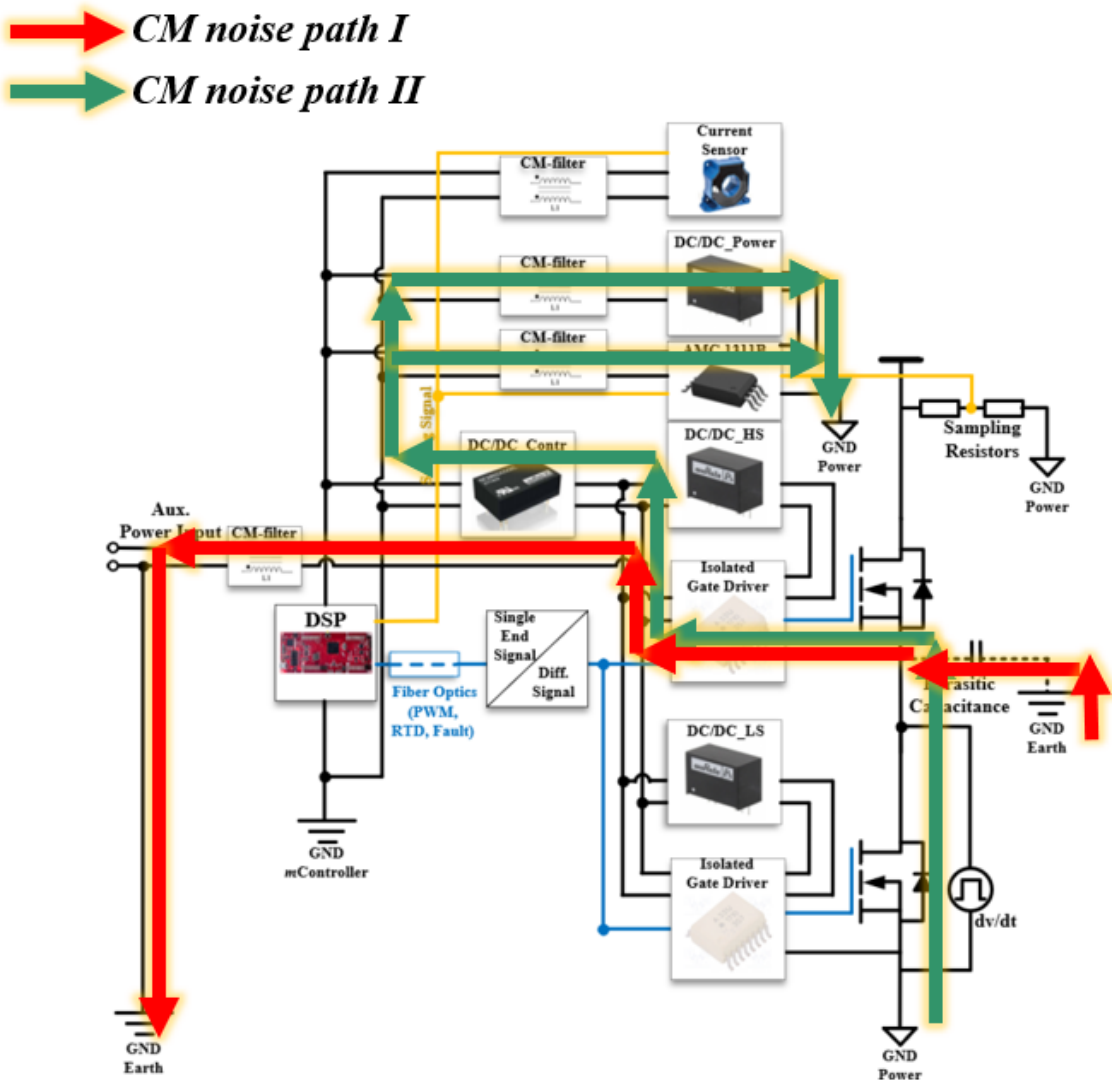


Fig. 2.11: Common-mode noise paths in auxiliary circuits.

inductance, on-state resistance and junction-to-case thermal resistance, the commercially available power modules are searched as compared in Fig. 2.8, with their parameters summarized as table 2.2. Based on the table 2.2 and fig.2.8, the Wolfspeed high-performance 62 mm power modules are used. for hardware design because of less stray inductance and better thermal conductivity.

TABLE 2.3: Major components in 450 kVA converter

Item	Description
Power Module	HB power module: Wolfspeed HT-3231, 1.7 kV, 245A 7.5mΩ, two in parallel per phase; CS power module: Wolfspeed HT-3220, 1.2 kV, 660A 2.5m Ω, one per phase;
DC-link Capacitor	WIMA polypropylene-based film capacitors, 800V 30uF, 10 capacitors per phase, 30 capacitors in total;
Busbar	4-layer customized busbar, copper thickness of 2mm;
Coldplate	AAVID Hi-contact liquid coldplate, 6-pass, aluminum plate, copper tube;
Power Connector	Amphenol heavy-duty 10mm bolt size, power connector; PL00X-301-10D10;
Current Sensor	LEM 510-S current transducer, 500Arms, 200 kHz
Voltage Sensor	Texas Instruments, reinforced isolated amplifiers AMC1311BDVR, 200 kHz, CMTI of 140 kv/μs;
Controller	Texas Instruments, DSP28379D, Dual Core, 150 MHz

2.4 Auxiliary Circuits in 450 kVA Converter

The designed 450 kVA converter is shown in Fig. 2.9, with all the important components listed as table 2.3. The detailed power stage design will be explained in the later chapter. Classified by the functions, converter auxiliary circuits include controller circuits, fiber signal transmitting and receiving circuits, sensor circuits, and signal conditioning circuits.

The power supply of the sensor board is shown as Fig. 2.10. It is seen that the converter

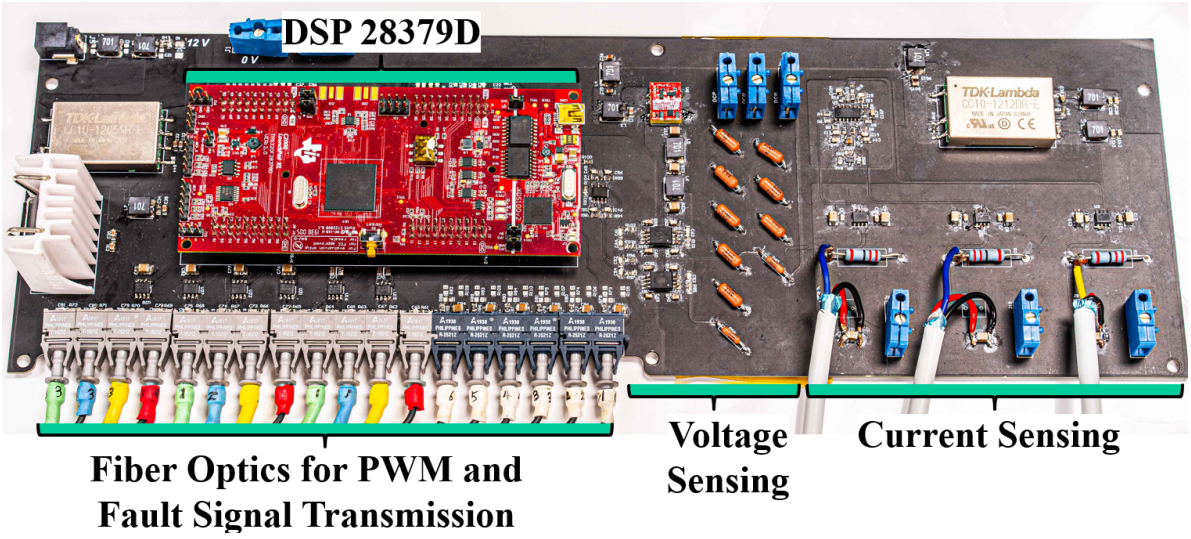


Fig. 2.12: The top view of control card PCB for 450 kVA motor drive.

relies on an external 12 V power supply to power the whole controller circuits. And depending on the function of auxiliary circuits, the voltage level is shifted by isolated DC/DC converters and low-dropout regulators (LDOs). For example, the 12 V can be transferred to the isolated voltage, 20 V and -5 V to power the gate driver and offer the SiC-MOSFET turn-on voltage of 20 V and turn-off voltage of -5V. The original voltage can also be transmitted to 3.3 V by low-dropout regulator for a stable power supply to the digital circuit processor (DSP). Moreover, the 12 V is transferred to +15 V and -15 V to the signal conditioning circuit of current sensor. Additionally, the isolated +5 V is transferred from the original 12V by using isolated DC/DC, for the signal conditioning circuits of voltage sensor.

Given the auxiliary circuits, Fig. 2.11 presents the possible common-node noise path for in auxiliary power supply. In this figure, the source of common-mode noise can be regarded as the voltage slew rate (dv/dt) during switching transition of SiC-MOSFET. Because of the faster switching speed of SiC-MOSFT, the noise source is higher than its Si counterpart. As the noted current path I in fig.2.11, the common-mode noise current can form the loop from gate driver

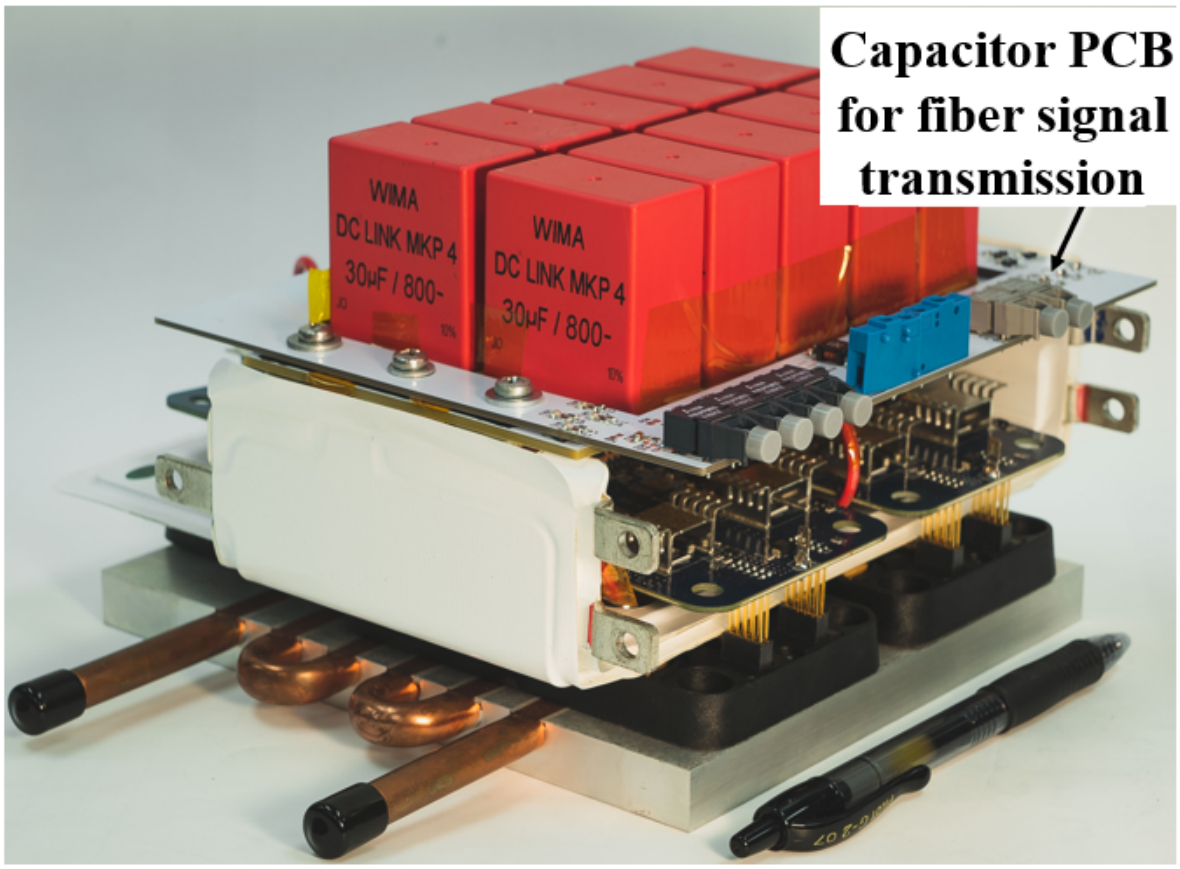


Fig. 2.13: Capacitor PCB for DSP-to-gate-driver signal adapting and transmission.

directly to the input terminals of power supply, and then flow back to the power ground through the parasitic coupling between earth ground and power ground. Additionally, as noted in current path II in fig.2.11, the common-mode noise current can also flow through on the path, including gate driver, and voltage sensor. The noise is unwanted especially for the voltage sensor, as it can distort the sampled voltage signals and make the voltage sensor malfunction.

Three methods are used in the auxiliary to eliminate the unwanted common-mode noise current. First, the fiber circuits are used to perform high fidelity signal transmission between the digital signal processor and the gate driver. As fiber is made by silicon, which shows high impedance to the noise, the digital signal processor can be protected from the noise.

Secondly, the common-mode filter is used in each of the important positions, as shown

TABLE 2.4: Key parameters for candidate voltage sensors

Model Number	Manufacture	Bandwidth	CMTI	Barrier Cap.	Isolation Method
ACNT-H87B	BROADCOM	100 kHz Typical	15kV/us Typical	0.5 pF	Optical Isolation
ACPL-C87B	BROADCOM	100 kHz Typical	15kV/us Typical	0.5 pF	Optical Isolation
MID400	On Semi	-	-	2.0 pF	Optical Isolation
AMC1311	TI	220 kHz Typical	30kV/us Typical	$\sim$1.0 pF	SiO2 - based
AMC1311B	TI	275 kHz Typical	140kV/us Typical	$\sim$1.0 pF	SiO2 - based

in fig. 2.10 and fig. 2.11. The common-mode filter will also increase the impedance on the transmission line of common-mode noise, thus it attenuates the amplitude of the noise.

Thirdly, the voltage sensor is selected to have larger barrier capacitance and high common-mode noise transient immunity. As shown in table 2.4, different types of voltage sensors from different manufactures are compared by bandwidth, common-mode injection ratio, barrier capacitance and isolation technologies. Based on the shoulder-by-shoulder comparison, the sensor manufactured by Texas Instruments, AMC1311Bc shows advantages in both high common-mode transient immunity and low barrier capacitance. Thus it is selected for the voltage sensor in this 450 kVA motor drive.

Eventually, the auxiliary control card is designed as fig. 2.12, which is screw mounted on the converter wall, as shown in fig. 2.9. The auxiliary control card integrates the voltage sensing and current sensing circuits, the digital signal processing circuits, and the fiber optic circuits for

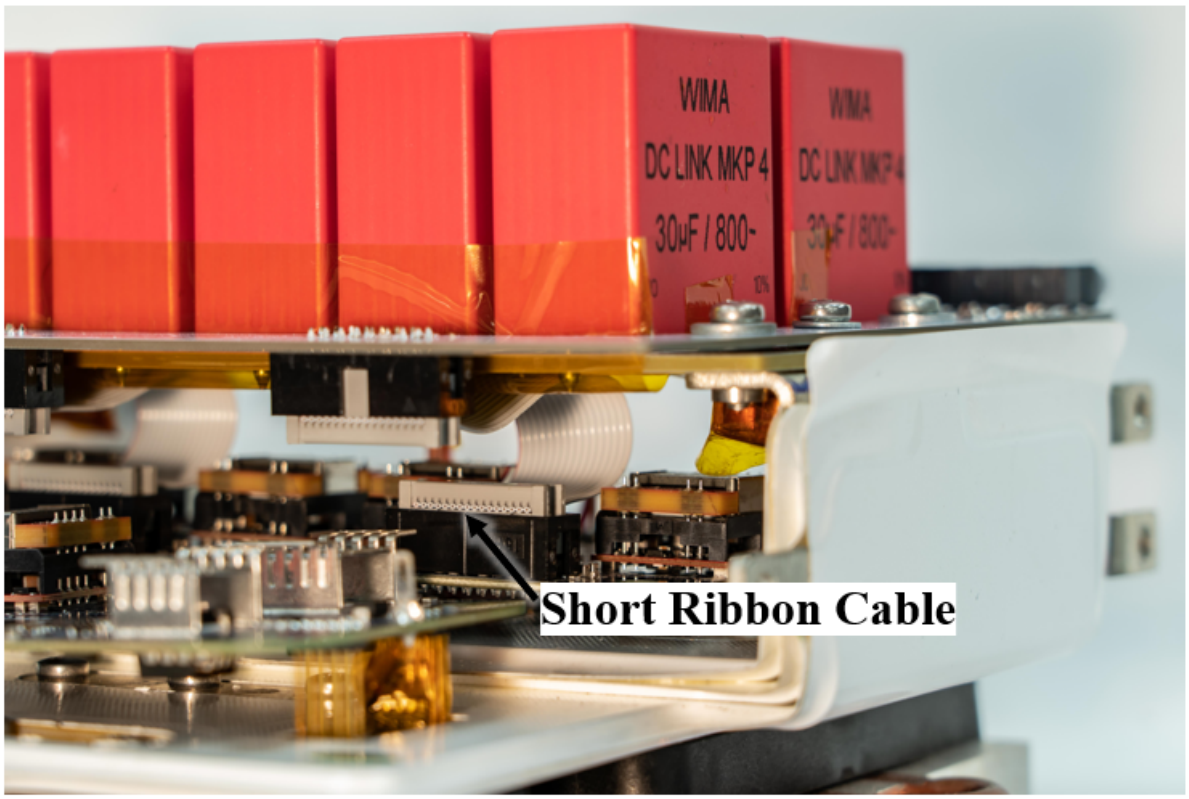


Fig. 2.14: Short ribbon cables for capacitor board to gate driver signal transmission to avoid radiated noises.

PWM and fault signal transmission.

While fiber circuit connects to each single phase at the top capacitor PCB shown in fig. 2.13. The top capacitor PCB transmit the fiber signal to electric signals, and then transfer the signals to gate driver by using short ribbon cables to avoid radiated coupled noise, as shown in 2.14.

2.5 Bibliography

[1] Mustafeez-ul-Hassan, Z. Yuan, H. Peng, A. I. Emon, Y. Chen and F. Luo, "Model Based Optimization of Propulsion Inverter for More-Electric Aircraft Applications Using Double Fourier Integral Analysis," 2020 AIAA/IEEE Electric Aircraft Technologies Symposium (EATS), New Orleans, LA, USA, 2020, pp. 1-7.

[2] Wei, Lixiang, and Richard A. Lukaszewski. "Optimization of the main inductor in a LCL filter for three phase active rectifier." In 2007 IEEE Industry Applications Annual Meeting, pp. 1816-1822. IEEE, 2007

[3] Y. Chen, Z. Yuan and F. Luo, "A Model-Based Multi-Objective Optimization for High Efficiency and High Power Density Motor Drive Inverters for Aircraft Applications," NAECON 2018 - IEEE National Aerospace and Electronics Conference, Dayton, OH, 2018, pp. 36-42, doi: 10.1109/NAECON.2018.8556757.

[4] Z. Yuan et al., "Design and Evaluation of A 150 kVA SiC MOSFET Based Three Level TNPC Phase-leg PEBB for Aircraft Motor Driving Application," 2019 IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA, 2019, pp. 6569-6574, doi: 10.1109/ECCE.2019.8913071.

[5] XM3 Power Module Family, SiC Power Modules, Wolfspeed, 2020. [Online]. Available: https://www.wolfspeed.com/power/products/sic-power-modules/xm3-power-module-family. [Accessed: 2-Nov-2020].

[6] 62mm Silicon Carbide Half-bridge Power Modules, Wolfspeed, 2020. [Online]. Available: https://www.wolfspeed.com/power/products/sic-power-modules/62mm-power-module-family. [Accessed: 2-Nov-2020].

[7] Silicon Carbide Power Modules, ROHM Semiconductors, 2020. [Online]. Available: https://www.rohm.com/products/sic-power-devices/sic-power-module. [Accessed: 2-Nov-2020].

[8] FF2MR12KM1, Infineon Technologies, 2020. [Online]. Available: https://www.infineon.com/cms/en/product/power/mosfet/silicon-carbide/modules/ff2mr12km1/. [Accessed: 2-Nov-2020].

[9] FS03MR12A6MA1B, Infineon Technologies, 2020. [Online]. Available: https://www.infineon.com/cms/en/product/power/mosfet/silicon-carbide/modules/fs03mr12a6ma1b/. [Accessed: 2-Nov-2020].

[10] FF6MR12W2M1P_B11, Infineon Technologies, 2020. [Online]. Available: https://www.infineon.com/cms/en/product/power/mosfet/silicon-carbide/modules/ff6mr12w2m1p$_b$11/.[$Accessed : 2-Nov-2020$].

[11] HM Power Module Family, SiC Power Modules, Wolfspeed, 2020. [Online]. Avail-

able: https://www.wolfspeed.com/power/products/sic-power-modules/hm-power-module-family. [Accessed: 2-Nov-2020].

3 Conduction Layer Design of Busbar with Low Inductance and Improved Current Sharing

This paper has been accepted and submitted as the final paper for IEEE JESTPE 2020.

List of author's name, Yuan, Z., Peng, H., Deshpande, A., Narayanasamy, B., Emon, A.I., Luo, F. and Chen, C.

3.1 Abstract

This paper focuses on providing the design guidance of conduction layer in laminated busbar for a 3-level T-type neutral-point-clamped inverter (3L-TNPC) to achieve low stray inductance and balanced inductance distribution between paralleled power switches. As a result, equalized dynamic current sharing can be accomplished. To discover the design strategy, the paper first derives mutual-inductance-decoupled equivalent circuit for 3L-TNPC. Then the effects of each inductance item on switching performance can be unveiled and the parametric targets are then summarized. Accordingly, the busbar design considerations are discussed. A step-by-step busbar design procedure to achieve the aforementioned design targets is provided in the next. The design procedure starts from two-dimensional (2-D) optimization to achieve the optimal component and terminal allocation, then it increases the optimization degree to three dimensions (3-D). Using this design procedure, we proposed a novel double-side-end busbar structure to achieve the busbar stray inductance of 12.7 nH, and inductance differences between the paralleled switches to be less than 2 nH. Extensive experiments are carried out in the end to evaluate the design procedure and demonstrate the performance of the busbar

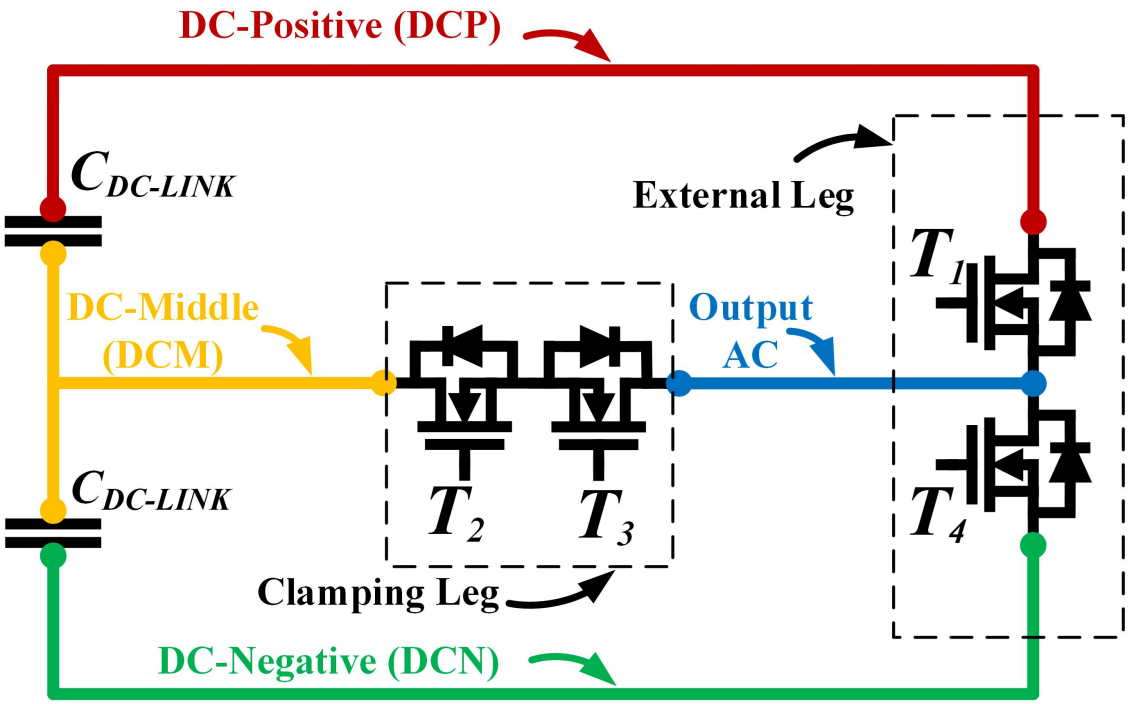


Fig. 3.1: The topology of 3L-TNPC

3.2 Introduction

More electric aircraft concept is recently attracting more attention because it reduces the overall costs and carbon emissions [1] - [4]. This concept requires the propulsion inverter to have higher power rating, higher efficiency and higher gravimetric power density than state-of-the-art. With this as motivation, the Department of Energy (DOE) and National Aeronautics and Space Administration (NASA) have proposed the roadmaps for future and the research projects are carried out as summarized in Table 3.1.

Model-based optimization (MBO) is widely used to design and optimize the inverter prior to physical implementation [8] - [10]. Based on the conclusion of MBO [11] - [13], the 3-level T-type neutral-point-clamped (3L-TNPC) inverter shows efficiency advantages over other topology, at around 1-kV-level of DC-link voltage and 100-kVA power or higher. Thus the paper focuses

TABLE 3.1: Roadmap and research projects for the future propulsion inverters

Parameters	DOE 2025 Targets[5]	NASA 30-year Roadmap[6]	General Electric[7]	University of Arkansas
Power Rating	100 kW	1 MW	1 MW	450 kW
Efficiency	-	99.50%	99.00%	99.45%
Power Density	33 kW/L	25 kW/kg	12 kVA/kg	34 kVA/kg

on the design and evaluation of the busbar for the 3L-TNPC. As a single-phase 3L-TNPC shown in Fig. 3.1, the combination of half-bridge (HB) module and common-source (CS) module are sufficient to build 3L-TNPC.

To achieve high efficiency, the previous works [10] - [15] have demonstrated the effectiveness of paralleling semiconductors to reduce the conduction loss. Since the high-speed motors have relatively the lower inductance and higher power factors [16] - [18], the external leg of 3L-TNPC has the predominant conduction losses compared to the clamping leg [19] - [21]. Therefore, more paralleled SiC-MOSFETs at T_1 and T_4 in Fig. 3.1 can effectively reduce the total semiconductor loss.

Nevertheless, some of the paralleled switches may carry different amount of current than the others, which results in the localized overheating problem [22] - [24]. In general, the static current sharing can be automatically compensated by a positive temperature coefficient (PTC) of on-state resistance distributed in the drifting region of SiC MOSFET [25], [26]. But the dynamic current sharing could be unbalanced and can result 267% of switching loss differences distributed between the paralleled SiC MOSFETs[27]. To solve this problem, [26] - [29] investigates the influence of device-level parameters on dynamic current sharing, for instance, the effects of threshold voltage, junction capacitance and trans-conductance. It is found that the negative temperature coef-

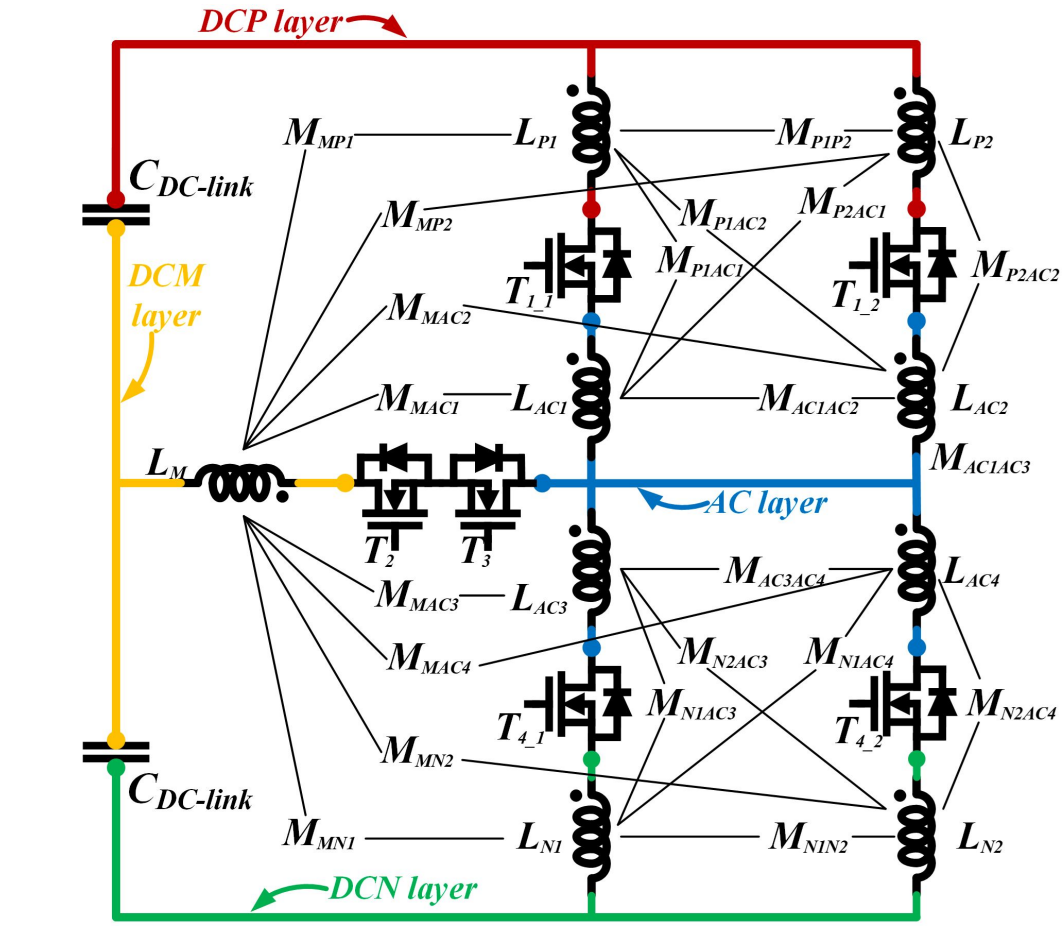


Fig. 3.2: The equivalent circuit of the busbar for 3L-TNPC

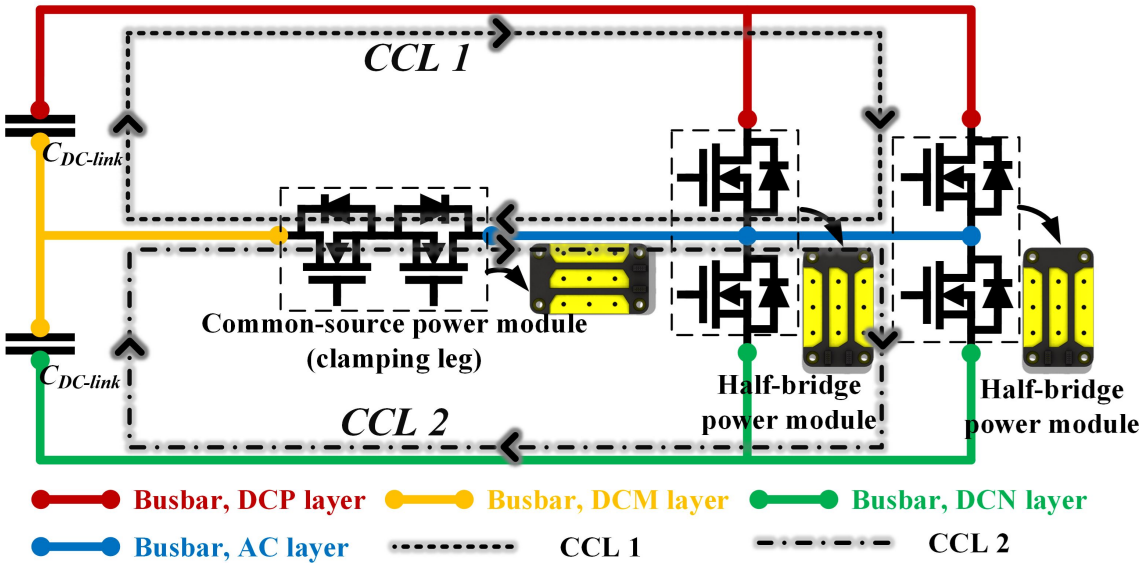


Fig. 3.3: The design schematic and the two CCL of 3L-TNPC, based on wolfspeed HT-3000-series half-bridge modules and Common-Source module.

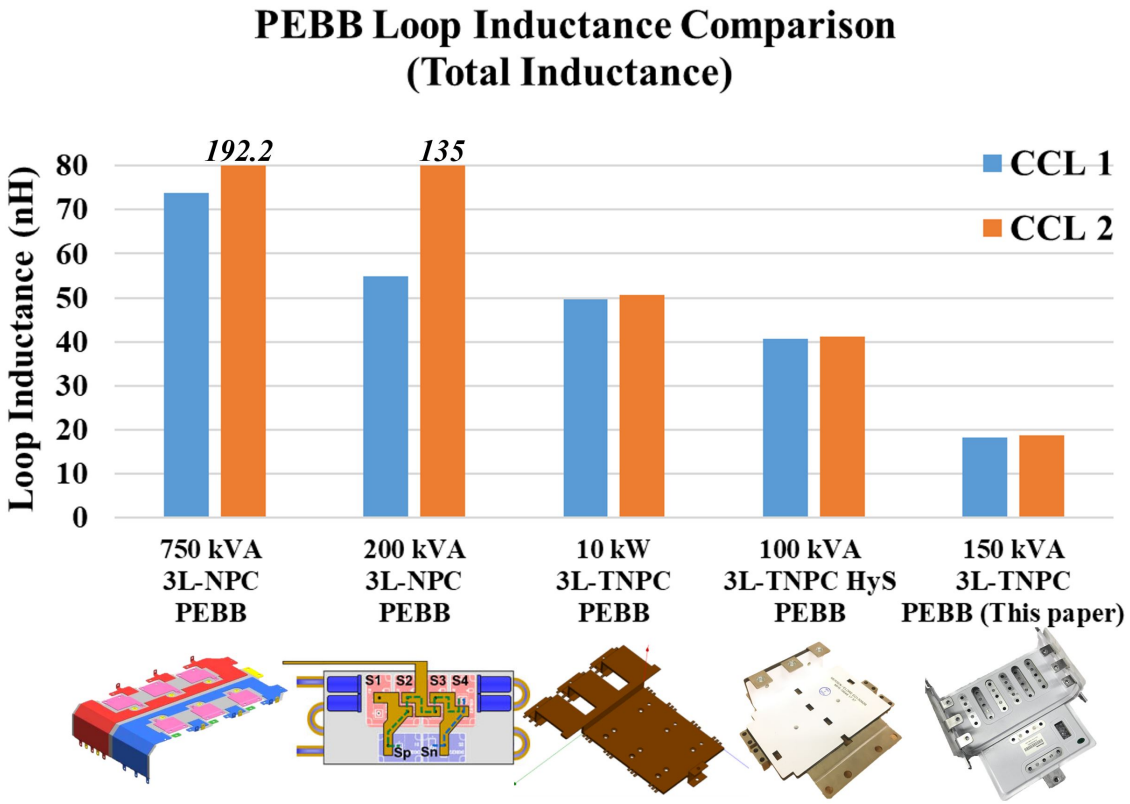


Fig. 3.4: Comparison of total CCL inductance for 3-level inverters

ficient (NTC) of the threshold voltage can further aggravate the dynamic current sharing problem. [23], [30] discuss the unbalanced dynamic current sharing caused by the mismatching of gate signal delay. Then the improved gate driver schemes are proposed to achieve gate synchronization enhancement. For example, [31] proposes an active-gate-resistance method to enhance synchronization. And [32] - [34] introduce the feedback loop in the gate driver to improve the delay matching. Besides, [35] - [37] analyze the current balancing problem induced by the differences of loop inductance. From the literature, comprehensive design considerations for dynamically balancing the current sharing can be summarized from three aspects:

1. At the semiconductor-device level, the paralleled power switches should have the uniform key parameters to guarantee the same switching speed. The key parameters include the threshold voltage (V_{th}), transfer conductance (g_{fs}), and semiconductor parasitic capacitance.

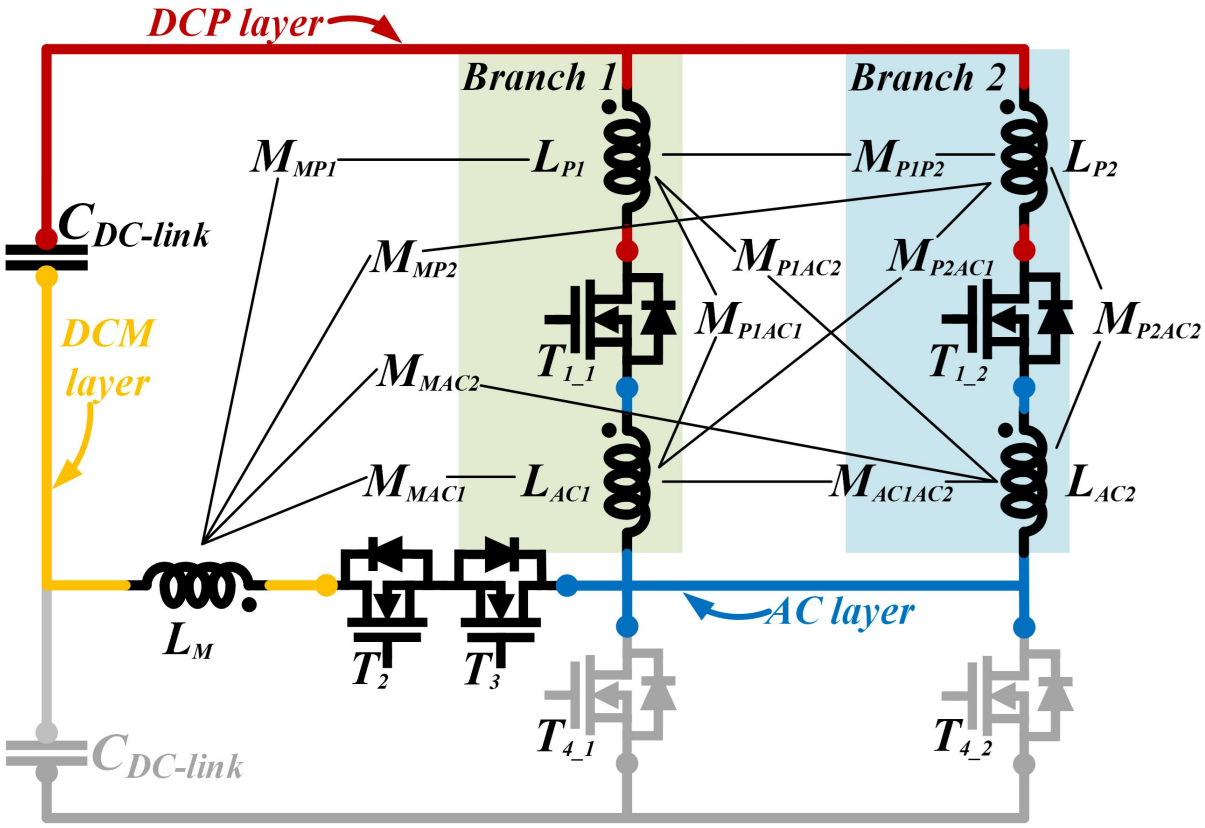


Fig. 3.5: The equivalent circuit of the configured PEBB.

2. From the gate driver aspect, the propagation delay and distortion induced by digital circuits should be tuned if independent gate drivers are used for parallel-driving. Otherwise, the quasi-common-source inductance should be minimized to avoid current circulating from power loop to gate loop [38], [39].

3. From the aspect of power-loop optimization, each paralleled branch should have the similar values of CCL inductance to keep the same speed of current commutation and equally distributed switching losses.

In general, the power-loop design and optimization for 2-level inverters (2-L) are well discussed [40] - [45], while few investigations are made for 3-level (3-L) inverters. Nevertheless 3-L inverters suffer from the higher value of parasitic inductance, due to the increased number of series-connected power switches in one current commutation loop (CCL) and geometrically larger

Fig. 3.6: Wolfspeed HT-3000 Series.

size of CCL [46] - [49]. As a result, the semiconductors will experience higher voltage stresses and more severe switching oscillations.

Moreover, the dynamic current sharing between parallel-switches is a great challenge for 3L-TNPC. As shown in Fig. 3.2, due to the more complex structure of 3L-TNPC, adding one parallel-branch will introduce more mutual-inductance items, thus making the analysis of inductance distribution more complicated. Unlike the useful power-loop design considerations summarized in [50] - [53] for the 2-L, the design considerations for 3-L inverter to achieve the equalized current sharing have not been fully developed.

The laminated busbar is one of the key components for high-power converter systems. It interfaces with power cables, passive filters, digital circuits, and power semiconductors. The thicker conductor layers can reduce the self-inductance and minimize resistive loss to avoid pathway overheating [54]. While the approximate lamination of busbar layers can effectively increase

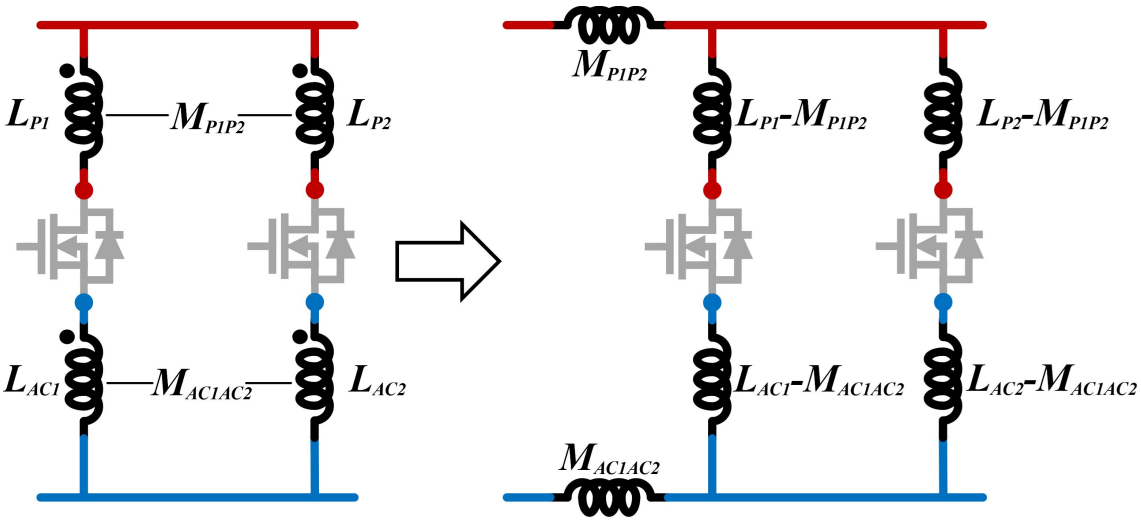


Fig. 3.7: Decoupling the mutual inductance at the two paralleled branches.

the magnetic cancellation effects and reduces power-loop inductance [41]. As the wide-bandgap devices (WBG) are used, the faster-switching characteristic will cause higher voltage and current overshoots during the transition. Therefore, minimizing busbar stray inductance is required.

This paper aims to solve the above problems as well as provide the optimized busbar geometrical design solutions. The paper first derives the mutual-inductance-decoupled busbar equivalent circuit from the highly coupled circuit by considering the busbar as three-port networks. This methodology has been previously utilized in the analysis of insertion gain of EMI filters [55], but has never been used to guide busbar design. With the decoupled-equivalent circuit, the effects of each inductance item on switching performance can be unveiled. And the parametric design target can be summarized accordingly.

A generalized five-step design procedure is then proposed to offer the optimized busbar design solutions. Instead of directly working on the busbar design in 3-D space, the proposed busbar-design procedure first focuses on 2-D optimization for power-module arrangement and busbar-terminal allocation. Then the 3-D busbar structure can be constructed from the optimized

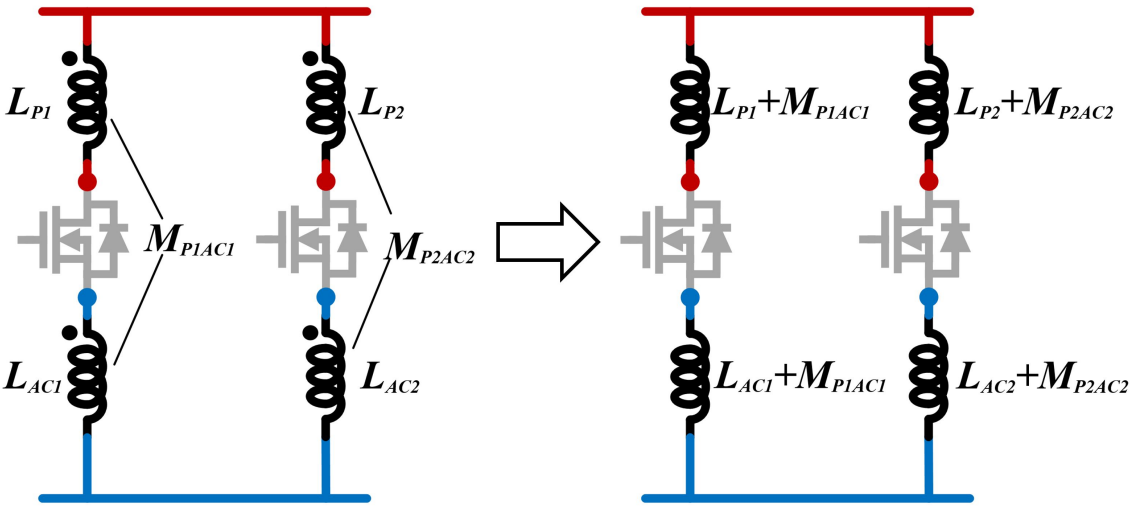


Fig. 3.8: Decoupling the mutual inductance at the same branch.

2-D schematics. Pre-manufacturing analysis can be performed to evaluate the performance and then the busbar is ready to be manufactured.

To provide a design instance, a busbar is proposed, designed and manufactured for a 150-kVA single-phase PEBB based on the wolfspeed HT-3000 modules. It shows lower value of busbar CCL stray inductance ($L_{stray,busbar}$) and the lower value of total CCL inductance ($L_{stray,busbar} + L_{stray,module}$) compared to the published literature, as shown in Fig. 3.4. And the inductance difference between the paralleled power-switches is less than 2 nH. By following the design procedure, a novel double-side-end decoupling busbar structure is derived and the advantages of this structure are evaluated extensively by experiments. The double-pulse test is performed under 500 A inductor current, 1000 V DC-link voltage. And the monitored case temperatures during continuous tests demonstrate the improvement on dynamic current sharing.

The paper is organized as the following. Section II introduces the busbar inductance model with considering mutual-inductance. Then the method to derive the mutual-inductance-decoupled circuit is provided. Based on the derived decoupled equivalent circuit, Section III discusses the

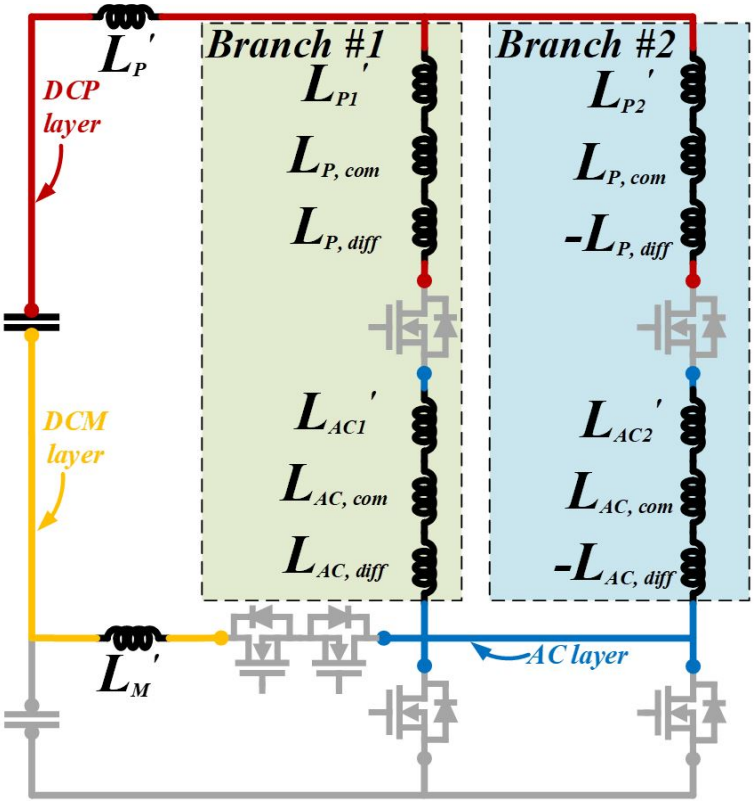


Fig. 3.9: The decoupled equivalent circuit of busbar.

method to reduce the total value of inductance and balance the parallel-branch inductance. A five-step design procedure is proposed and is exemplified by designing a busbar for 150-kVA 3L-TNPC phase leg. In Section IV, extensive experimental tests are carried out to evaluate the performance of the busbar.

3.3 Busbar Mutual-inductance-decoupled Equivalent Circuit

3.3.1 Power module introduction and busbar equivalent circuit

Power-module selection should be the starting point of the busbar design, as its profile significantly affects the busbar shape [42]. Directly using 3L-TNPC power-module can simplify the busbar design, nevertheless this plan suffers from limited commercial availability and fixed

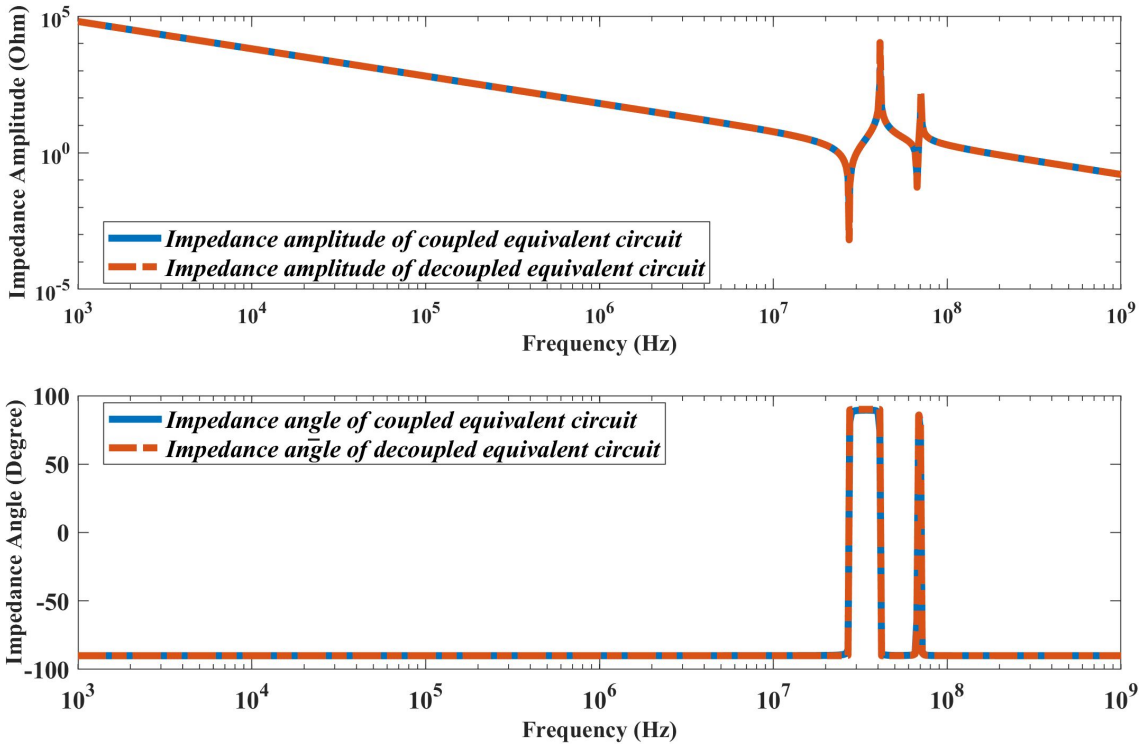


Fig. 3.10: Impedance measured from coupled circuit and decoupled circuit.

numbers of bare-die per switching position. The common-source (CS) power-modules, which are popular in DC-breaker applications, enjoy larger markets and commercial availability [59] - [59]. It can also be configured as the clamping leg of 3L-TNPC. And compared to using the single-switch module, the common-source module can effectively reduce the module-terminal inductance, module-to-module interfacing inductance, and simplifies the busbar structures. For the external leg of 3L-TNPC, two parallel half-bridge modules are used to reduce the conduction loss. The Wolfspeed high-performance HT-3000 series, as shown in Fig. 3.6 are utilized to build the inverter.

The equivalent circuit of 3L-TNPC is shown in Fig. 3.3. Four busbar layers are interfaced with modules to compose to 3L-TNPC. They are DC-positive (DCP) layer, DC-middle (DCM) layer, DC-negative (DCN) layer and output AC layer respectively. Because the 3L-TNPC shares two symmetrical current commutation loops (CCL), only one of CCL is analyzed, while the second

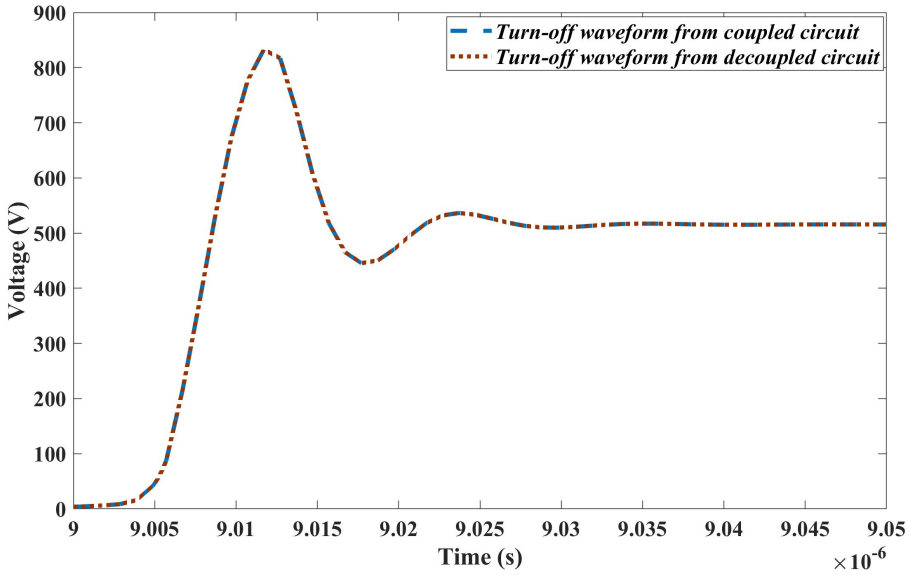


Fig. 3.11: Turn-off waveform of V_{DS} simulated based on coupled circuit and decoupled circuit.

one shares the same philosophy of analysis[11], [49]. Thus the equivalent circuit can be simplified as shown in Fig. 3.5. There are 5 self-inductance and 11 mutual-inductance, listed as the following,

1. Self-inductance of the two paralleled branches, on busbar DCP layer, L_{P_1} and L_{P_2}.

2. Self-inductance of the two paralleled branches, on busbar AC layer, L_{AC_1} and L_{AC_2}.

3. Self-inductance on DCM layer, L_M.

4. Mutual-inductance between the two paralleled branches,

   (a) $M_{P_1P_2}$, mutual-inductance between L_{P_1} and L_{P_2};

   (b) $M_{AC_1AC_2}$, mutual-inductance between L_{AC_1} and L_{AC_2};

   (c) $M_{P_1AC_2}$, mutual-inductance between L_{P_1} and L_{AC_2};

   (d) $M_{P_2AC_1}$, mutual-inductance between L_{P_2} and L_{AC_1}.

5. The mutual-inductance from the DCM layer, to the two paralleled branches,

TABLE 3.2: Busbar design consideration

Inductor Groups	Inductor Items	Parametric Design Target
Group 1	$L_{P1}\prime$	1. $L_{P1}\prime \simeq L_{P2}\prime$; 2. $L_{AC1}\prime \simeq L_{AC2}\prime$
	$L_{P2}\prime$	Equivalent to,
	$L_{AC1}\prime$	1. $L_{P1} \simeq L_{P2}$; 2. $L_{AC1} \simeq L_{AC2}$
	$L_{AC2}\prime$	3. $M_{P1AC1} \simeq M_{P2AC2}$;
Group 2	$L_{P,diff}$	1. $L_{P,diff} \simeq 0$; 2. $L_{AC,diff} \simeq 0$
	$L_{AC,diff}$	Equivalent to,
		1. $M_{MP1} \simeq M_{MP2}$ 2. $M_{MAC1} \simeq M_{MAC2}$
Group 3	$L_{P,com}$	Reduce self-inductance, increase mutual-inductance;
	$L_{AC,com}$	
Group 4	$L_P\prime$	Reduce self-inductance, increase mutual-inductance;
	$L_M\prime$	

(a) M_{MP_1}, M_{MP_2}, mutual-inductance between L_M and L_{P_1}, L_M and L_{P_2}, respectively;

(b) M_{MAC_1}, M_{MAC_2}, mutual-inductance between L_M and L_{AC_1}, L_M and L_{AC_2}, respectively.

Though balancing the parallel-branch inductance can improve the dynamic current sharing, for example, balancing the stray inductances from branch 1 and branch 2 in Fig. 3.5, the inductance value of each individual branch is impossible to be obtained directly, because of the mutual inductor items. Moreover, it is too complex to summarize the power-loop design considerations based on the mutual-inductance-coupled circuits, making busbar stray-inductance optimization more difficult. Therefore, it is necessary to derive the mutual-inductance-decoupled equivalent circuit.

3.3.2 The derivation of mutual-inductance-decoupled equivalent circuit

The method of deriving mutual-inductance-decoupled equivalent circuit relies on the theorem of three-port network. As shown in Fig. 3.8, the mutual inductance from the same-branch is decoupled first. Then based on the theorem of three-port network, Fig. 3.7 provides the method to decouple the mutual inductance when they are from two parallel branches. Eventually all the mutual-inductance can be decoupled while only the equivalent self-inductance items are left, as shown in Fig. 3.9. All the inductor items from Fig. 3.9 are described by Eq. (3.1) - (3.10).

$$L'_P = M_{P_1P_2} + M_{P_1AC_2} + M_{P_2AC_1} \tag{3.1}$$

$$L'_{P_1} = L_{P_1} + M_{P_1AC_1} \tag{3.2}$$

$$L'_{P_2} = L_{P_2} + M_{P_2AC_2} \tag{3.3}$$

$$L_{P,com} = -M_{P_1P_2} - M_{P_1AC_2} - M_{P_2AC_1} \tag{3.4}$$

$$L_{P,diff} = M_{MP_1} - M_{MP_2} \tag{3.5}$$

$$L'_{AC_1} = L_{AC_1} + M_{P_1AC_1} \tag{3.6}$$

$$L'_{AC_2} = L_{AC_2} + M_{P_2AC_2} \tag{3.7}$$

$$L_{AC,com} = -M_{AC_1AC_2} - M_{P_2AC_1} \tag{3.8}$$

$$L_{AC,diff} = M_{MAC_1} - M_{MAC_2} \tag{3.9}$$

$$L'_M = L_M + M_{MP_1} + M_{MP_2} + M_{MAC_1} + M_{MAC_2} + M_{AC_1AC_2} \tag{3.10}$$

To demonstrate the derived model, the original coupled model and the decoupled model are built in circuit simulator. AC-impedance frequency response and time-domain turn-off V_{DS} waveforms on T_1 from the two models are simulated respectively, as shown in Fig. 3.10 and 3.11.

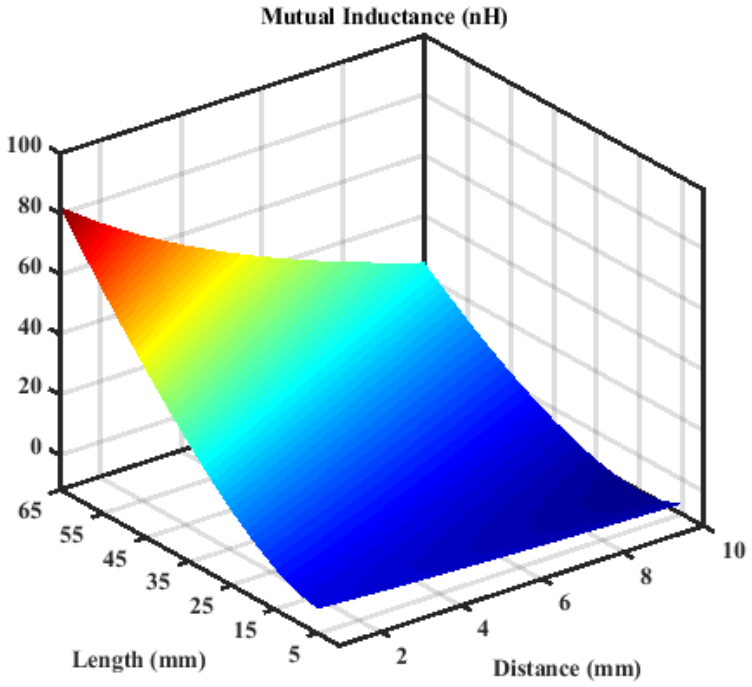


Fig. 3.12: The value of mutual inductance

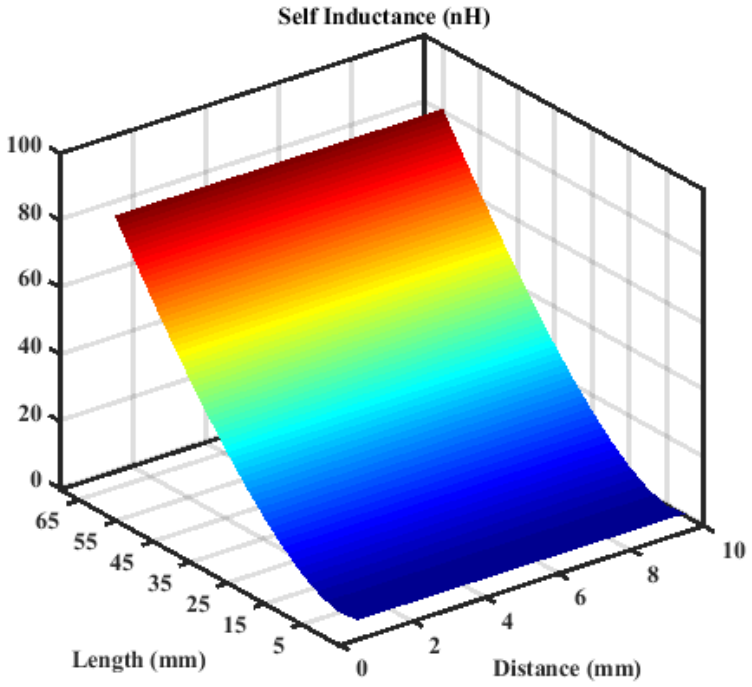


Fig. 3.13: The value of self inductance

It can be seen that the AC response of the two circuits are identical from 1 kHz to 1 GHz. And V_{DS} turn-off waveforms of T_1 from the two circuits are very close as well. Thus the consistency of the derived equivalent circuit can be verified.

3.4 Busbar Parametric Targets and Design Considerations

3.4.1 Parametric targets of busbar

The derived-equivalent model can provide direct comparison of stray inductance between the parallel power switches. Moreover, busbar design considerations can be discussed based on the derived circuit. Based on their effects on switching performance, the inductor items from Fig. 3.9 are purposely divided into four groups, as summarized in table 3.2.

Group I includes unique inductor items from each parallel branch, specifically meaning that these inductor items only exists in one parallel branch exclusively. For example, the inductor items L'_{P1}, L'_{P2}, L'_{AC1} and L'_{AC2} in Fig. 3.9 are included in group I. The values of group I inductance should be small to limit total stray inductance. Besides, to equalize inductance distribution, the values of group I inductance from each parallel branches should be similar. By combining with Eq. (3.2, 3.3, 3.6, 3.7), the parametric target for group I inductance is summarized in table 3.2.

Group II contains the so called differential inductance, specifically meaning that both parallel branches have the inductor items, but with different polarities. For example, the differential inductor items from branch 1 are $L_{P,diff}$ and $L_{AC,diff}$ in Fig. 3.9, while they become to $-L_{P,diff}$ and $-L_{AC,diff}$ at branch 2. As a result, the group II inductor items significantly diversify the inductance distribution between parallel branches, leading to unbalanced dynamic current sharing and uneven switching loss. Therefore, special efforts are necessary to minimize group II inductance. Based on

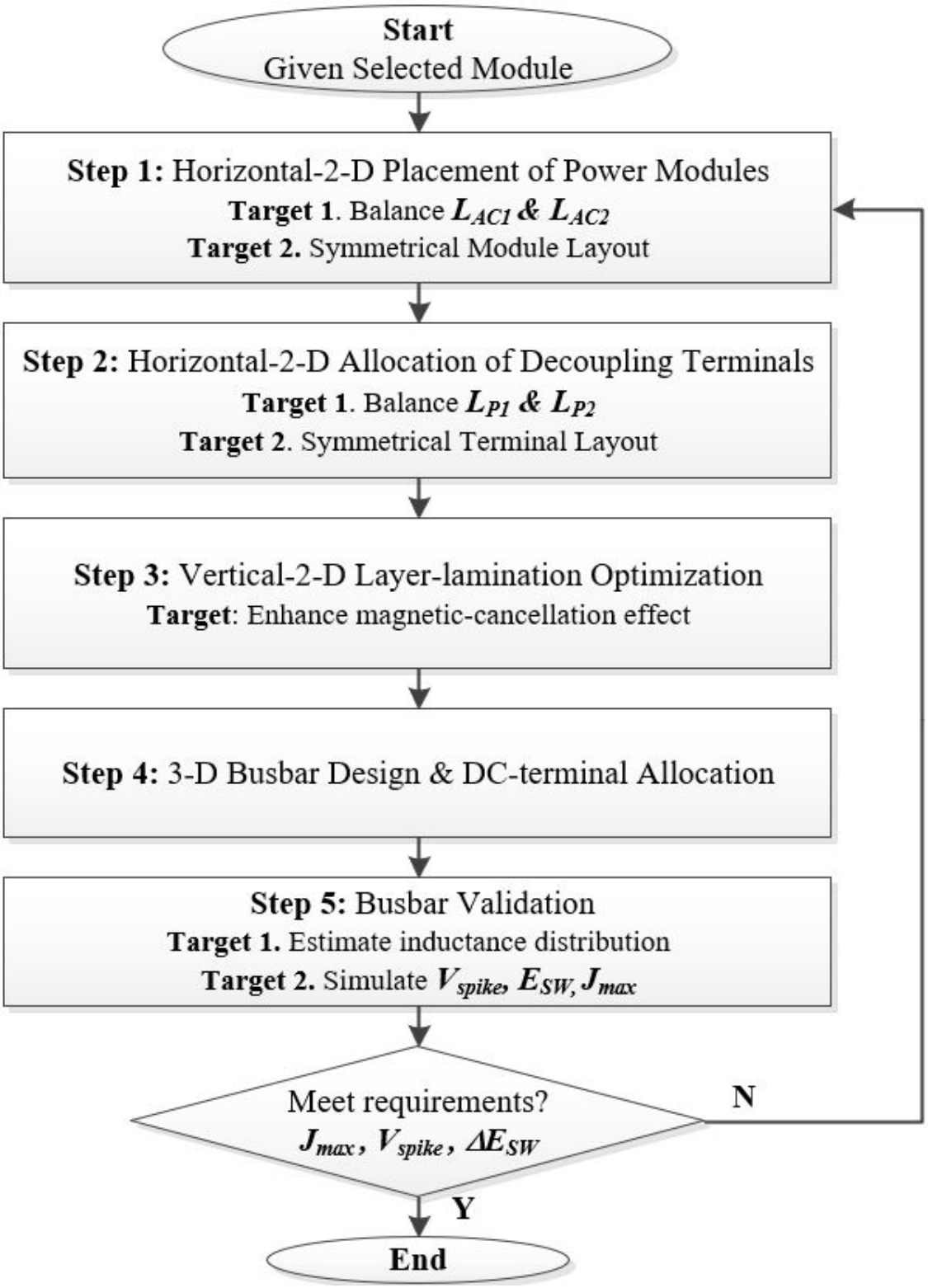


Fig. 3.14: Busbar design flowchart

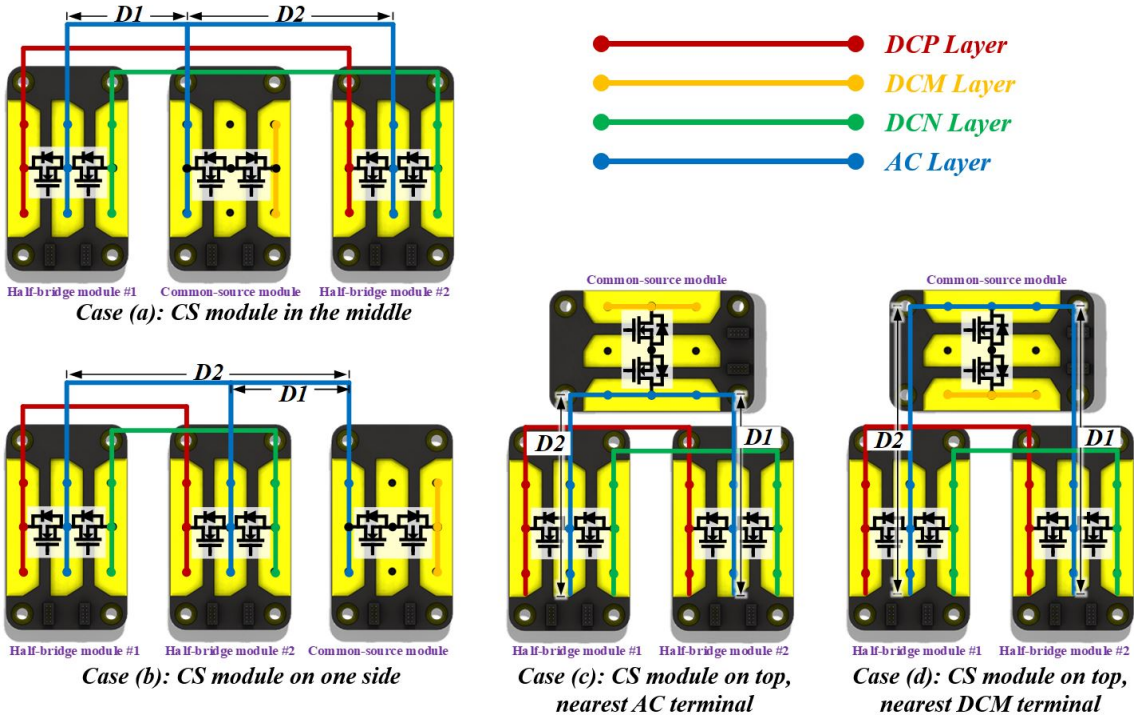


Fig. 3.15: 2-dimensional spatial arrangement of power modules

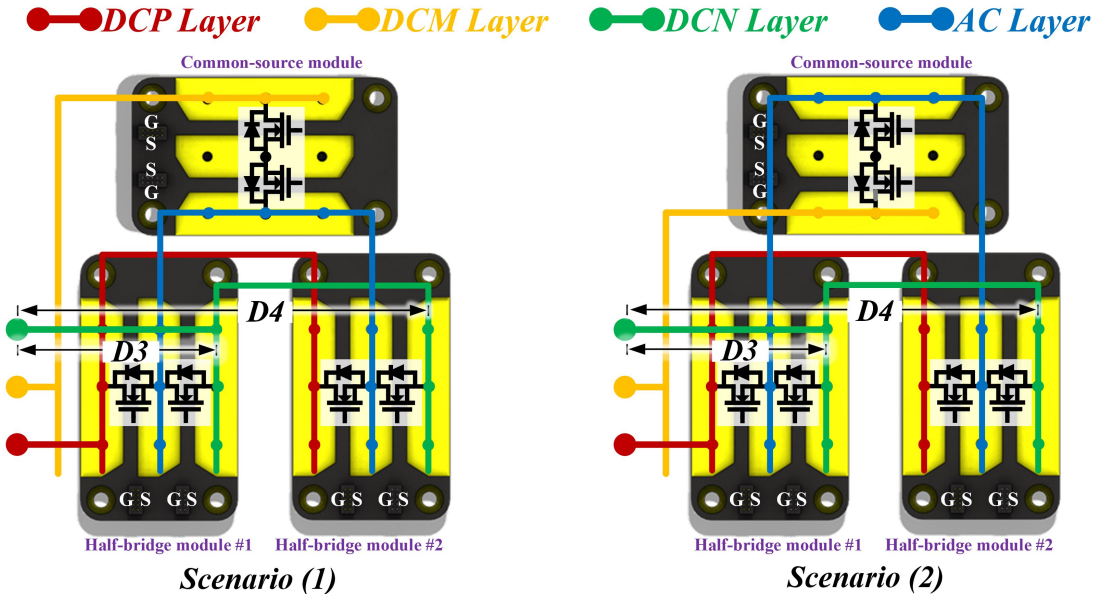


Fig. 3.16: 2-dimensional configuration single-side-end AC terminal

Eq. (3.5, 3.9), the parametric target can be derived in table 3.2.

Group III covers the so called common inductance items from the parallel branches, specifically meaning that all the parallel branches have these inductor items, with same values of inductance and same polarity, for example, $L_{P_{,com}}$, and $L_{AC_{,com}}$ shown in Fig. 3.9. Those inductor items will not contribute to the difference of branch-to-branch inductance.

Group IV is comprised of the inductor items which are outside from the parallel branch, such as L'_P and L'_M in Fig. 3.9. Similar to the effects of group III, the inductance values from group IV do not diversify branch-to-branch inductance distribution.

Though inductance values from group III and group IV do not worse the parallel-branch dynamic current sharing, those inductance values should be the minimized to limit the total CCL inductance. The well-discovered method for 2-level-topology busbar can be directly applied here, including adjacent decoupling-terminal allocation [60] and enhancement of magnetic-cancellation effects [41].

3.4.2 Busbar design considerations

To interpret the parametric targets to the specified busbar design considerations, it is necessary to understand the factors affecting self and mutual inductance. The self-inductance can be estimated by Eq. 3.11 and the mutual-inductance can be estimated by Eq. 3.12 [61] - [64], where l, w and t are the equivalent lengths, width and thickness of the busbar layer, and d is the distance between two laminated layers of busbar. The graphic interpretation of the equations are plotted as Fig. 3.13 and 3.12.

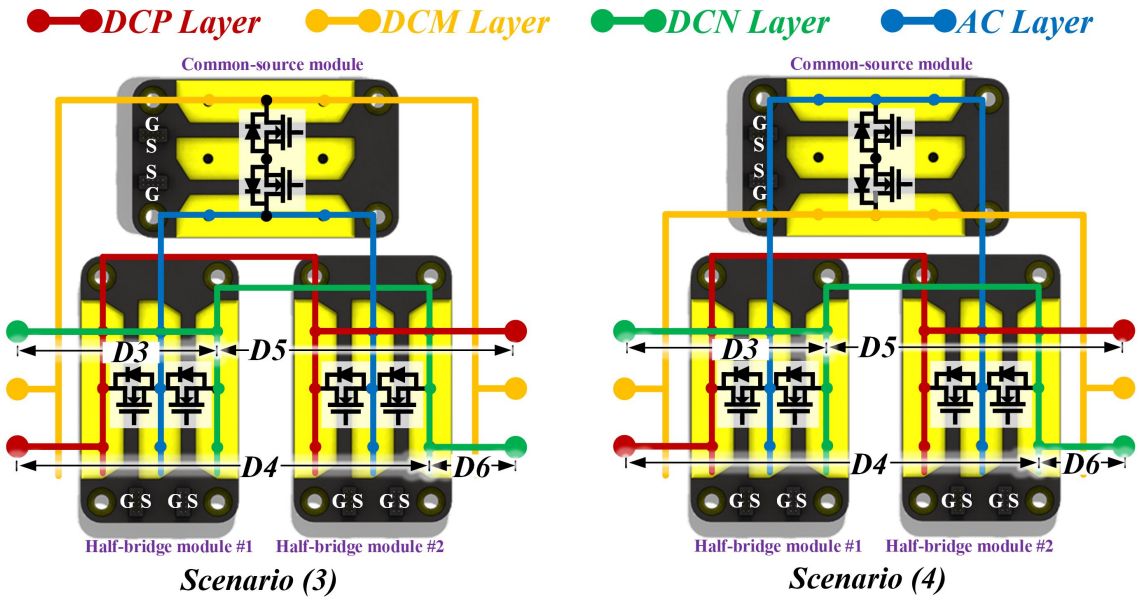


Fig. 3.17: 2-dimensional configuration double-side-end AC terminal

$$L = 2l\left[\left(\ln\left(\frac{2l}{w+t}\right)+0.5+0.2235\left(\frac{w+t}{l}\right)\right)\right]nH \tag{3.11}$$

$$M = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{l}{d}+\sqrt{1+\left(\frac{l}{d}\right)^2}\right)-\sqrt{1+\left(\frac{d}{l}\right)^2}+\frac{d}{l}\right] \tag{3.12}$$

Practically, the busbar shares the same thickness of each conducting layer, t and similar width w, the value of self-inductance is majorly affected by the equivalent conducting length. Thus, to meet the parametric target of matching the value of L_{P_1} and L_{P_2}, L_{AC_1} and L_{AC_2}, the designed busbar should provide the similar length of current commutation loop for each paralleled switches.

The value of mutual inductance is affected by both layer-to-layer distance, d and current-commutation length, l, as shown in Fig. 3.13. Thus the symmetrical layout is the better way to match the two mutual inductance. In conclusion, to achieve the matching value of $M_{P_1AC_1}$ and $M_{P_2AC_2}$, the current path from AC-layer should be symmetrical to DCP-layer. Similarly, the current

Fig. 3.18: Manufactured busbar

path in DCM-layer should be symmetrical to DCP layer and AC layer, to achieve the matching value between M_{MP_1} and M_{MP_2}, and between M_{MAC_1} and M_{MAC_2}, as summarized in Table. 3.2.

3.5 Conduction-layer Design Procedures

After having the busbar design targets clear, a design procedure to systematically achieve these targets is necessary. In this section, a step-by-step busbar design procedure is proposed, as shown in Fig. 3.14. Instead of directly starting with the 3-dimensional (3-D) busbar design, the proposed procedure starts with optimizing busbar schematic at the horizontal 2-dimensional (2-D) planar, then optimize the lamination sequence at vertical 2-D plane. The optimized busbar from 2-D schematics can be constructed to the real 3-D busbar structure in the next.

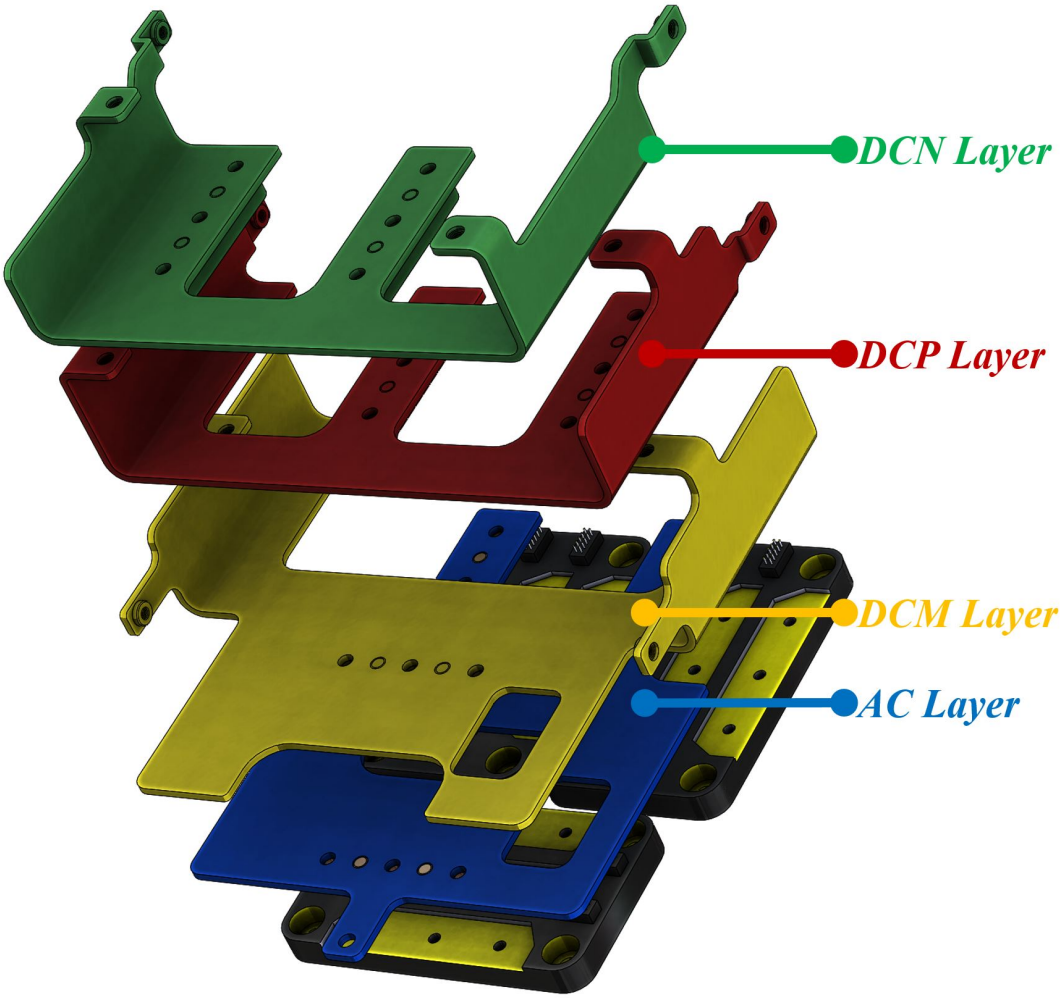


Fig. 3.19: Exploded view of busbar

The effectiveness of the method has been proven by a design example of 150-kVA phase leg busbar based on Wolfspeed HT-3000-series modules. As the output of the proposed design procedure, a novel double-side-end structure is derived. The busbar designed by following the procedure shows lower stray inductance than the literature, shown in Fig. 3.4 and the improved dynamic current sharing is demonstrated by monitoring the case temperature during the continuous test.

In Fig. 3.14, the first step of the busbar design is to properly arrange the modules on a horizontal plane. It is because that the module placement directly decides the overall busbar shape

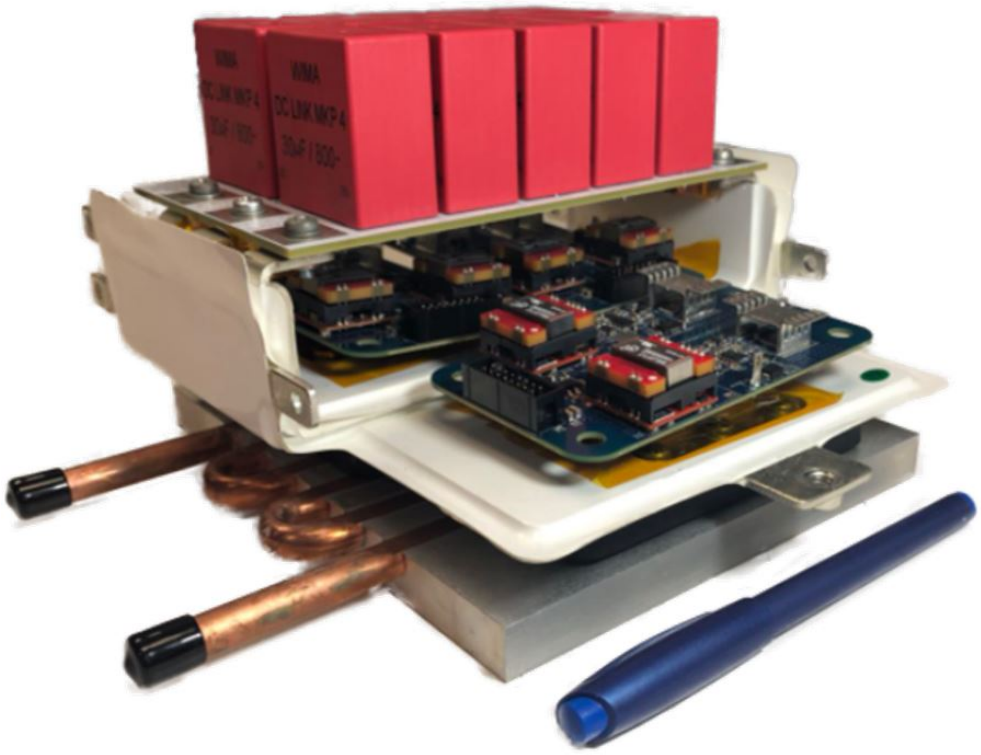


Fig. 3.20: Physically assembled PEBB

and greatly affects the values of self-inductance L_{AC1} and L_{AC2} in Fig. 3.5.

Four strategies of power module placement are listed in Fig. 3.15. The power module terminals with the same voltage potential are connected by the solid line to form the electric-connection schematics. The marked distance, D1 and D2 represent the shortest distance from the common-source module to the first and the second half-bridge modules respectively. As stated previously, value differences between D1 and D2 can reflect the inductance differences between L_{AC_1} and L_{AC_2}. Therefore it is necessary to equalize the distance, D1 and D2 to balance L_{AC_1} and L_{AC_2}.

To achieve this idea, case (a) and (b) in Fig. 3.15 illustrate the shoulder-by-shoulder placement of power modules. Case (a) places the common-source power module in the middle of half-bridge modules, while the common-source module is located on one side in case (b). It can

be concluded that case (a) offers more symmetrical module layout compared to case (b), and it has less differences between D2 and D1. Besides, the case (c) and (d) exemplify another ways to place power module, which rotate the common-source module by 90 degrees and place it on the wide-side of half-bridge modules. This module-arrangement strategy can achieve the same value of D2 and D1, which indicates similar values between L_{AC_1} and L_{AC_2}.

In addition, in case (c) and (d), the rotated AC terminal offers the better symmetry of pathway layout. Thus it will be helpful to balance $M_{P_1AC_1}$ and $M_{P_2AC_2}$. Therefore case (c) and (d) are selected for the analysis in the next step.

The next is to properly allocate the decoupling terminals. The decoupling terminals provide connecting ports to decoupling capacitors or DC-link capacitors to reduce the total CCL inductance. And the decoupling terminals are usually separated from the power-input terminals in order to separate the DC and AC current paths and avoid busbar overheating.

Fig. 3.16 and 3.17 illustrates four feasible decoupling-terminal optimization scenarios. Scenarios (1) and (2) in Fig. 3.16 place the decoupling terminal only on one side of the busbar. This method is commonly utilized for 2-level inverters and can effectively limit the busbar stray inductance [41], [42], [45]. But for three-level inverters, only one set of decoupling terminal is not sufficient to minimize the current commutation distance, thus this allocation strategy is not the optimum solution. For example, in Fig. 3.16, no matter in which scenario, the distance, D4 is always greater than D3. As a result, the self stray inductance from the second half-bridge power module has the higher value than the one from the first half-bridge module.

Compared to the traditional single-sided decoupling strategy, the proposed double-sided decoupling strategies can significantly improve the inductance uniformity between the two paralleled semiconductors. As shown in Fig. 3.17, thanks to the additional set of decoupling terminal,

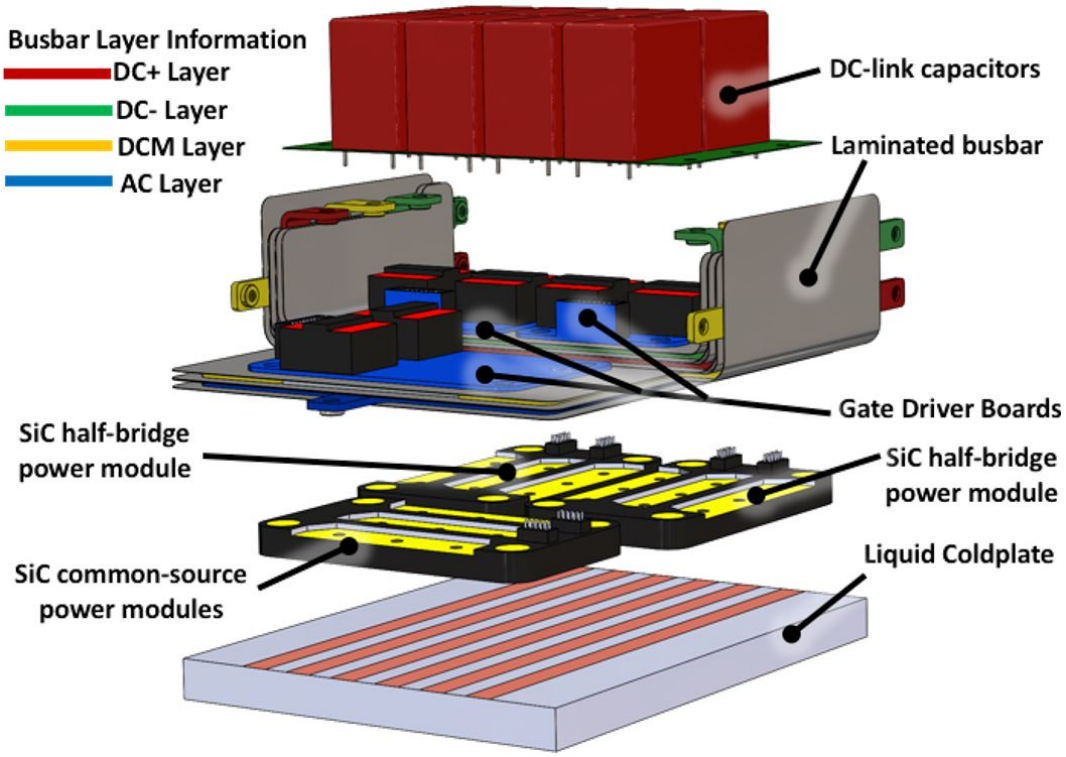


Fig. 3.21: Exploded view of PEBB

each of the half-bridge module has two independent current commutation paths in parallel. As a result, the self-inductance induced by the distance from module to terminals can be balanced. For example, the shortest distance in Fig. 3.17, D6 corresponds to the self-inductance, which has similar values of the equivalent inductance generated by D3 in parallel with D5.

Besides, the double-side-end decoupling strategy offers the better layout symmetry of DCM layer, DCN layer and DCP layer when compared to the single-side-end structure. This will help to limit the differential inductance in Eq. (3.5) and (3.9) and average the inductance distributions between the paralleled branches.

Adding the third-side decoupling terminal might help with the overall structural performance. Nevertheless, the manufacturability starts to become a limiting factor as each layer requires bending and stacking with thick metals. The process tolerance and assembly difficulty result in

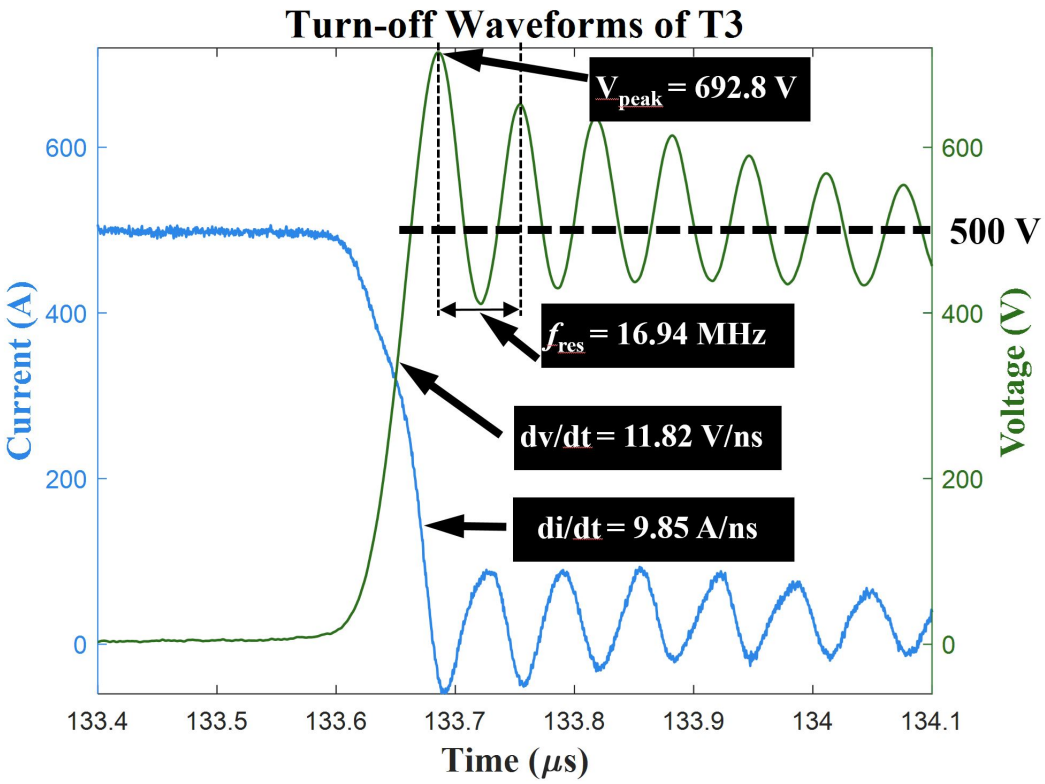


Fig. 3.22: Switching waveforms of T_3, at 1000V DC-link voltage and 500A commutation current

different performances than expectation. Besides, the decoupling terminal may also increase the difficulty of the power connection layout. It may block the input power wiring and screw terminals and thus further increase the complexity of the design. And the weight of the busbar will increase as well. Thus the double-side busbar structure is selected.

The design procedures on the horizontal plane are completed by step-one and step-two. Then the vertical lamination strategy should be implemented before forming the final busbar structure. References [41], [65] have discussed the lamination strategy for two-level inverters in detail. Specifically, the positive layer and the negative layer should be laminated as close as possible to magnify the magnetic cancellation effect and thus obtain the lower stray inductance. The lamination strategy of 3-level inverters can be directly adopted from 2-level inverters, thus it will not be explained in detail in this paper.

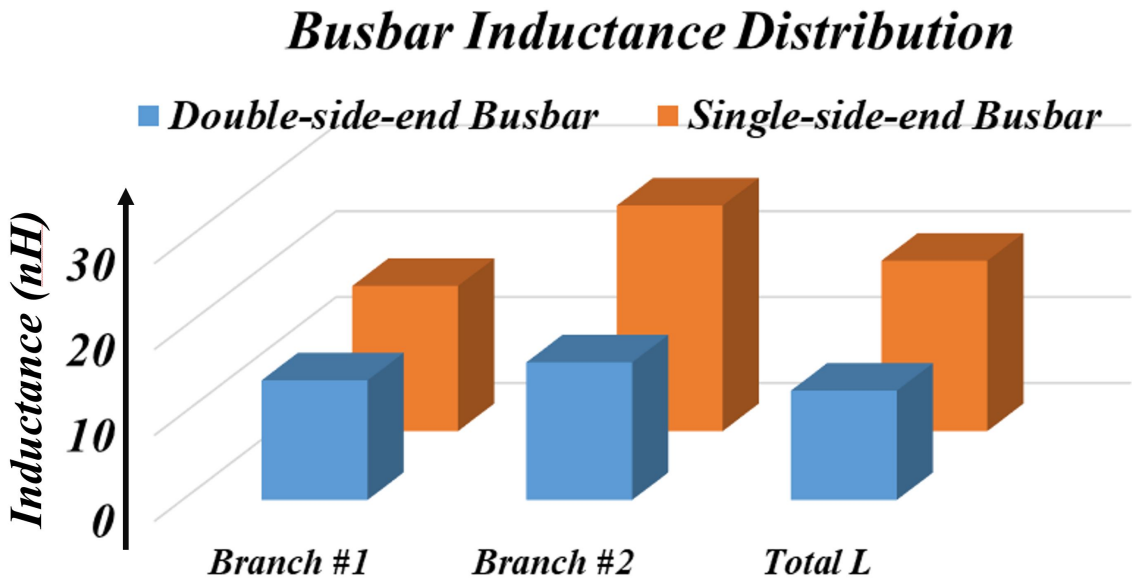


Fig. 3.23: Inductance distribution of the two busbar structures

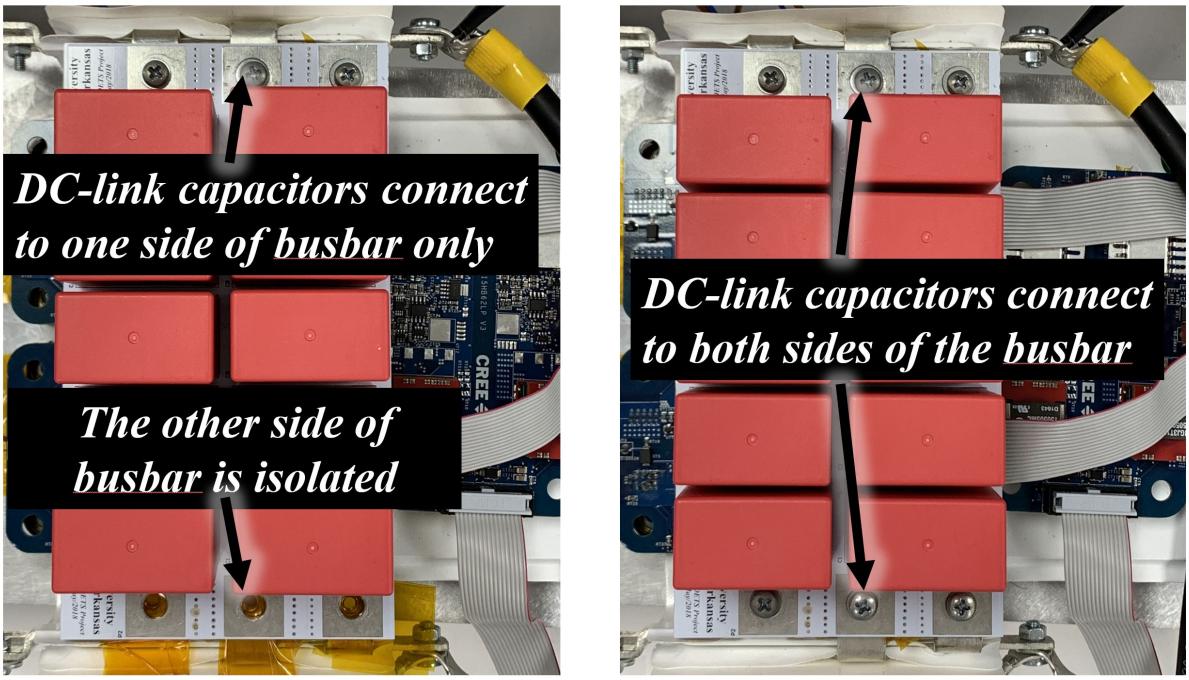
Based on the optimization completed at the 2-D planar, the 3-D busbar can be constructed. The physical structure of the busbar is shown in Fig. 3.18. With the insulation layers hidden, the busbar exploded view is shown in Fig. 3.19. The whole single-phase 3L-TNPC power inverter is assembled in Fig. 3.21 and 3.20.

3.6 Evaluation of Designed Busbar

3.6.1 Busbar stray inductance

To evaluate the stray inductance of the busbar, both the simulation and experiments are carried out. The designed busbar is firstly analyzed by the simulation based on ANSYS finite element analysis (FEA). For comparison, both the single-side-end structure and the double-side-end busbar structure are analyzed, with the stray inductance distribution shown in Fig. 3.23.

In Fig. 3.23, it is known that the double-side-end busbar structure shows the lower stray inductance of 12.73 nH, which is 7.21 nH less than the single-side-end structure. And the pro-

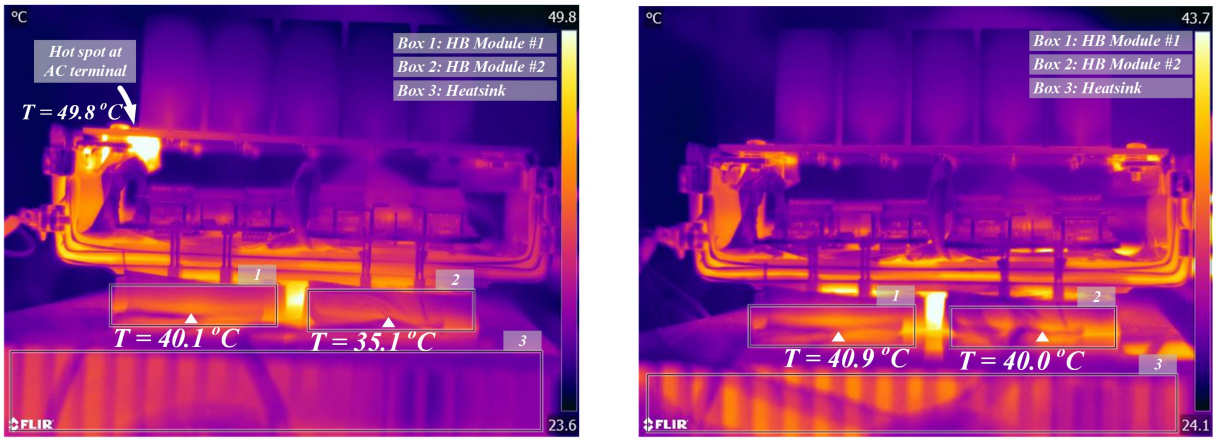


Setup (a): Single-side-end terminal **Setup (b): Double-side-end terminal**

Fig. 3.24: Test setups for single-side-end busbar structure and double-side-end busbar structure

posed double-side-end structure successfully limits the inductance difference between the first and the second parallel branch by 2.0 nH. As a comparison, the single-side-end structure has the differences of over 10 nH. Consequently, the localized overheating problem is more severe, as shown in the continuous test later.

Besides, on-busbar double-pulse test (DPT) are performed at DC-link voltage of 1-kV (device commutation voltage is 500 V), and commutation current at 500 A, as shown in Fig. 3.22. The resonant frequency during turn-off is utilized to estimate the total inductance [41]. Though the only the total inductance can be estimated, the module inductance has been well analyzed in paper [44], [66]. Therefore busbar inductance can be estimated by Eq. 3.14. In addition, Eq. 3.13 can also be used to estimate the total loop inductance.



Case (a): Single-side-end terminal **Case (b): Double-side-end terminal**

Fig. 3.25: Thermal map measured by thermal camera

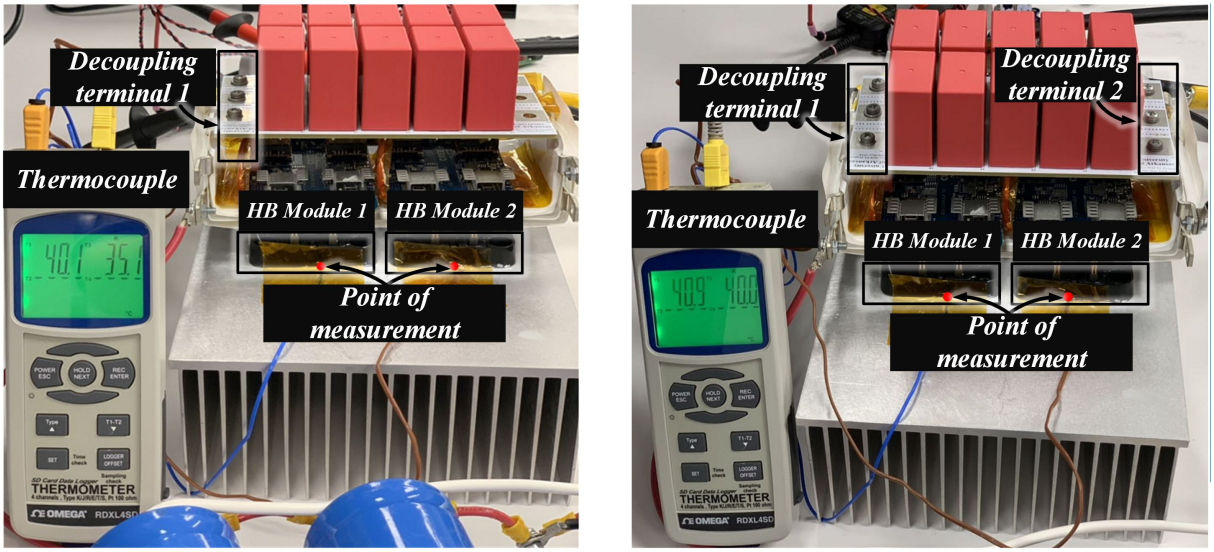
$$V_{\text{overshoot}} = L_{\text{Loop}} \frac{di_f}{dt} \tag{3.13}$$

It is known that both the methods show consistent results in busbar inductance. The Q3D method provides more details on inductance distribution at different branches, while the DPT method can experimentally verify the total busbar inductance on the physical busbar.

$$f_{res} = \frac{1}{\sqrt{(L_{busbar} + L_{module})(C_{oss} + C_{busbar})}} \tag{3.14}$$

3.6.2 Continuous test

As discussed previously, unbalanced dynamic current sharing can enlarge the temperature differences between the parallel switches. Therefore, the continuous tests are implemented for testing the thermal distribution as well as evaluate the busbar performance. To compare the performance differences, the busbar is configured as single-side-end end structure and double-side-end structure, as shown in Fig. 3.24. Both thermal camera and the thermocouple are used for temperature monitoring. To perform the accurate temperature measurement, the thermocouple pins are



Case (a): Single-side-end terminal **Case (b): Double-side-end terminal**

Fig. 3.26: Case temperature measured by thermocoupler

directly attached to the baseplate of the module.

The thermal distributions captured by thermal camera are shown in Fig. 3.25. And the case temperatures monitored by thermocouple are shown in Fig. 3.26. Because the decoupling-terminal connector suffers a thermal hotspot in the single-side-end structure, as it can be seen in Fig. 3.25, single-side-end structure is tested only at 20 kVA while the double-side-end structure is tested at 35 kVA. As the conclusion based on the test, by keeping the case temperature of half-bridge module 1 the same, the case temperature differences on single-side-end structure is around 5 ^oC, while it is less than 1^oC during the double-side-end structure. Thus the effectiveness of the double-side-end busbar structure is proven.

By using the double-side-end busbar structure, the continuous power is pushed to 70 kVA. The test setup for the higher-power continuous testing is shown in Fig. 3.27. The waveform captured at 70 kVA output power, 1000 V DC-link voltage, and switching frequency of 30 kHz is shown in Fig. 3.28. 150 kVA testing results are available in the later stage of this research project.

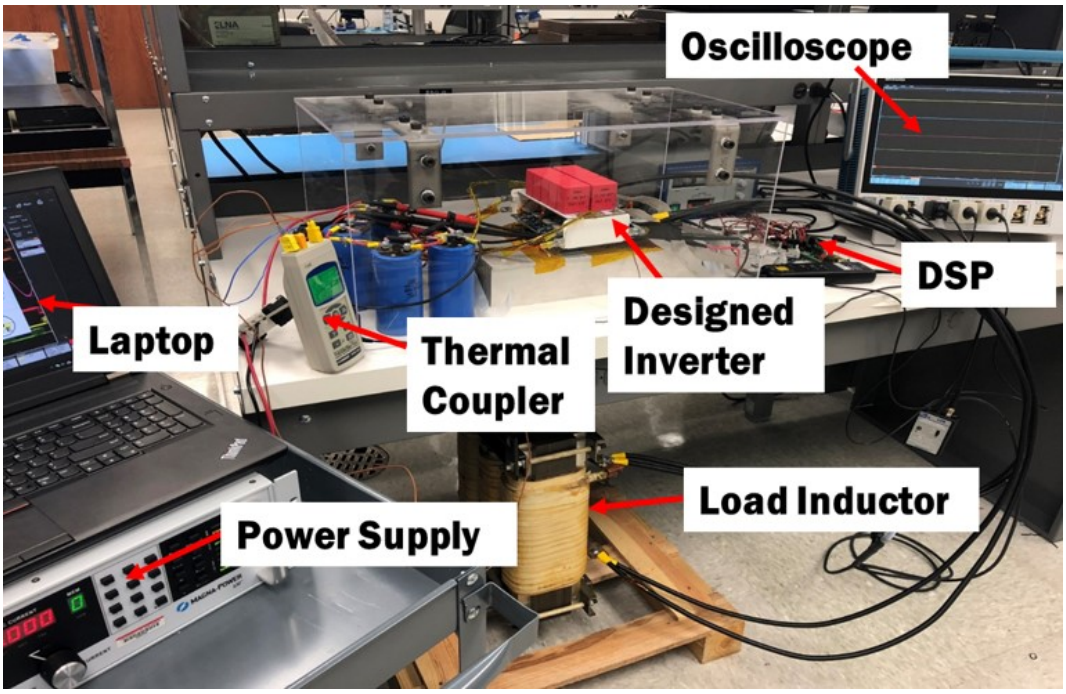


Fig. 3.27: Experiment setup for continuous test

However, the DPT result presented in this paper is tested at 500 A inductor current, and 1000 V DC-link voltage. The switching characteristics illustrated in the DPT is equivalent to continuous test at 150-kVA case. Although temperature stress tested at 70 kVA is not exactly the same as 150-kVA, the differences between hotspots and temperature distribution should stay the same. Thus we think the 70-kVA testing provides a projection for PEBB thermal performance at 150-kVA testing.

3.7 Conclusion

This paper provides a design guidance of the busbar for 3L-TNPC. The paper first introduced the method to derive mutual-inductance-decoupled equivalent circuit of laminated busbar. And based on the derived circuit, busbar design considerations are discussed and a five-step design procedure is proposed to offer the systematical way to design busbar for multi-level inverters. By taking the advantage of the proposed double-side-end structure, the designed busbar achieves the

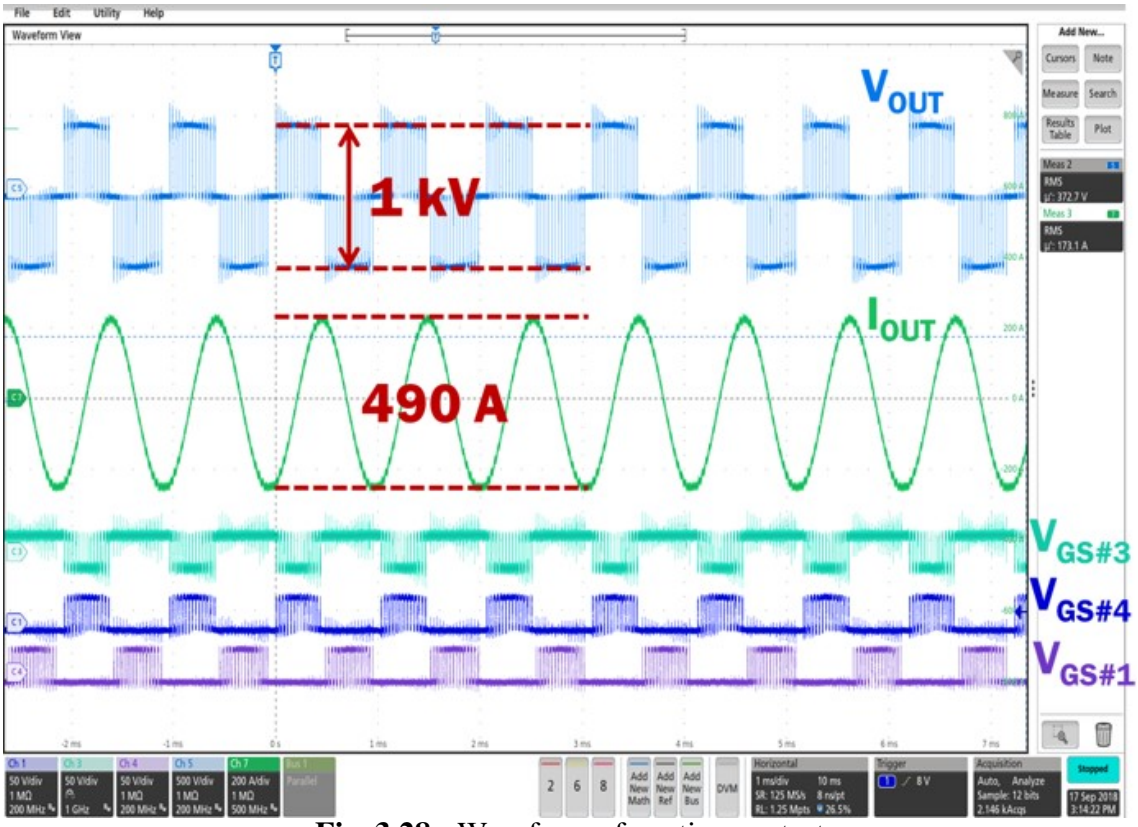


Fig. 3.28: Waveform of continuous test

lower stray inductance than the published literature. And the enhanced performance of dynamic current sharing are experimentally tested and compared.

Acknowledgment

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3.8 Bibliography

[1] J. A. Weimer, “Electrical power technology for the more electricaircraft,” in[1993 Proceedings] AIAA/IEEE Digital Avionics SystemsConference. IEEE, 1993, pp. 445–450.

[2] J. Rosero, J. Ortega, E. Aldabas, and L. Romeral, “Moving towardsa more electric aircraft,”IEEE Aerospace and Electronic SystemsMagazine, vol. 22, no. 3, pp. 3–9, 2007.

[3] W. Cao, B. C. Mecrow, G. J. Atkinson, J. W. Bennett, and D. J. Atkinson,“Overview of electric motor technologies used for more electric aircraft(mea),”IEEE transactions on industrial electronics, vol. 59, no. 9, pp.3523–3531, 2012.

[4] P. Wheeler and S. Bozhko, “The more electric aircraft: Technology and challenges.”IEEE Electrification Magazine, vol. 2, no. 4, pp. 6–12,2014..

[5] U. Drive, “Electrical and electronics technical team roadmap,”Partner-ship Plan, Roadmaps, and Other Documents, 2013..

[6] R. Jansen, C. Bowman, A. Jankovsky, R. Dyson, and J. Felder,“Overview of nasa electrified aircraft propulsion (eap) research forl arge subsonic transports,” in53rd AIAA/SAE/ASEE Joint Propulsion Conference, 2017, p. 4701..

[7] D. Zhang, J. He, and D. Pan, “A megawatt-scale medium-voltage high efficiency high power density “sic+ si” hybrid three-level anpc inverter for aircraft hybrid-electric propulsion systems,” in2018 IEEE Energy Conversion Congress and Exposition (ECCE).IEEE, 2018, pp. 806–813.

[8] R. M. Burkart, “Advanced modeling and multi-objective optimization of power electronic converter systems,” Ph.D. dissertation, ETH Zurich,2016..

[9] R. Burkart and J. W. Kolar, “Component cost models for multi-objective optimizations of switched-mode power converters,” in2013IEEE Energy Conversion Congress and Exposition.IEEE, 2013, pp.2139–2146.

[10] Y. Chen, Z. Yuan, and F. Luo, “A model-based multi-objective optimiza-tion for high efficiency and high power density motor drive inverters for aircraft applications,” in NAECON 2018 - IEEE National Aerospace and Electronics Conference, July 2018, pp. 36–42.

[11] M. Zhu, D. J. Perreault, V. Caliskan, T. C. Neugebauer, S. Guttowski, and J. G. Kassakian, “Design and evaluation of feed-forward active ripple filters,” *IEEE Transactions on Power Electronics*, vol. 20, no. 2, pp. 276–285, March 2005.

[12] M. Schweizer and J. W. Kolar, “Design and implementation of a highly efficient three-level t-type converter for low-voltage applications,”IEEE Transactions on Power Electronics, vol. 28, no. 2, pp. 899–907, 2013.

[13] M. Schweizer, I. Lizama, T. Friedli, and J. W. Kolar, “Comparison of the chip area usage

of 2-level and 3-level voltage source converter topologies," in IECON 2010-36th Annual Conference on IEEE Industrial Electronics Society. IEEE, 2010, pp. 391–396.

[14] M. Schweizer and J. W. Kolar, "High efficiency drive system with 3-level t-type inverter," in Proceedings of the 2011 14th European Conference on Power Electronics and Applications. IEEE, 2011, pp. 1–10.

[15] J. A. Anderson, E. J. Hanak, L. Schrittwieser, M. Guacci, J. W. Kolar,and G. Deboy, "All-silicon 99.35% efficient three-phase seven-level hybrid neutral point clamped/flying capacitor inverter,"CPSS Transactions on Power Electronics and Applications, vol. 4, no. 1, pp. 50–61, 2019.

[16] X. Yi, R. Sanchez, K. Haran, J. Veres, A. T. Perry, and P. J. Ansell,"Self-pumped air-cooling design for a high-speed high-specific-power motor," in2018 IEEE Transportation Electrification Conference and Expo (ITEC). IEEE, 2018, pp. 274–279.

[17] X. Yi, A. Yoon, and K. S. Haran, "Multi-physics optimization for high-frequency air-core permanent-magnet motor of aircraft application,"in Electric Machines and Drives Conference (IEMDC), 2017 IEEE International. IEEE, 2017, pp. 1–8.

[18] A. Yoon, X. Yi, J. Martin, Y. Chen, and K. Haran, "A high-speed, high-frequency, air-core pm machine for aircraft application," in2016 IEEE Power and Energy Conference at Illinois (PECI), Feb 2016, pp. 1–4.

[19] E. Serban, C. Pondiche, and M. Ordonez, "Power-loss analysis in 3-level tnpc inverters: Modulation effects," in2017 IEEE Energy Conversion Congress and Exposition (ECCE). IEEE, 2017, pp. 490–497.

[20] H. Peng, Z. Yuan, B. Narayanasamy, X. Zhao, A. Deshpande, andF. Luo, "Comprehensive analysis of three-phase three-level t-type neutral-point-clamped inverter with hybrid switch combination," in2019 IEEE 10th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), June 2019, pp. 816–821..

[21] R.Whitt,B.Nafis,D.Huitink,Z.Yuan,A.Deshpande,B. Narayanasamy, and F. Luo, "Heat transfer and pressure drop performance of additively manufactured polymer heat spreaders for low-weight directed cooling integration in power electronics," in201918th IEEE Inter society Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm), May 2019, pp. 451–455.

[22] J. Hu, O. Alatise, J. A. O. Gonz alez, R. Bonyadi, L. Ran, andP. A. Mawby, "The effect of electrothermal no nuniformities on paralell lconnected sic power devices under unclamped and clamped inductive switching,"IEEE Transactions on Power Electronics, vol. 31, no. 6, pp.4526–4535, 2016.

[23] T. Lopez and R. Elferich, "Static paralleling of power mosfets in thermal equilibrium," in Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, 2006. APEC'06.IEEE, 2006, pp. 7–pp.

[24] M. Tencer, J. S. Moss, and T. Zapach, “Arrhenius average temperature:the effective temperature for non-fatigue wearout and long term reliability in variable thermal conditions and climates,”IEEE transactions on components and packaging technologies, vol. 27, no. 3, pp. 602–607,2004.

[25] Z. Chen, “Electrical integration of sic power devices for high-power-density applications,” Ph.D. dissertation, Virginia Tech, 2013.

[26] Y. Mao, “Passive balancing of switching transients between paralleled sic mosfets,” Ph.D. dissertation, Virginia Tech, 2018.

[27] G. Wang, J. Mookken, J. Rice, and M. Schupbach, “Dynamic and static behavior of packaged silicon carbide mosfets in paralleled applications,”in2014 IEEE Applied Power Electronics Conference and Exposition-APEC 2014. IEEE, 2014, pp. 1478–1483.

[28] S. Bontemps and C. de Magret, “Parallel connection of igbt and mosfet power modules.”Application notes APT0405, Advanced Power Technology Europe, France, 2004.

[29] J. Ke, H. Huang, P. Sun, J. Abuogo, Z. Zhao, and X. Cui, “Influence of parasitic capacitances on transient current distribution of paralleled sic mosfets,” in2018 1st Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia). IEEE, 2018, pp. 1–6.

[30] J. J. Nelson, G. Venkataramanan, and B. C. Beihoff, “Investigation of parallel operation of igbts,” in Conference Record of the 2002 IEEE Industry Applications Conference. 37th IAS Annual Meeting (Cat. No.02CH37344), vol. 4. IEEE, 2002, pp. 2585–2591.

[31] M. Sasaki, H. Nishio, and W. T. Ng, “Dynamic gate resistance control for current balancing in parallel connected igbts,” in2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition(APEC). IEEE, 2013, pp. 244–249.

[32] R. Alvarez and S. Bernet, “A new delay time compensation principle for parallel connected igbts,” in2011 IEEE Energy Conversion Congress and Exposition, Sep. 2011, pp. 3000–3007. all other references

[33] Y. Xue, J. Lu, Z. Wang, L. M. Tolbert, B. J. Blalock, and F. Wang, “Active current balancing for parallel-connected silicon carbide mosfets,” in2013 IEEE Energy Conversion Congress and Exposition, Sep. 2013, pp.1563–1569.

[34] D. Bortis, J. Biela, and J. W. Kolar, “Active gate control for current balancing of parallel-connected igbt modules in solid-state modulators,”IEEE Transactions on Plasma Science, vol. 36, no. 5, pp. 2632–2637,Oct 2008.

[35] J. Lu, H. Bai, A. Brown, M. McAmmond, D. Chen, and J. Styles,“Design consideration of gate driver circuits and pcb parasitic parameters of paralleled e-mode gan hemts in zero-voltage-switching applications,”in2016 IEEE Applied Power Electronics Conference and Exposition(APEC), March 2016, pp. 529–535.

[36] Q. Haihong, Z. Ying, Z. Ziyue, W. Dan, F. Dafeng, W. Shishan, and Z. Chaohui, “Influences

of circuit mismatch on paralleling silicon car-bide mosfets," in 2017 12th IEEE Conference on Industrial Electronics and Applications (ICIEA), June 2017, pp. 556–561

[37] H. Li, S. Munk-Nielsen, X. Wang, S. Beczkowski, S. R. Jones, andX. Dai, "Effects of auxiliary-source connections in multichip power module,"IEEE Transactions on Power Electronics, vol. 32, no. 10, pp.7816–7823, Oct 2017.

[38] J. L. Lu and D. Chen, "Paralleling gan e-hemts in 10kw–100kw systems," in2017 IEEE Applied Power Electronics Conference and Exposition (APEC), March 2017, pp. 3049–3056.

[39] J. Lu, H. Bai, A. Brown, M. McAmmond, D. Chen, and J. Styles,"Design consideration of gate driver circuits and pcb parasitic parameters of paralleled e-mode gan hemts in zero-voltage-switching applications,"in2016 IEEE Applied Power Electronics Conference and Exposition(APEC). IEEE, 2016, pp. 529–535.

[40] Fachartikel, "Design kompakter 250-kw-dreiphasen-wechselrichter mitsic-mosfets," 2017, [Online; accessed 21-January-2019]. [Online].Available: https://www.all-electronics.de/250-kw-wechselrichter-mit-sic-mosfets/3/

[41] C. Chen, X. Pei, Y. Chen, and Y. Kang, "Investigation, evaluation, andoptimization of stray inductance in laminated busbar,"IEEE Transac-tions on Power Electronics, vol. 29, no. 7, pp. 3679–3693, July 2014.

[42] A. D. Callegaro, J. Guo, M. Eull, B. Danen, J. Gibson, M. Preindl,B. Bilgin, and A. Emadi, "Bus bar design for high-power inverters,"IEEE Transactions on Power Electronics, vol. 33, no. 3, pp. 2354–2367,March 2018.

[43] Mersen, "Design guide formulas," [Online; accessed 6-April-2019].[Online]. Available: https://www.busbar.com/resources/formulas/

[44] B. Aberg, R. S. K. Moorthy, L. Yang, W. Yu, and I. Husain, "Estimation and minimization of power loop inductance in 135 kw sic traction inverter," in2018 IEEE Applied Power Electronics Conference and Exposition (APEC), March 2018, pp. 1772–1777.

[45] N. R. Mehrabadi, I. Cvetkovic, J. Wang, R. Burgos, and D. Boroyevich,"Busbar design for sic-based h-bridge pebb using 1.7 kv, 400 a sicmosfets operating at 100 khz," in2016 IEEE Energy ConversionCongress and Exposition (ECCE). IEEE, 2016, pp. 1–7.

[46] J. Wang, B. Yang, J. Zhao, Y. Deng, X. He, and X. Zhixin, "Development of a compact 750 kva three-phase npc three-level universal inverter module with specifically designed busbar," in2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC),Feb 2010, pp. 1266–1271.

[47] Y. Jiao, S. Lu, and F. C. Lee, "Switching performance optimization of a high power high frequency three-level active neutral point clamped phase leg,"IEEE Transactions on power electronics, vol. 29, no. 7, pp.3255–3266, 2013.

[48] Q. Wang, T. Chang, F. Li, K. Su, and L. Zhang, "Switching transientanalysis and design of

a low inductive laminated bus bar for a t-typeconverter,"Journal of Power Electronics, vol. 16, no. 4, pp. 1256–1267,2016.[49] A. Deshpande and F. Luo, "Multilayer busbar design for a si igbt andsic mosfet hybrid switch based 100 kw three-level t-type pebb," in2017IEEE 5th Workshop on Wide Bandgap Power Devices and Applications(WiPDA), Oct 2017, pp. 20–24.

[49] A. Deshpande and F. Luo, "Multilayer busbar design for a si igbt and sic mosfet hybrid switch based 100 kw three-level t-type pebb," in2017IEEE 5th Workshop on Wide Bandgap Power Devices and Applications(WiPDA), Oct 2017, pp. 20–24.

[50] Z. Sun, J. Chen, T. Xu, L. Liu, and J. Kuang, "Current equalizingbusbar," Jun. 2 2015, uS Patent 9,048,722.

[51] C. Chen, X. Pei, Y. Shi, X. Lin, X. Liu, and Y. Kang, "Modeling and optimization of high power inverter three-layer laminated busbar," in2012 IEEE Energy Conversion Congress and Exposition (ECCE). IEEE,2012, pp. 1380–1385.

[52] C. Chen, Z. Huang, L. Chen, Y. Tan, Y. Kang, and F. Luo, "A flexible pcb based 3d integrated sic half-bridge power module with three-sided cooling using ultra-low inductive hybrid packaging structure,"IEEE Transactions on Power Electronics, 2018.

[53] C. Chen, Y. Chen, Y. Li, Z. Huang, T. Liu, and Y. Kang, "An sic-based half-bridge module with an improved hybrid packaging method for high power density applications,"IEEE Transactions on Industrial Electronics, vol. 64, no. 11, pp. 8980–8991, 2017.

[54] Z. Lounis, I. Rasoanarivo, and B. Davat, "Minimization of wiring inductance in high power igbt inverter,"IEEE Transactions on Power Delivery, vol. 15, no. 2, pp. 551–555, April 2000.

[55] Shuo Wang, F. C. Lee, and W. G. Odendaal, "Characterization and parasitic extraction of emi filters using scattering parameters,"IEEE Transactions on Power Electronics, vol. 20, no. 2, pp. 502–510, March 2005.

[56] Microsemi, "Common-source power modules," [Online; accessed 13-May-2019]. [Online]. Available: https://www.microsemi.com/product-directory/mosfet-modules/5370-common-source

[57] X. Song, C. Peng, and A. Q. Huang, "A medium-voltage hybrid dc circuit breaker, part i: Solid-state main breaker based on 15 kv sic emitter turn-off thyristor,"IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 5, no. 1, pp. 278–288, March 2017.

[58] Z. W. et al., "A compact 250 kw silicon carbide mosfet based three-level traction inverter for heavy equipment applications," in2018 IEEE Transportation Electrification Conference and Expo (ITEC).

[59] Z. Wang, Z. Zhao, M. Hammad Uddin, and Y. Zhao, "Current ripple analysis and prediction for three-level t-type converters," in2018 IEEE Energy Conversion Congress and Exposition (ECCE), Sep. 2018, pp.7251–7257.

[60] Y. Ren, X. Yang, F. Zhang, L. Wang, K. Wang, W. Chen, X. Zeng, and Y. Pei, "Voltage suppression in wire-bond-based multi chip phase-leg sic mosfet module using adjacent decoupling concept,"IEEE Transactions on Industrial Electronics, vol. 64, no. 10, pp. 8235–8246, Oct 2017.

[61] F. E. Terman, "Radio engineers' handbook," 1943.

[62] D. William, "Advanced electronic packaging with emphasis on multichip modules," 1999.

[63] Z. Piatek, B. Baron, T. Szczegielniak, D. Kusiak, and A. Pasierbek,"Mutual inductance of two thin tapes with parallel widths,"Przeglad Elektrotechniczny, vol. 89, no. 4, pp. 281–283, 2013.

[64] C. Chen, X. Pei, Y. Chen, and Y. Kang, "Investigation, evaluation, and optimization of stray inductance in laminated busbar,"IEEE Transactions on power electronics, vol. 29, no. 7, pp. 3679–3693, 2014.

[65] C. Chen, F. Luo, and Y. Kang, "A review of sic power module packaging:Layout, material system and integration,"CPSS Transactions on Power Electronics and Applications, vol. 2, no. 3, pp. 170–186, Sep. 2017.

[66] A. H. Wijenayake, K. J. Olejniczak, D. Simco, S. Minden, M. Feurtado,B. Passmore, T. McNutt, A. Lostetter, and D. Martin, "Design of a250 kw, 1200 v sic mosfet-based three-phase inverter by considering a subsystem level design optimization approach," in2017 IEEE Energy Conversion Congress and Exposition (ECCE). IEEE, 2017, pp. 939–946.

4 Insulation-and-inductance Optimization for Busbar for MEA Applications

Some content of this chapter comes from an accepted paper of IEEE EATS 2020.

List of author's name, Yuan, Z., Wang, Y., Emon, A.I., Wang, Z., Narayanasamy, B., Deshpande, A., Peng, H. and Luo, F.

4.1 Abstract

This chapter proposes a partial-discharge (PD) free insulation design method of laminated busbar for converters in more-electric-aircraft (MEA) applications. During high altitude operation, the converters are exposed in decompressed air-pressure conditions, making PD being triggered easier. Contrariwise, insulation overdesign increases busbar stray inductance, causing higher voltage overshoots. The paper is to solve this issue by proposing an insulation design strategy. It starts with an insulation structure analysis and determines the worst-stress scenario by considering the defects. The minimum insulation thickness is derived by comparing the worst-stress E-field and PD inception field. The strategy also defines the higher limit of insulation caused by stray inductance, which is achieved by quantitively modeling the trade-off between insulation and inductance. After that, an insulation design space can be chosen in the range between lower and upper limits. The insulation of a busbar for a three-level 450 kVA converter is designed to validate the proposed strategy, which is demonstrated PD-free with 43% insulation margins. With the balanced inductance-and-insulation trade-off, the design minimizes the inductance to 12.0 nH, which is lower than published literature for 3L converters. Benefited from it, accelerated switching speed is achieved with switching loss reduction by 66.7% at 1 kV 350A.

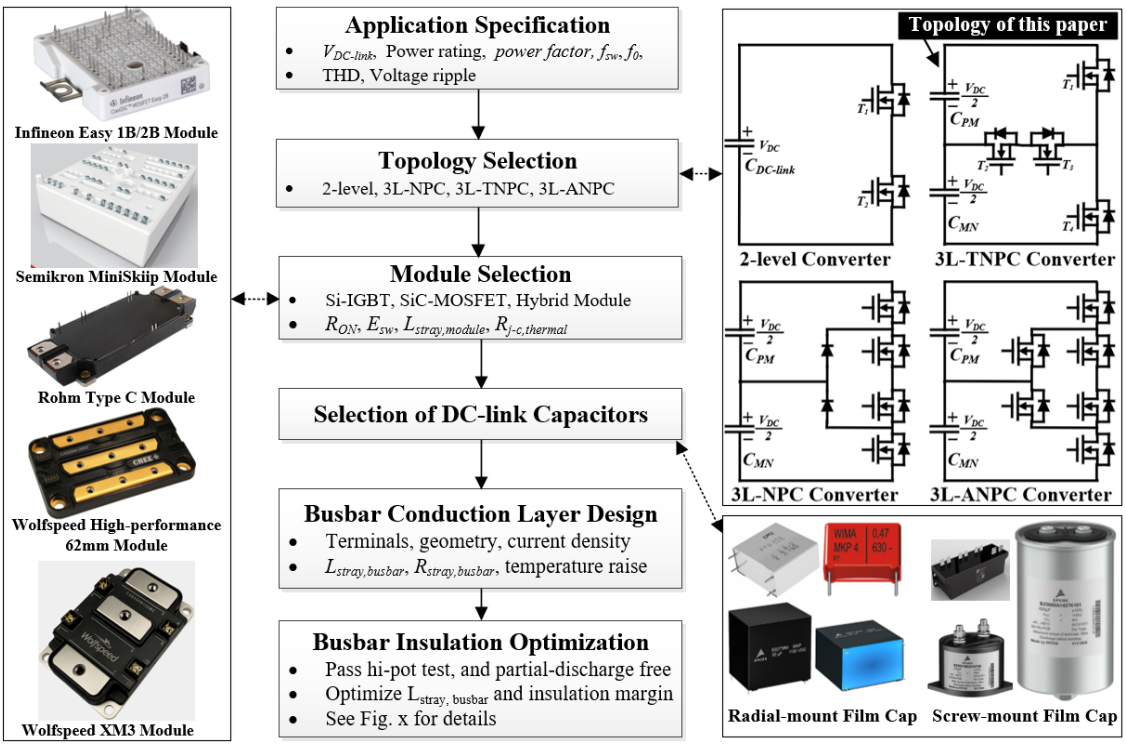

Fig. 4.1: A generalized converter design procedure

4.2 Introduction

More-electric aircraft (MEA) is an imposing concept as it relives fossil-fuel dependency, reduces carbon emissions, and improves overall system efficiency. Aligned with the concept, NASA proposed a roadmap, targeting a 5 megawatts MEA in ten years [1]. The concept requires power converters to be higher power rating, efficiency, power density, and reliability.

The laminated busbar is one of the critical components of a power converter in MEA applications. Compared to the printed circuit board (PCB), the busbar shows advantages in high-current applications as thicker copper preventing overheats. Copper layers of busbar are closely laminated and isolated by insulation papers sandwiched in between. The short distance between copper layers enhances magnetic cancellation, reducing stray inductance [2]. But it will also intensify the E-field distributed between cooper layers, challenging insulation design, which is known as

inductance-and-insulation trade-off.

Once the E-field around the busbar is higher than the partial-discharge inception field (E_{PDI}), partial discharge (PD) can be triggered, which is the primary reason causing insulation breakdown by accelerating insulation aging [3]. Nevertheless, a PD-free insulation system is one of the major challenges in MEA applications. The first reason is that the high power rating of MEA converters pushes its DC-link voltage higher to limit the current, with the cost of raised E-field on the busbar [4-6].

But more challenges come from the nature of the high-altitude operation. For example, the air pressure at 11 km altitude is only 0.2 atm. Consequently, its PD inception voltage (PDIV) is decreased by 40% according to experiments conducted by [7,8].

Significant works are done in achieving PD-free design by improving the insulation of power modules [9,10] and motors [11,12]. In 2013, the first paper conducting PD research on busbar was presented in [13], reporting the characteristic of PD behaviors on busbar, such as discharge amplitude, time, and spectrum of PD-induced noises. In 2018, papers [14,15] proposed a finite-element-analysis (FEA) based method to predict PDIV for a given busbar. The air-insulation-copper triple point was found causing PD because of the highly-crowded E-field. The following paper in 2019 [16] demonstrated the FEA-based PDIV prediction method by using standardized PD measurement procedures, IEC60270, and IEC60851-5. The influence of busbar defects, such as voids and delamination, were discussed in [17,18], showing that those defects can worse the E-field distortion, further facilitating PD.

The PD-free insulation design of the laminated busbar was discussed in [19]. It focused on reducing E-field magnitude on the triple point through manufacturing, including the refraction layer and encapsulation. Paper [20] designed an insulation system of a laminated busbar for a

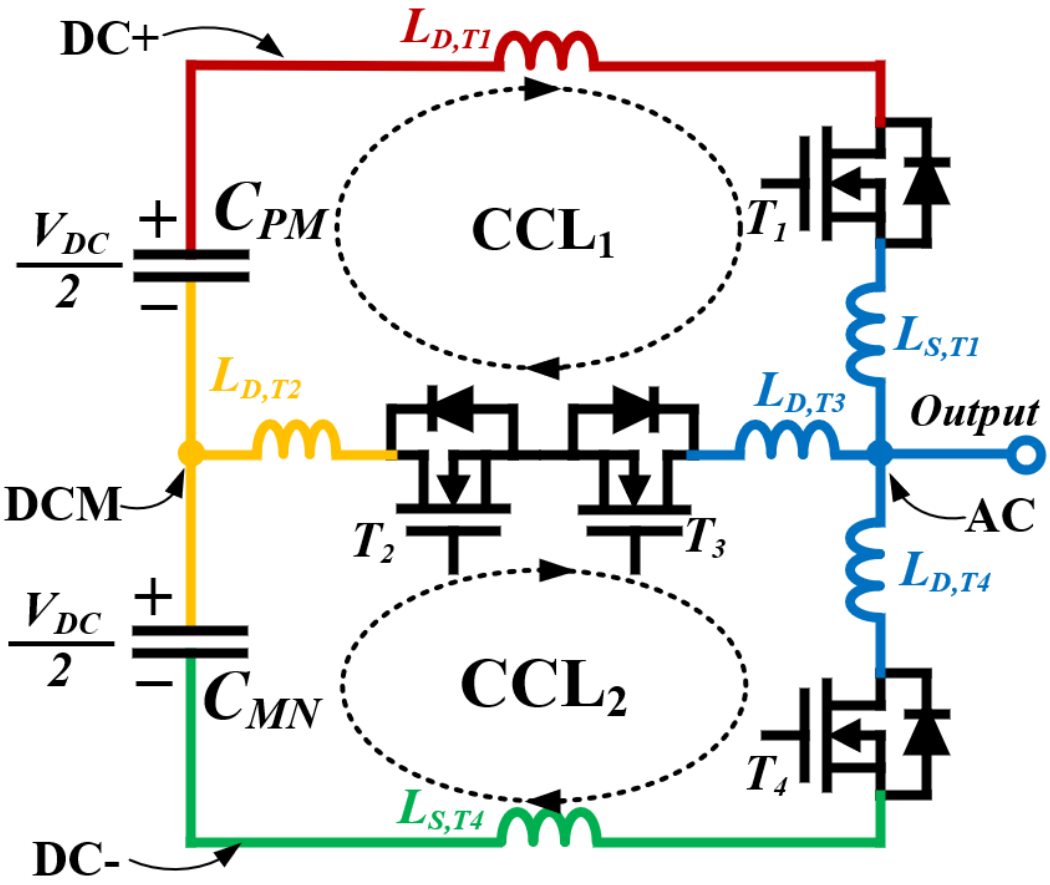

Fig. 4.2: Stray inductance distribution in a 3L-TNPC

medium-voltage converter. It discussed considerations for material selection, such as volume resistivity and dielectric constant. The processing to remove voids is suggested as well. However, entirely getting rid of defects in a busbar is impractical, especially after long-term running. Moreover, none of the papers explicitly explained how to choose a proper thickness of the insulation paper. Moreover, not a paper discussed the insulation design under the decompressed condition, which is more challenging than the design in normal conditions.

This paper is to solve the aforementioned challenges in insulation design. The contribution of the paper is summarized as the following;

(i). The paper proposes a generalized insulation design diagram, which determines the worst-stress scenario by classifying the insulation into different patterns and analyzing their E-

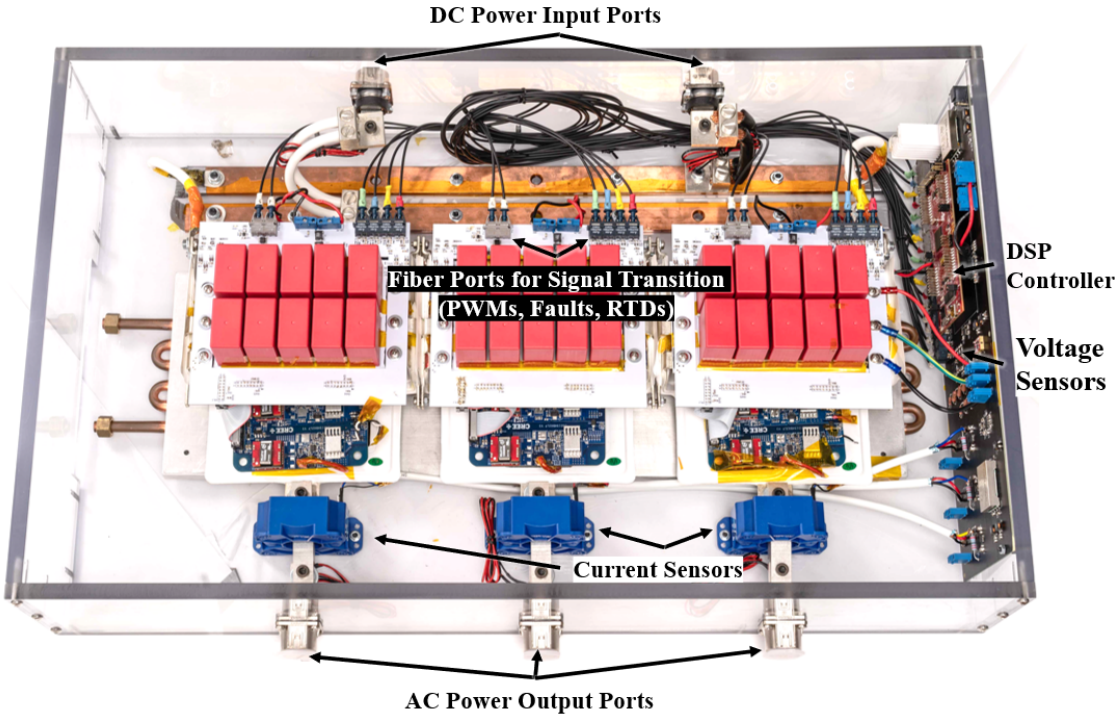

Fig. 4.3: Fabricated three-phase 450-kVA 3L-TNPC motor drive

field under both defects and non-defects conditions. Through combing the worst-stress scenario and low-air-pressure impacts, the design can guide to the minimum thickness of the insulation layer to achieve PD free.

(ii). The trade-off between insulation margin and busbar stray inductance is explicitly explained and quantitatively modeled. It helps designers choose the insulation in the range of lower limit (min. thickness to achieve PD free) and the higher limit (acceptable stray inductance due to voltage overshoots).

(iii). The paper provided a busbar design example for a 450 kVA three-level (3L) motor drive. Tests are performed to demonstrate PD-free insulation with additional 43% margins at 0.2 atm. Its inductance is also lower than the published design of 3L converters, enabling accelerated switching speed and switching loss reduction of 66.7% at 1kV, 350A.

The paper is constructed as the following. Chapter II introduces the baseline version of the

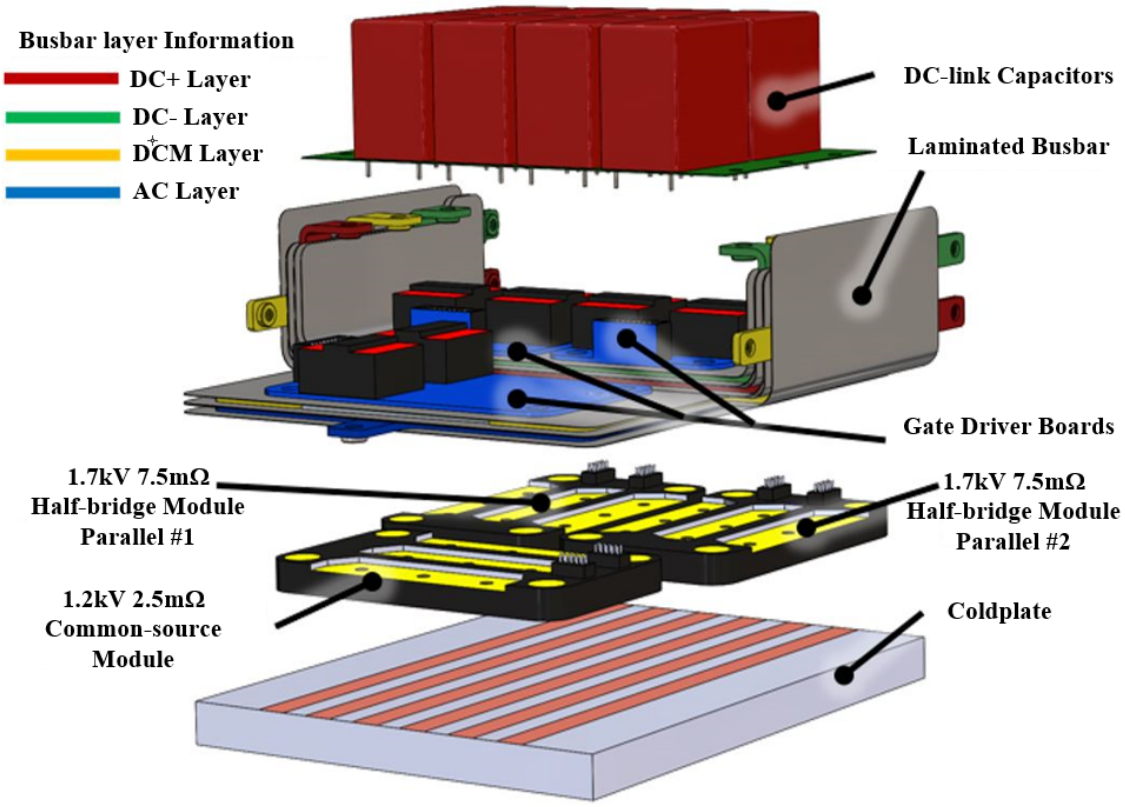

Fig. 4.4: Exploded view for one phase of the 450-kVA converter

busbar for 450kVA 3L converters. The insulation design method is discussed in chapter III. The optimization for inductance-and-insulation trade-off is provided in part IV. The proposed method is evaluated by experiments in Chapter V. The conclusion is summarized at the end of the paper.

4.3 Laminated Busbar for 450 KVA Motor Drive

Prior to insulation design and optimization, the function and structure of busbar are explained through converter introduction.

4.3.1 Busbar overview

Fig. 4.1 provides an overall converter design procedure. The design starts with selection of the optimal topology. For a specific application, the optimal topology can be derived based on

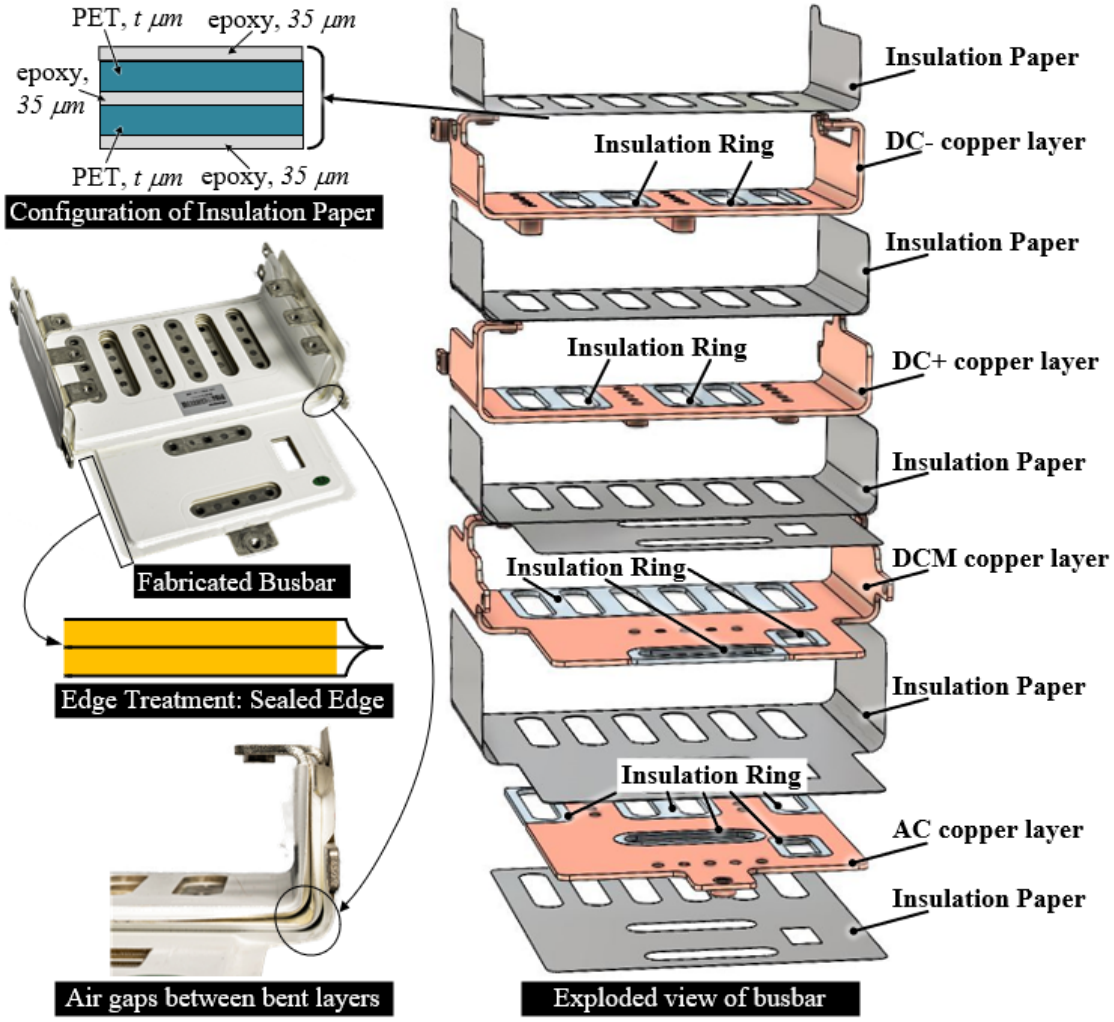

Fig. 4.5: The structure of laminated busbar for 450-kVA converter, and its configuration of insulation system.

semiconductor loss models [21,22]. The popular motor-drive topologies are included in Fig.4.1. Their advantages are compared in [23]. This paper uses 3L-TNPC, as Fig. 4.2 because of higher efficiency at DC-link voltage of 1 kV and switching frequency over 10 kHz.

The performance of a module is evaluated from both the electrical and thermal aspects. In summary, at the same voltage rating, parameters are preferred as low as possible, such as on-state resistance, switching loss, stray inductance, and junction-to-case thermal resistance [24]. This design utilizes Wolfspeed High-Performance 62mm SiC-MOSFET power modules because of the

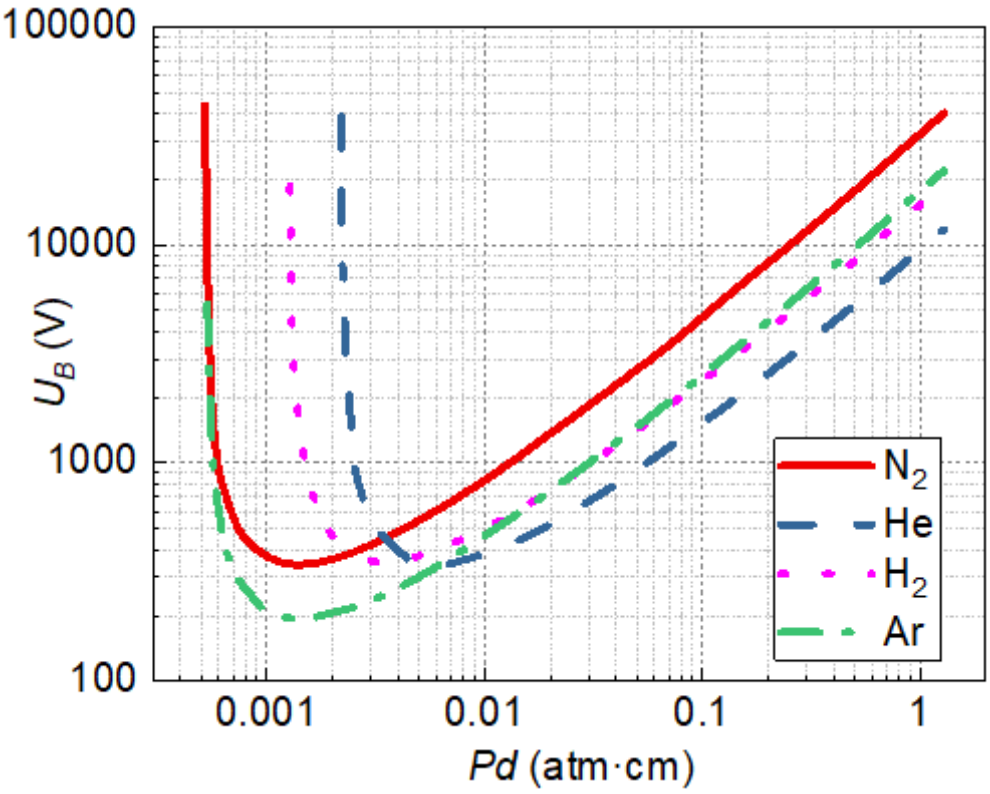

Fig. 4.6: Paschen curve of various gas types.

overall higher performance.

Busbar design is the next step after decisions on topology, power modules, and capacitors. Conduction-layer design is performed firstly, as it primarily affects the overall performance. The conduction layer should offer sufficient current capability [25]. The proper layout of the busbar is essential to limit its stray inductance and achieve equalized inductance distribution between parallel power modules.

Insulation optimization is performed at the last step; however, it greatly influences busbar functionality, reliability, and parasitic. It should help the busbar pass hi-pot test and guarantee PD-free at operational voltage and altitude. Moreover, insulation optimization is necessary to orient the optimal design space under the inductance-and-insulation trade-off.

The three-phase 450 kVA motor drive is designed and fabricated as Fig. 4.3 To better

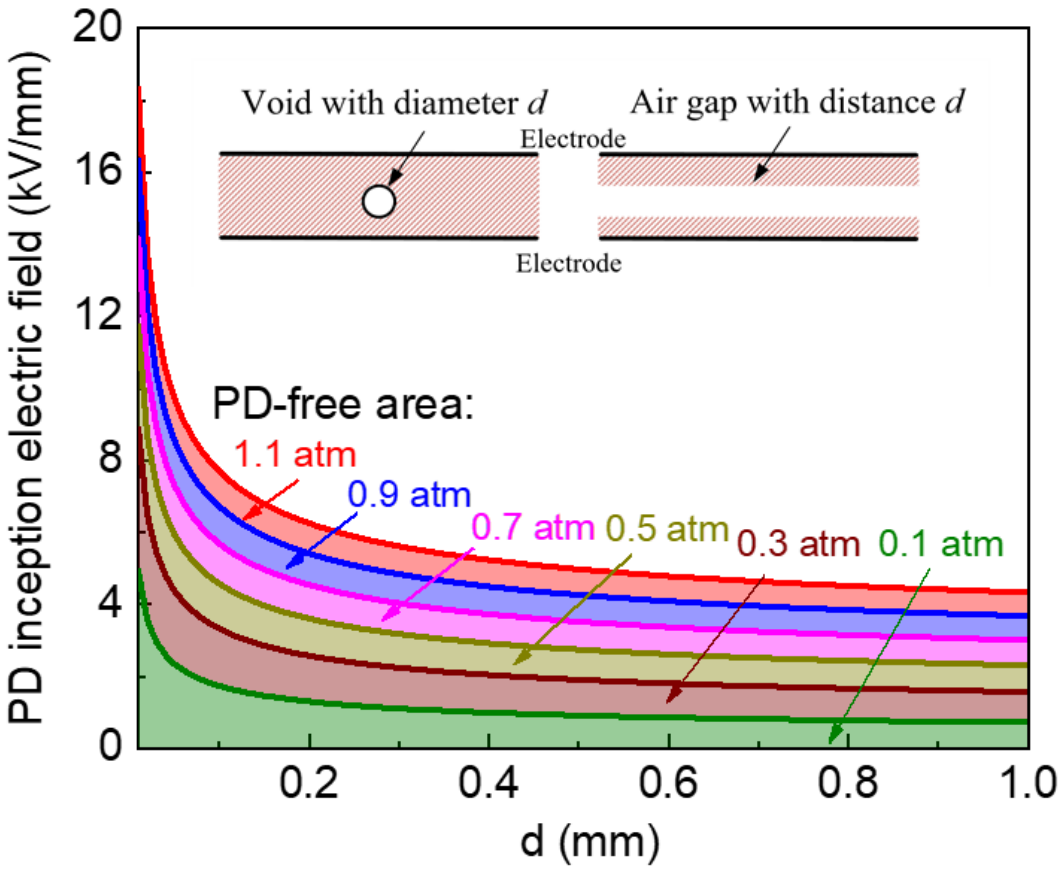

Fig. 4.7: PD inception field curves with air pressures and distances.

explain the structure of the three-phase converter, an exploded view of the one-phase is shown in Fig. 4.4. It is seen that each phase is configured by two parallel 1.7 kV 7.5 mΩ SiC-MOSFET power modules for T_1 and T_4 (see Fig. 2 for positions of T_1 and T_4); and one 1.2 kV, 2.5mΩ SiC-MOSFET module for T_2 and T_3. Busbar connects to three power modules and capacitors to form the topology. It also provides mechanical supports for gate drivers. Liquid coldplate is attached to the bottom of the power module for heat dissipation.

4.3.2 Baseline version of insulation structure

Busbar design should minimize stray inductance in each current commutation loop (CCL). Based on [26, 27], the two CCLs are noted in Fig. 4.2. And the total inductance of each CCL is

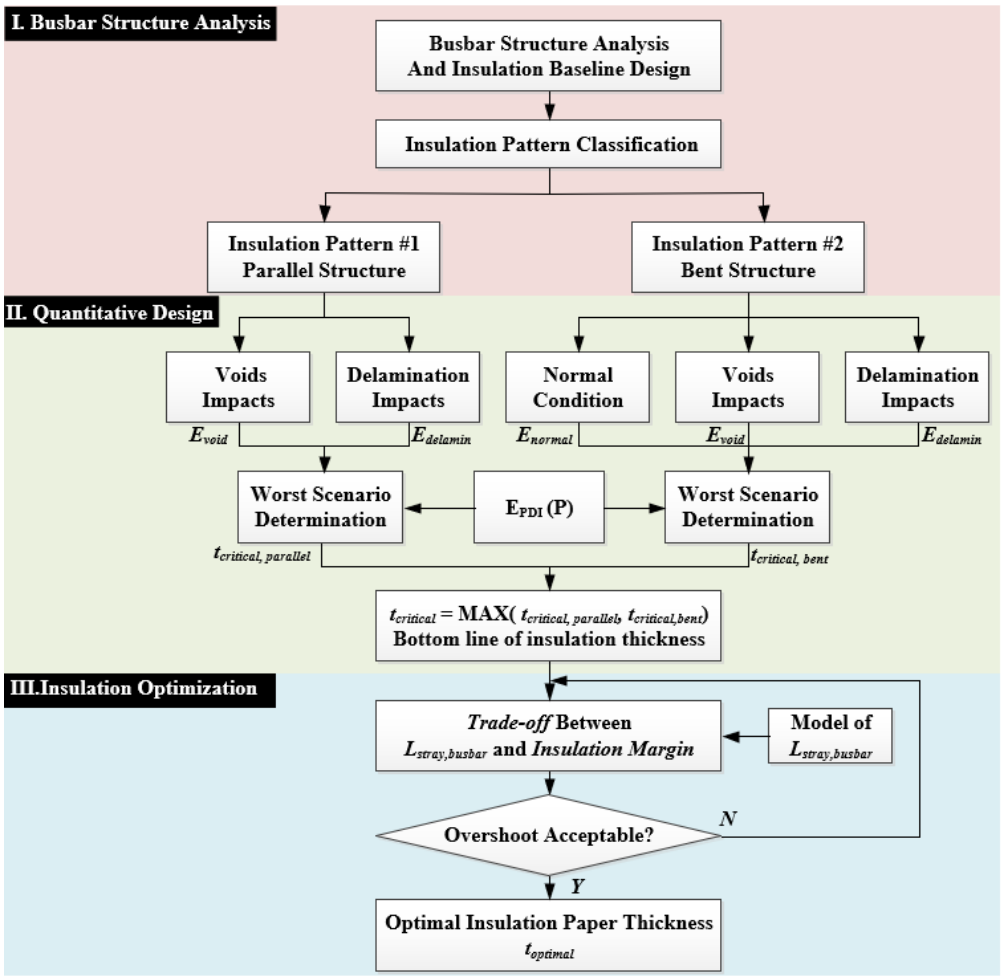

Fig. 4.8: Proposed insulation design method.

summarized as Eq. 4.1 and Eq. 4.2 .

$$L_{CCL1,\text{total}} = L_{D,T1} + L_{S,T1} + L_{D,T3} + L_{D,T2} \tag{4.1}$$

$$L_{CCL2,total} = L_{D,T4} + L_{S,T4} + L_{D,T3} + L_{D,T2} \tag{4.2}$$

The conduction layers of the busbar are designed as a double-side decoupling structure. It means that busbar connects to the DC-link capacitor board from both sides, as Fig. 4.4. The structure can decouple the stray inductance effectively. Besides, as the two parallel modules share

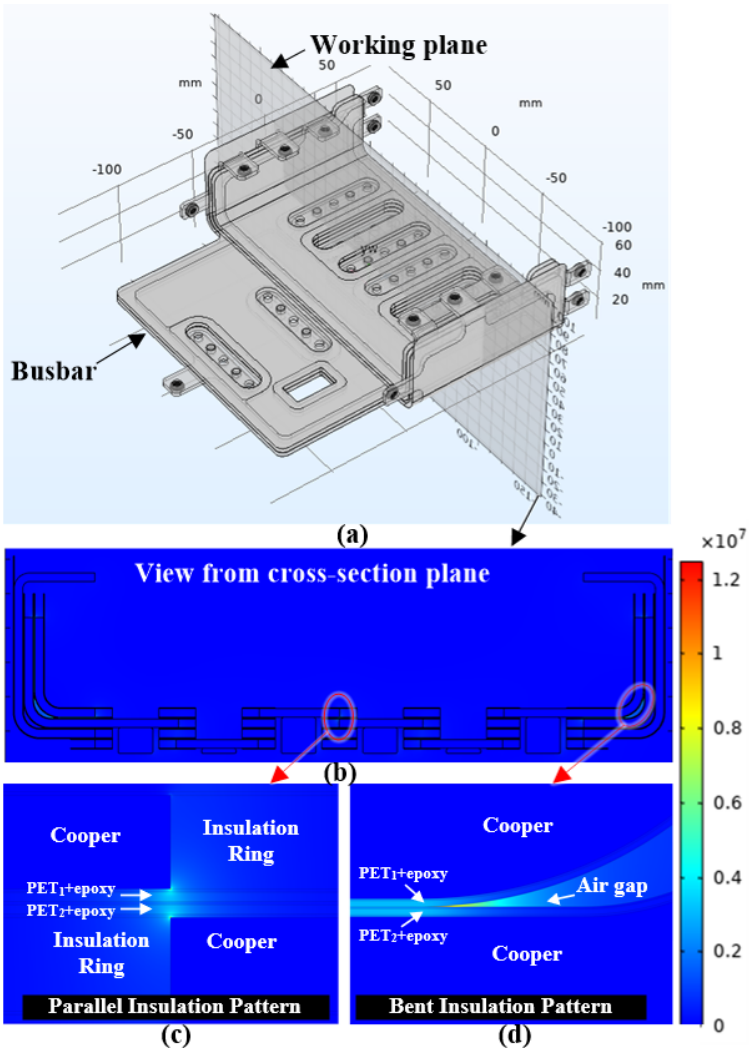

Fig. 4.9: E-field map in COMSOL. (a) 3D model of busbar; (b) cross-sectional view from working plane; (c) zoom-in view, parallel-insulation structure; (d) zoom-in view, bent insulation structure.

the same vertical distance to the DC-link capacitor board, the values of stray inductance seen by each module are equalized, which improves dynamic current sharing. The design of the conduction layer has been thoroughly studied in [28], which is not the primary topic of this paper. Exploded view of the busbar is as Fig. 4.5. Four copper layers are used to form the 3L-TNPC topology, and they present the four voltage potentials of 3L-TNPC in Fig. 2, which are DC+, DC-, DCM, and AC, respectively. The insulation system should enable the closed lamination of the four conduction layers while preventing PD and insulation breakdown. The baseline insulation system is configured

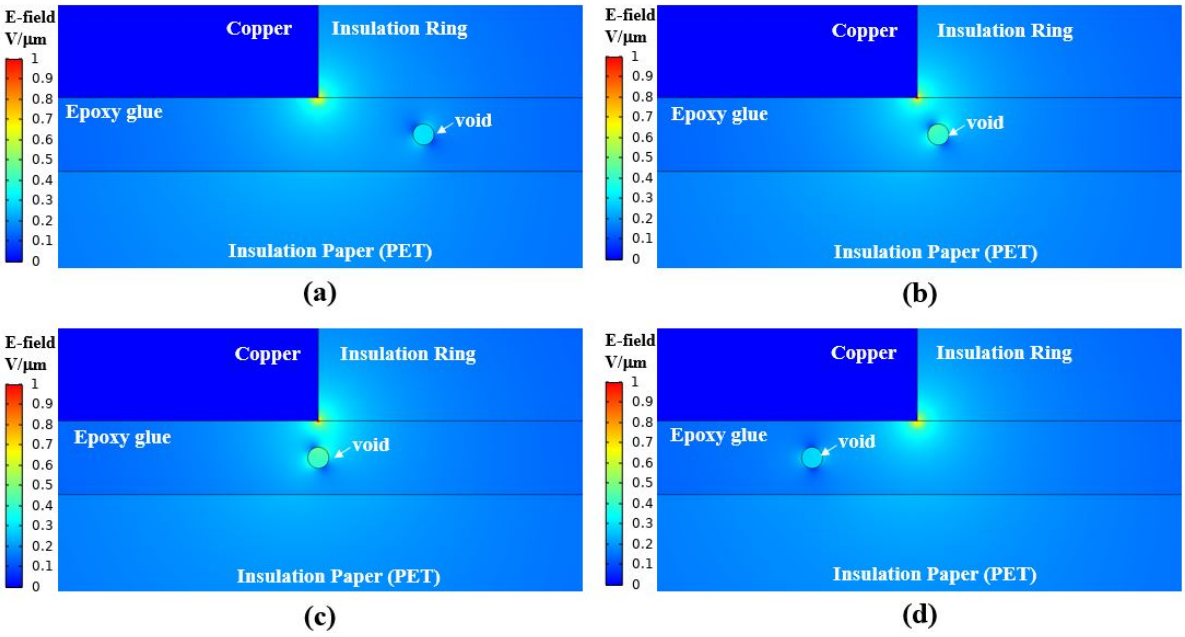

Fig. 4.10: E-field distribution for parallel insulation structure with voids, when the void is moving from right to left with vertical location a constant. The diameter of void is 10 μm. (a)-(d): void-to-center distance is 50 μm, 10 μm, 0 μm, and -50 μm, respectively.

as the following,

(i) As Fig. 4.5, insulation papers are sandwiched between copper layers. Each insulation paper is constructed by two layers of polyethylene terephthalate (PET) and three 35 μm epoxy-glue layers. PET is used for insulation because of high dielectric strength (300 V/μm at 25μm thickness), strong mechanical strength and wide temperature range. The epoxy-glue layers are used to firmly attach both PET and cooper. The PET-layer thickness is the variable to be fine-tuned to achieve PD-free while keep stray inductance low.

(b) Insulation rings are sticked to each of the copper layers. It allows spacers from other copper layers passing through it without insulation breakdown. It also fills the air gap between insulation layers to prevent contamination and pollutions.

(c) The insulation layers are pinched closed and sealed on itself at the external edge of the busbar. This is performed to prevent the pollution, small particles and waters entering the busbar,

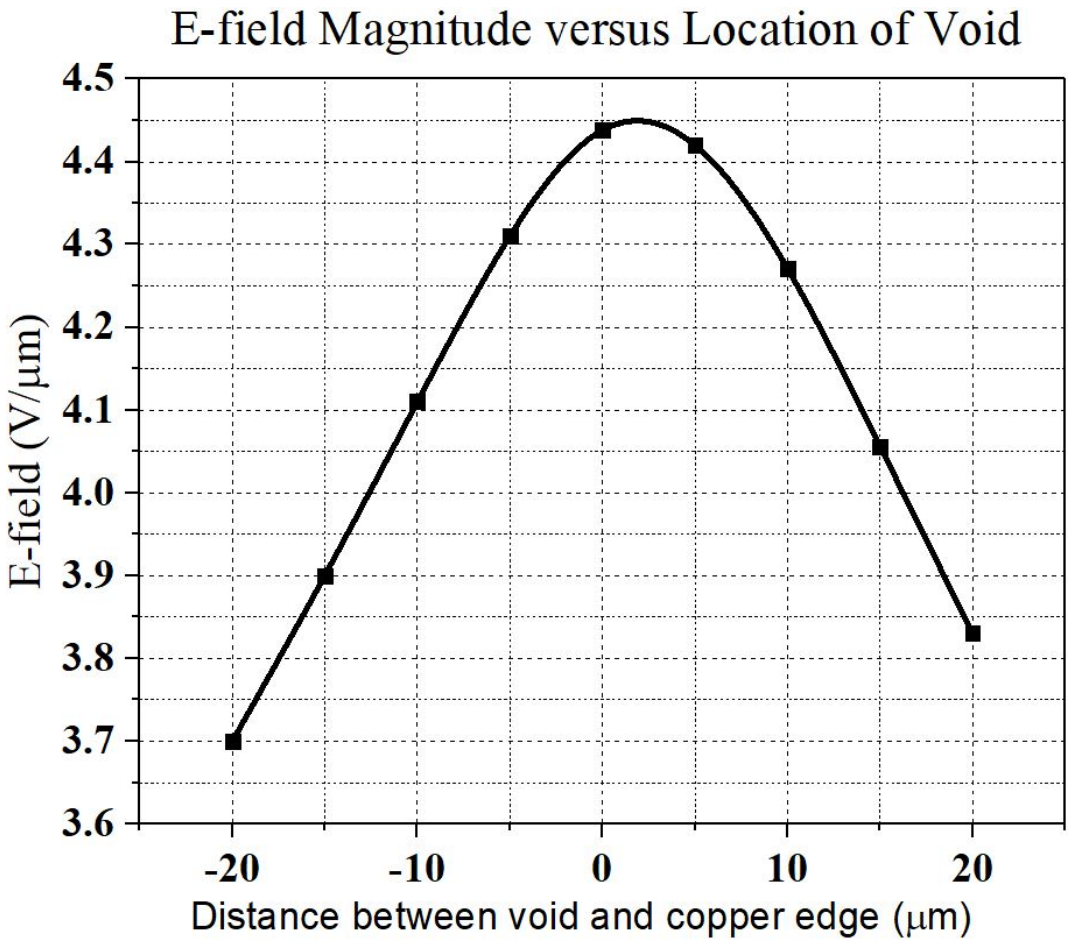

Fig. 4.11: Peak magnitude of E-field in void when the void is at different horizontal locations, with the vertical location a constant.

which may decrease the insulation thickness.

Air gaps at the bending corner of the busbar are noted in Fig. 4.5. Such airgaps are inevitable as the curving radius of copper cannot be precisely controlled during processing, possible voids between layers and possible delamination after long-time operation or difference in coefficient of thermal expansion (CTE). Nevertheless, airgaps are one of the roots causing PD in the bent structure. As it will be shown in the later part, even though the busbar has large bent radius (4.5*mm*,)significant amount of E-field are concentrated in the air gap in the bent area. When the air-gap E-field is larger than E_{PDI}, PD can happen.

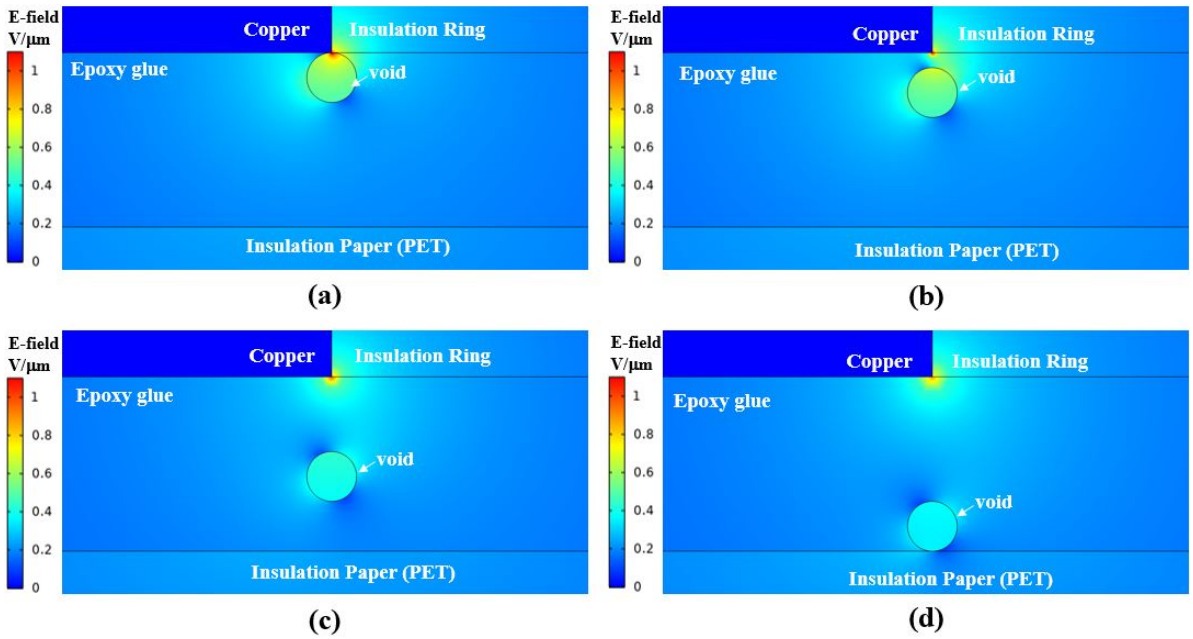

Fig. 4.12: E-field distribution for parallel insulation structure with voids, when the void is moving from top to bottom. The diameter of void is 10 μm. (a)-(d): void-center-to-top-epoxy distance is 5 μm, 8 μm, 20 μm, and 30 μm, respectively.

4.4 Insulation Design with PD-free at Low-pressure Condition

4.4.1 Effects of air pressure on PDIV and PD-Free criterion

PDIV is defined as the applied voltage at which repetitive partial discharges are first observed in the test object when the voltage applied to the object is gradually increased from a lower value at which no PD is observed [11]. Usually, PD occurs at the position of electric field concentration, such as the void in the sample and the interface between solid insulation and air [7]. Therefore, most of the PD actually is the breakdown of air. In terms of PDs in air, the PDIV is related to the air pressure and the way how the electric field is distributed. The most widely acknowledged law regarding PDIV of air in a uniformly distributed electric field is the Paschen's curve. It is found that the breakdown voltage between two electrodes in a gas as a function of pressure and gap length can be expressed by [29]:

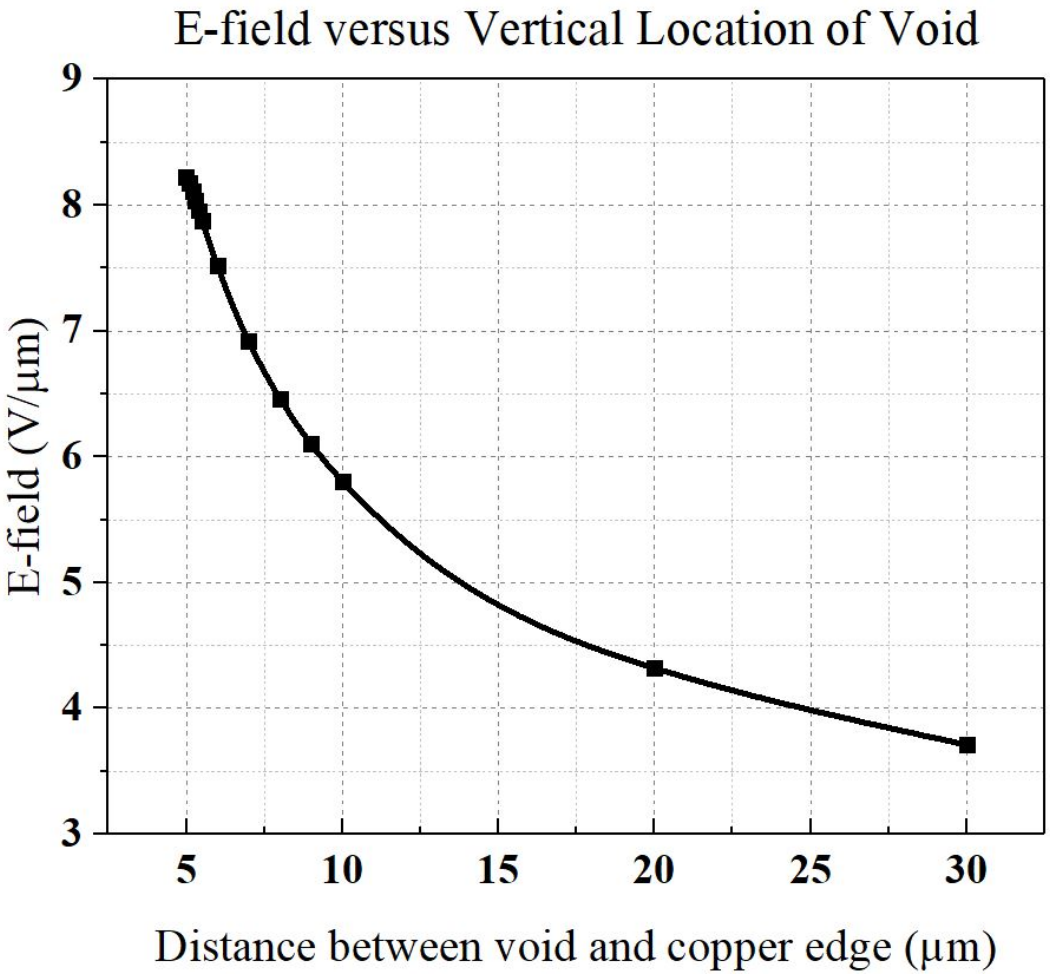

Fig. 4.13: Peak magnitude of E-field in void when the void is at different vertical locations, with the horizontal location a constant.

$$U_B = \frac{BPd}{\ln(APd) - \ln\left[\ln\left(1 + \frac{1}{\gamma_{se}}\right)\right]} \tag{4.3}$$

where U_B is the breakdown voltage in volts, P is the pressure, d is the gap distance, γ_{se} is the secondary-electron-emission coefficient (the number of secondary electrons produced per incident positive ion), A is the saturation ionization in the gas at a particular electric field/pressure, and B is related to the excitation and ionization energies. The Paschen curve is a U-shaped curve with a minimum and is shown in Fig. 4.6. Generally, Pd value in this study is on the right part of

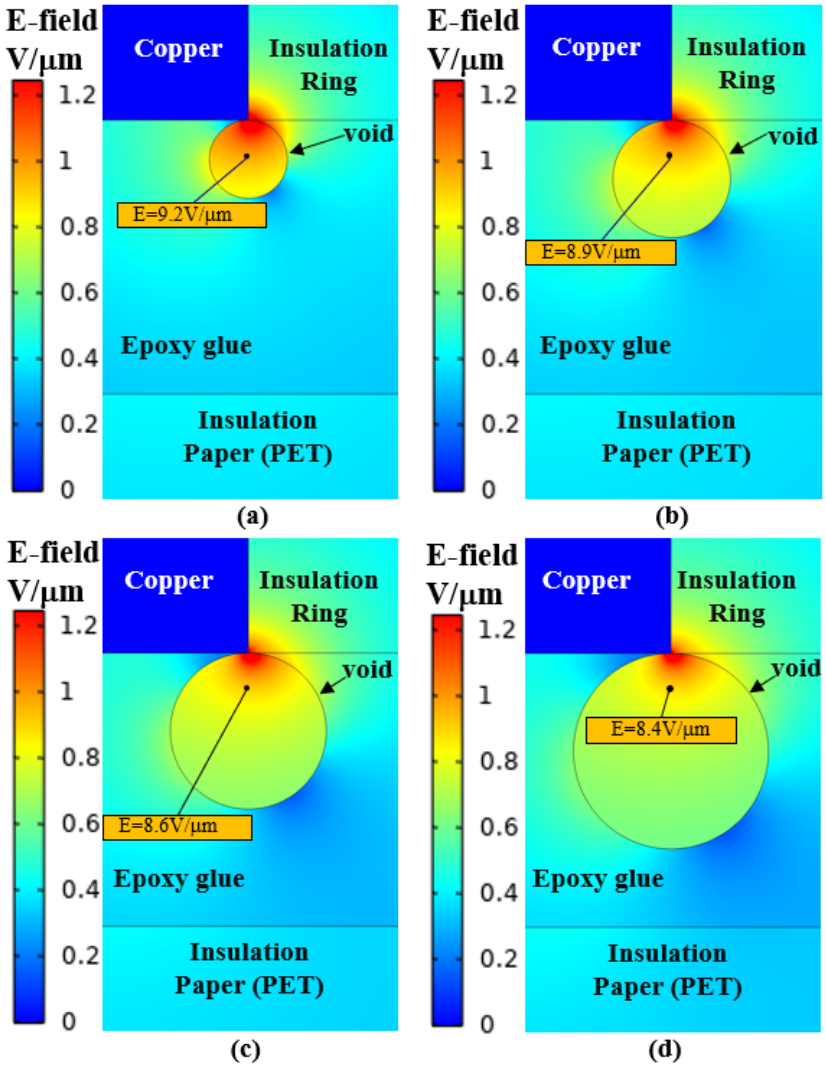

Fig. 4.14: E-field distribution for parallel insulation structure with voids. (a)-(d) keep PET-layer thickness (t_{PET}) constant as 100 μm, and change diameter of void (d_{void}) as 10 μ m, 15 μm, 20 μm, 25 μm, and 35 μm respectively.

the Paschen curve.

However, Paschen's curve is obtained from experimental results in the uniformly distributed electric field, which is not always the situation in practice. Researchers investigated the physics of breakdown in air and derived the PD inception field for air breakdown at various pressure conditions, which means that the PD inception is not determined by the voltage applied across the insulation but determined by the local electric field and the environmental conditions at the

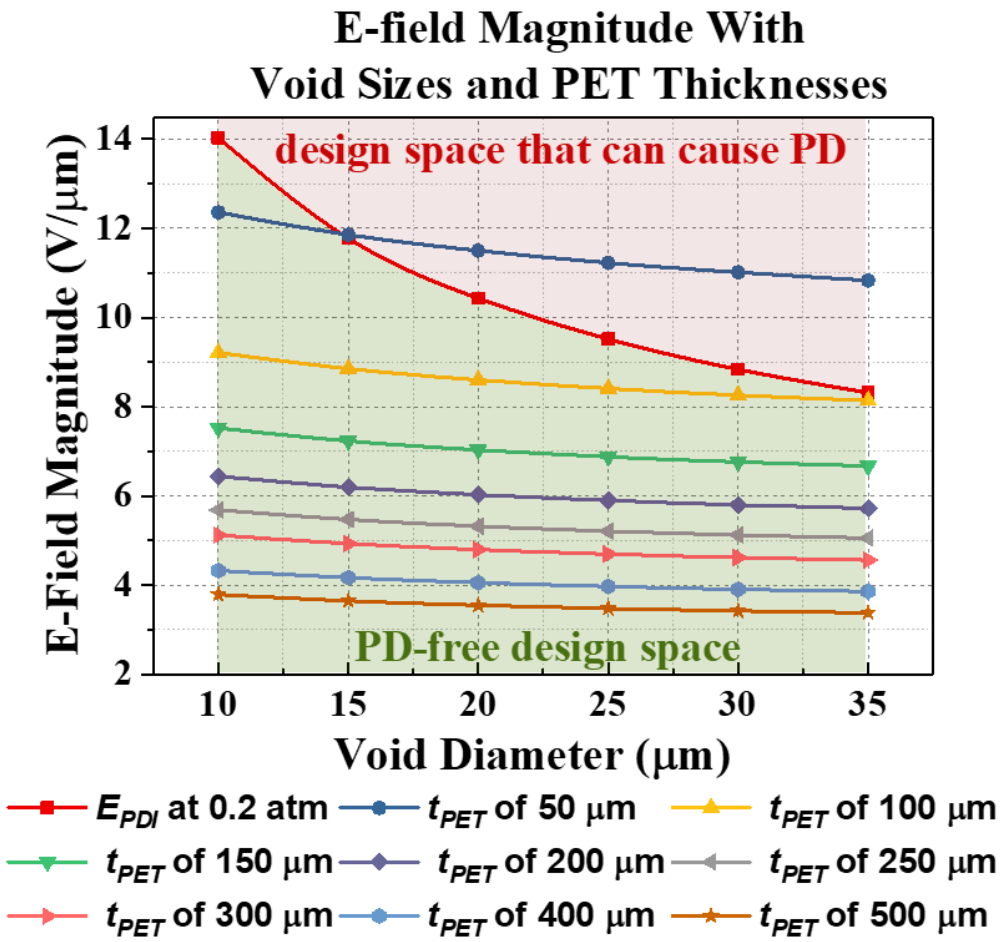

Fig. 4.15: Relationship between E-field with t_{PET} and d_{void} in parallel insulation structure.

place. Take the PD in a void as an example. According to the streamer mechanism of PD inception, the necessary condition is the well-known critical avalanche criterion. When enough electrons accumulate in the avalanche head, the avalanche can be self-propagating by its own space-charge field. The inception filed for streamer type PD depends on the void geometry and gas pressure, the dielectric permittivity, and the characteristic ionization processes within the void. The inception filed is defined as [7]:

$$E_{inc} = (E_1/p)_{cr}\, p\,[1 + B/(pd)^n]/f \tag{4.4}$$

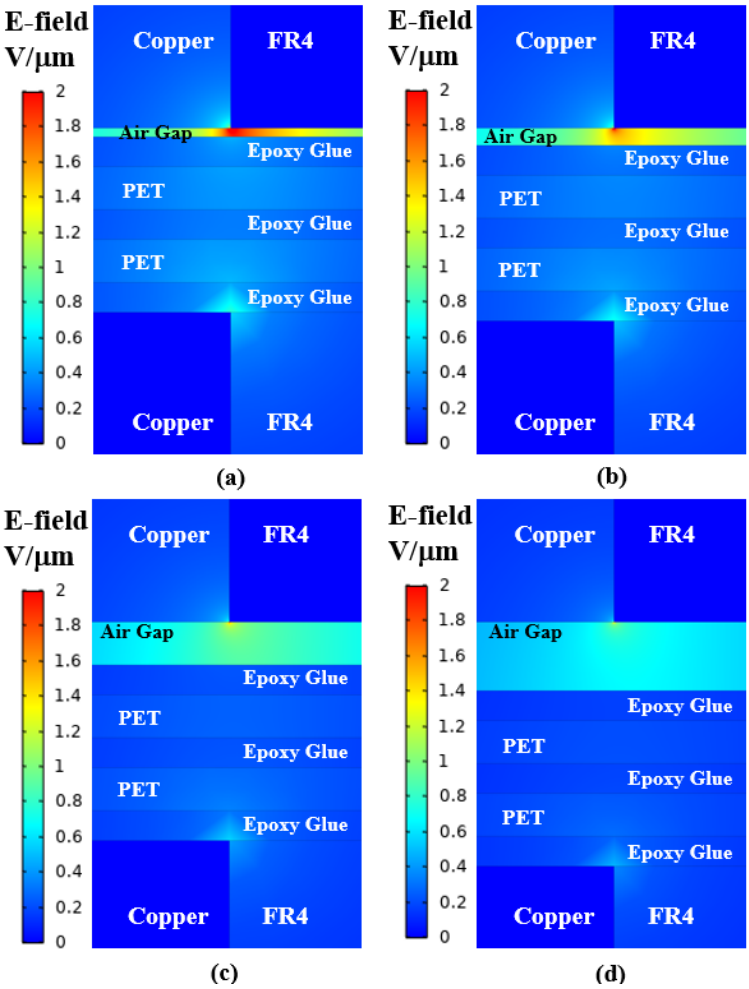

Fig. 4.16: E-field distribution for parallel structure with delamination. (a)-(d): PET-layer thickness is a constant at 50 μm, change delamination (air gap) distance as 10 μm, 30 μm, 50 μm, and 80 μm, respectively.

where $(E_1/p)_{cr}$, B, and n are the ionization parameters for the gas, p is the pressure in the void, d is the void diameter, and f is the dimensionless field enhancement factor. For air, $(E_1/p)_{cr}$ is 25 V/(Pa·m), B is 5.9 $Pa^{0.5}m^{0.5}$, n is 0.5, and f is 1. It appears that the E_{PDI} is also related to air pressure and the diameter of the void. This equation can be applied to air insulation with any irregular shape, and the p and d is the local air pressure and distance along the local electric field contour. The PD inception field with respect to pressure p and distance d are shown in Fig. 4.7. It can be observed that E_{PDI} decreases with air pressure and distance. The regions below the curves

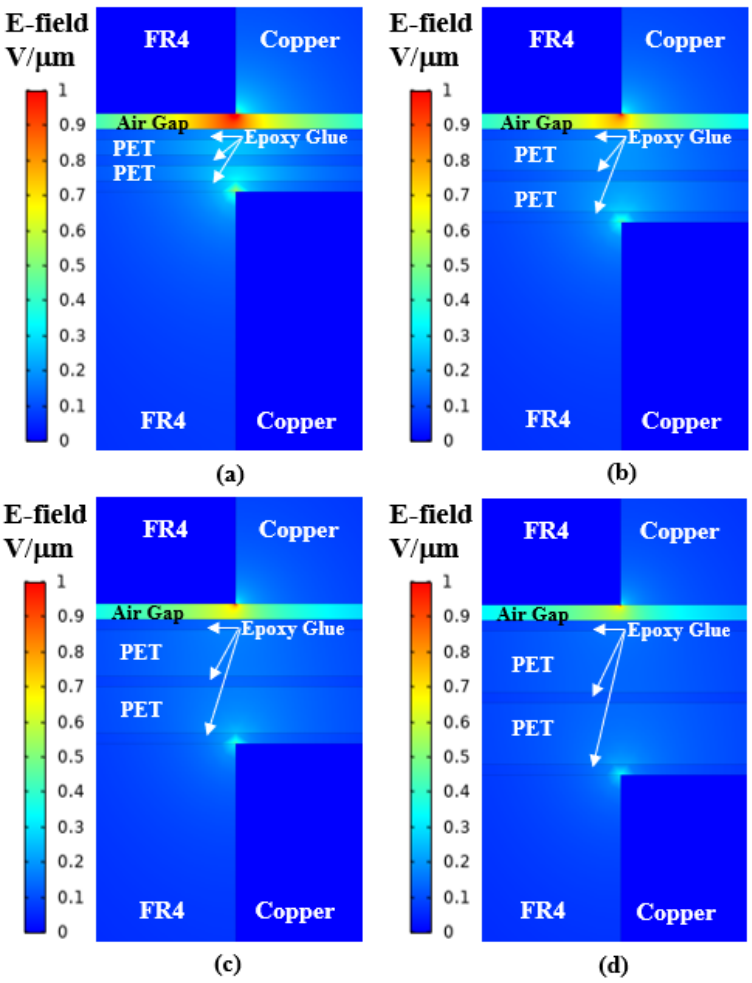

Fig. 4.17: E-field distribution for parallel structure with delamination. (a)-(d). Airgap distance is a constant at 50 μm, PET layer thickness is changed as 50 μm, 100 μm, 150 μm, and 250 μm, respectively.

of different air pressures present the PD-free area, which means if the maximum electric field in the void or air gap with these air pressures and distances is below the PD inception field, then PD will not occur. This equation serves as the PD-free criterion in this paper. Since the insulation design in this paper targets for an electric aircraft operating condition, the worst scenario of 0.2 atm (air pressure at the cruising altitude) is considered.

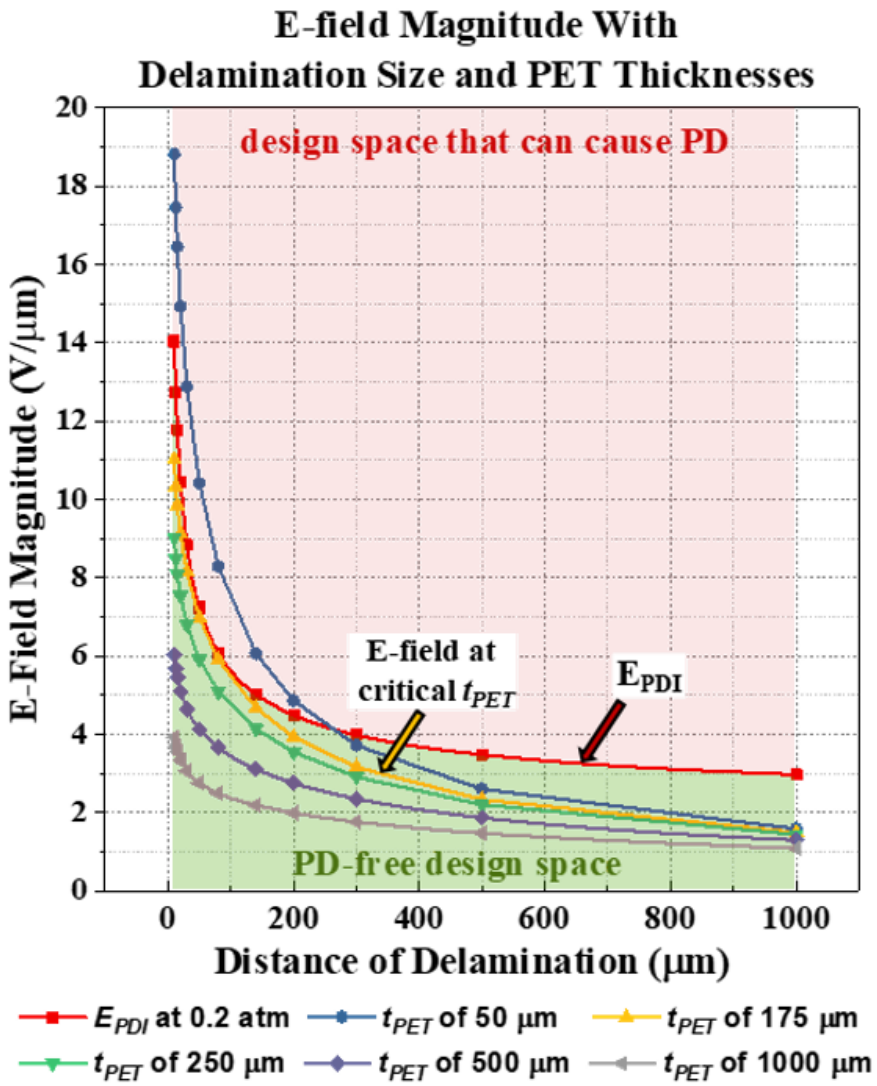

Fig. 4.18: E-field magnitude at different delamination distance and PET thickness under bent structure.

4.4.2 Busbar insulation design method

The insulation design method is proposed as Fig. 4.8, which consists of three major steps. The step I is to analyze the structure of busbar based on the developed conduction layer, then it designs a baseline insulation structure as described in chapter II, D. Based on E-field characteristics and shape of copper, insulation system is classified into different patterns.

For example, setp I first import the three-dimensional (3D) model of busbar to COMSOL

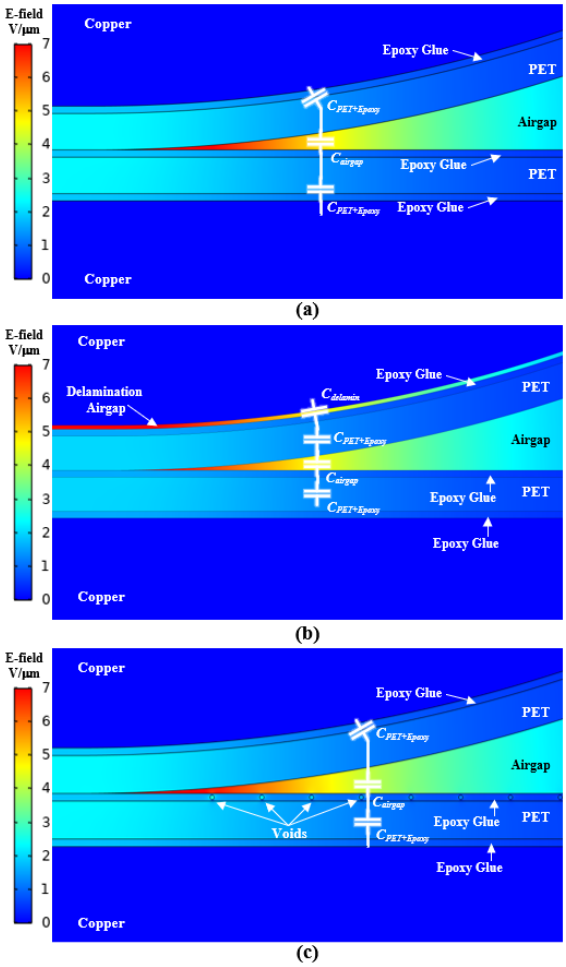

Fig. 4.19: E-field distribution at bent busbar structure, t_{PET}=175 μm, t_{epoxy} = 35 μm. (a) normal condition; (b) 20μm delamination between top copper and epoxy; (c) voids in epoxy glue, diameter of void is 20 μm.

for E-field analysis, as Fig. 4.9(a). As meshing and calculation in 3D model require huge computing resource, designers can use working plate to obtain the cross-section plane of the busbar, and perform the simulation on such 2D plane as Fig. 4.9(b). As E-field is concentrated on the corners of cooper and air gap around bending area, the insulation system, as Fig. 4.9(c), (d).

Step II is to find minimum PD-free insulation thickness through quantitative analysis. In each pattern, E-field distribution is obtained by electrostatic simulation on both normal cases and the defective cases. The worst condition is then found by comparing the simulated E-field results of

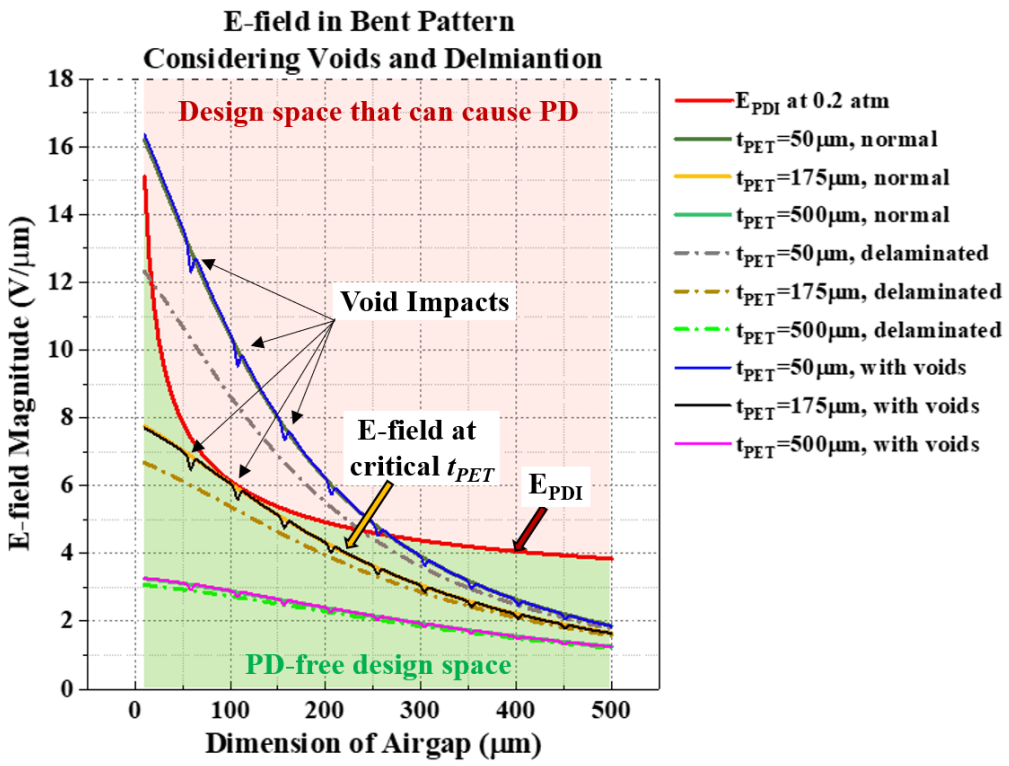

Fig. 4.20: E-field curve in bent structure including delamination and voids.

all cases. After that, minimum insulation-paper thickness (t_{min}) can be found when the worst-case E-field curve is marginally smaller than the E_{PDI} at the decompressed air pressure.

The t_{min} provides the lower-limit insulation design, while the margin is required for a robust insulation system. On the other hand, the higher limit of insulation thickness comes from the stray inductance of the busbar. Step III is to build a quantitative model of inductance-and-insulation trade-off, and select insulation thickness on the model with proper margins and acceptable over-shoots.

After the insulation design, the busbar completes all design space and will be sent for manufacture. The manufactured busbar will go through PD tests as will shown in later part, then its stray inductance wil be measured by using impedance analyzer for design evaluation purpose.

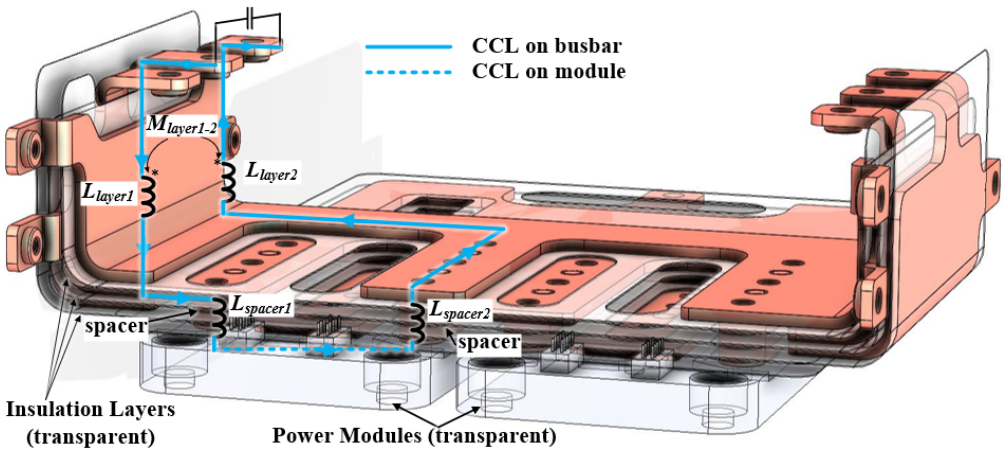

Fig. 4.21: A CCL in busbar with lumped model of self-inductance, L_{spacer}, $L_{layer,self}$ and mutual-inductance, $M_{layer1-2}$.

4.4.3 Insulation design for parallel structure

The parallel pattern is a copper-insulation-copper sandwiched structure as Fig. 4.9(c). As copper layers at the top-side and bottom-side have different voltage potentials, E-field is generated between them. The corner of copper further distorts the E-field, making the field crowded around it.

For an idea parallel insulation structure, perfect lamination between copper layers and insulation layers are assumed. However, such an assumption may not be valid, as voids and delamination can happen during manufacturing and long-term operation. These defects can introduce air gaps between the copper and insulation, and it may cause PD when the E-field in airgap is larger than the PD inception field, E_{PDI}.

The worst case of void condition is determined by using Fig. 4.10, Fig. 4.11, Fig. 4.12, and Fig. 4.13. It is seen that wen the void is moving from left to right as Fig. 4.10, the maximum E-field on such case is when the void is vertically aligned to the edge of the copper, as observed from Fig. 4.11. Moreover, when the void is moving from top to bottom, as Fig. 4.12, its peak

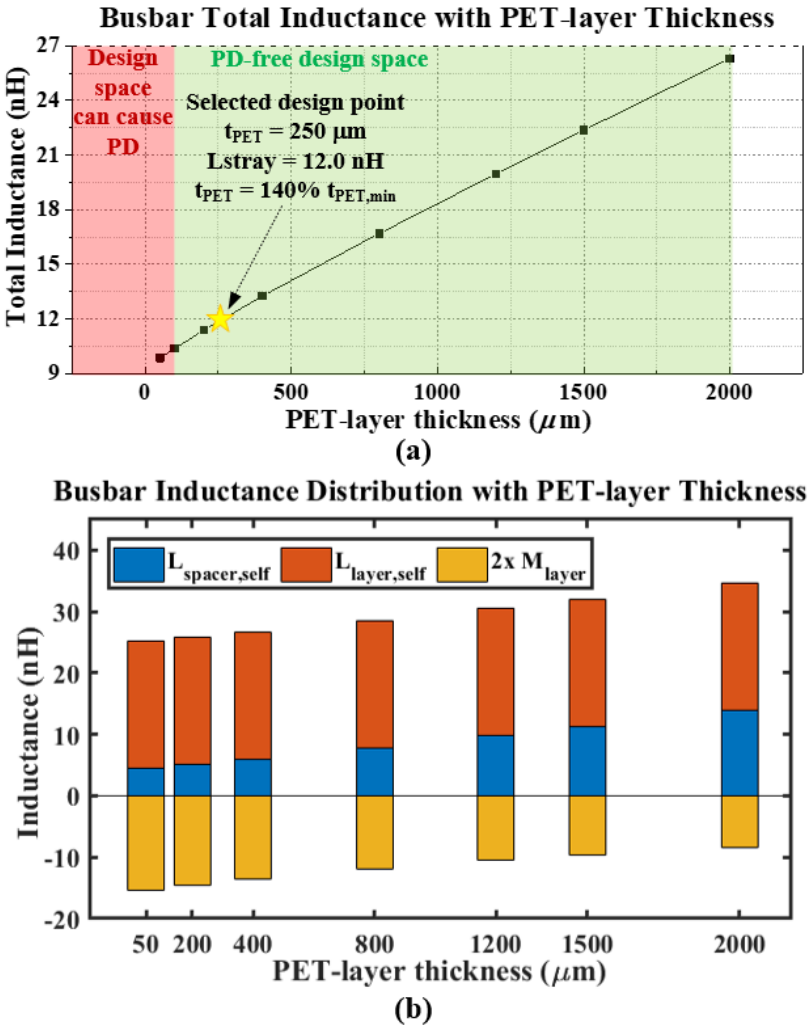

Fig. 4.22: Busbar total inductance and its distribution at different PET-layer thicknesses. Results obtained from electromagnetic simulation.

amplitude is when the void is tangent to the copper layer, as seen in Fig 4.13. Consequently, the worst case in such parallel structure is that void accidentally locates at the most crowded E-field area, which is around the copper corner, and inside the epoxy glue.

As seen in Fig. 4.14(a)-(d), the E-field maps are simulated under such scenarios, with void diameters varying from 10 μm to 35 μm. It shows a trend that a larger radius of the void comes with a lower peak magnitude of E-field. By performing the simulation at different PET-layer thicknesses, the corresponding E-field magnitudes are drawn as Fig. 4.15. The curve of E_{PDI}

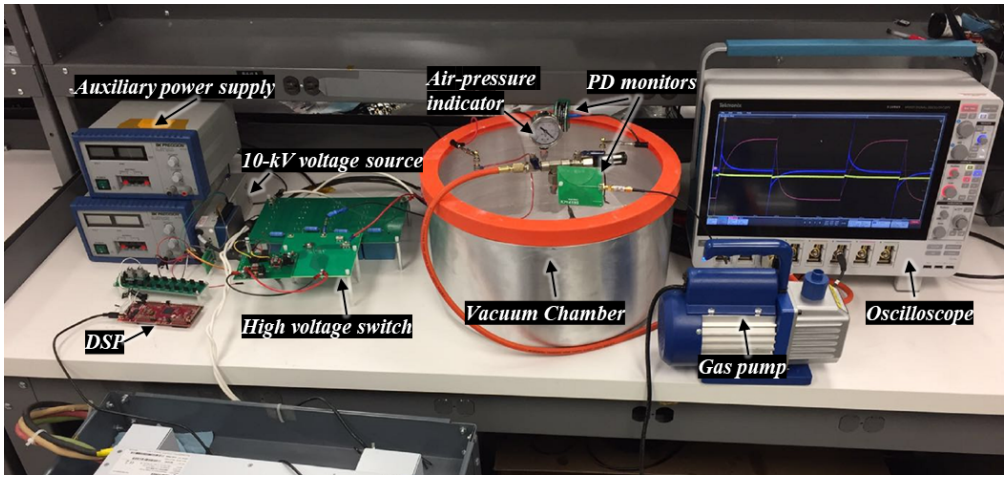

Fig. 4.23: PD testing platform for busbar PD characterization.

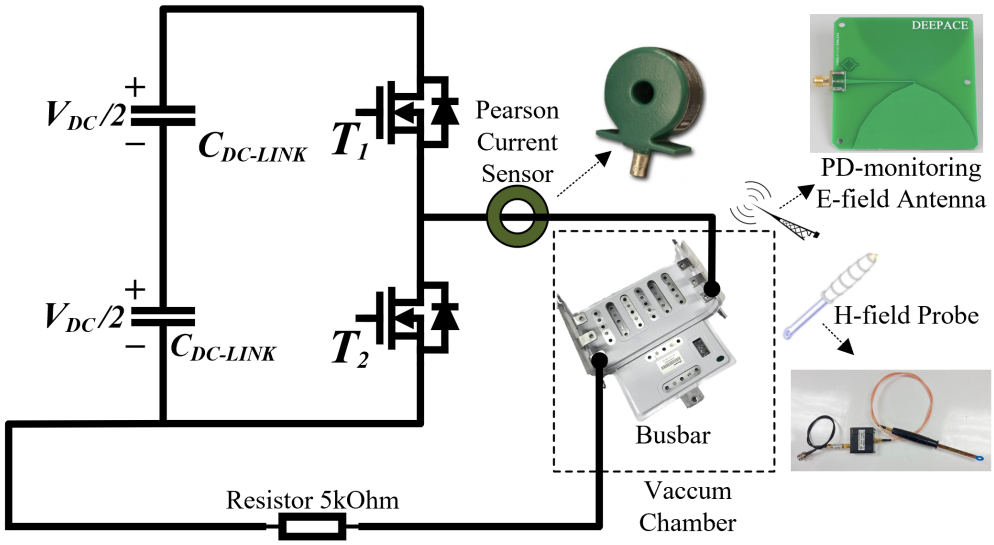

Fig. 4.24: Schematic of uni-polar PD testing circuit for busbar PD characterization.

at 0.2 atm, which is shown in Fig. 4.7, is drawn to determine the PD-free area. It is seen from Fig. 4.15 that the E-field is always lower than E_{PDI} when PET-layer thickness is 100 μm.

The vibrations and the power cycling can cause the epoxy glue detached from the copper layer, leaving an air gap between them. Such delamination phenomenon facilitates PD as the significant E-field can be concentrated in the air gap closed to the copper corner. As seen in Fig. 4.16(a)-(d), at the same PET-layer thickness (100 μm), the smaller airgap size can intensify E-field concentration, raising the peak E-field magnitude. Additionally, Fig. 4.17(a)-(d) show the E-field

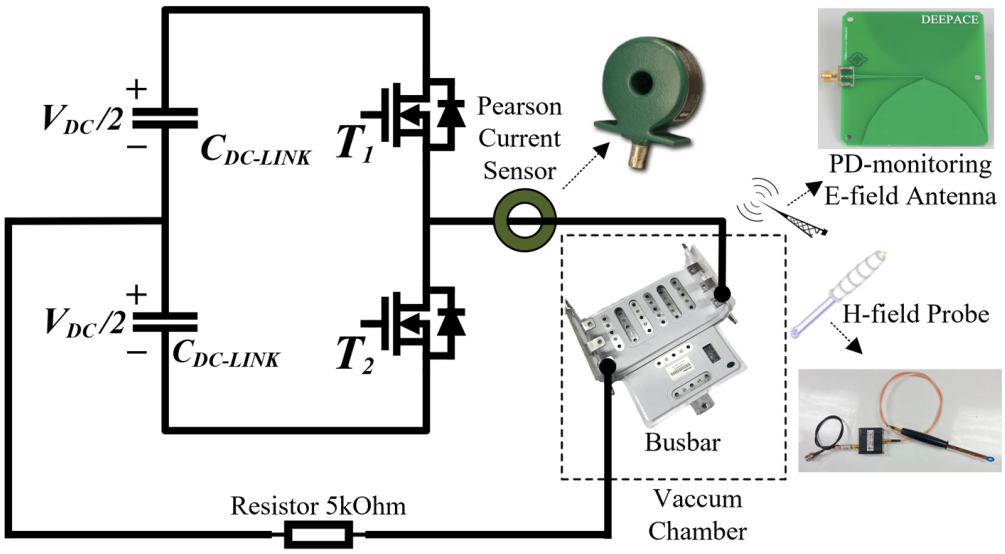

Fig. 4.25: Schematic of bipolar PD testing circuit for busbar PD characterization.

distribution when airgap is constant at 50 μm while changing PET-layer thickness. It is seen a decreased E-field magnitude in the air gap as PET-layer is thicker. This is because the thicker PET withstands more voltage drop, reducing the voltage drop in airgap. Thus, the E-field in the air gap is reduced. To quantify such a phenomenon, the peak E-field magnitudes at different distances of delamination and PET-layer thicknesses are drawn as Fig. 4.18. The E-field curve of t_{PET} at 175μm is marginally smaller than E_{PDI} at 0.2 atm. Therefore, the minimum thickness of each PET-layer is 175 μm to achieve PD free.

By combining the impacts of voids and delamination, the critical thickness of each PET layer can be derived as Eq. 4.5 , where $t_{paral,min}$ is the minimum thickness of each PET layer to achieve PD free. $t_{paral,min,void}$ and $t_{paral,min,delamin}$ are the minimum PD-free thickness by only considering the impacts of void and delamination, respectively. $t_{paral,min}$ can be derived as 175 μm based on the above analysis. Considering the insulation paper is constructed by two PET layers and three 35μm epoxy-glue layers as Fig. 4.5, the corresponding insulation paper should be 455 μm to achieve PD-free in parallel-insulation structure.

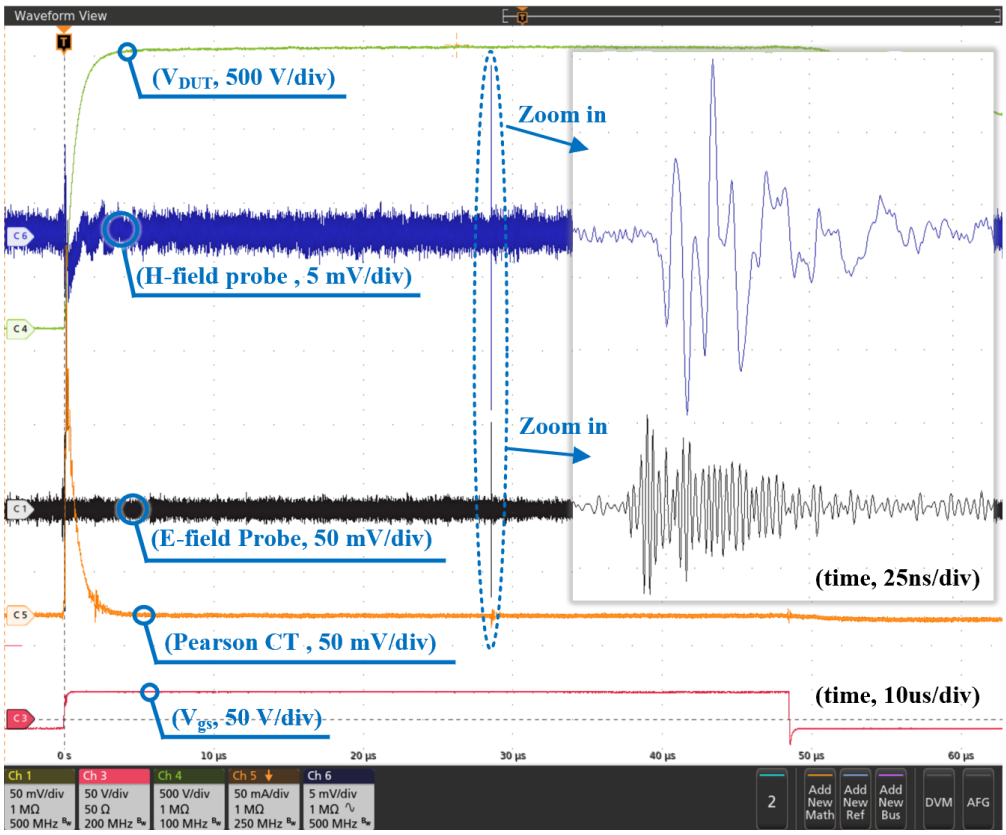

Fig. 4.26: Testing waveform of the unipolar test at 1.95 kV, 0.2 atm, with PD captured.

$$t_{\text{paral,min}} = MAX\left(t_{\text{paral,min,void}}, t_{\text{paral,min,delami}}\right) \tag{4.5}$$

4.4.4 insulation design for bent structure

Bent structure is commonly used in laminated busbar to enhance design flexibility and improve converter performance [30, 31]. However, it inevitably introduces the air gap because of the difference in bending radius, such as Fig. 4.6. Consequently, the E-field is concentrated in the bending-introduced airgap, causing PD if an improper insulation design.

While voids and delamination can also happen in a bent structure. To understand the impacts of them, electrostatic simulations are performed as Fig. 4.19, which includes normal condi-

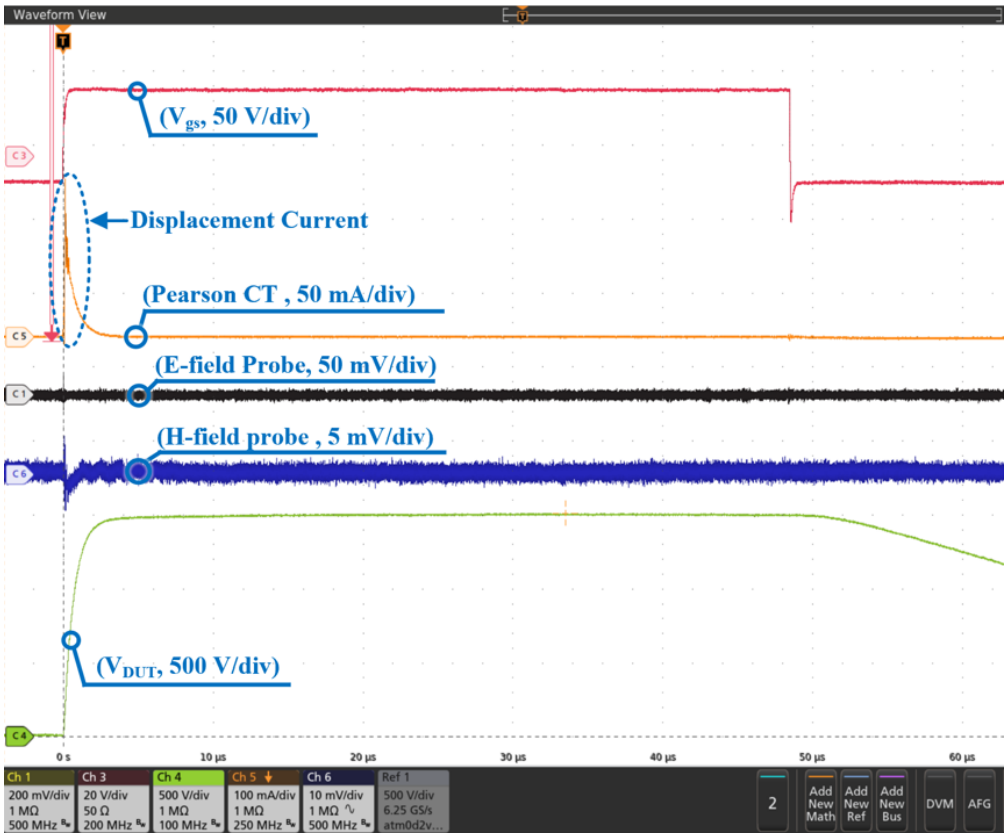

Fig. 4.27: Testing waveform of the unipolar test at 1.5 kV, 0.2 atm, without PD.

tion, scenarios which voids in the middle epoxy-glue layer, and scenario that epoxy glue is delaminated from top copper. By sweeping PET-layer thickness, the E-field curves in bent structure with different scenarios are drawn as Fig. 4.20.

The voids and delamination in bent structure can attenuate E-field in airgap. This is opposite to their influences at parallel insulation pattern, which was the root of causing PD and threaten the insulation. On the contrary, the voids in bent structure attenuate the E-field at the location where it is right above the void, causing a small dip of in E-field curves, as seen in Fig. 4.20. Moreover, when delamination happens, its corresponding E-field curve is dragged down.

This phenomenon can be explained by an equivalent model of a voltage divider. During the voltage transient, the magnitude of voltage drop on each layer is decided by its equivalent parasitic

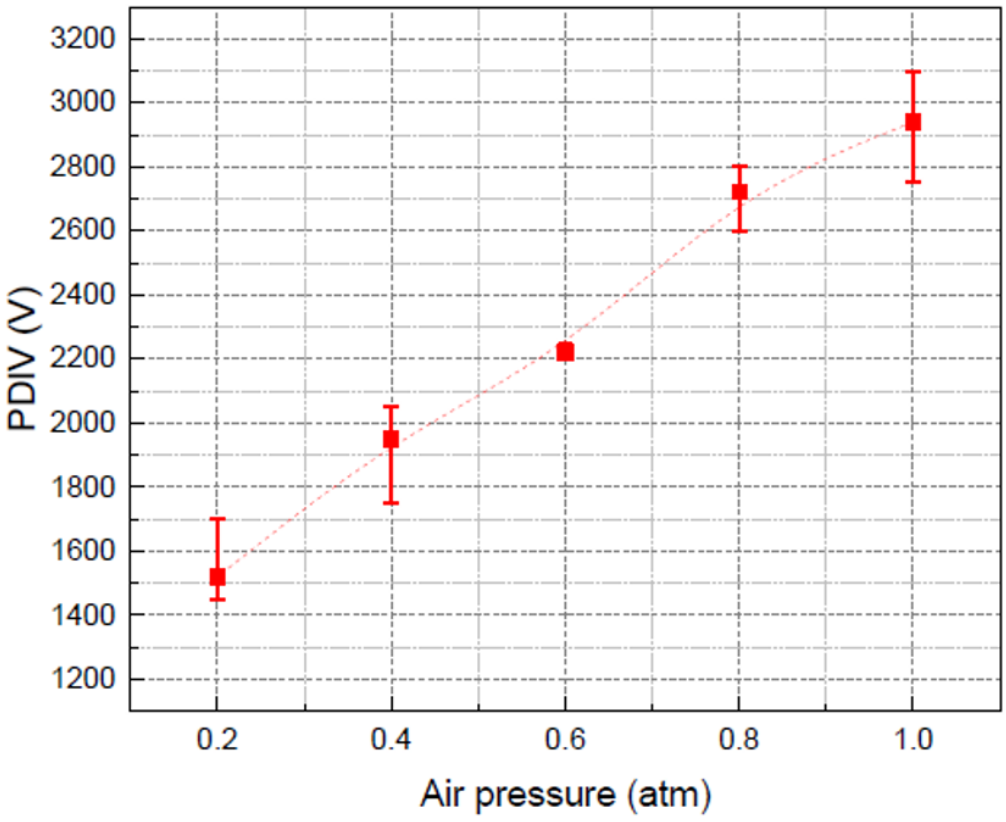

Fig. 4.28: Measured PDIV at different levels air pressure.

capacitance, as noted in Fig. 4.19. As a lower dielectric constant, the airgap has less capacitance than the insulation paper (PET layer with epoxy-glue layer). Thus the airgap withstands the majority of voltage drop and causes higher E-fields in it. Compared to the non-defect case as Fig. 4.21(a), both delamination and voids introduce another air gap, helping mitigate the voltage drop and E-field on the original airgap.

Through quantitatively analyzing both the parallel insulation pattern and bent insulation pattern, the minimum PET-layer thickness, t_{PET},min can be derived as Eq. 4.6. Where $t_{bent,min}$ is the minimum insulation of a bent structure without void and delamination. For the busbar in this paper, t_{PET},min is 175 μm. Accordingly, the minimum thickness of the insulation paper is 355μm, which considers that there are two 175 μm PET layers and three 35 μm layers in one insulation

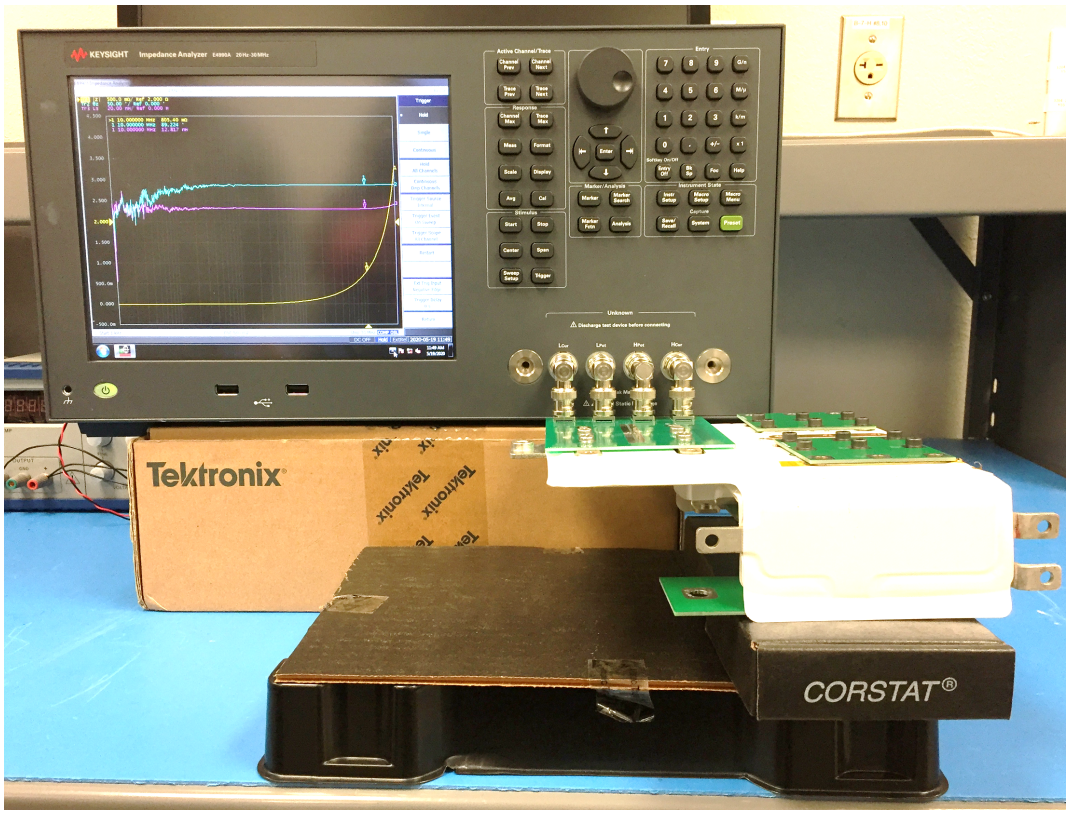

Fig. 4.29: Test setup of stray-inductance measurement by using ZA.

paper, as it was shown in Fig.4.5.

$$t_{PET,\text{min}} = \text{MAX}\left(t_{\text{paral,min}}, t_{\text{bent,min}}\right) \tag{4.6}$$

4.5 Trade-off between insulation margin and stray inductance

The lower limit of insulation thickness is discussed from the previous by warranting PD-free at the worst scenario. But design strictly at its lower limit is not necessarily an optional choice as the thicker insulation provides extra robustness.

One of the higher limits of insulation thickness is the stray inductance. Such a limit is mainly a critical factor for the wide bandgap devices due to the higher di/dt and overshoots. Given an example of CCL shown in Fig. 4.21, the total busbar stray inductance is contributed by self-

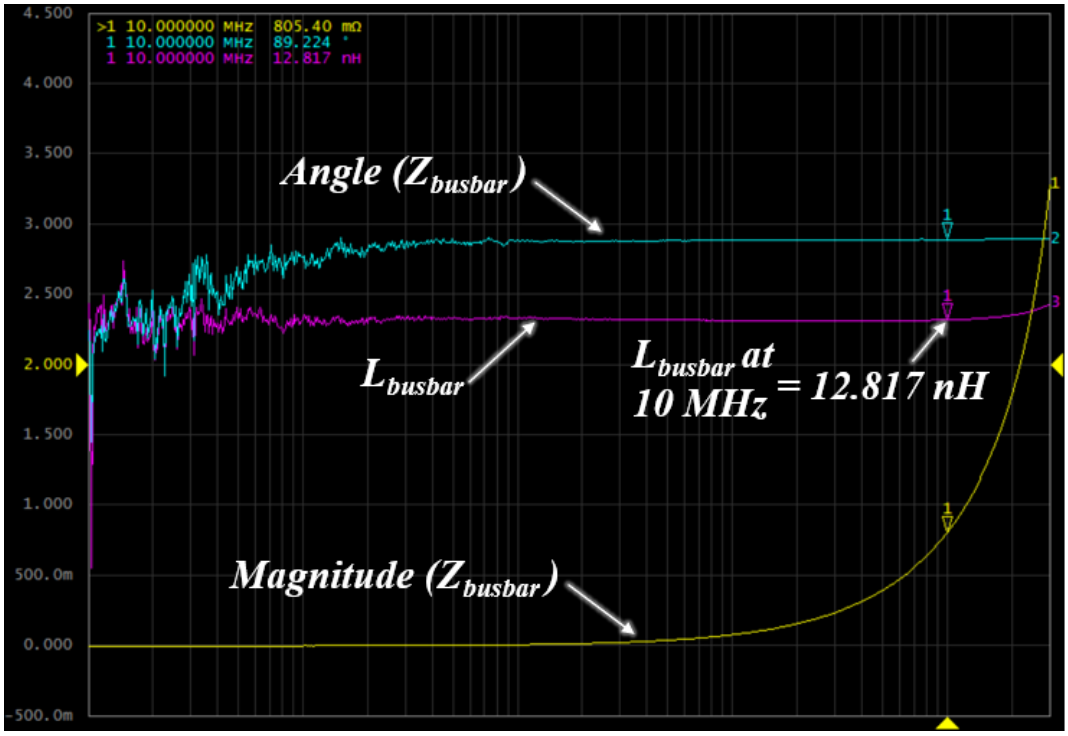

Fig. 4.30: Impedance response of busbar measured by ZA.

inductance from spacers ($L_{spacer,self}$), busbar layers ($L_{layer,self}$), and mutual-inductance between layers ($M_{layer1-2}$), as Eq. 4.7 and Eq. 4.8. The mutual inductance is a negative value as different current directions between layers.

$$L_{\text{busbar,total}} = \sum_{n} L_{\text{spacer\_}n\text{,self}} + L_{\text{layer,total}} \tag{4.7}$$

$$L_{\text{layer,total}} = L_{\text{layer1,self}} + L_{\text{layer2,self}} + 2M_{\text{layer1-2}} \tag{4.8}$$

Two aspects contribute to a positive correlation between insulation thickness and busbar stray inductance. First, the self-inductance from the spacer is enlarged as the thicker insulation. This is because the height of the spacer is extended to match the distance between top-side busbar layer and bottom-side power module, as seen in Fig. 4.21. Such extension prolongs the length of the current path, raising self-inductance, $L_{spacer,self}$. Second, the thicker insulation decreases the

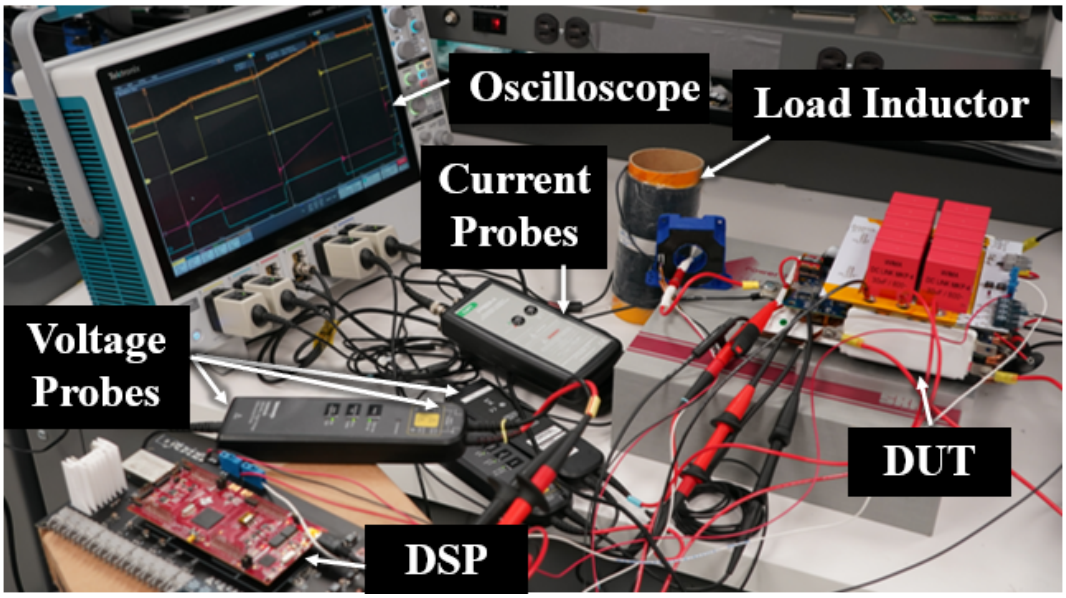

Fig. 4.31: DPT test setup.

magnitude of layer-to-layer mutual inductance, $M_{layer1-2}$. As $M_{layer1-2}$ is a negative value, the smaller magnitude of it increases total busbar inductance.

The above statement is demonstrated through performing electromagnetic simulations on the busbar at different PET-layer thicknesses. As seen in Fig. 4.22(a), higher PET-layer thickness causes higher stray inductance, where the inductance value is doubled when the thickness changes from 50 μm to 1 mm. The simulation results in Fig. 4.22(b) aligns with the above analysis: the thicker PET-layer is, the smaller value of mutual inductance is, and the higher self-inductance of the spacer is.

This paper utilizes 250 μm thickness for each PET layers, as shown in Fig. 4.22(a), which is 142.9% higher than the minimum thickness. Considering the structure of insulation paper in Fig. 4.5, the total thickness per insulation paper is 605 μm. The design can guarantee PD-free at decompressed condition, while its inductance is lower than published literature about 3L converters. As seen in later, such low inductance enabled accelerated driving speed and switching-loss

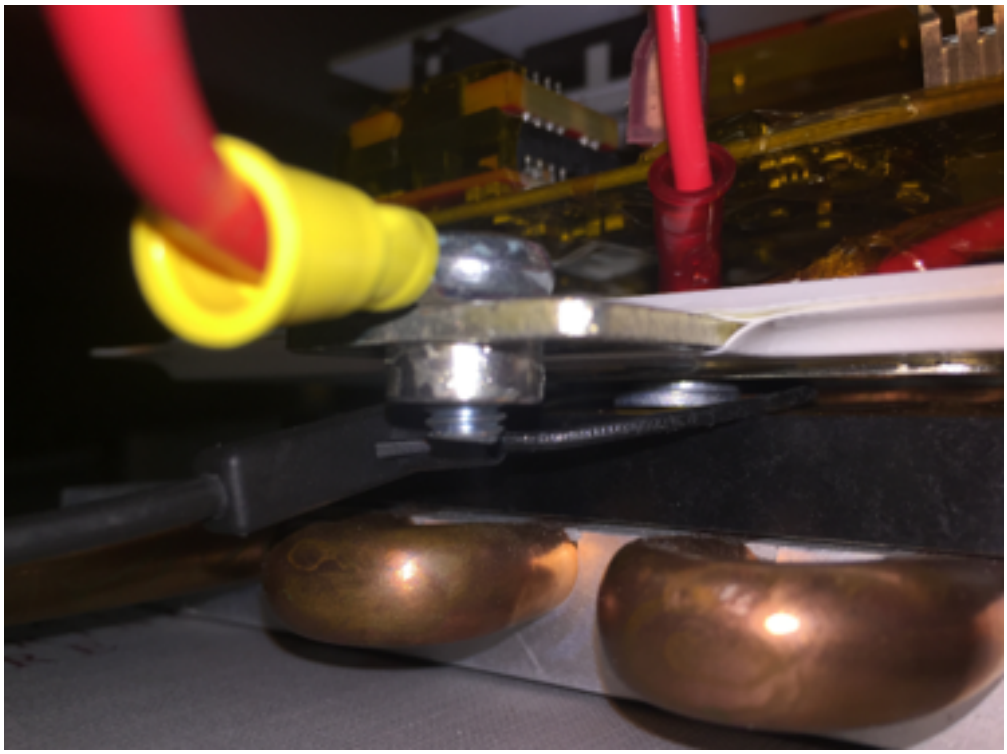

Fig. 4.32: Current measurement setup by using Rogowski coil inserted between module and busbar.

reduction within acceptable voltage overshoots.

4.6 Experiment Evaluation

4.6.1 Partial-discharge test

The PD test platform is present in Fig. 4.23. It consists of a high-voltage power source, high-voltage power switch, DC-link capacitors, DSP with fiber transmitters/receivers for gating signals, auxiliary power supply, vacuum chamber, air pressure indicator, gas pump, PD monitors, oscilloscopes.

The busbar is placed into a vacuum chamber with sufficient distance to the chamber surface. Terminals of busbar are connected to a half-bridge circuit, as Fig. 4.24. Such a setup can provide square-pulse with the amplitude changing from 0 V to the DC-link voltage. Another possible setup

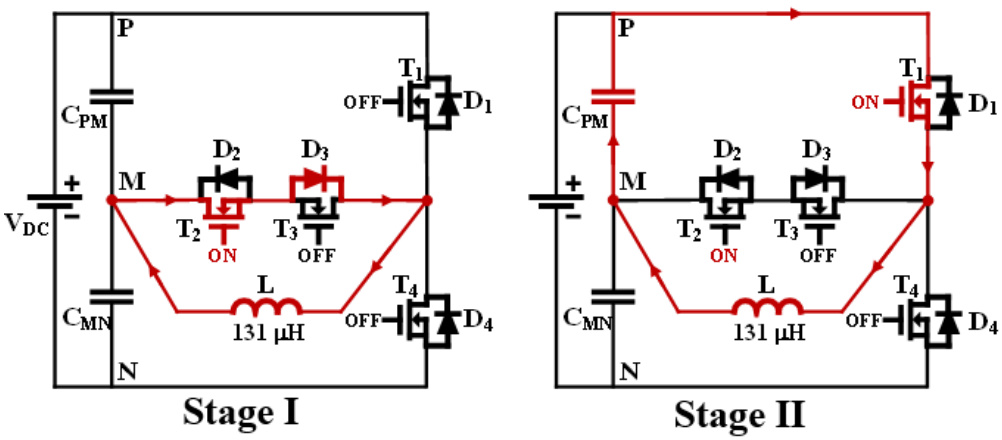

Fig. 4.33: Equivalent circuit of DPT and its corresponding two stage.

is the bi-polar setup, as in Fig. 4.25, which allows square-wave voltage changing from $-V_{DClink}/2$ to $-V_{DClink}/2$.

When PD happens, it generates noises with ultra-wideband frequency[13]. Thus, three sensing methods are used to monitor PD at extended frequency covering range. Pearson 4100 current transformer (CT) is placed as Fig. 4.24. It monitors the current on the cable, which flows through it. The bandwidth of such CT ranges from 140 Hz to 350 MHz. Both the E-field antenna and H-field probe are placed on the lid of the chamber for near-field radiation measurement. H-field probe, Tekbox TBPS01 connecting to a wideband amplifier, Tekbox TBWA1, enables measurement range between 1 MHz to 2GHz. And the E-field probe, DEEPACE UWB-4, bandwidth between 1.8 GHz to 9 GHz, is used for high-frequency radiation measurement. Because of the limited bandwidth of scope (2GHz), the output of the E-field probe is connected to the signal mixer to move down the frequency band by the designed value in the mixer.

The frequency range of PD is extensive, containing the entire measurement range, as aforementioned [13]. Therefore, all three methods should capture the PD simultaneously during the tests, which eliminate PD false detection because of noise picked up from a single sensor. Testing

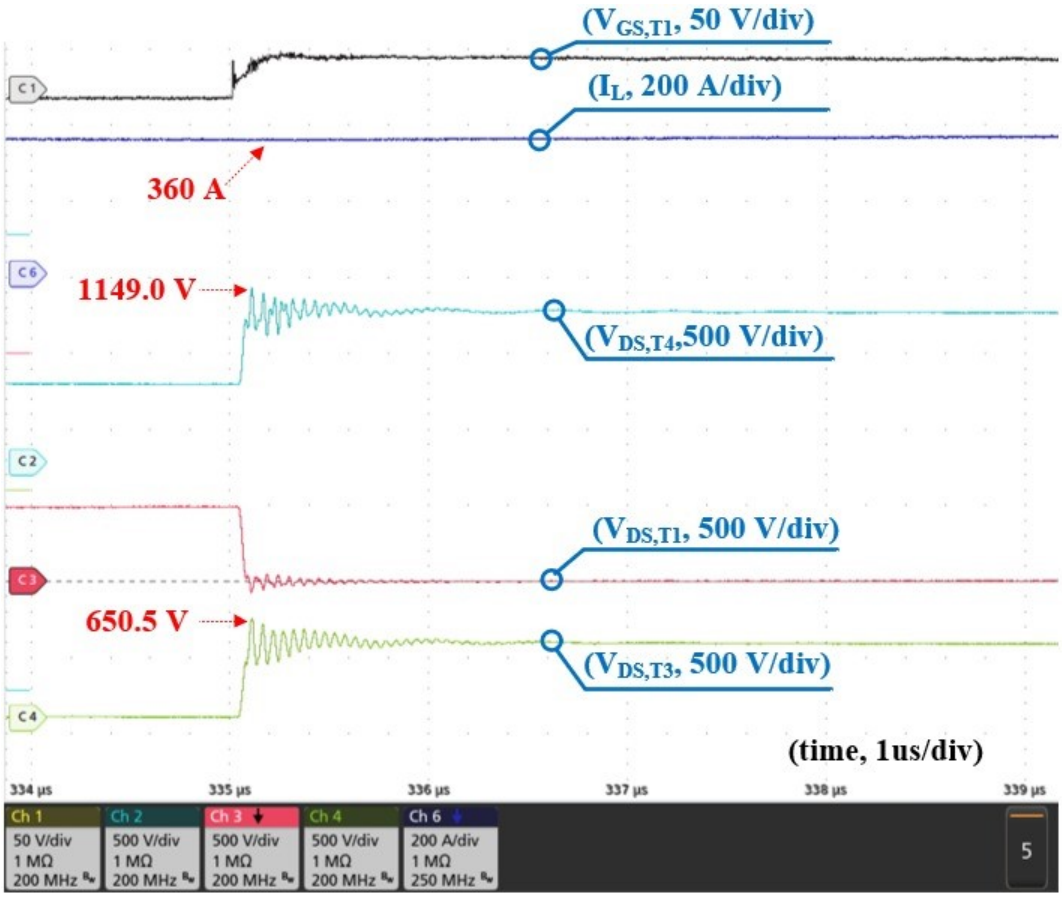

Fig. 4.34: Measured waveforms of DPT at 1 kV, 360 A.

waveforms at 1.95 kV 0.2 atm by using the platform is shown in Fig. 4.26. It is observed that different sensors capture PD at different frequency range. While the testing at 1.5 kV 0.2 atm is shown as Fig. 4.27, where no PD happens.

Ten independent PD tests are performed at each level of air pressure. By combining the 50 testing results, the partial-discharge inception voltage (PDIV) can be drawn as Fig. 4.28. The testing result aligns with Paschen's law, showing that PD happens easier at lower air pressure. At 0.2 atm, the lowest PDIV is 1430V, which is 43% higher than the voltage rating of the converter, 1 kV.

4.6.2 Stray inductance characterization

Though the busbar stray inductance can be estimated through electromagnetic simulation, it may deviate after fabrication because of manufacturing accuracy. Impedance characterization is necessary for post-fabrication evaluation.

Four-wire based characterization method is used in this paper. The measurement is conducted by using an impedance analyzer (ZA), Keysight E4990A as Fig. 4.29. To form the CCL, the ports of the busbar which connect to capacitors and power modules are shorted by coppers. Such shorting coppers may introduce additional inductance counted into the busbar. Thus, multilayer PCBs with wide and thick coppers are utilized for shorting purposes.

The measured frequency response of the busbar is shown in Fig. 4.30. At 10 MHz, the measured inductance is 12.817 nH, which is 6.7% higher than electromagnetic simulation. The extra inductance comes from the shorting coppers and potential manufacture error.

4.6.3 Double-pulse tests

The double-pulse test (DPT) setup is shown in Fig. 4.31. The high-voltage active probes, 200 MHz, Tektronix THDP0200, are used to measure both gate-source voltage and drain-source voltage of T_1, T_3, and T_4, respectively. The current is measured by 30 MHz Rogowski coil, PEM CWT MiniHF 3, by connecting the probe between busbar and the module as Fig. 4.32. A 131 μH air-core inductor is used to accumulate current.

Configure the circuit as Fig. 4.33, and use only 1 Ω of R_g. The DPT waveforms are captured at 1 kV 360A when the circuit changes from stage I to II, as shown in Fig. 4.34.

4.7 Conclusion and Future Work

This paper proposed a comprehensive insulation design method for the laminated busbar under decompressed air-pressure conditions. It can find the minimum insulation requirements under the worst scenario considering different insulation patterns and defects. The paper explicitly explained and modeled inductance-and-insulation trade-off, helping designers choose the insulation in the range between lower and higher limits.

The proposed method is verified by designing the insulation of a busbar for a 450 kVA 3L motor drive. PD tests are performed under different levels of air pressure, demonstrated the effectiveness of the insulation design method. The proposed insulation design also helps converter reaching lower stray inductance, enabling switching loss reduction of 66.7% at 1kV, 350A, with limited switching voltage overshoots.

4.8 Bibliography

[1] J. A. Rosero, dt. al, ”Moving towards a more electric aircraft,” in IEEE Aerospace and Electronic Systems Magazine, vol. 22, no. 3, pp. 3-9, March 2007.

[2] C. Chen, et al., ”Investigation, Evaluation, and Optimization of Stray Inductance in Laminated Busbar,” in IEEE Transactions on Power Electronics, vol. 29, no. 7, pp. 3679-3693, July 2014.

[3] D. Fabiani, et al.,”The effect of voltage distortion on ageing acceleration of insulation systems under partial discharge activity,” in IEEE Electrical Insulation Magazine, vol. 17, no. 3, pp. 24-33, May-June 2001.

[4] J. He, et al., ”PWM Strategy for MW-Scale “SiC+Si” Active NPC Converter in Electric Aircraft Propulsion Applications,” in IEEE Transactions on Industry Applications.

[5] D. Zhang, et al., ”Development of Megawatt-Scale Medium-Voltage High Efficiency High Power Density Power Converters for Aircraft Hybrid-Electric Propulsion Systems,” 2018 AIAA/IEEE Electric Aircraft Technologies Symposium (EATS), Cincinnati, OH, 2018, pp. 1-5.

[6] D. Zhang, et al., ”Development of A High-Power Density Megawatt-Scale Medium-Voltage Power Converter for Aircraft Hybrid-Electric Propulsion Systems,” 2019 AIAA/IEEE Electric Aircraft Technologies Symposium (EATS), Indianapolis, IN, USA, 2019.

[7] Y. Wang et al., ”Partial-Discharge-Free Insulation Design of Air-Core Permanent Magnet Synchronous Machine for Aircraft Propulsion,” IEEE Transactions on Transportation Electrification, Early access.

[8] A. Cavallini, et al., ”Modelling Partial Discharge Inception in magnet wires at different altitudes,” 2016 IEEE Conference on Electrical Insulation and Dielectric Phenomena (CEIDP), Toronto, ON, 2016.

[9] C. M. DiMarino, et al., ”10-kV SiC MOSFET Power Module With Reduced Common-Mode Noise and Electric Field,” in IEEE Transactions on Power Electronics, vol. 35, no. 6, pp. 6050-6060, June 2020.

[10] C. DiMarino et al., ”Design and Experimental Validation of a Wire-Bond-Less 10-kV SiC MOSFET Power Module,” in IEEE Journal of Emerging and Selected Topics in Power Electronics, March 2020.

[11] Y. Wang, et al., ”Partial Discharge Investigation of Form-Wound Electric Machine Winding for Electric Aircraft Propulsion,” IEEE Transactions on Transportation Electrification, Early access.

[12] D. Roger, et al., ”Proposition for Improving the Design of Motor Windings for Low-Pressure

Environment," in IEEE Transactions on Industry Applications, vol. 56, no. 3, pp. 2491-2499, May-June 2020.

[13] L. Zhang, et al., "The partial discharge characteristics study of insulated copper bus bar," 2013 Annual Report Conference on Electrical Insulation and Dielectric Phenomena, Shenzhen, 2013.

[14] Mallys Banda, et al., Simulation of Space Charge Impact on Partial Discharge Inception Voltage in Power Busbars Dedicated to Future Hybrid Aircrafts. Circuits and Systems, 2018, 09.

[15] M. Sellah, et al., "Partial discharge investigations in laminated busbars," IEEE 2nd International Conference on Dielectrics (ICD), Budapest, 2018.

[16] G. Parent, et al., "Determination of Partial Discharge Inception Voltage and Location of Partial Discharges by Means of Paschen's Theory and FEM," in IEEE Transactions on Magnetics, vol. 55, no. 6, pp. 1-4, June 2019.

[17] C. Zhang et al., "Partial Discharge Behavior of Epoxy/paper Insulated Tubular Busbars with Artificial Defects," 2019 2nd International Conference on Electrical Materials and Power Equipment (ICEMPE), Guangzhou, China, 2019.

[18] C. Park, "Electret: An Entirely New Approach of Solving Partial Discharge Caused by Triple Points, Sharp Edges, Bubbles, and Airgaps," in IEEE Access, vol. 8, pp. 78354-78366, 2020.

[19] Y. Xu, R. Burgos and D. Boroyevich, "Insulation design and evaluation via partial discharge (PD) test for power electronics application," IEEE Electric Ship Technologies Symposium (ESTS), Arlington, VA, 2017.

[20] Y. Xu et al., "Medium-Voltage SiC-Based Converter Laminated Bus Insulation Design and Assessment," in IEEE Journal of Emerging and Selected Topics in Power Electronics, Sept. 2019.

[21] Y. Chen, et al., "A Model-Based Multi-Objective Optimization for High Efficiency and High Power Density Motor Drive Inverters for Aircraft Applications," NAECON 2018 - IEEE National Aerospace and Electronics Conference, Dayton, OH, 2018.

[22] H. Peng et al., "Improved space vector modulation for neutral-point balancing control in hybrid-switch-based T-type neutral-point-clamped inverters with loss and common-mode voltage reduction," in CPSS Transactions on Power Electronics and Applications, Dec. 2019.

[23] A. Nawawi et al., "Design and Demonstration of High Power Density Inverter for Aircraft Applications," in IEEE Transactions on Industry Applications, vol. 53, no. 2, pp. 1168-1176, March-April 2017.

[24] J. Ke et al., "Investigation of Low-Profile, High-Performance 62-mm SiC Power Module Package," in IEEE Journal of Emerging and Selected Topics in Power Electronics.

[25] Z. Wang, et al., "Design and Validation of A 250-kW All-Silicon Carbide High-Density

Three-Level T-Type Inverter," in IEEE Journal of Emerging and Selected Topics in Power Electronics, March 2020.

[26] A. Deshpande, et al., "Design of a High-Efficiency, High Specific-Power Three-Level T-Type Power Electronics Building Block for Aircraft Electric-Propulsion Drives," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 407-416, March 2020.

[27] Z. Wang et al., "A Compact 250 kW Silicon Carbide MOSFET based Three-Level Traction Inverter for Heavy Equipment Applications," 2018 IEEE Transportation Electrification Conference and Expo (ITEC), Long Beach, CA, 2018.

[28] Z. Yuan et al., "Design and Evaluation of Laminated Busbar for Three-Level T-Type NPC Power Electronics Building Block With Enhanced Dynamic Current Sharing," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 395-406, March 2020.

[29] M. A. Lieberman, and A. J. Lichtenberg. Principles of plasma discharges and materials processing. New York: Wiley-interscience, 2005.

[30] A. D. Callegaro et al., "Bus Bar Design for High-Power Inverters," in IEEE Transactions on Power Electronics, vol. 33, no. 3, pp. 2354-2367, March 2018.

[31] Deshpande, Amol A., et al. "Modular Three-level T-type Power Electronics Building Block for Aircraft Electric-Propulsion Drives." AIAA Propulsion and Energy 2020 Forum. 2020.

[32] J. Wang, et al., "Development of a compact 750kva three-phase NPC three-level universal inverter module with specifically designed busbar," Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Feb 2010.

[33] Y. Jiao, et al., "Switching Performance Optimization of a High Power High Frequency Three-Level Active Neutral Point Clamped Phase Leg," in IEEE Transactions on Power Electronics, July 2014.

[34] Q. Wang, et al., "Switching transient analysis and design of a low inductive laminated bus bar for a t-type converter," Journal of Power Electronics, vol. 16, no. 4, pp.1256–1267, 2016.

[35] A. Deshpande et al., "Multilayer busbar design for a si igbt and sic mosfet hybrid switch based 100 kw three-level t-type pebb," IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Oct 2017.

[36] Z. Wang, et al., "Busbar Design and Optimization for Voltage Overshoot Mitigation of a Silicon Carbide High-Power Three-Phase T-Type Inverter," in IEEE Transactions on Power Electronics, Jan. 2021.

[37] Z. Yuan et al., "Design and Evaluation of A 150 kVA SiC MOSFET Based Three Level TNPC Phase-leg PEBB for Aircraft Motor Driving Application," 2019 IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA, 2019.

5 Design of A 1.2 kV, 300 A, High-performance Power Module for MEA Applications

This paper has been submitted to IEEE APEC 2021. The paper is under the review during the period of dissertation composition.

List of author's name, Yuan, Z., Emon, A.I., Huang, S., Wang, Z., Wang, Y., Whitt, R., Fang, L, and Huitink, D.

5.1 Abstract

Three-level T-type neutral-point-clamped converters (3L-TNPC) are widely used in motor drive and PV applications because of the higher efficiency, improved output THD, and lower common-mode noise. However, such topology suffers from high stray inductance because of the complicated power loop structure. Its power-module current density is less than the two-level (2L) converter as the increased switch counts. This paper proposes a SiC-MOSFET based 3L-TNPC power module with a hybrid packaging method to improve module performance. The module has a printed circuit board (PCB) directly soldered on the top of direct bounding copper (DBC), with bare dies soldered on DBC and connecting to PCB by bonding wires. Such a structure allows the power loop on both DBC and PCB. This reduces stray inductance through enhanced mutual-inductance cancellation. The introduced PCB can provide extra space and flexibility in gate-loop optimization, improved power density, and synchronous gate drive between parallel dies. The heat from dies can also be directly dissipated through DBC and the proposed direct-soldered coldplate, enhancing thermal conductivity because of thermal-paste elimination and thermal-couple reduction. A 1.2 kV, 300 A SiC 3L-TNPC module is fabricated with measured loop inductance of

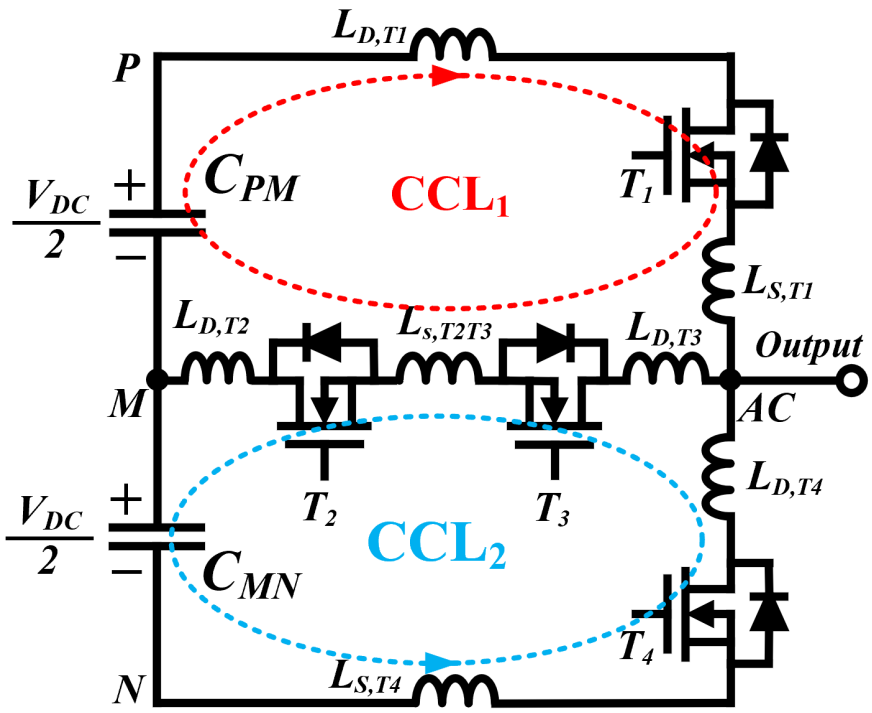

Fig. 5.1: Topology of 3L-TNPC with current commutation loop (CCL_1 and CCL_2) noted.

2.5 nH. Faster driving speed by using 0.33 Ω gate resistance is enabled to reduce switching loss. Eventually, the module is thoroughly evaluated from electromagnetic simulation, lamina-flow-and-thermal simulation, double-pulse tests up to 800 V/ 450 A, continuous tests up to 800 V/ 230 A, and thermal image monitoring.

5.2 Introduction

The three-level t-type neutral point-clamped (3L-TNPC) converters, as seen in Fig. 5.1, have been demonstrated with superior efficiency[1-3], THD[4,5], and EMI performance [6] at voltage ranges between 400 V to 1200 V. It has been widely used in applications such as motor drive [7,8], UPS systems, and PV inverter.

Various 3L-TNPC modules have been announced by semiconductor company such as Infineon, On Semiconductor, Vincotech, Semikron, Fuji Electric, and Mitsubishi. While Infineon ap-

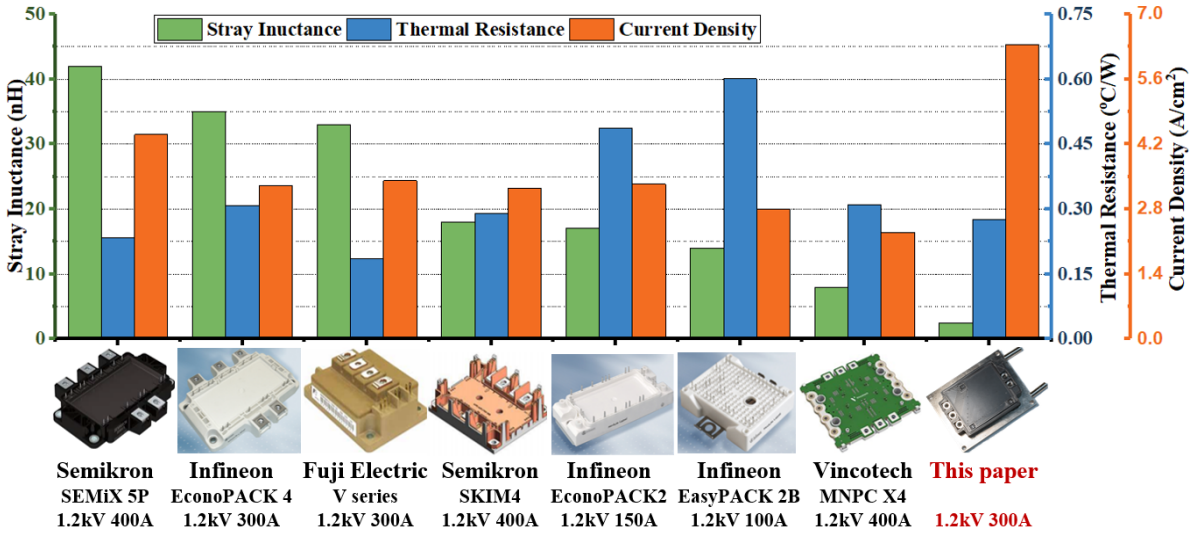

Fig. 5.2: Shoulder-by-shoulder comparison of power modules from Infineon, Vincotech, Semikron, Fuji Electric and this paper [20-26].

plied high-speed IGBT for such an application, enabling significant switching loss reduction. Fuji Electric utilized a novel reverse-blocking IGBT (RB-IGBT) as a clamping leg. Its bi-directional controllable feature helps to reduce switch count in 3L-TNPC [9]. The modules from Vincotech achieve lower stray inductance than their competitors through the multi-stage capacitor-decoupling strategy. The design embeds internal capacitors into the Vincotech module for closest loop decoupling, while it also places film capacitors externally right next to the terminal for the second-stage decoupling. Such configuration effectively suppresses turn-off voltage overshoots and mitigates voltage oscillation [10]. The key parameters of the recent modules are summarized as Fig. 5.2, such as stray inductance, thermal impedance, and current density.

Through the product survey, it is seen that most 3L-TNPC modules still suffer from higher stray inductance (>15 nH), which can cause higher voltage overshoots during switching transients, and it will also limit the switching speed. Minimizing such inductance is becoming crucial, especially when wide bandgap devices are used.

Module inductance reduction can be performed through optimizing wire-bounder induc-

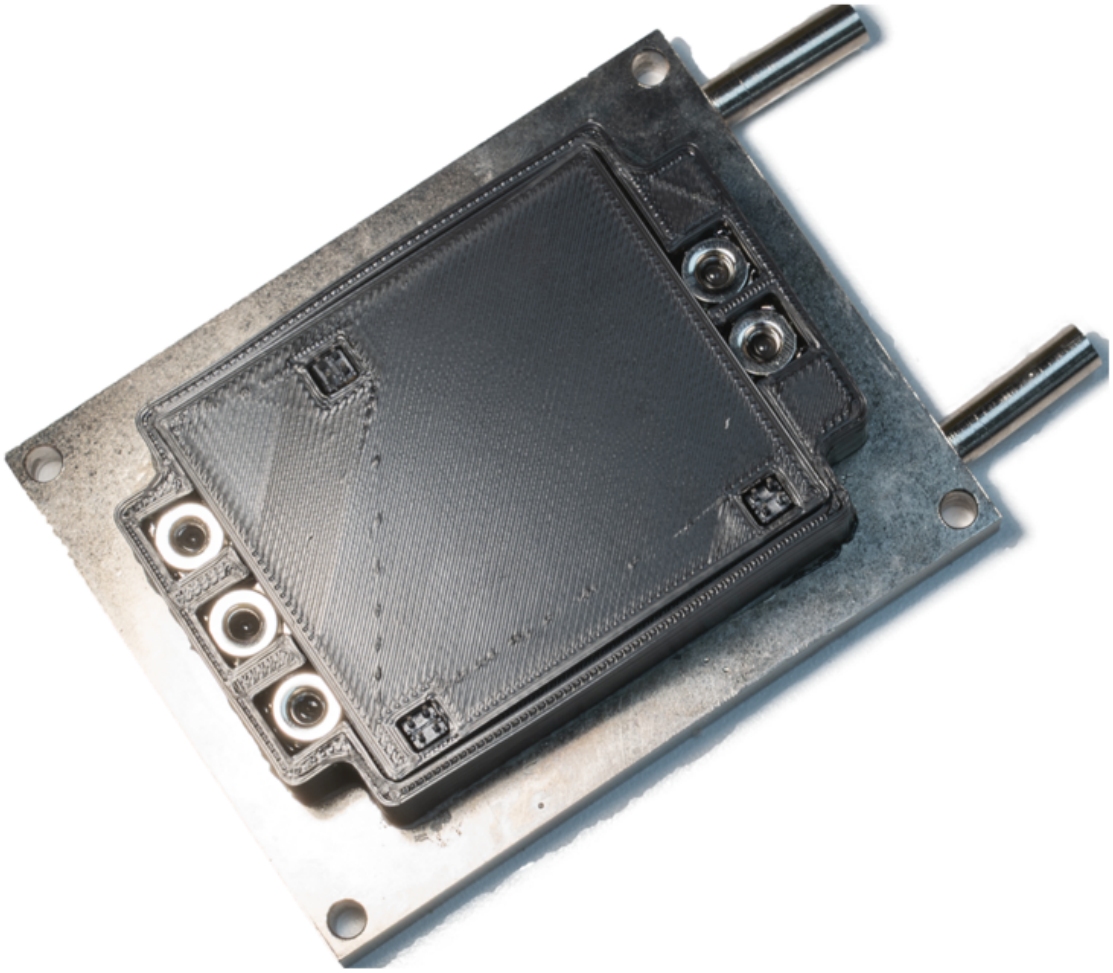

Fig. 5.3: Top view of the fabricated power module, with lid covered on top.

tance and substrate inductance, respectively. Novel wire-bounding methods can reduce its self-inductance through larger bonding conductors. For example, Mitsubishi direct-lead bounding technology enables interconnection between the top-surface of power bare die and power lead. Consequently, the designed module can reduce the internal inductance by 43% [11]. The SKiN structure proposed by Semikron replaces conventional wire bounds by flex printed circuit boards, which is demonstrated to save stray inductance by 10%[12]. Other methods are also reported with stray inductance reduction, such as metal post [13], fuzzy button [14], and planar copper interconnect [15]. Nevertheless, most of the novel top-side interconnection method requires remetalization

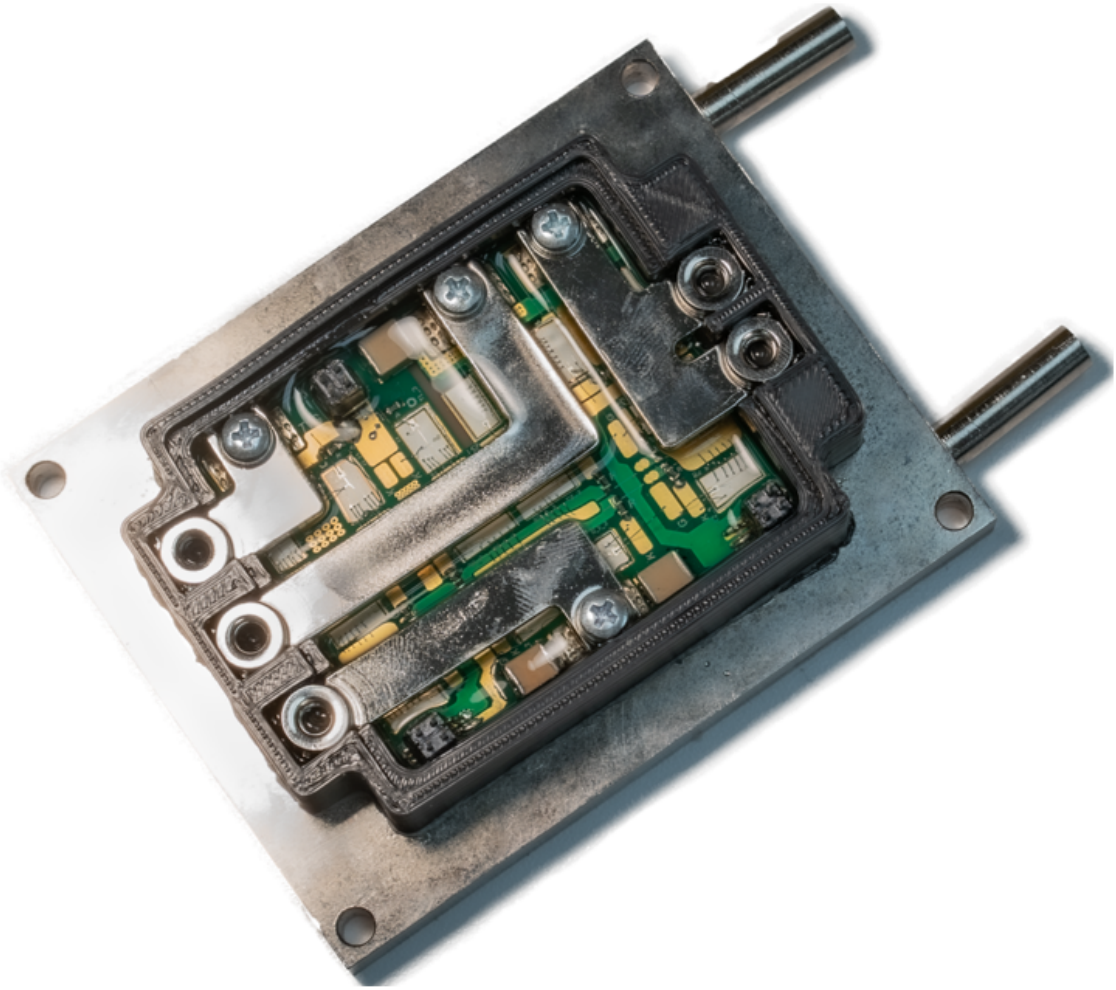

Fig. 5.4: Top view of the fabricated power module, without lid covered on top.

of power chip, increasing fabrication complexity.

Reducing the substrate-layer inductance is also essential. The conventional substrate structure has substantial limitations on power-loop optimization. Because the self-inductance is dominated in those structures, and it is correlated to the loop length. Those packaged modules typically have stray inductance over 15 nH, and it can be increased as a higher power rating. To solve the problem, W. Ruxi and C. Zhen from the Center for Power Electronics Systems (CPES), Virginia Polytechnic Institute and State University proposed a PCB + DBC hybrid structure in 2010 and 2013 [16, 17]. The structure can significantly shrink the length current commutation loop, achiev-

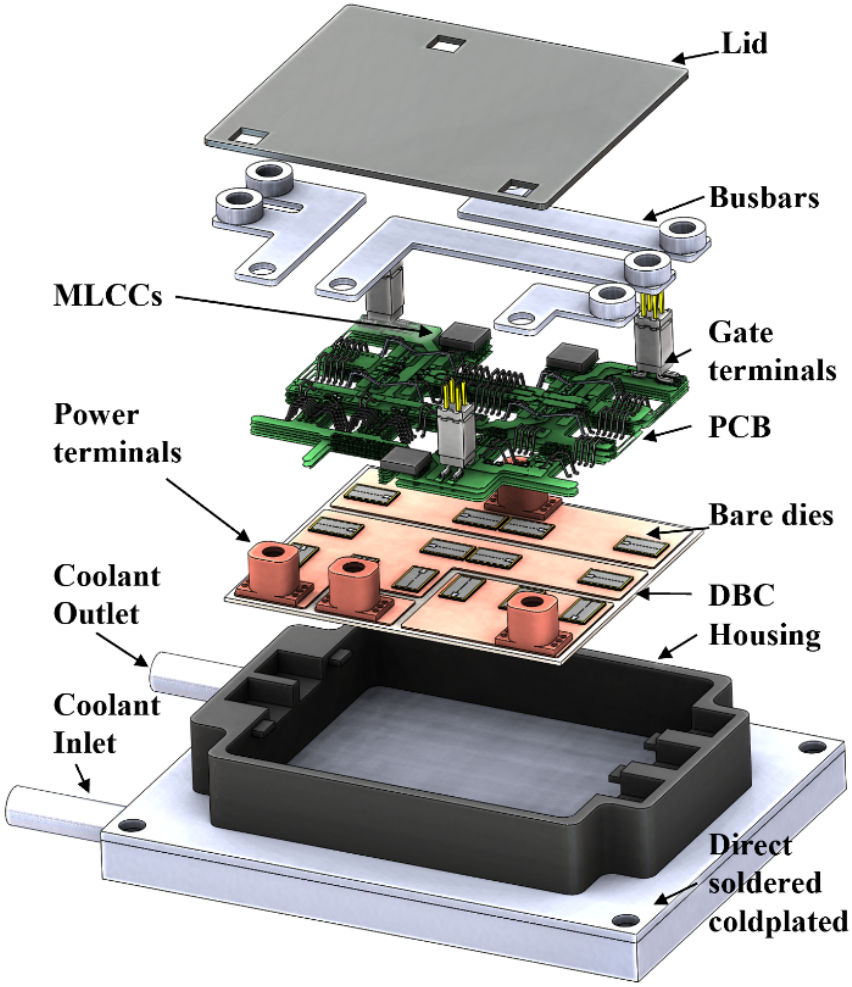

Fig. 5.5: Exploded view of the power module.

ing 3.8 nH stray inductance for their 1200 V, 10 A phase-leg power module. In 2017, an improved hybrid structure was announced by Huazhong University of Science and Technology (HUST) [18]. The design is the first time to design the module by relying on the impacts of the mutual-inductance cancellation. Their design of a 1200 V 24 A phase-leg module can achieve stray inductance as low as 0.9055 nH. Compared to the CPES design, which focuses on self-inductance minimization, the HUST design intentionally enhances the mutual inductance through introducing an additional current path on PCB, with the opposite current direction on DBC.

Nevertheless, the design has to allow the major current flowing through the PCB, whose

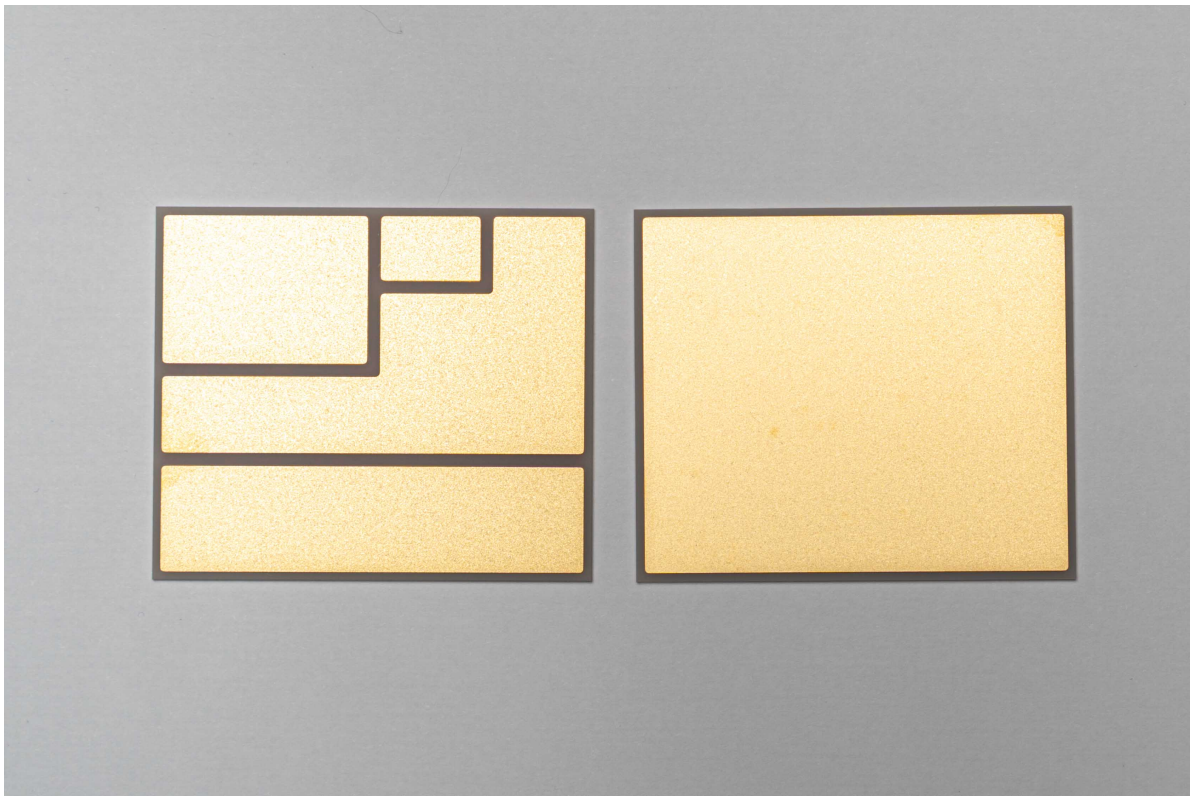

Fig. 5.6: The pattern of designed DBC for the 3L-TNPC power module. Left: top side; Right: bottom side.

copper is much thinner (3.47 μm to 10.41 μm) than the copper on DBC (300 μm). Thus the proposed structure could be limited in high current applications. Moreover, all the technologies mentioned above are restricted in 2L converters. While adopting the technology into a 3L-converter application is crucial and necessary. Limited power density is another challenge of 3L-TNPC. This can be quantified by defining the current density of a power module as Eq. 5.1, where $I_{c,80^oC}$ is the rated continuous current at the case-temperature of 80 ^oC.

$$J_{\text{module}} = \frac{I_{c,80^\circ\text{C}}}{w \times l} \tag{5.1}$$

As shown in Fig. 5.2, most of the power module has a current density of less than 3.5 A/cm^2, which is typically smaller than the 2L. For example, at the same standard housing, same

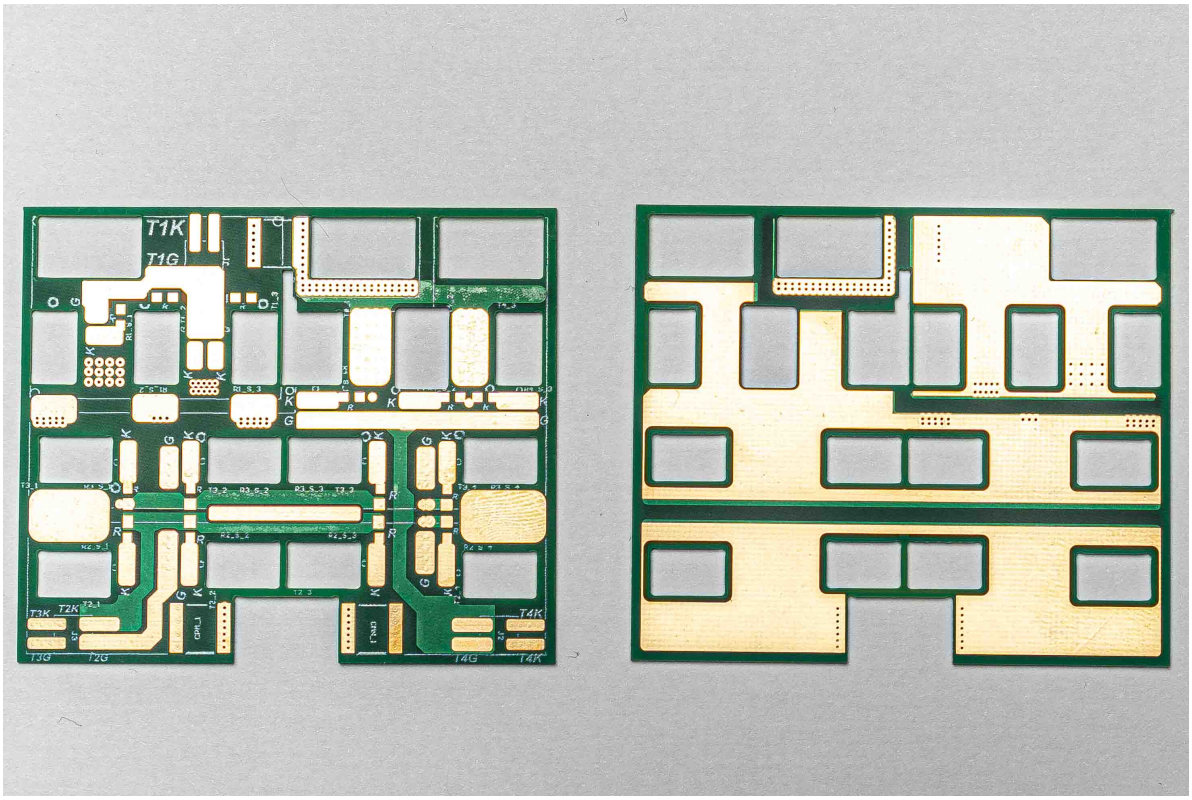

Fig. 5.7: The pattern of designed PCB for the 3L-TNPC power module. Left: top side; Right: bottom side.

voltage rating, and the same semiconductor technology, the 3L-TNPC module (Infineon F3L400-R12PT4P_B26) has a current rating of 400 A, while the 2L configuration (Infineon FS200R12PT4P) is rated at 600*A*. This is because that 3L converters have more switch counts compared to the 2L. Thus it requires more bare die area at the same current rating [19].

To further optimize stray inductance, improving the power density of the power module, this paper designed a high-performance hybrid-structure-based power module for a 3L-TNPC converter. Compared to the existent design, this paper has contributions as follows,

(1) First time to use an improved PCB + DBC hybrid structure to the 3L topology. Through custom PCB design, achieved power loop inductance of 2.5 nH.

(2) Solved issues that PCB is carrying primary current by the proposed current splitter

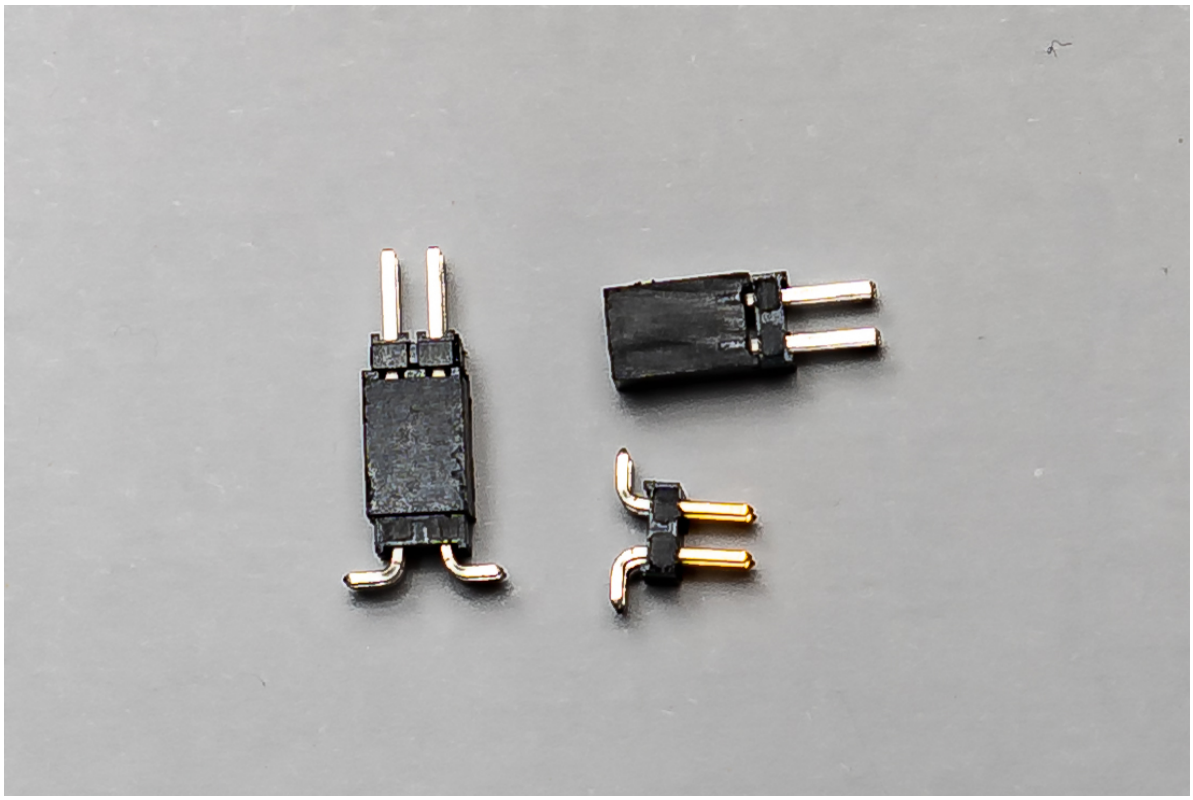

Fig. 5.8: The gate terminal pins used in 3L-TNPC power module.

structure. It allows PCB only to provide transient-support current during switching. The steady-state current only flows through the DBC and PCB vias. Thus the design can be extended to 300 A current rating.

(3) Utilizes PCB for gate loop design and damping of oscillation. Saved space for gate and kelvin source island on DBC, improved power density.

(4) Comprehensively evaluated the design through the double-pulse test, continuous test, and thermal imaging.

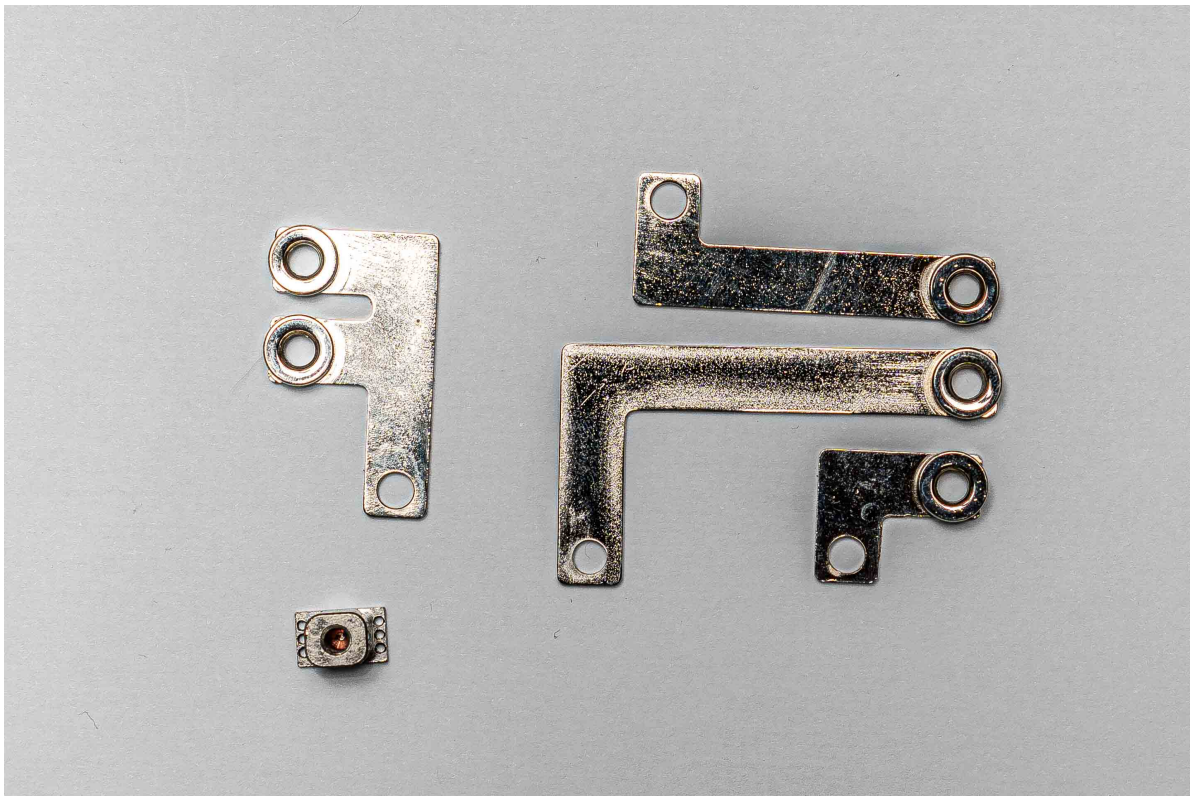

Fig. 5.9: The screw and power tabs designed for 3L-TNPC power module.

5.3 Design of High-performance 3L-TNPC Power Module

5.3.1 Stray inductance in 3L-TNPC converter

One of the phase of the 3L-TNPC topology is as shown Fig. 5.1. The three level converter stands for the three states of output, P-state, O-state, and N-state. They are defined with corresponding switching states as Table 5.1. Compared to two-level (2L) converters, the three output levels of phase-neutral voltage $V_{output-M}$, i.e., $+Vdc/2$, 0, and $-Vdc/2$ can improve current THD and reduce dv/dt during switching. Therefore, it can reduce the size of passives during such as common-mode filters and output filters. Besides, there are two current commutation loops (CCL_1, CCL_2) in a 3L-TNPC phase leg noted in Fig. 5.1.

The target of power-loop optimization is to reduce total inductance in CCL_1 and CCL_2,

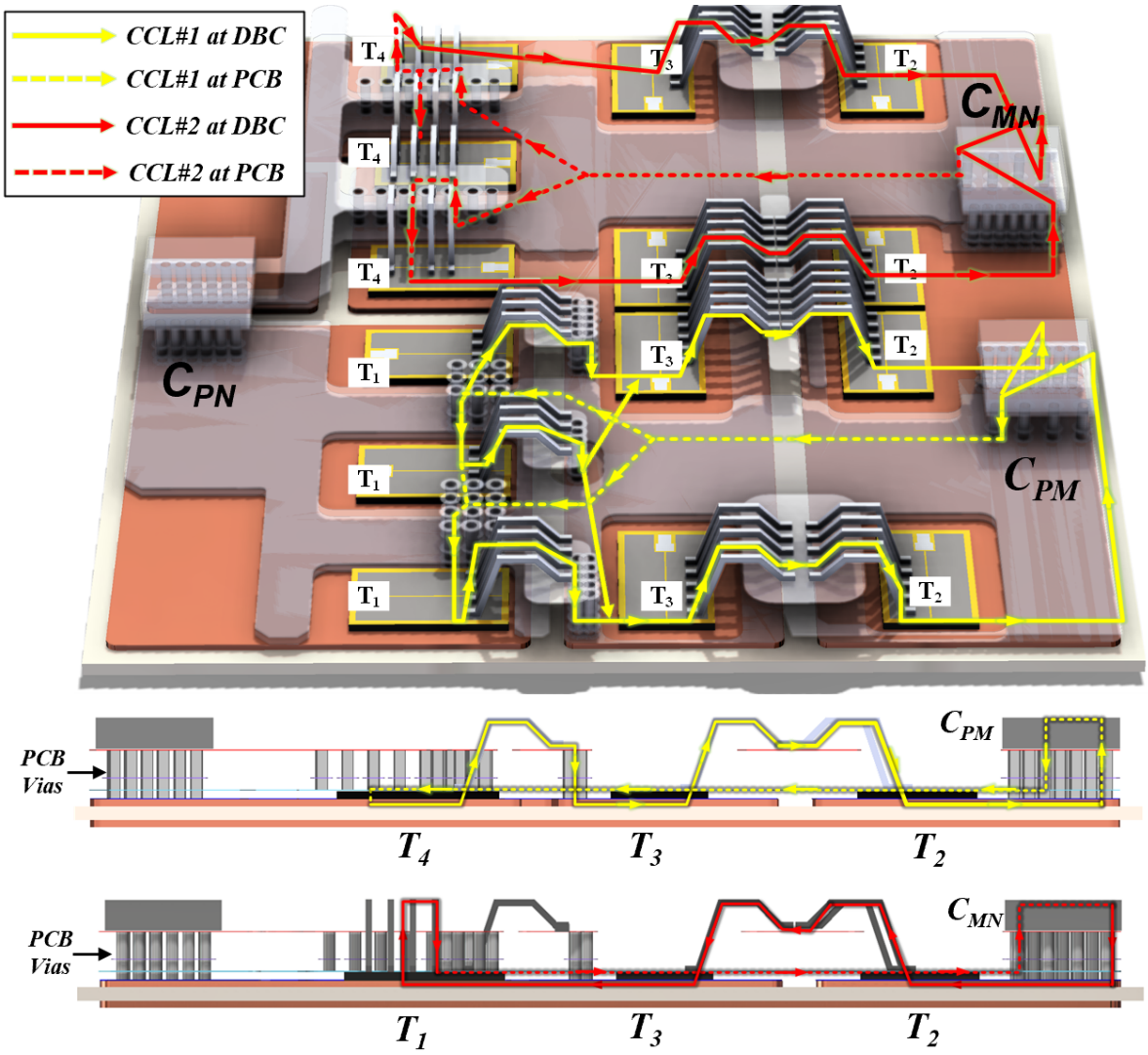

Fig. 5.10: Current commutation loops in designed power module structure.

which are expressed as Eq. 5.2 and Eq. 5.3, respectively. Where $L_{\text{total },\text{CCL}_1}$, and $L_{\text{total },\text{CCL}_2}$ are the total stray inductance of CCL_1 and CCL_2 respectively. L_{D,T_1}, L_{D,T_2}, L_{D,T_4} are the stray inductance from drain terminal of T_1, T_2, and T_4, respectively. L_{S,T_1}, L_{S,T_4} are the source-terminal inductance of T_1, and T_4, respectively. L_{S,T_2T_3} is the stray inductance between T_2 source terminal and T_3 source terminal.

$$L_{\text{total },\text{CCL}_1} = L_{D,T_1} + L_{S,T_1} + L_{D,T_3} + L_{S,T_2T_3} + L_{D,T_2} \tag{5.2}$$

TABLE 5.1: Switching states of 3L-TNPC

State	V_{xN}	S_1	S_2	S_3	S_4
P	$+V_{DC}/2$	ON	ON	OFF	OFF
O	0	OFF	ON	ON	OFF
N	$-V_{DC}/2$	OFF	OFF	ON	ON

$$L_{\text{total ,CCL}_2} = L_{S,T_4} + L_{D,T_4} + L_{D,T_3} + L_{S,T_2T_3} + L_{D,T_2} \tag{5.3}$$

5.3.2 Structure of the proposed power module

The power module is fabricated as Fig.5.3. For better understanding the structure, the module without lid covered is shown as Fig.5.4. And the exploded view of power module is shown as Fig. 5.5. The module is consisting of aluminum nitride (AlN) direct bounding copper (DBC), as shown in Fig. 5.6, PCB, as shown in Fig. 5.7, SiC power bare die, Polylactic acid (PLA) based, 3D-printed housing, customized copper-tube based coldplate, and gate terminal pins (assembled pins and disassembled pins) as shown in Fig. 5.8, and power tabs and their matching screw terminals as shown in Fig. 5.9. Detailed component model numbers, essential parameters, and soldering, bounding materials are listed in table II.

Different types of direct bounding copper are available to choose. For example, most of the commercial IGBT modules used aluminum oxide (Al_2O_3) based direct bounding copper, because of the cheaper price and good mechanical strength. While, aluminum nitride based direct bounding copper shows advantages in thermal conductivity. However, its mechanical strength is less compared to the aluminum oxide direct bounding copper. Beryllium oxide ceramic based direct bounding copper shows even better thermal conductivity. However, it is toxic to human

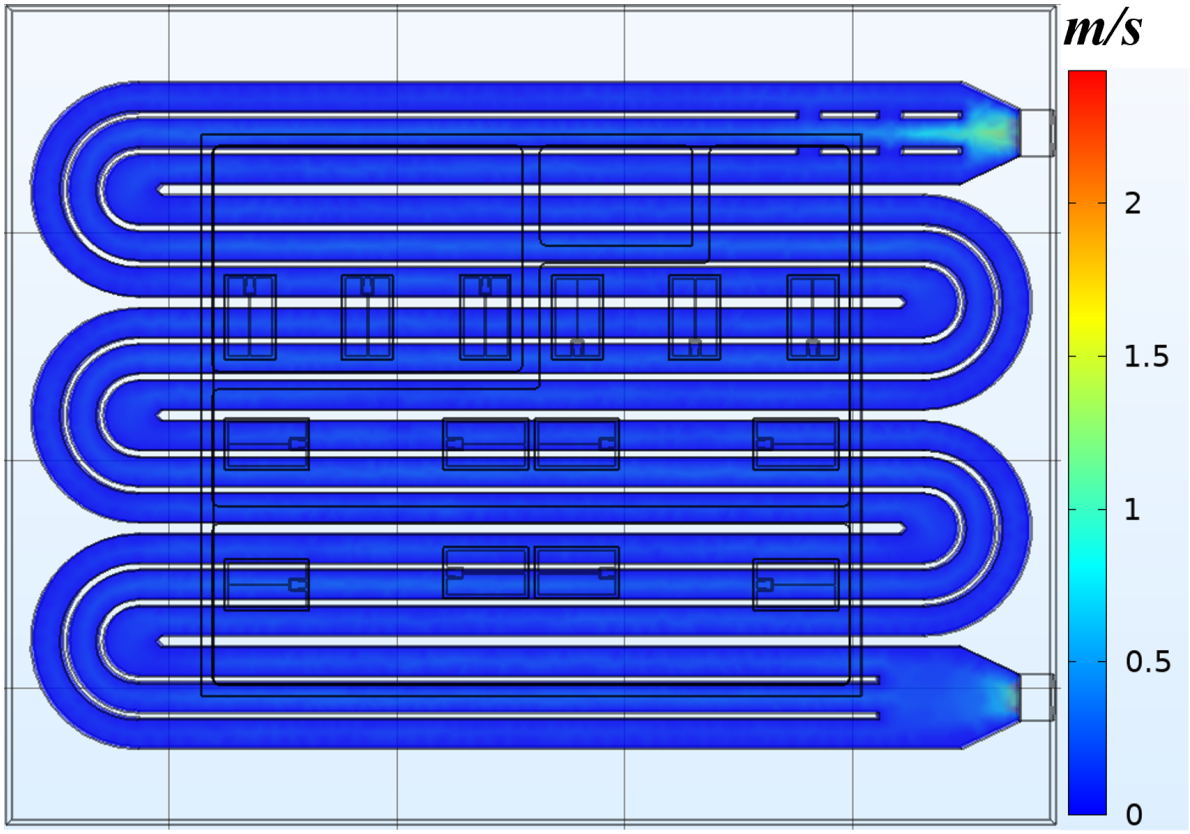

Fig. 5.11: Velocity distribution inside cooling channel under flow pressure of 1.5 psi.

health. And the vapor of beryllium oxide can be easily generated during packaging processing, endangering operators life.

Recently, silicon nitride (Si_3N_4) active metal brazing (AMB) copper shows the improved performance in terms of both mechanical strength and thermal conductivity. Because of the strong mechanical strength, the silicon nitride based active metal brazing board can be used at the thickness about the half of traditional aluminum nitride direct bounding copper. The thinner layer further reduces the thermal resistance, facilitating the thermal conductivity, while keep the mechanical strength similar to the thicker aluminum oxide direct bounding copper board.

Another consideration comes from the coefficient of thermal expansion (CTE). To improve the reliability, it is required that the CTE of substrate closed to the CTE of power bare dies. The

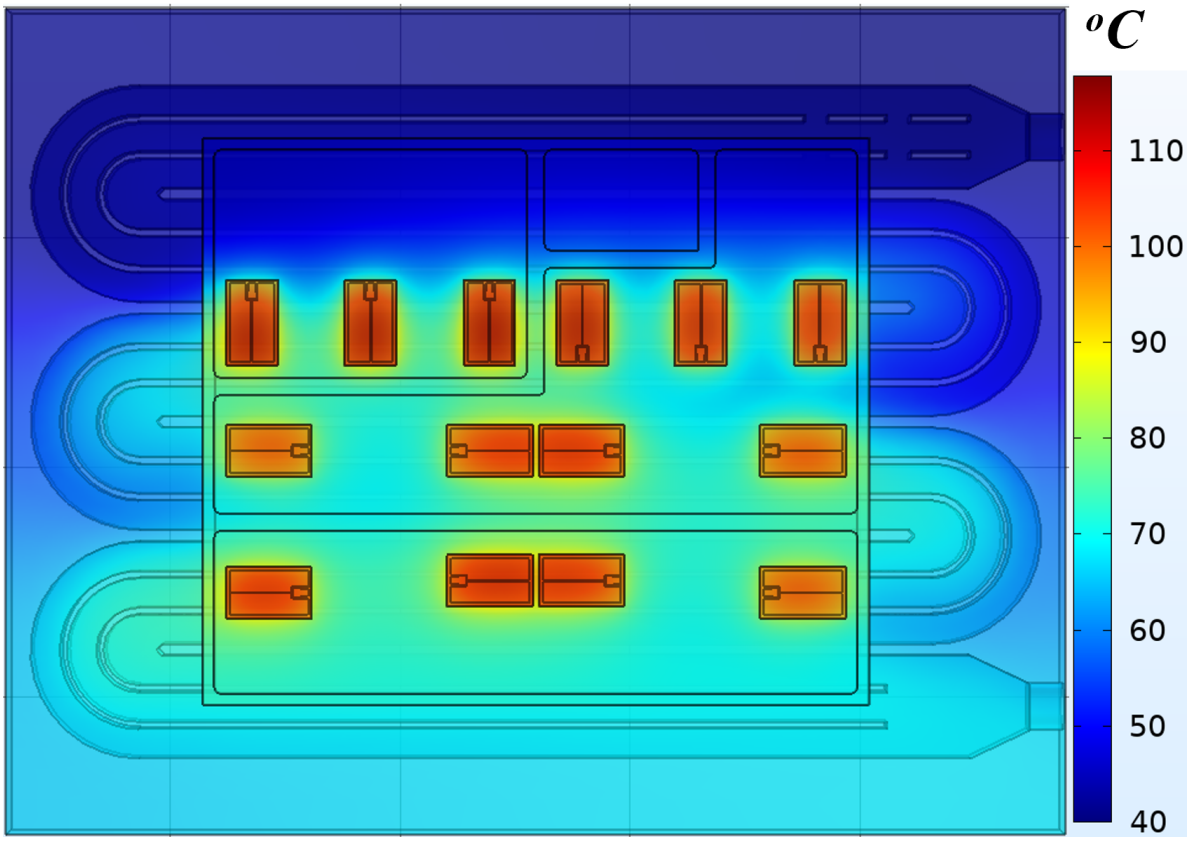

Fig. 5.12: Velocity distribution inside cooling channel under flow pressure of 1.5 psi.

CTE of silicon wafer is $2.6 * 10^{-6}\ ^{o}C^{-1}$, and the silicon carbide wafer is $3.7 * 10^{-6}\ ^{o}C^{-1}$. And the CTE of aluminum oxide direct bounding copper, aluminum nitride direct bounding copper, beryllium oxide direct bounding copper, silicon nitride active metal brazing board are $7.2 * 10^{-6}\ ^{o}C^{-1}$, $4.6 * 10^{-6}\ ^{o}C^{-1}$, , $9.0 * 10^{-6}\ ^{o}C^{-1}$, and $2.8 * 10^{-6}\ ^{o}C^{-1}$, respectively. Therefore, silicon nitride active metal brazing board and aluminum nitride direct bounding copper match to the CTE of silicon carbide wafer the most, which improve the reliability of the power module.

To achieve the optimal performance, the module chooses Wolfspeed third-generation silicon-carbide (SiC) metal oxide silicon field effect transistor (MOSFET) chips, CPM-1200-0013A. Such chip offers lower on-state resistance, which is helpful to reduce the conduction loss on the module. By taking the advantage of wide band-gap device, its switching loss is reduced as well.

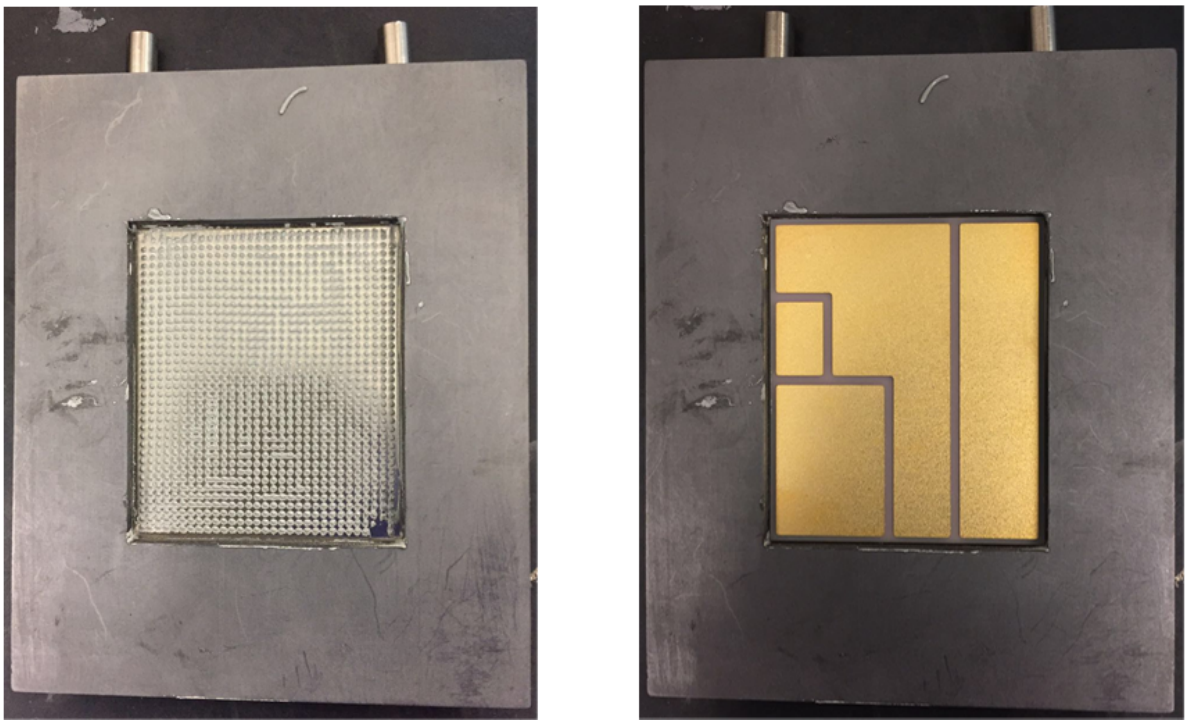

Fig. 5.13: Picture of fabrication process. step I (left), paste screen print on coldplate; and step II (right).DBC placement.

Consequently, the total semiconductor loss can be dropped significantly. As a result, the temperature raise inside the module can be reduced. Moreover, compared to the second-generation device, the third-generation SiC MOSFET improved gate-oxide reliability, and eliminated the aging issue during third-quadrant conduction, when current flows to the body diode. Therefore, Schottky diode can be avoid, which further reduced the design complexity and improve the power density of the power module.

5.3.3 Power-loop optimization

Current commutation loops, CCL_1 and CCL_2 are denoted as Fig. 5.10, where PCB is set as 50% transparency for a better explanation. Embedding the PCB inside the power module also helps with gate loop, including gate-loop inductance minimization through flexible layout, introducing

TABLE 5.2: Components and the material used in packaging the module

Part	Specifications
MOSFET	Wolfspeed CPM3-1200-0013A
Chips	1.2kV 13mΩ, Die size 4.37 x 7.26 mm^2
PCB	1 mm FR4, 1 oz copper, ENIG
Solder 1	100 μm SAC305: $Sn_{96.5}Ag_{3.0}Cu_{0.5}$
Bonding Wire	Aluminum, diameter 5 mil
Substrate	AlN, 48x56.5 mm^2, ENIG, 0.3mm/0.62mm/0.3mm
Solder 2	100 $/mu$m $Pb_{63}Sn_{37}$, liquidus/solidus points 183 ^oC / 151 ^oC
Housing	PLA, 3D printing, 80 x 54 x 13 mm^2
Encapsulation	SEMICOSIL 915 HT, 20 mL, plus ELASTOSIL CAT PT 2 mL
Coldplate	Custom, copper, 70mm x 90mm x 8mm

kelvin resistors to enhance synchronous gate driving, and eliminate quasi-source circulating current for parallel die [27].

The power loop optimization relies on the mutual-inductance cancellation to reduce the module total stray inductance in both CCL_1 and CCL_2. As it can be seen from Fig. 5.10, the design purposely guide the current on PCB with the different direction to the current on DBC. As a result, the mutual inductance is a negative value, which leads to the reduction of total inductance. Meanwhile, since the PCB is closely laminated with DBC, the negative-valued mutual inductance can be magnified.

By performing the power loop optimization, the total stray inductance of CCL_1 and CCL_2

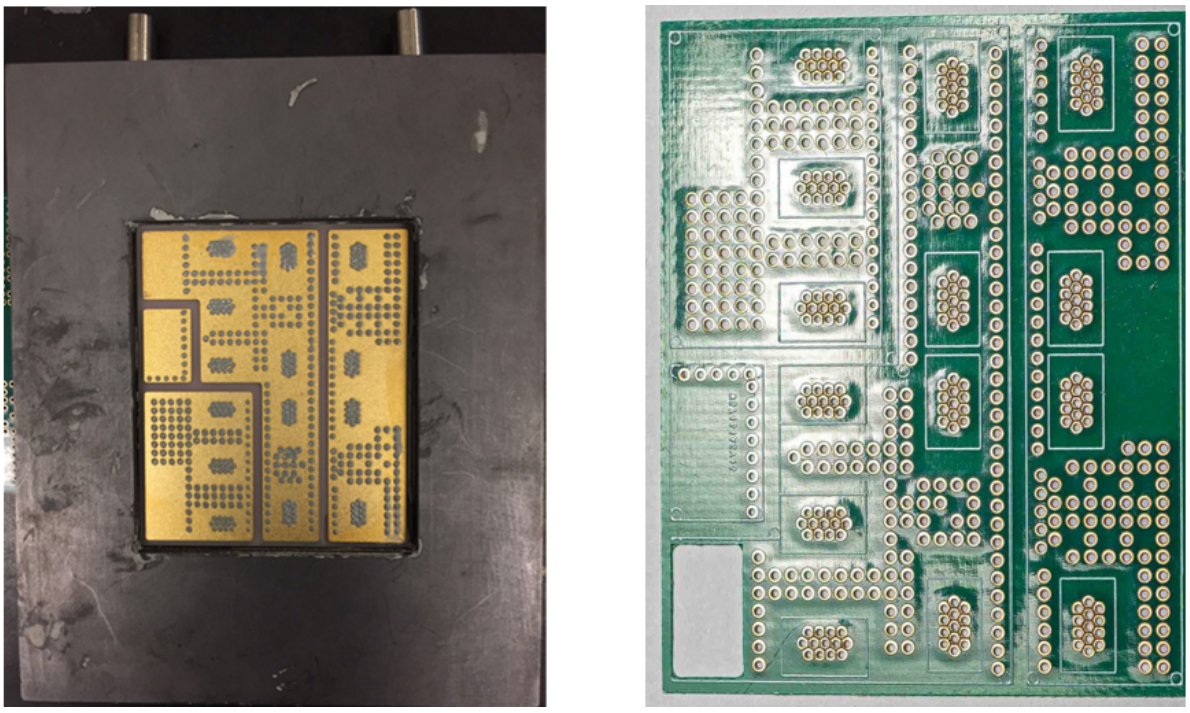

Fig. 5.14: Picture of fabrication process. step III (left), paste screen print on DBC; and the fixture for screen printing in step III. step IV(right) ,PCB placement.

are about 2.47 nH and 2.48 nH based on electromagnetic simulation performed on ANSYS Q3D. Because the symmetric design of power loops in CCL_1 and CCL_2, the stray inductance of the both loops are very similar.

5.3.4 Thermal and flow rate simulation

Comsol multi-physics simulations are performed to evaluate module thermal performance. Because the module is directly soldered with coldplate, the laminar-flow model is used for calculating coolant velocity. The static thermal model is coupled with the fluid-flow model for the estimation of junction temperature. The simulation assumes that the flow rate of the cold plate significantly influence the temperature distribution of the power module, while the impact from power-module temperature to the flow rate of coldplate is ignored.

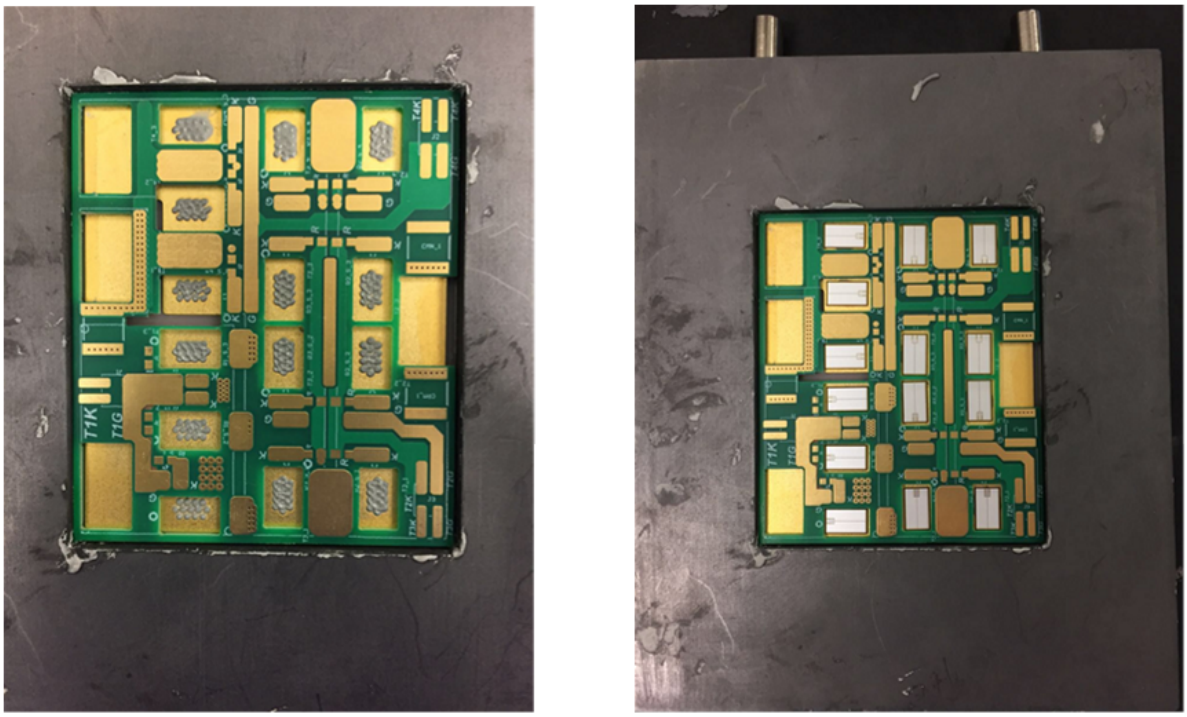

Fig. 5.15: Picture of fabrication process. step IV (left), PCB placement. step V (right), power bare die placement.

The simulation assumes inverter running continuously at 800 V / 400 A with a power factor of 0.8. Under such conditions, the total loss for T_1 and T_4 positions, T_2 and T_3 positions are 147 W per die, and 108 W per die, respectively. By setting the flow pressure of 1.5 *psi*, inlet coolant temperature of 40 ^oC, the thermal conductivity of solder pastes as 57 W/mK, the coolant velocity map is shown as Fig. 5.11. And the temperature map is as Fig. 5.12.

It is seen the coolant velocity are evenly distributed inside the cold plate. Because of the direct soldered colplate, which eliminates the additional thermal resistance introduced from thermal interface material (TIM), the thermal coupling between dies are well controlled. The peak junction temperature is less than 120 ^oC for 800V / 400 A continuous running, leaving 60 ^oC margins to the max working temperature of SiC-MOSFET. Based on the simulation, the junction-to-coolant thermal resistance is 0.27 $^oC/W$.

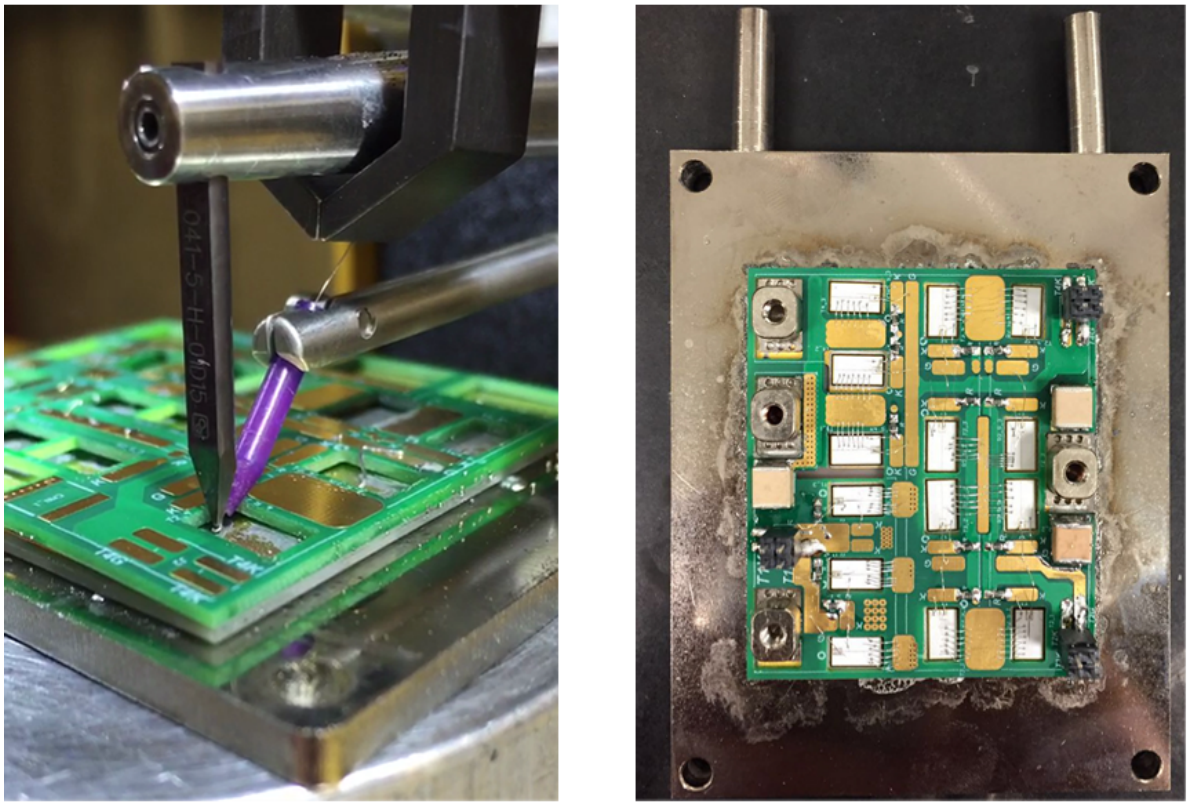

Fig. 5.16: Picture of fabrication process. step VII (left), wire bounding. IX (right): terminal, screw, gate resistor, and multi-layer ceramic capacitor placement.

5.4 Module Fabrication Process

The fabrication procedures are summarized from Fig. 5.13 to Fig. 5.18. The fabrication is using a bottom-to-top sequence. Therefore, step I is to place the coldplate on graphite fixture. And screen print paste on top of the coldplate. Then the direct bounding copper is placed on top of the coldplate in step II, as seen in Fig. 5.13.

Step III is to put the patterned screen print on direct bounding copper, by using the designed screen printer as shown in Fig. 5.14. Then the printed circuit board is placed on top of the direct bounding copper during step IV. And the power bare dies are placed on their corresponding positions in step V, as shown in Fig. 5.15.

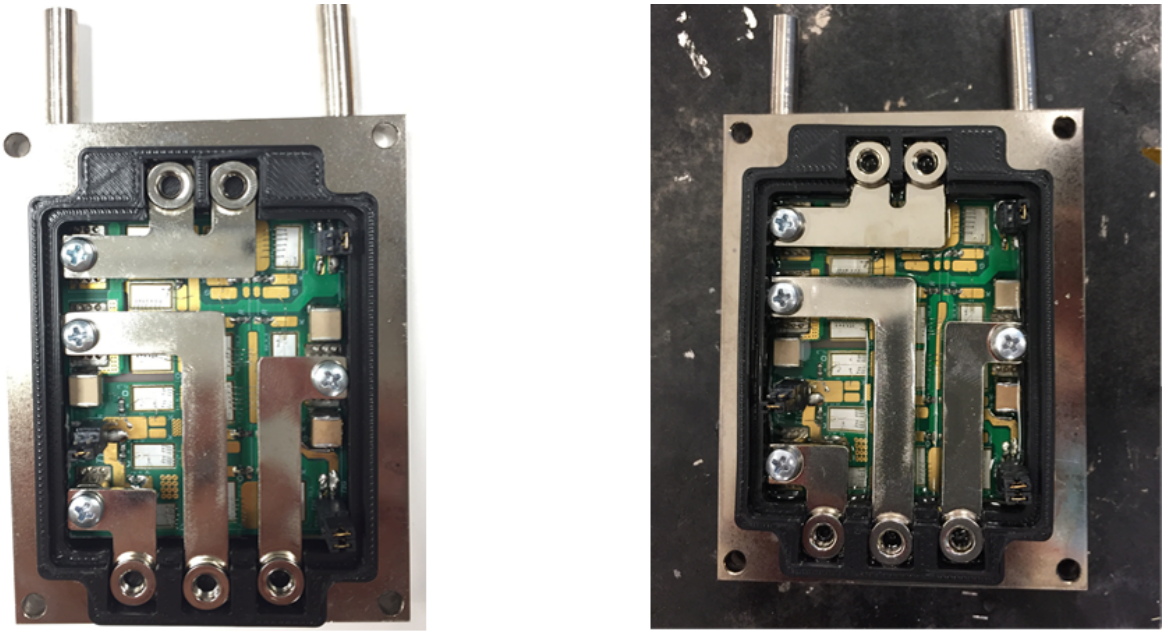

Fig. 5.17: Picture of fabrication process. Step XI (left), housing attachment, terminal installation. Step XII (right), encapsulation.

During step I to step V, all the components are kept aligned at the right position by using the designed graphite fixture. And the coldplate, DBC, printed circuit board and power bare dies are soldered together through reflow oven in step VI. It is necessary to put components on top of the PCB to ensure are well solder.

SAC305 is used as the solder paste for this reflow process. SAC is the abbreviation of Sn/Ag/Cu. Therefore, it is the alloy that contains 96.5 % of tin, 3 % of silver and 0.5 % of copper. Thus, SAC305 is a lead-free alloy and has less harm to human health compared to the soldering material contains lead. Meanwhile, the SAC305 has good fluidity, ensuring solder pasted evenly on the junction. And SAC305 is relatively cheaper compared to other solder materials. Moreover, the solidus temperature of SAC305 is 217^oC, which is above the maximum junction temperature of SiC MOSFETs. And the liquidus temperature of SAC305 is $220\ ^oC$, which is lower than maximum allowable processing temperature of SiC MOSFET. In a conclusion, SAC 305 is a proper soldering

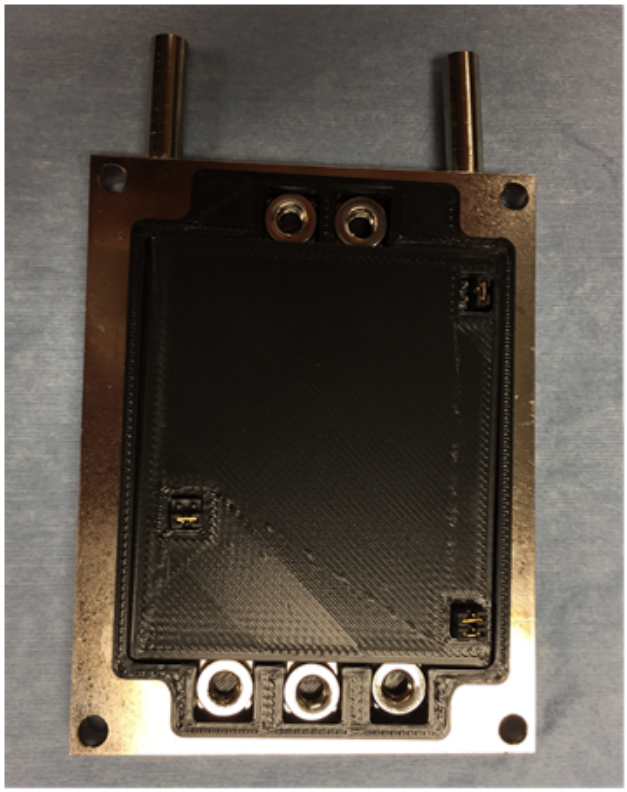

Fig. 5.18: Picture of fabrication process. Step XII, lid placement

material for SiC MOSFET based power module packaging.

Step VII is to place wire bound between power bare die and PCB. The 8 mil aluminum wire bound is used in this application. As seen in Fig. 5.16, typically 6 – 10 wire bounds are placed to connect from PCB to power bare die. After the wire bounding, multi-layer ceramic capacitors, gate resistors, gate terminals and screw nut for power terminals are placed on the corresponding position.

Step VIII is to reflow the multi-layer ceramic capacitor, power screws, gate terminals, gate resistors and printed circuit board on direct bounding coppers. In this step, the solder material is selected as the $Sn_{63}Pb_{37}$. The selected solder material should have liquidus temperature higher than maximum junction temperature of SiC MOSFETs. Moreover, the liquidus temperature should

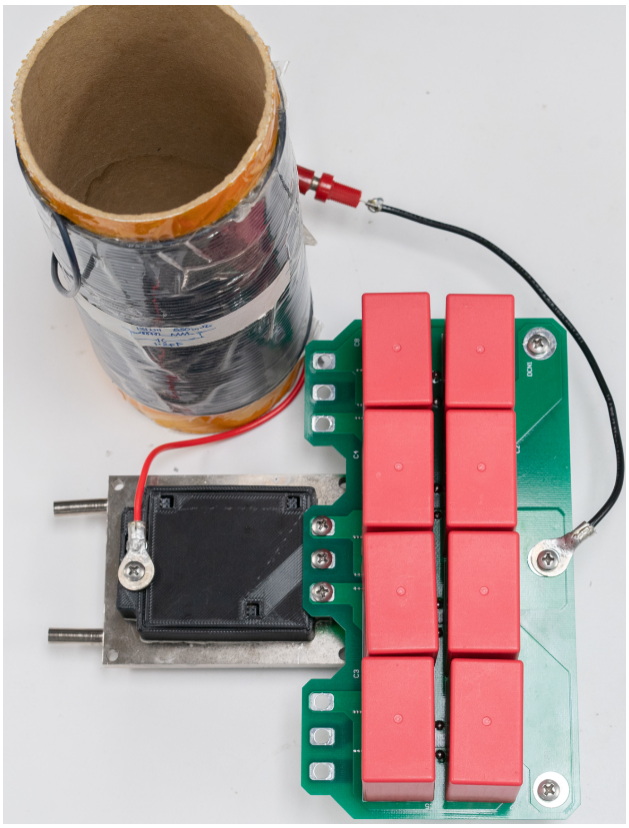

Fig. 5.19: DPT test setup.

be lower than the liquidus temperature of SAC305 to ensure the previous solder paste not melting again. As the $Sn_{63}Pb_{37}$ has solidus temperature of 183 ^oC and liquidus temperature of 210 ^oC, it is proper for this choice.

Step IV is to attach housing on the well soldered materials by using the epoxy glue. And then the busbar tabs are screwed on the power module. M3-sized screws are used to connect the power module, as shown in Fig. 5.17. And typically, the module should be set at least 24 hours for the epoxy glue getting cured. Thereafter, the encapsulation can be pulled intothe module, as shown in Fig. 5.17.

During encapsulation process, air and oxygen can be mixed into the encapsulation, which may degrade the performance of encapsulation. Therefore, pressure chamber is used during encap-

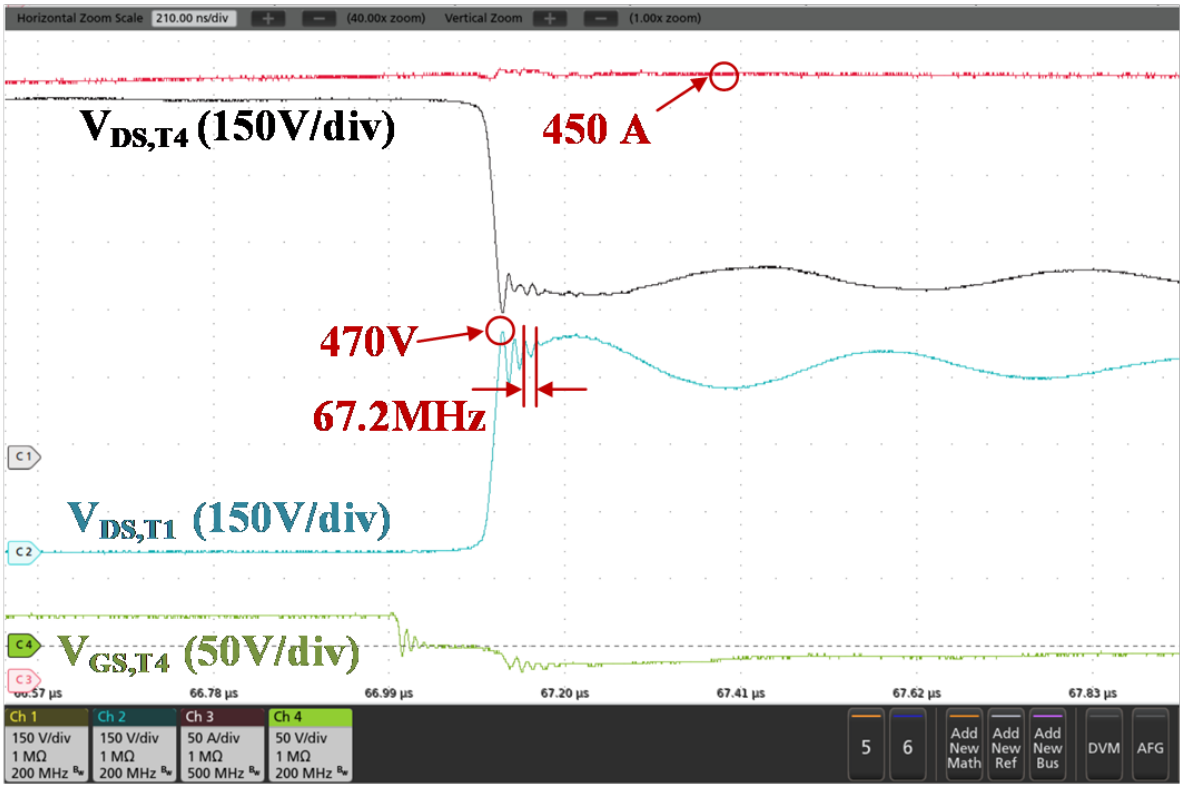

Fig. 5.20: Test waveform captured from DPT at 800V/450A.

sulation. The power module is placed into the pressure chamber and the air bubbles can be pushed out under the decompressed air pressure condition. Lastly, the lid is placed on top of the module, as shown in Fig. 5.18. And the module fabrication process is completed.

5.5 Experiment and Evaluation

The double pulse test (DPT) setup is shown as Fig. 5.19. The drain-to-source voltage of SiC MOSFET, V_{DS}, and gate-to-source voltage of SiC MOSFET, V_{GS}, are measured by high frequency Tektronix high-voltage differential probe, THDP0200. The probes enabled up to 1500 V measurement range, and 200 MHz bandwidth. The inductor current is measured by high-frequency rogowski coil, PEM CWT Mini HF 3.

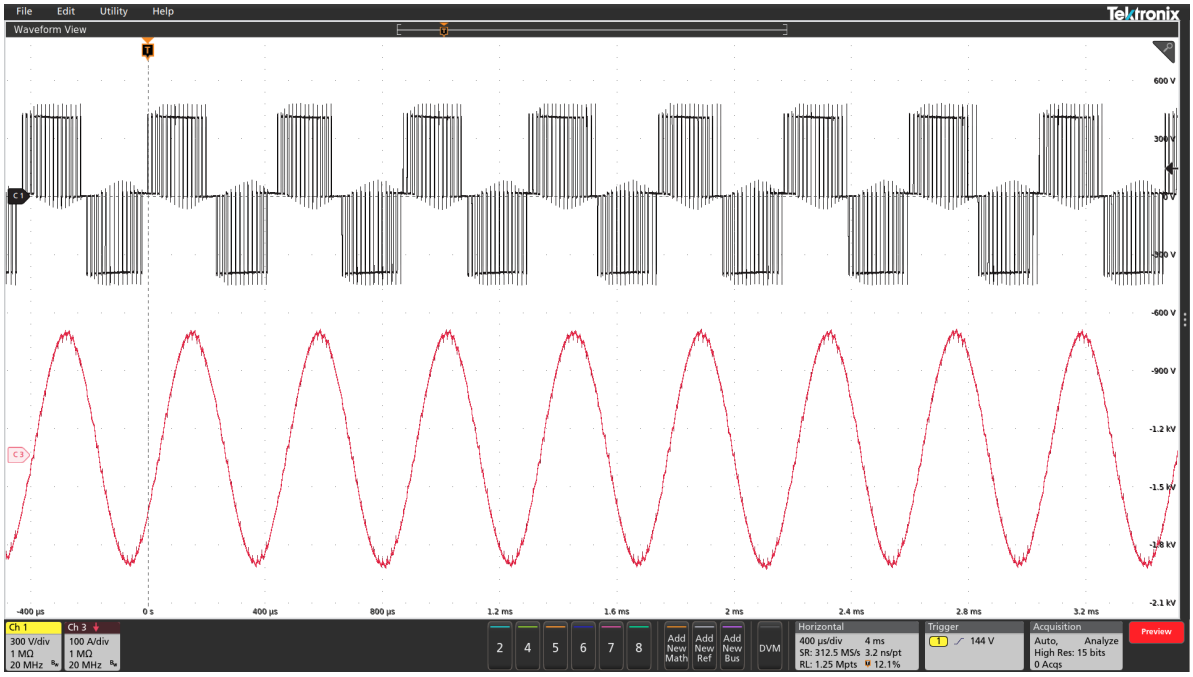

Fig. 5.21: Continuous test waveform at 800V/230A.

The measured waveform are present as Fig. 5.20. Because of the optimized power loop, gate resistance of 0.33 Ω is used to drive the module. Consequently, the dv/dt is $71V/ns$. Based on LT-spice simulation, the switching loss can be reduced by over 71%.

The continuous tests are performed at 800 V / 230 A with waveform captured as Fig.5.21. The case temperature of the power module is captured by the IR camera during the tests, as shown in Fig. 5.22. Efficiency is measured by the temperature difference between inlet and outlet and flow rate, which is estimated as 99.6%.

5.6 Conclusion

The contribution of this paper is summarized as the following. (A) It provides a novel packaging structure for 3L-TNPC power module. (B) Such a structure can effectively solve the major challenge in 3L-TNPC application, which is high stray inductance. (C) The design also

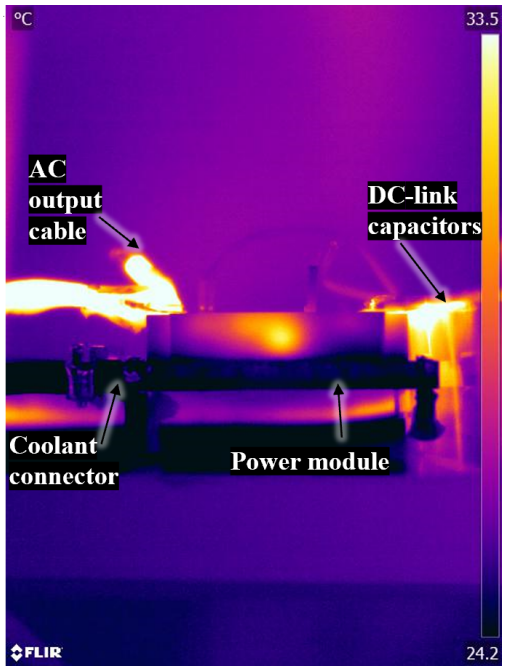

Fig. 5.22: Thermal map captured by IR camera during 800V/230A continuous tests.

provides additional flexibility of power-loop optimization inside the power module. (D) Direct solderable coldplate is used to enhance thermal conductivity by eliminating thermal grease. (E) The module is comprehensively tested and evaluated through double pulse tests up to $800\,V\,/\,450\,A$ with voltage overshoot less than 10% of DC-link voltage, continuous tests up to $800\,V\,/\,230\,A$ with thermal images captured.

5.7 Bibliography

[1] Hassan, Mustafeez U., Zhao Yuan, Hongwu Peng, Asif Imran Emon, Yingzhuo Chen, and Fang Luo. "Model Based Optimization of Propulsion Inverter for More-Electric Aircraft Applications Using Double Fourier Integral Analysis." In AIAA Propulsion and Energy 2020 Forum, p. 3596. 2020.

[2] Deshpande, Amol A., et al. "Modular Three-level T-type Power Electronics Building Block for Aircraft Electric-Propulsion Drives." AIAA Propulsion and Energy 2020 Forum. 2020.

[3] A. Deshpande, Y. Chen, B. Narayanasamy, Z. Yuan, C. Chen and F. Luo, "Design of a High-Efficiency, High Specific-Power Three-Level T-Type Power Electronics Building Block for Aircraft Electric-Propulsion Drives," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 407-416, March 2020, doi: 10.1109/JESTPE.2019.2952367.

[4] H. Peng, Z. Yuan, B. Narayanasamy, X. Zhao, A. Deshpande and F. Luo, "Comprehensive Analysis of Three-phase Three-level T-type Neutral-Point-Clamped Inverter with Hybrid Switch Combination," 2019 IEEE 10th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Xi'an, 2019, pp. 816-821, doi: 10.1109/PEDG.2019.8807618.

[5] H. Peng et al., "Improved space vector modulation for neutral-point balancing control in hybrid-switch-based T-type neutral-point-clamped inverters with loss and common-mode voltage reduction," in CPSS Transactions on Power Electronics and Applications, vol. 4, no. 4, pp. 328-338, Dec. 2019, doi: 10.24295/CPSSTPEA.2019.00031.

[6] B. Liu, R. Ren, F. F. Wang, D. Costinett and Z. Zhang, "Capacitive Coupling in EMI Filters Containing T-Shaped Joint: Mechanism, Effects, and Mitigation," in IEEE Transactions on Power Electronics, vol. 35, no. 3, pp. 2534-2547, March 2020, doi: 10.1109/TPEL.2019.2934478.

[7] Z. Yuan et al., "Design and Evaluation of Laminated Busbar for Three-Level T-Type NPC Power Electronics Building Block With Enhanced Dynamic Current Sharing," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 395-406, March 2020, doi: 10.1109/JESTPE.2019.2947488.

[8] A. Deshpande, Y. Chen, B. Narayanasamy, Z. Yuan, C. Chen and F. Luo, "Design of a High-Efficiency, High Specific-Power Three-Level T-Type Power Electronics Building Block for Aircraft Electric-Propulsion Drives," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 407-416, March 2020, doi: 10.1109/JESTPE.2019.2952367.

[9] S. Igarashi, S. Miyashita, H. Wakimoto, H. Nakazawa and Y. Okuma, "Advanced three-level converter with newly developed 1200V reverse blocking IGBTs," Proceedings of the 2011

14th European Conference on Power Electronics and Applications, Birmingham, 2011, pp. 1-7.

[10] Y. Ren et al., "Voltage Suppression in Wire-Bond-Based Multichip Phase-Leg SiC MOSFET Module Using Adjacent Decoupling Concept," in IEEE Transactions on Industrial Electronics, vol. 64, no. 10, pp. 8235-8246, Oct. 2017, doi: 10.1109/TIE.2017.2714149.

[11] T. Ueda, N. Yoshimatsu, N. Kimoto, D. Nakajima, M. Kikuchi and T. Shinohara, "Simple, compact, robust and high-performance power module T-PM (transfer-molded power module)," 2010 22nd International Symposium on Power Semiconductor Devices IC's (ISPSD), Hiroshima, 2010, pp. 47-50.

[12] P. Beckedahl, S. Buetow, A. Maul, M. Roeblitz and M. Spang, "400 A, 1200 V SiC power module with 1nH commutation inductance," CIPS 2016; 9th International Conference on Integrated Power Electronics Systems, Nuremberg, Germany, 2016, pp. 1-6.

[13] N. Zhu, H. A. Mantooth, D. Xu, M. Chen and M. D. Glover, "A Solution to Press-Pack Packaging of SiC MOSFETS," in IEEE Transactions on Industrial Electronics, vol. 64, no. 10, pp. 8224-8234, Oct. 2017, doi: 10.1109/TIE.2017.2686365.

[14] Z. Liang, "Integrated double sided cooling packaging of planar SiC power modules," 2015 IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, QC, 2015, pp. 4907-4912, doi: 10.1109/ECCE.2015.7310352.

[15] Z. Chen, Y. Yao, D. Boroyevich, K. Ngo and W. Zhang, "An ultra-fast SiC phase-leg module in modified hybrid packaging structure," 2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, 2014, pp. 2880-2886, doi: 10.1109/ECCE.2014.6953789.

[16] R. Wang, Z. Chen, D. Boroyevich, L. Jiang, Y. Yao and R. Kaushik, "A novel hybrid packaging structure for high-temperature SiC power modules," 2011 IEEE Energy Conversion Congress and Exposition, Phoenix, AZ, 2011, pp. 333-338, doi: 10.1109/ECCE.2011.6063788.

[17] C. Chen, Y. Chen, Y. Li, Z. Huang, T. Liu and Y. Kang, "An SiC-Based Half-Bridge Module With an Improved Hybrid Packaging Method for High Power Density Applications," in IEEE Transactions on Industrial Electronics, vol. 64, no. 11, pp. 8980-8991, Nov. 2017, doi: 10.1109/TIE.2017.2723873.

[18] M. Schweizer, I. Lizama, T. Friedli and J. W. Kolar, "Comparison of the chip area usage of 2-level and 3-level voltage source converter topologies," IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society, Glendale, AZ, 2010, pp. 391-396, doi: 10.1109/IECON.2010.5674994.

[19] F. Electric, "Datasheet of 4MBI300VG-120R-50 " Fuji Electric Europe, 2020. [Online]. Available: https://www.fujielectric-europe.com/downloads/4MBI300VG-120R-$50_1$734830.*PDF*.[*Accessed* : $26 - Oct - 2020$].

[20] Semikron, "SEMiX405TMLI12E4B " Power Modules and Systems, Semikron,

2020. [Online]. Available: https://www.semikron.com/products/product-classes/igbt-modules/detail/semix405tmli12e4b-21919490.html. [Accessed: 26-Oct-2020].

[21] Infineon, "F3L400R12PT4PB26" IGBT Modules, Infineon, 2020. [Online]. Available: https://www.infineon.com/cms/en/product/power/igbt/igbt-modules/f3l400r12pt4p$_b$26/.[$Accessed : 26-Oct-2020$].

[22] Semikron, "SKiM401TMLI12E4B" Power Modules and Systems, Semikron, 2020. [Online]. Available: https://www.semikron.com/products/product-classes/igbt-modules/detail/skim401tmli12e4b-23918950.html. [Accessed: 26-Oct-2020].

[23] Infineon, "F3L200R12N2H3B47" IGBT Modules, Infineon, 2020. [Online]. Available:https://www.infineon.com/cms/en/product/power/igbt/igbt-modules/f3l200r12n2h3$_b$47/.[$Accessed : 26-Oct-2020$].

[24] Vincotech, "VINcoMNPC X4" Vincotech, 2020. [Online]. Available: https://www.vincotech.com/products/product-details/70-W212NMA600NB02-M200P62.html. [Accessed: 26-Oct-2020].

[25] J. L. Lu and D. Chen, "Paralleling GaN E-HEMTs in 10kW–100kW systems," 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, 2017, pp. 3049-3056, doi: 10.1109/APEC.2017.7931131.

6 Conclusion and Future Work

6.1 Conclusion

This dissertation discussed the hardware design and optimization of the motor drive for more-electric aircraft applications. To improve the converter performance, the dissertation utilized a model-based design method for an optimal paper design of the power converters. Based on the paper design, this dissertation investigates the method to choose optimal power semiconductors by discussing the impacts of such parameters at the converter level. The dissertation explicitly explains the method of busbar design. Because of the complicated structure of the busbar, the dissertation splits the busbar design into two chapters, focusing on conduction layer design and insulation structure design, respectively.

Spending many efforts on busbar optimization gains a lot, such as lower stray inductance than the published paper for busbar in three-level converters. The lower stray inductance enabled faster-switching speed, resulting in much lower switching loss. Besides, careful design of the busbar insulation structure helps the system avoid partial discharge during high-altitude and low air-pressure conditions.

The dissertation is also expressing one of the design philosophies: optimize the converter at the power-module level. The author of this dissertation has noticed the significant performance improvement through design the converter at the power-module level. For example, five-fold reduced stray inductance, much higher power density, and notably improved thermal conductivity.

Chapter 2 of this dissertation introduced the design procedure of power converter for more-electric aircraft applications. The chapter explained the method of model-based converter design in

order to deliver the optimal paper design of the converter. Such paper design is the fundamental and basis of the hardware design. The remaining design steps are illustrated to provide a comprehensive and high-level understanding of converter design. The overall structure of the 450 kVA motor drive is introduced in this chapter as well.

Chapter 3 provided the design guidance for the conduction layer of the laminated busbar. This is step-by-step design guidance, which targets on minimizing the stray inductance of busbar, limiting the temperature difference between parallel power switch through improving the dynamic current sharing among them. The guidance utilizes a three-level t-type neutral-point-clamped converter as a design instance. Furthermore, the guidance is comprehensively examined and evaluated through electromagnetic simulations, circuit-level simulations, double-pulse tests, and continuous tests with thermal imaging.

Chapter 4 focused on the insulation structure design of the laminated busbar. It is known that partial discharge can shorten the converter lifetime, reduce converter reliability, and cause converter malfunction through insulation break down. This paper provided a comprehensive structural analysis of the busbar and found the most-stress insulation condition by considering the non-defects busbar and the busbar with defects such as voids and delamination. The insulation design is based on the most-stress condition to guarantee partial-discharge free under such circumstances. Meanwhile, the inductance-and-insulation trade-off is modeled quantitatively to help the designer choose the proper insulation thickness

Finally, chapter 5 introduced a design of a 1200 V, 300A power module for three-level t-type neutral-point-clamped topology. The power module utilizes a printed-circuit-board plus direct-bounding copper structure, which achieves the low stray inductance through magnetic cancellation. The directly soldered coldplate also helps improve thermal conductivity by reducing

thermal interface material and mitigates thermal coupling.

6.2 Future Work

This dissertation has investigated converter design from several aspects and revealed the trade-off between the insulation and stray inductance, between stray inductance and thermal resistance. However, there are additional design trade-offs that should be considered and modeled. For example,

1. The trade-off between common-mode noise and thermal conductivity;
2. The trade-off between stray inductance and parasitic capacitance;
3. The trade-off between the insulation and parasitic capacitance.

The optimal hardware design can be achieved by understanding all the design trade-offs and purposely choose a design space with a proper balance of such trade-offs.

In chapter 5, the dissertation focuses on the electrical performance of the designed module. The reliability of the power module should be further investigated before moving the design to the market.

In the end, all the researches are motivated by pursuing the optimal performance of converters. The research has not included the consideration such as costs, marketing factors such as marketing demands. The proposed method may eventually increase the product cost by increasing product development time and introducing additional components, such as a printed circuit board in the power module. Nevertheless, those costs can be mitigated and averaged through massive production. In comparison, the overall saving can be predicted because of improved efficiency and power density.

7 Appendix

This appendix shows the testing equipment's used to measuring the waveform and performance characterization

1. Oscilloscope: Tektronix, MSO58 series and MSO 56 series
2. Probes used in the tests:
    a. High-voltage differential probe: THDP0100.
    b. Rogowski coil: CWT MiniHF 3, CWT Ultra-mini 1, and CWT 3.
    c. Current transformer: Pearson 4100.
    d. High-voltage single-ended probe: TPP0850.
3. Impedance characterization:
    a. Impedance analyzer: KEYSIGHT E4990A.
    b. Vector network analyzer: KEYSIGHT E5061B.

A List of published and submitted work

1. Z. Yuan et al., "Design and Evaluation of Laminated Busbar for Three-Level T-Type NPC Power Electronics Building Block With Enhanced Dynamic Current Sharing," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 395-406, March 2020, doi: 10.1109/JESTPE.2019.2947488.

2. Z. Yuan et al., "Design and Evaluation of A 150 kVA SiC MOSFET Based Three Level TNPC Phase-leg PEBB for Aircraft Motor Driving Application," 2019 IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA, 2019, pp. 6569-6574, doi: 10.1109/ECCE.2019.8913071.

3. Yuan, Zhao, et al. "Insulation Design and Optimization of Laminated Busbar for More Electric Aircraft Motor Driver under High Altitude and Depressurized Environments." AIAA Propulsion and Energy 2020 Forum. 2020.

4. H. Peng, Z. Yuan, B. Narayanasamy, X. Zhao, A. Deshpande and F. Luo, "Comprehensive Analysis of Three-phase Three-level T-type Neutral-Point-Clamped Inverter with Hybrid Switch Combination," 2019 IEEE 10th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Xi'an, 2019, pp. 816-821, doi: 10.1109/PEDG.2019.8807618.

5. R. Whitt et al., "Heat Transfer and Pressure Drop Performance of Additively Manufactured Polymer Heat Spreaders for Low-Weight Directed Cooling Integration in Power Electronics," 2019 18th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm), Las Vegas, NV, USA, 2019, pp. 451-455, doi: 10.1109/ITHERM.2019.8757275.

6. A. Deshpande, Y. Chen, B. Narayanasamy, Z. Yuan, C. Chen and F. Luo, "Design of a High-Efficiency, High Specific-Power Three-Level T-Type Power Electronics Building Block for Aircraft Electric-Propulsion Drives," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 407-416, March 2020, doi: 10.1109/JESTPE.2019.2952367.

7. J. Ke et al., "Investigation of Low-Profile, High-Performance 62-mm SiC Power Module Package," in IEEE Journal of Emerging and Selected Topics in Power Electronics, doi: 10.1109/JESTPE.2020.2971623.

8. B. Narayanasamy, H. Peng, Z. Yuan, A. I. Emon and F. Luo, "Modeling and Analysis of a Differential Mode Active EMI Filter With an Analog Twin Circuit," in IEEE Transactions on Electromagnetic Compatibility, vol. 62, no. 4, pp. 1591-1600, Aug. 2020, doi: 10.1109/TEMC.2020.3006427.

9. Z. Wang, Y. Wu, M. H. Mahmud, Z. Yuan, Y. Zhao and H. A. Mantooth, "Busbar Design and Optimization for Voltage Overshoot Mitigation of a Silicon Carbide High-Power Three-Phase T-Type Inverter," in IEEE Transactions on Power Electronics, vol. 36, no. 1, pp. 204-214, Jan. 2021, doi: 10.1109/TPEL.2020.2998465.

10. B. Narayanasamy and F. Luo, "Design and implementation of a novel differential mode active EMI filter with a twin circuit," *2019 IEEE International Symposium on Electromagnetic Compatibility, Signal Power Integrity (EMC+SIPI)*, New Orleans, LA, USA, 2019, pp. 241-246. doi: 10.1109/ISEMC.2019.8825210

11. B. Narayanasamy, H. Jalanbo and F. Luo, "Development of software to design passive filters for EMI suppression in SiC DC fed motor drives," *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Blacksburg, VA, 2015, pp. 230-235. doi: 10.1109/WiPDA.2015.7369320

12. B. Narayanasamy, F. Luo and Y. Chu, "High density EMI mitigation solution using active approaches," *2017 IEEE International Symposium on Electromagnetic Compatibility Signal/Power Integrity (EMCSI)*, Washington, DC, 2017, pp. 813-818. doi: 10.1109/ISEMC.2017.8077979

13. B. Narayanasamy, F. Luo and Y. Chu, "Modeling and Stability Analysis of Voltage Sensing based Differential Mode Active EMI Filters for AC-DC Power Converters," *2018 IEEE Symposium on Electromagnetic Compatibility, Signal Integrity and Power Integrity (EMC, SI PI)*, Long Beach, CA, 2018, pp. 322-328. doi: 10.1109/EMCSI.2018.8495239

14. A. Deshpande, B. Narayanasamy and F. Luo, "Analysis of conducted EMI in Si IGBT + SiC MOSFET hybrid switch based converters," *2018 IEEE International Symposium on Electromagnetic Compatibility and 2018 IEEE Asia-Pacific Symposium on Electromagnetic Compatibility (EMC/APEMC)*, Singapore, 2018, pp. 127-127.

15. A. Deshpande, Y. Chen, B. Narayanasamy, A. S. Sathyanarayanan and F. Luo, "A three-level, T-type, power electronics building block using Si-SiC hybrid switch for high-speed drives," *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, 2018, pp. 2609-2616. doi: 10.1109/APEC.2018.8341385

16. Y. Yan, Z. Wang, C. Chen, Y. Kang, Z. Yuan and F. Luo, "An Analytical SiC MOSFET Switching Behavior Model Considering Parasitic Inductance and Temperature Effect," 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, 2020, pp. 2829-2833, doi: 10.1109/APEC39645.2020.9124548.

17. Whitt, Reece, Huitink, David, Hudson, Skyler, Nafis, Bakhtiyar, Yuan, Zhao, Narayanasamy, Balaji, Deshpande, Amol, Luo, Fang, Imran, Asif, Clarke, Zion, and Smith, Sonya. "Additive Manufactured, Low EMI, Non-Metallic Convective Heat Spreader Design and Optimization." Proceedings of the ASME 2019 International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems. Anaheim, California, USA. October 7–9, 2019. V001T06A015.

18. Z. Wang, Z. Wu, C. Chen, Y. Kang, Z. Yuan and F. Luo, "GaN Devices Based Integrated Two-Stage DC-DC Converter with Voltage Regulation," 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, 2020, pp. 2219-2224, doi: 10.1109/APEC39645.2020.9124549.

19. A. I. Emon, B. Narayansamy, H. Peng, Mustafeez-ul-Hassan, Z. Yuan and F. Luo, "Investigation of Power Converter's Near Field EMI Containment Using Passive Filters," 2020 IEEE International Symposium on Electromagnetic Compatibility Signal/Power Integrity (EMCSI), Reno, NV, USA, 2020, pp. 398-403, doi: 10.1109/EMCSI38923.2020.9191648.

20. H. Peng, B. Narayanasamy, A. I. Emon, Z. Yuan, R. Zhang and F. Luo, "Selective Digital Active EMI filtering using Resonant Controller," 2020 IEEE International Symposium on Electromagnetic Compatibility Signal/Power Integrity (EMCSI), Reno, NV, USA, 2020, pp. 632-639, doi: 10.1109/EMCSI38923.2020.9191623.

21. A. I. Emon, B. Narayanasamy, T. M. Evans, F. Luo and H. A. Mantooth, "Modeling and Analysis of Near-Field Radiated Emission in Wide Bandgap Power Modules," *2019 International Symposium on Electromagnetic Compatibility - EMC EUROPE*, Barcelona, Spain, 2019, pp. 333-338. doi: 10.1109/EMCEurope.2019.8871481

22. Deshpande, Amol A., Yingzhuo Chen, Balaji Narayanasamy, Zhao Yuan, and Fang Luo. "Modular Three-level T-type Power Electronics Building Block for Aircraft Electric-Propulsion Drives." In AIAA Propulsion and Energy 2020 Forum, p. 3595. 2020.

23. Hassan, Mustafeez U., Zhao Yuan, Hongwu Peng, Asif Imran Emon, Yingzhuo Chen, and Fang Luo. "Model Based Optimization of Propulsion Inverter for More-Electric Aircraft Applications Using Double Fourier Integral Analysis." In AIAA Propulsion and Energy 2020 Forum, p. 3596. 2020.