HEAT ROUTING WITH LIQUID-VAPOR PHASE CHANGE PHENOMENA IN MICROSCALE POROUS MEDIA

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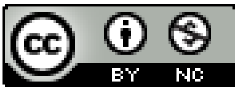

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Abstract

As electronic devices continue to miniaturize in size and grow in system complexity, conventional thermal management techniques must evolve to gradually include the concept of not merely heat dissipation, but controllable heat routing. To optimize lifetime reliability and overall device performance, many applications benefit from isothermalization within a narrow temperature window. Such devices often experience heat generation and environmental conditions that are transient and/or spatially variant, however, creating undesirable thermal profiles that cannot be addressed by constant heat removal strategies. Proper thermal management of such systems therefore benefits from the introduction of nonlinear thermal components that can exhibit properties such as heat flow transformation, thermal switching, and thermal isolation. This work examines the use of liquid-vapor phase change phenomena as a mechanism for controllable heat routing.

First, we examine the use of liquid-vapor phase change as a heat spreading mechanism. Vapor chambers or flat plate heat pipes have long existed as effective heat flow transformers used to reduce highly concentrated local heat fluxes before heat rejection to an external sink. Conventional vapor chamber materials are not coefficient of thermal expansion matched to semiconductor device materials, however, necessitating the use of intermediary thermal interface materials that act as bottlenecks to the overall system performance. We present the concept of a miniature silicon-based vapor chamber for die-matched heat spreading, and demonstrate that the vapor transport can effectively improve the die-level temperature uniformity even over relatively small (~1 x 1 cm^2) spreading areas. Due to the miniature volume of the device, we also develop an analytical model to predict the effect of liquid charge on the thermal resistance, and find the performance to be sensitive to be within ± 2 μL.

Second, we purposefully introduce a non-condensable gas (NCG) to act as a diffusion barrier to the vapor transport. In a one-dimensional transport scenario, the binary vapor/NCG diffusion process creates a highly nonlinear, temperature dependent thermal resistance that can act as a passive thermal regulator. We perform measurements

of the steady state thermal characteristics with varying amounts of NCG charge and find it to be an effective mechanism for tuning the regulatory properties of the device. We present an analytical model that captures the temperature dependent behavior of the binary diffusion process, and perform a parametric optimization to a resistance switching ratio of up to 14 in response to varying levels of heat input.

Third, we examine the implications of thermal capacitance when assessing the effectiveness of various thermal regulatory schemes. We perform transient measurements of the binary diffusion based regulator in response to pulsed heating inputs to characterize the thermal response time. We find that the diffusion process creates a phenomena where the temperature difference across the device becomes clamped to a constant, relatively heat flow independent value above a threshold temperature. When subjected to transient heat loads, this manifests in an asymmetric device response time, where the low resistance state approaches the steady state value rapidly, and the high resistance state is amplified over the steady state value.

Finally, we examine the more fundamental aspects of heat transfer during liquid to vapor phase change in microscale porous media. We leverage the highly ordered structure of inverse opal metal films to examine the limitations of capillary-fed evaporation and boiling in the porous wicks that drive the heat and mass transfer in device level heat routing applications. We find that maintaining the contact angle stability of the metal wicks is crucial for long term reliability and stable performance, and present results from different surface treatment schemes to generate various hydrophilic nano/microstructures.

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Chapter 1

Introduction

This section provides background and motivation for the work encapsulated in this dissertation. It presents some of the thermal management challenges in modern electronics cooling, and introduces vapor chambers and thermal regulators/switches as heat routing mechanisms to address some of those challenges.

1.1 Challenges in electronics cooling

The semiconductor industry has sustained rapid performance growth over the past few decades, largely following the scaling trends predicted by Moore's Law [1]. As applications become increasingly power-dense and space constrained [2], however, thermal challenges have risen to the forefront as critical issues that potentially inhibit future performance improvement. The heat generation in various electronics components is often spatially and/or temporally variant, leading to localized hotspots or large temperature swings that can drastically decrease device reliability [3] or lead to outright failure from thermal runaway [4] if left unchecked.

Traditional cooling solutions have primarily targeted the goal of constant heat dissipation, where an active cooling technology is used to remove the largest amount of heat possible from the system. Hotspot heat fluxes can range from the order of 0.1-1 kW/cm^2 [5,6] and typically require extremely effective active heat removal strategies with heat transfer coefficients in the range of 10,000 $Wm^{-2}K^{-1}$ or higher to maintain junction temperatures within operating limits [7]. A variety of active thermal management strategies have been developed in literature to achieve these high rates of heat removal, including microcontact Peltier coolers [8], jet impingement [9], embedded microchannels [10,11], and microgap coolers [12]. While effective, these active removal strategies frequently require additional components to function such as external power supplies, liquid pumps, and heat exchangers, etc., creating significant burdens on overall system cost and complexity [13].

1.2 Vapor chamber heat spreaders

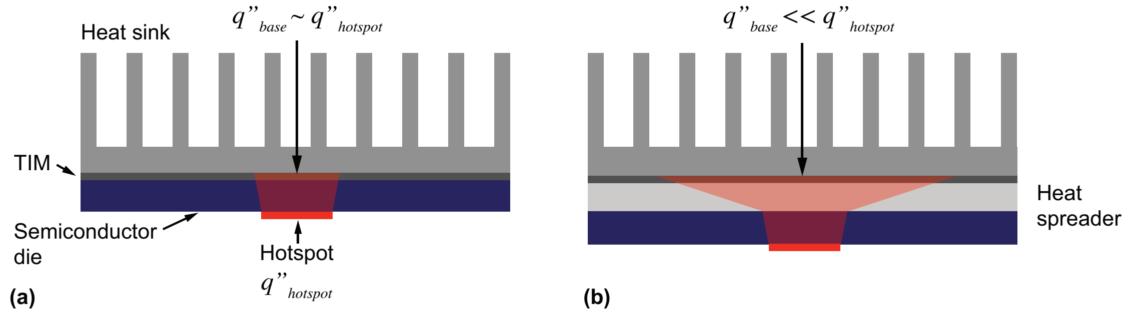

Figure 1-1. (a) A simplified representation of a semiconductor packaging scheme without a heat spreading layer. The heat flux experienced at the heatsink base is comparable to the heat flux generated at the hotspot. (b) A semiconductor packaging scheme with a high thermal conductivity heat spreading layer added between the die and the heat sink. The heat spreader greatly reduces the heat flux experienced at the heat sink base, relaxing the heat sink cooling requirements.

The use of an intermediary heat spreader layer between the heat source and sink can mitigate many of the challenges associated with hotspot cooling mentioned in the previous section. Figure 1-1(a) shows a simplified representation of a semiconductor packaging scheme where heat generated at a localized hotspot is cooled by a heat sink attached to the top of the semiconductor die. If no significant heat spreading occurs, the heat flux experienced at the base of the heat sink is comparable to the hotspot heat flux, and the heat sink must have a sufficiently high heat transfer coefficient to dissipate the concentrated heat flux to maintain a reasonable junction temperature at the die. As Figure 1-1(b) shows, however, the addition of a high thermal conductivity heat spreader layer between the die and the heat sink can substantially reduce the heat flux by the time the heat flow reaches the heat sink base, relaxing the heat removal requirement for the heat sink. Overall, the primary goal of an effective heat spreader is to provide impedance matching between the level of heat generation at the hotspot with the existing system-level cooling capability.

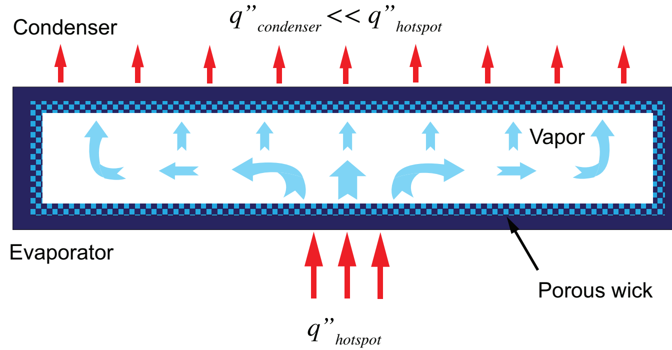

Figure 1-2. Cross-sectional schematic of operating principles of a vapor chamber. Heat generation at the heat source causes liquid in the evaporator wick to evaporate, spread through the vapor core, then condense back into liquid over the entire condenser side wick area. The condensed liquid recirculates to the hotspot through capillary action in the porous wick and creates a passive cycle of liquid-vapor phase change. The vapor spreading in the core typically occurs with minimal temperature drop and provides the high effective thermal conductivity region of the device.

Vapor chambers are high performance heat spreaders that utilize liquid-vapor phase change to achieve effective thermal conductivities often much higher than that of solids. Figure 1-2 shows a general schematic detailing the operating principles of a vapor chamber. A vapor chamber is formed from a hermetically sealed cavity typically lined with a porous wicking material. The entire cavity is charged with a fixed amount of working fluid and evacuated of all non-condensable gases to create a saturated environment within the chamber. As heat is supplied to the evaporator side of the device, the liquid in the porous wick evaporates, spreads throughout the vapor core, then condenses back into liquid upon reaching the condenser side wick. The vapor core provides the extremely high thermal conductivity portion of the device. With the exception of ultra-thin vapor chambers [14], the vapor spreading typically occurs with minimal pressure drop (and subsequent temperature drop), creating a nearly isothermal core region. The range of effective thermal conductivity values reported in literature for the core are on the order of 20,000 $Wm^{-1}K^{-1}$ or above [15].

The porous wick on the evaporator side of the vapor chamber plays a critical function in the overall device performance. The evaporator wick must fulfill the simultaneous functions of providing a high enough capillary pressure to drive fluid flow to the hotspot, while maintaining a low viscous pressure drop to avoid capillary-limited dryout. While various other operating limits exist for heat pipes and vapor chambers, including the sonic, entrainment, and boiling limits, the capillary limit is typically the dominant operational limit for vapor chambers [16].

The permeability of a porous material, K is roughly proportional to the square of the medium's characteristic length scale [17], or

$$K \propto \delta^2 \tag{1.1}$$

Depending on the composition of the porous material, the definition of the characteristic length scale varies. The permeability of sintered copper wicks comprised of packed particles, for example, depends primarily on the particle size [18], while inverse porous materials are more commonly defined by a characteristic pore size [19]. The capillary pressure of the wick, however, is typically proportional to the inverse of the characteristic length scale, or

$$P_c \propto \frac{1}{\delta} \tag{1.2}$$

This conflicts with the desired scaling trend for enhancing permeability. Additionally, the wick should ideally have a low thermal resistance to minimize the temperature drop between the vapor chamber wall and vapor region. As the heat must pass through the porous wick before reaching the high effective thermal conductivity vapor core, the evaporator wick resistance often acts as a thermal bottleneck for the entire vapor chamber. A majority of the evaporation in porous microstructures has been demonstrated to occur from a thin liquid film region near the three-phase contact line on the order of 1-10 μm thick [20–22]. Increasing the surface area to volume ratio is

therefore an important consideration in wick design to maximize the area available for evaporation from the thin liquid film region [23]. Overall, the simultaneous goals of achieving a low evaporator wick resistance while maximizing the capillary-limited dryout heat flux create a multi-objective design problem. Biporous and/or hierarchical porous structures have emerged as promising solutions, where wicks with two or more dominant feature sizes can be tuned to optimize multiple wick parameters at once [24–26].

The condenser side of a vapor chamber must fulfill two primary design considerations: a satisfactory mechanism must exist for returning liquid to the evaporator side wick, and condensation should ideally occur without the formation of a high thermal resistance, bulk liquid film. A few different approaches can be taken to achieve these goals. In a completely capillary driven vapor chamber, the condenser side is also lined with a porous wick that delivers liquid back to the evaporator side wick and prevents bulk liquid film formation. The thermal resistance across the condenser wick is not as critical as the heat is spread over the entire wick area as opposed to the evaporator side hotspot, so the condenser wick dimensions may differ from the evaporator wick dimensions. More important in this case is for the viscous pressure drop across the condenser side wick to be minimal compared to the evaporator wick pressure drop in order to reduce the contribution to the capillary dryout limit. An alternative to avoid the issue of condenser side viscous pressure drop while still maintaining a low condensation resistance is to combine microstructured surfaces with chemical patterning to create superhydrophobic surfaces for jumping droplet liquid return [27–29]. The maximum heat flux in jumping droplet liquid return may be sensitive to the entrainment limit, however, as well as condensate transport distance constraints when the jumping must take place against gravity [30].

Vapor chamber and heat pipes have traditionally been fabricated out of metals such as copper or aluminum due to their relatively high inherent thermal conductivities and associated ease of machining and manufacturing [31–33]. Metals, however, tend of have significantly higher coefficients of thermal expansion (CTE) compared with most semiconducting materials, which necessitates the use of mechanically compliant thermal

interface materials (TIMs) between the die and vapor chamber. A significant portion of the total temperature drop in the system can occur across these TIMs, which can minimize the overall benefit of having a high performance vapor chamber heat spreader. From a packaging perspective, therefore, there is great interest in exploring vapor chambers fabricated out of non-traditional materials that can achieve better CTE matching with semiconductor die.

1.3 Thermal regulators and switches

In addition to the use of passive heat spreading mechanisms to ease system level cooling constraints, a relatively newer approach to thermal management explores the capability of nonlinear thermal devices for controllable heat routing [34]. Electric vehicle batteries, for instance, operate most efficiently within a narrow temperature band but frequently experience large fluctuations in environmental conditions [35]. Ideally, a battery pack would be insulated during cold-start conditions to leverage internal heat generation to preheat the pack [36], then have efficient cooling in a hot environment to prevent overheating. These contrasting thermal management conditions can be realized through the implementation of a thermal regulator or switch, where the thermal resistance between the battery and external sink can be varied depending on the environmental temperature [37,38]. Similar strategies could be implemented for electronics cooling, where the heat generation is frequently spatially and/or temporally non-uniform. As an example, Yang et al. successfully used a liquid metal thermal switch to isothermalize two different GaN power transistors located on the same PCB [39]. A thermal regulator placed in parallel with a temperature sensitive component could also be used to block heat flow during regular operation, then act as a low resistance shunt to divert heat flow and prevent temperature swings during transient power spikes.

Conversely, thermal regulation may also be utilized to purposefully amplify the temperature difference within a system. Thermal energy harvesters, for example, demonstrate increased energy efficiency when operating with pulsed heating inputs [40–42]. When naturally occurring pulsed inputs are unavailable, appropriate thermal regulator usage can convert constant heat sources into oscillating heat sources [34].

Through all of the aforementioned applications, a critical opportunity emerges for the implementation of high performance thermal devices that can dynamically respond to variations in environmental and operational thermal loads.

The standard figure of merit used to evaluate the effectiveness of a thermal regulator design is the switching ratio, where

$$S_R = \frac{R_{OFF}}{R_{ON}} \tag{2.3}$$

The off-state resistance R_{OFF} is ideally as high as possible to minimize unwanted heat leakage through the regulator, and the on-state resistance R_{ON} should be as low as possible to minimize the temperature drop across the regulator itself.

Many different physical mechanisms have been leveraged to create devices with switchable and nonlinear thermal resistance behavior. One common method to create a switchable resistance is through making or breaking mechanical contact between the heat source and sink [43]. The contact can be initiated through active mechanisms such as the application of an electric field [44], or passive mechanisms such as differential thermal expansion induced flexing [45] and contraction/expansion from thermal strain recovery in shape memory alloys [37]. Phase or structural transitions in solid-state materials can also lead to changes in thermal conductivity that can be utilized for passive thermal regulation [46–49]. Polyethylene nanofibers, for instance, have demonstrated reversible thermal conductance changes with a 10x switching ratio during structural transitions between ordered and disordered phases [50]. Additional regulation schemes that can demonstrate highly variable thermal resistances include microscale gas-gap switches (primarily suitable for cryogenic applications [51]) or liquid-vapor phase change in the form of gas-loaded heat pipes [52] and highly nonlinear boiling heat transfer coefficients [53].

With many of these existing regulation mechanisms, however, the switching temperature range is typically fixed and difficult to tune without modifying the material composition of the regulator. Regulators actuated with active mechanisms such as electric fields can be switched freely, but require external components that add additional system complexity. Thermal management systems can therefore greatly benefit from the addition

of passive, versatile thermal regulators with resistance switching characteristics that can be easily tuned for a wide range of operating scenarios.

1.4 Organization and scope of work

Chapter 1 introduces the challenges associated with thermal management in space-constrained and power dense applications. Two potential methods are introduced to address some of these challenges: vapor chambers as effective heat spreaders to reduce system-level cooling constraints, and thermal regulators/switches to controllably route heat as opposed to constant heat dissipation.

Chapter 2 presents a review of silicon-based vapor chamber technology for integrated packaging schemes, as opposed to traditional copper/metal-based vapor chambers. We describe several of the challenges associated with the design and large-scale manufacturing of silicon-based devices, as well as unique opportunities for performance enhancement enabled by the precision of silicon micromachining processes.

Chapter 3 examines the performance of a miniature (1x1 cm^2 condenser area) silicon vapor chamber for die-level heat redistribution. The vapor core and evaporative/condenser wicking structures are fabricated through a novel lithography-free ultra violet (UV) laser ablation process. We also develop a semi-analytical model to predict the effect of liquid charge volume on the overall device performance and benchmark with respect to the heat spreading capabilities of solid silicon.

Chapter 4 introduces a novel thermal regulation mechanism that leverages binary vapor diffusion through a non-condensable gas cavity to create a passive, tunable thermal resistance switching mechanism. We present a steady-state characterization of the device performance and demonstrate that the resistance characteristics of the device can be easily varied through modulation of the non-condensable gas pressure. The device also exhibits behavior analogous to an electrical varistor, where the temperature difference across the regulator becomes clamped to a relatively heat-flow independent value above a certain threshold. An analytical model is derived for the steady-state switching behavior,

and a parametric optimization study is performed to increase the steady-state switching ratio to as high as 14.

Chapter 5 investigates the transient device behavior of the thermal regulator developed in chapter 4. We examine the various device components that dominate the transient thermal response, and characterize the device resistance switching in response to pulsed heating inputs. Through an experimentally validated model, we determine that the majority of the device transient response is dominated by sensible heat storage in the solid device volume. The thermal time constant of the device is characterized to be on the order of seconds, with some variation depending on the effective heat transfer coefficient of the cold side heat sink. Based on the transient response and steady-state switching ratio data, we discuss the applicability of this novel thermal regulation mechanism for temperature control in future systems.

Chapter 6 summarizes the primary findings of the dissertation, and places them in the context of broader research in the field. Additional opportunities and research directions are proposed for future thermal management schemes utilizing liquid-vapor phase change phenomena.

Chapter 2

Challenges and Opportunities with Silicon Vapor Chambers

This chapter provides a review and perspectives on the potential of silicon-based vapor chambers for use as high performance, integrated heat spreaders in future packaging schemes. Large portions of this chapter have been taken from T. Liu, et al., "Review of Silicon-based Vapor Chambers: State of Technology and Perspectives," (manuscript in preparation).

2.1 Vapor chamber material options

Traditional vapor chambers and spreaders are typically fabricated out of copper due to ease of manufacturing and the high thermal conductivity of solid copper (though this can depending on the fabrication process). Copper, however, has a much larger CTE compared to most semiconductor substrate materials used in electronic devices today. The CTE mismatch between the die and heat spreader is therefore a large source of stress generation in a typical package [54], necessitating the use of mechanically compliant but poor thermal conductivity thermal interface materials.

A summary of various materials and their linear thermal expansion coefficients at room temperature is given in Table 2-1. As seen in the table, common semiconductor substrate materials such as Si, GaN, and SiC all have similar linear coefficients of thermal expansion in the 2-4 ppm/K range, while metals such as Cu and Al have much larger CTE values greater than 15 ppm/K. Various studies in literature have therefore explored the fabrication of vapor chambers with walls formed from lower CTE materials to achieve better expansion matching in the semiconductor material range. Ju et al., for example, used aluminum nitride ceramic plates (CTE of 4.5 ppm/K) to form the vapor chamber walls, with internal wick structures formed from copper particles sintered to direct bonded copper layers on top of the ceramic [55]. Altman et al. fabricated a vapor

chamber from CuMo (CTE ~8 ppm/K) laminated substrates bonded to a copper frame [56]. Titanium also has been used as a novel vapor chamber material due to its lower CTE (~8.5 ppm/K) and compatibility with micromachining processes [57].

Table 2-1. Coefficients of linear thermal expansion at room temperature for various materials.

Material	CTE [ppm/K]	Source
Silicon	2.6	[58]
Gallium Nitride	2.8	[59]
Silicon Carbide	3.8	[60]
Copper	17	[61]
Aluminum	24	[61]
Diamond	0.8	[62]
Titanium	8.5	[63]

Based on the values in Table 2-1, however, silicon naturally emerges as the vapor chamber material candidate with the best CTE matching to various semiconductor substrates. Vadakkan et al. demonstrated through simulation that using a silicon vapor chamber in place of a standard copper lid could reduce the compressive stress in the die by as much as 96% [64]. From a packaging perspective, this creates the potential for new configurations utilizing better bonding interfaces between the die and the vapor chamber, or direct integration of silicon vapor chamber components into the die substrate as part of a streamlined process flow. Fabricating vapor chambers out of silicon brings a fresh set of challenges, as the vapor chamber dimensions are limited by the size of available silicon wafers, and traditional manufacturing approaches that have been well-established for metal vapor chambers are incompatible with silicon wafer processing. Silicon-based

vapor chamber fabrication can benefit, however, from the large array of precision silicon micromachining processes developed in the last few decades for MEMS and CMOS devices. The micron-scale precision of these processes creates many additional opportunities for thermo-fluidic optimization of the vapor chamber performance, particularly in terms of porous wick design.

2.2 Packaging opportunities with silicon vapor chambers

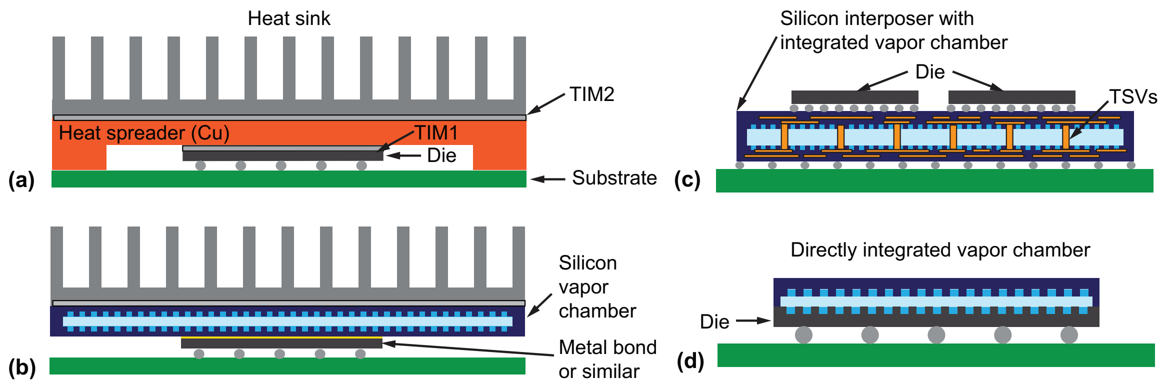

Figure 2-1. (a) A traditional packaging scheme with a solid copper spreader or copper vapor chamber. (b) A potential packaging scheme with a silicon vapor chamber as the heat spreader, where a lower resistance metal bond could be used for die attach. (c) Another possible configuration where a future silicon interposer has an integrated vapor chamber to spread heat between multiple die. (d) A directly integrated vapor chamber with evaporator wicking structures fabricated directly onto the backside of the die, eliminating the need for any thermal interface layer between the die and spreader.

Perhaps the simplest compelling use case scenario for a silicon vapor chamber can be envisioned by comparing a traditional microprocessor package with a copper heat spreader, as shown in Figure 2-1(a), with the various other packaging scenarios enabled by a silicon vapor chamber. As mentioned in the previous section, the thermal interface material between the die and copper spreader, typically referred to as TIM1, must be mechanically compliant to accommodate the CTE mismatch within the package. If the metal lid is replaced by a silicon vapor chamber as shown in Figure 2-1(b), however, the requirement for mechanical compliance could potentially be relaxed in lieu of lower

thermal resistance interfaces with the die. Eutectic die attach or similar could be utilized to achieve high thermal conductivity, minimal bond line thickness interfaces between the die and vapor chamber [65–67].

Another potential implementation of a silicon vapor chamber could be as shown in Figure 2-1(c). Solid silicon interposers with through silicon vias (TSVs) are widely accepted as cost-effective methods for creating power-efficient interconnects in multichip packages [68,69]. Though silicon can lead to higher electrical losses compared to organic and glass substrates [70], using an interposer with a higher thermal conductivity can play a significant role in reducing the overall package thermal resistance [71]. Packaging architectures where the heat primarily goes through the substrate may therefore benefit from higher thermal performance interposers such as the one shown in Figure 2-1(c), where a future interposer could form a self-contained silicon vapor chamber. Choice of a high dielectric strength working fluid would be important to ensure electrical isolation of TSVs that would have to transcend the vapor core, and fabrication would certainly be more challenging than existing solid interposers. As packages become increasingly thermally limited, however, such architectures may be worthwhile considerations.

Finally, yet another packaging opportunity with a silicon vapor chamber could be as shown in Figure 2-1(d), where evaporative wicking structures are etched directly into the solid substrate of the die. This approach would eliminate any thermal bottleneck associated with intermediary thermal interface materials, bringing the heat spreading as close to the heat generation sources as possible. A complete vapor chamber could be formed by then bonding a cap condenser wafer on top of the die. The condenser cap could either be larger than or equal to the die area depending on the heat source areas under consideration. While a larger condenser area equates with more heat spreading area, die-matched directly integrated vapor chambers may be simpler from a fabrication standpoint, enabling wafer-level matching of condenser cap and device wafers.

2.3 Scaling considerations for relevant thermofluidic phenomena

In this section, we present a brief overview of common modeling assumptions for heat and mass transport in vapor chambers. The relative importance of various physical mechanisms is assessed in terms of relevant dimensionless numbers and length scales.

To promote the capillary driven liquid circulation in a vapor chamber, the porous wicks typically contain feature sizes on the order of a few hundred microns or less. With these length scales, the Bond number, or ratio of gravitational forces to surface tension forces is typically much less than 1. Vapor chambers have demonstrated functionality with up to 10 g of gravitational loading without failure [5], though excessive working fluid pooling over the condenser can decrease the effective thermal conductivity compared to standard gravity conditions [72]. At the liquid-vapor interface, the Capillary number (ratio of viscous to surface tension forces) and Weber number (ratio of inertial to surface tension forces) are also typically much less than 1 [20]. The approximation of a constant meniscus shape is frequently used in modeling of evaporation from the wick liquid-vapor interfaces, though the possibility of Marangoni driven instabilities exists if the degree of superheat is high enough [73]. The liquid flow through the porous wick is laminar (with Reynolds numbers typically less than or equal to 10), and can be approximated with a porous medium approach [74]. The thermal resistance of the porous wick is frequently calculated with a conduction approximation [15] justified by the static meniscus assumption and low liquid velocities within the wick [75].

Within the vapor cavity, the vapor flow is typically modeled as laminar, and both compressible and incompressible approaches have been used to varying degrees of accuracy [16]. The effect of natural convection on heat transfer from the wick surface can usually be neglected, as the natural convection thermal resistance ($\sim 10^{-2}$ m^2-K/W) is typically orders of magnitude higher than the liquid-vapor interfacial resistance ($\sim 10^{-6}$ m^2-K/W) [20,75]. Similarly, we estimate thermal resistances due to conduction across the vapor cavity ($\sim 10^{-2}$ m^2-K/W) and radiation with a linearized heat transfer coefficient

(~10^{-1} m^2-K/W) as significantly larger than and negligible compared to the interfacial resistances.

2.4 Summary of existing silicon vapor chambers

2.4.1 Heat spreading configurations

Before we begin the discussion of existing silicon vapor chamber efforts in literature, a distinction must be made between silicon vapor chambers and silicon micro heat pipes. Silicon micro heat pipes were among the earliest passive, two-phase heat transport devices proposed for direct integration with semiconductor dies. The micro heat pipe concept was first presented by Cotter in 1984 as a convex, cusped groove where the mean curvature of the liquid-vapor interface is comparable to the inverse of the hydraulic radius for flow in the groove [76]. Multiple grooves may also be etched in an array to increase the heat transfer area. Since the initial conceptualization, a range of micro heat pipes have been fabricated in silicon wafers through various silicon etching techniques [77]. The key difference between silicon vapor chambers and silicon micro heat pipes, however, is in the heat transport configuration. In a micro heat pipe, evaporation takes place at one end of the grooves, and condensation takes place at the opposing end, typically with a 1:1 heated area to condenser area ratio. The heat pipe primarily serves as a high thermal conductivity one-dimensional heat transport mechanism, and not a spreader. The devices considered in this review of silicon vapor chamber technology will therefore consist only of silicon-based devices that rely on liquid-vapor phase change for heat spreading purposes. Figure 2-2(a) shows an example of a heat pipe used for one-dimensional heat transport, versus vapor chambers used in planar (Figure 2-2(b)) and radial (Figure 2-2(c)) spreading configurations. Silicon vapor chambers can leverage much of the manufacturing progress demonstrated from silicon micro heat pipe literature, but present a unique set of considerations due to the different heat transport geometry.

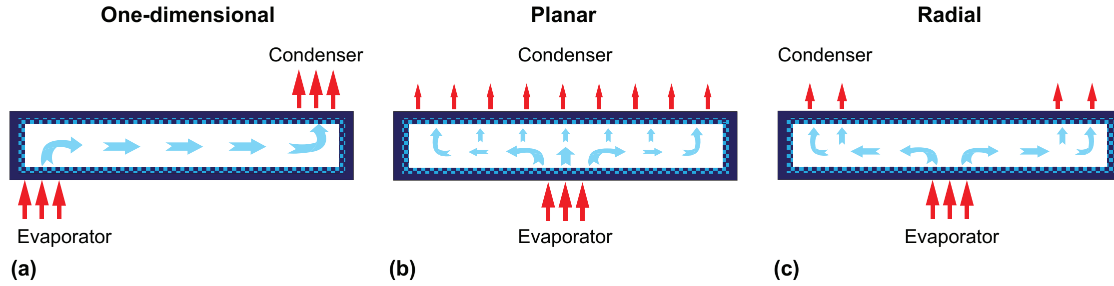

Figure 2-2. (a) Heat pipe operation with one-dimensional heat transport. (b) A two-dimensional heat planar spreading configuration with a vapor chamber, where heat rejection occurs over the entire face opposite of the evaporator. (c) A two-dimensional radial heat spreading configuration with a vapor chamber.

2.4.2 Heat spreading performance of silicon vapor chambers

Unlike heat pipes with one-dimensional heat flow, an effective thermal conductivity cannot be readily defined for vapor chambers without comparative numerical simulations due to the two-dimensional nature of the heat spreading. Cai et al. fabricated a silicon device meant for use as a vapor chamber, but experimentally characterized it as a one-dimensional heat pipe to more easily obtain an effective thermal conductivity value [78]. It is important to note that the effective thermal conductivity value calculated in this scenario (2500 $Wm^{-1}K^{-1}$) [78], however, cannot be applied to the device performance if used as a vapor chamber due to the different heat flow configurations involved. A direct comparison of the relative performance of various silicon vapor chambers is also difficult as the different form factors and hotspot to condenser area ratios lead to different innate spreading resistances. The performance of vapor chambers reported in literature is therefore often presented based on a relative comparison to a benchmark spreader, frequently that of solid silicon or copper. Results have also been reported in terms of performance improvement of the vapor chamber with and without working fluid [79,80], but this metric only provides confirmation that the vapor chamber is functioning, with minimal information on the degree of functionality.

Table 2-2 presents a summary of the various silicon vapor chambers developed in literature in terms of their form factors, hotspot to condenser area ratios, wick structures, and reported performance metric. Benson et al. performed one of the earliest investigations of silicon vapor chambers as heat spreading substrates for multichip modules at Sandia National Laboratories [81,82]. Various evaporator wick structures were formed from different approaches including bidirectional cuts with a wafer saw, as well as anisotropic plasma etching. A wickless vapor cap wafer was joined to the evaporator side wick structures with a silica glass bond to serve as the condenser. Based on the initial experimental results for the temperature gradient with the vapor chamber compared to a reference silicon spreader, the vapor chamber effective thermal conductivity was estimated to be approximately 800 $Wm^{-1}K^{-1}$.

A few other trends emerge from the summary of existing silicon vapor chambers in Table 2-2. First, the vapor chambers are all much larger than a typical die size, with total areas ranging from 5 - 25 cm^2. From a heat spreading perspective, it is beneficial to reduce the heat flux as much as possible by spreading to a much larger area. From a cost perspective, however, this would result in silicon vapor chambers that likely cost much more than a typical semiconductor die, both due to the larger silicon substrate area required, as well as cost of additional processing steps. It is therefore likely that in order to be cost effective, vapor chambers of these sizes would be more suitable for module level heat spreading between multiple dies, as opposed to the single heat source configurations used for testing.

Water also emerges as the predominant working fluid of choice. Water is easy to work with in a laboratory setting and has a relatively high capillary merit number [14], where

$$M_l = \frac{\sigma \rho_l h_{fg}}{\mu_l} \tag{2.1}$$

The merit number represents the potential of the working fluid to maximize the capillary dryout limit in the vapor chamber. A higher surface tension, σ creates a higher capillary

pressure in the wick, while a higher density ρ_l and latent heat h_{fg} result in a lower evaporative mass flux for the same heat input. A lower liquid viscosity, μ_l leads to a lower viscous pressure drop. Overall, water tends to have a merit number approximately 10 times higher than other working fluids in the 0 ^{o}C – 200 ^{o}C operating range [83]. The compatibility of water with silicon vapor chamber components should therefore be an important consideration in the overall vapor chamber design.

In general, when the comparison was provided, the studied silicon vapor chambers showed significant improvement in heat spreading performance over solid silicon benchmarks. The maximum input power limitation was not extensively studied, however, and the summary in Table 1 shows a large variation in reported input powers ranging from as low as 1.6 W to 70 W. Taking into account the different heater sizes used in the studies, the different input powers can be translated to a heat flux range of approximately 13 – 100 W/cm^2. Some studies identified a maximum capillary-limited dryout power, though this was not listed for all cases, and a number of studies reported that exploring higher heat fluxes was not possible due to maximum temperature limitations of various experimental components [84,85]. Overall, quantification of the maximum input power/heat flux for a vapor chamber is a critical parameter to determine what kind of heat spreading applications the device can be utilized for. The capillary-limited dryout power in vapor chambers is a strong function of the overall vapor chamber dimensions, and in particular depends on the design of the evaporator wick. To gain more perspective on this topic, the following section will provide a more in-depth look at fundamental studies on the capillary-fed evaporation and boiling performance of various porous materials that can potentially be utilized as evaporator wicks in silicon vapor chambers.

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Table 2-2. Summary of experimental characterizations of silicon vapor chambers in literature.

Authors	**Vapor chamber area**	**Hotspot to condenser area ratio**	**Tested heating configuration**	**Wick structure**	**Performance metric**	**Max input power**	**Initiation of dryout**	**Working fluid**
Benson et al. [81,82]	3.8 x 3.8 cm^2	1:25	Planar	Crosses	Estimated effective thermal conductivity ~ 800 $Wm^{-1}K^{-1}$	15 W	5 W	Methanol
Liang et al. [86]	2 x 2 cm^2	1:36	Radial	Biporous monolayer copper powder	Thermal resistance 10% improvement over solid Si	1.6 W	0.9 W	Water
He et al. [79]	3 x 3 cm^2	1:9	Planar	Micropillars	Thermal resistance 40% improvement over empty chamber	37 W	15 W	Water
Wei et al.	3 x 3 cm^2	1:9	Planar	Micropillars	Maximum dryout heat power of 98 W	98	98	Water
Kang et al. [87]	5 x 5 cm^2	1:25	Radial	Micro grooves	Evaporator temperature 27% improvement over solid Si	27 W	N/A	Water
Gillot et al. [80]	0.9 x 5 cm^2	1:5	Planar	Micro grooves	Thermal resistance 45% improvement over empty chamber	30 W	N/A	Water
Ivanova et al. [88]	1 x 5 cm^2	1:5	Planar	Micro grooves	Thermal resistance 65% improvement over empty chamber	60 W	20-30 W	Water
Ivanova et al. [84]	5 x 5 cm^2	1:9	Radial	Micro grooves	Thermal resistance 66% improvement over solid Si	70 W	N/A	Water
Cai et al. [78]	4 x 4 cm^2	1:1.25	One-dimensional	Micropillars	Effective thermal conductivity in 1D mode ~2500 $Wm^{-1}K^{-1}$	10 W	10 W	Ethanol
Liu et al. [85]	1 x 1 cm^2	1:10	Planar	Micropillars	Hotspot temperature uniformity 45% improvement over solid Si	10 W	N/A	Water

2.5 Porous Wick Fabrication and Optimization Strategies

As mentioned in section 2.1, a silicon-based vapor chamber can benefit from the vast array of microfabrication techniques available for the generation of precision micro/nanoscale structures. In particular, this fabrication flexibility is valuable to meet the multi-objective thermo-fluidic design problem of the evaporator wick. This section will discuss some of the porous wick fabrication strategies for silicon-based vapor chambers, and the advantages/disadvantages of the various approaches.

2.5.1 Monolithic silicon wicks

Standard photolithography combined with anisotropic etch processes such as deep-reactive-ion-etching (DRIE) can produce a wide range of structures in silicon. The advantages of such an approach include monolithic integration of the wick with the substrate, removing any potential issues of thermal boundary resistance, and almost infinite possibilities for different combinations of two-dimensional wick structures due to the ease of patterning with photolithography. The tendency of silicon to form a thin layer of native oxide is also beneficial, as silicon oxide is inherently hydrophilic [89], which creates a suitable surface for the capillary-fed wicking action required for the vapor chamber to function properly. As discussed in section 2.4.2, examples of such monolithic wick structures utilized in previously developed silicon vapor chambers include crosses [81] as well as rectangular and radially patterned groove arrays [80,87].

Perhaps the most extensively studied monolithic silicon wick structure for vapor chamber applications, however, has been silicon micropillar arrays [75,78,90–92]. The regular geometry of micropillar arrays makes them conducive to unit-cell modeling approaches for both the fluid flow and heat transfer, enabling relatively accurate model-based prediction of key parameters such as the wick thermal resistance and dryout heat flux [93–95]. In order to extend the dryout heat flux and reduce the wick thermal resistance, efforts have been made to create biporous structures with non-homogenous patterns of silicon micropillars. One such approach by Byon et al. involved interspersing

larger square openings into a denser micropillar array to increase the porosity of the wick [96]. The capillary performance was found to improve over a homogenous array by more than 30%. Similarly, Coso et al. combined square-packed micropillars (diameter d = 3 – 29 μm, pitch p = 5 – 28 μm, height h = 56 – 243 μm) with microchannels (30 to 60 μm in width) to reduce the viscous pressure loss across the wick while maintaining high capillary suction within the micropillars [97]. The thickest wick with a micropillar height of 243 μm was able to sustain a maximum heat flux of up to 277 W/cm^2 for a heated area of 1 cm^2, with a stable nucleate boiling regime of 185 W/cm^2 beyond the boiling incipience heat flux.

2.5.2 Wicks with other materials

In addition to monolithically fabricated wicks in silicon, porous structures composed of other materials grown on top of or bonded to silicon substrates may also be promising wick configurations. Some advantages to using other materials such as metals include the possibility of a higher thermal conductivity contribution to the solid wick fraction, potentially reducing the overall wick resistance, and further possibilities for multi-layered, three-dimensional porous structures. Disadvantages include additional fabrication steps needed to bond/grow additional material onto the silicon substrate, and any associated reliability issues with a poor bonding interface or thermal expansion mismatch. Here, we provide a brief overview of some porous structures comprised of materials other than silicon that could be integrated into future silicon vapor chambers.

Copper is an appealing wick material choice due to its high inherent thermal conductivity, and sintered copper in particular has been extensively studied as a wick structure for traditional copper-based heat pipes and vapor chambers [98–100]. The sintering process to form a connected wick from discrete copper powder, however, requires very high temperature processing (> 800 ^{o}C) [101] and can result in a wide range of effective wick thermal conductivities depending on the sintering conditions [102]. Such high temperatures would be incompatible with a direct integration scheme as discussed in section 2.2, where the evaporative structure would be fabricated directly on the semiconductor die. Additionally, the relatively large powder particle size (> 50 μm)

used in previous studies results in large wick thicknesses (> 500 μm) [103] that fall beyond the ideal range of length scales associated with silicon wafer processing.

A more promising alternative to form copper/other metal based wicks on silicon substrates is through electrochemical processes, which have a long history of widespread use in MEMS devices for low-cost, low-temperature, and scalable growth of metal layers of varying compositions [104,105]. To create a porous metal structure with electrodeposition, the substrate of interest must have an electrically conductive surface. This can be achieved on silicon by using highly doped wafers [106] or evaporating/sputtering a thin metallic layer on the surface of interest to act as a conductive seed layer. The use of a template or pattern over the seed layer or conductive area then defines the shape of the resulting porous metal film after electroplating. Copper inverse opals are one example of porous metal films fabricated through a templated electrodeposition process that have demonstrated great promise for use as evaporative wicks [53,107,108]. The highly ordered, three dimensional porous network is fabricated by using self-assembled polystyrene spheres to form a template, electroplating through the template, then dissolving the polystyrene with an organic solvent to create the resulting inverse opal structure [109]. Extremely high critical heat flux values (> 1 kW/cm^2) have been reported for such structures with very low superheat (< 15 ^oC), albeit for small wicking lengths (< 200 μm) [53]. Additional high permeability fluidic structures integrated with the inverse opals could be a promising route to scale up the inverse opal thermal performance to the millimeter length scales required for use in a vapor chamber wick, similar to the approaches used for biporous silicon micropillar wicks [96].

Hierarchically structured copper micropillars electroplated on silicon substrates have also been studied as potential high performance wicking materials [24,110]. To increase the wettability of water on copper, Nam et al. used a chemical oxidation scheme to form a conformal superhydrophilic nanostructure on top of the copper micropillar [110]. The nanostructuring was found to improve the dryout heat flux by over 70% compared to bare micropillars, with a maximum heat flux reached of approximately 200

W/cm^2 over a 5 x 5 mm^2 heated area. Other intricate structures that have been fabricated through electroplating on various substrates include Cu meso-lattices formed by direct laser writing 3D patterns into photoresist [111], though the efficacy of such structures in capillary fed evaporation/boiling has not been thoroughly studied.

Other potential wick structures that can be fabricated on silicon substrates include various nanowire/nanotube arrays. Carbon nanotubes (CNTs) are particularly of interest, as vertically aligned films of varying heights can be directly grown on silicon substrates with relative ease [112]. Some additional attractive attributes of CNTs include the possibility of functionalization to create hydrophilic surfaces [113] and high axial single tube thermal conductivities of approximately ~2000 Wm^{-1}K^{-1} [114] (though this has been shown to be highly dependent on the CNT growth quality [115]). The nanoscale pores of the nanotube arrays can generate very high capillary pressures within the wick, but also lead to large viscous flow resistances that prevent uniform CNT arrays from being used as the sole wicking material. Weibel et al. proposed to circumvent this issue by using CNTs just over the heated area and a higher permeability material such as sintered copper mesh over the rest of the evaporator wick [26]. Cai and Chen created biporous CNT arrays by patterning the CNT growth on silicon substrates to form parallel stripes with 50 μm wide microchannels for liquid delivery [116]. The biporous CNT structure was able to dissipate up to 600 W/cm^2 over a 2 x 2 mm^2 heated area.

In the majority of the aforementioned studies of capillary-driven evaporation/boiling in porous wicks, biporous and/or hierarchical structures have emerged as higher performance alternatives to their homogenous counterparts. Depending on the different combinations of length scales considered, however, heterogenous wicks may not always perform better than homogenous structures. Ravi et al., for instance, showed that silicon micropillar wicks (d = 42 μm, p = 90 μm, h = 100 μm) capped with a mesh structure to increase the capillary pressure could greatly reduce the dryout heat flux compared to the homogenous baseline wick if the mesh thickness (1 μm) and pore size (4 μm) was too small [117]. With a sufficiently thick mesh (180 μm) and larger pore openings (15 μm), however, the dryout heat flux could be improved by

almost 200% over the baseline. The precision afforded by the vast array of micro/nanomaterials fabrication techniques compatible with silicon substrates creates many promising opportunities for thermofluidic optimization of the heat and mass transport within silicon vapor chambers, though careful design is necessary to ensure performance improvement as opposed to detriment.

2.6 Manufacturing approaches and challenges for silicon vapor chambers

In the majority of silicon vapor chambers developed to date, the vapor chamber is formed from two silicon wafers, with the evaporator side and corresponding wick structure formed on one wafer, and the condenser side located on the other. To define the vapor core, a cavity can be etched into one or both wafers, though as seen in Figure 2-3(a), this can require complicated multi-height etching processes if a monolithic silicon wick structure is also desired. To circumvent this, previous approaches have involved using triple-stack processes where the vapor core is formed from an entirely separate wafer, as seen in Figure 2-3(b) [78]. Alternatively, as shown in Figure 2-3(c), utilizing a wickless condenser allows the vapor cavity to be confined to just the condenser side wafer, and wick structures can be etched into the evaporator wafer without the need for multi-height etching [79]. The formation of a liquid film over the condenser cavity may impact the overall device resistance, however, and the lack of a condenser wick structure also renders the device operation orientation-dependent. In anti-gravity configurations, liquid pooled on the condenser surface will be unable to drip back to the evaporator side without a wick structure. The third alternative, as mentioned in section 2.5, is to form a non-monolithic wick on the silicon substrate by electroplating or bonding a different material. Liang et al. followed this approach by etching the silicon vapor cavity first, then depositing copper powder on top of adhesive dot arrays to form the evaporator wick [86]. While this approach simplifies the etching processes needed, it also introduces the possibility of poor thermal interfaces and/or CTE mismatch between the wick and the substrate.

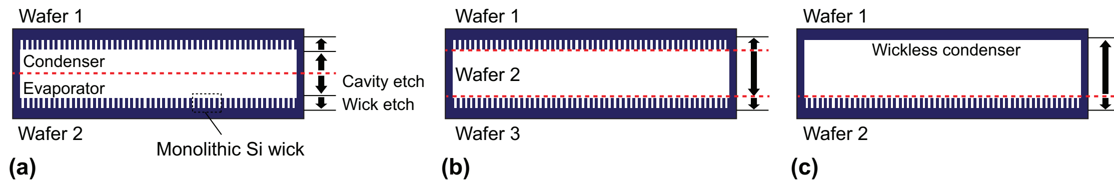

Figure 2-3. (a) Vapor chamber formed from two Si wafers with monolithic condenser and evaporator wicks. Multi-height etching steps are required for both sides to form the cavity and monolithic wick structures. (b) Triple stack vapor chamber fabrication process where vapor core is formed from separate wafer to avoid multi-height etching steps. (c) Vapor chamber with wickless condenser. Evaporator wick is etched into one substrate, and vapor core is fabricated entirely in the condenser side substrate.

After forming the cavity and the wick structures, the wafers are typically bonded together under dry conditions. One or more through-holes are usually defined for use as external charging ports to evacuate non-condensable gases and charge the vapor chamber with working fluid after the wafers are bonded together. The methods used to bond the various silicon wafers together include glass frit [78,85], Au/Si eutectic [79,87], direct silicon fusion bonding [80], and spin-coated epoxy [86]. After bonding, external tubing can be attached to the charging ports through either soldering on top of metallized port surfaces[80,88,118,119] or joining with epoxy [85,86]. The tubing is then pinched off or closed with a valve to seal off the vapor chamber after evacuation and charging. External evacuation and charging post-bonding has many advantages when performing laboratory-level characterization, as it allows for experimental iteration to find the impact of liquid charge amount. This approach is also relatively simple to integrate with existing laboratory equipment such as syringe pumps and vacuum pumps.

While convenient on a laboratory scale, such filling and evacuation processes may be difficult and impractical for large-scale manufacturing. From a cost perspective, the majority of the silicon vapor chamber manufacturing processes should ideally be performed on a wafer-level as opposed to individual device level. In a review of early pioneering work on silicon micro heat pipes, Peterson discussed several potential

evacuation, charging, and bonding methods for micro heat pipes that could be translated to large-scale silicon vapor chamber production approaches [120]. One proposed method was to place an unsealed micro heat pipe array in a high pressure chamber, evacuate the chamber of NCGs, then fill the chamber with a predetermined amount of working fluid. After heating the chamber above the critical temperature of the fluid, the micro heat pipes could then be sealed while still inside the chamber with an ultraviolet bonding process or similar. A similar principle could apply to the fabrication of silicon vapor chambers, though the use of an ultraviolet bonding process requires a UV transparent condenser cap wafer, which could present compatibility issues and impact the overall heat transfer performance of the silicon vapor chamber. An alternative sealing approach could be to place solder preforms around the charging through-holes, then melt and seal the openings with inductive heating while the vapor chamber is contained within the saturated chamber [121].

Finally, mechanical considerations also play an important role in silicon vapor chamber design. The internal pressure of the vapor chamber is directly related to the vapor temperature, potentially placing restrictions on the maximum operating temperature due to mechanical burst pressure limitations. Power electronics devices utilizing wide bandgap semiconductors such as GaN and SiC frequently operate at 200 ^{o}C or above [122], corresponding to vapor chamber internal pressures of more than 1.5 MPa with water as the working fluid. While silicon electronic devices typically do not operate above 120 ^{o}C, a silicon vapor chamber attached to a silicon device may still need to survive higher temperatures during various other packaging processes such as die attach and reflow. Cai et al. demonstrated that mechanical support pillars between the evaporator and condenser surfaces were necessary to prevent bursting above 180 ^{o}C for a 3x3 cm^2 silicon vapor chamber [78]. Other techniques such as rounding of etched cavity edges can also be implemented to prevent stress concentration at sharp corners, similar to techniques leveraged in piezoresistive silicon pressure sensors [123].

2.7 Conclusions

Silicon-based vapor chambers are appealing candidates as high performance heat spreaders in space-constrained, power dense applications. In the survey of existing silicon vapor chambers characterized to date, the majority demonstrated a significant improvement in heat spreading performance compared to solid silicon. Since silicon is CTE matched to most semiconductor substrates, the use of a silicon vapor chamber enables a variety of new packaging configurations, such as high thermal performance metal bonding between the die and the vapor chamber or direct integration of evaporative wicking structures into the die substrate. Silicon vapor chambers also present an array of new challenges compared to traditional metal vapor chambers, however, and manufacturing approaches developed in literature have sometimes necessitated trade-offs between fabrication ease and performance. Existing methods for liquid charging and NCG evacuation are also more suited for laboratory level settings and must be scaled up for large-scale production and widespread usage of silicon vapor chambers to become feasible. Overall, however, the outlook for silicon-based vapor chambers remains positive, with many potential benefits for use in integrated packages to address the challenges of chip-level hotspot management.

Chapter 3

Miniature Silicon Vapor Chambers for Die-level Heat Spreading

This chapter describes the fabrication and characterization of a miniature (1 x 1 cm^2) silicon vapor chamber developed for the purpose of die-level heat redistribution. We present experimental results for the device thermal performance, as well as a semi-analytical model to describe the effects of liquid charge volume on the overall thermal resistance. Large portions of this chapter are taken from Liu et al., "Characterization and Thermal Modeling of a Miniature Silicon Vapor Chamber for Die-Level Heat Redistribution," *International Journal of Heat and Mass Transfer*, 2020 [85].

3.1 Device Fabrication

The dimensions of previous silicon vapor chambers in literature described in section 2.4 are typically much larger than a standard die size in order to reduce the heat flux to the condenser side as much as possible, with condenser areas ranging from 3 x 3 cm^2 to 5 x 5 cm^2 [78–80,86,124]. While this is beneficial from a thermal perspective to reduce the heat flux as much as possible, it may not always be feasible from a cost and packaging perspective for manufacturers to implement a silicon vapor chamber much larger than the die. Silicon processing is often thought of in terms of cost per unit area, a factor that has stayed roughly constant over the past few decades [125]. We therefore investigate the potential benefit to overall system thermal management in implementing an integrated, die-area matched silicon vapor chamber with an active area of 1 x 1 cm^2.

As described in the section 2.6, it can be challenging to fabricate both the vapor cavity and monolithic wick structure in the same silicon substrate with traditional dry/wet etching processes. We therefore utilize a novel fabrication approach with ultra-violet (UV) laser ablation to form the vapor core and evaporator/condenser wicks with a lithography-free process. This avoids the need for a triple stack process and any issues of

thermal boundary resistance or CTE mismatch with non-monolithic wicks. Figure 3-1(a) shows the overall fabrication process flow for the miniature silicon vapor chamber. The active vapor chamber area of the device is 1 x 1 cm^2, with a total vapor chamber thickness of 1.5 mm. 5 mm of solid silicon is included around the periphery of the active vapor core area to allow space for bonding and patterning of electrical contact pads for a thin-film heater and resistance temperature detectors (RTDs). A 1 mm thick, 4 inch silicon wafer is used for the evaporator side in order to account for the vapor core cavity thickness, and a 500 um thick, 4 inch wafer is used for the condenser side with no vapor core cavity. Both wafers go through an initial thermal oxidation step to grow approximately 400 nm of SiO_2 for electrical passivation. Standard photo-lithography techniques are used to expose, develop, and pattern 100 nm of platinum with a 10 nm chromium adhesion layer for the heater and RTDs.

The electrical heater and RTD mask layouts for both the evaporator and condenser sides of the device are shown in Figures 3-1(b) and (c). On the evaporator side, a serpentine heater over a 3.2 x 3.2 mm^2 area represents the heat source from the die, and 7 different RTDs (labeled as T_{E1-7} in Figure 3-1(b)) are distributed across the 10x10 mm^2 active evaporator area as well as interspersed between the serpentine heating lines to measure the temperature distribution across the entire evaporator/hotspot for various heat inputs. The average hotspot temperature used in the thermal resistance calculation is estimated by taking the average of T_{E7}, T_{E6}, and T_{E3}. The condenser side has 9 RTDs located at various points across the condenser area to similarly provide information about the condenser side temperature distribution as a function of heat input. Due to microfabrication defects, only 5 of the patterned RTDs were functional on the condenser side (T_{C1-4} and T_{C6}). The average condenser temperature is calculated from the average of measurements obtained from T_{C1}, T_{C2}, T_{C4} and T_{C6}. No central temperature measurement was available on the condenser side, but the resulting error in the average temperature is expected to be minimal due to the high thermal conductivity of the vapor core. Measurements from a separate, identically fabricated device with a functional central RTD showed a less than 1% difference between an average condenser temperature calculated with and without the central RTD measurement.

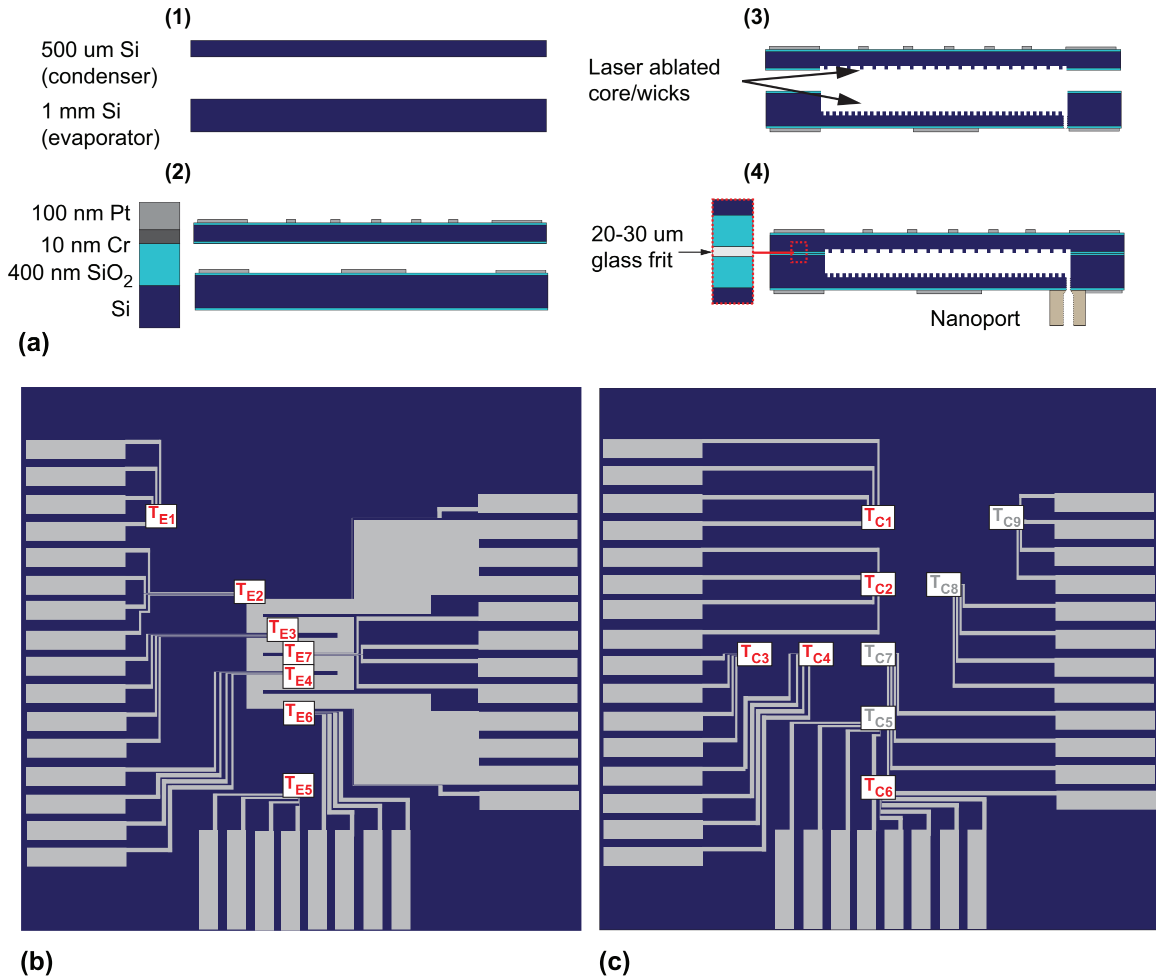

Figure 3-1. (a) Fabrication process flow for condenser and evaporator sides starting from (1) 500 µm thick and 1 mm thick substrates for condenser and evaporator sides, respectively (2) thermal oxidation, then photolithography and metal evaporation to define heater and RTDs, (3) laser ablation to etch vapor core, wick structures, and through-hole, (4) glass frit bond and Nanoport attachment. (b) Evaporator side heater and RTD layout. *(*c) Condenser side RTD layout. Due to microfabrication defects, only T_{C1-4}, and T_{C6} were functional.

After patterning the heater and RTDs, the vapor core and evaporator/condenser wick structures are fabricated through UV laser ablation with a pulsed neodymium-doped yttrium orthovanadate (Nd/YVO4) laser (Samurai UV Laser Marking System from DPSS (Diode Pumped Solid State) Lasers Inc). While the use of laser ablation limits the

minimum feature size achievable to around 70 μm, deep etch features such as the vapor core can be performed with relative ease. Additionally, the laser ablation generates a conformal microscale roughness on the etched features that increases the surface area for heat transfer and promotes superhydrophilicity, potentially providing a pathway for performance enhancement over smooth, traditionally microfabricated surfaces. Figure 3-2(a) depicts a scanning electron micrograph (SEM) of a laser-ablated micropillar, with distinct surface roughness generated on the pillar sidewall as well as pillar base (Figure 3-2(b)). The laser ablation process results in slightly conical pillars due to the change in laser focus plane as more material is ablated away. The wick structures on both the evaporator and condenser sides of the vapor chamber are square packed cylindrical pillar arrays, linked by perpendicular grooves around the periphery of the vapor cavity for condensate return. A through-hole, visible in Figure 3-2(c), is also defined for each device during the etching process on the evaporator side to serve as a port for evacuation and liquid charging.

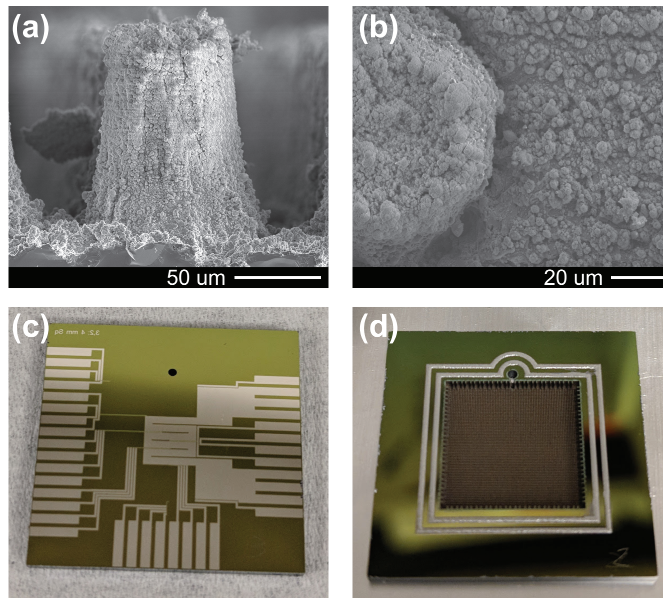

Figure 3-2. (a) Sideview of micropillar fabricated through laser ablation. (b) Top view close up of microscale roughness generated on micropillar wick structures from laser ablation. (c) Evaporator side device with patterned heater/RTDs and through-hole. (d) Glass frit pattern after initial glazing step.

After defining the vapor core and wick structures, the devices are sonicated for 20 seconds to remove any accumulated silicon debris from the ablation process. The evaporator and condenser sides are then joined together with a glass frit bond (Koartan 5645-Si sealing glass paste). The frit includes organic binders mixed in with glass particles that must be burned out first during a high temperature (~ 450 ^{o}C) glazing step, otherwise incomplete binder burnout will lead to a weak bond with potential outgassing and generation of non-condensable gases during the device operation. The printed glass frit sealing rings after the initial glazing step can be seen in Figure 3-2(d). In order to perform parametric liquid charging experiments without the added uncertainty of device variation, a non-permanent and reusable connection is used to link the vapor chamber with external fluid lines through a microfluidic Nanoport (Idex HS). A leak-tight connection is formed between the Nanoport and silicon surface through an o-ring face seal, and epoxy is applied to maintain the compressive sealing force. The Nanoport was chosen mainly for experimental convenience, and other methods to form more robust and permanent connections for future devices could involve soldering metal tubing to a metalized port [78], or performing the device bond step in a saturated environment [77].

3.2 Analytical model for effect of liquid charge volume

We develop a reduced order thermo-fluidic model to predict the effect of both heat flux and liquid charge on the overall thermal resistance of the vapor chamber. The thermal performance of vapor chambers and heat pipes has been observed to be strongly dependent on the liquid charge volume [87,126,127], a factor that becomes even more critical when working with a miniaturized device with expected charge volume on the order of microliters. A standard approach to identify the ideal charge volume is to iterate experimentally. Full-scale numerical simulation of the conjugate, two-phase heat and mass transport within a vapor chamber is computationally expensive and can present minimal benefit over an experimental approach. Many models in literature also make the simplification of a saturated wick and cannot account for the effect of varying liquid charge on the overall thermal performance [15,128–131]. The assumption of a saturated wick neglects microscopic pore level effects on wick permeability and effective thermal conductivity, which can be significant depending on the geometry and heat flux level

considered. Ranjan et al. developed a detailed conjugate simulation that coupled a wick microstructure model with a vapor chamber macro-model through an evaporative mass flux correction factor [132], and noted that accounting for microstructure effects is especially critical for wick thicknesses on the order of 100 μm or less. More work has been done in the area of modeling micro heat pipes, as accounting for the meniscus curvature in the heat pipe grooves is required to drive the liquid flow from the condenser to evaporator section [133,134]. Do et al. developed a numerical model capable of predicting the effect of liquid charge on thermal resistance as well as maximum heat flux for a flat, grooved wick micro heat pipe [135]. Similar work, however, has not been extended to a two-dimensional capillary driven vapor chamber configuration such as the one considered here. In this section, we therefore provide a model to predict the effect of liquid charge and heat flux on the thermal performance of a miniature vapor chamber, accounting for wick microstructure effects, without the need for a full conjugate numerical simulation.

The model does not attempt to calculate the operational limits of the device, thereby allowing the thermal resistance to be calculated from an equivalent solid conduction model without a full numerical simulation of the coupled flow and temperature fields [15]. The effective thermal conductivities of the condenser/evaporator wicks are dependent on the liquid distribution and temperature within the device, however, requiring still some knowledge of the fluid flow. Fluid flow sub-models are therefore developed for each region to account for wick microstructure effects and provide a more accurate estimate of the device resistance without the need for a full conjugate numerical simulation. Additionally, the fluid flow sub-models provide a means to track the total mass of working fluid within the vapor chamber, allowing the model to account for the effect of liquid charge volume. The following sections will go over the thermo-fluidic models for the evaporator wick, condenser wick, and overall model calculation flow.

3.2.1 Evaporator model

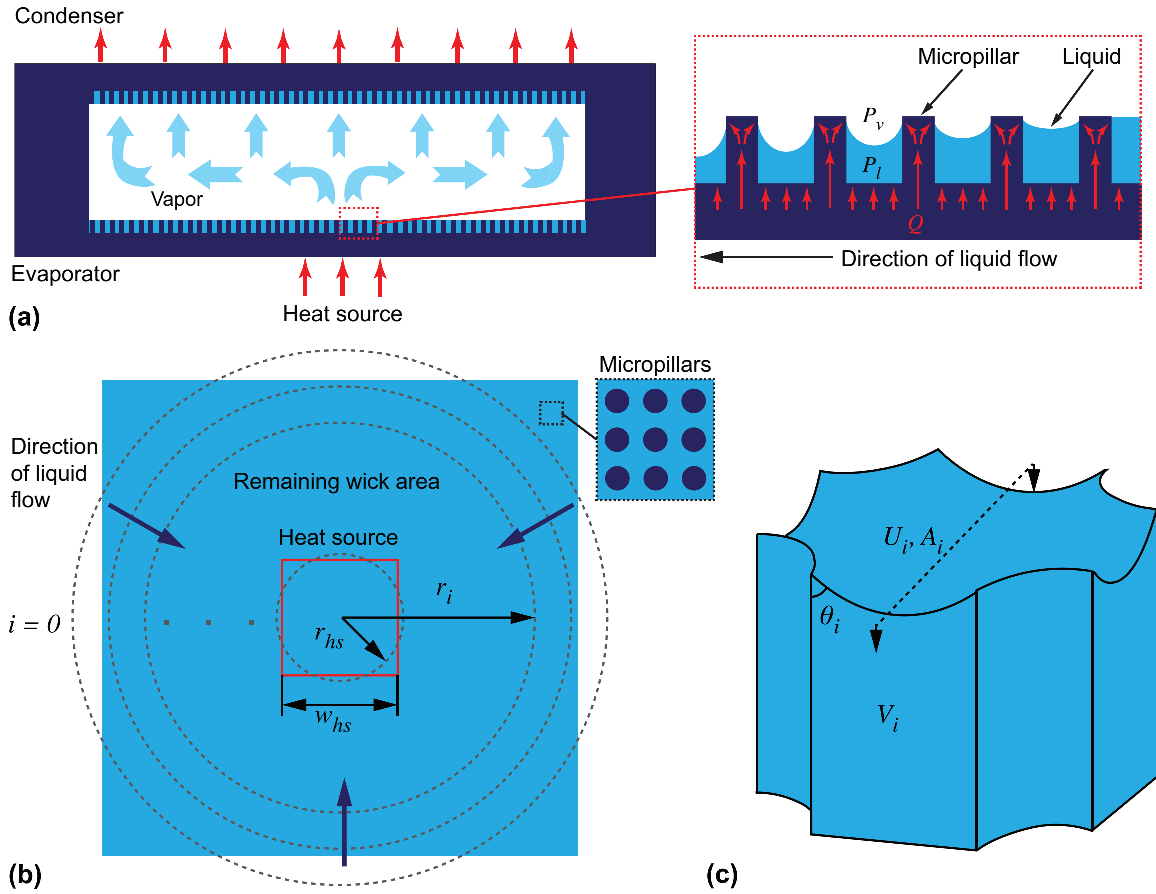

Figure 3-3. (a) Cross-sectional schematic showing the general principles of the miniature silicon vapor chamber. Inset shows the variation in meniscus distribution and heat flux vectors in the evaporator wick. (b) Top view of radial representation of flow through evaporator wick. The wick is divided into a set of unit rings, with i = 0 starting at the edge of the wick. (c) Representation of a single unit cell within the ith unit ring. The cross sectional area, A_i, unit cell volume, V_i, and area-averaged velocity, U_i, are tabulated as a function of pressure drop across the unit cell for a range of different meniscus curvatures and apparent contact angles, θ_i.

An overall cross-sectional schematic of the capillary wicked silicon vapor chamber considered in this work is shown in Figure 3-3(a). Heat generated from a square

hotspot on the evaporator side of the device causes the liquid within a square-packed micropillar wick to evaporate into vapor, which then spreads throughout the vapor core region before condensing back into liquid in the condenser wick. In the evaporator micropillar wick, evaporation from the centrally located heat source creates a non-uniform liquid distribution as shown in inset of Figure 3-3(a). As the input heat flux increases, further recession of the liquid into the pores of the heated region increases the area for evaporation and reduces the overall wick resistance [23,90,94,97]. Therefore, to accurately capture the effective thermal conductivity as a function of heat flux and liquid charge, the model must be able to incorporate the effect of varying meniscus shape along the length of the evaporator wick. To account for this, we adapt the experimentally validated fluid flow model developed by Zhu et al. to solve for the liquid meniscus distribution along the wick as a function of input heat flux [94].

We extend their model to account for a non-uniform heat input and approximate the liquid flow as one-dimensional, radial flow from the edges of the wick towards the central heated region. As shown in Figure 3-3(b), the actual flow field is not precisely radial due to the square geometry of the heated area and overall wick area. To enable the radial approximation, the square heated area is therefore converted to a circular area by defining an equivalent radius, r_{hs}, such that

$$r_{hs} = \sqrt{\frac{A_{hs}}{\pi}} \tag{3.1}$$

The square wick is similarly converted into a radial equivalent with the same method, then divided into an array of unit rings as shown in Figure 3-3(b), where the rings are numbered such that $i = 0$ at the wick edge and increases monotonically towards the wick center. While this conversion leads to sections of rings that span outside of the physical device borders, it preserves the total areas of the heat source and wick and provides a more accurate accounting when calculating the total liquid charge contained within the wick. Each ith unit ring is assumed to be comprised of a number of unit cells, n_i, equal to

$$n_i = \left\lfloor \frac{2\pi r_i}{p_i} \right\rfloor \tag{3.2}$$

where r_i is the radius of the ith ring, and p_i is the pitch of the micropillars within that ring. The unit cells within each ring have a distinct meniscus shape that satisfies the Young-Laplace equation. The Young-Laplace equation describes the capillary pressure difference sustained across the liquid vapor interface, which can be written as

$$\Delta P_{lv} = P_v - P_l(r) = 2\sigma\kappa(r) \tag{3.3}$$

where P_v is the vapor pressure, P_l is the radially dependent liquid pressure, σ is the liquid-vapor surface tension, and κ is the radially dependent meniscus curvature. We assume that the radial gradient in vapor pressure is small compared to the liquid pressure gradient, as is typical in vapor chambers, such that P_v can be considered approximately constant.

Unique unit cell meniscus shapes are generated for a large range of vapor-liquid pressure differences using a force balance model in COMSOL, details of which can be found in [94]. The liquid is assumed to exist in a pinned state at the top of the micropillars, with a minimum sustainable contact angle equal to the receding contact angle for the working fluid and solid surface under consideration. The contact angle for each unit cell, θ_i, is defined as shown in Figure 3-3(c) as the angle between the meniscus interface and the pillar surface. The difference in meniscus curvature from the unit cells within one ring to the next creates the capillary pressure difference that drives fluid flow from the wick outer edge to the central heated area. The average cross sectional area A, flow velocity U, and unit cell volume V are tabulated through computational fluid dynamics (CFD) simulations in COMSOL as functions of the liquid meniscus shape and pressure drop across the unit cell. Due to the tedious nature and large number of simulations required to create such reference tables, the working fluid properties for each simulation are held fixed at a reference point of 100 ^{o}C. When using water as the working fluid, the primary effect of this assumption is to underpredict the contact angle at temperatures below 100 ^{o}C due to the increase in surface tension with decreasing

temperature. The effect of the underprediction is small, however, for the range of vapor liquid pressure differences considered in this paper (< 150 Pa). For example, the variation in predicted apparent contact angle for the pressure difference of ΔP_{lv} = 150 Pa is only around 1.2% when using reference temperatures of 100 ^{o}C versus 50 ^{o}C. If the model were to be extended for the prediction of dryout heat flux, however, a potentially much larger pressure difference range would need to be considered, and temperature dependent meniscus shapes would need to be taken into account.

The total mass flux across each ring can be found through the summation of the mass flux through each unit cell. For non-circular packed arrangements of micropillars, this radial treatment will lead to an underprediction of the mass flux per unit cell near the wick center where the effective radius is of the same order as the micropillar pitch. The error in total mass balance for the square packed pillar arrays considered in this study, however, is still less than 2%. A mass and energy balance across each unit ring couples the capillary pressure and mass flux with neighboring rings such that

$$\rho\left(n_{c,i-1}A_{i-1}U_{i-1} - n_{c,i}A_iU_i\right)h_{fg} = q_i"\pi({r_{i-1}}^2 - {r_i}^2) \tag{3.4}$$

where q'' represents the heat flux for each ring, and h_{fg} is the latent heat of vaporization of the working fluid. Setting the starting capillary pressure, ΔP_{lv}, and average fluid velocity, U, at i = 0 gives the boundary conditions at the wick edge and enables the solution of the full meniscus distribution across the wick. The starting capillary pressure boundary condition is linked with the condenser sub-model as described in the following section. The starting velocity is set based on the assumption that all the fluid being evaporated must enter at the wick edge. With knowledge of the meniscus distribution and total liquid volume contained in each unit ring, we can calculate the total mass of liquid within the evaporator wick, m_e, through a summation over all unit rings, and begin the procedure to solve for the effective thermal conductivity.

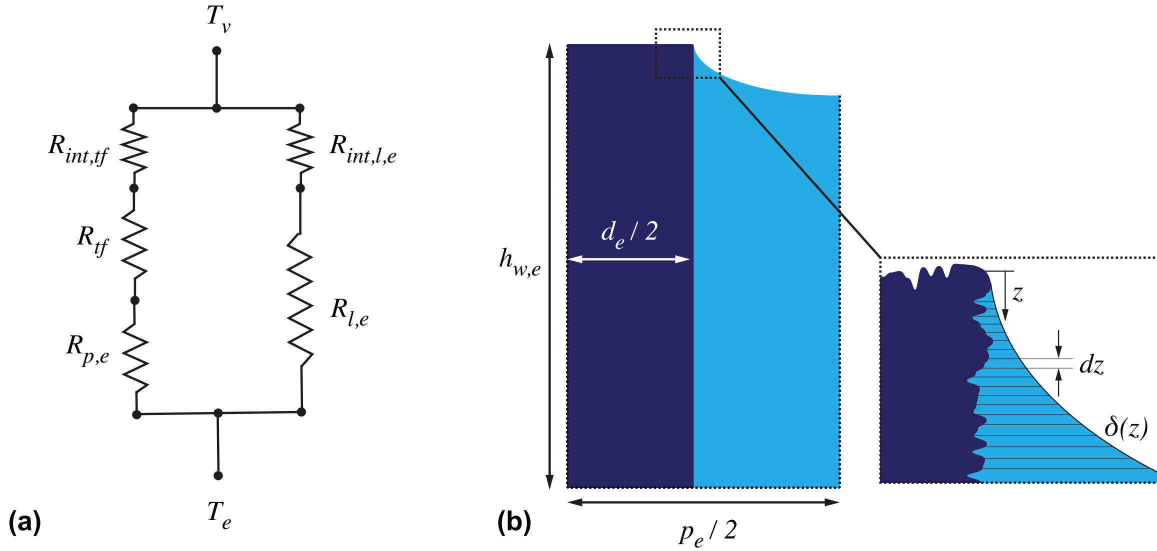

Figure 3-4. (a) Resistance network for calculating the total thermal resistance across a micropillar unit cell in the evaporator wick. (b) Side view of evaporator wick with micropillar height $h_{w,e}$, pitch p_e, and diameter d_e. Inset shows a representation of the thin-film liquid profile, $\delta(z)$, where majority of evaporation occurs.

We use a thermal resistance network as shown in Figure 3-4(a) to derive the effective thermal conductivity of a micropillar unit cell. For a base heated micropillar unit cell, heat travels in parallel through the solid micropillar and bulk liquid film. Due to the low thermal conductivity of the neighboring bulk liquid, we assume that the heat flow in the micropillar is essentially one-dimensional, and the micropillar conduction resistance can be expressed as

$$R_{p,e} = \frac{h_{w,e}}{(1-\varphi_e){p_e}^2 k_s} \tag{3.5}$$

where k_s is the thermal conductivity of the solid, and $h_{w,e}$, φ_e, and p_e represent the evaporator micropillar height, wick porosity, and pitch, respectively.

The bulk liquid conduction resistance is defined as

$$R_{l,e} = \frac{h_{w,e}}{\varphi_e {p_e}^2 k_l} \tag{3.6}$$

where k_l is the liquid thermal conductivity. For the combination of solid silicon and water as the bulk liquid, $R_{p,e} \ll R_{l,e}$, and the majority of the heat is expected to travel through the solid then evaporate from a microscale liquid film region along the top circumferential edge of the pillar. As the liquid meniscus in the evaporator wick becomes more concave, this thin liquid film area increases. For the range of microscale pore sizes considered here, various studies in literature have concluded that the thickness of this highly evaporative meniscus region (representing > 50% of the total evaporative heat transfer) ranges from approximately 1-10 μm [21–23,136]. This portion of the meniscus has been defined as the micro-region in some studies [22,136], however, various other studies on evaporation from microstructures have referred to this section of the meniscus as the thin-film region [23,90,97]. In this work, we refer to this highly evaporative region as the thin-film region, and define it as the portion of the meniscus with a liquid film thickness less than or equal to 5 μm. We neglect disjoining pressure effects on evaporation rate suppression as this has been shown to be insignificant for length scales > 100 μm [20,22], which is of the same order as the micropillar wick dimensions considered here.

For a given meniscus shape, we can estimate the thin-film area through integration of the meniscus curvature around the pillar surface. Due to the cylindrical pillar geometry under consideration, minimal variation of the thin-film profile is expected to occur around the pillar circumference. As shown in Figure 3-4(b), the thin-film resistance is calculated through integration of the thin-film profile, $\delta(z)$. We treat each infinitesimal slice of the thin-film liquid profile as a parallel resistor with a thickness equal to $\delta(z)$ and area calculated from a surface of revolution approach. This leads to the following expression for the thin-film resistance R_{tf}, where

$$R_{tf} = \left[2k_l \pi \beta \int_0^{z_{tf}} \frac{\left(\delta + \frac{d_e}{2}\right)\sqrt{1 + \left(\frac{d\delta}{dz}\right)^2}}{\delta} dz \right]^{-1} \tag{3.7}$$

z_{tf} is the distance from the micropillar top that marks the end of the thin-film region, d_e is the diameter of the evaporator micropillar, and β is a geometric fitting parameter that accounts for any enhancement in surface area that may occur from additional surface roughness on the micropillar, as well as additional thin-film evaporation that may be unaccounted for with the 5 um film thickness assumption. The inset in Figure 3-4(b) depicts an artistic rendering of an example micropillar surface texture. For micropillars fabricated through standard deep-reactive-ion-etching (DRIE) processes, β is expected to be close to 1. For micropillars that have undergone any additional surface treatment such as chemical etching, etc., β will be > 1.

The interfacial resistance is calculated using the Schrage equation [137] as

$$R_{int} = \frac{1}{A_{int}} \frac{2-\alpha}{2\alpha} \left(\frac{T_v v_{fg}}{{h_{fg}}^2}\right) \sqrt{\frac{2\pi R_u T_v}{M}} \left(1 - \frac{P_v v_{fg}}{2h_{fg}}\right)^{-1} \tag{3.8}$$

where A_{int} is the area of the interface, α is the accommodation coefficient, T_v is the vapor temperature, v_{fg} is the vapor-liquid specific volume difference, M is the molar mass of the working fluid, and R_u is the universal gas constant. The accommodation coefficient α is chosen as 0.1 in this work, on the same order as previously reported experimental values for evaporation of water from micropillars into a vapor saturated environment [90]. Note that the interfacial resistance is calculated separately for the thin-film and bulk liquid regions due to an expected variation in interfacial temperature along the meniscus. A non-isothermal interface may lead to the formation of thermocapillary vortices from Marangoni convection [73], though this effect has been reported to be small for the typical superheat range expected in a vapor chamber wick pore (< 5°C) [20] and is neglected to preserve model simplicity.

The final expression for the unit cell effective thermal resistance is

$$R_{cell} = \left((R_{p,e} + R_{tf} + R_{int,tf})^{-1} + (R_{l,e} + R_{int,l,e}{}^{-1}\right)^{-1} \quad (3.10)$$

The equivalent resistance for the entire wick can then be expressed as

$$R_{w,e} = \left(\sum_{i=1}^{n_e} R_{cell,i}{}^{-1}\right)^{-1} \quad (3.11)$$

where n_e is the number density of unit cells in the evaporator wick. Finally, the equivalent resistance is converted into an effective thermal conductivity for use in the solid conduction model as

$$k_{w,e} = \frac{h_{w,e}}{R_{w,e} A_e} \quad (3.12)$$

3.2.2 Condenser model

Unlike the evaporator region of the device, we approximate the condenser region with a uniform vapor mass flux [83] due to the highly efficient nature of vapor transport and spreading in the core. This assumption applies as long as the pressure drop in the vapor core is minimal, as addressed in the following section. Condensation is expected to occur throughout the entire wick area, including the micropillar top surfaces and bulk liquid. This provides one of the primary advantages of a condenser side wick, which is to create a more uniform heat removal surface. In the absence of a wick structure, the formation of a bulk liquid film would introduce additional thermal resistance into the system. Other methods of potentially addressing this issue include chemical treatment to induce dropwise condensation on wickless hydrophobic condensers, or active droplet jumping on a superhydrophobic structured condenser [30].

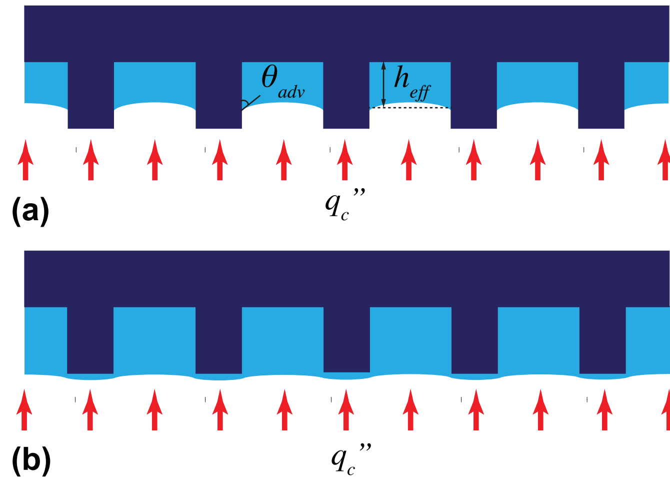

Figure 3-5. Schematics of liquid distribution for two cases of liquid volume. (a) Model of condenser liquid distribution without flooding. (b) Condenser liquid distribution in the event of flooding, where a thin film forms on top of the micropillars and creates extra thermal resistance.

For a superhydrophillic wick surface, we assume that the majority of liquid condensed on the pillar tops will wick into the liquid bulk. We relax the requirement of pinned liquid menisci at the micropillar top edges, and allow for the fact that for charge volumes with a total wick saturation ratio less than 1, the liquid in the condenser may not fill the wick to the full height of the condenser pillars. Additionally, if the condenser wick has a higher porosity than that of the evaporator wick, it would be energetically unfavorable for extremely concave, pinned meniscus shapes to form at the condenser side. We acknowledge that for low amounts of liquid charge volume, intermediary menisci states may also exist within the evaporator wick that are not necessarily pinned at the micropillar top edges, particularly if the micropillar surface is rough. The inclusion of these states would improve the accuracy of the model for low liquid charge volumes or near dryout heat fluxes, but would require additional computation beyond the scope of the current work. By assuming a pinned evaporator wick and unpinned condenser wick, we provide a system constraint to track the liquid redistribution within the device. We assume that in the event of overcharging, the entire condenser wick may become flooded and additional liquid condensate will form a steady film on the micropillar top surfaces.

In reality, if the device is overcharged, the evaporator wick may flood as well. However, as the applied heat flux increases, the liquid will eventually redistribute to the condenser side. We therefore assume in the model that significant liquid redistribution will only occur on the condenser side, and the two different liquid distribution scenarios are depicted in Figure 3-5.

In the case of a non-flooded wick as shown in Figure 3-5(a), the fluid flow in the condenser can be approximated with an effective medium approach through the implementation of Darcy's law with a uniform condensation mass flux. We assume minimal variation in meniscus curvature throughout the length of the wick and approximate using an average meniscus contact angle, θ_{adv}, equal to the advancing contact angle. The value of θ_{adv} for water on SiO_2 is approximately 70° [89]. The permeability of the wick can be calculated through an analytical expression derived by Byon et al. for a fixed contact angle as

$$K_c = K_{2D}\left[1 - \frac{\exp\left(2\sqrt{\frac{\varphi_c}{K_{2D}}}h_{eff}\right) - 1}{\sqrt{\frac{\varphi_c}{K_{2D}}}h_{eff}\left(\exp\left(2\sqrt{\frac{\varphi_c}{K_{2D}}}h_{eff}\right) + 1\right)}\right] \tag{3.13}$$

where φ_c is the porosity of the condenser wick and h_{eff} is the effective height of liquid in the wick that accounts for a uniformly curved meniscus while conserving the total liquid volume [93]. K_{2D} is the permeability for the micropillar array without meniscus effects, and is given as

$$K_{2D} = \frac{{p_c}^2 \ln\left({\varepsilon_c}^{-0.5} - 0.738 + \varepsilon_c - 0.887{\varepsilon_c}^2 + 2.038{\varepsilon_c}^3\right)}{4\pi} \tag{3.14}$$

for a square packed pillar array, where p_c is the pitch of the condenser wick and ε_c is the solid fraction of the wick, equal to 1 - φ_c . The expressions listed for K_c and K_{2D} are valid for arrays with $\varepsilon_c < 0.25$ and $d_c/p_c < 0.57$ [93]. The effective liquid height, h_{eff} is expected to vary with heat flux and liquid charge amount, and is calculated iteratively through the procedure described in Section 3.2.5.

To derive the capillary pressure boundary condition at the evaporator/condenser wick interface, we model the condenser wick using Darcy's Law with a uniform condensation mass flux. For a given liquid height, h_{eff}, the radial liquid pressure drop and superficial velocity, u_c, are related through Darcy's law, where

$$\frac{dP_l}{dr} = \frac{-\mu}{K_c} u_c \tag{3.15}$$

Assuming all of the liquid evaporated is re-condensed, we can solve for the pressure drop explicitly through a mass balance as

$$\frac{d}{dr}\left[\int_0^{h_{eff}} \rho_l u_c 2\pi r dz\right] dr = \frac{Q}{A_c h_{fg}} 2\pi r dr \tag{3.16}$$

where A_c is the area of the condenser, Q is the total heat input being evaporated, and ρ_l is the density of the liquid. Integrating Equation (3.16) and substituting in Equation (3.15) gives the final result in terms of the condenser side heat flux, q_c'', as

$$P_{l,c}(r) = P(r = 0) - \frac{q''_c \mu}{4\rho_l h_{fg} h_{eff} K_c} r^2 \tag{3.17}$$

Assuming that the wet point of the vapor chamber occurs at r = 0 in the condenser wick [30], we can rewrite $P(r = 0) = P_v$, leading to the final result for the capillary pressure boundary condition at the edge of the condenser wick as

$$\Delta P_{lv,c} = \frac{q''_c \mu}{4\rho_l h_{fg} h_{eff} K_c} r_c^2 \tag{3.18}$$

Equation (3.18) then provides the boundary condition for the starting capillary pressure at the outer edge of the evaporator wick, effectively coupling the liquid flow in the two portions. When the condenser is in the flooded scenario (Figure 3-5(b)), we treat the condenser as a liquid reservoir for flow to the evaporator and set the starting capillary pressure boundary condition equal to zero.

Since vapor is condensed over the entire wick area, the effective thermal conductivity of the condenser can be calculated by treating the solid micropillar and

liquid bulk resistances in parallel. The solid micropillar and liquid bulk resistances are calculated in a similar manner to the evaporator wick, and the exact expressions are not repeated again for brevity. The final expression for the effective condenser thermal conductivity is thus

$$k_{w,c} = \frac{h_c + \Delta h}{\left(R_{p,c}{}^{-1} + R_{l,c}{}^{-1}\right)^{-1} A_c} \tag{3.19}$$

where

$$\Delta h = \begin{cases} 0, & h_{eff} \leq h_c \\ h_{eff} - h_c, & h_{eff} > h_c \end{cases} \tag{3.20}$$

and the interfacial resistance across the bulk liquid-vapor interface based on Equation (3.8) has been lumped into $R_{l,c}$.

3.2.3 Vapor core model

Due to the relatively thick vapor core and small vapor spreading distance (675 μm and ~5 mm, respectively) considered in our miniature vapor chamber, the pressure drop and subsequent temperature drop in the vapor core are expected to be insignificant compared to the wick regions. The vapor core can thus be modeled as a block with very high thermal conductivity. A previous study reported an effective vapor core conductivity of 23,000 $Wm^{-1}K^{-1}$ for a vapor chamber with a vapor core thickness comparable to our device (635 μm) and significantly longer vapor spreading distance (~ 45 mm) [15]. We choose a conservative value of k_v = 20,000 $Wm^{-1}K^{-1}$ for the remainder of our model calculations to serve as a lower bound to the vapor core conductivity. The model is not sensitive to the exact value of k_v, as the thermal resistance of the vapor core is negligible compared to the effective wick resistances. Note that this assumption will no longer be appropriate if the spreading distance increases significantly or the core becomes drastically thinner. For ultra-thin vapor chambers with core thicknesses on the order of 100 um, the vapor resistance is expected to dominate the system performance, and additional calculations are needed to accurately account for the effective vapor core conductivity and pressure drop [14].

3.2.4 Solid conduction model

Since the effective thermal conductivities of the evaporator and condenser wicks are functions of heat flux, it is important to characterize any parallel heat flow that may occur outside of the active phase change region of the device. This will be particularly significant for cases where flooding of the condenser wick may occur and create higher resistance states that cause more heat flow to be diverted elsewhere. We therefore estimate the active power contributing to evaporation/condensation within the porous wicks by accounting for two parallel heat transfer pathways, one flowing through the active vapor chamber region where phase change occurs, Q_{act}, and another flowing through the bonded solid sidewalls that form the periphery of the active vapor chamber region, Q_{side}.

We estimate the sidewall conduction resistance, R_{side}, to be approximately 8.2 ^{o}C/W by performing a finite element simulation in COMSOL on a dry vapor chamber with no working fluid. Figure 3-6(a) shows an example COMSOL simulation result to calculate R_{side} for an input heat flux of 100 W/cm^2. h_∞ and T_∞ are taken as 2500 Wm^{-2}K^{-1} and 20° C, respectively, and a 30 um thick, 500 um wide glass frit bond line with a thermal conductivity of 1 Wm^{-1}K^{-1} is used to approximate the bonding interface between the condenser and evaporator sides of the device.

To calculate Q_{act}, we estimate the resistance of the active vapor chamber region, R_{act}, based on the geometry as shown in Figure 3-6(b) where the evaporator wick, condenser wick, and vapor core thermal conductivities are calculated from the sub-models described in the previous sections, and the remainder of the vapor chamber stack is composed of solid silicon. To facilitate rapid iteration and incorporation of the sub-models on the same computing platform, an estimate of R_{act} is obtained for the active region geometry in Figure 3-6(b) by using the analytical influence coefficient method developed by Muzychka [138]. A uniform heat transfer coefficient is applied to the condenser side with a localized heat source on the evaporator side and insulated sidewalls. As shown in Figure 3-6(c), the source plane on the evaporator side is divided into a 2D power map array with discrete heat sources over the heated area and zero heat

flux for the remaining sources. A grid discretization size of Δx = Δy = 150 μm was chosen for our influence coefficient calculations to balance accuracy and computation time. Moving to a finer grid discretization of 100 μm and increasing the number of heat sources by 2.25 times tripled the computation time and showed a less than 3.5% change in the calculated R_{act}.

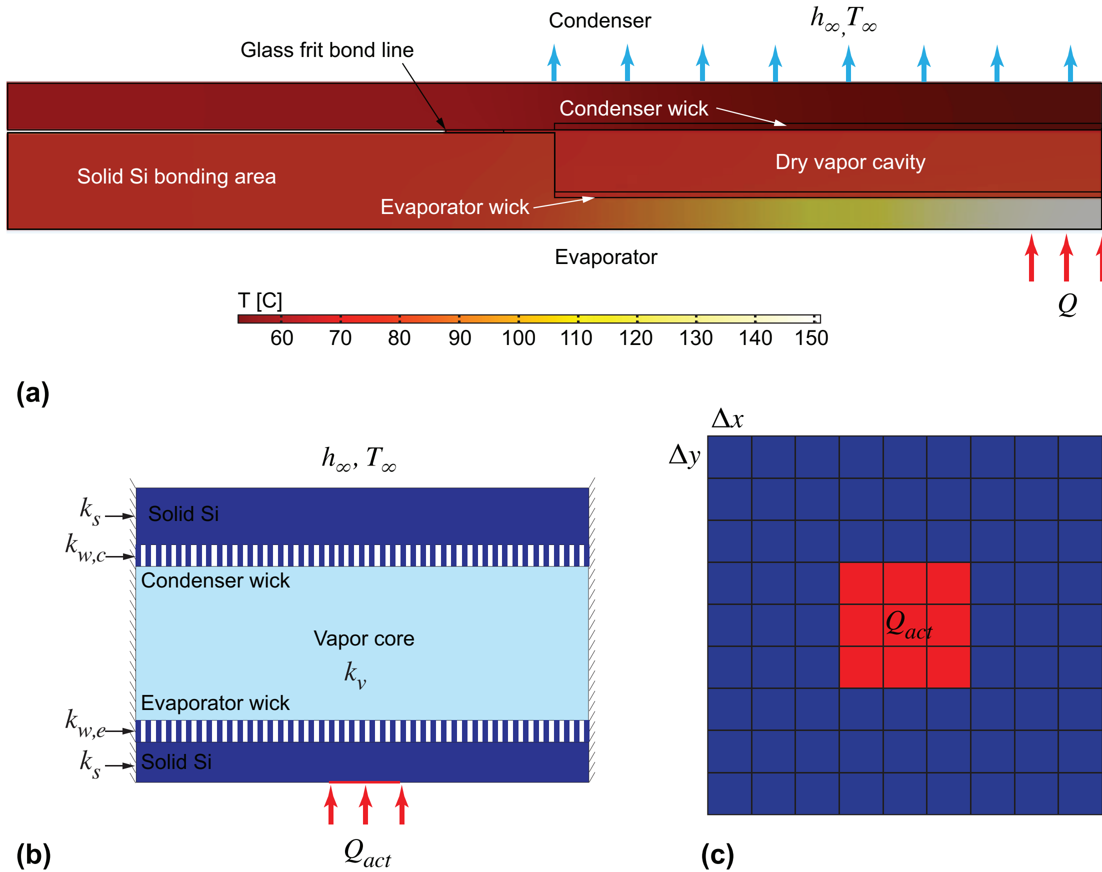

Figure 3-6. (a) Finite element simulation for input heat flux of 100 W/cm^2 to calculate conduction resistance through bonded device sidewalls, R_{side}, by approximating vapor chamber as a dry device with no working fluid. (b) Solid conduction model representation of vapor chamber with analytical influence coefficient method approach. Each component is treated as a solid block with a defined thickness and equivalent thermal conductivity as calculated from the sub-models described in sections 3.2.1 – 3.2.3. A uniform heat transfer coefficient is applied to the condenser side with a localized heat source on the evaporator side and insulated sidewalls. (c) Example grid

discretization to form 2D power map array of the source plane at the evaporator side heated surface.

The effect of each source on the total temperature excess throughout the stack is found through the principle of linear superposition applied to a Fourier series solution. This method has been validated against numerical simulation in various other works in literature, and further details can be found in [138–140]. Information regarding the contribution of each source to the temperature rise in a neighboring source is contained in an influence coefficient matrix, which transforms the solution for the net temperature distribution into a simple matrix equation as shown below

$$\begin{bmatrix} \psi_1 \\ \psi_2 \\ \psi_3 \\ \vdots \\ \psi_s \end{bmatrix} = \begin{bmatrix} f_{11} & f_{12} & f_{13} & \cdots & f_{1s} \\ f_{21} & f_{22} & f_{23} & \cdots & f_{2s} \\ f_{31} & f_{32} & f_{33} & \cdots & f_{3s} \\ \vdots & & & & \\ f_{s1} & f_{s2} & f_{s3} & \cdots & f_{ss} \end{bmatrix} \begin{bmatrix} q_1 \\ q_2 \\ q_3 \\ \vdots \\ q_s \end{bmatrix} \tag{3.21}$$

where ψ_i and q_i represent the temperature excess and heat flux at each source, and f_{ij} is the influence coefficient describing the effect of the ith source on the temperature excess in the jth source. R_{act} can then be extracted directly from the calculated temperature distribution for the heater area and condenser plane.

Finally, Q_{act} can be calculated from the relative resistance ratio of R_{side} and R_{act}, and the effective evaporator and condenser wick thermal conductivities as functions of Q_{act} are input into a solid conduction simulation in COMSOL to obtain the complete, three-dimensional temperature distribution within the vapor chamber. The total device resistance can then be calculated as

$$R_{vc} = \frac{T_{hs,avg} - T_{c,avg}}{Q} \tag{3.22}$$

The model flow to calculate $k_{w,c}$ and $k_{w,e}$ as functions of Q_{act} is shown in Figure 3-7.

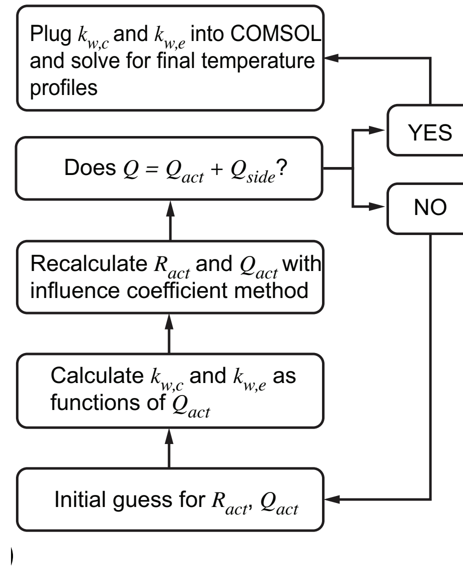

Figure 3-7. Flow chart showing calculation procedure to estimate active heat flow and heat flux dependent wick thermal conductivities. An initial guess is made for R_{act} and Q_{act}, then updated until an energy balance is satisfied.

3.2.5 Model Calculation Procedure

The overall system of equations for the evaporator/condenser wick sub-models and analytical influence coefficient model are programmed in MATLAB. Temperature dependent thermophysical properties of the working fluid are computed at each step based on tabulated values in literature using the average vapor temperature of the system, or $T_{v,avg}$ [141]. The general model calculation flow to find the vapor chamber thermal resistance as a function of total heat input, Q, and liquid charge mass, m_{ch}, is as follows:

1. Initialize a guess for the average vapor temperature, $T_{v,avg}$, condenser side liquid film thickness, h_{eff}, and active vapor chamber resistance, $R_{act.}$

2. Solve the condenser wick sub-model for $\Delta P_{lv,c}$, $k_{w,c}$, and m_c as functions of Q_{act}, h_{eff}, and $T_{v,avg.}$

3. Using the results from the condenser sub-model, set $\Delta P_{lv,c}$ as the boundary condition at i = 0 for the evaporator wick sub-model, solve for $k_{w,e}$ and m_e as functions of Q_{act} and $T_{v,avg}$.

4. Calculate the mass of vapor, m_v by treating it as an ideal gas with temperature and pressure equal to $T_{v,avg}$ and $P_{v,avg} = P_{sat}(T_{v,avg})$

5. Using $k_{w,c}$, $k_{w,e}$ and k_v as inputs to the analytical influence coefficient model, solve for an updated guess on $T_{v,avg}$ and R_{act} for heat input Q_{act}.

6. Check if $m_e + m_c + m_v = m_{ch} \pm 1\%$ and $Q_{act} + Q_{side} = Q \pm 1\%$. If not, repeat steps 1-5 until the tolerance is met.

7. Plug in $k_{w,c}$ and $k_{w,e}$ to COMSOL for a final calculation of the temperature distribution.

3.3 Experimental Methods

The approximate physical dimensions of the vapor chamber versus dimensions used in the model are tabulated in Table 3-1. For model simplicity and due to the relatively imprecise nature of the laser machining process, we approximate both the condenser side and evaporator side wicks as consisting of 100 μm tall, perfectly cylindrical pillars. The estimated difference in fully saturated wick liquid volume using the measured versus approximate model values is less than 6% when taking into account the conical shape of the fabricated pillars. Additionally, the serpentine heater is approximated as a uniform heat source in the evaporator wick model to simplify the unit cell calculations. To ensure that this assumption does not significantly impact model results, the solid conduction model was run for the case of 11.9 μL liquid charge volume with both heating distributions. The predicted values for the temperature distribution at the RTD measurement locations varied by less than 1.3 % when using a uniform heater versus the serpentine pattern. Based on these results, we concluded that the serpentine heat source can be reasonably represented by a uniform heat source, as sufficient heat spreading occurs in the solid silicon in between the patterned heating lines.

Table 3-1. Approximate dimensions versus model values for the silicon vapor chamber studied in this work.

Dimension	w_{vc} [mm]	w_{hs} [mm]	$t_{s,c}$ [μm]	$t_{w,c}$ [μm]	t_v [μm]	$t_{w,e}$ [μm]	$t_{s,e}$ [μm]
Actual Value	10	3.16	394±17	106±17	679±44	110±7	321±51
Model value	10	3.16	400	100	675	100	325

A custom electrical connector was designed and fabricated in order to power the evaporator side heater and collect measurements from the thin-film RTDs on both sides of the device. To avoid the tedious process of wirebonding a double-sided device, two arrays of spring-loaded pogo pins mounted in PEEK are used to electrically connect to either side of the vapor chamber in a sandwich configuration. A four-wire configuration is used for each of the RTDs and the serpentine heater to eliminate the issue of contact resistance between the pogo pins and patterned metal surface. One side of the pogo connector with no vapor chamber present is shown in Figure 3-8(a). The pogo pins are visible as the gold colored protrusions lining the center of the connector. An open window is purposefully left in the connector on both sides to allow for connection to a condenser side cooling mechanism and thermal insulation of the evaporator side. Figure 3-8(b) shows the fully assembled doubled-sided connector configuration with the evaporator side of the vapor chamber facing up. A detailed cross sectional view of the various components comprising the connectors is given in Figure 3-8(c). A miniature copper microchannel cold plate was designed for heat removal from the condenser side. To minimize parasitic heat loss through the non-active, solid bonding area of the vapor chamber, the contact area between the cold plate and vapor chamber was limited to only the 1 x 1 cm^2 active area of the vapor chamber through the use of a precisely sized thermal pad (Fujipoly). The temperature of the water supplied to the cold plate is maintained at 20^oC by an external chiller (Neslab RTE 7). Figure 3-8(d) shows the cold plate assembled with the electrical connectors and vapor chamber (hidden from view).

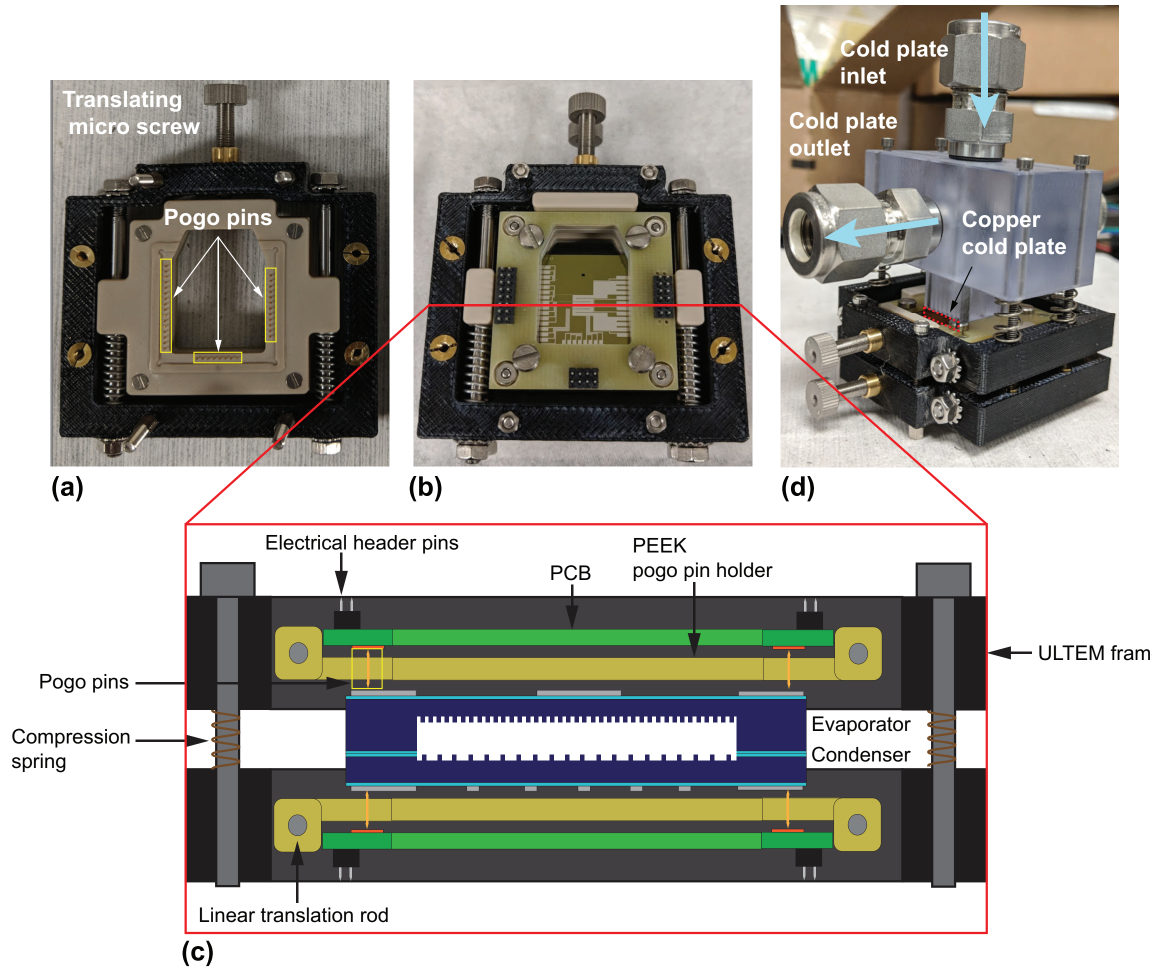

Figure 3-8. (a) Single side of electrical connector with pogo pins exposed. (b) Electrical connector assembled with vapor chamber sandwiched in between. (c) Cross sectional schematic of assembled electrical connector in (b). Each connector consists of a PEEK pogo pin holder mated to a custom PCB to facilitate connections from the pogo pins to external measurement equipment. Once pins are precisely aligned, both connectors are compressed to make the electrical connections with the vapor chamber heater and RTDs. (d) Cold plate assembled on top of condenser side of vapor chamber.

During the heat transfer experiments, power is supplied to the evaporator heater in steady increments through a DC power supply (BK precision 9206). A 5 mm layer of silicone insulation is mounted on top of the evaporator side of the vapor chamber to

prevent excessive heat loss to the environment. The voltage across the heater and resistances of the RTDs are monitored using a switching multimeter (Keithley DAQ 6510). Steady state is defined as the time at which the measured temperatures change at a rate of less than 0.05 ^{o}C/min over a 5-minute period. The RTDs are calibrated prior to the experiment by submerging the entire electrical assembly into a heated liquid bath and creating calibration curves for resistance versus temperature. A T-type thermocouple is attached to each side of the device, and the difference between the temperature readings from the two thermocouples is less than 0.3 ^{o}C at each bath set point, within the given accuracy range for Omega special limits of error T-type thermocouples of +/-0.5 ^{o}C. This reference thermocouple uncertainty dominates the experimental uncertainty in absolute temperature and thermal resistance. We estimate the heat loss from the device to the environment to be approximately 4% by running a finite element simulation in COMSOL with approximate system parameter values to account for natural convection to the environment and parasitic conduction through the solid silicon sidewalls. The reported heat flux values, q'', in the following sections represent the measured input heat flux, q_{inp}'', adjusted for 4% heat loss, with minimal error bars due to the high accuracy of the voltage and current measurements across the heater. The error bars reported for thermal resistance represent standard propagation of error incorporating the uncertainties in the steady-state temperature average and RTD calibration curves calculated for 95% confidence intervals.

3.4 Experimental Results and Model Validation

To verify the model, the thermal performance of the miniature silicon vapor chamber was characterized as both a function of heat flux and liquid charge following the experimental procedures detailed in the previous section. To preserve the device integrity for repeated liquid charge experiments, the maximum heat flux was limited in each case to approximately 103 W/cm^2 to avoid any sudden temperature overshoot. The maximum operational heat flux of the device may be higher, though that limit was not explored in this work since the primary aim was prediction of thermal resistance. Figure 3-9 shows the thermal resistance of the vapor chamber as defined by Equation (3.22) as a function of heat flux for a range of liquid charge volumes from 11.9 μL - 20.3 μL. The relatively

high uncertainty values at low heat fluxes are due to the fact that the measured temperature differences are close to the uncertainty of the temperature sensors (approximately ± 0.6 °C). The thermal resistance of the vapor chamber noticeably decreases with decreasing liquid charge and increasing heat flux. At the maximum heat flux considered of approximately 103 W/cm^2, increasing the injected volume from 11.9 μL to 20.3 μL increases the resistance by more than 300%. The resistance behavior of the device is similar for the two lower charge volumes of 11.9 μL and 12.9 μL, but a clear transition occurs when the charge volume is increased to 15.5 μL.

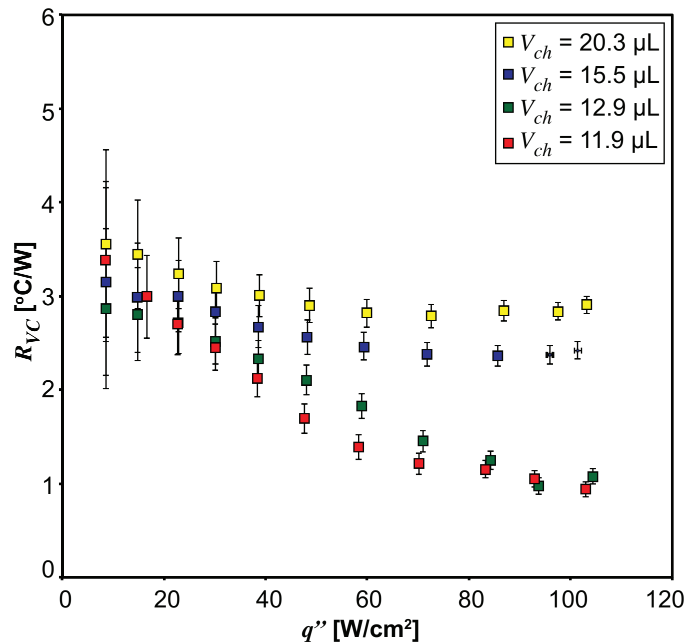

Figure 3-9. Vapor chamber thermal resistance, R_{vc}, versus heat flux for different liquid charge volumes ranging from 11.9 μL to 20.3 μL. The resistance decreases with increasing heat flux for all liquid charge volumes. Increasing the liquid charge from 11.9 μL to 20.3 μL at the highest heat flux level considered of approximately 103 W/cm^2 increases the resistance by more than 300%.

Figure 3-10(a) shows the model prediction against experimental results for the liquid charge volume of 12.9 μL with a range of different values for β, the fitting parameter to describe the enhancement in micropillar surface area due to the roughness

generated from laser ablation. The experimental best fit is for $\beta = 3$, representing an approximately 3x enhancement in the laser ablated micropillar surface area over perfectly smooth pillars. We obtain a separate measurement of the roughened micropillar surface area enhancement over a smooth surface using a 3D laser scanning confocal microscope (Keyence VK-X Series) with 120 nm lateral and 500 nm vertical resolution. The laser microscope scans the surface using 408 nm violet laser light and measures the reflected laser light to create a detailed 3D depth map of the object of interest. A direct surface area measurement of the micropillar sidewalls is difficult due to the underlying curvature of the cylindrical micropillar. Therefore, we measure instead the surface area enhancement of the sidewalls that form the vapor core cavity, which have relatively flat surfaces and are created during the same ablation process as the micropillars. An example line profile showing the roughness over a small area of the vapor core sidewall obtained using the laser microscope is shown in Figure 3-10(b). The average value for β returned by the microscope using an area scan over various portions of the sidewall is 8.3+/-3.3, the same order of magnitude as the model best fit. To provide another estimate, we also model the surface roughness based on the approximate values generated by the line profile as a uniform coating of 2 μm diameter pillars with 5 μm pitch and 3 μm height, which gives a lower bound of $\beta = 1.8$. The experimental best-fit value of $\beta = 3$ therefore seems a reasonable value and is used in all subsequent model calculations.

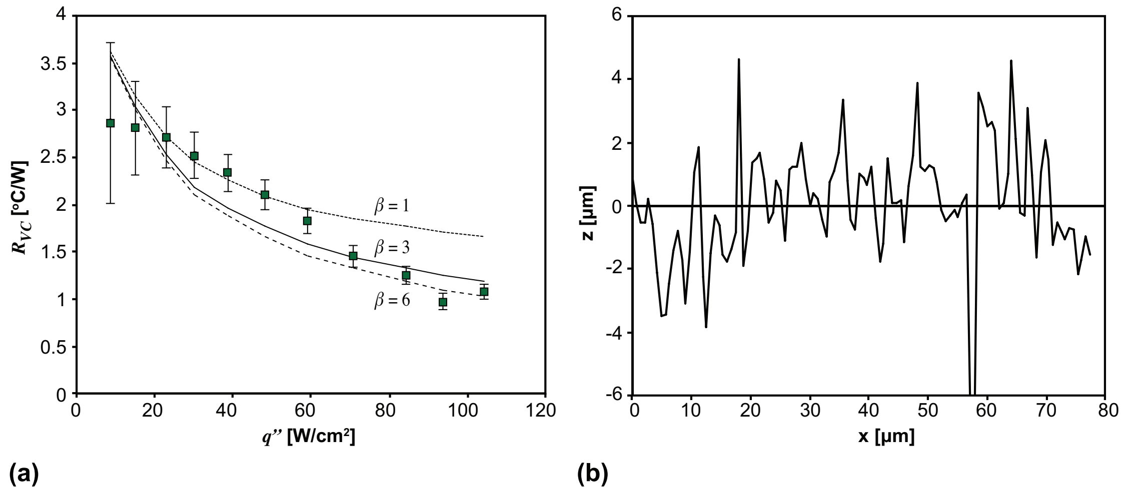

Figure 3-10. (a) Model fit against experimental data for 12.9 µL charge volume for β, surface area enhancement factor due to the roughness of the laser ablated micropillars. Best fit against experimental results is for $\beta = 3$. (b) Laser scanning line profile of surface roughness measured from vapor chamber sidewalls.

Figure 3-11(a) shows the experimental temperature profiles plotted against model results for RTDs T_{E7}, T_{E6}, and T_{E5} on the evaporator side of the vapor chamber. The model shows fairly good agreement with the experimental profiles for T_{E6} and T_{E5}, but overpredicts the temperature rise for T_{E7} at higher heat fluxes. This may be due to the fact that the model calculates an area averaged thermal conductivity for the evaporator wick by treating all of the micropillar unit cells in parallel, when in fact the local resistance near the center of the wick may be lower due to increased curvature of the meniscus. For a more exact treatment, it may be appropriate to extend the model to account for anisotropy in the effective wick thermal conductivity, though the area averaged model approach still shows good agreement with experimental results within 10%.

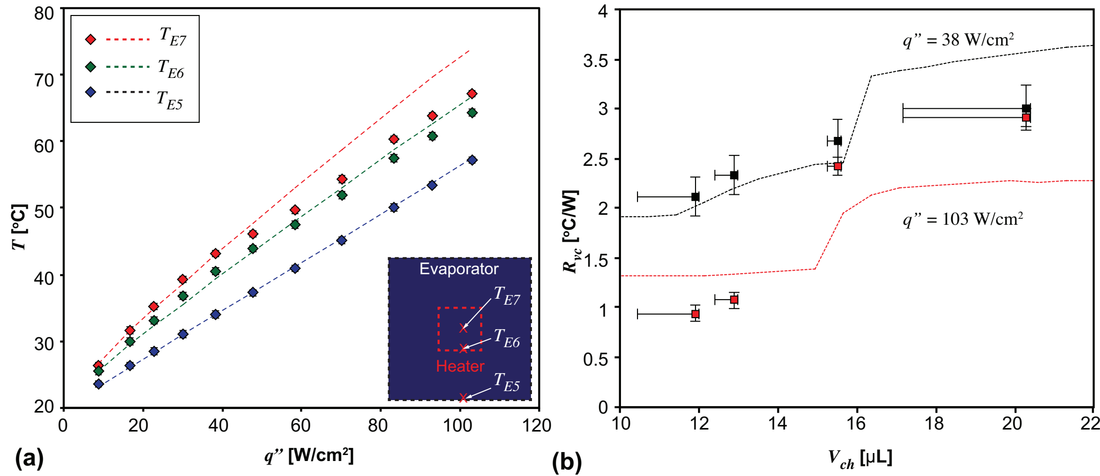

Figure 3-11. (a) Experimental data and model fit for temperature profiles at three different RTD locations of T_{E7}, T_{E6}, and T_{E5} on the evaporator surface as a function of input heat flux for a liquid charge of 11.9 μL. The location of the RTDs relative to the heater and overall evaporator area are shown in the inset. (b) Experimental data and model fit for thermal resistance at two different heat fluxes of 38 W/cm^2 and 103 W/cm^2 as a function of liquid charge. A clear transition point exists at charge volumes between 15-17 μL, above which the condenser becomes flooded and the device resistance increases drastically.

The model results for the vapor chamber thermal resistance as a function of liquid charge are plotted for two different heat fluxes of 38 W/cm^2 and 103 W/cm^2 against the experimental results in Figure 3-11(b). The resistance behavior of the vapor chamber shows a clear transition at liquid charge levels approaching a wick saturation ratio greater than 1. This is due to the formation of a flooded liquid layer on the condenser side wick that provides a significant series resistance to the overall device and creates an undesirable operational mode. The device resistance varies by approximately 0.05 ^{o}C/W/μL of liquid below the threshold value, but shows a sudden increase of around 0.5 ^{o}C/W/μL once the threshold is crossed. Proper identification of the threshold value and charging precision of at least +/- 2 μL around that value is therefore necessary to ensure optimal device performance. The threshold charge level also appears to shift to the left at the higher heat flux considered, as significant redistribution of liquid from the evaporator

to the condenser side can cause flooding to occur at lower charge levels. The net effect on the device resistance with increasing heat flux is then the interplay between a decreasing evaporator resistance and increasing condenser resistance. The model also implies that above a certain heat flux, decreasing the liquid charge level may no longer have a significant impact on the overall device resistance. For the maximum heat flux value considered of 103 W/cm^2, increasing the charge level from 10 μL to 15 μL shows a less than 6% change in total thermal resistance. Increasing the liquid charge by the same amount at the lower heat flux of 38 W/cm^2, however, causes the resistance to increase by more than 25%. The optimal liquid charge volume will therefore also depend on the desired operational heat flux of the device.

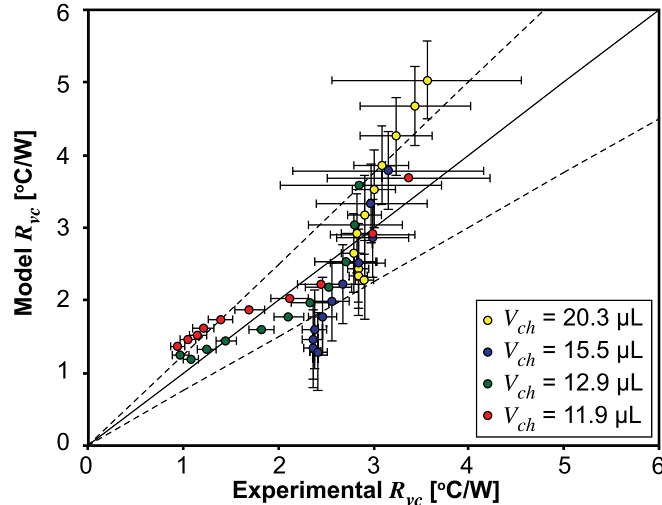

Figure 3-12. Model prediction for vapor chamber thermal resistance versus all data for experimentally measured thermal resistance. Overall, model prediction agrees with experimental values within 25%, with better agreement for lower liquid charge levels.

The complete experimental data set for thermal resistance is plotted against the model prediction in Figure 3-12. Overall, the model results agree with the experimental values within +/- 25%, though the agreement is closer for the lower levels of liquid charge. The majority of the model uncertainty comes from the uncertainty in the height of the micropillar wicks and subsequent saturated liquid charge volume. The predicted thermal resistance is particularly sensitive to the micropillar height in the flooded regime

and leads to a larger model uncertainty for higher liquid charge levels, as any extra liquid film formation on the condenser side contributes a significant series resistance. This may explain some of the model discrepancy for the liquid charge volumes of 15.5 uL and 20.3 uL. The model appears to consistently underpredict the values for the higher charge volumes in the lower resistance ranges, however, which implies that the effect of increasing heat flux is not decreasing the measured resistance values as much as the model prediction. This may be due to the fact that some flooding is actually occurring in the evaporator wick with the higher liquid charge levels, and the pinned evaporator meniscus model is not applicable over the full heat flux range considered.

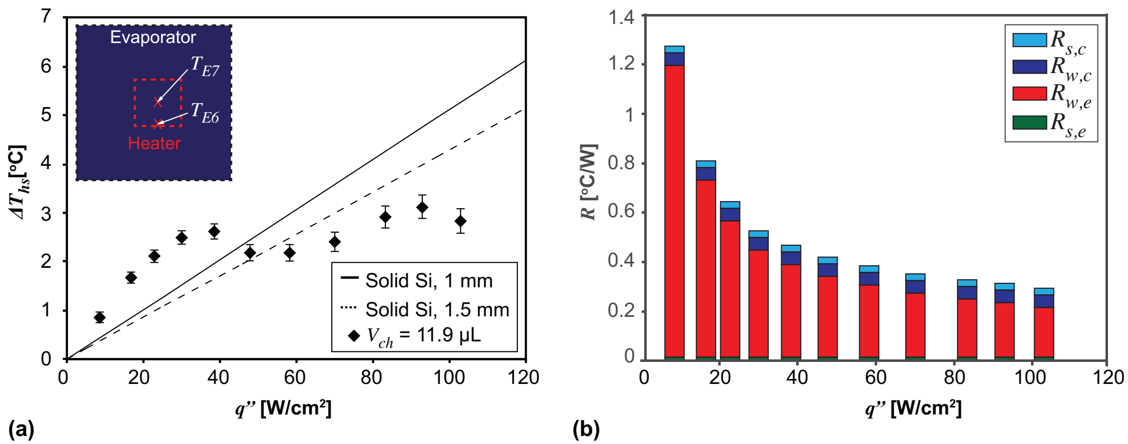

Figure 3-13. (a) ΔT_{hs}, or the difference between T_{E7} and T_{E6}, as a function of heat flux for simulated solid bare silicon slabs of 1 mm and 1.5 mm thickness, respectively, compared against experimental results for a liquid charge volume of 11.9 µL. The vapor chamber shows an improvement over the solid silicon slabs for heat fluxes above 60 W/cm^2. (b) 1D resistance stack up of various vapor chamber components as a function of heat flux for modeled liquid charge volume of 11.9 µL. The evaporator wick resistance, $R_{w,e}$, is strongly dependent on heat flux and dominates compared to the solid evaporator/condenser silicon resistances, $R_{s,c}$ and $R_{s,e}$, and condenser wick resistance, $R_{w,c}$.

To benchmark the miniature vapor chamber thermal performance, simulations were performed in COMSOL for two solid silicon slabs of different thicknesses with the same heating and condenser side cooling boundary conditions as the vapor chamber experiment. A direct comparison with other existing silicon vapor chambers is difficult

due to the different form factors and innate spreading resistances involved. Therefore, solid silicon slabs were chosen as an appropriate baseline case to assess the potential benefit of using the miniature vapor chamber for die-level heat spreading. Figure 3-13(a) compares the experimental results for the vapor chamber with 11.9 μL liquid charge for the temperature drop across the hotspot, ΔT_{hs} , defined as T_{E7}-T_{E6}, with the simulation results for solid silicon slabs of 1 mm and 1.5 mm thickness. The total vapor chamber thickness of 1.5 mm was chosen primarily for ease of fabrication to enable a one-step etch to define the vapor core, but leaves approximately 400 μm of solid silicon on the condenser side with minimal contribution to the thermal spreading performance. As the overall stack thickness can be easily reduced to 1 mm or thinner without impacting the vapor chamber performance by dividing the vapor core between the evaporator and condenser side wafers, we include the 1 mm thick solid silicon slab as a benchmark of a more realistic commercial form factor. The vapor chamber shows an improvement in hotspot temperature non-uniformity over both the 1.5 mm and 1 mm slabs of approximately 36% and 46%, respectively, at the maximum heat flux considered. At heat fluxes below 60 W/cm^2, however, the vapor chamber has no clear benefit over a solid spreader.

To investigate the origin of this threshold heat flux, we use the model to examine the various components that form the 1D resistance stack of the vapor chamber in Figure 3-13(b). The evaporator wick resistance, $R_{w,e}$, dominates compared to the condenser wick resistance, $R_{w,c}$, as well as the solid silicon resistances on both sides of the device, $R_{s,e}$ and $R_{s,c}$. $R_{w,e}$ decreases with increasing heat flux due to two simultaneous effects: an increase in the thin-film area with increasing rates of evaporation, as well as a decrease in interfacial resistance with increasing temperature. At heat fluxes above 50 W/cm^2, the evaporator wick shows a diminishing dependence on heat flux and appears to approach a minimum resistance value of approximately 0.2 ^{o}C/W. This corresponds to the experimental trends observed in Figure 3-13(a), where the vapor chamber appears to become more effective at heat fluxes higher than 50-60 W/cm^2. Operating at a higher condenser side temperature to decrease the interfacial resistance throughout the device would perhaps extend the effective vapor chamber range to lower heat fluxes, as would

moving to an evaporator wick structure with a lower thermal resistance. The strong heat flux dependence of $R_{w,e}$ at lower heat fluxes implies that for the wick dimensions considered, the interfacial and thin-film resistances have a large contribution to the overall stack resistance. The minimum wick resistance value may ultimately be limited by the conduction resistance across the wick, however, so simultaneously moving to a higher density and thinner micropillar wick could be an effective solution to reduce the overall thermal resistance of the device and improve the low heat flux performance. A higher density and thinner wick may also potentially reduce the maximum capillary-limited heat dissipation capability of the vapor chamber, however, so careful consideration of both the thermal properties as well as fluidic transport is necessary for future design optimization.

It is clear from Figure 3-13(a) that the miniature vapor chamber will have a much more significant improvement compared to a solid spreader of the same dimensions if it can be reduced to a thinner form factor. As the only high thermal conductivity portion of the vapor chamber is the vapor core, the extra silicon thickness on the condenser side in the current form factor only serves to obscure the effectiveness of the phase change region when compared to a solid spreader of equal dimensions. Reducing the overall vapor chamber thickness to 1 mm should have minimal impact on the current thermal performance, and provides a much more significant improvement over the solid silicon equivalent.

3.5 Conclusions

A miniature vapor chamber with an active vapor transport region of 1 x 1 cm^2 was fabricated and experimentally characterized for a range of liquid charge volumes and heat flux inputs. A model was developed to predict the impact of both heat flux and liquid charge on the vapor chamber thermal performance and experimentally validated to agree within +/-25%. The model demonstrates that the liquid charge dependence of the vapor chamber resistance increases sharply near the wick saturation threshold due to the flooding of the condenser wick and creates an undesirable high thermal resistance operational mode. The evaporator wick resistance dominates the overall 1D vapor

chamber resistance stack and decreases with increasing heat input. Above a certain heat flux level, however, the heat flux dependence of the wick diminishes and approaches a minimum value.

The vapor chamber thermal performance was benchmarked against simulation results for solid silicon spreaders of varying thickness. The current prototype vapor chamber thickness of 1.5 mm contains extra silicon thickness on the condenser side with minimal thermal impact that makes for a relatively ineffective comparison with an equivalent solid silicon spreader. The experimental results did demonstrate, however, that the vapor chamber shows superior temperature uniformity over a 1 mm thick solid spreader for heat fluxes greater than 50-60 W/cm^2. If the unused silicon can be removed, the vapor chamber can achieve significant improvement in thermal performance over a solid silicon spreader of equivalent thickness and effectively improve die-level temperature uniformity over an area as small as 1 x 1 cm^2.

The modeling methodology developed in this work can be used to aid the design of future small-scale vapor chamber heat spreaders. The thermal performance of the vapor chamber is dependent on a number of internal as well as system design parameters, and due to the small spreading distances considered, may not always have an obvious impact over a solid spreader of equivalent dimension. Comparison of the model with experiment results elucidates the primary resistance components that dominate the vapor chamber performance, as well as the sensitivity of the vapor chamber performance to the liquid charge level. Due to the small liquid charge volume involved (on the order of microliters), this provides important guidelines to aid the process development of other future microscale devices. This work shows that there is potential benefit for vapor chambers to be implemented over spreading areas as small as 1 x 1 cm^2, but careful assessment of different parameters such as the desired operating heat flux range is necessary to determine whether or not such a small-scale device is beneficial.

Chapter 4

Passive Thermal Regulation with Binary Vapor Diffusion: Steady-State Characterization

This chapter presents an investigation of the steady-state thermal regulatory characteristics of a novel device utilizing binary vapor diffusion through a non-condensable gas cavity. Large portions of this chapter have been taken from Liu et al., "Tunable, Passive Thermal Regulation Through Liquid to Vapor Phase Change," *Applied Physics Letters*, 2019 [142], as well as Liu et al., "Steady-state Parametric Optimization and Transient Characterization of Heat Flow Regulation with Binary Diffusion," *IEEE TCPMT*, 2020 [143].

4.1 Thermal regulation with liquid-vapor phase change

As mentioned in section 1.3, thermal regulators and switches have the potential to greatly aid in the thermal management of spatially and/or temporally varying heating events. One of the most widely studied mechanisms to control the thermal resistance between hot and cold surfaces is by improving/suppressing conduction heat transfer through making and breaking mechanical contact [37,39,43,144–147]. A potential issue with these types of switching mechanisms, however, is mechanical fatigue after repeated deformation [148]. Other mechanisms such as solid-state phase transitions are also limited by relatively fixed switching temperature ranges only tunable through permanent procedures such as doping [49].

Liquid-vapor phase change is a relatively tunable, nonlinear thermal process that can be harnessed for thermal regulation [30,38,149]. One challenge, however, is packaging the devices in a compact form factor that can be easily integrated with existing electronic systems. Variable conductance heat pipes, for instance, are highly effective

temperature regulators but require a large condenser area to function, limiting their use to large-scale devices such as Stirling engines [150].

In this chapter, we present a passive, tunable thermal device that utilizes vapor transport in a non-condensable gas (NCG) cavity to achieve a switchable thermal resistance in response to varying levels of heat flow. Compared to existing liquid-vapor phase change regulators, the device is relatively compact with an active working area of 1 x 1 cm^2. In addition to a switchable resistance, the device is able to clamp the hot and cold sides to a heat flow independent temperature difference. The resistance switching and clamped temperature difference, ΔT_{cr},, are tunable based on the pressure of the NCG. We present a roadmap to increase the steady-state resistance off/on ratio utilizing this phenomenon to greater than 14, and define a switching efficiency metric to assess the effectiveness of the device design.

4.2 Steady-state thermal model

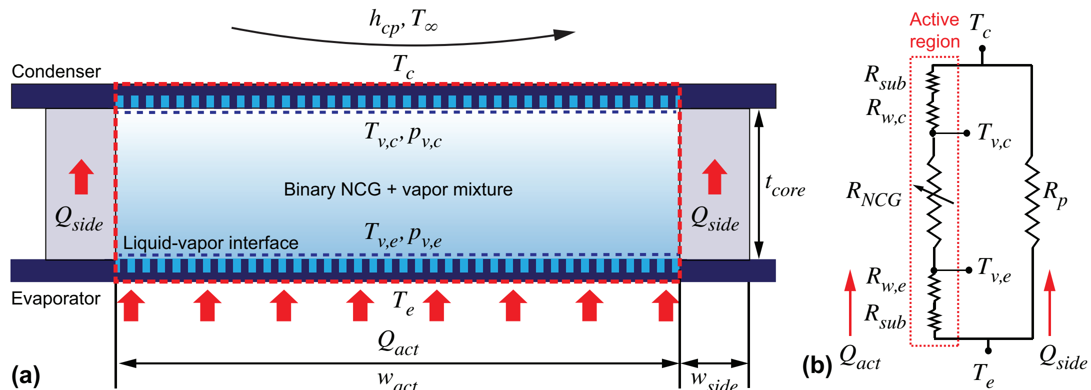

Figure 4-1. (a) Thermal regulator cross-sectional schematic. Heated liquid evaporates from a porous wick, diffuses through an NCG-filled cavity to reach the cold side of the device, then condenses and circulates back to the heated side through capillary action. Parasitic conduction occurs through the device sidewalls. (b) Steady-state thermal resistance network for the temperature drop across the device. The resistance R_{NCG} varies with P_{NCG} and total heat input, creating the device thermal regulatory properties.

Figure 4-1(a) shows a cross-sectional schematic that highlights the main working principles of the regulator. The device is comprised of a sealed chamber lined with a porous micropillar wick and charged with a fixed amount of working fluid (water) and NCG (air). Heat applied to the evaporator side of the device causes fluid in the porous wick to evaporate then diffuse through the NCG to the condenser side, where it condenses into liquid. Capillary action then drives the condensed liquid back to the evaporator side, and the cycle repeats. The NCG acts as a diffusion barrier to the vapor transport and has an equivalent thermal resistance, R_{NCG}, that varies based on the pressure of the NCG, P_{NCG}, as well as the temperature difference between the hot and cold sides, ΔT. As ΔT increases, the vapor mass fraction gradient also increases and has a nonlinear effect on the vapor transport, reducing R_{NCG}.

The resistance network shown in Figure 4-1(b) approximates the steady state heat transfer across the device. Heat supplied to evaporator side travels in two parallel pathways, with one portion, Q_{act}, going through the device active phase change region (outlined in red in Figures 4-1(a)-(b)), and the other portion, Q_{side}, going through the device sidewalls. The parallel sidewall conduction resistance, R_p, can be estimated through a solid conduction simulation of the device with a dry cavity. The resistance stack in the device active region includes the solid substrate, R_{sub}, the evaporator/condenser wick resistances, $R_{w,e}$ and $R_{w,c}$, respectively, and the NCG/vapor mixture resistance, R_{NCG}. T_e and T_c represent the average temperatures of the evaporator and condenser side substrates, respectively.

Based on the resistance network shown in Figure 4-1(b), a few design guidelines emerge to optimize the resistance contrast across the device. Since R_{NCG} is the only significantly variable resistance component, any parallel or series resistance components will minimize the overall resistance contrast. R_p should ideally be much larger than R_{NCG}, otherwise parasitic heat flow outside of the active region leads to an undesirable thermal shunting effect that shorts the regulator. Any series resistances should ideally be as low as possible to avoid inflating the on-state resistance and decreasing the switching

contrast. The following sections will present physics-based models to predict the approximate values of the various parallel and series resistance components.

4.2.1 Vapor transport model

We estimate the temperature drop across the vapor/NCG mixture by considering the vapor mass diffusion problem between the evaporator and condenser wick interfaces. The introduction of NCG presents a significant diffusion barrier to vapor transport between the evaporator and condenser. Here we leverage the NCG to achieve a switchable device resistance due to the decrease in effective NCG resistance, R_{NCG} with increased operating temperatures and heat fluxes. In the following model, we assume that the NCG and vapor exist as a binary mixture. The local component partial pressures may therefore be written in terms of the total chamber pressure as

$$P_{tot} = P_{NCG} + P_v \tag{4.1}$$

The local mass fractions are described by

$$\omega_v = \frac{\chi_v M_v}{\chi_v M_v + (1-\chi_v) M_{NCG}} \quad , \quad \omega_{NCG} = \frac{(1-\chi_v) M_{NCG}}{\chi_v M_v + (1-\chi_v) M_{NCG}} \tag{4.2}$$

where χ_v is the local vapor mole fraction, and M_v and M_{NCG} are the vapor and NCG molecular weights, respectively.

We assume that the vapor directly above the evaporator/condenser porous wick interfaces is saturated [151], and the interface temperatures ($T_{v,e}$ and $T_{v,c}$) can be related to the vapor partial pressures ($P_{v,e}$, $P_{v,c}$) through the Clausius-Clapeyron equation. In steady state, all the liquid being evaporated must be condensed. We neglect condensation along the cavity sidewalls due to the much smaller surface area and lower external heat transfer coefficient compared to the active condenser region. Therefore, the vapor transport is one-dimensional, and

$$\frac{d\dot{m}_v}{dz} = 0 \tag{4.3}$$

$\dot{m}_v$ represents the total vapor mass flux, and the z coordinate represents the vapor flow direction between the evaporator and condenser.

Heating and cooling at the evaporator/condenser surfaces sets up a temperature gradient across the mixture space, resulting in a corresponding vapor mass fraction gradient. This mass fraction gradient then drives the vapor transport through the NCG barrier. Assuming insignificant dissolution of NCG at the porous wick interfaces creates a no-penetration boundary condition, where the NCG must be stationary and $\dot{m}_{NCG} = 0$. The vapor mass fraction gradient, however, creates a complementary NCG mass fraction gradient and diffusional mass flux, leading to a Maxwell-Stefan flow scenario [152]. In order to meet the zero net NCG mass flux condition, an induced counterdiffusion velocity accounting for bulk flow of the mixture counteracts the diffusional NCG flux. In steady state, this leads to the following vapor mass flux equation where

$$\dot{m}_v = \omega_v \dot{m_{tot}} - \rho_m D_{vg} \frac{d\omega_v}{dz} \tag{4.4}$$

ρ_m is the mixture density and D_{vg} is the temperature dependent, binary diffusion coefficient calculated based on Chapman-Enskog theory[152].

From an energy balance in the device active region,

$$Q_{act} = \dot{m}_v h_{fg} A \tag{4.5}$$

where h_{fg} is the working fluid latent heat of vaporization and A is the cross sectional area normal to the vapor transport. Substituting Equation (4.5) into Equation (4.5) and integrating with respect to z links the active region heat transfer with the vapor transport equation, where

$$Q_{act} = \frac{\rho_m D_{vg} \dot{h_{fg}} A}{t_{core}} ln\left(\frac{\omega_{v,c} - 1}{\omega_{v,e} - 1}\right) \tag{4.6}$$

$\omega_{v,c}$ and $\omega_{v,e}$ are the vapor mass fractions at the condenser and evaporator sides, respectively, and t_{core} is the transport distance, or cavity height.

4.2.2 Wick resistance model

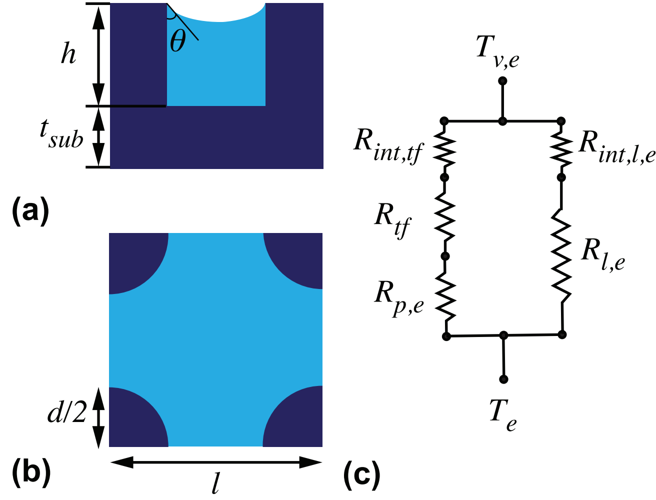

Figure 4-2. (a) Micropillar wick unit cell cross-sectional view. (b) Top view of micropillar wick with diameter *d* and pitch *l*. (c) Evaporator micropillar wick resistance network.

Figure 4-2(a) shows a cross-sectional schematic of the micropillar wick and underlying substrate. The substrate thermal resistance can be calculated through a one-dimensional conduction resistance. The evaporator micropillar wick resistance is evaluated by considering the heat transfer in a unit cell. Assuming that $k_{sub} >> k_{liq}$, the solid pillar resistance is calculated as

$$R_{p,e} = \frac{4h}{k_{sub}\pi d^2} \tag{4.7}$$

where h and d are the pillar height and diameter, respectively as shown in Figures 4-2(a)-(b). The bulk liquid conduction resistance is described by

$$R_{l,e} = \frac{h}{k_{liq}(l^2 - \frac{\pi d^2}{4})} \tag{4.8}$$

where l is the micropillar pitch. With the exception of cases involving high thermal conductivity fluids such as liquid metals, $R_{p,e}$ is typically much less than $R_{l,e}$, and the majority of the heat traveling through the wick evaporates from a thin liquid film near the

meniscus three-phase contact line. We estimate this thin-film resistance by calculating the area of an approximately 5 μm thick liquid film around the micropillar surface for a given contact angle of θ through a force balance model in COMSOL.

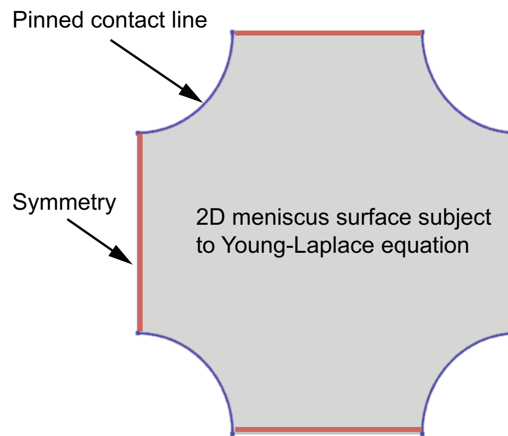

Figure 4-3. Boundary conditions for 2D force balance model used to generate the appropriate meniscus shape and calculate the capillary pressure for the micropillar dimensions considered.

The meniscus is modeled as a 2D surface as shown in Figure 4-2(a), with pinned constraints applied to the micropillar contact lines, and symmetry conditions at the remaining borders. The curvature of the meniscus is then calculated through a numerical solution of the Young-Laplace equation in COMSOL subject to an applied pressure that represents the capillary pressure difference across the wick interface. Further details of the calculation can be found in [94]. Different applied pressure differences lead to different contact angles between the meniscus and micropillar surface, and the pressure is swept until a contact angle of approximately 70° is reached, corresponding to the advancing contact angle of water on SiO_2 [89]. The generated meniscus shape is then used to calculate the thin-film area for the evaporator micropillar resistance model, and the applied pressure is taken as the capillary pressure of the entire wick.

The thin-film conduction resistance, R_{tf}, is calculated by integrating the thin-film profile, treating each infinitesimal slice of liquid as a parallel resistor. Details of the thin-film resistance calculation can be found in section 3.2.1. As the applied heat flux increases, the meniscus recedes within the micropillar wick, increasing the thin-film area

and reducing the overall resistance. This effect is significant in vapor chambers and heat pipes where the evaporator resistance normally dominates the overall system resistance [25], but is expected to be minimal when the NCG resistance dominates. Therefore, we neglect any variation in the thin-film area with applied heat flux and use a fixed contact angle, θ, to calculate the evaporator wick resistance. Finally, the liquid-vapor interfacial resistances in the thin-film and bulk liquid regions are calculated with the Schrage equation as given by Equation 3.8. Figure 4-2(c) shows the overall resistance network for the evaporator wick.

The treatment of the condenser wick resistance is relatively simpler than the evaporator wick, as condensation is expected over the micropillar top surfaces as well as the liquid bulk. We therefore assume parallel heat conduction through the micropillar wick and liquid bulk with an effective thermal conductivity where

$$k_{w,c} = \phi k_{liq} + (1-\phi)k_{sub} \tag{4.9}$$

and ϕ is the volume fraction of the wick.

The final system of equations for the overall device resistance network is solved iteratively with the Trust Region Dogleg method in MATLAB to find the temperatures at each resistance node. The total device resistance is defined as

$$R_{th} = \frac{T_e - T_c}{Q} \tag{4.10}$$

where Q is the total heat input and equal to the sum of Q_{act} and Q_{side}.

Temperature-dependent thermophysical properties of the working fluid are calculated based on tabulated values in literature [152]. Temperature-dependent mixture properties such as the mixture density, binary diffusion coefficient, and total chamber pressure are evaluated using a mean temperature, T_m, that represents the average of the evaporator and condenser side vapor temperatures, where

$$T_m = \frac{1}{2}(T_{v,e} + T_{v,c}) \tag{4.11}$$

4.3 Experimental Methods

4.3.1 Device fabrication

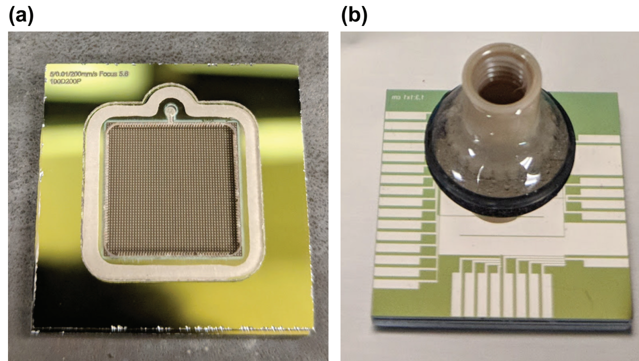

Figure 4-4. (a) Image of Pyrex frame overlaid on top of the 1 x 1 cm^2 micropillar wick area on one side of the device after glass frit bonding. The charging port is visible as the circular through-hole at the top center of the wick and Pyrex insert. (b) Fully bonded device with Nanoport attachment and part of 1 x 1 cm^2 serpentine heater area visible. The face seal o-ring is not visible, and the outer o-ring is used to prevent overflow of the epoxy. Additional metal pads are visible around periphery of the device for extra RTDs that were not used in this experiment.

The device is fabricated from two 500 um thick pieces of silicon bonded to a Pyrex insert. Approximately 500 nm of thermal oxide is grown onto each silicon wafer to provide electrical insulation for the deposition of a 1 x 1 cm^2 serpentine platinum thin-film resistor. The thin-film resistor simultaneously serves as a heater and resistance temperature detector (RTD) during the thermal experiments to measure the area averaged temperature on the hot and cold sides, T_e and T_c. The heaters/RTDs are fabricated by depositing 120 nm of platinum with a 5 nm chromium adhesion layer using standard photolithography, metal evaporation, and lift-off techniques. After the heater/RTD fabrication, a micropillar array with approximately 100 um diameter, 200 um pitch, and 100 um height is etched into the opposite side of the silicon using ultra-violet laser

ablation to act as the porous wicking material within the device. A 750 um diameter outlet through-hole is etched into one side of the device to facilitate liquid charging and NCG injection. The Pyrex frame is similarly fabricated through laser ablation, and a sawtooth groove structure is etched around the periphery of the cavity to enable condensate return from the cold side to the hot side. An approximately 400 um wide, 20 um thick glass frit bond line is printed onto each piece of silicon, and all pieces are joined and fired at 450^oC to perform the final seal. Figure 4-4(a) shows an image of the Pyrex frame after glass frit bonding to one side of the device.

After bonding, a 1 mm bead of epoxy is added around the Pyrex frame for additional mechanical stability and secondary sealing. As a final step, a Nanoport for external fluidic connections is mated to the solid silicon surface surrounding the through-hole with an o-ring face seal (Figure 4-4(b)). Epoxy is then applied to the port with the o-ring under compression to maintain the seal. The epoxy used to maintain the Nanoport seal (Devcon 2-ton) has a maximum recommended working temperature of approximately 95 ^oC. Therefore, the total input power in each experiment is limited to approximately 14 W in order to prevent degradation of the epoxy and leakage through the Nanoport bonding surface at temperatures significantly higher than the maximum rating. The active phase change region of the completed device is 1 x 1 cm^2 with a cavity thickness of 500 um, and total stack thickness of 1.5 mm. The total area is 2 x 2 cm^2 to allow space for bonding and electrical contact pads.

Table 4-1: Summary of approximate device dimensions, with active region width w_{act}, Pyrex insert width w_{side}, Pyrex insert and vapor/NCG cavity thickness t_{core}, solid silicon substrate thickness t_{sub}, and micropillar wick height, diameter, and pitch of h, d, l, respectively.

Parameter	w_{act} [mm]	w_{side} [mm]	t_{core} [μm]	t_{sub} [μm]	h [μm]	d [μm]	l [μm]
Value	10	1.8	500	400	100	100	200

4.3.2 Experimental procedure

Prior to each experiment, the device is charged with approximately 14 μL of deionized, ultra-filtered water. A copper cold plate connected to a chiller maintained at a bath temperature of 20 ^oC is mounted to the condenser side of the device. The device is then evacuated until the total chamber pressure reading from a pressure transducer is approximately equal to the saturation pressure of water at 20 ^oC, or 2.3 kPa. Ambient air is then re-injected slowly into the device until the desired total chamber pressure set point is reached. The total pressure reading P_{tot} is used in the model to calculate the starting NCG pressure, P_{NCG}, assuming that the partial pressure of the vapor is equal to the saturation pressure at 20 ^oC. The effective thermal resistance across the device is defined as $R_{th} = \Delta T/Q$, where ΔT is calculated as the difference of the area-averaged temperatures of the hot and cold sides, $T_e - T_c$, and Q is the total heat input. During experiments, the power to the hot side heater is incremented in a step-wise manner with a DC power supply (BK Precision 9206). For a more precise measurement of the supplied power, a 4-wire measurement of the voltage across the heater and a separate measurement of the sourced current are obtained with an external multimeter. The device is judged to have reached steady state after the average change in the measured temperatures over a 5 minute time interval is less than 0.06 ^oC /minute. The final reported temperature readings are taken as the average of 150 samples over a 5 minute time period after the device reaches steady state.

4.3.3 Uncertainty analysis

We perform standard error propagation analysis to estimate the uncertainty in the two primary parameters of interest, ΔT and R_{th}. We estimate the heat loss, or difference between Q_{in} and Q_{out} by performing finite element simulations in COMSOL of the device with approximate boundary conditions to replicate the experimental test conditions. A heat transfer coefficient of 2,600 $Wm^{-2}K^{-1}$ representing the copper cold plate is applied over a 1 x 1 cm^2 area on the cold side of the device, and a natural convection coefficient of 10 $Wm^{-2}K^{-1}$ is applied to all remaining exposed areas. A 5 mm thick piece of silicone insulation is placed over the heated area to provide additional thermal insulation during

experiments and is included in the simulation as a block with an approximate thermal conductivity of 0.15 $Wm^{-1}K^{-1}$. The Pyrex insert and 1 mm wide epoxy bead are assigned thermal conductivities of 1 $Wm^{-1}K^{-1}$ and 0.3 $Wm^{-1}K^{-1}$, respectively. Since the effective thermal conductivities of the wick and non-condensable gas are not known *a priori*, a range of values are considered for each as a part of a sensitivity analysis. The estimated heat loss for the range of k_{NCG} and k_w considered is shown in Table 4-2. From the results, we can see that the heat loss is not particularly sensitive to k_{wick} (only 0.6% variation in expected heat loss for k_w = 1- 10 $Wm^{-1}K^{-1}$). The heat loss varies between 4.8%-7.7% for the range of k_{NCG} considered and becomes insensitive for k_{NCG} > 10 $Wm^{-1}K^{-1}$. For the remainder of the analysis, we approximate the heat loss with a fixed value of 6% and include +/- 1.5% in the uncertainty calculation.

Table 4-2. Finite element simulation results to estimate heat loss in experimental set up for different values of NCG/vapor mixture effective thermal conductivity, k_{NCG}.

k_w [$Wm^{-1}K^{-1}$]	k_{NCG} [$Wm^{-1}K^{-1}$]	Q_{in} [W]	Q_{out} [W]	% heat loss
5	0.25	10	9.23	7.7
5	1	10	9.36	6.4
5	2.5	10	9.44	5.6
1	5	10	9.42	5.8
5	5	10	9.48	5.3
10	5	10	9.49	5.2
5	10	10	9.50	5.0
5	25	10	9.52	4.9
5	50	10	9.52	4.8

To calibrate the thin-film platinum serpentine resistors for use as RTDs, the entire set up is submerged into a recirculating liquid bath with one thermocouple attached to each side of the device (Omega T-type, Special Limits of Error). The thermocouples are previously calibrated against a high accuracy platinum reference probe (Fluke 5615-12-J)

to an accuracy of +/- 0.1°C. The agreement between the two reference thermocouples at each bath set point is typically within 0.05 °C, which is within the ±0.1 °C uncertainty of the thermocouples. The resistors on each side of the device are then calibrated based on the average of the two reference thermocouple temperatures to extract the linear temperature coefficient of resistance for each, α. The uncertainty in absolute temperature measured by the RTDs is thus the combination of the 95% confidence interval uncertainty in the steady state average and the uncertainty in absolute temperature based on the resistance to temperature conversion equations of the RTDs. The uncertainty in the average cold side temperature is approximately ±0.4 °C, and the uncertainty in the average hot side temperature is approximately ±0.7 °C, with a larger uncertainty due to the fact that the resistor is simultaneously subjected to a heating current. The uncertainty in R_{th} is calculated from standard propagation of error including the uncertainty in absolute measured temperature and the uncertainty in the total heat input due to heat loss. The approximate uncertainties for the various the components in the system are given in Table 4-3.

Table 4-3. Approximate errors from the instrumentation and resistance-temperature calibration curves for each RTD.

T_{ref} error, u_{Tref} [°C]	Resistance measurement error, u_R [Ω]	α error, u_α [1/°C]	Voltage measurement error [V]	Current measurement error [A]
±0.1	±0.02	8e-6	1e-3	1e-4

4.4 Steady-state thermal behavior

4.4.1 Resistance switching

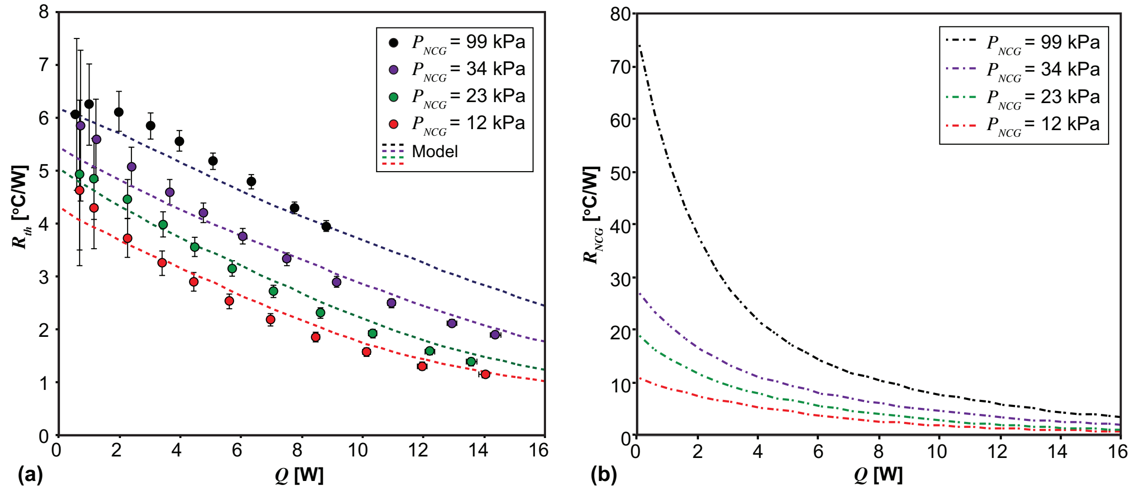

Figure 4-5. (a) Steady state experimental results for overall device resistance, R_{th}, for P_{NCG} = 12 kPa – 99 kPa. Model prediction is shown with dashed lines. (b) Model predictions for R_{NCG} as a function of heat input for P_{NCG} = 12-99 kPa. The achievable resistance contrast in R_{NCG} is much greater than what manifests in the total device resistance, R_{th}, due to parallel and series resistance components.

The steady state model results for the device thermal resistance, R_{th}, as a function of input power are plotted with the experimental results for different levels of P_{NCG} in Figure 4-5(a). Due to the maximum temperature limitation of the charging port sealing epoxy, the maximum heat input for P_{NCG} = 99 kPa is limited to 9 W. The model shows reasonable agreement with the experimental results and captures the decrease in R_{th} with increasing power, as well as the shift in R_{th} with varying P_{NCG}. Increasing P_{NCG} raises the vapor mass transport resistance and increases R_{th} for a given heat input. Raising P_{NCG} from 12 kPa to 99 kPa, for instance, causes R_{th} to increase by approximately 1.5 times. For a given NCG charging pressure, the vapor mass fraction gradient between the hot and cold sides increases as more heat is supplied and reduces the effect of the NCG. This is evidenced by the steady decline of R_{th} with increasing Q for the different P_{NCG} considered. With NCG present, the device essentially acts like a thermal switch that

responds passively to variations in Q. When placed in parallel with a temperature sensitive component of comparable resistance, the switchable R_{th} behavior could be leveraged in combination with a heat spreader or similar to act as a heat flow surge protector. If an active regulation scenario is desired, the amount of NCG could be utilized as the switching mechanism by dynamically modulating P_{NCG} at a given heat flow input. The dynamic scenario opens up a larger range of possibilities for device operation, but would require the implementation of a freezing cycle or additional system level components to prevent excess loss of water vapor during multiple chamber evacuation/pressurization cycles. For the remainder of the analysis, we therefore focus primarily on the passive scenario, where P_{NCG} would be tuned and preset during device fabrication to obtain the desired operating characteristics.

We evaluate the resistance switching in terms of the conventional switching ratio metric, or R_{off}/R_{on}. As the "off" and "on" states of our device depend on Q, we define R_{off} and R_{on} as R_{th} at the minimum and maximum input powers considered of approximately 0.6 W and 14 W, respectively. The device switching ratio, S_R, is therefore

$$S_R = \frac{R_{off}}{R_{on}} = \frac{R_{th}(Q_1)}{R_{th}(Q_2)} \tag{4.12}$$

where Q_1 and Q_2 represent off and on-state power inputs. With this definition, the maximum switching ratio observed in the experiments is 4 for P_{NCG} = 12 kPa. As shown in Figure 4-5(b), however, the switching ratio of the NCG resistance, R_{NCG} is significantly higher than this. For each P_{NCG} considered, R_{NCG} varies by at least 10x over the heat input range considered. The NCG resistance is also much more sensitive to variations P_{NCG} than the overall device resistance, R_{th}. For Q less than 1 W, increasing P_{NCG} from 12 kPa to 99 kPa causes an approximately 7x increase in R_{NCG}, but only a 1.5x increase in R_{th}. In the physical device embodiment, much of the achievable resistance contrast in R_{NCG} therefore appears to be truncated due to the parallel and series resistances that decrease the overall switching effect.

4.4.2 Temperature clamping

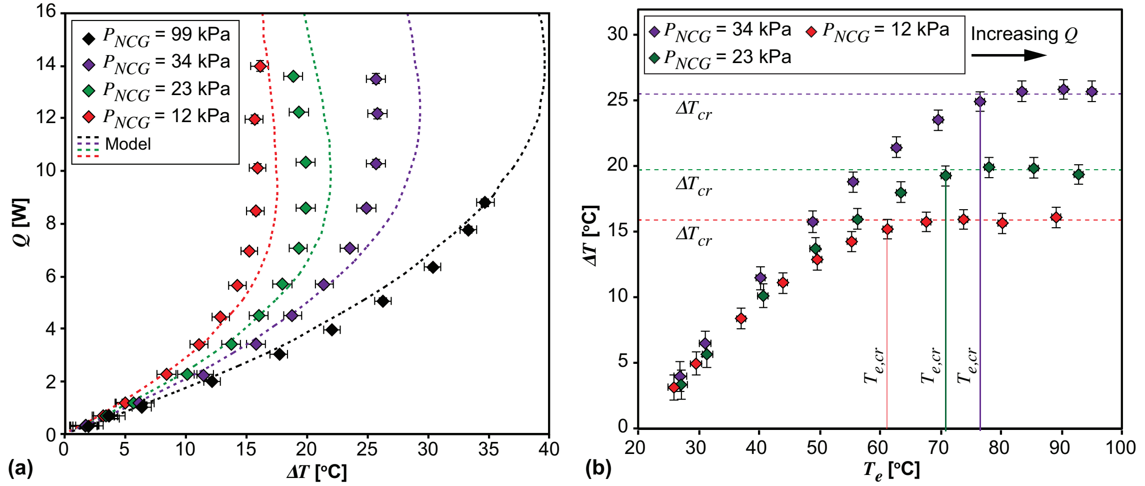

Figure 4-6. (a) Steady state experimental results for overall device resistance, R_{th}, for P_{NCG} = 12 kPa – 99 kPa. Model prediction is shown with dashed lines. (b) The temperature difference ΔT as a function of T_e for P_{NCG} = 12 – 34 kPa. ΔT becomes clamped to ΔT_{cr} at a different $T_{e,cr}$ value depending on the value of P_{NCG}.

Figure 4-6(a) demonstrates an additional attribute of the device, where the temperature difference across the two sides, ΔT becomes clamped to a relatively heat-flow independent value above a critical threshold. Varying P_{NCG} shifts the critical ΔT value where the resistance begins to decline. The values of this critical temperature difference, ΔT_{cr} for P_{NCG} = 12 kPa, 23 kPa, and 34 kPa are approximately 16°C, 20 ^{o}C, and 26 ^{o}C, respectively. No clamping is observed experimentally for P_{NCG} = 99 kPa due to the lower range of input power considered, though the model predicts that ΔT would clamp to a value of approximately 40 ^{o}C at higher heat inputs. Further details are revealed in Figure 4-6(b) where ΔT is plotted versus the hot side temperature, T_e. In the presence of NCG, ΔT becomes clamped to a relatively fixed value of ΔT_{cr} at a certain threshold temperature, $T_{e,cr}$ that varies based on P_{NCG}. We define the initiation of clamping as the point when ΔT is within 1 ^{o}C of ΔT_{cr}. With this criteria, $T_{e.cr}$ equals 61 ^{o}C, 71 ^{o}C, and 78 ^{o}C for P_{NCG} = 12 kPa, 23kPa, and 34 kPa.

The temperature clamping behavior can be explained by rearranging equation 4.6 in section 4.2.1 to describe the hot side vapor mass fraction, ω_h as a function of the heat input, where

$$\omega_h = 1 + (\omega_c - 1)exp\left(\frac{-Qz}{\rho_m D_{vg} h_{fg} A}\right) \tag{4.13}$$

Assuming for the moment that all of the heat input goes towards phase change, analyzing the behavior of Equation (4.13) reveals that as ω_h approaches 1, $d\omega_h/dQ$ decays exponentially with increasing Q. In terms of temperature, as T_e approaches the saturation temperature of water at the total cavity pressure, $T_{sat}(P_{tot})$, the NCG mass transport resistance decreases such that large increases in heat input lead to relatively smaller increases in ω_h, and subsequently T_e. This causes dT_e/dQ to decline, potentially initiating the clamping behavior for ΔT. We confirm our theory by estimating $T_{sat}(P_{tot})$ for each P_{NCG} at the onset of clamping when $T_e = T_{e,cr}$. As seen in Table 4-4, the experimentally observed $T_{e,cr}$ for each case is within 8-12% of the estimation for $T_{sat}(P_{tot})$. Note that as T_e approaches $T_{sat}(P_{tot})$, there is also the possibility of the initiation of boiling within the wick. In this case, the hot side wick resistance would potentially decrease and further reduce the total device resistance.

Table 4-4. Calculated values for the vapor temperature of water, $T_{sat}(P_{tot})$ at the onset of clamping for each of the different NCG charge pressures.

P_{NCG} **[kPa]**	**12**	**23**	**34**
$T_{e,cr}$ **[°C]**	61.25	70.7	76.6
T_c **[°C]**	46.1	51.5	51.7
$T_{sat}(P_{tot})$ **[°C]**	66.9	79.6	87.3
% difference	8.4	11.1	12.3

Figure 4-7 provides more insight into the change in hot side temperature behavior for T_e greater than $T_{e,cr}$. T_e and T_c are plotted as functions of the input power, Q for P_{NCG} = 34 kPa. The dashed lines are provided as visual guides to track the change in slope for T_e versus Q. As the experimental cold side is not a fixed reservoir, T_c shows a linear dependence on Q due to the constant heat transfer coefficient boundary condition enforced by the cold plate. At location 1 on the plot, dT_e/dQ is greater than dT_c/dQ, and

ΔT increases with increasing Q. For $T_e > T_{e,cr}$, however, dT_e/dQ begins to decline as R_{NCG} decreases significantly based on the principles of Maxwell-Stefan diffusion, and approaches a value equal to the slope of the cold side temperature. At locations 2 and 3 on the plot, dT_e/dQ is approximately equal to dT_c/dQ, initiating the clamping behavior for ΔT.

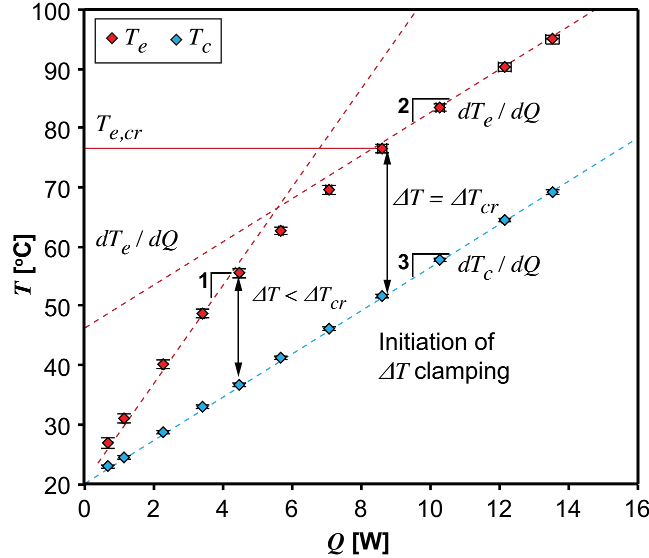

Figure 4-7. T_e and T_c versus input power, Q, for P_{NCG} = 34 kPa. At location 1, $T_e < T_{e,cr}$ and clamping has not initiated, causing ΔT to increase with increasing Q. At location 2, $T_e < T_{e,cr}$ and dT_e/dQ is approximately equal to dT_c/dQ (location 3), which results in the ΔT clamping behavior.

4.5 Switching ratio optimization

Based on the results in Figure 4-5, R_{NCG} exhibits high contrast switching behavior, but the actual contrast in overall device resistance, R_{th} is significantly dampened in comparison. The following sections will therefore explore a parametric geometric optimization to increase the switching ratio through reduction of parallel heat flow pathways and series resistance components. For consistency with the previously reported experimental results, we consider the minimum and maximum power inputs of 0.6 W and 14 W as the off/on-state powers, respectively. Note that different absolute values of

switching ratios would result if different heat flow ranges were considered, though the general optimization strategies would remain the same.

4.5.1 Effect of vapor core thickness

Ideally, R_p should be much greater than R_{NCG} to fully employ the nonlinear thermal behavior associated with vapor transport across the NCG cavity. One way to increase R_p is to increase the total cavity thickness, t_{core}. Figure 4-8(a) shows the model and experimental results for t_{core} = 500 µm - 1 mm with P_{NCG}=12±1.3 kPa. Based on the figure, doubling t_{core} increases the off-state resistance by about 170%. The total switching ratio, however, only increases slightly by around 10% from 4 to 4.4. Figure 4-8(b) shows the model results for R_{NCG} as a function of heat input for t_{core} equal to 500 µm - 1 mm with the sidewall conduction resistances, R_p, for each t_{core} overlaid on the plot. Increasing t_{core} raises R_p as well as R_{NCG} due to the longer required vapor transport distance. The relative off-state resistance ratio of R_p to R_{NCG} therefore remains constant at around 0.5 regardless of the t_{core} value, and the same percentage of heat continues to leak through the device sidewalls.

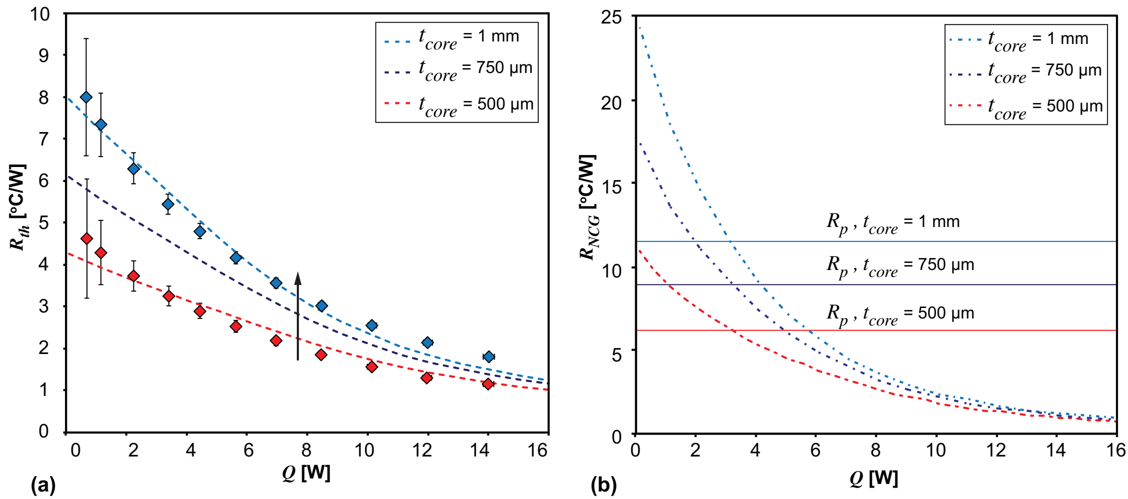

Figure 4-8. (a) Steady state experimental and model results for overall device resistance with P_{NCG} = 12 kPa and t_{core} = 500 µm - 1 mm. (b) Model results for R_{NCG} and R_p for t_{core} = 500 µm - 1 mm. R_p and R_{NCG} increase proportionally with t_{core}, which minimizes the impact on the overall switching ratio.

4.5.2 Effect of sidewall conduction area

Based on the results in Figure 4-8, modifying the insert thickness alone is not an effective method of increasing the switching ratio due to the concurrent and proportional increase in R_p and R_{NCG}. We therefore explore the additional method of increasing R_p by varying the insert width, w_{side}. We simplify the calculation by neglecting any conduction through the epoxy bead, as the current purpose is merely to provide mechanical support for the extra overhanging silicon areas used for electrical contact. The modified sidewall conduction resistance is calculated as

$$R_p = \frac{t_{core}}{k_p(4{w_{side}}^2 + 4w_{side}w_{act})} \tag{4.14}$$

where k_p is the thermal conductivity of Pyrex.

Figure 4-9 shows the predicted steady state switching ratio, S_R, for w_{side} = 200 µm - 1500 µm and P_{NCG} = 5 kPa - 99 kPa. Overall, reducing w_{side} leads to a higher switching ratio for all P_{NCG} considered. For w_{side} greater than approximately 500 µm, the lowest charge pressure of P_{NCG} = 5 kPa exhibits the highest switching ratio. A crossover regime occurs for $w_{side} < 500$ µm, however, where S_R increases slightly with increasing P_{NCG}. Overall, S_R is more sensitive to variations in w_{side} as P_{NCG} is increased. The NCG resistance R_{NCG} increases with P_{NCG}, which causes S_R to be more significantly limited by the parallel resistance, R_p, if R_p is comparable to R_{NCG} in the off-state. The highest NCG charge pressure considered of P_{NCG} = 99 kPa shows a significant increase in S_R from approximately 2 to 6.8 as w_{side} is decreased from 1500 µm to 200 µm.

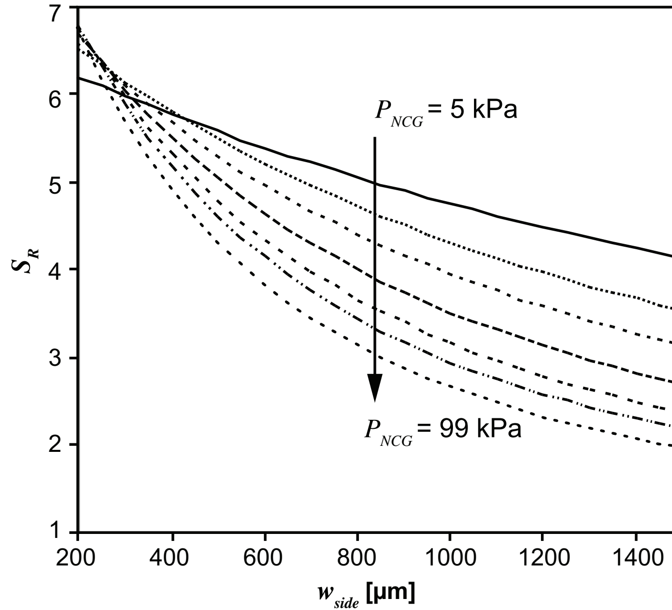

Figure 4-9. Device switching ratio, S_R, for t_{core} = 500 μm as the sidewall width, w_{side} is varied from 200 μm -1500 μm for P_{NCG} = 5 kPa – 99 kPa. S_R is more sensitive to variations in w_{side} for higher P_{NCG}.

Figure 4-10(a) shows S_R as a function of P_{NCG} for w_{side} = 200 - 1000 μm as t_{core} is increased from 500 μm to 1000 μm. As w_{side} decreases, increasing t_{core} becomes a more effective method of increasing S_R. Simultaneously tuning w_{side} and t_{core} ensures an increase in the ratio of the sidewall resistance R_p to R_{NCG}, preventing the effect demonstrated in section 4.5.1, where increasing t_{core} alone merely resulted in a fairly proportional increase in both resistances. As w_{side} decreases, S_R becomes less dependent on $P_{NCG.}$ As seen in Figure 4-9(a), S_R is fairly constant for w_{side} = 200 μm and ranges between 6.7 ± 0.2 and 10.8 ± 0.2 for t_{core} equal to 500 μm and 1000 μm, respectively, for all P_{NCG} considered. When R_p is high enough that R_{NCG} dominates, increasing P_{NCG} causes the absolute off/on-state resistances to shift fairly proportionally, and the total switching ratio becomes less sensitive to P_{NCG}. When R_p is comparable to R_{NCG}, however, R_p limits the off-state resistance and increasing P_{NCG} serves to increase the overall on-state resistance only, reducing S_R.

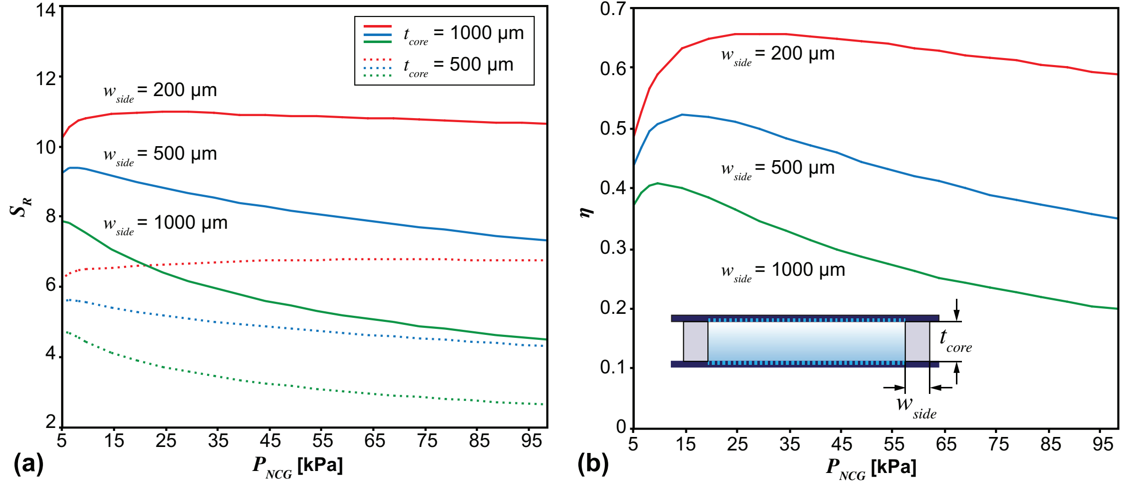

Figure 4-10. (a) Device switching ratio, S_R, for sidewall width w_{side} = 200 µm – 1000 µm, P_{NCG} = 5 kPa – 99 kPa, and t_{core} = 500 – 1000 µm. Increasing t_{core} is more effective for increasing S_R as w_{side} is reduced to prevent R_p and R_{NCG} from scaling proportionately. (b). Switching efficiency of the device, η, for t_{core} = 1000 µm and w_{side} = 200 - 1000 µm.

We further explore this phenomena by defining a switching efficiency for the device, η, equal to the overall device off/on resistance ratio divided by the NCG off/on resistance ratio, where

$$\eta = \frac{R_{th}(Q_1)/R_{th}(Q_2)}{R_{NCG}(Q_1)/R_{NCG}(Q_2)} = \frac{S_R}{S_{NCG}} \tag{4.15}$$

S_{NCG} is the switching ratio of R_{NCG} at the off/on-state heat inputs. A value of η approaching 1 therefore means the device is approaching the limits of the maximum possible switching ratio for a given P_{NCG}. Figure 4-10(b) shows the calculated switching efficiencies over the range of P_{NCG} considered for t_{core} = 1000 µm and w_{side} = 200 - 1000 µm. For the current configuration considered, the efficiency peaks at 0.66 for P_{NCG} approximately equal to 30 kPa and w_{side} = 200 µm.

4.5.3 Effect of porous wick thermal resistance

A final aspect that limits the device switching efficiency other than the parallel resistance of R_p is the series resistance across the micropillar wicks. Figure 4-11 shows the 1D resistance stack up across the device including the NCG resistance R_{NCG}, the

evaporator/condenser wick resistances, $R_{w,e}$ and $R_{w,c}$, and the silicon substrate resistance, R_{sub}, as a function of heat input for P_{NCG} = 12 kPa. In the off-state, R_{NCG} is at least an order of magnitude larger than the remaining resistances and dominates the total stack. As Q increases, however, R_{NCG} decreases steadily and becomes comparable to the evaporator wick resistance, $R_{w,e}$, which limits the on-state resistance.

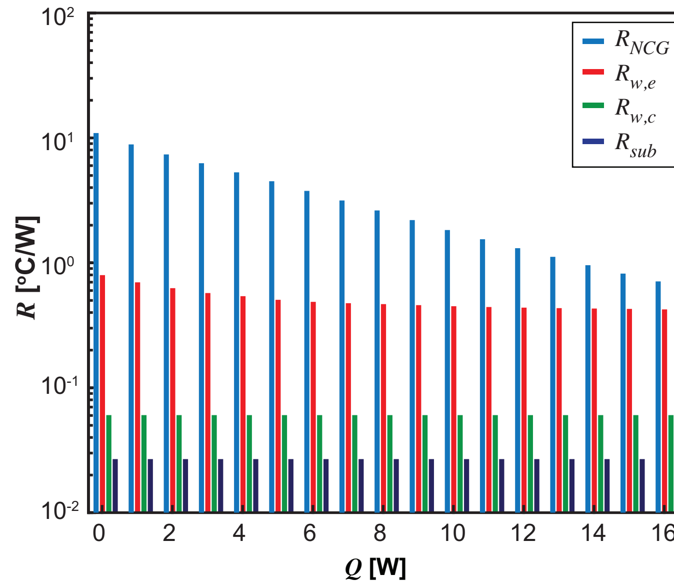

Figure 4-11. Device resistance stack up for P_{NCG} = 12 kPa. R_{NCG} dominates for low heat inputs but approaches the evaporator wick resistance, $R_{w,e}$ as Q increases, potentially limiting the on-state resistance.

To investigate the effect of varying the micropillar wick resistance, the micropillar dimensions were modified from the values listed in Table 4-1 to include cases with diameters d = 12 µm, 25 µm, 50 µm and pitches l = 25 µm, 50 µm, 100 µm. Moving to a finer wick creates more evaporative heat transfer surface area and reduces the overall wick resistance. A denser wick also creates a higher viscous flow resistance, however, potentially limiting the capillary-driven maximum heat flux of the device. A fluid flow simulation was therefore performed for each micropillar array dimension in COMSOL to confirm that the maximum heat input considered in each case could be sustained without capillary-limited dryout.

For the pressure drop calculation, the wick is modeled through an effective medium approach with an analytically derived permeability from Byon et al. [93], also given in Equations 3.13 and 3.14 from chapter 3. The simulation boundary conditions are as shown in Figure 4-12, with zero pressure assigned to each of the wick edges, and a uniform mass flux representing evaporation from the wick surface where

$$\dot{m}'' = \frac{q''}{h_{fg}} \tag{S3}$$

To account for the worst case scenario, we assume that all of the applied heat goes towards evaporation.

The pressure contour in Figure 4-12 shows the pressure drop across the wick for the case of d = 12 μm, l = 25 μm, and h = 100 μm. The maximum pressure drop is approximately 165 Pa, which is less than 13% of the estimated capillary pressure from the force balance model approach (~1350 Pa). Simulations for the other micropillar dimensions also resulted in viscous pressure drops that were significantly smaller than the capillary pressure threshold, meaning the device could reasonably sustain 14 W with the modified wick dimensions without risk of dryout.

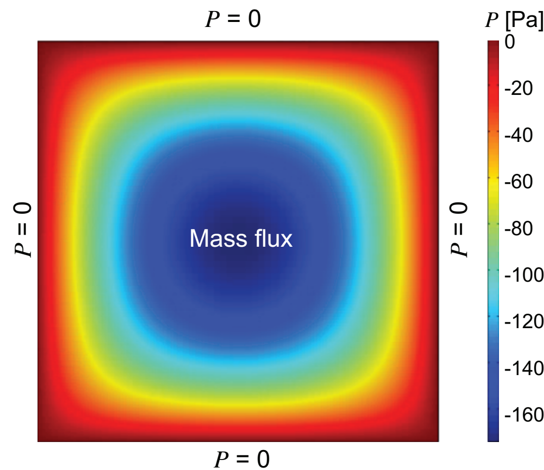

Figure 4-12. Pressure contour and boundary conditions for the viscous pressure drop simulation in COMSOL, where the wick is treated as an effective porous medium with an analytically calculated permeability.

Figure 4-13(a) shows the variation in S_R as a function of P_{NCG} for the different micropillar dimensions considered with w_{side} = 200 µm and t_{core} = 1000 µm. Reducing the overall wick resistance appears to have the most significant impact on S_R in the low P_{NCG} range. A maximum switching ratio of approximately 14.5 is achieved for the highest density wick with P_{NCG} = 5 kPa. For higher P_{NCG}, R_{NCG} remains substantially higher than $R_{w,e}$ in the on-state and continues to dominate the resistance stack, minimizing the impact of reducing $R_{w,e}$. This is also evidenced in Figure 4-13(b), which plots the switching efficiency η for each of the different micropillar array dimensions considered. As the overall wick resistance is decreased, the maximum efficiency point shifts left towards lower values of P_{NCG}, with a maximum η reached of approximately 0.76 for the finest micropillar wick dimensions of d = 12 µm and l = 25 µm. Lower P_{NCG} levels therefore appear sufficient to create a high switching ratio thermal regulator, but higher P_{NCG} levels can be used to tune the absolute off/on-state resistances.

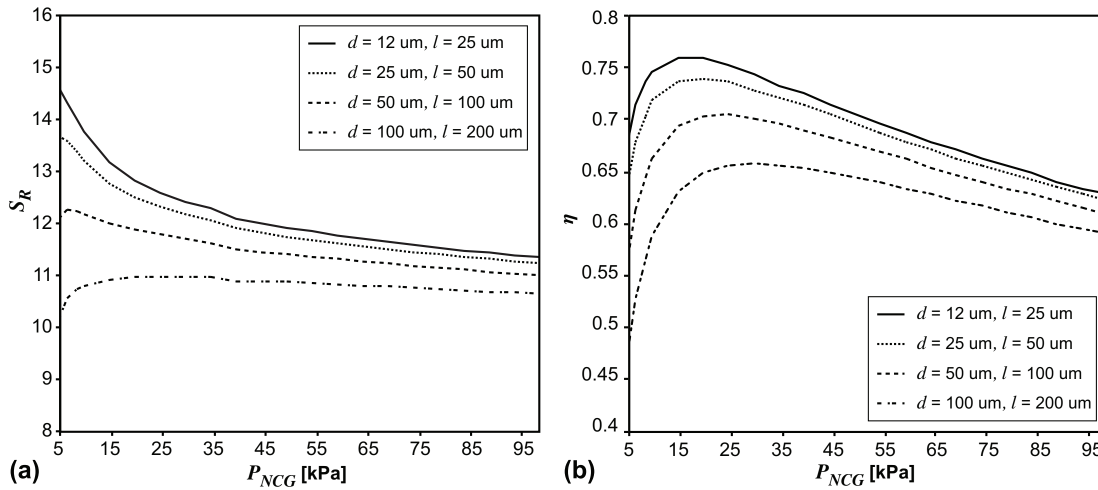

Figure 4-13. (a) Switching ratio S_R as a function of P_{NCG} for w_{side} = 200 µm and t_{core} = 1000 µm as micropillar wick dimensions are varied from d = 12 – 100 µm and l = 25 – 200 µm. Reducing $R_{w,e}$ with a higher density pillar array has the most significant impact on increasing S_R in the low P_{NCG} range. (b) Switching efficiency, η, with varied micropillar array dimensions to reduce $R_{w,e}$. A maximum efficiency of approximately 0.76 is reached for the finest pillar dimensions considered of d = 12 µm and l = 25 µm.

4.6 Conclusions

In conclusion, we have demonstrated a thermal regulator that leverages vapor diffusion through a NCG barrier to exhibit a switchable resistance over a range of power inputs. The device is passive, with a thermal resistance that naturally decreases as the input power increases, making the device concept potentially suitable for use as a thermal shunt or surge protector against sudden power spikes. Experimental results for the current device configuration demonstrated a maximum switching ratio of 4 over the heat flow range of 0.6 W to 14 W. Through a parametric optimization of the device geometry, however, we demonstrated a pathway to increase the switching ratio over the same heat input range to more than 14. Overall, the device geometry should be optimized such that the vapor/NCG resistance dominates the device resistance stack in order to achieve the maximum resistance switching contrast. Larger switching ratios are also possible depending on the off/on-state powers under consideration.

The device also demonstrates the ability to clamp the temperature difference across the hot and cold sides to a heat flow independent, fixed value of ΔT_{cr}. Both the resistance switching behavior and value of ΔT_{cr} are adjustable with the amount of NCG charge, an advantage over many existing regulators that are limited to fixed operating temperature ranges. The tunability of the device presented here provides a valuable addition to the current arsenal of existing thermal circuitry components, and increases the opportunity for electro-thermal co-design in future systems.

Chapter 5

Passive Thermal Regulation with Binary Vapor Diffusion: Transient Behavior

This chapter focuses on the importance of characterizing the transient behavior of thermal switches and regulators, and presents experimental and model results for the transient switching performance of the binary diffusion based regulator introduced in Chapter 4. Large portions of this chapter are taken from Liu et al., "Steady-state Parametric Optimization and Transient Characterization of Heat Flow Regulation with Binary Diffusion," *IEEE TCPMT*, 2020 [143].

5.1 Relevance of transient thermal response

The transient thermal behavior of various switches and regulators is an important aspect often neglected in studies that primarily treat the steady-state switching ratio as the predominant figure of merit. While steady-state studies provide a baseline for the relative comparison of different regulators, it becomes impractical to assess their impact in system-level implementations without a thorough discussion of transient behavior. Table 5-1 shows a summary of several different switching mechanisms in terms of not only their switching ratios, but also their transient thermal response times. For a more comprehensive view of how these mechanisms could be implemented in practice, both attributes must be taken into account. For instance, Guo et al. utilized differential thermal expansion with a flexible rod to achieve a high switching ratio variable resistance between a heated metal cylinder and cold disk [45]. Thermal expansion is a weak effect, however, and relatively large feature sizes are required to achieve sufficient expansion to actuate this type of switch. The large thermal masses involved in these systems thus tend to create a slow thermal response time on the order of minutes instead of seconds [45]. On the contrary, solid-state phase transitions in vanadium oxide occur extremely rapidly

on the order of nanoseconds [153], but with relatively low switching ratios of approximately 2 [49].

Table 5-1. Comparison of various thermal regulation mechanisms and their associated response times.

Regulation mechanism	Switching ratio	Response time	Actuation method
Differential thermal expansion [45]	390	~ 12 min	Passive
Liquid metal slug [44]	70	~ 1 s	Electric field
Shape memory alloy induced flexing(SMA) [37]	2070	~ 10 s	Passive
Solid-state phase transition in VO_2 [49,153]	2	<< 1 s	Passive

Depending on the application, a system may benefit from a regulator with either a slower or faster thermal response time. For instance, a fast response time thermal switch would be ideal for generating transient heat loads of various waveforms, such as for a pulsed energy harvester. A thermal regulator to limit sudden temperature spikes, however, may benefit from additional thermal capacitance to smooth out the temperature rise. We therefore analyze the primary components that affect the thermal response time for the binary diffusion-based regulator, and evaluate the switching behavior in response to a pulsed heating input.

5.2 Transient device model

For the transient thermal analysis, we assume that the timescale associated with the vapor diffusion is much smaller than the thermal response time of the device solid portions [154,155]. We neglect the effect of varying liquid velocities in the porous wick and assume that the steady-state conduction model remains sufficient to describe the heat transfer across the micropillar array [74,156]. Similarly, we neglect the time to initiate

capillary flow within the micropillar wick, which is typically on the order of ms [157]. With this treatment, the majority of the transient device behavior is governed by sensible heat storage. The resistance of the NCG/vapor core is comparable to the condenser side external heat transfer resistance (Bi ~ 1), meaning the transient device behavior cannot be accurately modeled with a lumped analysis as done for heat pipes [158]. Therefore, we use a three-dimensional solid conduction model in COMSOL to capture the device transient behavior. The NCG/vapor core mixture is modeled as a block with an NCG pressure and temperature-dependent effective thermal conductivity derived from the steady-state model results. Due to the small mass of NCG/vapor contained in the core, the thermal capacitance of the mixture is expected to be negligible compared to the wick and solid portions of the device (on the order of 1e-5 J/K).

Figure 5-1 shows the steady state model results for the NCG/vapor mixture thermal resistance R_{NCG} as a function of the evaporator side temperature, T_e for P_{NCG} = 12 kPa. As seem in the figure, R_{NCG} can be expressed as purely a function of T_e relatively independent of variation in the condenser side boundary condition. While the vapor mass transport equation depends on the evaporator side vapor mass fraction as well as the condenser side vapor mass fraction, the condenser side vapor mass fraction is fixed by the condenser side external boundary condition. Varying the condenser side heat transfer coefficient therefore simply shifts the heat flux dependence of R_{NCG}, but not the temperature dependence on T_e. The curves for R_{NCG} as a function of T_e therefore collapse onto each other for the three different condenser side heat transfer coefficients shown of h_{cp} = 2400, 5000, and 10,000 $Wm^{-2}K^{-1}$.

A second order polynomial fit for $R_{NCG}(T_e)$ is generated with an R^2 value of 0.99 for h_{cp} = 2400 $Wm^{-2}K^{-1}$, where

$$R_{NCG} = 0.00146{T_e}^2 - 0.306T_e + 16.72 \tag{5.1}$$

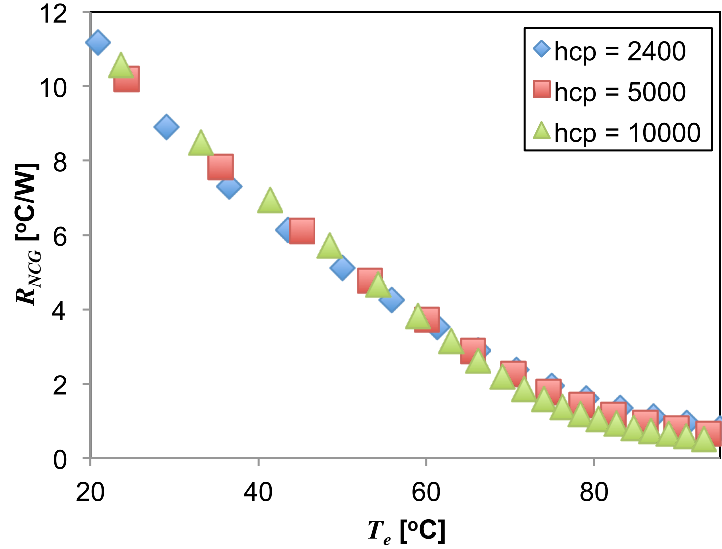

Figure 5-1. Steady state model results for R_{NCG} as a function of T_e for P_{NCG} = 12 kPa. R_{NCG} is relatively independent of the condenser side condition and can be expressed primarily as a function of T_e. A second order polynomial fit is generated for use as an input to the transient COMSOL simulation.

The effective thermal conductivity input to the transient COMSOL simulation is thus

$$k_{NCG} = \frac{t_{core}}{R_{NCG} {w_{act}}^2} \tag{5.2}$$

A similar fit can be made from the steady state model results for the evaporator wick resistance, $k_{w,e}$ as a function of T_e, where

$$k_{w,e} = -0.000166{T_e}^2 + 0.0341T_e + 0.607 \tag{5.3}$$

The condenser side wick resistance has minimal temperature dependence due to the relatively low liquid-vapor interfacial resistance compared to the evaporator side wick and is assigned a constant value of 16 $Wm^{-1}K^{-1}$ based on Equation 4.9 from section 4.2.2. The equivalent densities and heat capacities of the evaporator/condenser wicks are calculated based on the wick porosity, ϕ, as

$$\rho_w = \emptyset\rho_{liq} + (1 - \emptyset)\rho_{sub} \tag{5.4}$$

$$c_{p,w} = \emptyset c_{p,liq} + (1 - \emptyset) c_{p,sub} \tag{4.5}$$

Figure 5-2 shows the simulation boundary conditions for the transient solid conduction model in COMSOL, where a quarter geometry view of the device is shown. Heat is supplied to the evaporator side heater based on the experimentally measured values for Q_{in}, and a constant heat transfer coefficient boundary condition is assigned to the active 1 x 1 cm^2 condenser area of the device to represent cooling from the copper cold plate. An approximately 5 mm thick layer of silicone insulation is used in the experiments to minimize heat loss from the evaporator side heater to the environment and is included in the simulations for consistency, though the capacitance of the silicone has a minimal contribution to the overall device response time. A natural convection coefficient of 10 $Wm^{-2}K^{-1}$ is assigned to all remaining exposed surfaces. Table 5-2 summarizes the material properties used for the various device components in the transient conduction simulation. We note that if significant redistribution of liquid occurs within the device such as liquid starvation within the wick, it may no longer be accurate to model the wicks and NCG/vapor mixture as blocks with equivalent thermal conductivities and heat capacities. The model is therefore only appropriate for heat input ranges within the capillary limits of the device operation.

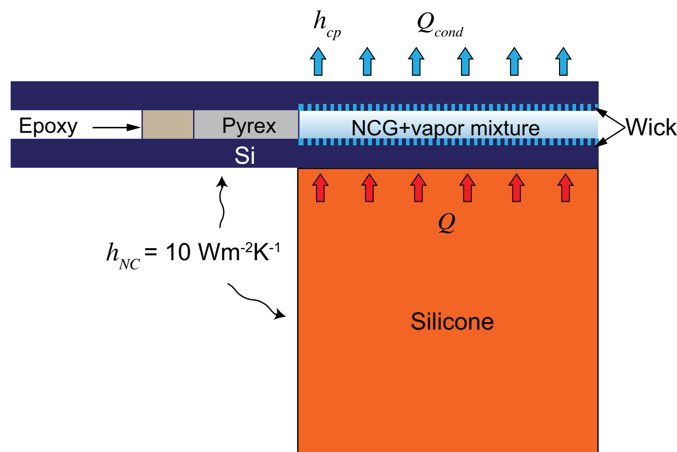

Figure 5-2. Boundary conditions and geometry used in transient solid conduction simulation in COMSOL.

Table 5-2. Material properties used for various device components in transient conduction simulation.

Material	Thermal conductivity, k [$Wm^{-1}K^{-1}$]	Density, ρ [kg/m^3]	Porosity, ϕ	Specific heat capacity, c_p [$Jkg^{-1}K^{-1}$]
Silicon	149	2320	N/A	712
Pyrex	1	2230	N/A	753
Epoxy	0.3	1100	N/A	1000
Water	0.6	998	N/A	4180
Silicone insulation	0.15	1500	N/A	1200
NCG/vapor core	$k_{NCG}(T_e)$ Eqn. S5	Negligible	N/A	Negligible
Evaporator wick	$k_{w,e}(T_e)$ Eqn. S6	$\rho_w(\phi.\ \rho_{Si},\ \rho_{water})$, Eqn. 13	0.8	$c_{p,w}(\phi,\ c_{p,Si},\ c_{p,water})$ Eqn. 14
Condenser wick	16	$\rho_w(\phi.\ \rho_{Si},\ \rho_{water})$, Eqn. 13	0.8	$c_{p,w}(\phi,\ c_{p,Si},\ c_{p,water})$ Eqn. 14

5.3 Transient experimental results

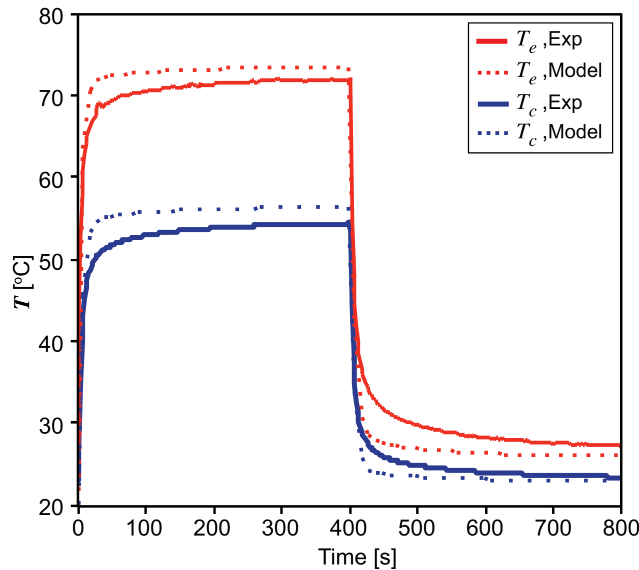

Figure 5-3. Transient model and experimental temperature profiles for the average evaporator/condenser side temperatures, T_e and T_c in response to step high and low heat inputs of approximately 9 W and 0.7 W, respectively.

Figure 5-3 shows the transient model and experimental device temperature profiles as the power to the heater is first stepped up to approximately 9 W, then stepped down to 0.7 W for P_{NCG} = 12 kPa and t_{core} = 500 μm. Overall the model shows fair agreement with the experimental temperature profiles, confirming the assumption that the majority of the transient temperature response is governed by sensible heat storage. We assess the device thermal response time in terms of a time constant, τ_h, which represents the time required for T_e to reach 63% of the total steady state temperature rise. The model and experimental values for τ_h agree well with values of approximately 4.4 seconds and 4.9 seconds, respectively. In addition to the internal device resistances, τ_h also depends strongly on the external condenser side heat transfer coefficient, h_{cp}. As h_{cp} is varied from 500 – 10,000 $Wm^{-2}K^{-1}$, τ_h ranges from approximately 15 – 1 seconds. The model results for τ_h as a function of h_{cp} are listed in Table 5-3.

Table 5-3. Thermal time constant, τ_h, as a function of external condenser side heat transfer coefficient, h_{cp}. h_{cp} is approximately equal to 2400 $Wm^{-2}K^{-1}$ in the experiments.

h_{cp} [$Wm^{-2}K^{-1}$]	τ_h [s]
500	15.3
2400	4.4
5000	1.8
10,000	1

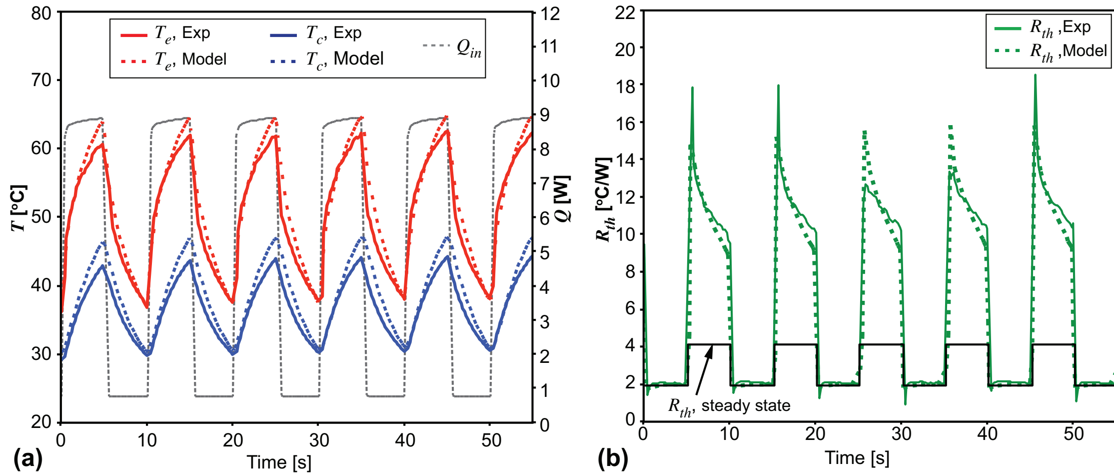

Figure 5-4. (a) Model and experimental temperature profiles when the applied heat input, Q_{in} is pulsed in 5 second durations from 0.7 W to 9 W. (b) Transient device resistance in response to the pulsed heating input. The device takes longer to reach the steady-state resistance value in the cool-down phase, leading to transient off-state resistances much higher than steady-state values.

Figure 5-4(a) shows the transient temperature profiles in response to a pulsed heating input where Q_{in} is modulated between on/off-state powers of 9 W and 0.7 W, respectively, over a period of 10 seconds. As shown in the plot, the applied heat input is not a true square wave due to the temperature-dependent resistance of the serpentine heater/RTD. To account for this, the experimentally measured heating profile is directly used as a simulation input. Figure 5-4(b) shows the effective device resistance in response to the pulsed heat input. As seen in Figure 5-4 (b), the device responds rapidly when transitioning from the off to on-state and reaches the steady-state on-state resistance with almost no delay. When the heat load is reduced, however, the difference in the response times of the condenser and evaporator sides leads to a large spike in the apparent device off-state resistance up to as high as 18 ^{o}C/W. This is much higher than the predicted steady-state resistance value of approximately 4 ^{o}C/W. The off-state resistance slowly declines over 5 seconds to around 8 ^{o}C/W, but still remains approximately 2x greater than the steady-state value. This leads to an interesting phenomenon, where the transient switching ratio appears significantly higher than the

steady-state ratio. The difference between the off-on and on-off transitions can be explained by considering the heat transport pathways in the two different scenarios.

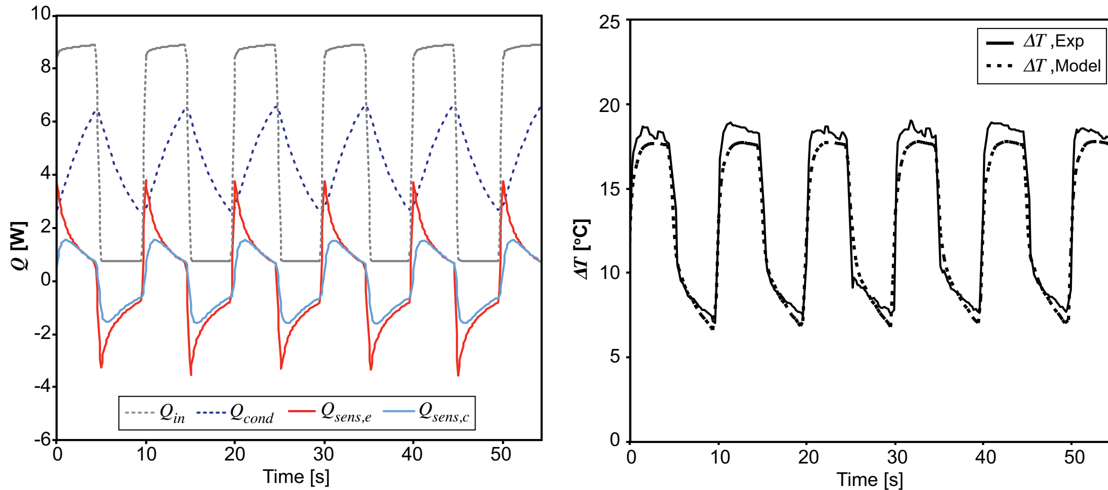

Figure 5-5. (a) Model results for the device transient heat flow pathways in terms of the total heat supplied to the heater, external heat removal from the condenser side, and the rate of change in sensible heat storage in the evaporator/condenser substrates. (b) Transient model and experimental profiles for the temperature difference ΔT in response to a pulsed heat input. The clamping behavior of the device fixes ΔT in the on-state and causes the device resistance to rapidly approach the steady state value.

Figure 5-5(a) shows the model results for the transient heat flow pathways within the device in terms of the heat applied to the heater, Q_{in}, the amount of heat removed from the condenser side, Q_{cond},, and the rate of change in sensible heat storage in the evaporator/condenser side substrates, $Q_{sens,e}$ and $Q_{sens,c}$, respectively. As heat is supplied to the evaporator side heater, a significant portion of the heat is initially stored as sensible heat in the evaporator side substrate. The heat eventually reaches the condenser side, increasing the amount of heat rejection through the external cold plate. $Q_{sens,e}$ and $Q_{sens,c}$ approach the same value approximately 2 seconds after the initial heating pulse, and decline steadily as Q_{cond} continues to rise.

In the cool down phase, Q_{in} is suddenly decreased, and an excess amount of heat is removed from the condenser side. Some amount of variation in the response times for

on-off and off-on transitions is expected, as the higher steady-state device resistance in the off-state naturally increases the thermal time constant. The effect is greatly amplified, however, by the ΔT clamping behavior of the device as shown in Figure 5-5 (b). In the on-state, enough heat is supplied that the device crosses the ΔT clamping threshold (as previously shown in Figure 4-6), and the temperature difference across the device becomes relatively independent of heat flow. This causes ΔT to quickly approach a fixed value of approximately 18 ^{o}C with relatively minimal impact from sensible heat storage within the device. In the off-state, the device falls outside of the ΔT clamping regime as the heat input is reduced, and the ΔT heat flow dependence returns. The effect of sensible heat storage therefore becomes more apparent, and ΔT decreases with time to approach the steady-state value. The high apparent transient off-state resistance is therefore not a true change in device resistance, but an effect of sensible heat storage that causes ΔT to be higher than the steady-state value. The combination of this with the ability of the device to clamp to a fixed ΔT above a certain threshold leads to the asymmetric transient behavior, where the off-on resistance response time appears much shorter than the on-off resistance response time. The transient switching ratio of the device therefore also appears higher than the steady-state ratio due to the combined effect of sensible heat storage in the off-state and temperature clamping in the on-state.

5.4 Conclusions

Transient experiments and modeling of the regulator revealed that the majority of the device thermal capacitance is comprised of sensible heat storage in the solid device volume. The device thermal time constant ranges from approximately 1-15 seconds depending on the external heat transfer coefficient. For transient events occurring with significantly shorter time scales, the device will likely not be able to respond fast enough for resistance switching to occur. For transient events occurring on the order of a few seconds, the temperature clamping behavior of the device creates a highly attractive attribute where the on-state resistance of the device is reached relatively quickly, and the apparent off-state resistance is magnified over the steady-state value. This asymmetric transient response promotes the device as a good candidate for use as a thermal regulator to mitigate sudden temperature swings. The temperature clamping behavior can also

potentially create a thermal buffering effect to protect sensitive components from fluctuations in ambient environmental conditions [34]. However, it remains difficult to predict the effect of implementing the device in a system-level regulation scenario, as the overall temperature response will depend on the system-level thermal resistances and capacitances. With this work, the aim is to produce an accurate picture of the standalone regulator behavior that can feed into future system-level experiments and/or models.

Chapter 6

Conclusions and Future Work

In this chapter, we summarize some of the primary findings and contributions of this dissertation, and propose directions for future work in the field.

6.1 Integrated heat spreading mechanisms for electronics thermal management

In chapter 2, we presented a detailed discussion on the operating principles and performance prospects of silicon vapor chambers. Since silicon is CTE compatible with most semiconductor substrates, the adoption of silicon vapor technology enables a variety of novel, integrated packaging configurations that could eliminate many of the thermal bottlenecks associated with poor thermal interfaces in existing packages. Significant work still remains, however, in developing robust manufacturing processes for silicon vapor chambers before they can be utilized at a commercial scale. At the same time, the vast array of silicon micromachining processes available also creates opportunities to implement unique porous wick structures to optimize the heat and mass transport within the vapor chambers.

As discussed in chapter 3, however, cost considerations may limit the use of silicon vapor chambers much larger than a typical die size. One approach to creating more cost effective silicon vapor chambers could be to scale down the size of the vapor chamber. We demonstrated in chapter 3 that a miniature, 1 x 1 cm^2 silicon vapor chamber could be utilized for die-matched heat spreading with significant improvement in temperature uniformity (> 45%) over solid silicon. An alternative approach and practical area of future research could involve silicon vapor chambers with multiple integrated die for multi-chip heat spreading. Careful consideration of the working fluid and compatibility of various devices would be necessary to ensure that no electrical interference occurred between different die.

While silicon is a promising material for creating integrated vapor chambers, a range of other CTE matched materials also exist that could prove more cost effective in the long run. Kovar, for example, has a CTE close to silicon and can be processed with inexpensive stamping methods. Benson et al. estimated that a heat pipe fabricated out of Kovar could be made for 1/10th the cost of a silicon heat pipe [82]. The thermal conductivity of Kovar, however, is almost two orders of magnitude lower that silicon, which may limit the use of Kovar based vapor chambers to low heat flux applications only. Other low CTE vapor chamber envelope materials that could potentially compete with silicon include copper molybdenum [56], copper tungsten [159], and ceramics such as aluminum nitride [160].

Finally, an exciting area of future research remains in other opportunities for integrated heat spreading in non-traditional components of electronics packages. Cho et al. recently fabricated a vapor chamber embedded into a printed circuit board, and demonstrated a 20% improvement over a standard copper-plated PCB [128]. We also proposed in chapter 2 the possibility of an interposer with an integrated vapor chamber. While the initial proposal was for a silicon interposer, the same concept could theoretically be applied to glass and ceramic interposers as well, each with their unique set of fabrication challenges. Additionally, as integrated circuits move towards 3D stacked chip architectures, a key challenge will arise in intra-layer thermal management. Integrated heat spreaders or heat pipes will be crucial to aid heat flow isolation and redistribution in stacked configurations.

6.2 Capillary-fed evaporation/boiling in biporous and hierarchical structures

The thermofluidic performance of vapor chambers and heat pipes is critically dependent on the porous wicking structure that drives the heat and mass transport within the device. To obtain the simultaneous goals of reducing the wick thermal resistance and increasing the capillary dryout limit, we made the case in chapter 2 for biporous and/or hierarchical porous structures to simultaneously optimize for both parameters. In addition to providing examples from literature where biporous/hierarchical structures have

demonstrated improved capillary performance over homogenous structures, we also investigated a hierarchical silicon micropillar array structure in chapter 3 fabricated through ultra-violet laser ablation. The conformal microscale roughness generated from the laser ablation was found to potentially enhance the area for thin-film evaporation by a factor of 3.

There still remains great opportunity, however, to further the understanding and intelligent design of porous structures for capillary-fed heat transfer applications. As we presented in chapter 2, incorrect combinations of different length scales can also lead to performance degradation in biporous structures compared to their homogenous counterparts. Much room remains, therefore, for future work to explore deeper fundamental knowledge on how different pore geometries, surface properties, and operating conditions affect various performance attributes in capillary-fed evaporation and boiling processes.

The ever-expanding arsenal of materials fabrication capabilities also introduces continuous possibilities for new and unique porous structures that can potentially be utilized in capillary-fed heat transfer applications. A key component to generating a better understanding of the effects of various porous wick properties on thermofluidic performance is to study structures with well-defined, repeatable geometry. Figure 6-1 contains two examples of biporous structures fabricated in the Stanford Nanoheat group. Figure 6-1(a) shows a top view SEM image of a copper nanowire array interspersed with microscale cavities. A porous polycarbonate membrane is rolled on top of an Au seed layer to form the template for copper nanowire growth [161], and the seed layer is selectively patterned to control the areas for nanowire formation during electroplating. Previous studies on boiling from copper nanowires have attributed bubble nucleation at low superheats to the presence of microscale cavities that form due to fabrication defects in densely packed nanowire arrays [162]. The cavity size formation is frequently irregular and difficult to characterize with a single length-scale, however. Intentionally creating microscale cavities with a repeatable technique such as a patterned seed layer therefore

creates an opportunity for a controllable study on the effect of cavity size on bubble nucleation and capillary wick performance.

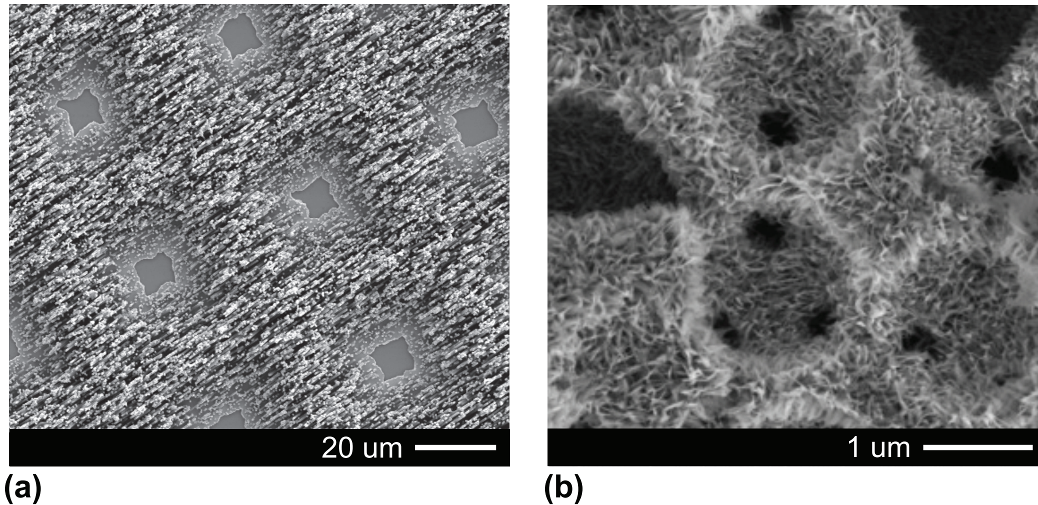

Figure 6-1. (a) Biporous copper nanowire arrays fabricated through electroplating with a patterned seed layer. The microscale cavities can potentially act as bubble nucleation sites for enhanced boiling. (b) Copper inverse opals with a hierarchical cupric oxide nanostructured coating after a chemical oxidation process. The cupric oxide coating alters the wettability of the structure and makes it superhydrophilic.

Another example of an exciting material candidate for capillary-fed evaporation/boiling experiments is copper inverse opals. In addition to the high capillary-fed boiling performance observed in literature [53] (briefly discussed in chapter 2), the highly repeatable and tunable nature of copper inverse opals makes it an ideal structure for fundamental studies on microstructural effects in capillary-fed scenarios. Layered inverse opal structures with graded pore sizes in the out-of-plane direction could lead to promising configurations where the capillary pressure and wick permeability could presumably be tuned independently of one another. As shown in Figure 6-1(b), a hierarchical nanostructured coating can also be formed on top of an existing inverse opal porous matrix. The initial copper inverse opal matrix is formed from a templated electrodeposition process, where copper is electroplated through a self-assembled polystyrene sphere template [53,109]. After the spheres are dissolved with an organic solvent, the entire porous structure is submerged in an alkaline solution formula (16 g

$NaClO_2$, 1 g NaOH, 100 mL water) [163] and chemically oxidized to form a cupric oxide nanostructure. The nanostructure renders the wick superhydrophillic and creates a method of varying the contact angle without significantly impacting the remaining wick parameters.

In summary, an abundance of opportunity remains in exploring the effects of various porous wick parameters on liquid-vapor phase change phenomena for capillary-fed heat transfer applications. Combinations of porous structures with various length-scales can be achieved through a wide range of different fabrication approaches, and detailed studies on these biporous and/or hierarchial wicks with controllable, tunable microstructures can elucidate the dependence of various thermofluidic transport processes on overall wick geometry. This enables intelligent design of future wick structures that have the potential to significantly elevate the performance of two-phase heat transfer devices.

6.3 Nonlinear thermal devices for heat flow regulation

In chapters 4 and 5, we presented a thorough characterization of a passive, tunable thermal regulator that achieves a switchable thermal resistance through the process of binary vapor diffusion through a NCG cavity. We characterized the device in terms of standard figures of merit such as the steady-state resistance switching ratio and transient thermal response time. The key distinction of our device over others developed in literature lies in the tunability, as the resistance switching behavior can be adjusted through variation of the NCG charging pressure.

A key future research direction in the area of nonlinear thermal devices for heat flow regulation is identifying how these devices would perform in actual system-level thermal regulation scenarios. Figure 6-2 shows an example of how the thermal regulator presented in chapters 4 and 5 could be utilized in a real-world scenario. In normal operation of the active device, the thermal regulator resistance would ideally be high in the off-state, and the majority of the heat removal would take place through the heat sink. If a sudden power surge were to occur for the device, however, due to a change in operational load or similar, the thermal regulator resistance would drop passively in

response to the increase in input power. Heat flow could then be diverted through the PCB to provide a parallel pathway to minimize the rise in the active device junction temperature. Whether or not the thermal regulator is actually effective in this hypothetical scenario, however, becomes a question of system-level impedance matching. If the thermal regulator resistance is significantly higher than the heat sink resistance in both the off and on-states, the existence of a parallel pathway will be relatively ineffective. Additionally, the transient response times of all the different system-level components will contribute to the actual temperature response at the device active layer, and whether or not the regulator resistance transition occurs over an appropriate period of time to affect the device temperature response.

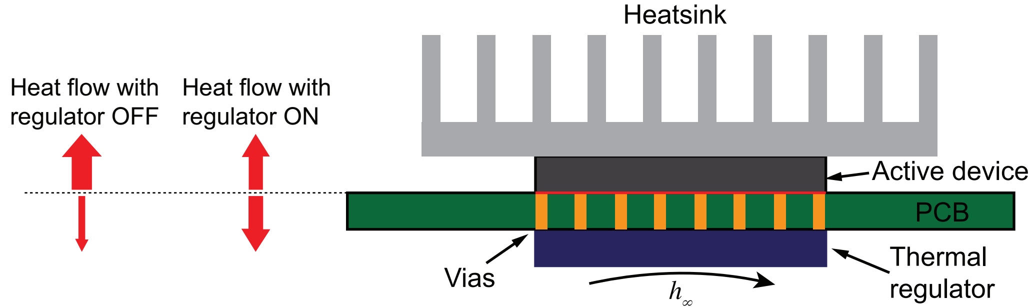

Figure 6-2. Example implementation of the thermal regulator presented in chapters 4 and 5. In ordinary operation, the thermal regulator is in the off-state, and the majority of heat removal takes place through the top of the active device from the heat sink. If a sudden power surge occurs, the thermal regulator enters the on-state, the thermal resistance decreases, and heat flow is diverted through the PCB as well, limiting the maximum junction temperature rise for the active device.

Overall, research in the area of nonlinear thermal devices for thermal regulation and switching applications has been largely devoted to the characterization of such devices in standalone experiments, where the resistance switching and transient response can be easily characterized independently of external factors. These works have been valuable in providing thermal designers with a rich arsenal of thermal devices to choose from for a variety of different applications. The next step in this field, therefore, must be to assess how these devices will behave in actual systems. Simple thermal resistance and

capacitance models could be utilized where appropriate in system-level thermal circuit representations as a first step, and potentially integrated with electrical circuit design models in software such as LTSpice. Electro-thermal co-design efforts stand to benefit greatly from these types of modeling approaches as the capability of thermal devices grows to encompass more complex heat routing behaviors, paving the way for unique thermal and electrical system architectures.

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