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The Development of Novel Interconnection Technologies for 3D Packaging of Wire Bondless Silicon Carbide Power Modules

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The Development of Novel Interconnection Technologies for 3D Packaging of Wire Bondless Silicon Carbide Power Modules

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by

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Abstract

This dissertation advances the cause for the 3D packaging and integration of silicon carbide power modules. 3D wire bondless approaches adopted for enhancing the performance of silicon power modules were surveyed, and their merits were assessed to serve as a vision for the future of SiC power packaging. Current efforts pursuing 3D wire bondless SiC power modules were investigated, and the concept for a novel SiC power module was discussed. This highly-integrated SiC power module was assessed for feasibility, with a focus on achieving ultralow parasitic inductances in the critical switching loops. This will enable higher switching frequencies, leading to a reduction in the size of the passive devices in the system and resulting in systems with lower weight and volume. The proposed concept yielded an order-of-magnitude reduction in system parasitics, alongside the possibility of a compact system integration. The technological barriers to realizing these concepts were identified, and solutions for novel interconnection schemes were proposed and evaluated. A novel sintered silver preform was developed to facilitate flip-chip interconnections for a bare-die power device while operating in a high ambient temperature. The preform was demonstrated to have 3.75× more bonding strength than a conventional sintered silver bond and passed rigorous thermal shock tests. A chip-scale and flip-chip capable power device was also developed. The novel package combined the ease of assembly of a discrete device with a performance exceeding a wire bonded module. It occupied a 14× smaller footprint than a discrete device, and offered power loop inductances which were less than a third of a conventional wire bonded module. A detailed manufacturing process flow and qualification is included in this dissertation. These novel devices were implemented in various electrical systems—a discrete Schottky barrier diode package, a half-bridge module with external gate drive, and finally a half-bridge with integrated gate driver in-module. The results of these investigations have been

reported and their benefits assessed. The wire bondless modules showed < 5% overshoot under all test conditions. No observable detrimental effects due to *dv/dt* were observed for any of the modules even under aggressive voltage slew rates of 20-25 V/ns.

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I would like to thank my colleagues. Through these last four years they helped make my life a lot easier and made me appreciate the value in having s close-knit community at work. I need to mention a few names in particular. It was a great experience working with Chris Farnell and Yuzhi Zhang on our "Arkansas Powerbox" inverter. Working alongside them taught me most of the nuances of power electronics system design that I know. Nan Zhu, Andrea Wallace, and Audrey

Dearien—thanks a ton for helping me and doing your part toward the end. I would never have made it in time without you.

Finally, and most importantly, I would like to thank this country for giving me the opportunity to pursue my dreams. I have met exceptional human beings during my stay here, whose dedication and sense-of-purpose inspired me. I am extremely grateful to the United States of America and the University of Arkansas for supporting me during this crucial period in my career.

Dedication

This dissertation is dedicated to my parents—Mr. Ashim Seal and Mrs. Jyotsna Seal—and to the unmitigated, unconditional, and sometimes overwhelming love and support they have provided through thick and thin.

Table of Contents

CHAPTER 1: Introduction

With the low switching losses that wide bandgap (WBG) devices incur, there arises a possibility of increasing the switching frequency into the MHz-range. High-frequency switching will help reduce the size of the passive devices in the system. After all, the potential for high power density is one of the main benefits that wide bandgap devices bring to the table. However, load currents transitioning at ultrahigh slew rates will lead to inductive voltage overshoots (and ringing) resulting in a catastrophic failure. Keeping the voltage and current levels constant, the only variable we can control to address this concern is the parasitic inductance of the switching loops.

At present, wire bonding is the preferred interconnect technology for SiC power modules. Wire bonds have an inherent parasitic inductance associated with them. Using a large number of wire bonds in parallel is one of the standard solutions that module manufacturers employ. With shrinking die sizes, this is not a practical solution to the problem. It has also been demonstrated that there is a point of diminishing returns with this approach [1]. This dissertation investigates methods to employ an alternative interconnection scheme for SiC devices. The proposed methods allow for a highly-integrated packaging approach—one in which critical loop inductances can be reduced by an order of magnitude compared to wire bonding. This is an important first step in realizing a high power density.

Section 1.1: Motivation and problem statement

SiC is a much superior semiconductor material as compared with silicon. However, the packaging concepts for SiC are exactly the same as silicon. The integration technologies employed for silicon devices are tailored to the physics of silicon as a semiconductor material. High temperature materials are not considered for silicon modules because silicon itself cannot operate

satisfactorily in a high ambient temperature. Similarly, low-inductance wire bondless packaging methods are not a necessity for silicon power modules owing to the high switching losses encountered by silicon devices at high switching frequencies. SiC devices do not have these performance limits. They have been demonstrated to operate at temperatures in excess of 500 ºC, and have been shown to have a fraction of the switching losses as compared to silicon devices at high switching frequencies. Hence the packaging solutions for silicon power devices are not necessarily the best choices for SiC modules. However, this currently standard practice for all commercial SiC power modules. Despite this, SiC modules outperform comparable silicon modules—but their benefits are not realized to the fullest.

Wire bonded interconnections are a weak link in SiC modules. Wide bandgap (WBG) power devices have the potential to bring about a reduction in the weight and volume of power systems. Passive devices and thermal management schemes are the principal contributors to the weight and volume of a power electronics system. The demand on thermal management systems are already reduced in WBG power modules due to their high temperature capability. To be able to use physically smaller and lighter passive devices requires high-frequency switching of the power devices. Wire bonds have an inherent parasitic inductance. This is why radiofrequency, microwave, and memory circuits employ flip-chip bonded devices. High-density and low-inductance interconnects like ball-grid arrays (BGAs) found their origins in these applications. However, most of these applications are targeted toward low power applications. Gallium nitride (GaN) power devices have also adopted wire bondless packaging techniques to achieve MHz-level switching. Even though GaN power devices are not high-voltage rated, their current ratings are comparable to SiC devices. High-frequency switching has been demonstrated to bring about a significant reduction in the volume of GaN power converters. Wire bondless packaging techniques

have also demonstrated improvements in silicon power modules—improved reliability, reduced overshoots, and provision for double-sided cooling to name a few.

This dissertation aims to explore wire bondless packaging techniques for SiC power modules. The goal was to investigate novel low-inductance packaging architectures for bare die SiC power devices. A flip-chip capable SiC package was developed and evaluated. The concept, manufacturing processes, and test results have been documented in detail—and the following section provides a description of the organization of this information.

Section 1.2: Organization of dissertation

This work is organized into nine separate chapters. The content of each chapter is summarized below:

Chapter 2: A comprehensive survey of silicon carbide packaging technology is presented here. The content encompasses main requirements of silicon carbide packaging technology, trends in silicon carbide integration, a discussion on the viability of 3D wire bondless integration as a path for SiC packaging, and a summary of 3D integration efforts thus far for power electronics modules.

Chapter 3: The concept of an integrated wire bondless power module is introduced, followed by a complete evaluation of the proposed concept. The module is investigated from the standpoint of thermal feasibility, performance under thermo-mechanical stress, and projected reduction in the parasitic inductance of the critical elements in the module. The chapter concludes with a discussion on the chief perceived concerns with the practicality of the material choices for the proposed module.

Chapter 4: Flip-attachment is proposed in Chapter 3 as a mode of interconnection for bare die SiC power devices. This chapter documents the development the test results for a novel sintered silver preform—an interconnect methods targeted toward achieving highly customizable and reliable flip-chip bonds for bare die SiC power devices.

Chapter 5: The concept of a flip-chip capable chip-scale power device package is introduced in this chapter. This new proposal addressed the materials-related concerns for the concept presented in Chapter 3. This allows a bare die SiC power device to be configured into an ultralow inductance component, thus giving a system designers complete freedom to incorporate it into their design. The concept is subject to a rigorous evaluation process in software from the standpoint of performance under thermal-stress and reduction in parasitic inductance. This was to ensure that the revised design and material choices did not offset the favorable effects evaluated for the concept in Chapter 3.

Chapter 6: A complete documentation of the process flow required to reconfigure a bare die SiC power device to a flip-chip power package is described. A rigorous process qualification is also included, where known-good reliability tests are employed to evaluate the process quality associated with the major steps. Finally, the performance of a flip-chip Schottky barrier diode package is evaluated to verify electrical functionality after the bare die is subjected to the entire process flow.

Chapter 7: The implementation of a flip-chip MOSFET package in a wire bondless half-bridge is the subject of this chapter. The switching performance of the novel devices were evaluated against the state-of-the-art, and the results are documented in this chapter. This work was a stepping stone to realizing the concept presented in Chapter 3.

Chapter 8: This chapter presents the practical implementation of the concept presented in Chapter 3, using the novel power device package introduced in Chapter 5. The evaluation and test results of a novel gate-drive-integrated 3D half-bridge power module is included.

Chapter 9: The final chapter focuses on the chief conclusions drawn from the efforts presented in this dissertation. The impact of the work from the viewpoint of improving the power density of future SiC modules is discussed alongside some concepts involving the same.

References

[1] F. Yang, Z. Liang, Zhiqiang Wang and Fred Wang, "Parasitic inductance extraction and verification for 3D planar bond all module," *2016 International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM)*, Raleigh, NC, 2016, pp. 1-15.

CHAPTER 2: A Survey of Silicon Carbide Packaging

DISCLAIMER: This chapter is a reproduction of a review paper by the author. The quoted text was published in a paper titled "Silicon Carbide Power Packaging—Past Trends, Present Practices, and Future Directions" in *Energies* 2017, *10*, 341.

"Wide bandgap (WBG) power devices are dictating the pace of development of power electronics today. There has been considerable advancement in the field of WBG semiconductor power devices. These have the benefits of enabling a high power density at high junction temperatures, coupled with faster switching speeds as compared with their silicon (Si) counterparts [1–6]. Thus far, silicon carbide (SiC) [1–3] and gallium nitride (GaN) [4–6] have been the materials of choice for most WBG modules. While GaN is the preferred choice in applications requiring <500 V, SiC excels in applications exceeding 500 V. SiC devices rated 900 V and above are available in chip sizes spanning just tens of square millimeters. In addition, the switching losses associated with SiC are much lower than the values reported for silicon power devices. SiC devices can be switched at higher frequencies resulting in filtering circuits that occupy less package real estate than their silicon counterparts.

Contributing further to the cause of power density is the fact that WBG devices may operate at high junction temperatures, thus introducing the possibility of employing more volumetrically efficient thermal management schemes. This combination can have a great impact on system miniaturization to help realize system architectures that do not even exist at the present time [7]. Although the properties of WBG materials seem almost too good to be true at first glance, the realized performance of these power devices are only as good as the package design. Even as the

die sizes of the WBG power devices are continually shrinking and the performance is improving, packaging technology is not keeping pace with these developments.

In a modern power electronics module, the size of the passive components and thermal management dictate the overall size. The power stage typically occupies a small fraction of the total volume. This, coupled with weak interconnections using wire bonds, introduces a spate of opportunities for improvement. In fact, eliminating wire bonds and designing shorter interconnects with lower parasitics itself could lead directly to a reduction in the size of passive circuit elements.

3D packaging has always been an attractive buzzword in the world of electronics packaging [8–11]. Most of the efforts in this area have been largely focused toward microelectronics, but the benefits translate to higher power modules as well [12]. However, it is necessary to take a step back and critically evaluate the need for a 3D approach and weigh it carefully against any foreseen disadvantages. It has been mentioned before that even in current state-of-the-art multi-chip modules (MCMs), coefficient of thermal expansion (CTE) mismatch of a single interface is a cause of concern—3D electronics packaging takes this problem and literally multiplies it by the number of tiers in the design. This poses the threat that 3D electronics packaging may open a plethora of design challenges.

The immediate benefits of using a 3D topology are clearly apparent—a reduction in parasitics, use of efficient distributed cooling schemes, a reduction in footprint and consequent increase in power density. However, caution should be exercised regarding the implementation of such a scheme and the ramifications it may have on the overall system performance. The question being asked here is: are we solving a problem, or trading one problem for a host of others?

Research in electronics packaging over the past two decades bears testimony to the desire to move away from wire bonding as an interconnection method [13–16]. There have been several attempts to propose alternative methods, and many of these will be investigated in this paper in due course. Most of the methods reported a decrease in the parasitic inductance in the critical switching loops and projected a relative increase in reliability as compared with modules having wire bonded interconnections.

The packaging of SiC power devices are deeply rooted in the wire bonding approach used for silicon metal-oxide-semiconductor field-effect transistors (MOSFETs) and insulated gate bipolar transistors (IGBTs). Wire bonding has been the standard approach used in MCMs because of ease-of-use and low production costs. As far as performance of an interconnect goes, parasitic inductance, reliability, and cost/manufacturability are the major parameters. Wire bonds offer a significant parasitic inductance; however, it does not manifest itself too adversely at switching frequencies ranging up to tens of kHz. Since most commercially available silicon power modules are well within this specification, switching transients resulting from the parasitic inductance of a wire bond are still within tolerable limits. However, the situation is very different with WBG devices which have shown promise at frequencies exceeding 1 MHz. It is for this reason that many GaN manufacturers have adopted a land grid array (LGA) or ball grid array (BGA) approach in favor of wire bonding. On the down side, the reliability concerns of such approaches have prevented a wide-spread adoption of these techniques across the WBG industry.

This paper aims at investigating the trends in SiC power packaging over the past decade and highlights some of the high-performance modules. *Section 2.1* summarizes the chief requirements of SiC packaging. From a survey of these advanced wire bonded SiC modules in *Section 2*.2, the major technology bottlenecks for the further advancement of SiC packaging technology are

assessed. *Section 2*.3 makes a case for wire bondless packaging. Investigations into previous work in silicon 3D wire bondless packaging are presented in *Section 2.4*. Some of the more recent 3D integration efforts in SiC modules are described in *Section 2.5*, followed by a summary of future efforts and directions in *Section 2.6*.

Section 2.1: Requirements of Silicon Carbide Packaging

In the case of any power device technology—Si, SiC, or GaN—the goal should be to ensure that the package does not hinder the performance of the device. A common example of this is package parasitics. Through hole and surface mount packages have been standard choices for discrete power devices for an extended period of time. In fact, many high performance power electronics systems still use discrete devices—they are simple to assemble and easy to replace upon failure. Most of these applications used switching frequencies in the range of 1–5 kHz. As packaging materials are added to the package, the electrical path to the terminals increases significantly. Additional parasitic inductance is perhaps the most significant adversity that arises at the result of this. As power MOSFETs were introduced and became popular, the major manufacturers began making power devices available in bare die form. This offered power module designers more flexibility to minimize parasitics and increase power density. This became especially important as switching frequencies increased. Switching frequencies up to 25 kHz are becoming increasingly common for SiC power modules. This requires a more thoughtful consideration with respect to module layout and interconnect technologies. Some practices, such as including a Kelvin source terminal for the gate driver return path, have become extremely helpful for SiC module design. Some manufacturers like Wolfspeed have also been including an additional Kelvin source terminal with their discrete devices as well.

SiC power devices have the potential to impact power density at all levels in the package—a reduction in the size and number of power devices, a reduction in the size and number of passives for filtering circuits, and a reduction in the volume of thermal management [1]. The advent of high voltage SiC power devices will eliminate the need to parallel a large number of power die. This will reduce system complexity and improve system reliability. However, a careful examination is required to be able to assess the requirements of SiC packaging.

Although measures are being taken to reduce the critical switching loop parasitics in SiC power modules, it must be acknowledged that wire bonds are one of the major causes of parasitics. Even a short wire bond has an inherent parasitic inductance that often dominates the total parasitic inductance of the entire loop [2]. These stray inductances do not affect the circuit if the switching frequencies are low enough. Considering that the switching losses of Si power devices increased significantly with switching frequency, rudimentary parasitic minimization strategies provided satisfactory electrical performance. However, despite having relatively lower switching frequencies the overshoot arising from the power loop parasitic inductance ensured that selected power devices had to be over-rated to able to accommodate this.

Meade conducted a detailed study on the parasitic problem in 2008 [3]. A simple DC-DC converter topology was chosen to demonstrate the effect of parasitic loop inductances on electrical performance. The turn-off losses dominated, especially as the switching frequency approached 2 MHz. A drastic reduction of the turn-off losses was demonstrated for a wire bond-less packaging method at 3 MHz switching frequency. The losses were much worse for discrete devices. Traditional wire bonded techniques resulted in nearly twice the turn-off losses as compared with the wire bond-less technique. Another interesting fact was that paralleling wire bonds does not alleviate he parasitic problem. The mutual inductance between adjacent wires starts dominating,

and there is a limit to which increasing the number of wire bonds can help—a fact presented in a 2016 publication by Yang [17]. Wire bond-less packaging must be pursued as a thrust area for SiC packaging if high voltages and currents are desired to be switched at several MHz. However, faster switching would directly translate to a risk of producing greater electromagnetic interference (EMI), and caution must be exercised to prevent this.

EMI suppression is another cardinal aspect of package design that has assumed importance owing to rising *dv/dt* rates in power electronic circuits. One of the common design philosophies which we will encounter in due course is to integrate the gate driver circuit closer to the power device to form low-area switching loops to reduce parasitics. Although this is the correct approach in principle, high slew rates introduce injected current spikes through the parasitic capacitances in the circuit. Future SiC modules must take this into account. As gate drivers and decoupling capacitors are included in the module itself, care should be taken to decouple spurious current spikes from influencing false turn-on events and leading to premature module failure.

From the viewpoint of thermal design, there are two principal thrust areas: (1) thermo-mechanical design strategies for low stress and high reliability; and/or (2) double-sided cooling methodologies. While the first area is advantageous regardless of package type, the latter depends on the critical performance criteria for a given module.

There has been a substantial amount of work in identifying and developing materials having a close CTE match with SiC. Many of the approaches are discussed in this paper in due course. Die attach failure and interconnect failure are among the chief ways in which CTE mismatch manifests itself. This may be attributed to the CTE of a wire bond or bond pad being significantly different as compared with SiC. Another common location at which delamination occurs is the interface

between the substrate and heat spreader (or heat sink). Some of the solutions that have been proposed to address these issues are using compliant mechanical materials like sintered silver as the die attach material. The "sponge-like" nature of this material makes it adept at cushioning CTE mismatch stresses. Other methods include the development of alloys and metal-matrix composite materials like MoCu or AlSiC. The CTE of these materials are very well matched to SiC and can be tailored by altering the composition of the compounds. These materials are easy to plate and bond to both the devices and heat sinks (or baseplates).

Double sided cooling is another option in order to reduce thermo-mechanical stresses. If the junction temperature is controlled to a low enough value, CTE mismatch stresses will not adversely impact module reliability. However, a double-side cooled module necessitates a wire bond-less packaging approach. Double-sided cooling is also advantageous in modules employing a large number of chips. This may be a very good proposition for vehicle under hood applications, where the ambient temperature is already at elevated levels. A single-sided cooling solution may simply not be enough to handle the thermal load as power densities increase.

While we are on the issue of thermal performance, there is an important factor to consider. Contemporary Si devices are rated to operate at a junction temperature of 175 ℃. Most commercially available SiC devices are also rated for a similar temperature range, although researchers have been able to demonstrate a decent performance at higher temperatures as well. The theoretical limit of SiC as a semiconductor material is well beyond 500 ℃. Yet the ratings of commercially available devices do not reflect this advantage. One issue could be the reliability of the chip metallization at elevated temperatures—an extremely valid concern. However, there are other factors at play here. These concerns have been echoed in a 2009 publication by Wrzecionko [18]. They demonstrated that although the theoretical limit for the operation of SiC power devices

can be as high as 700 °C, in reality the optimum temperature was less than 300 °C. The authors were of the opinion that if a device is operated below the optimum temperature, it was not possible to take complete advantage of the junction gate field-effect transistor (JFET). A higher than optimum temperature of operation, on the other hand, ran the risk of thermal runaway. The paper also demonstrated that the power density could be improved greatly by either using a chip with a larger area and/or using double-sided cooling. Both the suggested methods were prescribed with the intention of reducing the thermal resistance. This particular study involved SiC JFETTs, but the same concerns are applicable to MOSFETs as well. A cooler junction temperature also has a positive influence on module reliability.

One of the other concerns of SiC packaging is the metallization of the bare die power devices. The surface finish for all SiC power devices is aluminum for the top side bond pads. This is understandable, since aluminum wire bonding is one of the most widely used means of interconnection. The bottom side finish is usually silver to aid wetting during the soldering process. The silver finish also facilitates advanced die attachment processes like silver sintering. To be able to implement wire bond-less procedures, a reliable and solderable top surface finish is required. One way to circumvent this issue is the use of pressure contacts on the top pads. However, there may be contact resistance issues using these methods that may need to be addressed. A metallurgical bond will require the top side finish to be a solderable metal. This may be done during device fabrication, or re-engineered during the assembly process by incorporating a plating, evaporation, or sputtering. Electroless Ni/Ag has been a standard plating process for rendering IC chips solderable in the past, and it could work for power devices as well. However, there is no evidence to address the long-term reliability of these approaches, especially in high temperature

environments. There is no clear answer for an optimized metallization stack up that can attain the same thermal performance standards that SiC devices have been reported to have.

Material concerns should not be limited to metallization alone. Interconnects and encapsulation materials should also withstand comparable thermal stresses. Perhaps the most exhaustive subject of thermo-mechanical stress analysis has been die attach materials. This is perhaps because the die attach interface is both electrically and thermally critical, and extremely prone to cracking under thermal stress. There are analytical models of die attach materials and long-term reliability prediction algorithms based on these models. However, as the operating temperature rises, all parts of the package will assume importance and have to be thoroughly studied before it can be incorporated into a commercial product.

Section 2.2: Trends in Wire Bonded Silicon Carbide Packaging

SiC power devices have been predicted to have tremendous potential to be the next generation material in the semiconductor industry [1–3, 19–21]. These devices have been shown to operate in extremely high ambient temperatures with very low degradation in performance [22]. The packaging methods employed for SiC power modules, however, have not witnessed much change from the traditional silicon die attach and wire bond process flow.

This was not considered to be a huge obstacle until recently, since the SiC material system itself was found to be much superior to silicon. SiC devices performed much better than their Si counterparts, even while using standard packaging approaches. However, as engineers around the world are gaining a better understanding of SiC devices, the limits of the Si-based packaging schemes are becoming more evident. Most of these packaging approaches bear fundamental performance limits imposed by the physical limits of Si device physics. For example, wire bonding

has sufficed as an interconnect technology in modules that switched at the safe operating limits of SiC power devices. Similarly, CTE mismatch stresses were tolerable in Si power modules, most of which were rated at much lower maximum operating temperatures as compared with SiC. As SiC power devices are demonstrated to operate in ambient temperatures pushing the 500 °C mark, most Si power module material choices will be rendered unusable. Nevertheless, even without employing unconventional and "out-of-the-box" packaging methods, SiC packaging efforts over the years have successfully demonstrated some noteworthy feats.

A 2007 study from Arkansas Power Electronics International (APEI) Inc. (now Wolfspeed, Fayetteville, AR, USA) documented the test results of a 4 kW three-phase power inverter operating at a junction temperature of 250 °C [23]. The design and choice of packaging materials used was a combination of known-good approaches for MCMs using Si IGBTs. The power devices in the module were SiC JFETs. Extending the results to a 10 kW inverter based on an identical approach, the authors predicted a 75% overall decrease in the volume as compared with a comparable Si inverter. One major reason for this was the high temperature operability of the SiC devices, which reduced the requirement of volume-intensive thermal management methods.

Most packages developed around this time did not push the envelope in terms of incorporating novel packaging materials, but there was a growing consensus among industry and academia for the need to think unconventionally to extract maximum benefits.

This issue was addressed in a 2008 paper from General Electric, in which design choices were explored to ensure operation at 250 °C [24]. Substrates, die, attach materials, interconnects, and encapsulation materials were explored individually. Direct bonded copper (DBC) substrates were observed to fail within the first 20-30 cycles of testing, clearly exposing the need for new substrate

technologies at higher temperatures. Sintered thick film silver metallization on alumina performed the best showing no failures up to 1000 thermal cycles. Direct bonded aluminum (DBA) on aluminum nitride also performed comparably and may be a high temperature alternative as well. As far as die attach materials were concerned, it was reported that 95Pb5Sn high temperature solder was good at absorbing CTE mismatch stresses. A novel miniature top-loading laminated bus structure was designed for this module. This enabled a low-inductance path to the power devices, and in-turn allowed them to switch at a faster frequency.

Interconnect inductances were further reduced by using vertical spring-loaded pins instead of wire bonds. The spring-loaded pins were also reported to be more compliant under thermo-mechanical stress. Common epoxy mold compounds did not hold up to partial discharge testing under high temperatures. Nusil and Sylgard were the only compounds that yielded satisfactory performance up to at least 400 hours of testing. The temperature for module testing however was limited to 100 ℃, and there was no documented data for the system/module reliability with respect to time or temperature.

A more recent study published in 2011 documented the design benefits of SiC power converters over silicon based converters [25]. In this study, a 1.5 MW wind turbine frequency converter was designed. The first step in this study was a characterization of the switching characteristics of the SiC power device as a function of temperature. It was reported that the switching loss of the SiC device were almost unaffected by temperature, but that for silicon devices the losses increased by 56.3% when the case temperature increased to 125 °C from 25 °C.

The system was also analyzed at switching frequencies of 3 kHz and 50 kHz. At both frequencies, the losses associated with the silicon converter far exceeded the SiC converter. The

loss in efficiency for a Si IGBT beyond 20 kHz made it unusable, while the efficiency of the SiC converter even at 50 kHz exceeded 85%. This, of course, introduced possibilities for a significant reduction in the size and cost of the passive circuit elements for the filtering circuitry. The power losses associated with the filtering passives were also reported to decrease.

Another interesting part of this study was high temperature operation of the converters. At an operating temperature of 150 °C the volume of the SiC based converter was substantially smaller than the Si converter. Moreover, the SiC converter did not need liquid cooling, and the overall cost of the heatsink was also much lower than the Si converter. At a junction temperature of 300 °C, the situation improved further for the SiC converter offering a 49.5% additional reduction in volume as compared with the 150 °C converter. Silicon power modules cannot operate at these temperatures, and SiC modules can go even higher with the appropriate packaging choices. Unfortunately, no hardware was tested over time to validate the reliability of operation in a 300 °C ambient.

An effort from APEI Inc. in conjunction with the University of Arkansas in 2008 showcased a leap in next generation packaging for SiC modules [26]. The highly integrated half bridge module (Figure 2.1) was capable of operating at 250 °C and also won the R&D100 award in 2009.

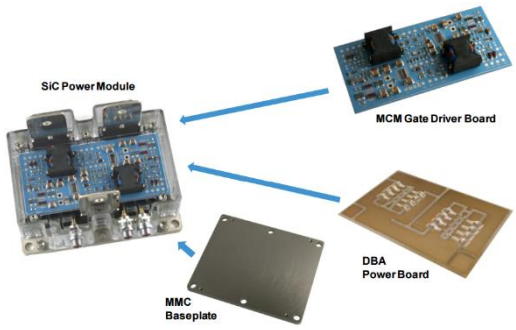
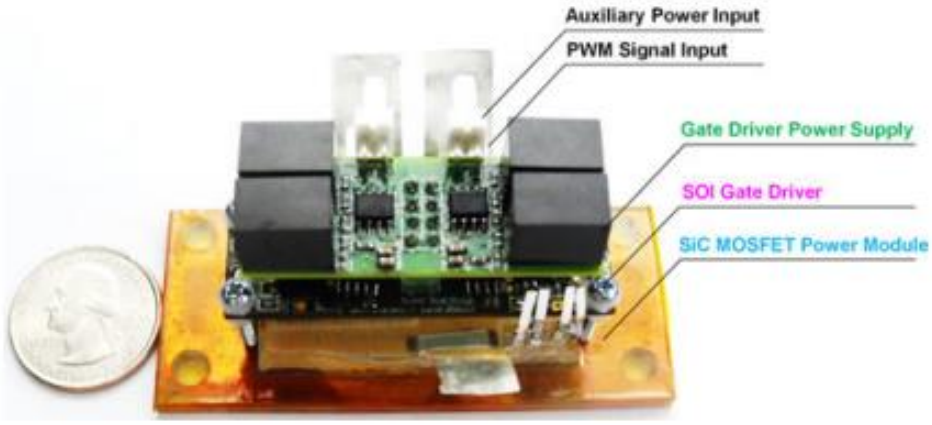


Figure 2.1: The high temperature half-bridge SiC module [26]. DBA: direct bonded aluminum.

The gate driver board was made of low temperature co-fired ceramic (LTCC) material capable of withstanding high temperatures. The magnetics used were fabricated in-house in order to meet the temperature requirements, and the size of the passives were reduced considerably by driving the half-bridge at 150 kHz switching frequency. To enable an increased switching frequency, the gate driver board was mounted directly atop the power stage to offer a low inductance vertical path for the gate signal. The stacked approach also reduced the footprint of the module, enabling high density integration even at elevated temperatures. As a proposition for future work for reducing the size and enhancing performance, it was discussed that the gate driver would be placed on the power stage to further reduce parasitics.

For most applications involving high voltage slew rates at high temperatures, the choice of gate driver becomes a limitation. In many investigations, the SiC module itself was tested inside a high temperature oven, while the gate driver and controls were placed in a lower ambient temperature. This problem was addressed in a 2015 publication by Wang et al. [27], in which a silicon-on-insulator (SOI) gate driver was integrated with a SiC power module. The integrated module shown in Figure 2.2(a) was operated at a temperature of 200 °C and a switching frequency of 100 kHz [Figure 2.2(b)]. This study brings to light the importance and necessity of gate drivers which match the performance of the SiC power devices. A denser integration of the gate driver and the power devices would mean that the driver chip also experiences similar temperatures as the power die.

From all the above studies, it was clear that the performance of a module is package limited. Not one of the studies investigated revealed that SiC had failed as a material at high temperatures. All the expressed concerns dealt with the dearth of adequate packaging materials and technologies at these temperatures.



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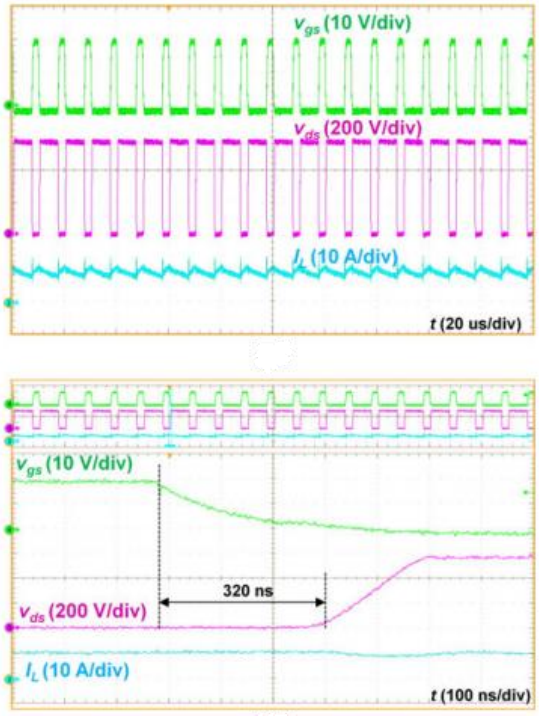

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Figure 2.2: (a) A photograph showing the module developed by Wang et al. [27]; and (b) waveforms showing the operation of the power converter. SOI: silicon-on-insulator; and MOSFET: metal-oxide-semiconductor field-effect transistor. Reprint with permission [4062710688514]; Copyright 2014, IEEE.

The story of the high frequency applications of SiC bears a striking resemblance to the high temperature applications. The material itself can switch well into the MHz range. At these

frequency levels, the passives employed may be a fraction of the size compared with what is used today. The overall system cost, volume, weight, and losses will also decrease. However, the system implementation is the bottleneck. A high switching frequency implies a high slew rate for the switching currents and voltages. This induces undesirable current spikes through the parasitic capacitances present within the system, leading to a potential system failure due to a false switching event. This phenomenon discourages applications involving frequencies in excess of several hundred kHz. Nonetheless, switching reliably and efficiently at 50 kHz is in itself a huge improvement over silicon MOSFETs and IGBTs. This section explores notable efforts in pushing toward higher switching frequencies, and aims to identify the barriers that prevented a further increase in frequency.

A 2003 study by Elasser et al. [28] contrasted the performance of the then novel SiC diode against commercially available silicon diodes. Switching losses during reverse recovery at high *di/dt* were one of the parameters of comparison, and the performance was compared at room temperature as well as at 150 °C. The circuit was tested in a boost converter topology switched at 100 kHz, with a silicon IGBT. It is important to note that this was a low power application with a 500 W full load, but it was sufficient to illustrate the benefits of SiC technology and the concerns with inferior packaging of SiC devices. Table 2.1 lists the results of the analysis. The results showed an order of magnitude decrease in the switching losses associated with the SiC devices. Furthermore, the reduction seemed impervious to an increase in junction temperature, where the losses for the silicon based counterparts nearly doubled with an identical temperature increase.

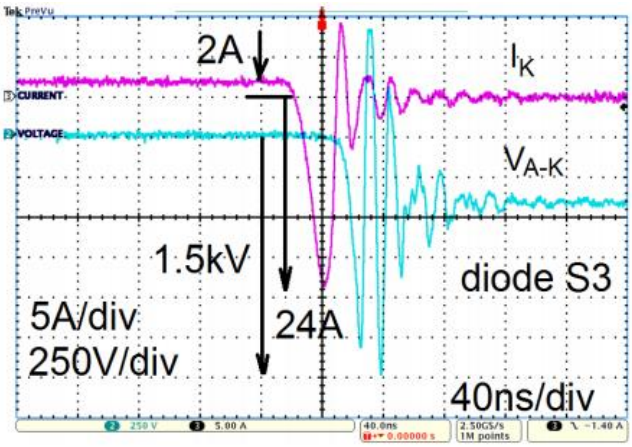
Table 2.1: Performance comparison of Si vs SiC diodes at 25 °C and 150 °C at 480 A/μs [28]. DUT: device under test. Reprint with permission [4062720248056]; Copyright 2003, IEEE.

	DUT T_j = 25 °C			**DUT T_j = 150 °C**		
	Fast Si Diode	Ultra-Fast Si Diode	SiC Diode	Fast Si Diode	Ultra-Fast Si Diode	SiC Diode
Diode Losses	344 μJ	86 μJ	8 μJ	704 μJ	268 μJ	26 μJ
IGBT Losses	320 μJ	88 μJ	56 μJ	912 μJ	172 μJ	56 μJ
Total	664 μJ	174 μJ	64 μJ	1616 μJ	440 μJ	92 μJ

Several studies have been published since, which have supplemented the favorable recovery characteristics of SiC SBDs. It is hardly surprising that they are ubiquitous in most high performance power modules that are produced today. In 2011, Adamowicz et al. [29] conducted a similar study, with a cardinal difference. They fully appreciated the benefits of a near-zero reverse recovery offered by SiC diodes, but with caution toward the implications from the standpoint of EMI. A 100 kHz converter was constructed using SiC JFETs and SiC freewheeling diodes (FWDs). The performance was also contrasted by using a Si FWD in conjunction with the SiC JFETs.

Figure 2.3(a) shows the turn-off waveform for the silicon fast diode. The performance was unacceptable at 100 kHz with the reverse recovery current exceeding 24 A while carrying just 2 A. Voltage perturbations were also reported in the test circuit as a result of EMI with magnitudes

exceeding 1.5 kV. This could potentially kill power supplies, gate drivers, and even the power devices themselves.



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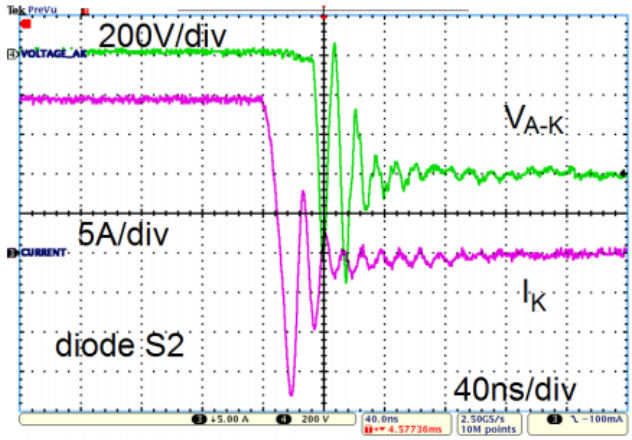


(b)

Figure 2.3: Comparison of reverse recovery transients using (a) Si fast recovery diode; and (b) SiC diode [29]. Reprint with permission [4062730593351]; Copyright 2011, IEEE.

Figure 2.3(b) shows the result for one of the SiC diodes under investigation. Oscillations could still be observed in the turn-off waveforms, but were tolerable. An interesting observation was that two diodes with similar characteristics showed slightly different damping on the gate-source signal. It was deduced that the source lead parasitic inductance contributed the gate-source ringing.

This is another instance where it was proved yet again that the performance of the SiC device was packaging limited. The estimated lead inductances in the discrete components used for this study were reported to be around 20 nH.

Since this time, most integration efforts have been focused on tighter integration to reduce interconnect inductances and mitigate the EMI arising as a consequence. This is a compelling reason for most major SiC manufacturers providing an additional Kelvin sense terminal in their discrete component packages [30].

A significant step forward in high frequency operation and its impact on system size and performance was presented in a 2013 publication from APEI Inc. and Toyota, in conjunction with the University of Arkansas [31]. The illustrated high power density plug in HEV battery charger also won an R&D100 award in 2014. The designed converter was switched at a frequency of 500 kHz and yielded an efficiency of 93.4%. The efficiency increased to 96.5% as a result of decreasing the switching frequency to 200 kHz, which is still an impressive frequency as compared with the competition.

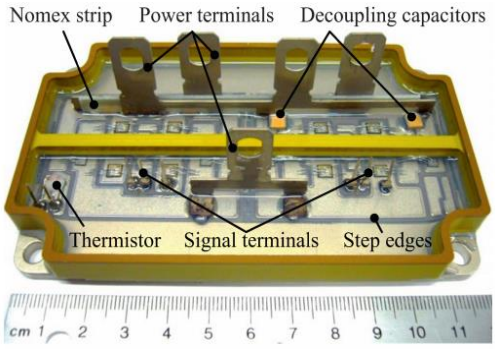
The increase in switching frequency allowed the designers to reduce the size and weight of magnetics and relax the demands required by the heat sink. The result was a volumetric power density of 12 kW/L, and a gravimetric power density of 9.1 kW/kg. The weight was especially important since this module was designed to operate in a mobile system. The researchers reported that customized package design was a key enabler in being able to push the performance of SiC technology closer to what it is capable of. Design improvements included a customized low inductance power module. The gate driver board with the associated circuitry was mounted in close proximity with the power module.

The power module was mounted on a MMC baseplate to reduce the CTE mismatch and weight, and facilitated high temperature operation. Even with these commendable efforts to leverage high frequency operation, the authors reported that the thermal management and the inductors used in the module comprised 73% of the weight, and 66% of the volume respectively. It was discussed that pushing the operating frequency beyond 500 kHz would help further volumetric gains, but it was not clearly stated what prevented the authors from doing so in this revision itself.

In a separate publication in the same year, APEI reported that they had operated the X5 module at frequencies in excess of 1 MHz while maintaining an efficiency greater than 93% up to nearly 4 kW output power [32]. It was reiterated in the paper that the design philosophy for switching at these unprecedented frequencies relied heavily on tighter integration between the power devices, drive circuitry, and decoupling capacitors.

The need for a high temperature and high frequency module was also the underlying motivation for a 1.2 kV, 120 A phase leg module using SiC devices by Chen et al. [33] in 2016. By optimizing the layout of the module, a 40% reduction in the switching loop inductance was possible, even while using wire bonded interconnections. The module was also demonstrated to operate at 200 °C junction temperature. The power module is shown in Figure 2.4(a). The substrate used was DBC with AlN as the ceramic—a common material if choice for SiC power modules. However, DBC substrates have gained a negative reputation for delamination during high temperature swings. To remedy this, a step-edge approach was used in which the edges of the copper traces on the DBC were etched so that they formed a tapered step on the edge. This makes the copper less prone to peeling under thermal stress [34]. A photograph showing the patterned substrate with a step-edge is shown in Figure 2.4(b).

The parasitic ringing and overshoot for this module were reported to be 20% lower as compared with a commercial module even without embedding decoupling capacitors within the module. VDS slew rates as high as 13.9 V/ns were achieved with using a 0 Ω external gate resistor due to the favorable switching transient behavior. The overshoots and switching energy comparison is shown in Figure 2.4(c). No EMI related issues were reported despite the unprecedentedly high voltage slew rates.



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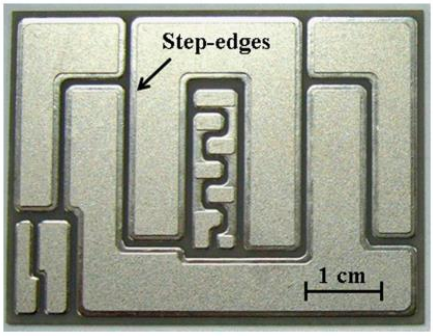

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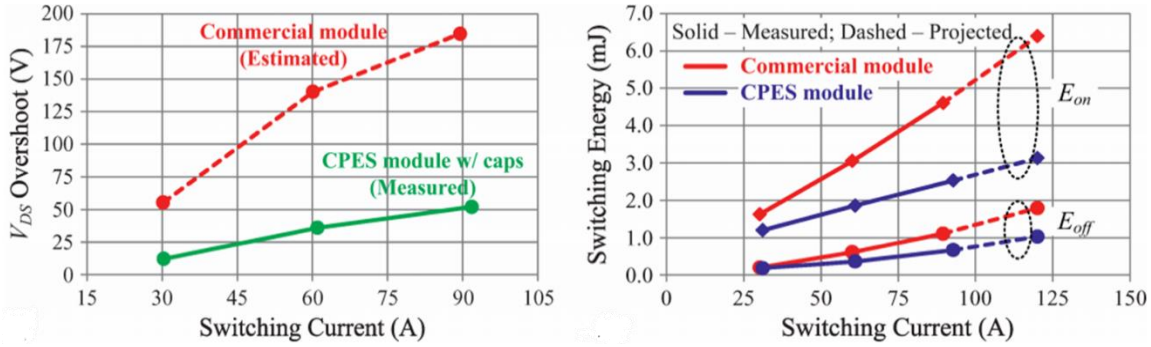

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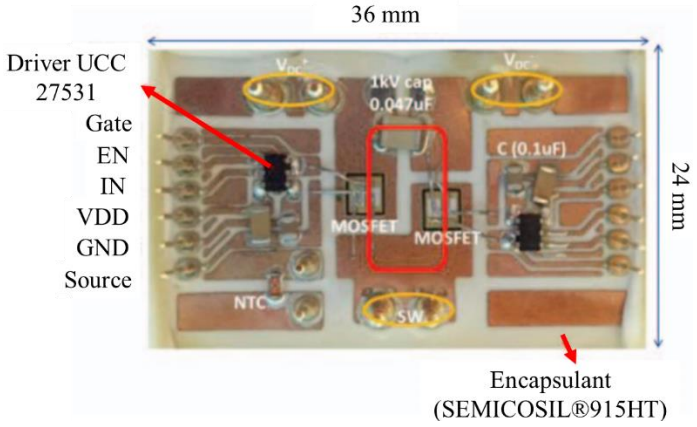
Figure 2.4: (a) Photograph showing the power module; (b) step edge technology for improved reliability at high temperatures; and (c) a comparison of switching performance between the (Center for Power Electronics Systems (CPES) module and a comparable commercial product.

Another noteworthy accomplishment in the recent past came from researchers at the Future Renewable Electric Energy Delivery and Management (FREEDM) center (North Carolina State University, Raleigh, NC, USA). The authors in their abstract mentioned with respect to power modules that "The era for high voltage-megahertz switching has arrived [35]." A 1.5 MHz synchronous boost converter and a 3.68 MHz half bridge inverter were demonstrated. Figure 2.5(a) shows a photograph of the top view of the power module. It can be noticed that the gate drivers for the respective switches were mounted as close as possible to the power die on the power module itself. This resulted in a significant reduction in the gate loop parasitic inductance and prevented false turn on effects due to the EMI generated at the high *dv/dt* levels generated in the circuit. Figure 2.5(b) shows a photograph of the module with the heatsink, and Figure 2.5(c) shows the switching waveforms.



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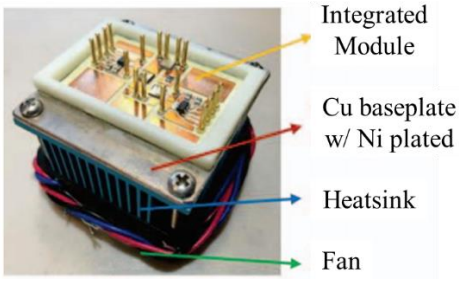

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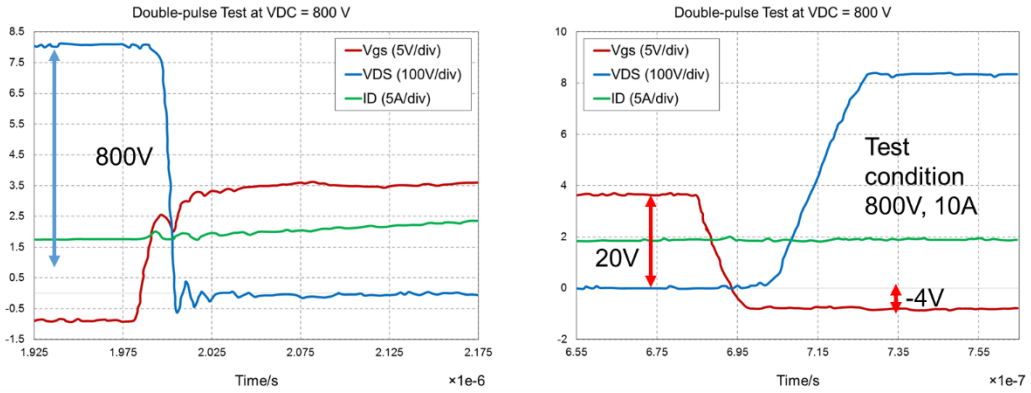

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Figure 2.5: A 3.68 MHz SiC power module from the FREEDM center at North Carolina State University [35]. EN: enable; IN: input; VDD: drain voltage; and GND: ground. (a): A photograph showing the top view of the module; (b): A photograph showing the whole module assembly with the heat sink; and (c): Test waveforms showing the switching characteristics of the module. Reprint with permission [4062731030342]; Copyright 2015, IEEE.

The efforts presented in this section summarize admirable research to place SiC technology a cut above conventional silicon power modules in terms of performance. All the above approaches used existing packaging technologies and materials in novel ways, and employed good engineering practices to develop next generation power electronics modules. However, the achievements still grossly underutilized the full gamut of performance benefits that SiC devices have to offer. One of the key enablers in pushing performance would be the interconnect technology.

Some issues are common for the packaging and integration of any class of semiconductor technology. Heat sinks and passive devices are two examples of such issues. Be it silicon, SiC, or GaN—these components occupy maximum space and weight in the package. Using WBG technology to help relax the demands of a big and heavy heat sink may alleviate the issue from the standpoint of thermal management. It will also encourage innovations in heat sink technology. However, efficiency is really a more dominant concern in power converters. Producing efficient topologies and packaging solutions may not even create substantial waste heat to begin with. This coupled with the high temperature operability of SiC devices have the potential of greatly impacting the volume occupied by the thermal management in a power module. A far as passive devices are concerned, significant reductions in size and weight are possible when switching frequencies are increased, as have been documented by several of the aforementioned research efforts.

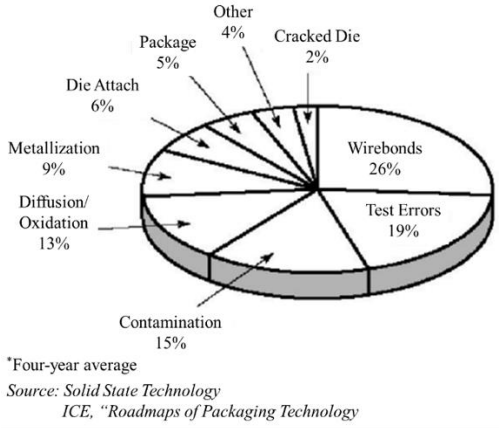
Section 2.3: Wire Bondless Packaging—The Road Forward?

The quality and reliability of power modules has a direct influence on resource utilization, the cost of production, and energy efficiency in the industry. We are at the peak of global electrification, and the trends predict a steady increase in the foreseeable future. The sphere of applications of electronic modules is ever-increasing—and it is perhaps time to move past the "one

size fits all" packaging solutions that have been strongly adhered to up to now. Conventional packaging materials and methods have been known to perform poorly under both thermal and electrical stress. Hence, applications involving harsh environments have typically been most accepting of novel packaging technologies. In fact, most innovations pertaining to the field of electronics packaging have been targeted toward applications with harsh temperatures, harsh environments, high power levels, large voltage swings—or any combinations thereof.

In their 2011 paper summarizing the challenges in power packaging, Liu and Kinzer [36] from Fairchild Semiconductor hailed SiC as a foreseeable future replacement for silicon power devices. However, they agreed that the interconnection scheme had to improve. They discussed alternatives to conventional wire bonding—such as copper ball bonding, wedge bonding, clip connections, copper stud bumps, flip-chip bonding, etc. Many of these approaches will be discussed in due course. They also discussed that as SiC chip sizes shrink, there needs to be effective mechanisms for increased heat transfer. Double-sided cooling can be explored as an example, by adopting wire bondless sandwich-type modules.

In 2007, Bower et al. [37] documented some of the common issues that were being reported in relation to the failure of SiC modules. Unsurprisingly, wire bond fatigue topped their list, in itself accounting for the most failures associated with a single component [Figure 2.6(a)]. Figure 2.6(b), (c) show the dominant failure mechanisms in wire bonds.



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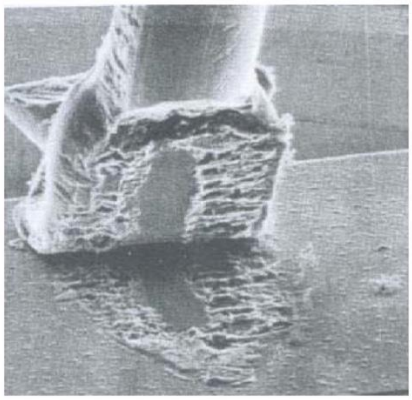

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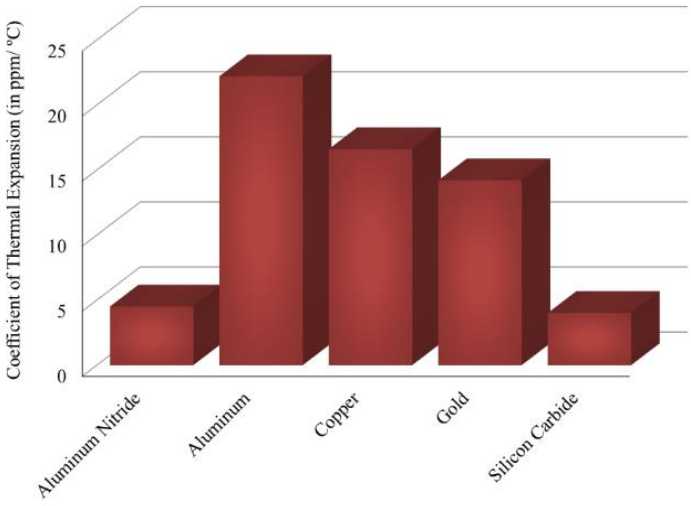
Figure 2.6: (a) A pie-chart depicting the failure modes in SiC power modules; (b) a photograph showing wire bond lift off; and (c) a photograph showing wire bond heel fracture [37]. Reprint with permission [4062731448789]; Copyright 2008, IEEE.

Wire bond lift off occurs due to the same reason that solder interfaces fail—due to CTE mismatch stresses between the bond pad and bonding material. However, the CTE of the metals used for wire bonding differ by a large margin from the substrate materials as shown in Figure 2.7(a). Hence, they are prone to fail much sooner under repeated thermal stress or high temperature than a solder joint would. In fact, CTE is not all that materials for a thermo-mechanical stress. Even eutectic solder and sintered silver have a high CTE, but they are better at absorbing thermo-mechanical stresses due to their low Young's modulus. Figure 2.7(b) shows a comparison of the Young's modulus of wire bonding metals and common die attach materials.



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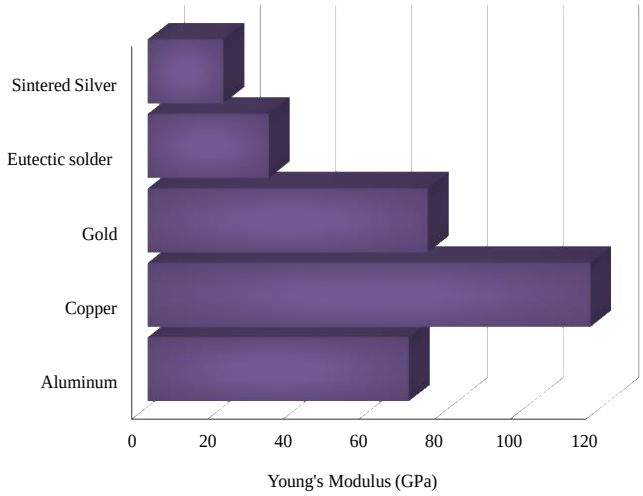


(b)

Figure 2.7: A bar graph comparing the (a) coefficient of thermal expansion (CTE) and (b) Young's modulus of materials used in a state-of-the-art SiC power module.

To improve the mechanical strength of wire bonds, some measures have also been taken to utilize thick Cu/Al-Bi ribbon bonding instead of aluminum [38]. However, like with most copper wire bonding approaches, this has the risk of damaging the die due to excessive bonding force/energy [36]. Ribbon bonding does not, however, solve the problem of connecting the gate

pad of a SiC MOSFET. With the shrinking die sizes of SiC devices, justifying the use of ribbon bonding is going to become increasingly more difficult. Also, any type of wire bonding technology eliminates the possibility of double-sided cooling or 3D integration, which brings us to our next topic.

Section 2.4. 3D Integration Efforts

There have been several attempts to provide better alternatives to wire bonding through 3D wire bondless technology. Although the industry has adopted a handful of these propositions, most of the proposed solutions exist only as proof-of-concept. The main explanation for this is that the reliability and performance benefits offered by a large majority of these solutions can seldom justify the cost of a complete retooling of a manufacturing facility. If a simple solder and wire bond based module of sufficient engineering quality meets the target module lifetime with satisfactory performance, there is hardly a need to think about 3D solutions. However, this situation is rapidly changing with elevated demands on the performance and operating conditions that power modules are expected to meet. There are numerous other advantages to be realized in a well-engineered and non-conventional packaging scheme—decreased material costs, faster performance, reduced electromagnetic interference, and improved thermal management to name a few. Among the innovative schemes proposed in the last 5–10 years, only a few have managed to successfully transition into a commercial module from a proof-of-concept.

Power electronics packaging has always borrowed liberally from microelectronics packaging advances in the past. Most of the chip-on-board, flip-chip, and 3D through silicon via (TSV) research that exists in the literature is targeted toward low power microelectronics or sensor applications [39–44]. Low power RF circuits have also adopted wire bondless BGA-based packaging methods as state-of-the-art due to the parasitic reduction offered by such 3D integration

schemes, reduced cost, and reliability benefits [45–48]. There is also a wealth of literature in support of the favorable aspects of BGAs. In fact, an application note from Fairchild Semiconductor a silicon BGA package has been described as a step in the direction of realizing the "perfect MOSFET" [49]. However, in this investigation we only intend to include the advances in 3D/wire bondless power module packaging in detail.

Most of the 3D packaging solutions proposed to date utilize Si devices. These propositions came at a time when Si technology was hitting a limit in terms of performance. Wire bondless integration offered hope from the standpoint of better signal integrity and reliability. The inherent properties of WBG were found to be so much more superior to their existing Si counterparts, that even standard Si MOSFET and IGBT packaging techniques used for packaging SiC devices reaped huge benefits. This situation must change with the realization that the Si-based packaging approaches were tailored to the performance limits of Si semiconductor technology. It is instructive to take a close look at what benefits 3D packaging techniques had for Si packaging, and reflect upon whether this is the path to follow for highly integrated SiC modules.

The power overlay technology proposed by General Electric in 1995 [50] was also presented as a viable approach for wire bondless interconnections (Figure 2.8). In this technology, the flexible interposer is 2 mil thick Kapton polyimide film. Vias are formed on top of the power device connections by laser ablation, and are metallized by sputtering or plating to form interconnections. Surface mount devices could be directly mounted on top of the power devices, and vertical interconnections ensured that the parasitic circuit elements were reduced significantly. This technology was capable of handling high operating voltages of up to 2400 V and a device power dissipation of up to 200 W.

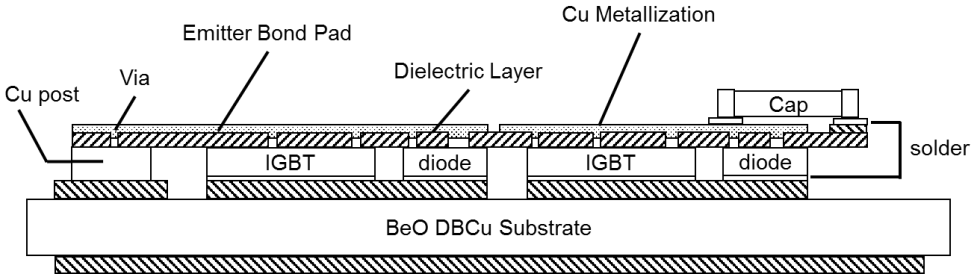


Figure 2.8: A schematic showing the cross section of the General Electric (GE) power overlay technique [48]. Reprint with permission [4062740331943]; Copyright 1995, IEEE.

The skin interconnect technology introduced by Semikron in 2011 (Figure 2.9) was a major step towards both wire bond-less interconnections, as well as 3D integration [51]. Metal traces printed on a flexible foil serve as interconnections. This foil has patterns that mate directly on top of power devices and connect to them by silver sintering technology. A 400 A, 600 V dual IGBT module using SKiN interconnections was fabricated. The thermal solution used for this module is a pin fin heat sink which is also sintered to the substrate, and is fluid cooled. This ensures high reliability performance for the module [52] as compared to conventional solder technology. The wire bond-less SKiN module showed an average reduction of 9.68% in parasitics over a comparable wire bonded module. It was apparent from the inspection of the failure mechanisms that the joint between the flexible foil and the power device is the weak link in power cycling tests. It must be mentioned that the SKiN module survived more power cycles than any comparable state-of-the-art (SOA) module using wire bonds and bettered them by at least an order of magnitude.

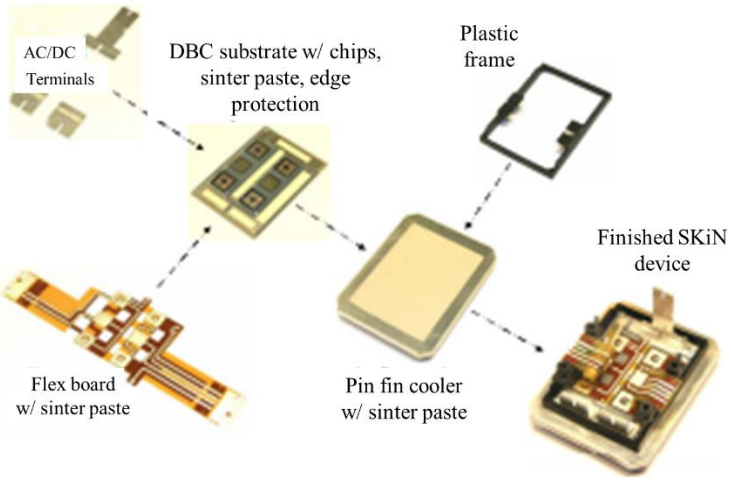


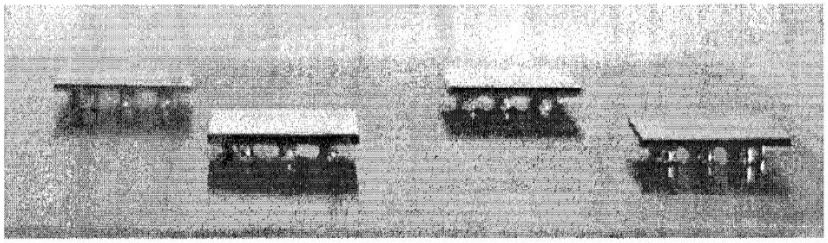
Figure 2.9: Exploded view of the SKiN module from Semikron [51]. Reprint with permission [4062740751911]; Copyright 2011, IEEE.

In 2012, the planar interconnect technology (SiPLIT) module from Siemens was realized, which utilized copper plating over a conformally deposited insulation layer to form interconnections [53]. The vias or openings in the insulating layer formed interconnections to the power die bond pads, and was achieved by the layer structuring process. Because of using planar interconnections, the stray inductance in these power modules showed a 50% decrease as compared to conventional wire bonded modules. The on state resistance showed a 30% decrease.

The thermal resistance offered by this packaging scheme was also lower than an aluminum wire bonded module; and the least thermal resistance was realized by using liquid cooling. From failure analysis results, it could be ascertained that the failure occurred at the junction between the copper interconnect layer and the silicon power device. The onset of failure, however, was much delayed as compared with an aluminum wire bonded module. This was attributed to the fact that copper was a relatively better match to silicon with regard to the CTE as compared to aluminum. Another reason was because this interconnect technology had a larger surface area of contact with the power die and thus the thermomechanical stresses were distributed more uniformly. This was

one of the only studies that published a comprehensive reliability analysis to quantify that this approach met industry standards.

Chip-scale packaging of integrated power modules was explored by Liu et al. [54] in 2001 as a plausible approach to improve the performance of Si IGBT power modules using 3D packaging techniques. Figure 2.10(a) shows a photograph of the solder ball bumped devices flip-chipped onto the substrate. An 8.6% percent voltage overshoot was observed for the flip-chip module as compared with 14% overshoot of a commercially available wire bonded module [Figure 2.10(b)]. The reliability reports suggested that under thermal cycling form 0 °C to 100 °C the resistance of the solder ball interconnects did not degrade after at least 2800 cycles, and that all specimens were functionally intact after 4000 cycles.



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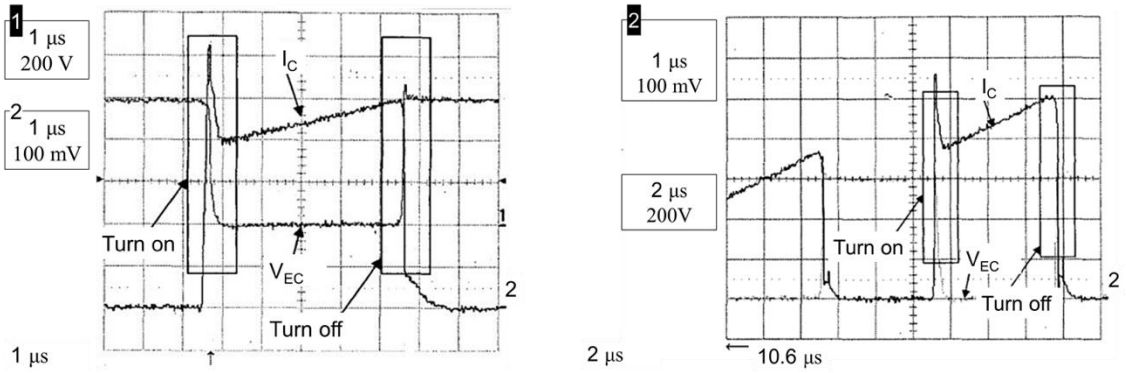

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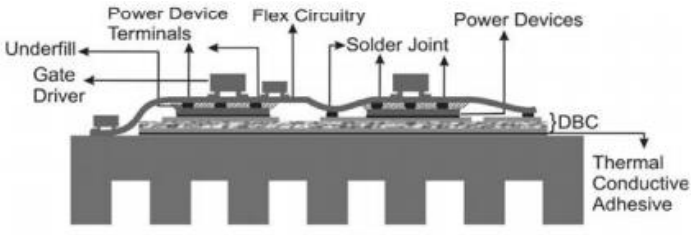
Figure 2.10: Flip-chip integrated power module showing: (a) a photograph of the flip-chipped devices; and (b) the switching waveforms for a module using commercially packaged wire bonded devices (left) and the flip-chip on flex (FCOF) module (right) [54]. Reprint with permission [4062750066013]; Copyright 2001, IEEE.

In 2004, another integrated flip-chip module incorporating a flex-circuit was demonstrated to have 40% lower voltage overshoot and 24% lower losses as a result of implementing wire bondless techniques [55]. Figure 2.11 shows the schematic of the module and the electrical benefits of the flip-chip bonding method over commercially available discrete devices. Although this is a low power module using Si devices, the benefits directly transfer to modules in the higher power range—especially since the voltage and current slew rates encountered will be more severe as the power levels rise.



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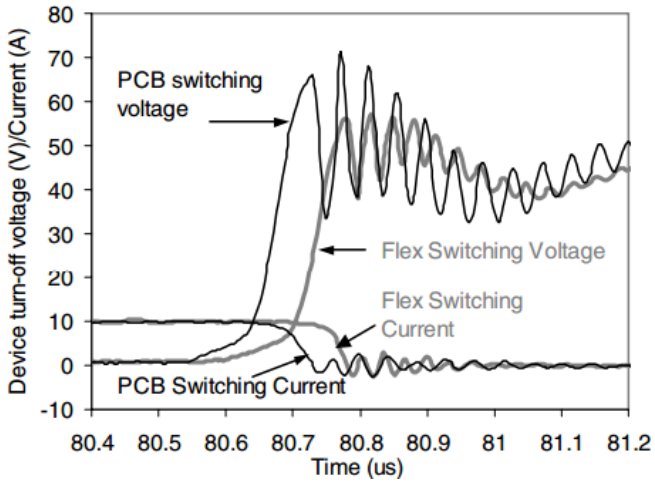

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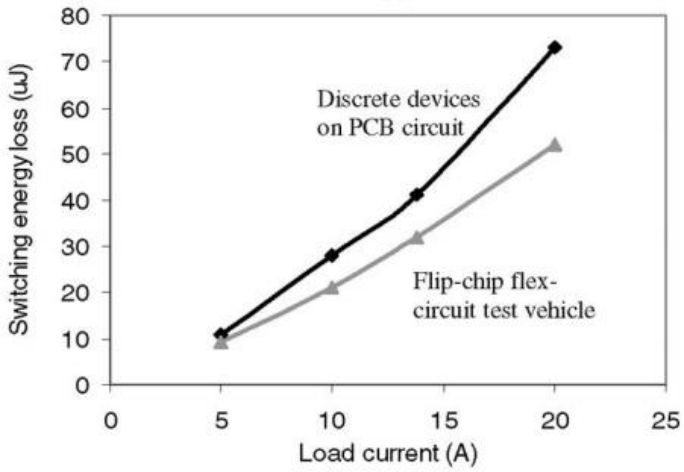

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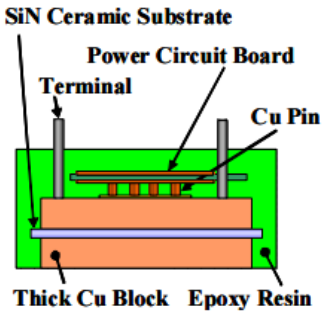
Figure 2.11: Flip-chip on flex package showing (a) a schematic of the package cross-section; (b) the experimental waveforms showing a reduction in the turn-off transients; and (c) the reduction in switching energy losses as a result of wire bondless packaging methods. Reprint with permission [4062750364316]; Copyright 2004, IEEE.

In 2011, Fuji Electric [56] proposed the use of copper pins to connect to the device bond pads instead of wire bonds(Figure 2.12). The copper pins fit into the through-hole connections on the power circuit board. The copper pins were attached to the bond pad of the power device using solder. Connections to the bottom side of the die were made using copper pins as well. There were several advantages of this design apart from the obvious reduction in parasitic circuit elements: the DBC surface did not need patterning and hence the thermal resistance offered by this scheme was significantly lower than conventional methods in which the DBC must be patterned, thus eliminating conductive copper from the DBC surface and compromising thermal conductivity. The module used a rigid epoxy molding compound instead of soft silicone encapsulants normally used in wire bonded modules. It was shown in this study that rigid epoxy induced 35% less strain on the solder connections as compared to using silicones. Another interesting feature that was revealed through reliability testing was that the chief failure mode in this topology was the interfacial joint material, namely the solder. A fin heat sink was used for heat removal.



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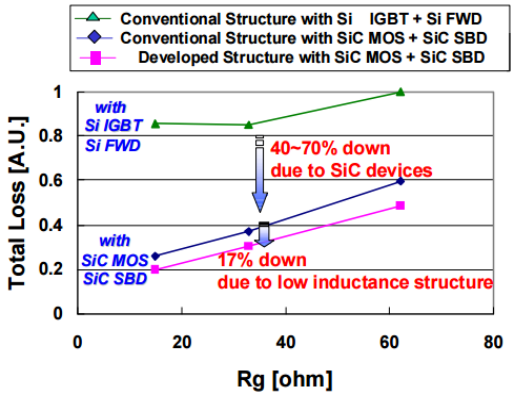

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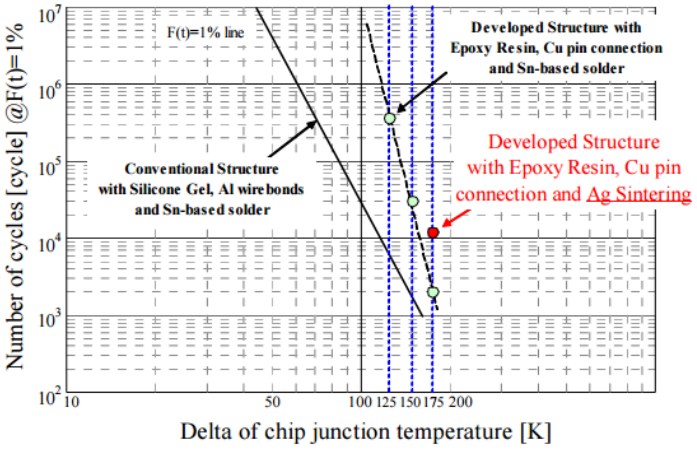


(c)

Figure 2.12: Copper pin interconnected epoxy molded design from Fuji Electric Co., Ltd. Showing: (a) a schematic of the cross-section of the package; (b) loss comparison between the developed structure and wire bonded SiC and Si variants; and (c) reliability curves against junction temperature and interconnect type [56]. Reprint with permission [4062741117252]; Copyright 2012, IEEE.

The metal post interconnected parallel plate structure (MPIPPS) module design was part of the power electronic building block (PEBB) initiative at Virginia Tech [57,58]. A 15 kW inverter was constructed that was capable of switching at 20 kHz, at least twice as fast as the switching speed achieved using a comparable wire bonded device.

Vertical copper posts were used to connect a driver DBC to an underlying DBC populated with power devices. The copper "posts" in this approach were separate from copper "pins" (from Fuji Electric) in that they contacted a larger area of the bond pad. This, the authors claimed provided a larger contact area for thermally induced stress distribution in the copper post. It also reduced current crowding at the junction between the interconnection post and the power device bond pad.

This study also included a detailed survey of materials that were as closely matched in CTE as physically possible in order to reduce thermal stress at the various material interfaces. This was crucial and had a direct impact on module lifetime. Inter-layers like thermal interface materials (TIMs) have also been considered. A poorly engineered interface layer drastically increases the thermal resistance of the module. Minimizing the number of interfaces from the chip to the heat sink had been proposed as a crucial aspect of the PEBB design philosophy.

One encouraging fact was revealed from the MPIPPS module—even a silicon MOSFET could be switched at a frequency of 20 kHz by adopting a wire bondless packaging scheme. This was easily double the frequency of any comparable wire bonded silicon power module of the time. Using the copper posts reduced the parasitic inductance of the interconnects to less than 2 nH, thus enabling silicon technology to be pushed to its theoretical limits.

In addition to the above power modules it is important to mention a few commercial MOSFET modules based on wire bondless technology. Although they were originally designed for low

voltage silicon power MOSFETs, the design principle may serve as a base for the architecture of wire bondless SiC power modules of the future. The BGA MOSFET from Fairchild Semiconductor [59,60], the FlipFET, CopperStrap, and DirectFET [61] from International Rectifier are good examples. Most of these approaches were developed to address the high parasitic source inductance and high package thermal resistance associated with the standard wire bonded SO-8 MOSFET package. Of these, the most benefits were observed for the completely wire bondless and double-side cooled DirectFET, which was reported to improve these parameters by more than 10×.

Another interesting low power silicon module was the DrMOS from Infineon. In this module, the gate drive circuit was integrated within the power module itself. This resulted in extremely low losses and high efficiencies, resulting in an increase in the allowable switching frequency. Not to mention, all this was possible at a much higher power density as a result of a highly integrated assembly. Perhaps some of the gate-driver-in-module approaches for higher power modules bear testimony to the direct adoption of the DrMOS design philosophy.

Press pack modules are among the more popular wire bondless solutions available in the market today. This solution employs mechanical pressure contacts to bond to power devices [62, 63]. Although the target application for this is typically in the MW power range, the benefits of using this design translate directly across all power ranges. This class of modules does away with unreliable metallurgical joints like wire bonds and solder, that are prone to breaking under thermo-mechanical stresses. This type of module also has integrated short circuit protection, and is most commonly used for parallel connections between high power devices. It is not, however, an integrated power module and the gate signals must be applied externally.

Another keen insight into the packaging design problem is presented in [64]. Material interfaces are the Achilles' heel in power modules. The CTE mismatch between the various components in a module lead to the cracking of die attach layers and the lifting of wire bonds from the bond pads. Attachment surfaces with comparatively larger surface areas are more prone to failure by delamination.

In light of these observations, the article cites various efforts aimed at "un-packaging" where a module is stripped of unnecessary material interfaces and components in a bid to eliminate the failure modes associated with the corresponding constituents. This would directly manifest itself as an increase in reliability and module lifetime. This approach sounds ideal and gives the sense of approaching virtually monolithic electronics modules. Concepts involving embedded systems with power die, passives, and interconnections within a single interposer block follow this approach. It is also possible, if desired, to integrate thermal management within the interposer, to compensate for the comparatively lower thermal conductivities of most existing interposer materials. Is this, however, the answer to all problems?

This approach sounds ideal and theoretically solves most issues pertaining to reliability and lifetime. The cost and complexity of building such a module may be prohibitive. Integrating different components together also makes serviceability a challenge. Any kind of rework is difficult to do and may prove to be too expensive to be practical. Therefore, caution must be exercised to maintain a balance between extending the life of a module while keeping an eye on seamless serviceability in case an untimely and unforeseen failure arises.

Research in SiC power modules has redefined our conception of the performance limits of a power electronics module. Researchers continue to demonstrate prototypes capable of functioning

at switching frequencies in the MHz range. SiC modules targeted toward high temperature, on the other hand, have been demonstrated to operate at temperatures above the physical limits of silicon semiconductor technology. These efforts are truly remarkable and herald in a new paradigm in the design and performance of power electronics. However, before these novel technologies are incorporated as part of systems that have a direct impact on our lives, some questions need to be answered with absolute certainty.

Let us consider the case of the high frequency SiC modules first. The information on the reliability analysis of these modules is scarce. The applications benefiting from an increased power density (as a consequence of an increased switching frequency) also require a high degree of reliability. Data centers, solar inverters for the grid, vehicular electronics—a failure to quantify reliability of these systems will have a significant impact on human life and property. It is understood that academic publications and prototypes are targeted toward demonstrating key enabling technologies. However, system reliability must be demonstrated at some level to make a technology transition possible.

As devices are switched at higher frequencies, EMI analysis is imperative. Any failures that may have occurred due to uncontrolled EMI emission must also be reported and studied. Best practices from the printed circuit board (PCB) design world may be utilized to design power modules meeting rigorous EMI specifications.

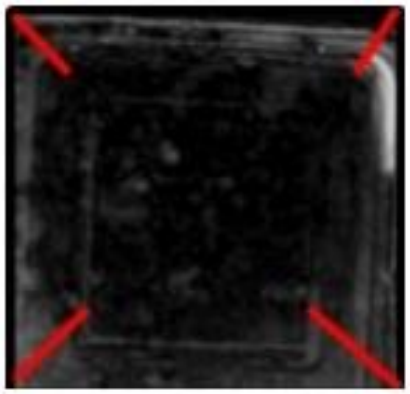
System level reliability analysis is also important for modules targeted to operate at high temperatures as well. In many studies focused on high temperature SiC modules, gate driver and control circuit boards are excluded from the elevated temperature ambient. It is well appreciated that most gate driver ICs and passives that are currently commercially available are rated for

maximum operating temperatures around 125 °C. This limits researchers from demonstrating system level reliability at elevated temperatures. If the high temperature performance of the associated components around the SiC power devices are not improved, it will be difficult to justify the added costs of choosing SiC over Si IGBTs. Today commercially available Si IGBTs are rated for temperatures up to 175 °C. Hence from a strictly "high temperature" viewpoint, there needs to be some fundamental system level technological research to be able to conclusively qualify SiC as superior.

Having said that, the power density improvement offered by SiC cannot be ignored. Even if a SiC power module operates at an identical temperature level as that of a Si power module, it may theoretically operate at a much higher switching frequency and induce little or no increase in the associated switching losses. However, whether the performance gains that accompany this power density enhancement can justify the cost of using SiC technology is uncertain. There are also not many studies that relate the variation of switching losses with a variation in the junction temperature of the device. There are a few studies which suggest that it may not be possible to switch MOSFETs as fast as one might think. STMicroelectronics published an application note showing marked increase in the gate resistance with temperature [6]. This will inhibit fast switching and may even result in higher losses in the drive circuits. Some of the above studies included in the review illustrate the advantages of using SiC technology beyond the shadow of a doubt. However, a degree of skepticism must be maintained to ascertain whether a claimed improvement in system performance would be absolutely impossible without SiC power devices. These devices are part of a larger and more complex system. While a piece-wise validation is an important first step, the need for a high level view of reliability encompassing the system as a whole cannot be disregarded.

Section 2.5. Present Efforts In Wire Bondless Integration of SiC

The realm of wire bondless SiC power MOSFET packaging, where it is capable of a much greater impact, is fairly uncharted. In 2012, researchers at the University of Arkansas developed a 6.5 kV wire bondless power module [65]. This was followed by a similar demonstration of an LTCC-based high temperature, double-sided cooled power module in 2013 [66]. In the 2012 version, solder was used for bonding both sides of the die to patterned DBC substrates on either side. An underfill material was used for relieving thermo-mechanical stresses. Additionally a benzocyclobutene (BCB) coating was used on the top and bottom layers to aid electrical isolation. However, after 260 thermal cycles between -40 °C and 200 °C, the solder layer was found to delaminate from the edges [Figure 2.13(a)]. The 2013 version included a rigid LTCC fixture for mechanical support instead of the underfill material [Figure 2.13(b)]. Also, sintered silver was used as the die interconnection material instead of solder owing to its superior thermo-mechanical properties. This change enabled the new version to operate at higher ambient temperatures. A double-sided cooled approach helped these novel structures maintain satisfactory operation up to 150 °C.



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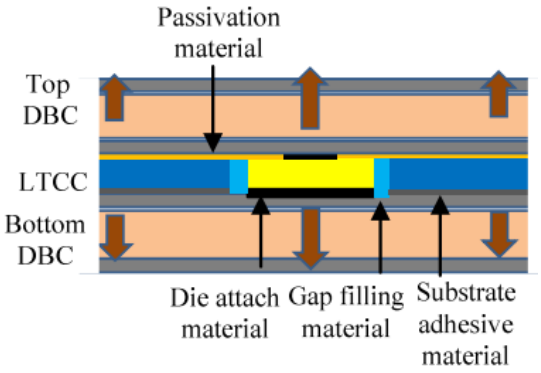


(b)

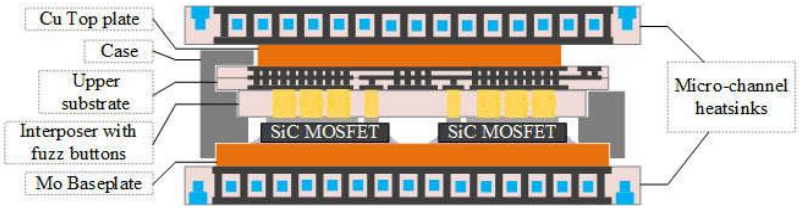
Figure 2.13: Recent wire bondless power module packaging efforts from the University of Arkansas showing: (a) a scanning acoustic microscope (SAM) image of solder delamination in the 2012 module, and (b) a schematic showing the design approach.

Additional LTCC 3D wire bondless power modules are being pursued at the University of Arkansas. One of the main reasons for using LTCC as an interposer material is the excellent CTE match it offers to SiC [67]. The 9K7 material system from Dupont has a near perfect CTE match with SiC. Also, LTCC offers very good electrical isolation and can operate at high temperatures [67]. This is supplemented by the fact that LTCC substrates have been the state-of-the-art for several RF and microwave engineering applications in the past, due to low dielectric losses at high frequencies. They have also been used in actuators and sensors. The LTCC material system has

exhibited good reliability in these applications. All these factors work in favor of LTCC as the choice of material for an interposer in 3D SiC modules.

The 2016 3D stacked module by Dutta and Ang [68] featured two LTCC-based standalone parallel MOSFET modules that were interconnected to form a half bridge. Each standalone module served as a switching position. The half bridge connection was facilitated by using spring loaded metallic connectors, housed in an LTCC fixture. Spring loaded interconnects have been previously used in electronics for high speed I/O with some success. The classical press pack for IGBTs has also demonstrated the viability of pressure contacts as a highly reliable interconnect approach. It will be interesting to observe the test results for high speed and high power SiC MOSFETs. The initial simulation results of the switching characteristics show promise.

The second LTCC based effort came from Zhu et al. [69]. An LTCC interposer was used as a fixture for fuzz button interconnects. There have been several studies corroborating the benefits of using fuzz button interconnects for RF applications [70–73]. Figure 2.14(a) shows a schematic of the cross section of the fuzz button press pack module. Another interesting feature of this module was the presence of an LTCC microchannel heat sink. This enabled the heat dissipation of the MOSFETs to be controlled adequately without adding significant volume to the module. Conductive traces were printed on the microchannel sink for carrying current. Figure 2.14(b) shows a photograph of the LTCC-based heat sink. The fuzz buttons were investigated in software to show that the parasitics were contained to a minimum. Also, the thermal management was tested with a dummy heat load, and performed to expectation. The results had good correlation with the maximum temperature predicted by finite element analysis.



(a)

(b)

Figure 2.14: 3D stacked power module with a fuzz button embedded interposer by Zhu et al. [69]. (a) A schematic showing the cross section of the module; and (b) photographs showing the top and bottom views of the low temperature co-fired ceramic (LTCC) microchannel heat sink.

3D packaging of SiC modules has been embraced by APEI Inc. In some of their more recent efforts they used a stacked gate driver board atop the power stage for low inductance interconnections. However, the parasitic inductance of the wire bonds is still the limiting factor in switching performance. This fact is touched on in a 2015 publication by APEI Inc., where they demonstrated the concept of a wire bondless power module for the very first time [74]. However, a prototype based on the design has not been released yet. The wire bondless power module used the PowerStep connector in favor of wire bonded interconnections. The connector was made of etched copper with a gold finish. Sintered silver, solder, and electrically conductive adhesives were described as possible attachment methods.

The paper presented a detailed finite element analysis of the favorable effects of adopting a wire bondless approach. Aside from the obvious reduction in loop parasitics, it was found that the

thermo-mechanical stresses of the PowerStep connector were much lower than a wire bond at a junction temperature of 200 ℃. This is an important feature considering the fact that one of the major benefits of SiC power devices is their ability to operate efficiently at elevated temperatures. Also, the Joule heating associated with the PowerStep connector was found to be much lower as compared with a wire bond at current loads of 100 A and above. The module was also tailored for a switching frequency of 500 kHz, enabled by the reduction in parasitics.

The modules discussed thus far in this section show great promise to offset the drawbacks associated with wire bonding. The approaches like spring pins and fuzz buttons have already been proven to be beneficial in high speed electronic circuits in the past. With careful design considerations, these benefits should translate to high power modules as well. The success of press pack modules bears testimony to the success of this design philosophy. However, it is important to note that the described approaches are power modules. They must still be routed to a gate driver board to operate in the field. This implies that the parasitic gate inductance of the module is not the sole force to reckon with. The connection to and from the gate driver board, and the board parasitics will also play a key role in determining the behavior of the switching transients and associated EMI behavior. This fact has been highlighted in some of the integrated power modules that have been presented in this paper. Implementing the gate driver "on board" or "in module" was the driving factor behind their success.

Conclusions

SiC devices are fast becoming the semiconductor device of choice in most advanced applications. The demand will only continue to increase as the world becomes more electrified. Having access to power converters that fit within the palm of our hands may give rise to innovations that are yet to be imagined.

The enormous potential that SiC offers as a semiconductor material has not been explored completely. We tend to use performance limiting packaging technologies and restrain the full benefits of SiC technology. Researchers had already encountered the glass ceiling of package performance with silicon devices in the past. Many examples in this paper bear testimony to the adoption of unconventional silicon power packaging solutions in a bid to extricate that much more in terms of thermal and electrical performance. SiC packaging research needs to progress along the same line.

The bottlenecks in state-of-the-art SiC power modules needs to be identified. Investigations need to be conducted to ascertain the part/parts of the package giving rise to these performance limits. This must be followed by innovative redesign in the appropriate direction to push SiC modules further. Interconnect technology is one of the major limiting factors plaguing SiC modules of the present. Wire bonding offers too much parasitic inductance to be able to run SiC power devices at the frequencies it is capable of. Ringing and overshoots due to parasitic loop inductance are only a part of the problem—EMI emissions are a worse consequence which may lead to a catastrophic failure due to a false switching event. Many power electronics research groups around the globe are realizing this, and a there has been a noticeable push in the direction of low inductance SiC package designs in the recent past.

Efforts at the University of Arkansas are focused on providing high-performance alternatives to wire bonding. Approaches involving spring pin interconnects, fixtured fuzz buttons, and solder ball interconnects have proven to be winning choices in high speed, low power electronics applications in the past. The endeavor is to re-engineer these methods to render them applicable to SiC power modules at all power levels. Some of the recent efforts in this direction have been described, and these will help lay the bedrock of a better understanding of these interconnect

technologies as it applies to SiC packaging. Evaluating and weighing these approaches against one another will help establish new standards for packaging technologies suited to the needs of a particular application.

Wire bondless integration will also introduce possibilities of double-sided cooling and 3D integration, once again depending on what the end application would benefit the most from. Compact integration coupled with faster switching frequencies will enable an unprecedented power density. In a rapidly growing electronics market, less is more. Smaller and lighter power electronics may completely change the way we perceive the world.

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CHAPTER 3: The Concept of an Integrated Wire Bondless Power Module

DISCLAIMER: A majority of the content of this chapter has been reported in three previous publications by the author [1—3].

Section 3.1: Problem definition—a case for pursuing 3D wire bondless packaging for SiC devices

3D wire bondless integration of SiC devices has not evolved sufficiently. In fact, a review of the literature provided more instances of 3D wire bondless integration in silicon as compared with SiC. Most of these schemes were implemented to realize one/all of three main benefits—better thermal management through double sided cooling, low-parasitics leading to a reduction in the switching transients, and/or improved reliability. A good number of these proposed solutions have also made it to the market as commercial-of-the-shelf parts. It is not completely understood why there is a comparative lack of research thrust dedicated to developing similar novel architectures for SiC power modules. Thus far, SiC devices have been utilized chiefly as drop-in replacements for silicon power devices. This approach, although grossly inefficient, has nonetheless yielded significant improvements in system performance. SiC is simply outstanding as a semiconductor material as compared with silicon regardless of the drawbacks introduced by the package it is contained in.

Traditionally SiC power modules (and a vast majority of silicon power modules) are commercially available in one of two forms—as discrete devices having a standard footprint (TO-247 and the like) or in the form of a wire bonded module. In either case, the power devices are controlled externally using a gate driver board containing a gate drive chip in packaged form. Thus the electrical current path from the output pad of the gate driver die to the gate pad of the device has to traverse a certain length. The elements contributing the electrical length of the path are:

1. The output wire bond of the gate driver package;

2. The traces of the gate driver printed circuit board (PCB);

3. The power module terminals;

4. The power module trace leading to the gate pad of the module; and

5. The gate wire bond to the gate pad on the device.

This path is depicted in Figure 3.1(a) and manifests itself as a parasitic inductance (and resistance) in the gate loop of a circuit. The package parasitics result in voltage overshoots and conduction losses in switching circuits in the system. Similar parasitics are encountered in the drain-source loop as well. Together, these elements adversely impact the transient behavior of switching circuits.

The presence of stray parasitic inductances also prevents switching power electronics devices at high frequencies. High-frequency switching is an important design goal for any electronic system because it enables the use of physically smaller inductors and capacitors for the filter circuits. The volume of passive devices alone is a chief contributor to total system volume—thermal management being the other. The impact of increasing the switching frequency of the power stage on system volume is well-understood. The properties of the SiC devices themselves contribute favorably to the cause of high-frequency switching—they incur negligible switching losses at high switching frequencies. However, the parasitic inductance imposes a limitation on the extent to which the switching frequency can be increased. The goal of any system design endeavor is to minimize these stray circuit elements as far as possible. 3D integration is proposed in this study as a means to achieve this end by closely integrating the gate driver and power devices

in a wire bondless fashion. This approach was expected to minimize the trace inductances and eliminate the stray inductances associated with wire bonds. Comparable efforts in silicon power electronics have provided favorable results in the past, but the effect on SiC power modules has not been documented convincingly. Even though a slew of innovative 3D packaging solutions have been demonstrated for silicon power modules, the reliability performance of a vast majority of these have not been the focus of the investigations, which brings us to our next issue.

Co-efficient of thermal expansion (CTE) mismatch between the various interfaces in a power module is a leading cause of failure. Contemporary power electronics modules have several interfaces. A schematic describing a conventional SiC power module is shown in Figure 3.1. It can be observed there are many interfaces between dissimilar materials. The interfacial CTE mismatch causes the bonding materials to crack or delaminate under repeated cycles of thermal stress. This eventually leads to module failure as an electrical and/or thermal fault. Managing the CTE mismatch stresses is already a challenge in 2D planar module topologies as shown in Figure 3.1. For 3D topologies with multiple tiers of dissimilar materials, the risks are compounded. Hence the material choices are of prime importance while proposing a novel 3D architecture.

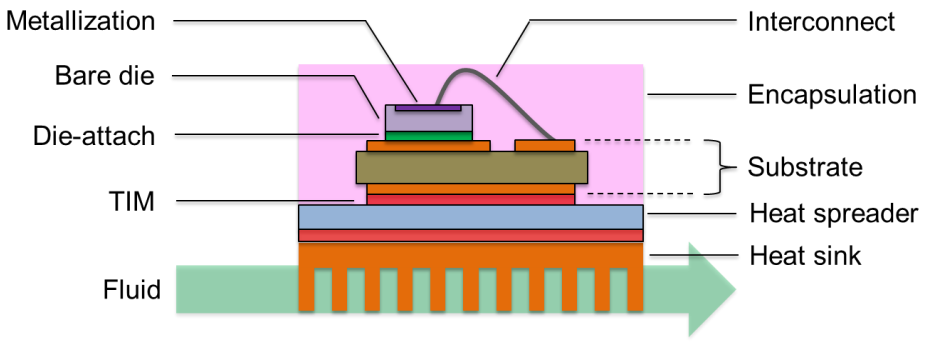


Figure 3.1: A schematic showing a traditional wire-bonded power module.

Heat removal from a 3D stacked architecture is also an area of concern. The power devices generate high amounts of waste heat, and this tends to be concentrated in the central area of the 3D stack.

In this section, the concept of an integrated wire bondless power module is presented. The structure and material choices will be described in *Section 3.2*. The thermal characteristics of the module were evaluated in software to validate the viability of the proposed thermal management scheme, and the results are documented in *Section 3.3*. The mechanical stresses at the interfaces of the module were evaluated under the influence of a thermal load, and this analysis is presented in *Section 3.4*. *Section 3.5* focuses on the extraction of the parasitic elements of the proposed module architecture. The parasitic elements of a wire bonded control module were also evaluated as a base for comparison. Finally, the extracted parasitics were incorporated into circuit simulations to evaluate the transient effects during switching events.

Section 3.2: The Integrated Wire Bondless Power Module (IWPM)

The proposed module provides a highly integrated platform for incorporating power devices, gate drivers, passive circuit elements, and control circuits. Physically closer integration was expected to significantly reduce the area of the critical switching loops in the circuit. This directly translates to a reduction in the parasitic inductance that the high-frequency signals encounter. A simplified schematic of the concept is presented in Figure 3.2. The proposed configuration contains power devices bonded to one side of a central interposer, with gate drivers and passive devices on the opposite side—thus constituting low inductance vertical electrical paths to the power device. A control architecture may be integrated either on the interposer itself or as an external plug-in control board as presented in Figure 3.2.

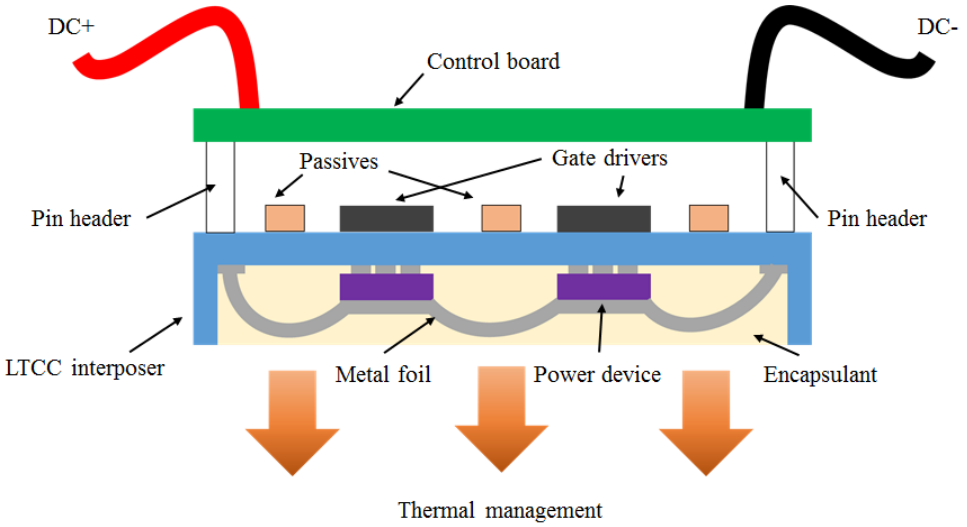


Figure 3.2: A schematic showing the concept of the IWPM.

The central interposer is one of the key features of this proposition. The material of the interposer was chosen to be a low temperature co-fired ceramic (LTCC). These materials have been employed extensively in RF and microwave engineering owing to the scope for a high integration density and low dielectric losses at high frequencies [4]. On account of being ceramics, they can also withstand very high temperatures [5]. Most importantly, the CTE of LTCC materials closely match SiC. For example, the LTCC material selected for this application was GreenTape^{TM} 9K7 from Dupont, with a CTE which differed from SiC by only 10%. This was expected to lower the thermo-mechanical stress on the bonding medium between the interposer and power devices, thus delaying the onset of cracking mechanisms. In addition, the choice of bonding material was sintered silver, which has a proven record for superior reliability and a promise for high temperature operation [6].

Since a commercial SiC power die is a double-sided device, electrical connections have to be provided on both sides of the die. Flip-chip bonding only services the top-side contacts of the device. The connections to the bottom side of the device were achieved using a flexible copper

foil. The foil will be plated with 1-5 µm of silver to facilitate a sintered silver bond to the device pad. A more reliable option would be to use silver foil at some additional expense. The flexible foil will be ideal for matching CTE mismatch stresses, and may be etched into custom shapes to form low-inductance signal paths. Using this foil will also address the issue of bonding die of different thicknesses. The die thickness often differs from manufacturer to manufacturer—and also between separate power devices from the same manufacturer at times. Using a rigid bottom connector would require highly precise etching processes and would not provide as much flexibility under thermal stress.

The metal foil also has the ancillary benefit of serving as a heat spreader due to a high thermal conductivity. As can be observed in Figure 3.2, the LTCC is shaped like a shallow container. The power devices are essentially housed in a shallow cavity that is filled with an encapsulant with a very low CTE (Durapot 810 from Cotronics). The encapsulant serves three major functions: (1) it provides heat spreading within the LTCC cavity, (2) it bolsters the mechanical strength of the flip-chip joints, and (3) it serves as a thermal interface material between the power devices and the heat sink. A heat sink will be bonded to the reverse side of the power devices using Resbond 920 from Cotronics—an alumina filled ceramic hydroset with properties identical to the encapsulant. Thus the entire structure is very well matched in terms of CTE and has the potential of managing thermo-mechanical stresses proficiently.

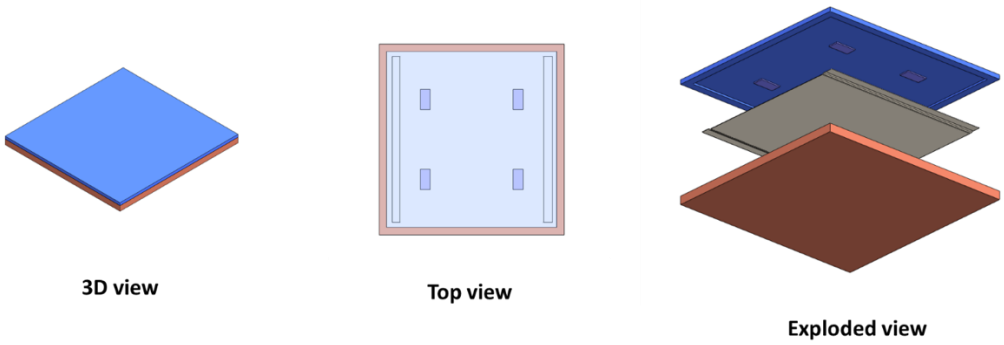
Section 3.3: Thermal analysis

A conventional direct bonded copper (DBC) substrate was not employed in the proposed module architecture. In the conventional power module shown in Figure 3.1, the thermal path has to traverse the top DBC copper layer, the alumina layer, the bottom DBC copper layer, and a thermal interface material to reach the heat sink. In contrast, the thermal path offered by the

proposed IWPM has to traverse through the thin copper foil and encapsulation material only. The voltage isolation offered by the ceramic-based materials in questions are rated at 270 V/mil. The switches selected for this study have a maximum voltage rating of 1.2 kV, and hence the maximum DC bus voltage for this module should be limited to at most 1 kV. This would require a thickness of passivation thickness of about 94 μm between the electrically hot metal foil and the surface of the heat sink. This translates to a shorter thermal path as compared with a conventional wire bonded module.

To verify these findings, a finite-element simulation was conducted. The simulation model is shown in Figure 3.3(a). The footprint of the module measures 3.03 in × 2.95 in and is 0.19 in thick. It must be noted that these were the nominal dimensions of the interposer and power stage only. The final dimensions of the module will be dictated by the volume of the passives and thermal management. In the model, the interposer has been rendered transparent to show the four power devices flip-chip bonded to the bottom surface. Two of the four power devices are assumed to be in the ON state at given time, representing the switching pattern in an H-bridge topology. The ON-state power devices were assumed to dissipate 15 W of heat per chip. The ambient temperature was assume to be 300 K and the thermal resistance of the heat sink itself was assigned as 1 K/W. This corresponds to a very standard specification for a fan-cooled heat sink. High-performance heat sinks with much lower thermal resistance may be used for high current applications with no change in the module architecture. Figure 3.3(b) shows the thermal profile of the IWPM. The ON-state power devices are the hot-spots in the module with a maximum temperature of 74.82 ºC, but the temperature variation across the entire module is only 20 ºC. This prevents localized heating at the location of the power devices and bears testimony to good heat spreading. This heat spreading occurs chiefly due to the presence of the metal foil bonded to the bottom side of the

power devices. This was clearly observable when the thermal profile was plotted on the metal foil alone, and is also shown in Figure 3.3(b). In the absence of the metal foil, the peak die temperature was found to increase by 32.6% to 100 ºC with highly localized hot-spots [Figure 3.3(c)]. The temperature difference across the module was found to be nearly 50 ºC. The thickness of the metal foil used for this simulation was 4 mils, but can be tailored to meet current carrying requirements.



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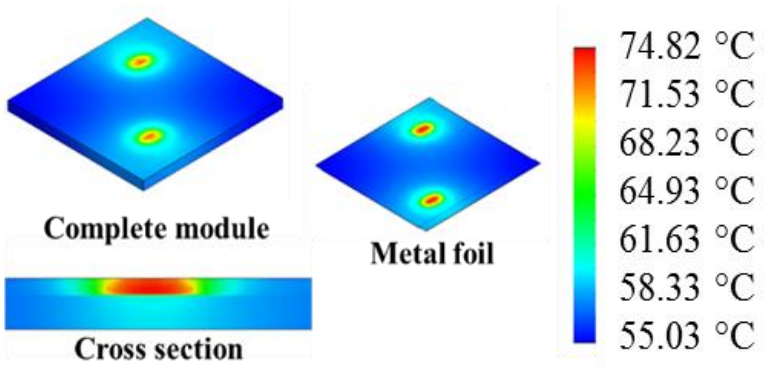

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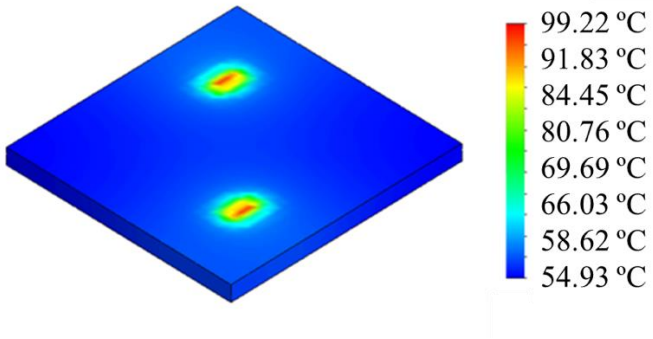


(c)

Figure 3.3: (a) The simulation model for the IWPM, (b) the thermal profile of the IWPM with the metal foil, (c) the thermal profile of the IWPM without the metal foil.

The interposer material has a thermal conductivity of only 4.6 W/mK. Hence, it does not actively provide any thermal relief. Fortunately, this situation can be easily remedied by providing

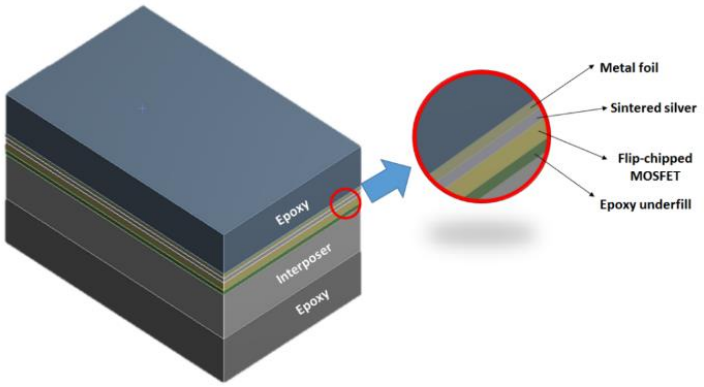
thermal through-vias around anticipated hot spots in the module. This is standard procedure in LTCC technology [6]. The heat spreading can also be supplemented by embedding heat spreaders within the volume of the LTCC interposer, also a well-known aspect of the LTCC manufacturing process [7]. Such additional features were omitted from this study to be able to obtain a worst case estimate of the thermal performance of the conceived module topology.

Section 3.3: Mechanical analysis under thermal stress

As mentioned before, CTE matching between the individual components of the system is the primary requirement to be able to design for reliability. In the proposed IWPM design, the CTE of SiC is 4 ppm/ ºC and that of the LTCC interposer is 4.3 ppm/ ºC. The mechanical deformations of these materials will be very similar under thermal stress. In addition, the material used to bond these devices—sintered silver—is well-known for its proficient handling of thermo-mechanical stress. The flexible metal foil was also expected to conform well to thermal stress as compared with a rigid bottom substrate. The fact that the electronics assembly is encapsulated also aids in distributing the mechanical stress under thermal loading. To verify these assertions a FEM model of the material stack was constructed and is shown in Figure 3.4(a). The model for the power device used for the simulation was constructed with reference to the 1200V-rated CPM2-1200-0025B SiC MOSFET from Wolfspeed. The modeled section only comprised of a die-sized area measuring 6.44 mm × 4.04 mm. This reduced approach reduces the computation time and enhances the accuracy of the results by allowing for ultrafine meshing.

A transient thermal load of 80 ºC was applied to all the components of the model for 1 second to replicate a thermal shock. Figure 3.4(b) shows a map of the Von-Mises stress on the flip-chip sintered silver joints. The maximum stress was found to be concentrated at the edges of the joint, and this is in direct correlation with the fact that cracking mechanisms in die attach layers originate

at the edges. The maximum Von-Mises stress on the sintered silver bonds was found to be about 52 MPa. This observation validated the initial assumption that the thermo-mechanical stress can be significantly reduced by choosing CTE-matched materials. One of the areas of concern in the module was the interface between the metal foil and the power device. The CTE of copper, for example, is about 17 ppm/ ºC—and this significant mismatch with SiC was expected to result in a very high thermal stress. Owing to the flexibility and thinness of the foil, and the fact that sintered silver was used as the die attach material, the maximum stress along this interface was found to be about 83 MPa [Figure 3.4(c)]. This low stress despite the CTE mismatch may also be attributed, in part, to the presence of the encapsulation material which successfully arrested excessive structural deformations.



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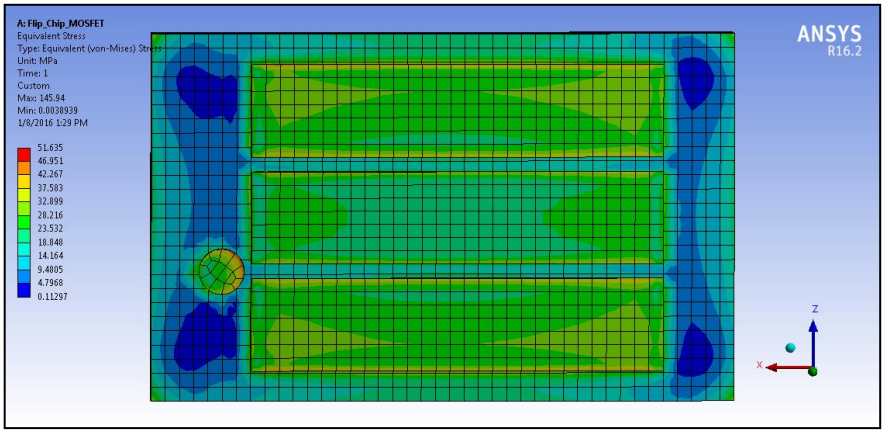

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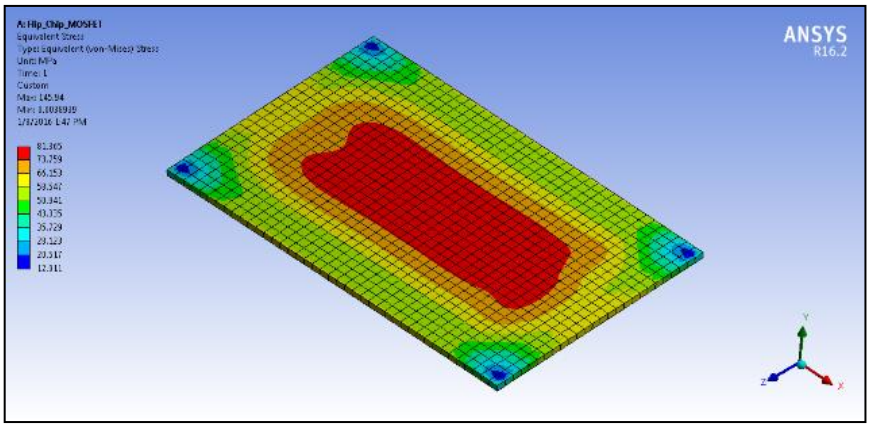


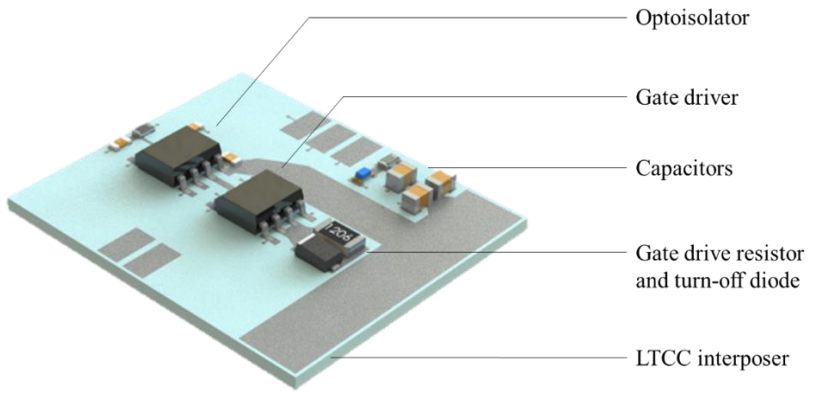
(c)

Figure 3.4: (a) the simulation model for the IWPM, the equivalent (Von-Mises) stress distribution on (b) the flip-chip bonds, and (c) the surface of the metal foil.

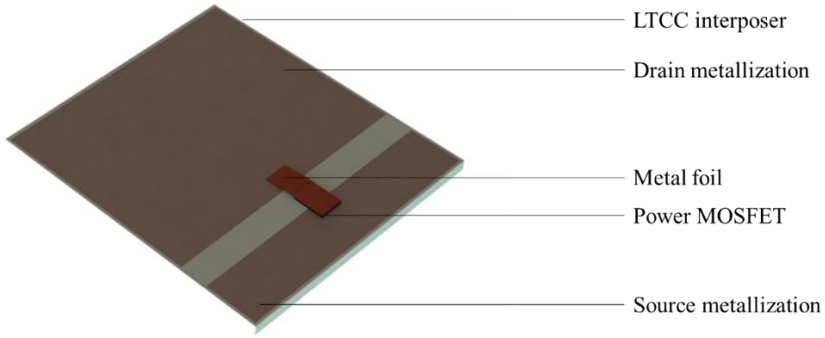
Section 3.4: Electrical analysis of the IWPM

For the electrical analysis, a single switch position was considered, the goal of the simulation was to evaluate the parasitics offered by the flip chip interconnections and contrast it with the parasitic elements offered by wire bonds. A double-pulse test circuit was then constructed in software, where the package parasitics of the respective modules were accounted for.

Figure 3.5 shows a rendering of the simulation model used for the parasitic analysis. The module contains a central LTCC interposer with an opto-isolator, gate driver, and passives on the top surface [Figure 3.5(a)]. The power device, a typical SiC MOSFET, was flip-chip bonded to the bottom layer. The drain pad of the device was bonded to the drain plane of the interposer using a 4 mil thick flexible copper foil [Figure 3.5(b)]. Figure 3.5(c) shows a zoomed-in top view of the gate drive path. The interposer is hidden from view to show the gate driver resistor (and turn-off diode), and the top side of the MOSFET. The output pad of the gate resistor is indicated with a red dotted rectangle. An electrically conductive via of 20 mil diameter connects this pad to the gate pad on the bottom side of the interposer, to which the gate pad of the device is bonded. The via diameter was selected to provide maximum coverage for the device gate pad to ensure the minimum parasitic inductance. A Kelvin sense trace was also provide to facilitate a low-inductance return path for the gate signal.



(a)



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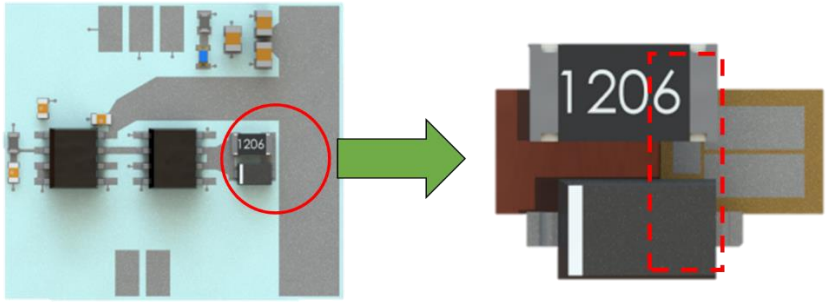
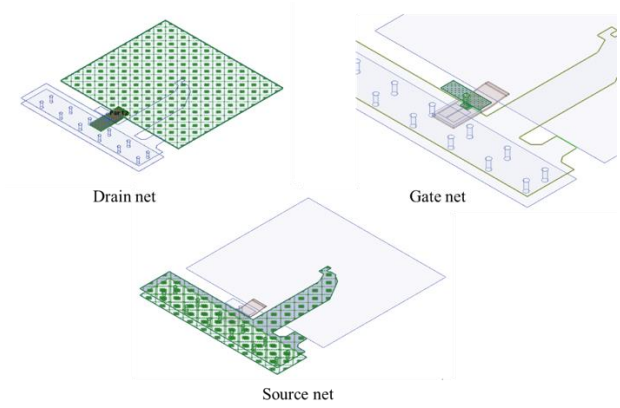


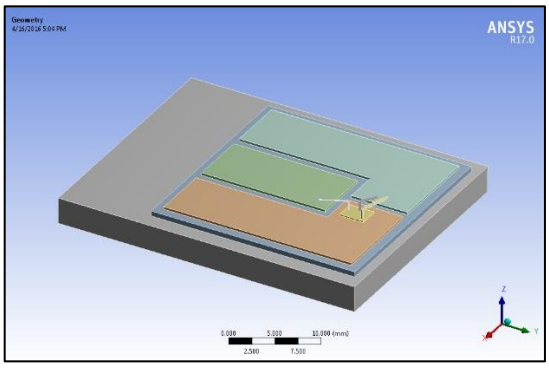
(c)

Figure 3.5: The electrical model of the IWPM for a single switch position showing (a) the top view, (b) the bottom view, and (c) a representation of the position of chip with respect to the gate driver output.

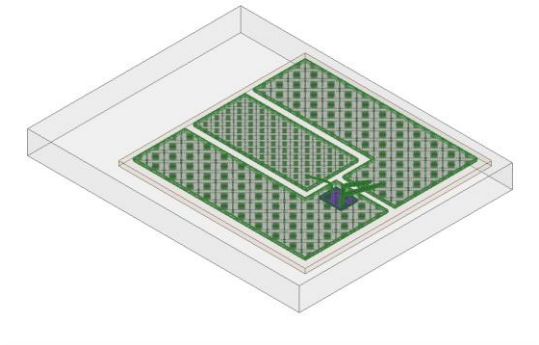
A simplified version of the above model was imported into ANSYS Q3D to estimate the electrical parasitic elements. The IC packages and surface mount passives were omitted to facilitate the meshing process. The signal nets of the simplified model in ANSYS is shown in Figure 3.6(a). To provide a baseline for comparison to the state-of-art, a wire bonded control module was also modeled. Figure 3.6(b) shows the Q3D model of the wire bonded module.



(a)



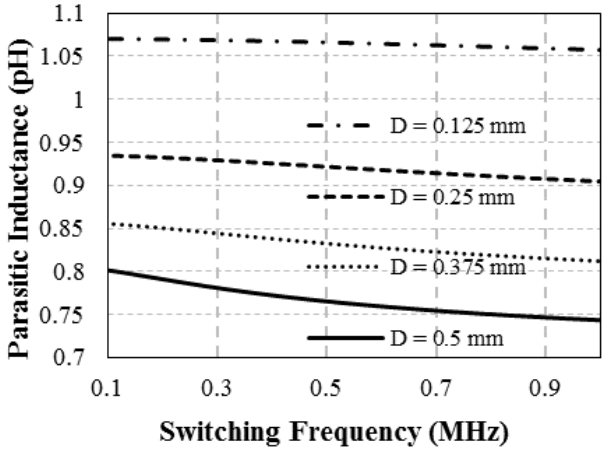
(b)



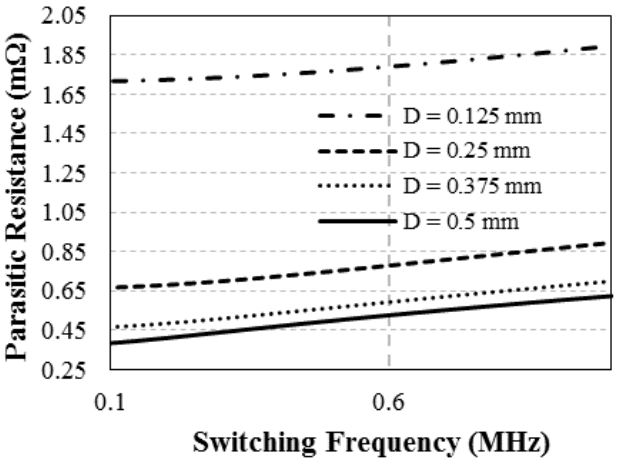
(c)

Figure 3.6: (a) The simplified ANSYS Q3D model of the single-switch IWPM showing the signal nets for the gate drain and source, (b) ANSYS Q3D model of a wire bonded control module consisting of a single switch, and (c) the signal nets of the same.

Even before simulating the inductances of the critical switching loops in the module, the gate via diameter was optimized across a frequency range of 100 kHz to 1 MHz. It was found that a via covering the maximum area on the gate pad presented minimum parasitics. These results are presented in Figure 3.7: Parametric sweeps of the via diameter versus the (a) parasitic inductance and (b) parasitic resistance, as a function of frequency.



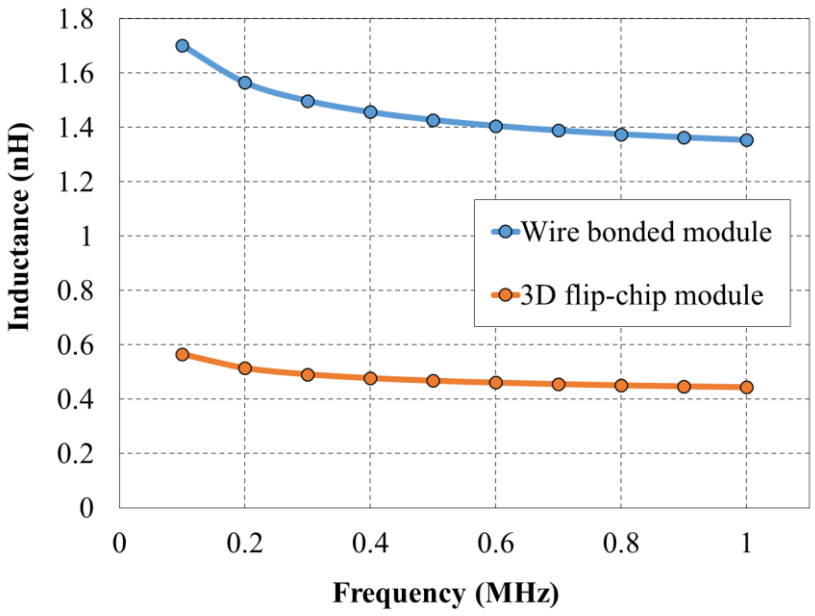
(a)



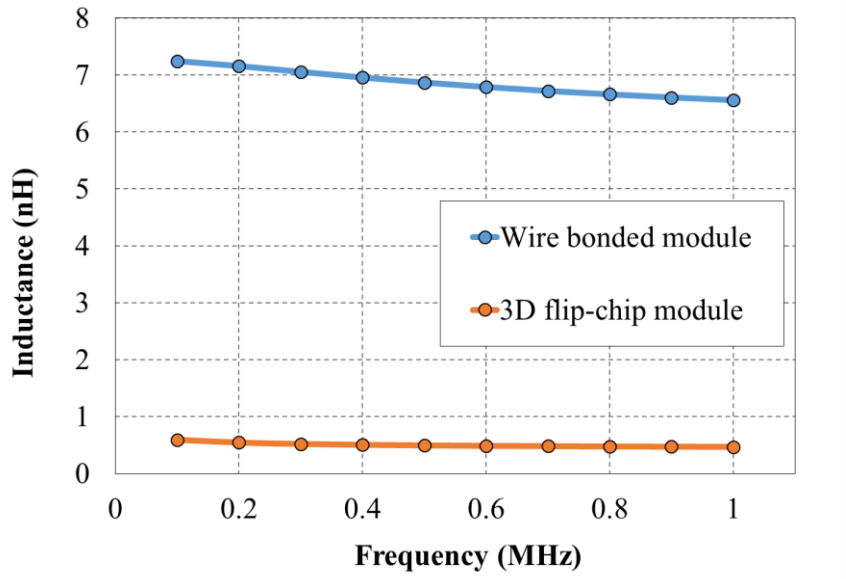
(b)

Figure 3.7: Parametric sweeps of the via diameter versus the (a) parasitic inductance and (b) parasitic resistance, as a function of frequency.

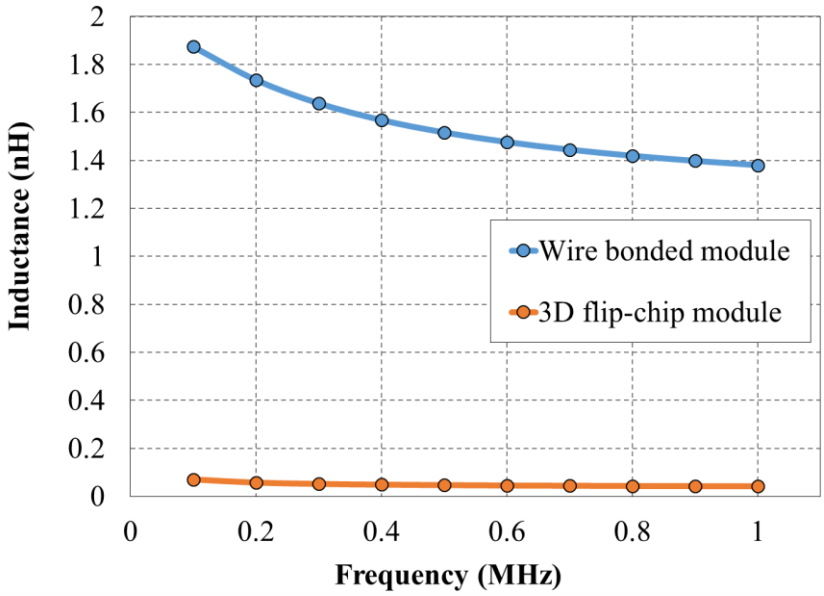
The diameter of the gate via was chosen as 20 mil (to comply with the standard LTCC punch tool bit size) and kept fixed throughout the remaining simulations based on the above findings. The results of the simulations for the power-loop and gate-loop are presented in the graphs shown in Figure 3.8. For the above models, a frequency sweep was defined and ranged from 100 kHz to 1 MHz. The step size for the analysis was chosen as 100 kHz. In general the parasitic elements associated with the 3D flip-chip module were found to be much lower as compared with their wire-bonded counterparts. In addition to the self-inductances of the power-loop and gate-loop, the mutual inductance between the gate and source was also simulated for the two modules. The mutual inductance manifests itself in series with the source self-inductance in a low-side power MOSFET. Even if a Kelvin connection is used for the return path for the gate signal, the gate-source mutual inductance must be included while evaluating the total gate-loop inductance. Similarly the total power loop inductance must include the mutual inductance of the gate-source in addition to the self-inductances of the drain and source paths.



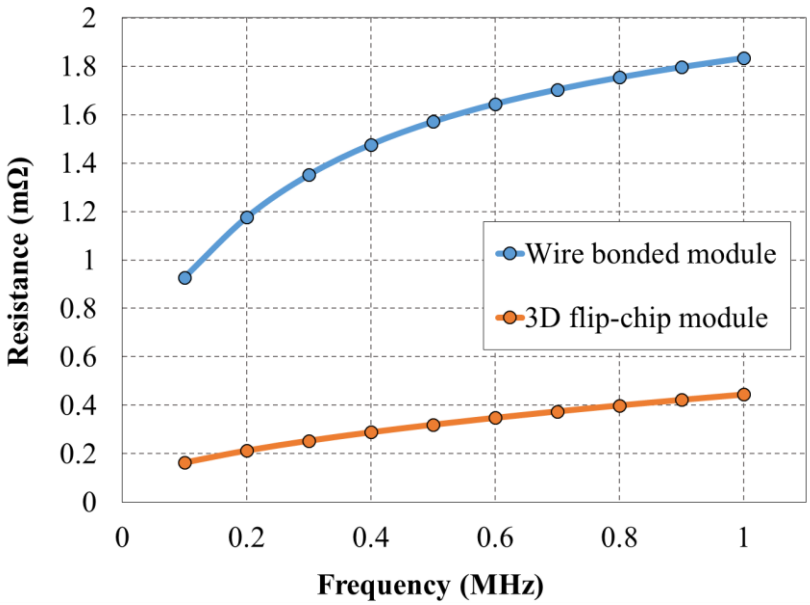
(a)


Inductance (nH)
8
7
6
5
4
3
2
1
0
0
0.2
0.4
0.6
0.8
1
Frequency (MHz)
Wire bonded module
3D flip-chip module

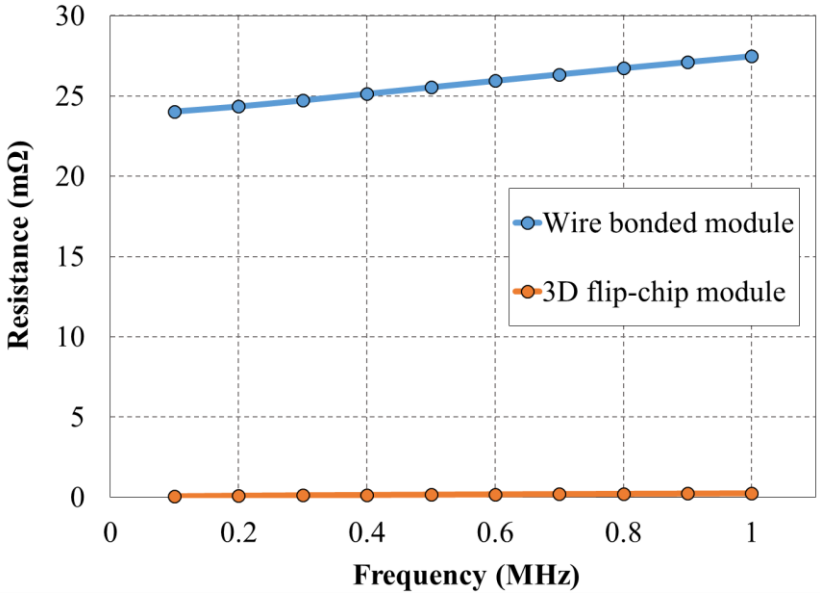
(b)


Inductance (nH)
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
0.2
0.4
0.6
0.8
1
Frequency (MHz)
Wire bonded module
3D flip-chip module

(c)



(d)



(e)

Figure 3.8: Plots showing (a) the power-loop parasitic inductance of the two modules, (b) the gate-loop parasitic inductance of the two modules, (c) the mutual inductance between the gate-source terminals of the two modules, (d) the power-loop parasitic resistance of the two modules, and (e) the gate-loop parasitic resistance of the two modules as a function of frequency.

Conclusions and concerns moving forward with the LTCC platform

Wire bondless integration provides a significant reduction in the parasitics in switching circuits. A part of this study investigates this in the case of a novel LTCC-based power module with an integrated gate driver. Close integration via a 3D topology coupled with wire bondless interconnections, provides ultralow inductance paths to the circulating currents. The proposed module is unique however, in the way that it also minimizes the thermo-mechanical stress in the interconnect layers between the SiC power devices and the interposer. Low mechanical stresses at elevated temperatures will ensure a delay in the onset of failure in the module.

This benefit was enabled by using a CTE-matched LTCC interposer for routing interconnections to and from the circuit components. LTCC materials are capable of achieving a very high interconnection density coupled with high voltage isolation. From an initial evaluation, the proposed module seems to be a reasonable way forward for 3D integrated modules with SiC power devices. However, there are some concerns.

One of the issues for implementing the proposed approach is bonding to LTCC with sintered silver. Solderable LTCC metallization schemes are well-known, but there is no evidence of using sintered silver to bond to LTCC metallization. Sintered silver is preferable to solder due its superior properties and high-temperature capability. Also, sintered silver paste readily tends to extrude and smudge outside the intended bonding area. Using sintered silver in paste form is an unviable proposition for bonding the top side gate and source pads of a SiC power MOSFET for instance. It would be virtually impossible to prevent an electrical short between these closely spaced pads. A solution for this issue has been investigated and is addressed in Chapter 4.

The chief concern, however, is the electrical conductivity of LTCC metallization. The LTCC process employs sintered thick-film metallization. This is essentially an agglomerate of metallic particles. The conductivity of these materials is much lower than the thick copper layers used in power modules and printed circuit boards (PCBs). For high-current operation, this will result in undesirable voltage drops across traces. The Joule heating loss under high current is also another concern. One way to remedy the situation is to use thick-copper plating for the high current traces and planes. Although this seems straight forward, incorporating this process into the LTCC process flow is not trivial. This is especially true for the internal layers which are co-fired with the green tape.

Highly conductive metallization schemes need to be developed for LTCC technology if the proposed IWPM can be truly realized as a viable replacement for existing power module technologies. However, the concept of 3D wire bondless SiC power electronics is still a potential game-changer, but perhaps LTCC is not a mature platform for realizing this yet. In the meantime, there is a need for alternative creative solutions, which can achieve the same end using known-good manufacturing practices. A detailed description of an alternative approach and its demonstration constitutes the crux of the discussion presented in Chapters 5-7.

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CHAPTER 4: The Sintered Silver Preform

DISCLAIMER: The content of this chapter has been the subject of two previous publications and an invention disclosure by the author [1 – 3].

The work described in this chapter is targeted chiefly toward enabling a novel interconnection scheme for the bonding of commercially available SiC power devices using sintered silver. A commercially available bare die SiC power device is a vertical device with electrical contacts on either side of the die. Even before a vertical bonding scheme can be devised, the mode of interconnection needs to be determined. As discussed in Chapter 2, some of the chief modes of 3D interconnections for vertical devices are:

1. Direct solder layer on both surfaces
2. Copper pins/posts or fuzz buttons/spring loaded pins on top pads and solder layer on bottom pad.
3. Solder spheres on the top pads and a solder layer on the bottom pad.

There are two major issues with the above approaches. Firstly, using solder imposes a maximum temperature limit on the system which is far below the allowable temperature limit for SiC electronics. Soldered modules will struggle to provide satisfactory performance upwards of 250 ºC. In addition to mechanical concerns, the formation of intermetallic compounds at higher temperatures also compromises the structural integrity of a solder joint. The second concern is the quality of the bond. The success and reliability of such 3D schemes depends greatly on the planarity of the bond structure. If a bond is preferentially skewed toward a certain edge, the narrow edge becomes susceptible to premature cracking. Voiding within the volume of the die-attach layer

is another concern. This is also difficult to control and gives rise to inconsistent reliability. It is for this reason that solder preforms exist and are preferred for precise and void-free die attachment. However, the problem of a limited temperature range remains. As far as the top-side interconnections go, the use of metal posts/pins is not a reliable proposition. The co-efficient of thermal expansion (CTE) of commonly used metals are severely mismatched with SiC, and directly translates to a reliability issue. The most suitable method to address this would be to employ a direct solder layer or solder sphere approach that many studies have pursued, but it would still not address the high temperature limitation.

Sintered silver die attach material has shown great promise as a high-temperature die-attach material in the past. Both pressure-assisted and pressure-less paste compositions and processes have been explored, and these have been found to be greatly superior to solder material. The electrical and thermal conductivity of sintered silver material is much greater than solder. Although the CTE of this material is high, it does not pose a reliability risk. This is due to its porous and sponge-like microstructure, which enables it to absorb CTE mismatch stresses efficiently [1]. Also, once the material has been cured, the melting temperature is ~1000 ºC. This is extremely desirable for high-temperature SiC modules. However, there are several processing challenges related to sintered silver, and the technology is not as mature and easy-to-use as solder.

Let us consider the case of sintered nanosilver paste as an example. Pressure-less sintering of nanosilver paste has gained popularity over earlier formulations with micron-sized silver particles. Due to a nanoscale particle size, the material had enough surface energy to sinter into a silver nanoparticle agglomerate without any application of external pressure. This grew to be a preferred option due to a simpler process flow as compared with sintered microsilver. After dispensing the sintered nanosilver paste and die placement, a manual scrub-in step is required to ensure proper

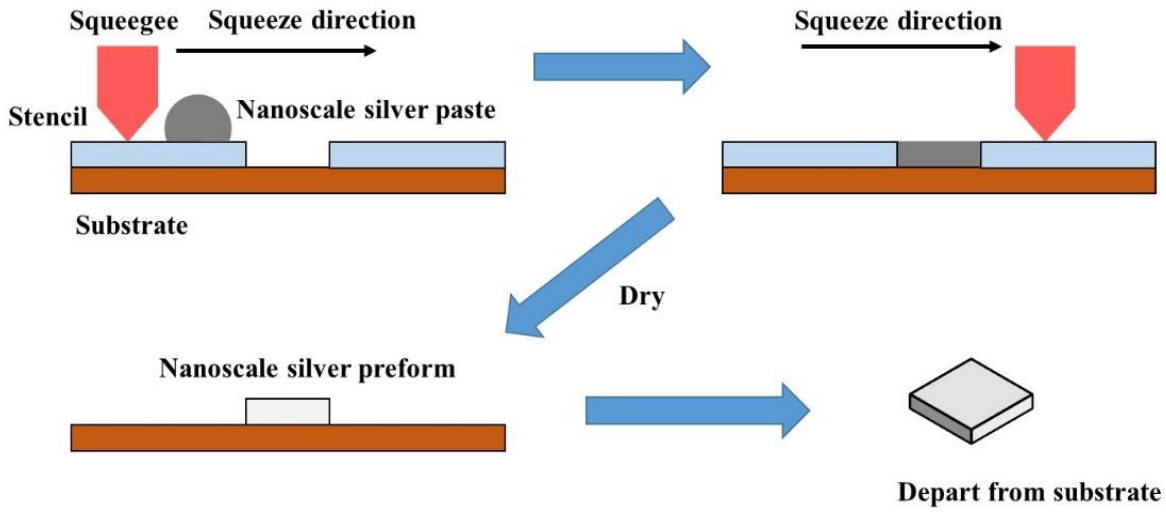
wetting of the die bonding surface. This results in an unpredictable and inconsistent bond line thickness, similar to the skewed bond line issue which was mentioned earlier. Also, if the top pads of a SiC were desired to be bonded using sintered nanosilver in a 3D type module topology, the scrubbing in step would definitively result in an electrical short (bridging) between the closely spaced device pads. There is always some unwanted paste extrusion outside the targeted bonding region while using the conventional sintered silver bonding process.

Inconsistent voiding is another a major issue with sintered nanosilver. Voiding within the volume of the material is related to several factors—the die area, silver loading in the paste, temperature, and sintering time being a few chief contributors. Despite the highly superior properties that sintered nanosilver possesses, the processing and application methods seem to offset the reliability benefits. Sintered silver would be an ideal candidate for 3D chip bonding if there was a way to arrest the paste extrusion and obtain a highly flat, void-free, customizable, and reliable bond line using an easy-to-implement process flow. The focus of this chapter is to introduce a novel solution to address this issue. This potential remedy strives to marry the performance benefits of sintered silver with the practicality of solder preforms. *Section 1* describes a detailed process flow by which a commercially available sintered silver paste formulation was used to manufacture dry nanosilver preforms. The die attachment process will also be described in this section alongside an evaluation of the die bonding strength. The drawbacks of using these dry nanosilver preforms will be discussed to lay the foundation for the introduction of sintered nanosilver preforms. *Section 2* will provide a detailed account of the manufacturing method and die-attach process using sintered silver preforms. An insight into the reliability of this novel technology will also be provided. Multiple preform-bonded sample sets were subjected to thermal shock tests to evaluate the robustness of the preforms, and the results will be discussed.

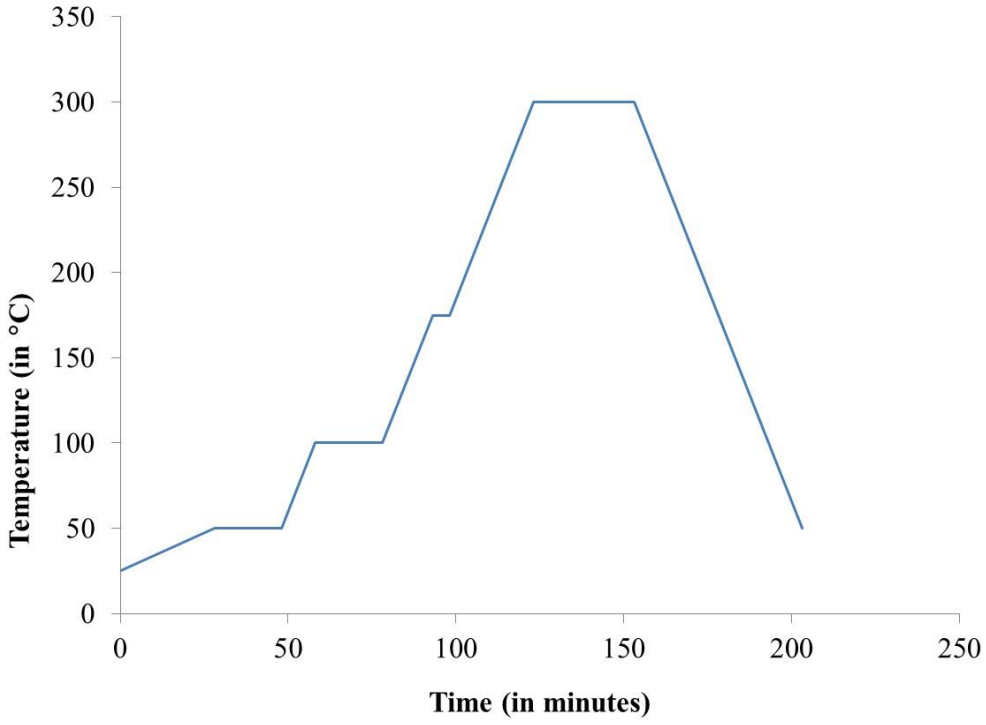
Section 4.1: The Dry Nanosilver Preform

4.1.1: Manufacturing Process

Commercially available sintered silver paste was acquired having the product name "Nanotach®-X" from NBE Tech, LLC, Blacksburg, VA. The datasheet can be found in Appendix A. The average particle size in this particular formulation was about 50 nm for completely pressure-less die attachment. The process flow for the manufacture of sintered silver preforms is represented in the schematic shown in Figure 4.9(a). A predetermined pattern of the wet nanosilver paste was applied to a non-stick substrate through a stencil fashioned out of a 3 mil thick Kapton® sheet. The substrate choices for this experiment varied between a Kapton® film and a bare alumina substrate—and both worked equally well. As long as the silver does not penetrate and bond to the substrate, any selected material may be expected produce identical results. A soft rubber squeegee was used to stencil the paste in a back-and-forth motion several times to ensure a flat and uniform layer of paste. The stencil was then carefully lifted off the substrate, and the sample was dried in an oven according to the temperature profile shown in Figure 4.9(b). If an ultra-low voiding is desired the material may be dried and cured in a vacuum oven. However the process profile may change considerably from the recipe shown in Figure 4.9(b).



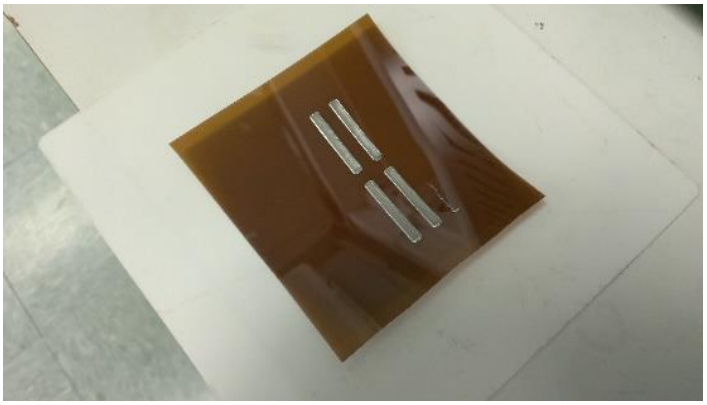
(a)



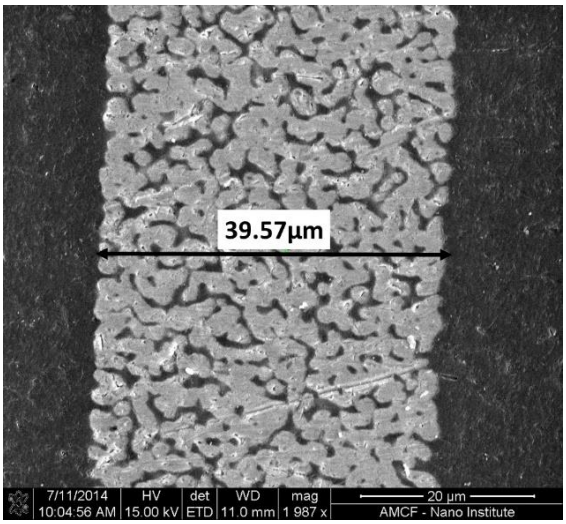
(b)

Figure 4.9: (a) A schematic representing the process flow for the manufacture of sintered silver preforms, and (b) the drying profile used for the same.

The preform was de-bonded using isopropyl alcohol (IPA). A sharp scalpel was used to assist the de-bonding process and care was taken to ensure that the dry preforms did not warp or disintegrate due to improper handling. Figure 4.10(a) shows a photograph of the sintered silver preform strips on the substrate, and a cross-sectional image of a de-bonded preform strip was observed under a scanning electron microscope (SEM). This is shown in Figure 4.10(b) and the nominal thickness of the preform was found to be 40 μm. It must be noted that the preform may be tailored to any specific shape, size, or thickness. The thickness variation may be achieved using stencils of various thicknesses to dispense the initial layer of wet nanosilver paste. According to the manufacturer's recommendation, the initial wet paste layer thickness should be maintained below 50 μm to ensure minimum voiding in the material after curing. To obtain thicker layers thin layers may be printed and dried in several alternate steps involving multiple precisely aligned stenciling processes.



(a)



(b)

Figure 4.10: (a) A photograph showing the dried preforms on a Kapton® film, and (b) a cross-sectional SEM image of the same.

4.1.2: The Die Attachment Process using Dry Nanosilver Preforms

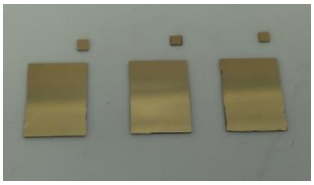
The die-attachment process followed, and to evaluate the performance of the preforms, three different samples were prepared. Both the chip and sample were gold-plated silicon chips. A gold or silver surface finish was mandatory to be able to achieve a bond using sintered silver material. The thickness of the gold layer was 5 µm and the die measured 1.5 mm × 1.5 mm. the die and substrates are shown in Figure 4.11(a). The samples were bonded using three different processes:

Process 1: In this process the sample was prepared exactly per the manufacturer's recommendation. A syringe containing nanosilver paste was mounted on a vortex mixer and mixed for 20 minutes. The paste was inspected to ensure that it appeared homogenous. Additional mixing must be performed in case the paste appears visually inhomogeneous. Any signs of inconsistency essentially means that the silver nanoparticle loading is not uniform throughout the volume of the paste in the syringe. This ensures inconsistencies in the bond line thickness and voiding in the final cured bond. After a thorough mixing process, the paste was stenciled through a die-sized hole in a Kapton® film. The die was carefully placed on this layer of wet paste using a pair of tweezers. Per the manufacturer's recommendation, the die was scrubbed in gently using a sparing amount of manual pressure. The assembly was then sintered in an oven according to the profile shown in Figure 4.11(d). Exposure to ambient air was prescribed as a requirement during the curing process, and hence the oven was not evacuated.

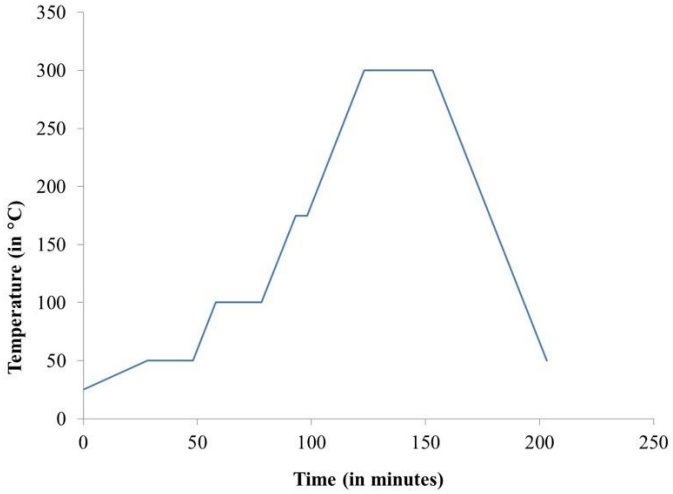
Process 2: The same die and substrate pair was used in this process [Figure 4.11(a)]. However, the sintered silver preform was used as the die-attach material. The bonding surfaces on both the die and the substrate were smeared using a sparing amount of nanosilver paste in order to provide adequate wetting during the bonding process. It was found that proper nanosilver permeation and subsequent bonding could not be achieved in the absence of this wetting medium. Before applying the wet paste, it was thoroughly mixed in a vortex mixer as in Process 1. The nanosilver preform was cut to match the die footprint using a sharp scalpel. The preform was then gently placed on the surface of the wet paste on the substrate. The die was finally placed atop the preform and pushed down using a foam Q-tip with gentle fingertip pressure to ensure proper wetting of all bonding surfaces. In this case the application of pressure at this stage did not run the risk of producing a thin and weak bond line as with Process 1. This was because the preform acted as a

standoff and maintained adequate separation between the die and the substrate. The assembly was sintered in an oven according to the profile shown in Figure 4.11(b).

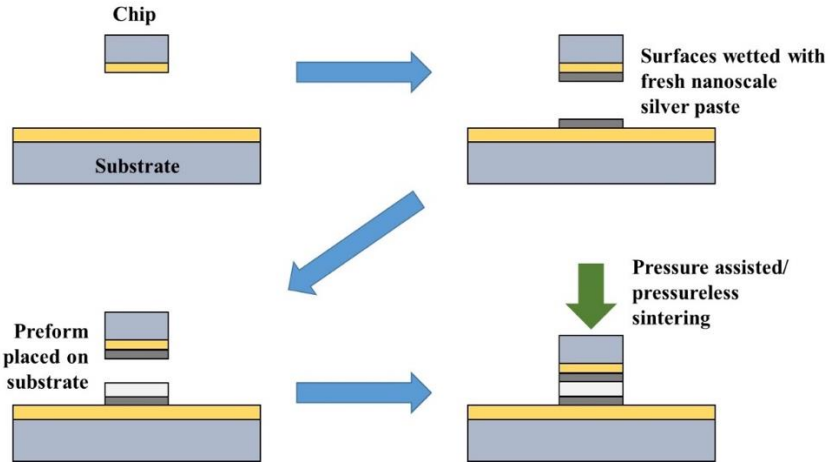
Process 3: A gold-plated silicon chip and substrate were used in this process as well, and they were bonded using a sintered silver preform. However, a pressure of 8 MPa was used during the bonding process. As with Process 2, the substrate and die bonding surfaces were pre-wet with nanoscale silver paste. The paste was mixed thoroughly before application. The sintered preform was cut to match the footprint of the die and placed gently on the surface of the substrate. The chip was placed next and the assembly was sintered in an oven with 8 MPa pressure applied directly on the chip. The sintering profile was the same as the previous two processes, and a schematic representing Process 3 can be seen in Figure 4.11(c). The application of pressure during sintering has found to have a positive impact on the bond quality, especially for large area die [2].



(a)



(b)

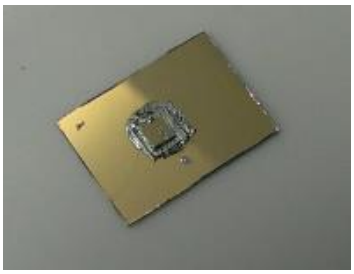


(c)

Figure 4.11: (a) A photograph showing the gold plated die and substrate samples used for the bonding process, (b) the sintering profile used for die attachment, and (c) a schematic outlining the die bonding process.

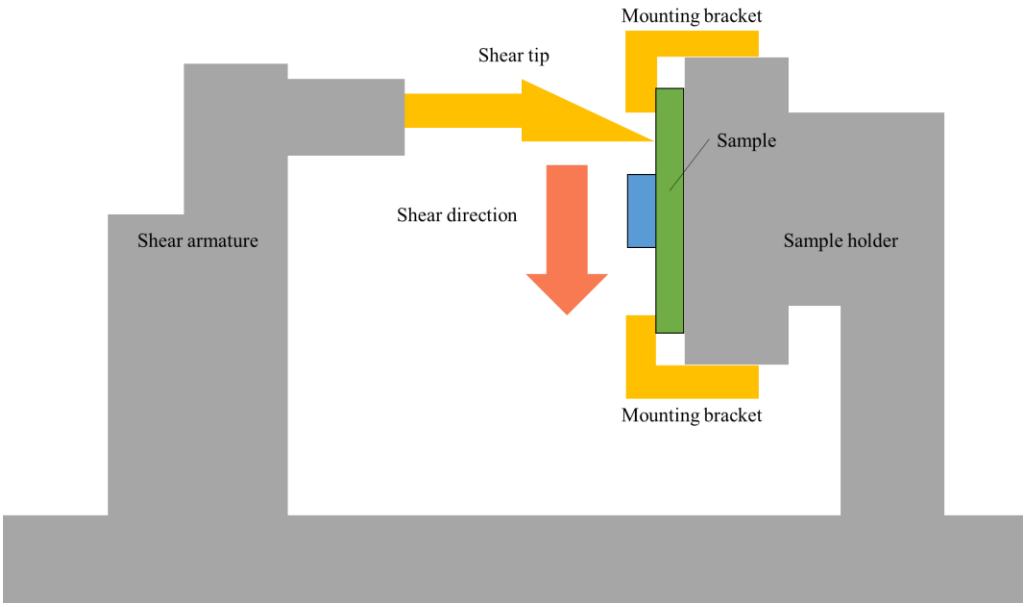
4.1.3: Bonding Strength Evaluation and a Discussion of Results

After curing the samples, they were subject to a die shear test to evaluate the bonding strength. Figure 4.12(a) shows a photograph of the sample subject to Process 3, and Figure 4.12(b) shows the Sebastian 5 die shear tool used for evaluating the bonding strength of the samples fabricated according to the three processes described earlier. The sample was mounted and clamped to the sample holder on the Sebastian 5, while the armature fitted with the shear tip was adjusted to be contacting the edge of the die and parallel to it. This is schematically represented in Figure 4.12(c). Once the force function was enabled, the shear tip applied an incrementally increasing force on the chip until the die was broken. The maximum force prior to the break-point was recorded and displayed through a readout. Figure 4.12(d) shows a comparison of the bonding strength of the samples fabricated according to Processes 1, 2 and 3.



(a)

(b)


Mounting bracket
Shear tip
Sample
Shear direction
Shear armature
Sample holder
Mounting bracket

(c)

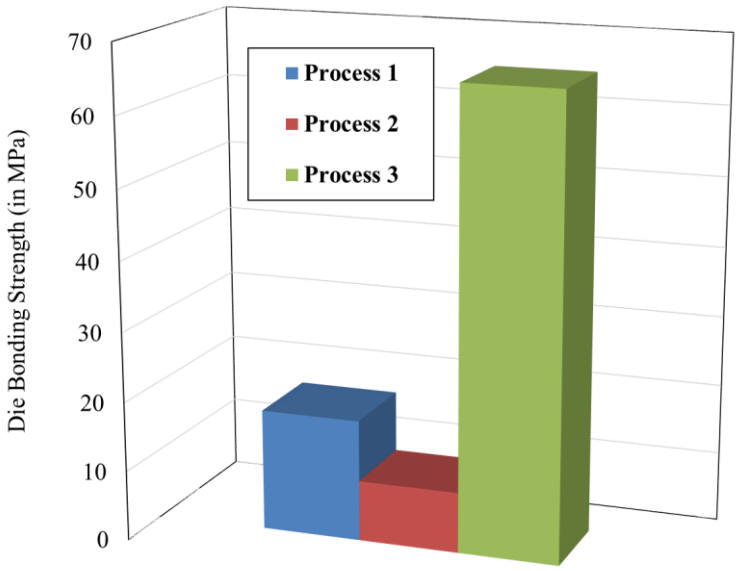
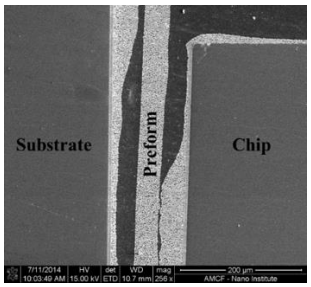


Figure 4.12: A photograph showing a representative sample bonded to the substrate using a sintered silver preform, (b) a photograph showing the Sebastian 5 die shear tool used for bonding strength evaluation, (c) a schematic representing the operation of the Sebastian 5 die shear tool, and (d) a bar graph showing the comparative bonding strength of the three samples.

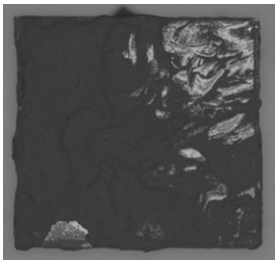
For the sample fabricated using Process 1, the die shear strength was found to be around 17.4 MPa. This agreed well with the values reported in the literature. The second sample showed a very low die bonding strength of 8.72 MPa, which was very uncharacteristic of sintered silver die attach material. The third sample showed a very high bonding strength of 65.4 MPa. This was much higher than any reported values for sintered silver die attach, and 3.75× higher than the sample bonded with sintered silver paste only. The failure analysis of the three samples will presented next.

The failure mode for the sample fabricated according to Process 1 was a break in the middle of the sintered silver joint. This was found to be the typical failure mode in multiple samples fabricated using the conventional sintered silver die-attachment process. The sample manufactured according to Process 2 formed the weakest bond. The reason was clearly apparent once the sample

was cross-sectioned. In the absence of eternal pressure weighing the die down, the wetting was inadequate. During the curing process, the preform may have warped and/or lost contact with the either/both bonding surfaces. Figure 4.13(a) shows the cross-sectional SEM image illustrating this fact. This fact was also echoed upon an examination of the failure surfaces on the die [Figure 4.13(b)] and substrate [Figure 4.13(b)] bonding surfaces for the Process 2 sample. The dark areas on the surface indicate the areas where the sintered silver paste was not able to inter-diffuse and form a bond, while the white areas indicate regions where bond formation was successful. The failure surfaces in the die and the substrate showed that a sintered silver joint could not form successfully across most of the bonding area of the sample. For the sample fabricated according to Process 3, the failure mode was chip cracking. This was the best possible scenario where the bonding strength was not the weakest parameter in the system. A photograph showing the ruptured die after the die shear test is shown in Figure 4.13(d).



(a)



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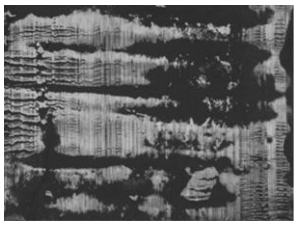

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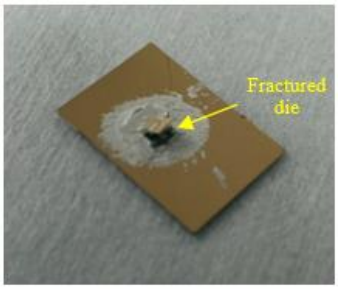
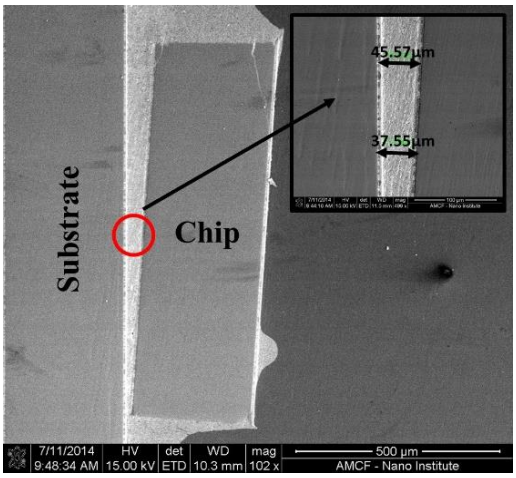


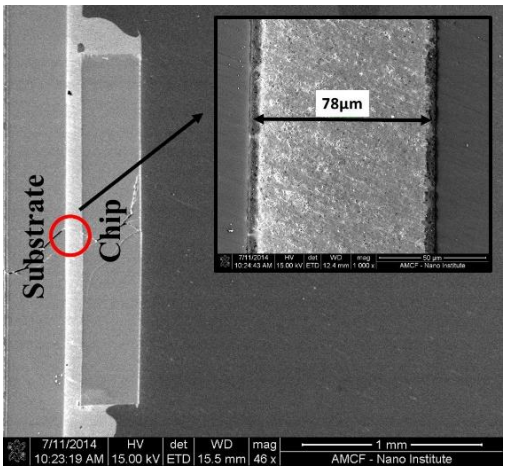
(d)

Figure 4.13: Failure analysis of the sample set showing (a) a cross-sectional SEM illustrating inadequate wetting and contact in the Process 2 sample, (b) an optical microscope image showing the failure surface on the die of the Process 2 sample, (c) an optical microscope image showing the failure surface on the substrate of the Process 2 sample, and (d) a photograph showing die fracture in the sample fabricated according to Process 3.

Another interesting feature contrasting the Process 1 and Process 3 sample bonds is shown in Figure 4.14(a). Due to manual die placement and the recommended scrub-in step, the bond line of the sample in Process 1 was found to be tilted as shown in Figure 4.14(a). This situation is unavoidable in case of manual die placement and pressure-less bonding with sintered nanosilver paste. There is no self planarizing effect due to surface tension like solder paste/preform bonding. The average thickness of the bond line was about 42 μm. In contrast, the bond line of the sample prepared according to Process 3 showed excellent planarity [Figure 4.14(b)]. Also the thickness of the bond was close to 80 μm. The thicker bond line was a possible reason for the higher bonding strength obtained for this sample. The thick and highly planar bond line will provide significant reliability benefits in comparison with samples bonded with the conventional sintered nanosilver process. As mentioned earlier, skewed bond lines are likely to fracture prematurely at the narrower edge.



(a)

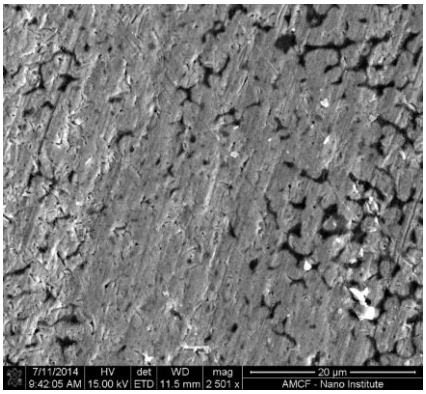


(b)

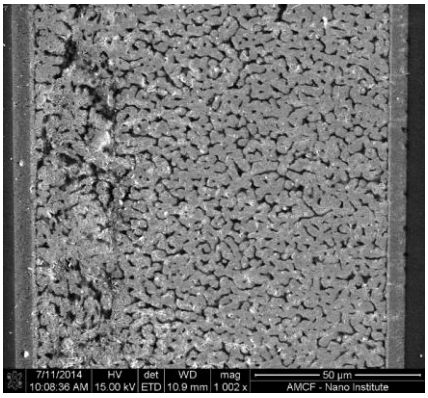
Figure 4.14: SEM image of the bond line of the sample fabricated according to (a) Process 1 and (b) Process 3.

Excessive voiding within the bond line is another major concern in die-attach materials and processes. The microstructure of the samples manufactured according to Processes 1, 2, and 3 were examined under a scanning electron microscope. The results are presented in Figure 4.15. For the Process1 sample, the porosity varied between regions having low/no porosity and regions with much higher porosity. The high porosity areas occurred mainly at the edges of the die. There were also some areas with graded porosity [Figure 4.15(a)], and this may have occurred due to a non-

uniform silver loading between adjacent areas of the bond. This situation was more clearly apparent in the sample prepared according to Process 2 [Figure 4.15(b)]. Due to inadequate wetting and contact, the demarcation between the regions of different porosities was clearly visible. The cross-sectional image of the Process 3 sample, however, showed the least porosity. The degree of porosity was also found to be uniform across the entire bond line. The constant porosity in the preform combined with pressure-assisted bonding seemed to have a positive impact on the microstructure of the bond.



(a)



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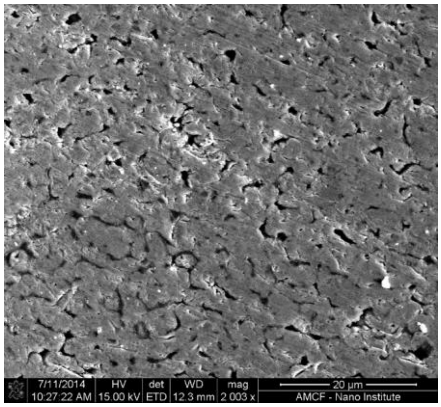


(c)

Figure 4.15: SEM images showing the microstructure of the samples prepared using (a) Process 1, (b) Process 2, and (c) Process 3.

It may be concluded from this study so far that dry nanosilver preforms enable a superior bond quality as compared with bonding using sintered nanosilver paste only. The proposed method yielded a die bonding strength was 3.75× higher than a bond using the conventional sintered nanosilver process. The bond line was highly planar, and did not present a reliability risk that a preferentially skewed bond line presents. The quality of the bond was also found to be much superior to a conventional nanosilver bond as evidenced by a close examination of the respective microstructures under a scanning electron microscope.

One of the greatest advantages of the process was the high degree of customizability. The dry nanosilver preforms may be tailored to fit bond pads of various shapes and sizes, and can produce consistent bond lines of custom thicknesses. The simplicity and consistency of the process makes it highly amenable to high-volume manufacturing. It also helps to arrest the wastage of expensive nanosilver paste in a manufacturing setup. Wastage is inherent in the stenciling/screen-printing processes which are typically employed for paste-based die attach materials.

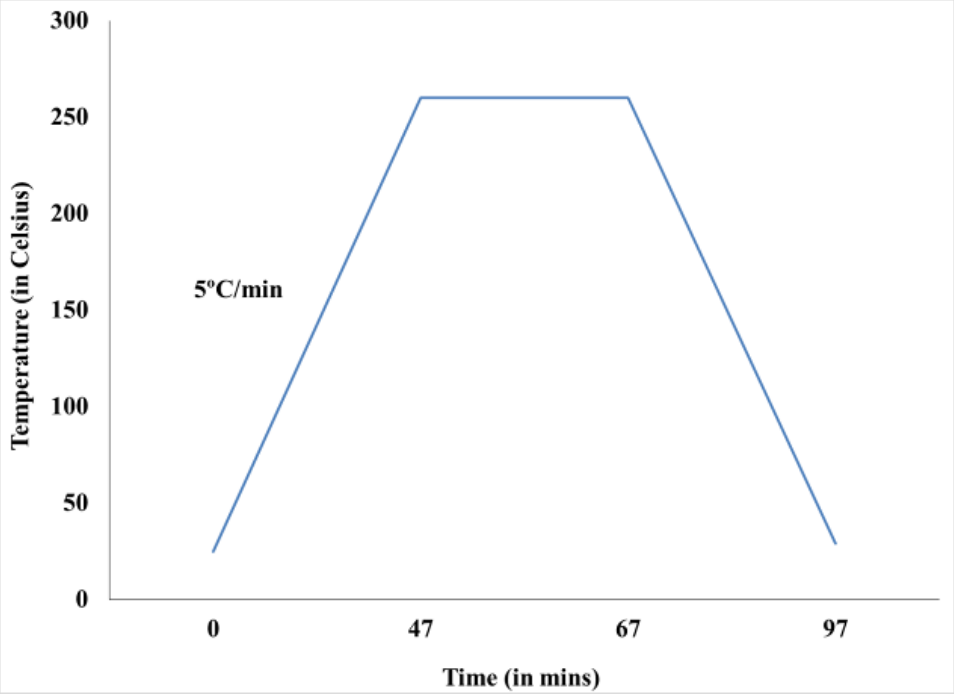
One of the drawbacks of the process was the poor structural integrity of the dry preforms. The user has to be very careful in the de-bonding and subsequent handling of the preforms. It was found that the preforms crumbled and split easily while handling with precision tweezers during the pick-and-place process. Using a vacuum pickup tool improved the situation to an extent, but did not resolve the issue of breakage during the de-bonding process. The robustness of the preform was a much required area of improvement for this technology to be competitive in the market. Another drawback with sintered silver die bonding in general is paste extrusion out of the sides and up the walls of the die. If sintered silver bonding is used for 3D double-sided bonding of power die, this situation may result in an electrical short and/or an electric discharge between the top and bottom

layers. The following section provides a solution to the issues by introducing sintered nanosilver preforms.

Section 4.2: The Sintered Nanosilver Preform

4.2.1: Manufacturing Process

The same commercially available nanosilver paste (Nanotach®-X) from NBE Tech, LLC was used to manufacture the sintered silver preforms as well. The paste was stenciled through a Kapton stencil to a non-stick substrate (Kapton® or alumina for example) as before, and sintered. The approximate preform thickness after a single stencil and cure schedule was 50 µm. A second stenciling and curing step was performed to obtain a final preform thickness of approximately 80 µm. As mentioned in the earlier section, the reason for the two-step stenciling process was to ensure minimum voiding. The sintering profile used for the process is shown in Figure 4.16(a). The die used for the bonding process measured 5 mm × 5 mm in area, but the preforms were undersized to 4 mm × 4 mm. this was to ensure that the there was no paste extrusion out of the side and up the walls of the die during the die placement and sintering process. Once sintered, the preforms were de-bonded from the substrate using 0.01% diluted hydrochloric acid. The de-bonding process was influenced from a similar process described in the literature [3]. The specimens were then baked in an oven at 100 ºC for 15 minutes to remove any residual traces of moisture. Figure 4.16(b) shows a photograph of the de-bonded sintered silver preforms.



(a)

(b)

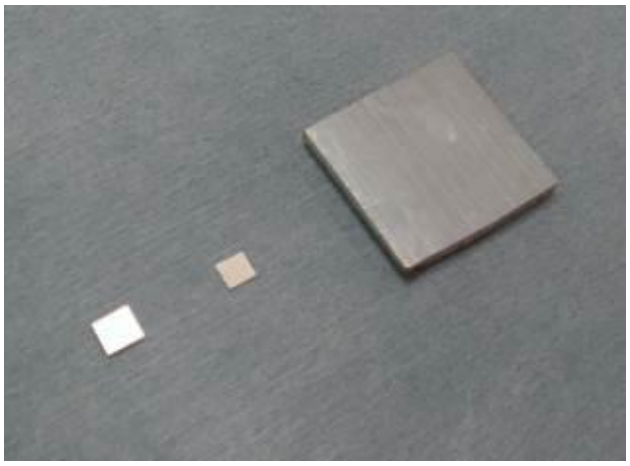
Figure 4.16: (a) The sintering profile used for the manufacture of sintered nanosilver preforms and (b) a photograph showing the sintered silver preforms.

4.2.2: The Die Attachment Process Using Sintered Nanosilver Preforms

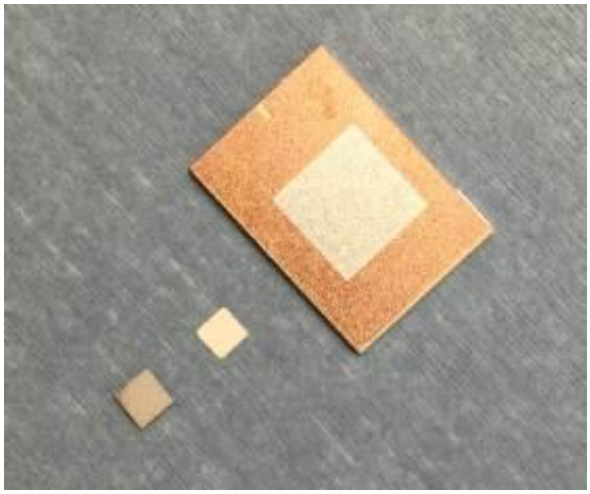
Silver plated dummy die made of silicon were used for the bonding process. The footprint of the dummy die measured 5 mm × 5 mm. A bare silicon wafer was electroplated with 0.8 µm nickel followed by 0.6 µm silver to mimic the metal stack-up of commercially available devices from

CREE Inc. The substrate used for process development was a 1" × 1" piece of copper. The substrate used for the reliability test was a silver-plated Curamik® direct-bonded copper (DBC) substrate from Rogers Corporation.

The bonding surfaces of the die and the substrate were thoroughly cleaned using IPA and blown dry using a nitrogen gun. As before, the bonding surfaces of the die and the substrate were pre-wet by smearing a sparing amount of nanosilver paste. The substrate was placed on the sample stage of a flip-chip bonder and secured by enabling the stage vacuum. The flip-chip bonder was capable of running thermal profiles, and hence accurate placement and sintering could be performed without transferring the sample to an oven. The preform was mounted on the top arm of the flip-chip bonder using a pair of tweezers. The sintered preforms were significantly more robust to handling as compared with the dry silver preforms, and none of the samples disintegrated during de-bonding or subsequent handling. The optical alignment system of the flip-chip bonder was used to precisely place the preform on the pre-wet area on the substrate surface. Die-placement followed, and the assembly was weighed down using a mild pressure of 1.2 MPa. Sintering was performed by running the profile shown in Figure 4.16(a) through the sample stage of the flip-chip bonder using a microcontroller. Figure 4.17(a) shows a photograph of a die, undersized preform, and silver plated copper substrate for the bonding process. Figure 4.17(b) shows the photograph of the die, preform, and DBC substrate used for manufacturing the reliability test samples. A photograph showing the sample on the flip-chip bonder is shown in Figure 4.17(c). The microcontroller and temperature sensor can also be seen as part of the setup. Photographs showing a typical finished sample bonded to a copper substrate can be observed in Figure 4.17(d). The set of samples bonded to the DBC coupons for reliability testing can be seen in Figure 4.17(e).



(a)



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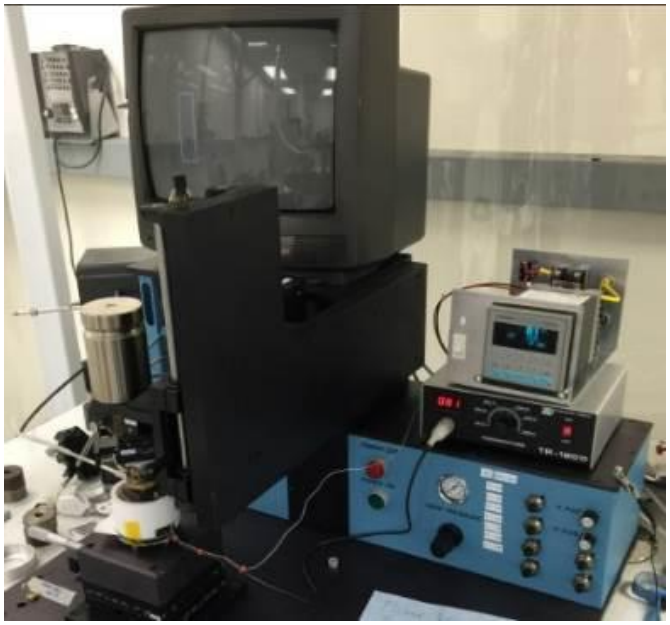

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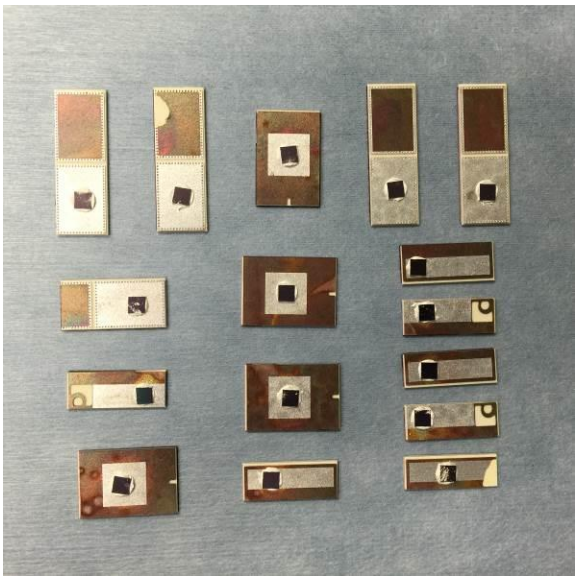


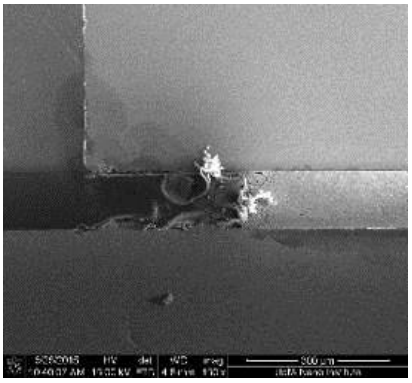
(e)

Figure 4.17: A photograph showing (a) the material set for bonding silicon dummy die to copper substrate, (b) the material set for bonding silicon dummy die to a DBC substrate for reliability testing, (c) the sample mounted on the flip-chip bonder, alongside the microcontroller and temperature sensor used for the bonding process using sintered silver preforms, (d) finished sample on a silver plated copper substrate, and (e) the sample set bonded to DBC coupons for reliability testing.

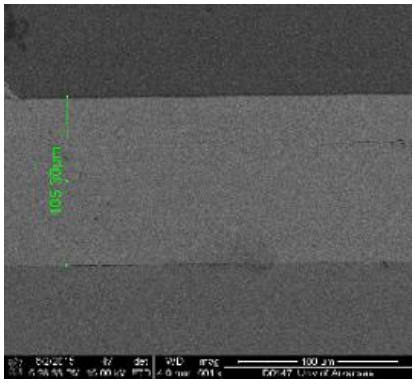
4.2.3: Bond Quality Inspection and Reliability Testing of Sintered Nanosilver Preform Assisted Die Attachment

For the estimation of bond quality, the copper substrate bonded samples were cross-sectioned and shear tested. The shear test for the samples was conducted on a Nordson Dage 4000 series die-shear tester, which was expected to provide more accurate results as compared with the Sebastian 5 described earlier. As before, the cross-section of the samples was observed under a scanning acoustic microscope to accurately inspect the microstructure of the bond. The results of the analysis are presented in Figure 4.18. Figure 4.18(a) shows the SEM image of the left edge of a sample bonded using the undersized sintered silver preform. The preform appeared inset to the die area and there was no paste extrusion out of the side of the sample or up the side walls. A zoomed-out view of a section of the bond line is presented in Figure 4.18(b) and was found to be highly

planar and virtually void-free. The nominal bond line thickness obtained using this process was found to be approximately 100 µm, with less than 10% variation across the entire bond line. The extremely low voiding is also apparent upon zooming in further into the bond line, and one such image is presented in Figure 4.18(c). During the die shear test, the die disintegrated before a break in the bond line of the sample, reflecting the same results that were obtained with the dry nanosilver preforms. Figure 4.18(d) shows a photograph of the remains of the ruptured die still attached to the substrate after the die shear test, and Figure 4.18(e) shows a magnified optical microscope image of the failure surface on the substrate. The die attach layer was unharmed even at the maximum-force point of the die shear test.



(a)



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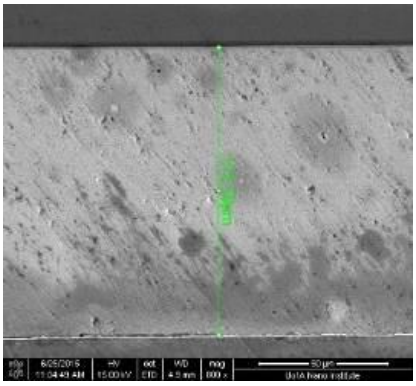

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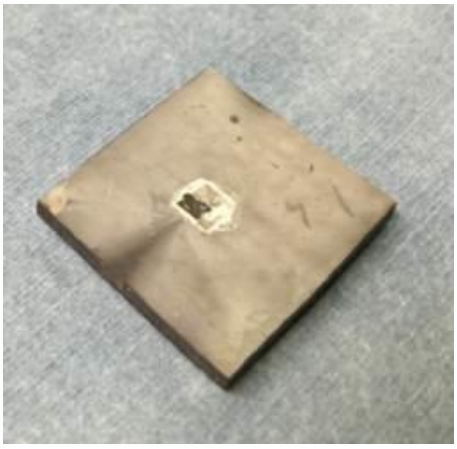


(d)

(e)

Figure 4.18: (a) An SEM image showing the inset bond formed using undersized sintered silver preforms, (b) An SEM image showing a zoomed-out view of a highly planar bond line using sintered silver preforms, (c) A zoomed-in SEM image of the bond line showing a virtually void-free microstructure in the bond line, (d) a photograph showing the bottom surface of the ruptured die still attached to the substrate surface after die shear testing, and (e) an optical microscope image showing the failure surface on the substrate following the die shear test.

At this point in the study, the benefits of preform-assisted silver sintering were clearly apparent. However, it was important to evaluate the performance of the novel preform technology using reliability tests. It was crucial to investigate whether the preforms retained their favorable bonding strength through several cycles of rigorous accelerated testing. For this purpose the die

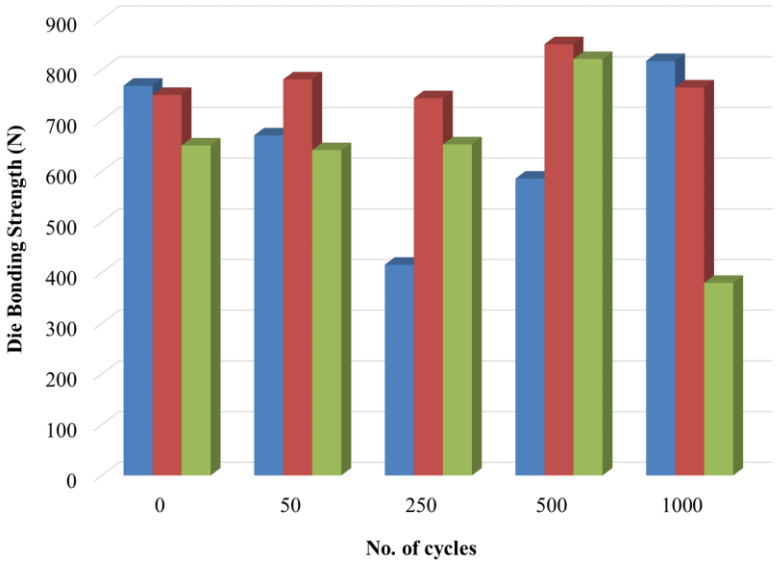
bonded to the DBC substrate using sintered preforms were subject to a thermal shock test. The parameters of the thermal shock test are outlined in Table 4.1. These conditions follow JEDEC standards used for evaluation of die-attach materials. The photograph of the thermal shock chamber is shown in Figure 4.19. The chamber contains two separate reservoirs containing Galden fluid (D02-TS). The temperature of the first reservoir (under right window of chamber) was maintained at 125 ºC, while the second reservoir (under left window of chamber) was held fixed at -55 ºC. According to the dwell time set on the dials in the front panel, a sample basket was dipped in one of the reservoirs and submerged. The process was repeated for the second reservoir. A few seconds of wait time was added in between reservoirs to allow the samples to drip-dry.

Table 4.1: Thermal shock test parameters

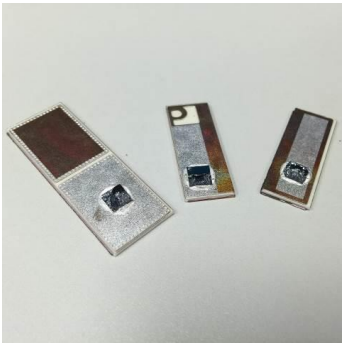
Temperature range (ºC)	125 to -55
No. of cycles	1,000
Dwell Time (minutes)	2
No. of samples	19

Figure 4.19: A photograph showing the thermal shock chamber.

In between the 1000 cycles of thermal shock, a few samples were extracted every few hundred cycles and subject to a die shear test in a bid to investigate the reduction in the bonding strength as a function of the increasing number of thermal shock cycles. The results of the periodic die shear tests are documented in the graph presented in Figure 4.20(a). In most cases, the failure mode was die fracture rather than a break in the bond—adhering to the same trend as observed thus far. Some representative samples can be seen in Figure 4.20(b). However, these were very high bonding strengths in their own right, and the strength of the bond may be assumed to be greater than these values. The test was halted at 1000 cycles when the internal alumina layer of the DBCs started cracking under the die shear test. A photograph showing a completely sheared off DBC substrate is shown in Figure 4.20(c).



(a)



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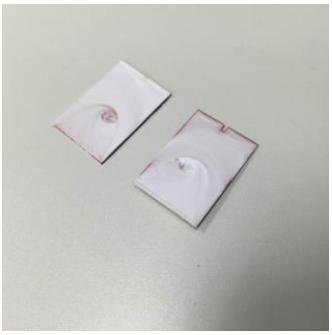
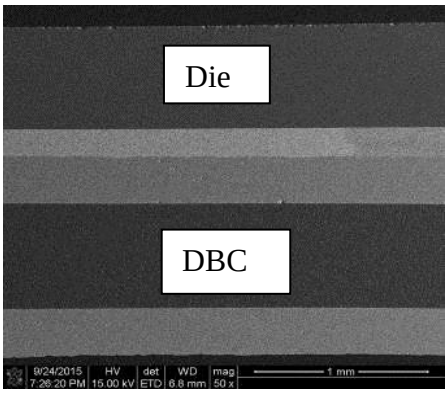


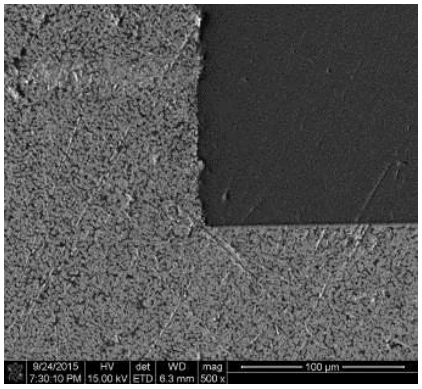
(c)

Figure 4.20: (a) A bar graph showing the die bonding strength as a function of the number of thermal shock cycles, (b) a photograph showing samples with ruptured die after the die shear test, and (c) a photograph showing a cracked and sheared-off DBC after 1000 thermal shock cycles.

For a further analysis of the failure mode and reliability performance of the preform-bonded samples, the samples surviving 1000 thermal shock cycles were cross-sectioned. “Figure 4.21(a) shows the SEM image of the bond line of a sample after 1,000 thermal shock cycles. No widespread cracks or evidence of voids were observed. Figure 4.21(b) shows a zoomed in image of the left edge of the die showing no signs of voiding or degradation after 1000 cycles. Figure 4.21(c) shows a zoomed in image of the right edge of the die, where initial signs of crack formation and voiding are visible. Upon closely observing the base of the die on the right side [Figure 4.21(d)], it can be observed that a crack is initiated and propagates toward the center of the sample. However, at 1000 cycles, the crack did not spread into the bond line enough to cause a reduction in the die bonding strength. As can be seen from Figure 4.21(e), the center of the bond line shows no voiding or signs of cracking. Figure 4.21(f) is an optical microscope image of the DBC substrate taken after 1000 cycles. It confirmed the delamination of the copper layer from the ceramic. In fact, it was observed that a horizontal crack initiated in the ceramic layer. Hence, before the die attach strength becomes a limiting factor at the harsh temperature swing of the experiment, the substrate technology was found to fail.


Die
DBC
9/24/2015 HV det WD mag
7:26:20 PM 15.00 kV ETD 6.8 mm 50 x
1 mm

(a)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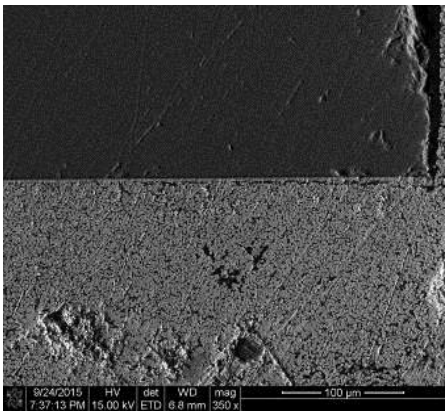
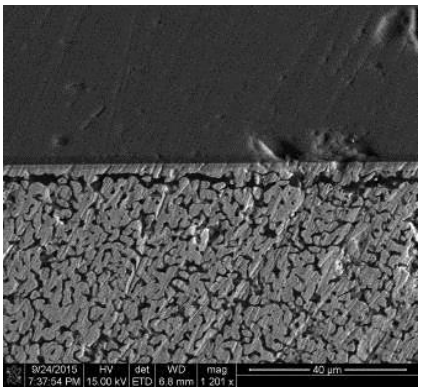
100 µm

(b)


9/24/2015 HV det WD mag
7:37:13 PM 15.00 kV ETD 6.8 mm 350 x
100 µm

(c)



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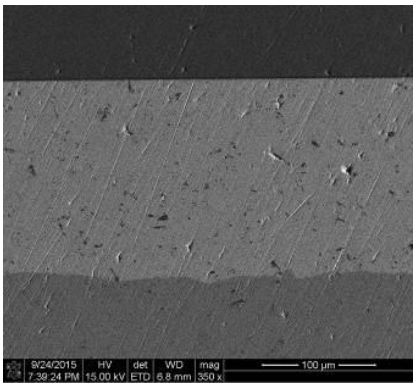

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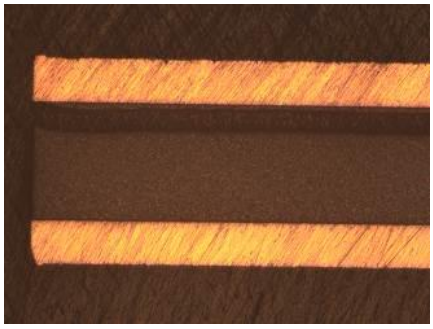


(f)

Figure 4.21: SEM images showing (a) the bond line after 1000 cycles, and (b) the left edge of the sample showing no signs of degradation after 1000 thermal shock cycles, (c) the right edge of the die showing signs of voiding and crack formation after 1000 cycles, (d) a zoomed in image of the base of the doe on the right edge of the sample showing crack formation which could lead to delamination, (e) a zoomed in image of the center of the bond line showing no voiding or cracking even after 1000 thermal shock cycles, and (e) the DBC substrate showing delamination due to thermal stress."

Conclusions and Impact

Die attachment process using sintered nanosilver preforms yielded a much superior performance as compared with bonding processes using nanosilver paste alone. The process was highly repeatable and yielded consistently flat bond lines of very high quality. Sintered nanosilver preforms were preferable to dry nanosilver preforms since it demonstrated a superior structural integrity. This translated to better handling and eliminated the risk of accidental damage to the preform during the bonding process.

The sintered preforms could be tailored to match the bond pads of any commercially available bare die device. The thickness of the preform may also be tailored to a specification by using a single-step or multi-step stencil and cure process. The process flow for preform-assisted die attachment was very well-suited to be adapted to a high-volume manufacturing setup. The resulting bond line also has very low porosity and was found to withstand as much as 1000 cycles of intense accelerated testing. In fact, a state-of-the-art substrate material was found to fail at the end of the 1000 cycles, but there was hardly any degradation observed in the die-attach layer.

One of the most important implications of this technology is from the standpoint of 3D die bonding. Sintered nanosilver material has superior properties as compared with solder and is one of the sole options in ambient temperatures in excess of 300 ºC. In paste form however, the material easily extrudes out of the boundary of the desired bonding area and also up the side walls of a die. The extrusion will result in an electrical short or arcing in a 3D stack. It was demonstrated in this study that paste extrusion could be arrested successfully by using undersized sintered silver preforms. This essentially means that sintered nanosilver may be used to bond both the bottom pad and top pad of a SiC power device to a substrate or interposer. The resulting bond would be of a customized and optimized thickness and shape, and would not melt up to a temperature of nearly

1000 ºC. This would herald in a completely new interconnection scheme, which could outperform contemporary 3D interconnect technologies (solder spheres, solder pastes, metal posts/pins, fuzz buttons, spring pins, etc.) from an electrical, thermal, and reliability standpoint.

References

[1] H. Zheng, D. Berry, J. N. Calata, K. D. T. Ngo, S. Luo and G. Q. Lu, "Low-Pressure Joining of Large-Area Devices on Copper Using Nanosilver Paste," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 3, no. 6, pp. 915-922, June 2013.

[2] Kewei Xiao, Susan Luo, K. Ngo and G. Q. Lu, "Low-temperature sintering of a nanosilver paste for attaching large-area power chips," *2013 IEEE International Symposium on Advanced Packaging Materials*, Irvine, CA, 2013, pp. 192-202.

[3] T. Wang, G. Chen, Y. Wang, X. Xhen, and G. Q. Lu, "Uniaxial ratcheting and fatigue behaviors of low-temperature sintered nano-scale silver paste at room and high temperatures," Materials Science and Engineering A, Vol. 527, pp. 6714-6722, 2010.

CHAPTER 5: The Flip-Chip Power Device Package—bridging the gap between wire-bonded modules and 3D wire bondless LTCC modules

DISCLAIMER: The content of this chapter has been the subject of a previous publication and an invention disclosure by the author [1 – 2].

The concept of using an LTCC interposer in conjunction with customized sintered silver preforms has its advantages with respect to reliability. As explained earlier, the standard LTCC metallization process does not have adequate electrical conductivity to be employed in power module applications. As the demand on power density rises, the current-carrying requirement will increase within a small volume. The comparatively high resistance of LTCC metallization will lead to undesired voltage drops along with Joule heating of the traces. This will offset the signal fidelity advantages obtained from using a 3D packaging scheme and further complicate the thermal management. A direct LTCC copper plating process needs to be developed for this technology to be a success in power module applications. The reliability of any such plating schemes also needs to be evaluated and contrasted with the state-of-the-art. Summarizing the above concerns, it is safe to ascertain that the LTCC process has to be reconfigured sufficiently before a novel 3D power module topology is evaluated based on it. A failure to proceed with the current LTCC process will run the risk of LTCC metallization deficiencies being misconstrued as drawbacks of the 3D power packaging paradigm.

Four cardinal factors were considered carefully while refining the design for the 3D wire bondless topology—cost, serviceability, simplicity of implementation, and a holistic approach. For a vast majority of power electronics applications, cost and serviceability are critical metrics of the design process. This will become increasingly important as the market for power electronics expands and finds a wider consumer base. The goal was to propose a unified concept, which could

be scaled in cost, serviceability, and reliability depending on the demands of the application. This would provide the platform for flexible adoption by all applications—ranging from low cost, serviceable consumer-grade power electronics (like solar inverters), to highly reliable, rugged power systems (like aerospace applications).

Simplicity of implementation was another priority in the design. Silicon carbide power devices need to be more closely integrated into a power electronics system. The modern-day wire bonded power module is a weak electrical interface to the rest of the system. Granted that it is customizable to a degree, the contemporary power electronics system designer still regards the power module as a "black-box" with input and output terminals. This is against the philosophy of a highly efficient co-design approach, where the system is treated as a whole and optimized for performance. Treating a power module as a separate entity is principally against this holistic approach. A platform is required where adequate creative opportunity is handed to the system designer to be able to realize an optimally efficient system. Each switching position should be flexible and configurable with respect to placement and routing.

Section 5.1: The concept of a chip scale power device package

Chip-scale packages provide a performance that is very close to that of a device in bare die form. The parasitic effects distorting the electrical performance can be minimized using chip-scale integration processes. If designed correctly, they can be constructed using relatively low cost materials while providing a comparable thermo-mechanical performance to the LTCC approach described in Chapter 3. The process and evaluation of converting a SiC bare die power device to a chip-scale package will be described in this chapter. Flip-chip bonding is a well-known process for the bonding of chip-scale devices. The flip-chip bonding process has been historically demonstrated to provide low-parasitic interconnections [3]. SiC power devices are commercially

available as vertical devices, with electrical interconnections on both sides of the chip. To be accommodated into a system at a chip-scale, both sides of the chip need to be bonded. This implies the requirement of an electrical interposer for both the top and bottom layers. What complicates matters even more is if die with different thicknesses are used in the module—which is the situation more often than not. The flip-chip power device package described in Figure 5.1 provides a solution to this issue.

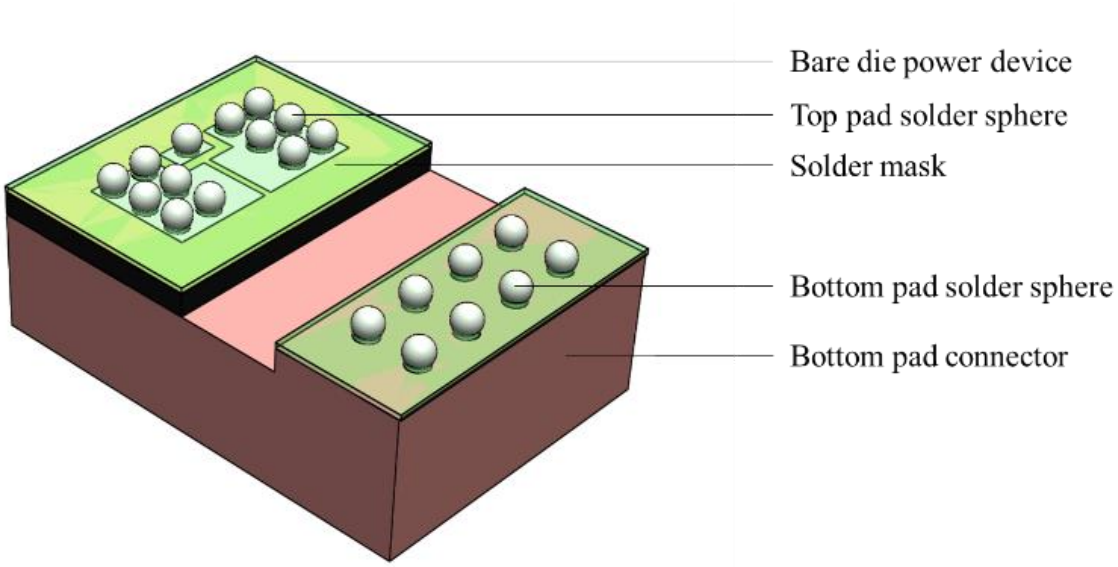


Figure 5.1: The concept of a flip-chip power device.

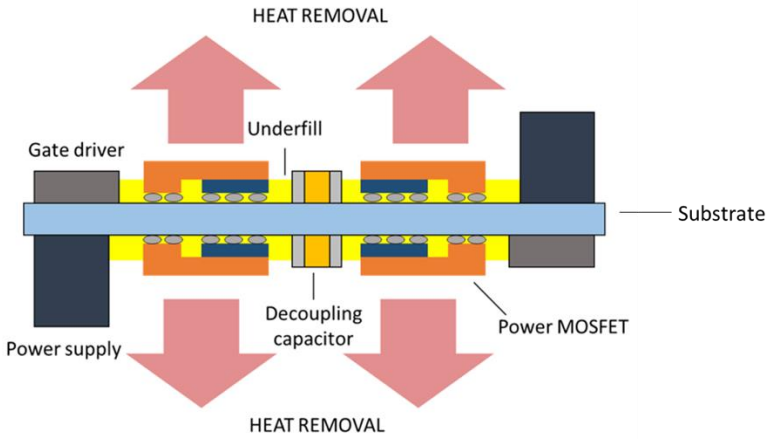
In Figure 5.1, a bare die power device is seen bonded to a copper connector. Die attachment may be accomplished using soldering or silver sintering. The device is representative of the 1200 V-rated S2301UCSF SiC power MOSFET from ROHM Semiconductor. The description, process flow, and implementation is adaptable, however, to any SiC power device in bare die form. The copper terminal is shaped like a raised shelf, and the thickness of the extruded section is equal to the thickness of the die. Alternatively put, the depressed section of the connector is as deep as the die is thick. The top plane of this assembly presents a flip-chip capable surface containing electrical

contacts to all the device pads. Thus, the bottom connector effectively translates the bottom terminal of the chip to a top side contact. This concept has several advantages:

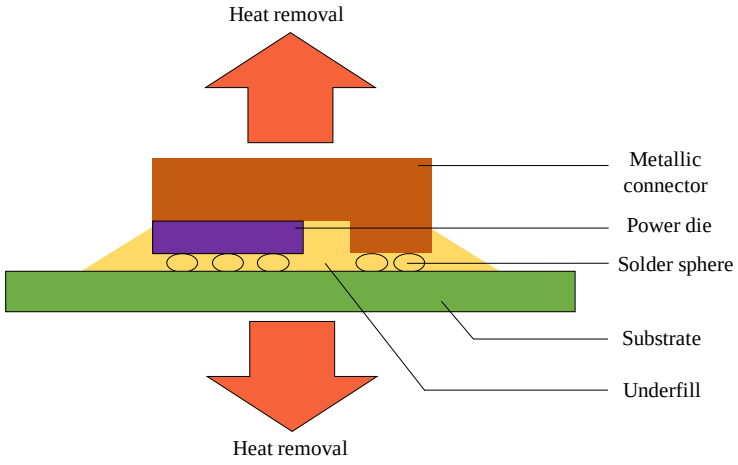
1. Wire bondless interconnections: The resulting chip-scale package may now be flip-chip bonded to any choice of substrate through low inductance flip-chip interconnections. It will result in a closely integrated system as described in Chapter 3. This will be quantified in greater detail in due course, but a simple schematic is provided in Figure 5.2(a) to serve as a visual aid.

2. Low thermal resistance path to the heat sink: The flat reverse side of the bottom connector will be used as the principal surface for heat removal. The material used for the bottom connector will be copper, molybdenum, or a SiC-CTE-matched metal matrix composite (MMC). Each of these materials have high thermal conductivities which will present an extremely low resistance path for the waste heat generated by the chip to the heat sink. An electrically insulating thermal interface material will have to be employed for heat sink attachment if multiple devices belonging to different signal nets are desired to be bonded to a common heat sink. This scheme also introduces the scope for double sided cooling by incorporating thermally conductive features within the interposer. A diagrammatic representation is shown in Figure 5.2(b).

3. Devices of different thicknesses will have a coplanar profile: If devices with different thicknesses are used in the same system, each device can be configured into a chip-scale package of a common thickness. This can be achieved by adjusting the depth of the step in the bottom connector. This is illustrated in Figure 5.2(c).


HEAT REMOVAL
Underfill
Gate driver
Substrate
Decoupling capacitor
Power MOSFET
Power supply
HEAT REMOVAL

(a)


Heat removal
Metallic connector
Power die
Solder sphere
Substrate
Underfill
Heat removal

(b)


Equal Height
Thicker die with deeply milled metallic connector
Thinner die with shallow metallic connector

(c)

Figure 5.2: Schematics depicting (a) the implementation of chip-scale power devices in a 3D wire bondless module topology, (b) the thermal management of the proposed chip-scale devices, and (c) package height equalization for die of different thicknesses.

Also observed in Figure 5.2, solder spheres were placed on the electrical pads of the chip-scale package. Note that the electrical interconnection may be achieved by using a plurality of alternative methods—direct solder, solder preforms, sintered silver, sintered silver preforms, and the like. For methods involving a flat layer of solder, there are risks of electrical shorting because of the close proximity of the pads on the top surface of the chip. Also, a flat solder layer is typically a few tens of microns thick. This increases the risk of an unsatisfactory underfill process. It is highly desirable to incorporate an underfill step in any flip-chip process to help cushion thermo-mechanical and enhance the voltage isolation. Using sintered silver preforms for bonding, on the other hand, would necessitate a gold or silver surface finish on both the die and the substrate. This would introduce additional steps and cost in the process.

Underfilled solder spheres have been a highly reliable method for flip-chip bonding in microelectronic circuits. They provide a very high interconnection density, coupled with self-planarization and self-centering properties arising from the surface tension of solder. Flip-chip BGAs have coped exceptionally well with the high thermal stress in microelectronics circuits, and this benefit can be realized in power electronics systems as well. BGAs also serve as a low parasitic electrical interconnect in circuits with very high speed switching requirements [4]. Due to the versatility and low cost of solder spheres, they were preferred as the material-of-choice for fabricating the proposed prototype. The use of solder spheres also facilitated the use of FR4 PCBs for the interposer material. Despite the larger CTE-mismatch, it will be shown in the following section that using an FR4 substrate (with solder spheres) provides comparable stress relief with the CTE-matched LTCC scheme (with sintered silver).

Section 5.2: Thermo-mechanical analysis

The thermo-mechanical analysis of the flip-chip structure was conducted in ANSYS. A transient temperature spike of 175 ºC was applied to the chip, and the thermal profile was imported as a load for the mechanical stress simulation. The model is presented in Figure 5.3. The bottom connector and chip have been rendered transparent to obtain an unhindered view of the solder sphere array. Only half the module was modeled across a plane of symmetry. This is a standard approach in finite-element simulation to decrease the computation time and increase the accuracy of the results through finer meshing. The assembly was fixed along the plane of symmetry to serve as reference point for evaluating the stresses and displacements resulting from the thermal load. The material for the chip, connector, and solder and substrate were assigned as SiC, copper, Pb63Sn37, and FR4 respectively. This provided a truly economical choice of materials while still enabling low-inductance flip-chip interconnections.

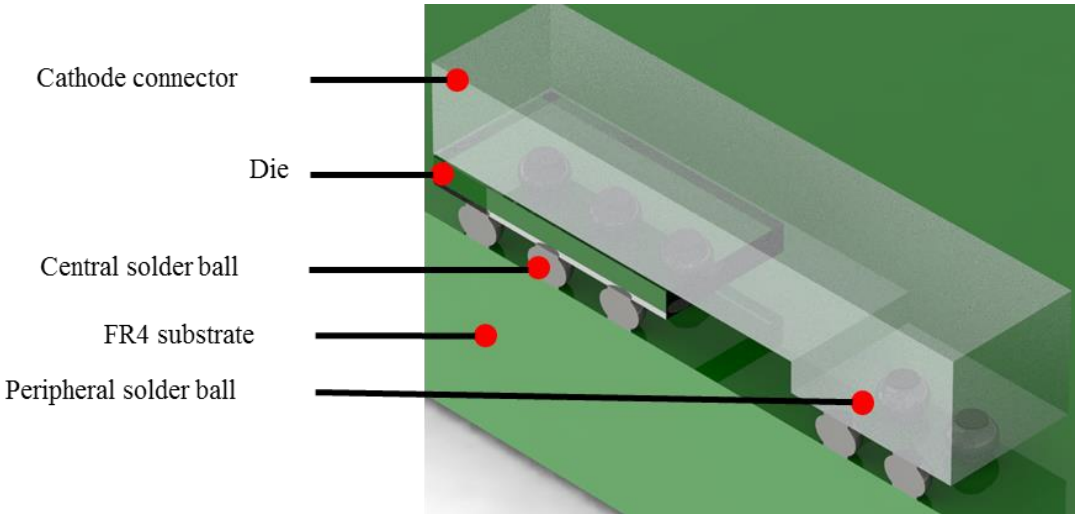


Figure 5.3: Simulation model for thermo-mechanical stress evaluation.

The temperature was limited to 175 ºC since the maximum allowable temperature of a commercially available SiC power device does not exceed this value. Also, the selected solder spheres had a melting temperature of 183 ºC. Solder with a higher reflow temperature could be a

simple answer if a higher temperature capability is desired, but this would require the characterization of the solder material. The Young's modulus of solder changes with temperature. For the solder composition used for this study, the variation is well-documented in the literature and is presented in Eq. 5.1 [5].

$$E\,(T) = 34470 - 151.7 * T\,(MPa) \qquad \text{(Eq. 5.1)}$$

The performance of the module under test was contrasted with a conventional wire-bonded module. The control model is shown in Figure 5.4. This module was also symmetrically cleaved and consists of a SiC chip on a DBC substrate with aluminum nitride (AlN) as the dielectric. This is a common choice of substrate for SIC power modules due to the near-ideal CTE match of AlN with SiC. The material for the wire bonds was defined as aluminum with a 10 mil diameter.

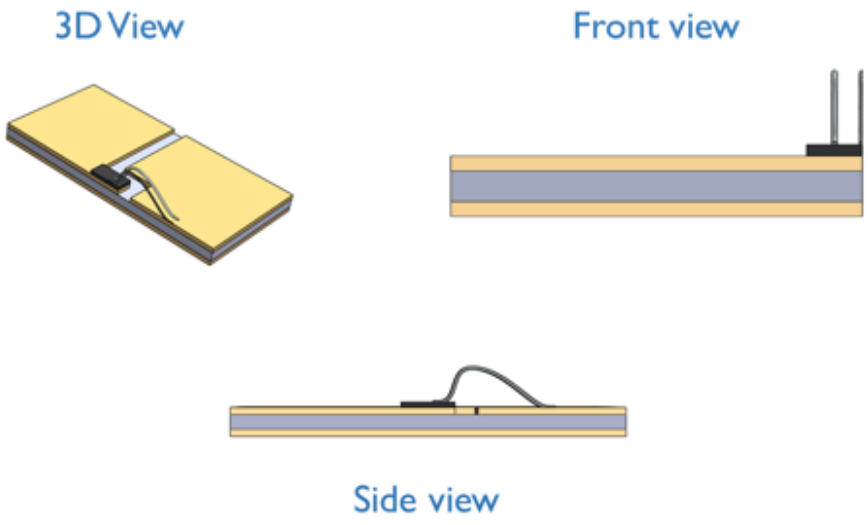
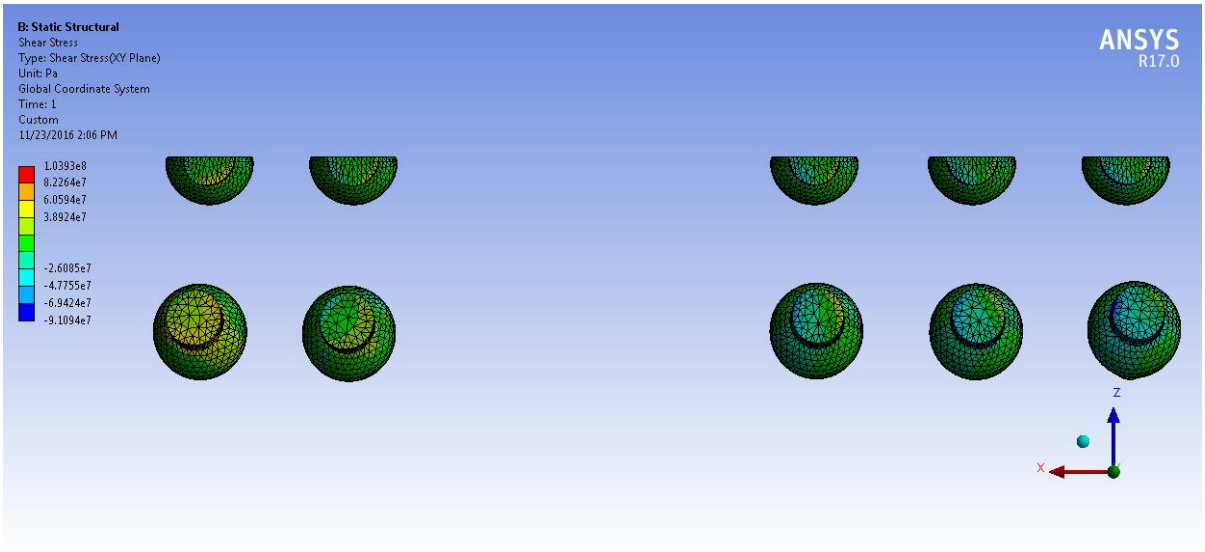


Figure 5.4: The model for the wire-bonded control module

The results of the simulation for the flip-chip module are presented first. Figure 5.5(a) shows a top view of the module. All other components except for the solder spheres were hidden to be able to view the shear stress on the interface between the solder sphere and the SiC die. Figure

5.5(b) shows a view from the bottom, highlighting the interface between the solder sphere and the substrate. The maximum shear stress on the solder spheres was found to be about 104 MPa. However the maximum stress occurred at a specific location in the assembly. It was found to reside on the edge of a peripheral solder ball. This is clearly visible in the alternate views of the stress pattern presented in Figure 5.5(c) and (d). The stress on the solder balls connecting the copper connector and the FR4 were observed to be greater than those connecting the SiC die and the substrate. This was probably due to the higher CTE of the copper and the FR4 material which results in greater expansion. The central solder spheres experienced about 30 MPa lower maximum stress as compared with the substrate interface [Figure 5.5(e)]. The peripheral solder sphere farthest from the fixed plane of symmetry showed the maximum stress since it experienced the largest lateral deformation during thermal expansion.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Shear Stress
Type: Shear Stress(XY Plane)
Unit: Pa
Global Coordinate System
Time: 1
Custom
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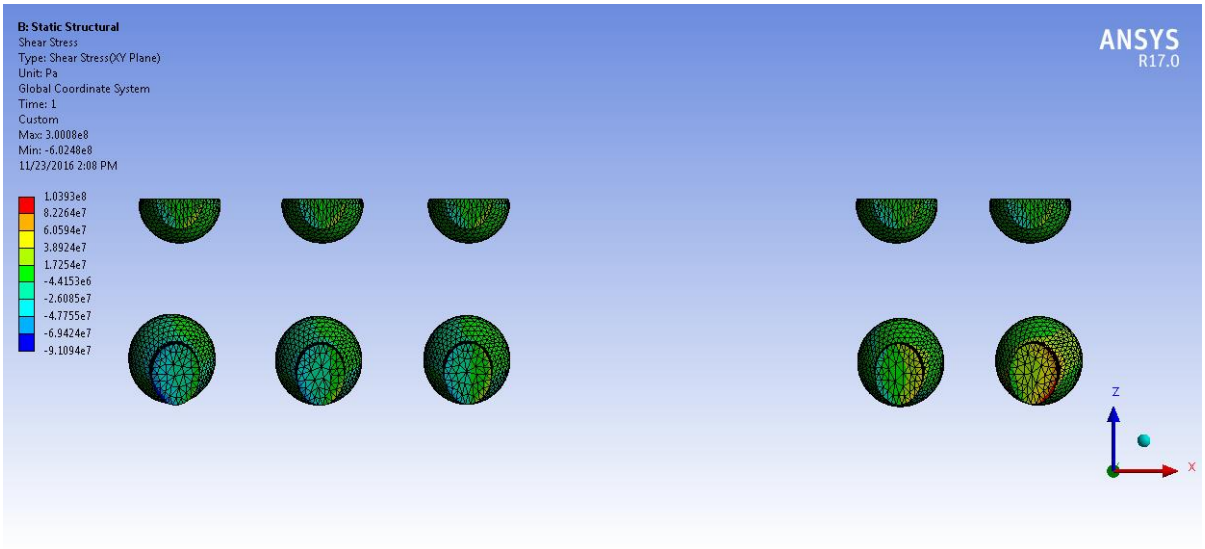
6.0594e7
3.8924e7
-2.6085e7
-4.7755e7
-6.9424e7
-9.1094e7
ANSYS
R17.0
Z
X

(a)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1.7254e7
-4.4153e6
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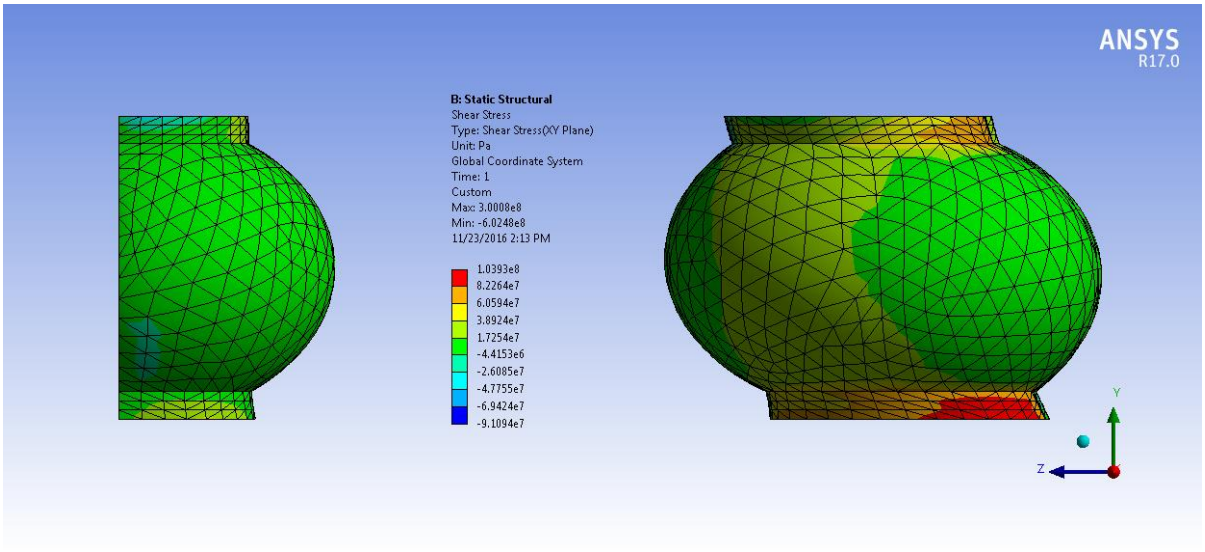
(b)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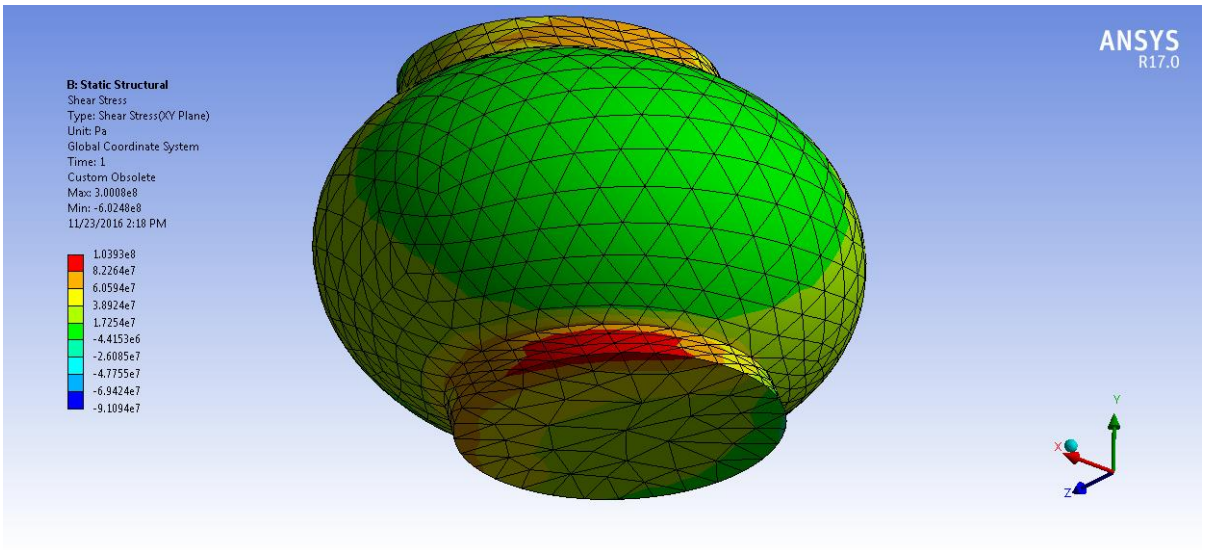
Y
Z

(c)


ANSYS
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Shear Stress
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Unit: Pa
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Min: -6.0248e8
11/23/2016 2:18 PM
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1.7254e7
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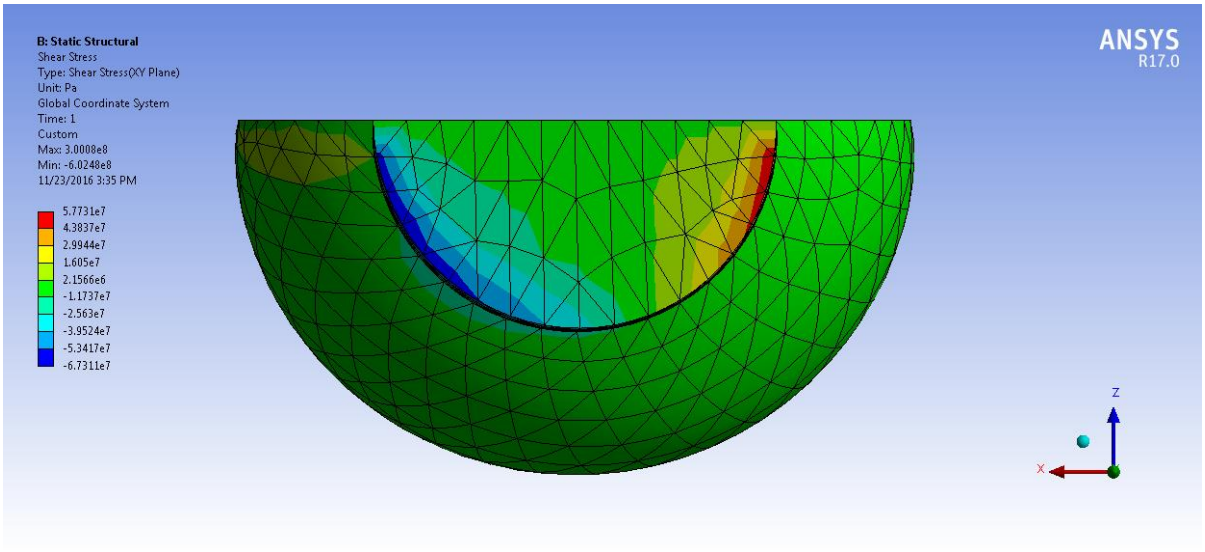
(d)

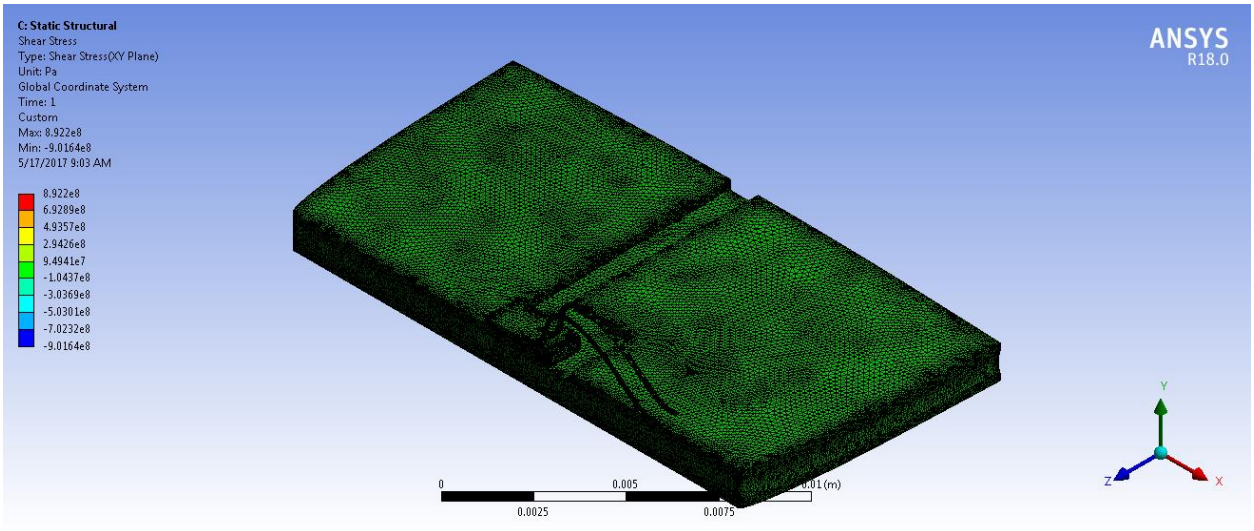


(e)

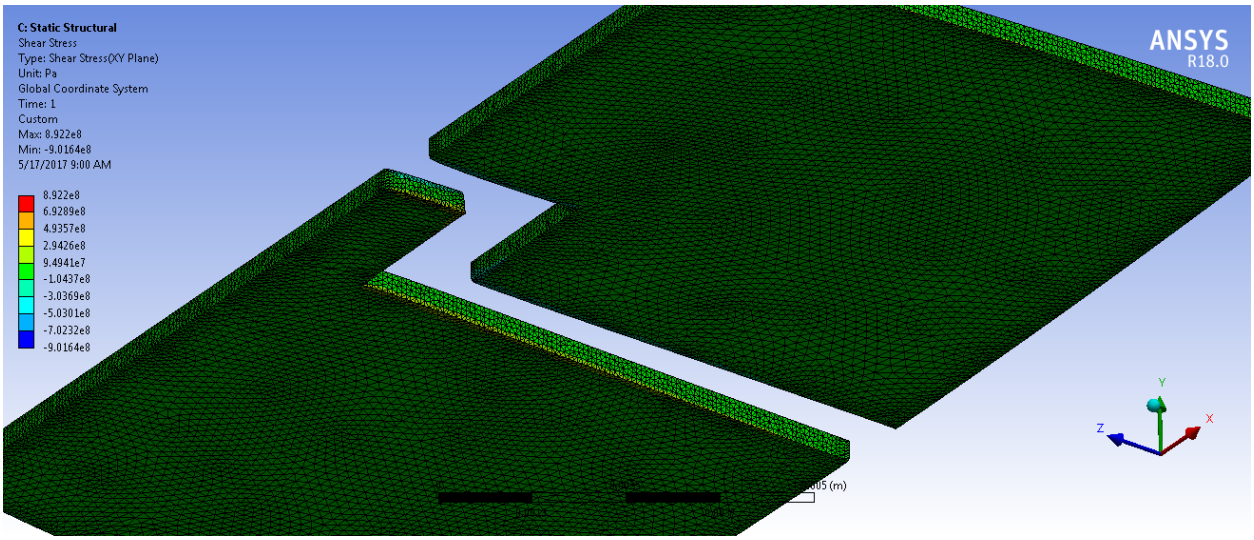
Figure 5.5: Thermo-mechanical stress analysis of the flip-chip module showing (a) the top view of stress distribution in the solder ball array, (b) a bottom view of stress distribution in the solder ball array, (c) side view of the peripheral solder balls experiencing maximum shear stress, (d) stress distribution on the outermost solder ball, and (e) a top view of the same.

A similar analysis for the wire bonded module is shown in Figure 5.6. A very fine mesh was selected for this model as well, to be able to allocate a sufficient number of mesh elements to thin features. The meshed model showing the thermomechanical shear stress in response to a thermal load of 175 ºC on the chip is presented in Figure 5.6(a). A common failure mode in power modules is the delamination of the copper layer of the DBC [6]. The stress plot of the top DBC layer indicates this and is presented in Figure 5.6(b). A very high stress was found to exist along the edges of the top metallization, which usually initiates cracking mechanisms at the edges. This was also observed in the DBCs sued for the reliability studies in Chapter 4. The proposed flip-chip approach does not run this risk since the approach is entirely DBC-less. Such alternative approaches and novel substrate technologies are the need of the hour to increase the reliability SiC power modules if an elevated operating temperature is desired. DBC is traditionally used, but perhaps not best suited for the purpose.

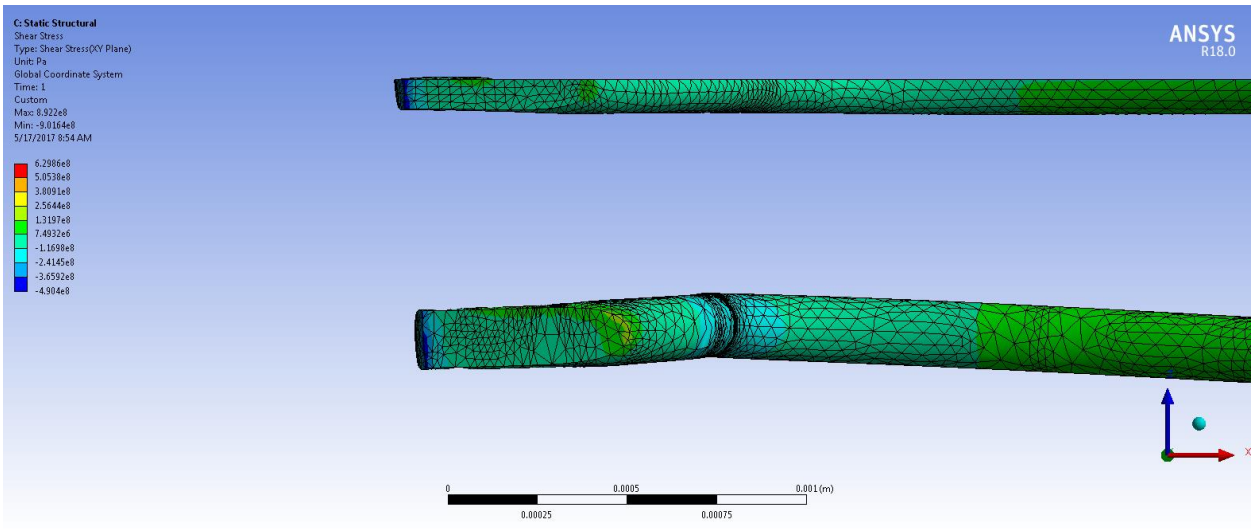
The focus of the investigation, however, was the stress on the interconnects. There are two principal mechanisms by which wire bonds have been reported to fail—heel cracking and lift-off [7]. This was easily understood upon plotting the stress pattern of the wire bond feet. A high concentration of CTE mismatch shear-stresses were observed on the heel and foot areas on both the die side [Figure 5.6(c)] and the substrate side [Figure 5.6(d)].



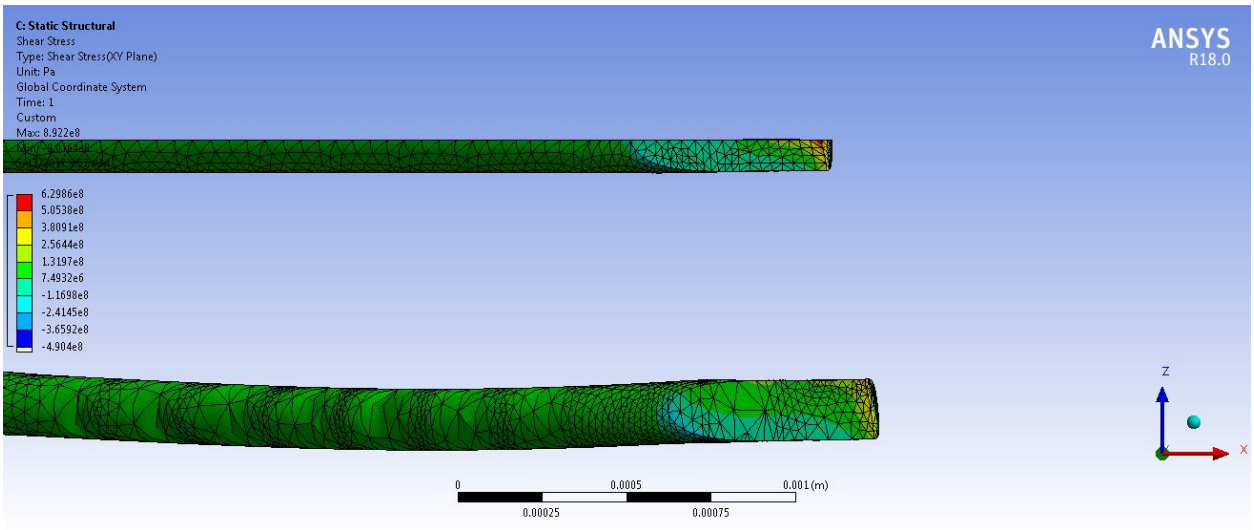
(a)



(b)



(c)



(d)

Figure 5.6: Thermo-mechanical stress analysis of the wire bonded control module showing (a) the mesh and overall thermo-mechanical shear-stress pattern on the wire bonded control module, (b) the high stresses on the edge of the DBC layer, (c) the stress pattern on the die side of the bonding point of the wire bonds, and (d) the same for the substrate side of the wire bonds.

As initially expected, the shear stress for a wire bond was found to greatly exceed the solder sphere array. The maximum stress on the wire bonds amounted to nearly 630 MPa, compared with

about 103 MPa for the solder spheres. It must also be noted that the maximum stress was located mainly in a peripheral solder ball. The maximum stress for the wire bonds was experienced by each and every wire bond. In the solder sphere approach there is always the option of adding sacrificial peripheral solder spheres to build redundancy into the system and hence delay catastrophic failure.

Simulations were also conducted to verify the optimal choice for a substrate. The maximum shear stress on the solder ball is plotted for different commonly used substrate materials in Figure 5.7. Quite intuitively, FR4 material was found to perform much better than CTE-matched alternatives lie Dupont 9K7 (LTCC) and aluminum nitride (AlN). The reason for this was the higher elasticity of FR4. In case of the rigid ceramic materials, the highly elastic solder balls expanded rapidly in the center with increasing thermal stress, while the bonding interface resisted due to the lack of elasticity of the ceramic materials. In the case of FR4, they were allowed to expand at the interface as well. This situation was clearly visible upon animating the respective stress plots in the ANSYS Workbench environment.

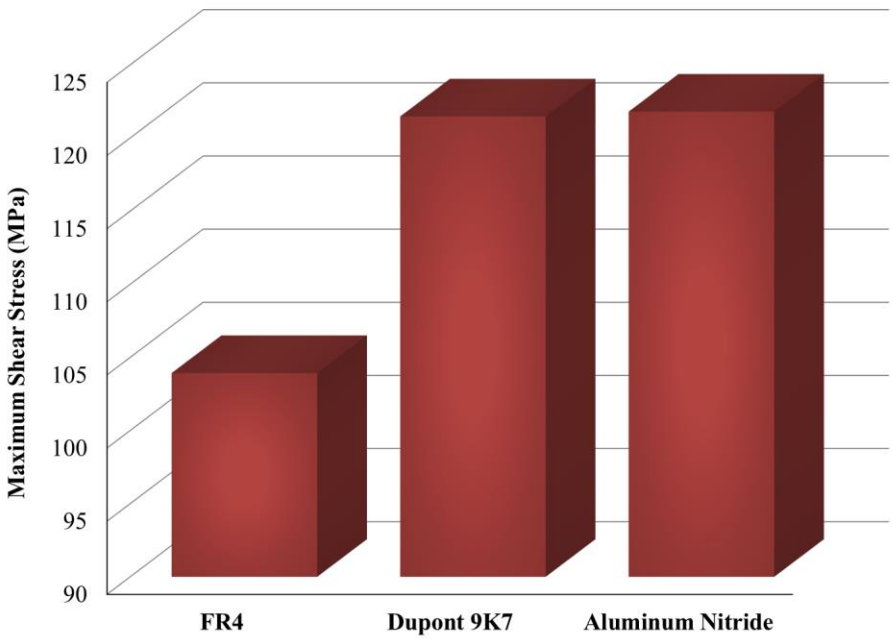


Figure 5.7: A graph showing the maximum shear stress as a function of substrate material.

The thickness of the bottom connector was also an unknown variable in the design. To optimize this, the thickness of the connector was increased in steps of 0.5 mm, and the thermal stress on the solder spheres and the die bonding layer was evaluated. It was found that changing the connector thickness had no significant effect on the thermo-mechanical stress at the die-attachment interface. However, the maximum stress on the solder spheres decreased with increasing thickness. This was expected intuitively since a thinner connector would warp easily under thermal stress, while a thicker conductor would remain flat. It was also observed that the maximum stress did not change appreciably beyond a connector thickness of 1.5 mm. In the interest of obtaining the least resistive thermal path, 1.5 mm was chosen as the optimum connector thickness. Since the reverse side of the bottom connector serves as the interface for heat removal from the assembly, thicker metal would present a higher resistance to the thermal path. These results are plotted in Figure 5.8.

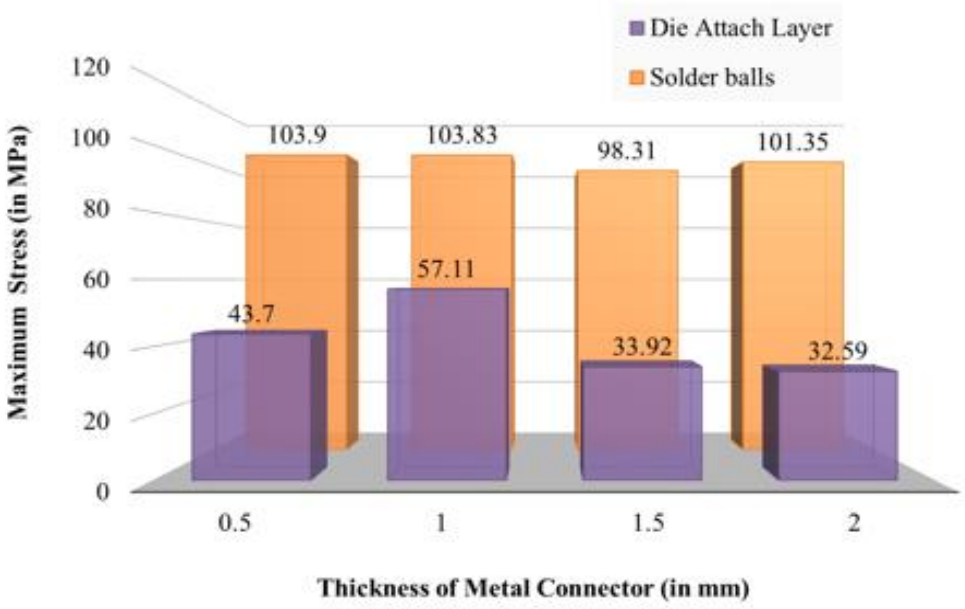


Figure 5.8: Bar graph showing the variation of the maximum stress in the solder sphere array as a function of increasing metal connector thickness.

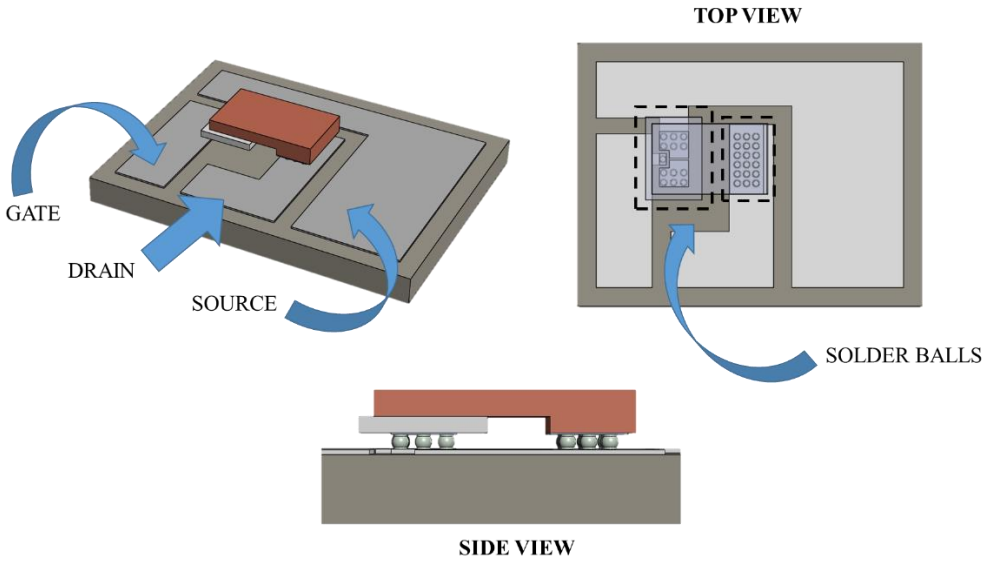
It must be noted that the stresses on the die attach interface may be greatly reduced by using a molybdenum or AlSiC MMC connector with a much closer CTE match with SiC than copper.

Section 5.3: Parasitic analysis

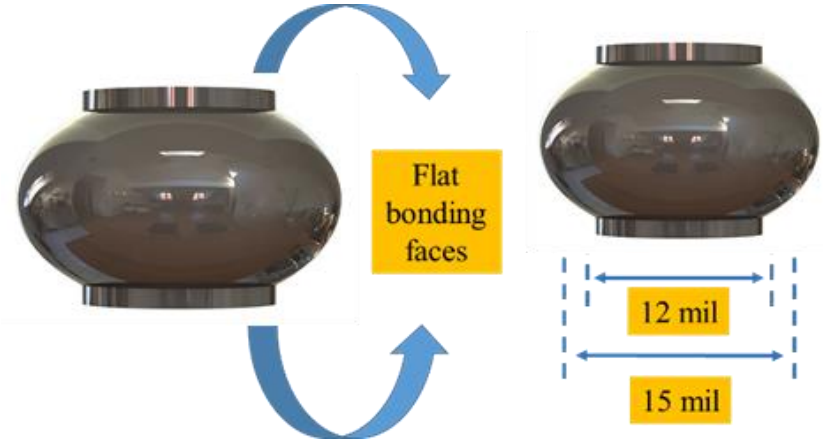
In Chapter 3, the parasitic inductances associated with the flip-chip module was found to be significantly lower than its wire bonded counterpart. However, the contact between the bond pads of the device and the interposer was assumed to be a thin layer of sintered silver. Both the electrical resistivity and electrical path length may increase as a result of using a solder sphere to achieve the same end. Also the solder sphere array will have a slightly lower bond pad coverage as compared with a blanket layer of sintered silver, depending upon the diameter and spacing of the solder spheres. These factors are expected to have an impact on the parasitics of the resulting

switching loops. The goal of the simulations presented in this section is to evaluate whether this impact is significant enough to reconsider the proposed approach.

For this purpose, the model shown in Figure 5.9(a) was considered. It shows a single flip-chip type MOSFET bonded to a patterned substrate using an array of solder spheres. The diameter of the solder sphere was chosen to cover a maximum area of the gate pad. As has been illustrated earlier in Chapter 3, maximum gate pad coverage ensures the least parasitics. The gate of the device in question measured 0.3 mm × 0.8 mm. Hence a 15 mil solder sphere diameter was chosen. Once the diameter of the gate solder spheres was fixed, the source and drain contacts were configured as arrays of 15 mil solder spheres to maintain the planarity of the assembly after reflow. Figure 5.9(b) shows the model of the solder ball used in the simulation. Instead of a perfect sphere, the model assumed a flattened solder sphere with truncated edges to be able to obtain a faithful estimate of the parasitics associated with it. "The pads for solder sphere attachment were undersized from the solder sphere size by 20%—a standard practice in BGA design. A pad diameter of 12 mil was used to bond to the 15 mil solder sphere. The geometry shown in Figure 5.9(b) closely approximates the shape of the solder joint after reflow".



(a)



(b)

Figure 5.9: Models showing (a) a flip-chip MOSFET mounted on a substrate to be simulated for parasitic extraction and (b) a single solder sphere with flat bonding surfaces and a central spherical region.

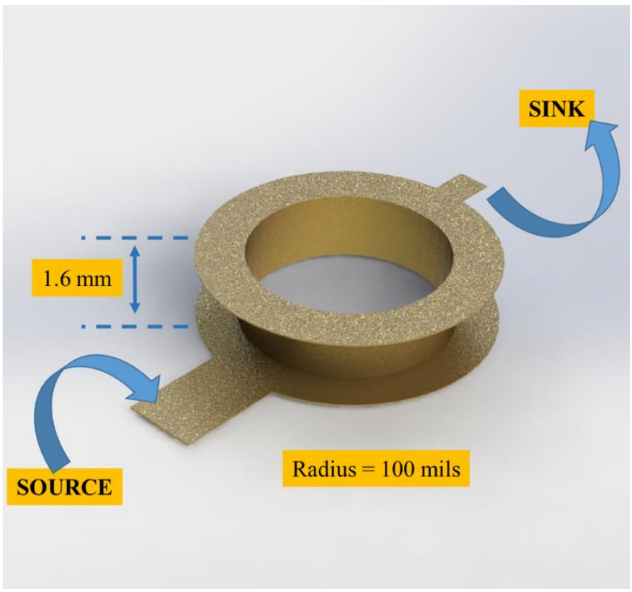
The substrate was modeled as a standard FR4 PCB with 1 oz. copper metallization. It was demonstrated in the previous section that the thermo-mechanical stress associated with using a PCB was better than the highly CTE-matched LTCC approach as described in Chapter 3. The parasitics were evaluated in ANSYS Q3D, and the parasitic inductances and resistances of the

main signal nets were calculated as a function of frequency. The gate-loop and power-loop parasitics were estimated individually.

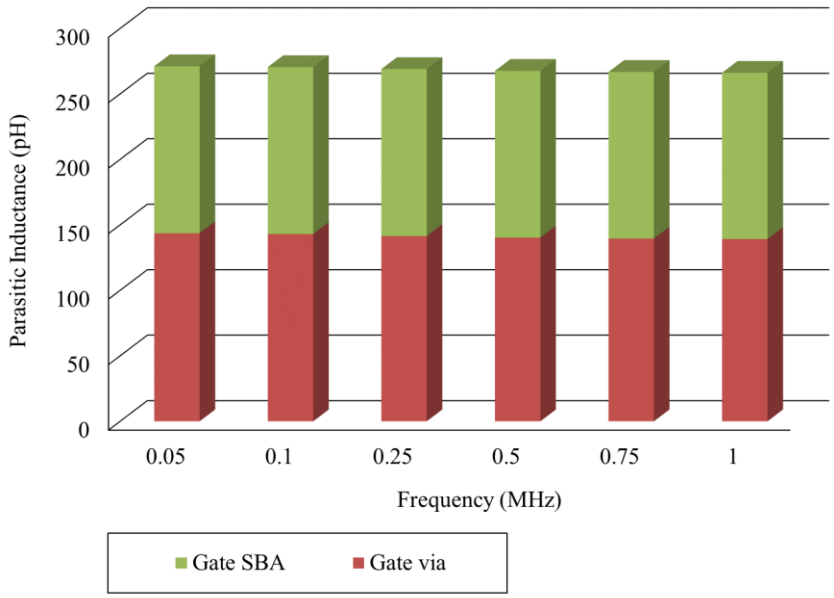
5.3.1 Gate-loop parasitic estimation

A simple estimation of the interconnect parasitics would not provide adequate information about the overall path parasitics. The signals are required to be routed to (or from) these interconnects through traces, pads, and vias on a substrate of choice. In keeping with the idea of a chip-on-board solution and in the interest of low cost, the substrate chosen was an FR4 printed circuit board. The mode of the gate interconnection was one in which a MOSFET, flip-chip bonded to the top layer, was driven by a gate driver package positioned on the bottom layer through a plated through hole via. The via diameter was chosen to be 100 mils with a standard 1 mil copper plating, and the length was modeled to be 1.6 mm. This was made equal to the thickness of a standard two-layer PCB. Although this particular via is assigned for the gate signal, similar vias may also be used to access the drain or, additionally, the source plane. The drain (or source) plane itself is usually composed of a relatively large area of 1 oz. copper, thereby presenting negligible resistance/inductance to the current path. Further, multiple vias may be used in parallel to enhance amperage—thus further reducing the inductance (and resistance). Figure 5.10(a) shows the model of a typical PCB via used to compute the parasitic inductance at different switching frequencies.

The results of the simulation are presented in Figure 5.10(b). Figure 5.10(a) shows the parasitic inductance added to the gate loop by the solder ball interconnection as a function of the switching frequency. The total path inductance is 271 pH at its maximum with a 1.8% reduction at 1 MHz. An encouraging observation was that the parasitics did not demonstrate a strong correlation with switching frequency. The total parasitic inductance estimated for this solution was substantially lower than the reported values found in the literature for that of a wire bond.



(a)



(b)

Figure 5.10: (a) The gate via model and (b) the estimated gate-loop parasitics of the flip-chip MOSFET.

One concern with using a single gate via was the current handling capability of the via metallization. The thickness of the via plating for most major PCB manufacturers is 1 mil (25.4

μm). The via is unfilled, thus making it a 1 mil thick annular cylinder. Fortunately, as the signal frequency approaches 1 MHz, skin effect will cause most of the current to be concentrated to a peripheral region of a conductor.

For copper, the variation of skin depth with frequency is shown plotted in Figure 5.11. It was observed that as the signal frequency increased, the skin depth was reduced to a little over 2 mils. Therefore, using a filled via or solid vertical connector does not offer any additional benefit. Even though the resistance did increase by about 19% across the frequency range, it is incapable of resulting in a significant voltage drop to cause switching anomalies. In fact, the internal gate resistance of the die under consideration was larger in comparison by an order of magnitude. An array of smaller vias occupying the same area may be considered for further minimizing the parasitic inductance, but the value obtained was sufficient to contain gate voltage overshoots to ultra-low levels.

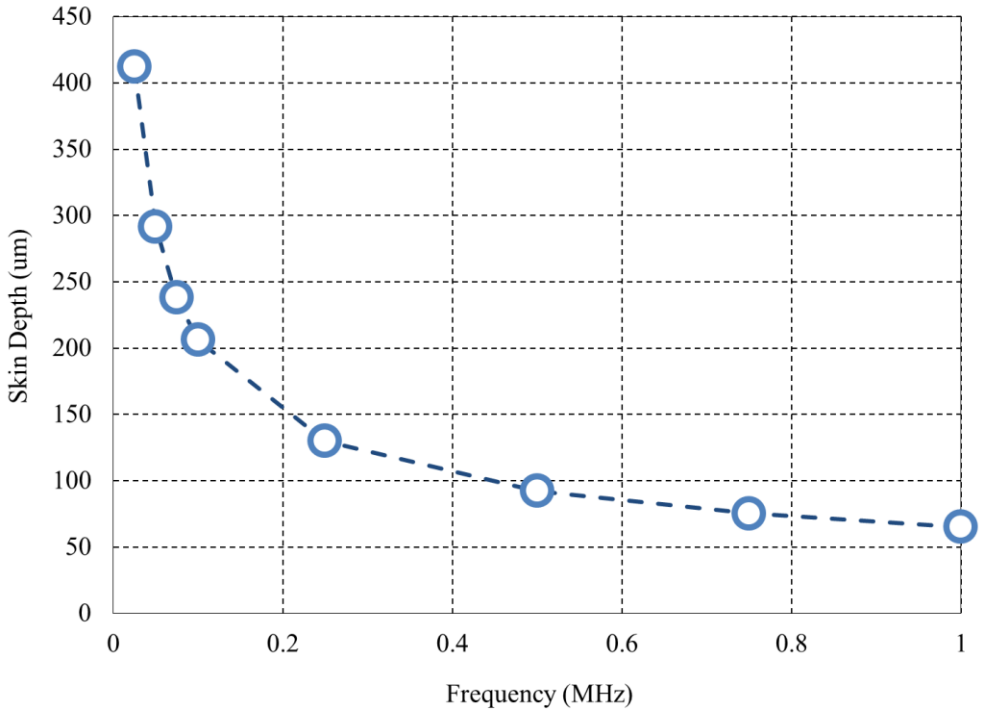
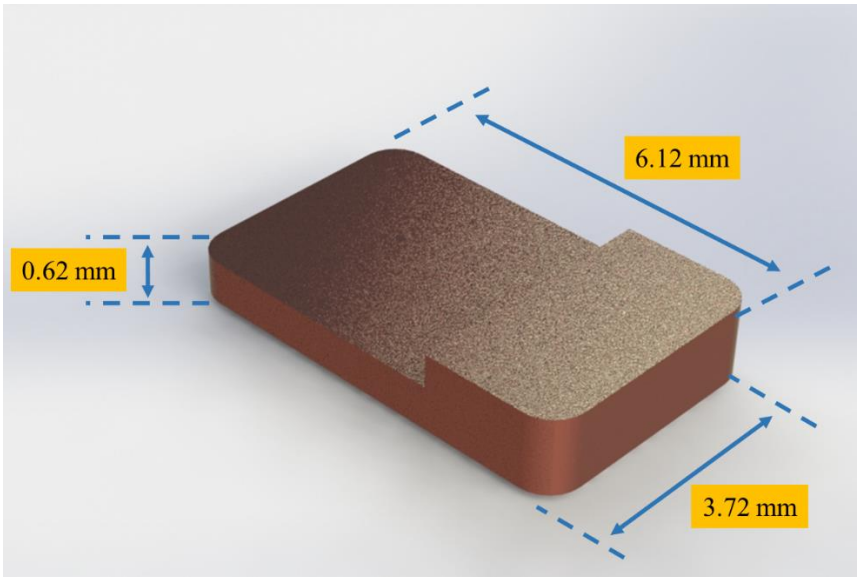


Figure 5.11: A graph showing the variation of skin-depth in copper as a function of the frequency.

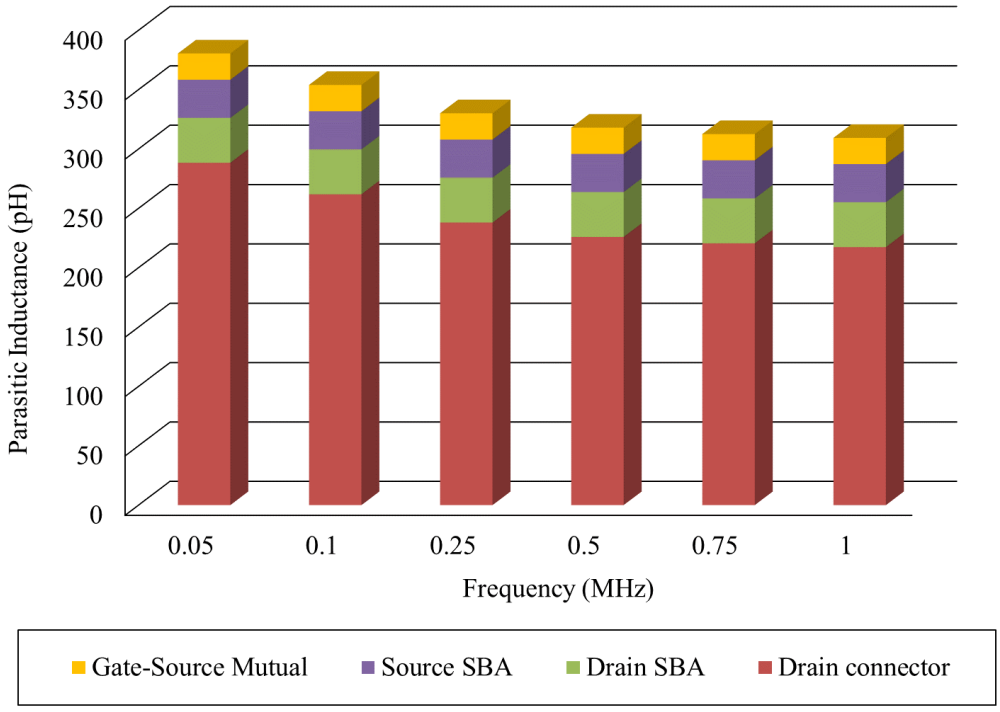
5.3.2: Power loop parasitic estimation

Just as the gate via presents an additional impedance in the gate loop, the drain connector is a source of additional impedance in the power loop. It is imperative to have an estimate of the impedance offered by this additional packaging element, and ascertain whether it could lead to undesirable switching artifacts or voltage drops in the power loop. This case was also simulated in Q3D, and Figure 5.12(a) shows the simulation model and Figure 5.12(b) shows the results of the simulation. The mutual parasitic inductance between the gate-source interconnections was also evaluated, since it manifests itself electrically in series with the source parasitic inductance. The combined parasitic inductance offered by the source solder ball array (SBA), drain SBA, and the mutually coupled gate-source inductance amounts to a little in excess of 350 pH at its maximum. The parasitic resistance for this signal net was also evaluated, and was found to be an order of magnitude lower than the $R_{ds,ON}$ of the MOSFET under consideration. The results were consistent across the entire frequency range of interest.

It was observed that the drain connector added a significant amount of inductance to the power loop. The interconnect inductances due to the solder balls were found to be 10x or lower in comparison across the entire frequency range. This value, however, needs to be put into the proper perspective to realize that it is not a concern. Even in the case of a conventional power module, the signal from the drain needs to be routed along traces presenting comparable parasitics. At a fraction of 1 nH, the inductance offered by the inclusion of the drain connector was not deemed a concern for clean switching waveforms within the power loop. Keeping this connector as long and wide as practically possible implies possible reliability benefits with respect to lower thermal resistance and greater stress relief; that discussion, however, is beyond the scope of this study".



(a)



(b)

Figure 5.12: (a) the model used for the bottom terminal and (b) the inductance estimation results for the power-loop.

The observed parasitic inductances in both the gate and power loops were found to be comparable to the flat sintered silver layer modeled in Chapter 3. It was concluded that using solder spheres did not add appreciably to the parasitic inductance or resistance of the critical switching loops in the circuit.

Conclusions

The concept of the flip-chip power device is highly versatile. It provides the ease-of-assembly of a discrete device and combines it with a performance that potentially exceeds wire bonded devices. Even while using low cost materials like copper, FR4, and solder—the CTE mismatch stresses were far less than a traditional wire bonded module. This was because the solder sphere array expertly cushions and absorbs thermo-mechanical stress. No underfill was modeled during these evaluations to obtain a worst-case estimate. If an even more superior thermal and/or reliability performance is desired, it can easily achieved by upgrading the materials to CTE-matched alternatives at additional cost. For the design evaluation presented in this chapter, the cost was prioritized over exceptional reliability. Despite this fact, the critical stresses in the flip-chip module were found to be far less as compared with a state-of-the-art wire bonded module.

Although the pillar-like solder sphere array provided mechanical relief, the implications of this structure from the viewpoint of parasitics was not intuitively clear. The interconnect parasitics of the proposed scheme were evaluated to check if the physical height and geometry of the solder spheres held the same low-inductance benefits as the flat sintered silver layer in Chapter 3 was demonstrated to have. Additional structures of concern included the through-interposer gate via and the copper bottom connector, and they were included in the respective signal loops. It was found that the results for a flat sintered silver layer were of the same order as the solder sphere array—even while accounting for the aforementioned additional structures.

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CHAPTER 6: The Fabrication Process and Qualification for the Manufacturing of Flip-Chip Capable Power Devices

Section 6.1: Fabrication process leading from a bare die power device to a flip-chip module

The process flow for fabrication of a typical flip-chip power module follows FIVE major steps:

1. Re-metallization of the top pads of the commercial power device in bare die form.

2. Attachment of the re-metallized die to the metallic connector.

3. Solder masking to expose the pads for attaching solder spheres.

4. Attachment of the solder spheres.

5. Flip-chip bonding to a patterned interposer/substrate.

The sequence of the process flow in depicted in Figure 6.1.

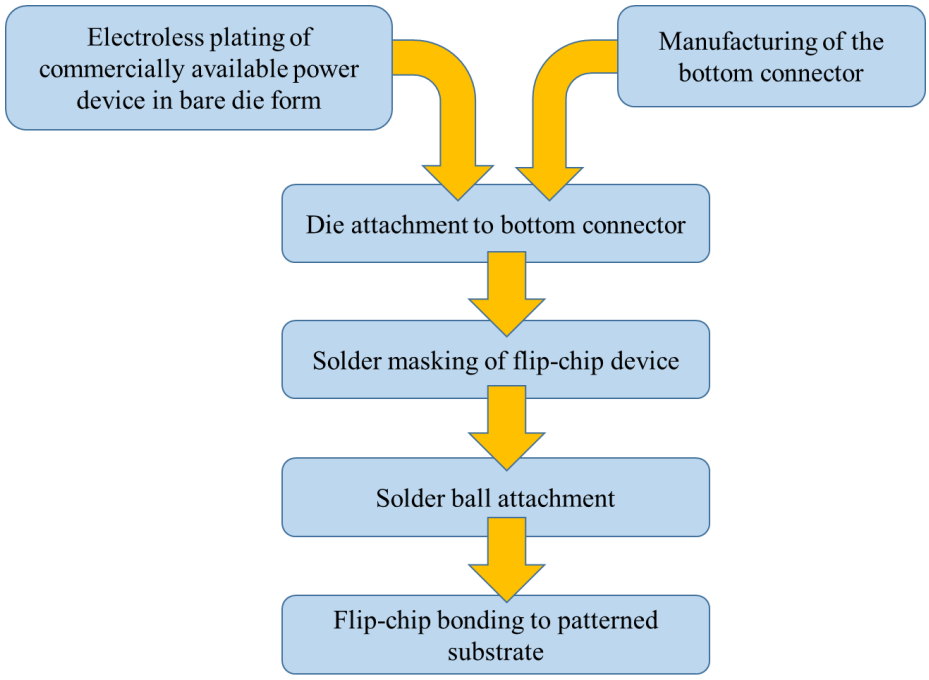


Figure 6.1: A flowchart depicting the process flow for reconfiguring a bare die power device to a flip-chip capable component.

The preliminary step in this process was re-metallization. Commercially available SiC power devices are tailor-made for wire bonding. Hence, the top pads of these devices are aluminum. In order to obtain a solderable finish, an electroless nickel plating process was pursued. An electroless nickel gold (ENIG) finish has been well established as a preferred re-metallization process for aluminum bond pads as evidenced by the literature [1]. A process flow was developed in-house for the re-metallization of commercially available SiC die. A flowchart outlining the developed process is shown in Figure 6.2. It is based largely on the known-good processes reported in the literature [1]. Some process variations were necessary to form a uniform and highly adherent coating, but the underlying philosophy was identical to a standard electroless nickel plating process on an aluminum device pad. The process involved the stripping of the native oxide layer of the aluminum bond pad, followed by the deposition of a very thin zinc adhesion layer. The nickel layer was then deposited atop the zinc layer.

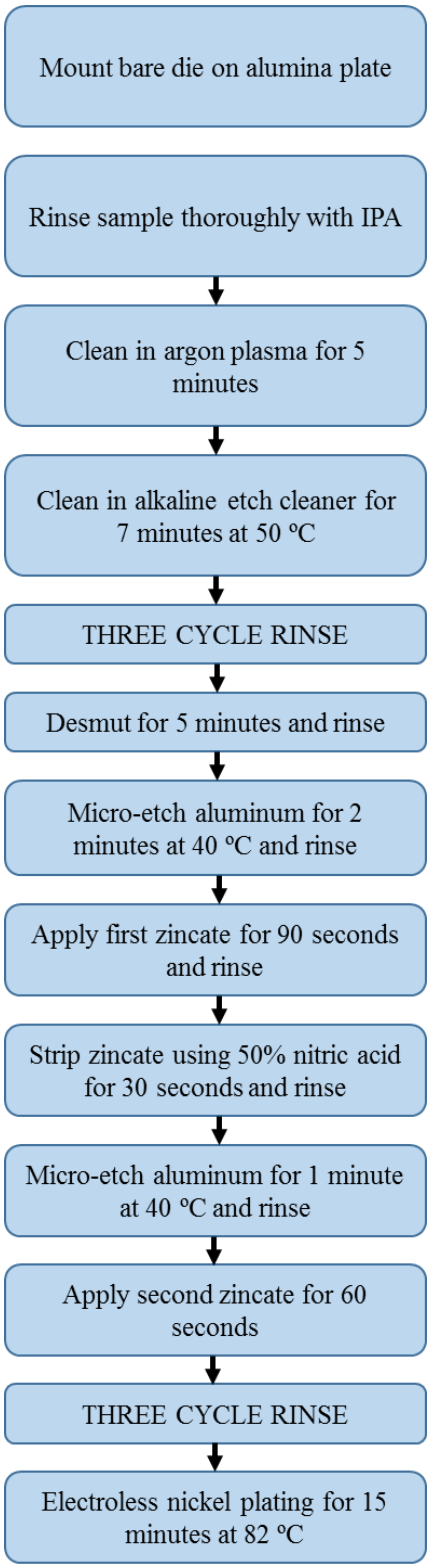
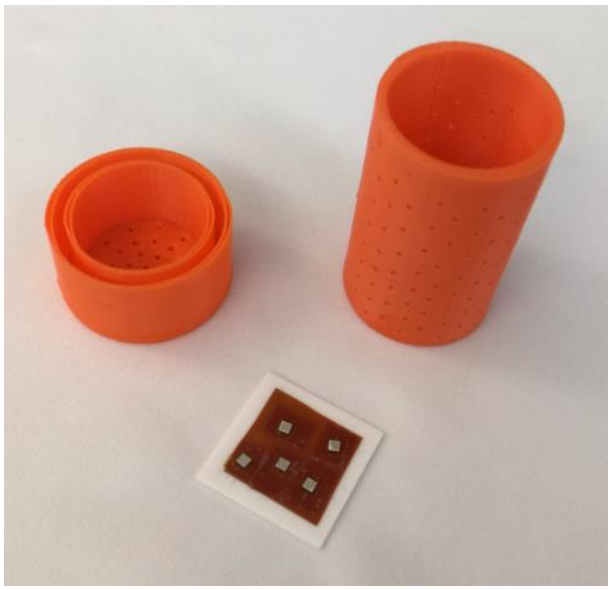


Figure 6.2: A flowchart outlining the re-metallization process developed in-house at the University of Arkansas.

The electroless plating process is preferable to conduct at a wafer level. However, due to high cost of SiC wafers, the process development was conducted on die. A dip-basket was 3D printed to cycle multiple chips through the electroless plating baths. The dip-basket had a lid and perforations on all sides to allow the plating solutions to pass freely. Multiple chips were secured to an alumina plate using double-sided Kapton tape. This not only allowed the processing of multiple samples at a time, but it also allowed the masking of the bottom terminal of the SiC power devices. The bottom contact is already plated with a solderable silver finish and needs to be protected from the electroless process for the top side. Figure 6.3(a) shows a photograph of the 3D printed dip basket and a batch of SiC die mounted on an alumina plate using double-sided Kapton tape. Figure 6.3(b) shows an optical microscope image of the thin zinc layer on the top pads of a bare die ROHM MOSFET. The probe marks on the gate pad were still visible after zinc deposition. Figure 6.3(c) shows the optical microscope image of the final thick nickel layer, and the probe marks can no longer be observed as a result. An interesting feature of choosing electroless plating was the self-patterning nature of the process. No additional photolithography (or masking) step and lift-off process was required—thus reducing the cost and complexity of the process. As can be observed in Figure 6.3(b) and (c), no dendritic formations or conductive bridges were found after the metallization steps were completed. After the metallization step, the Kapton tape was gently removed using isopropyl alcohol and a pair of tweezers and the sample was thoroughly cleaned to remove organic residues.



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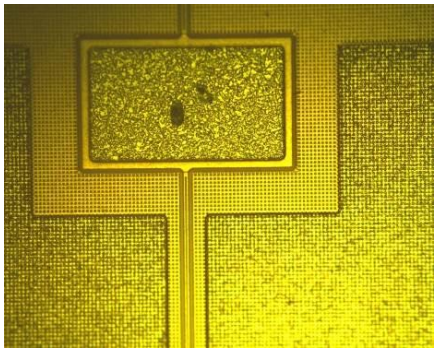

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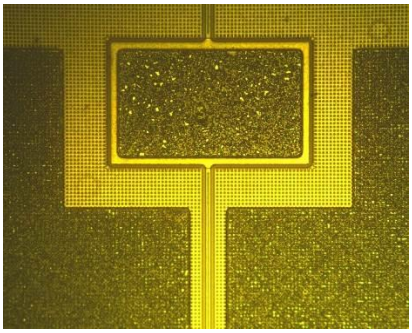
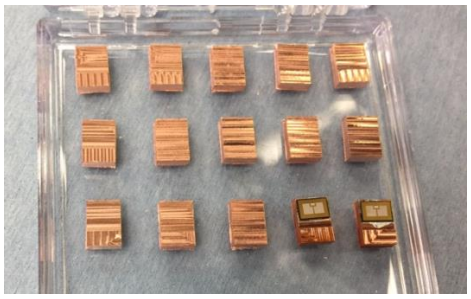


(c)

Figure 6.3: Photographs showing (a) the 3D printed dip-basket for electroless plating, (b) the thin zinc seed layer on the aluminum bond pad, and (c) the thick final layer of nickel.

The next step in the process involved the attachment of the re-metallized die to the metallic connector. The material chosen for the bottom connector was copper for reasons cited in a previous section. The connector was milled out of a 1.5 mm sheet of copper. The parts were milled on a CNC machine as shown in Figure 6.4(a). A couple of samples are shown with die attached to them for a comparison of size. The die attach material was SAC305 solder with a peak reflow temperature of 249 ºC. This was to maintain a suitable solder hierarchy since the maximum reflow temperature of the solder spheres was around 225 ºC. A stencil fashioned out of a Kapton sheet was used to hold the die in place during solder reflow. A photograph showing this setup is shown in Figure 6.4(b). A Sikama zone reflow oven was used for the die attachment process, and Figure 6.4(c) shows a photograph with the temperatures for each of the stations (or zones). The soak times in each zone were assigned to be 90 seconds. The values of temperature and soak time need to be optimized based on the material of the solder and the thermal resistance offered by the substrate. This was achieved by studying the reflow behavior of SAC305 paste on a dummy FR4 board mounted on a hot plate with respect to temperature and soak time.



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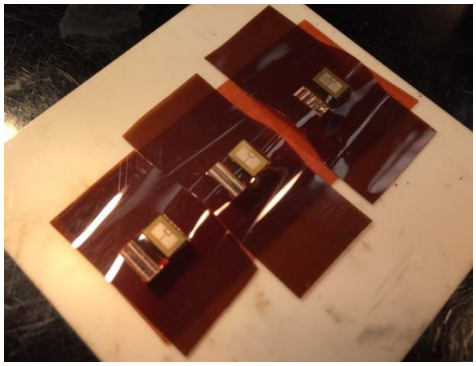


(b)

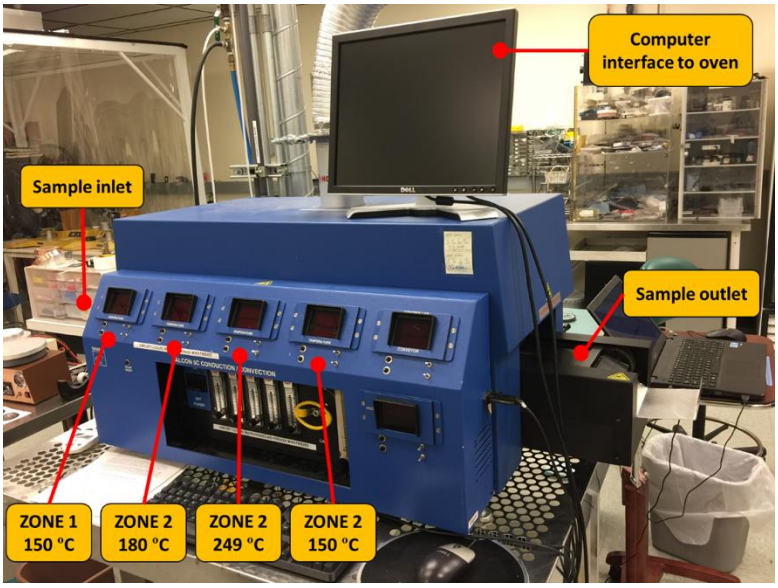


Figure 6.4: A photograph showing (a) a batch of CNC milled copper bottom connectors, (b) the process for die attachment using Kapton film fixturing, and (c) a photograph showing the Sikama belt reflow oven with the different zones.

The chip-and-connector assembly was solder-masked using a UV-patternable dry film solder resist. The part number of the dry film solder resist was Dynamask® 5000 series from Rohm and Haas Electronic Materials LLC. The procedure for solder masking, exposure, and development can be found on the vendor's website. The prescribed process was strictly adhered to, with the exception of the exposure time. The exposure time varies with the intensity of the UV light source and was optimized for the source used for this study. The dry film was laminated on to the surface of the chip-scale package using a desktop thermal laminator. A photolithography step was conducted on the sample through a mask containing the solder ball array pattern. Upon development, pads were exposed on the package surface designating the position of the solder spheres. The developer was a 10% solution of baking soda in de-ionized water. The sample was cured under ultraviolet (UV) light to complete the solder masking process. The photolithography process for the solder mask had to be optimized for exposure time. The development time was kept fixed at 6 minutes. It was found that a 20 second exposure time yielded the desired 12 mil opening. Using a larger exposure time over-exposed the solder masked and constricted the bond pad openings. The results of this process development are presented through a series of photographs in Figure 6.5.

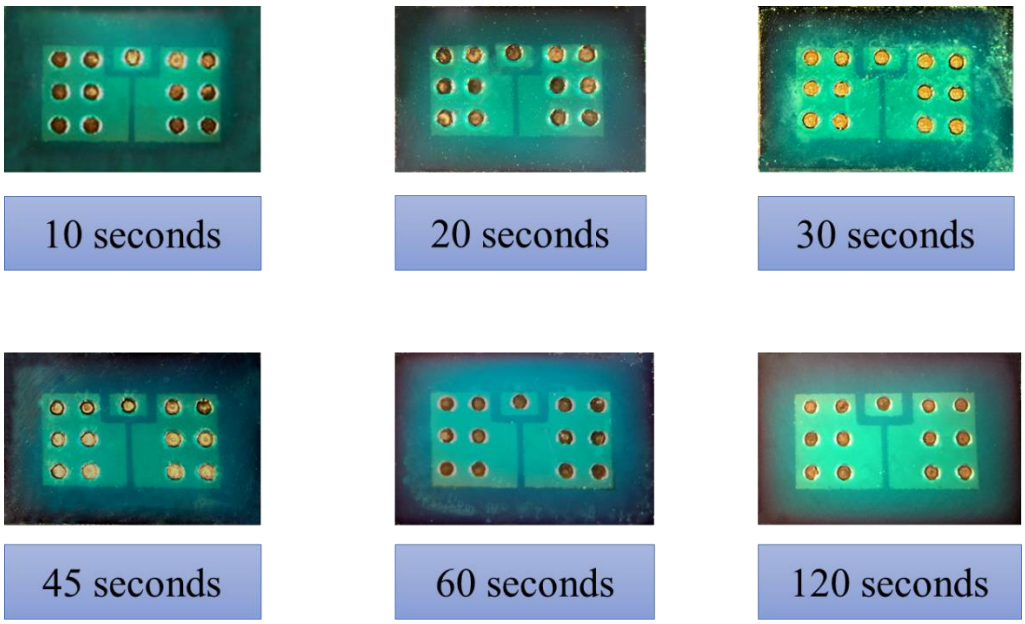
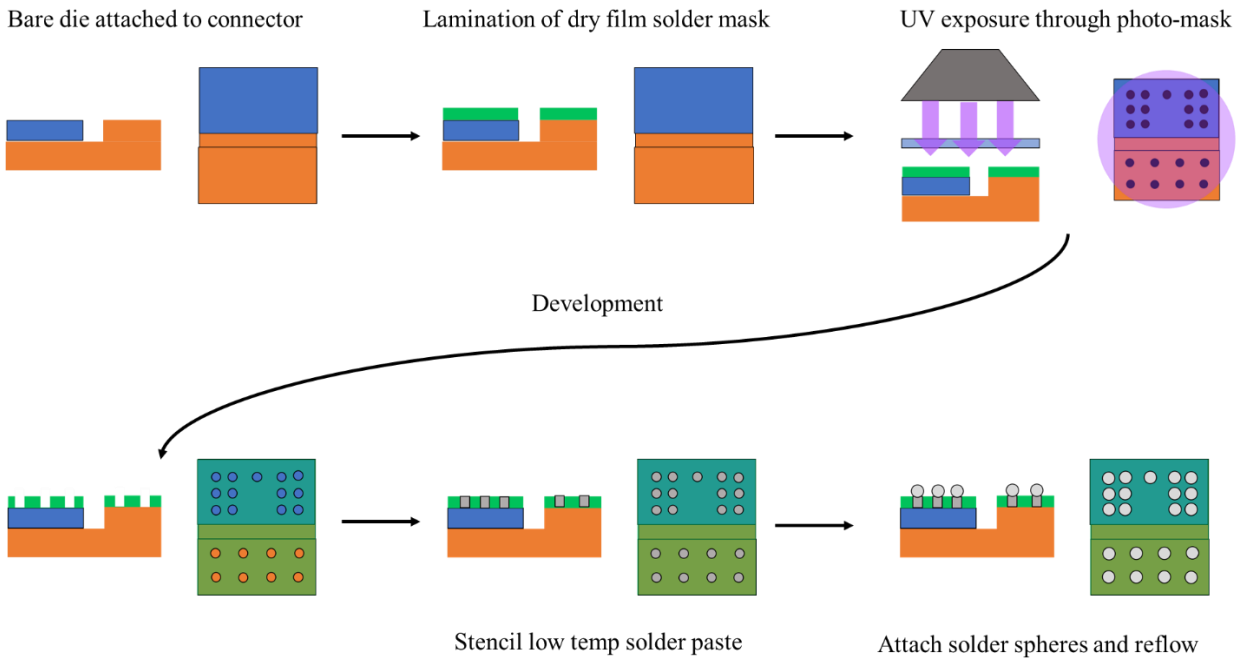


Figure 6.5: The process development for exposing pads on the solder mask.

Solder sphere attachment was the next step of the process. A squeegee was used to stencil solder paste into the circular open pad areas on the chip scale package. 15 mil solder spheres were hand-placed on to the wet solder paste. The assembly was reflowed in a Sikama reflow oven. The melting temperature of the attachment solder paste was lower than the solder spheres. Hence the spheres retained their shape but attached securely to the bond pads on the chip-scale package. The process flow is described in the schematic shown in Figure 6.6(a). The reflow step for the ball-attachment was accomplished using a Sikama zone reflow oven. The melting temperature of the low-temperature solder used for ball attachment (Sn42Bi58) was around 160 ºC, with a prescribed reflow time of 60-80 seconds. However, process optimization using this solder paste revealed that 170 ºC for 90 seconds was a satisfactory dwell time and temperature for the process. A photograph of the reflow oven with the temperatures of the various zones is presented in Figure 6.6(b).



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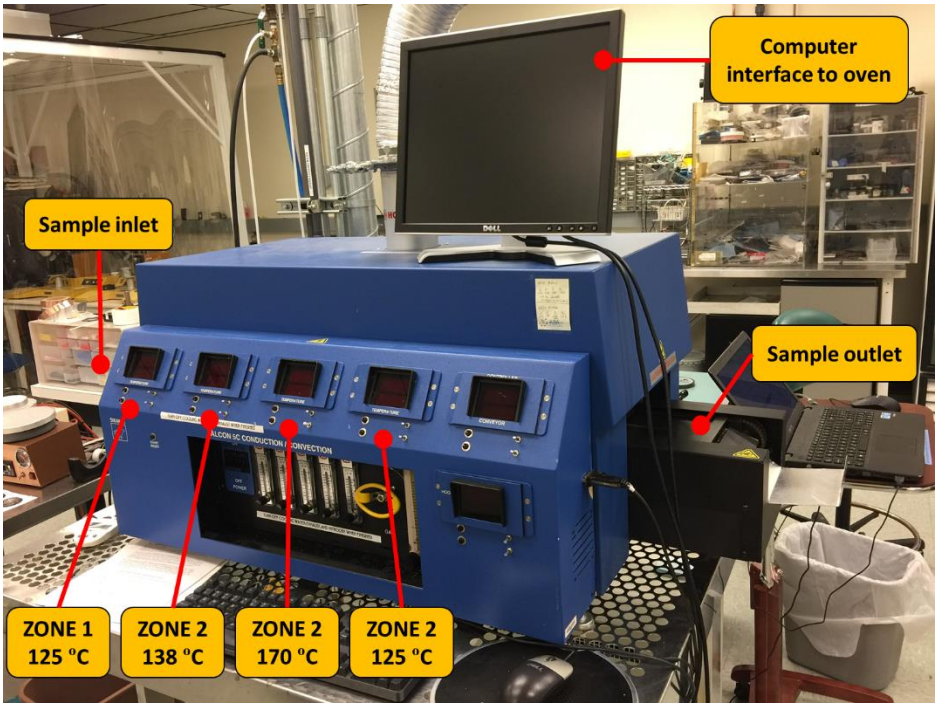


(b)

Figure 6.6: A schematic depicting the process flow for the solder masking step.

The assembly was now capable of being flip-chip bonded on to a substrate with matching bond pads, much like a discrete MOSFET. However the footprint of this device is approximately 14× smaller as compared with a discrete TO-247 device. Figure 6.7 shows a photograph comparing the two packages to illustrate this fact.

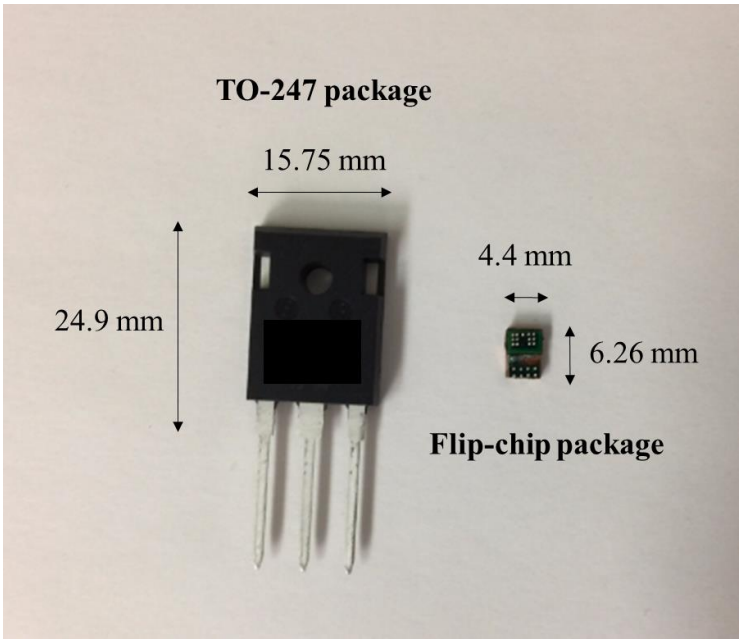


Figure 6.7: A photograph of a ball-bumped sample alongside a TO-247 MOSFET package for comparison.

The final step in the fabrication process was the flip-chip attachment of the chip-scale package on to matching pads on a substrate/interposer. As stated before, FR4 was used as the interposer material since it provide a versatile-yet-inexpensive platform for the demonstration of the key benefits of this technology. The substrate was patterned with the same solder mask, and the openings for the bond pads matched the pattern of the solder sphere array. A Finetech Fineplacer flip-chip bonder was used for both die placement and reflow and a labeled diagram depicting the same is presented in Figure 6.8.

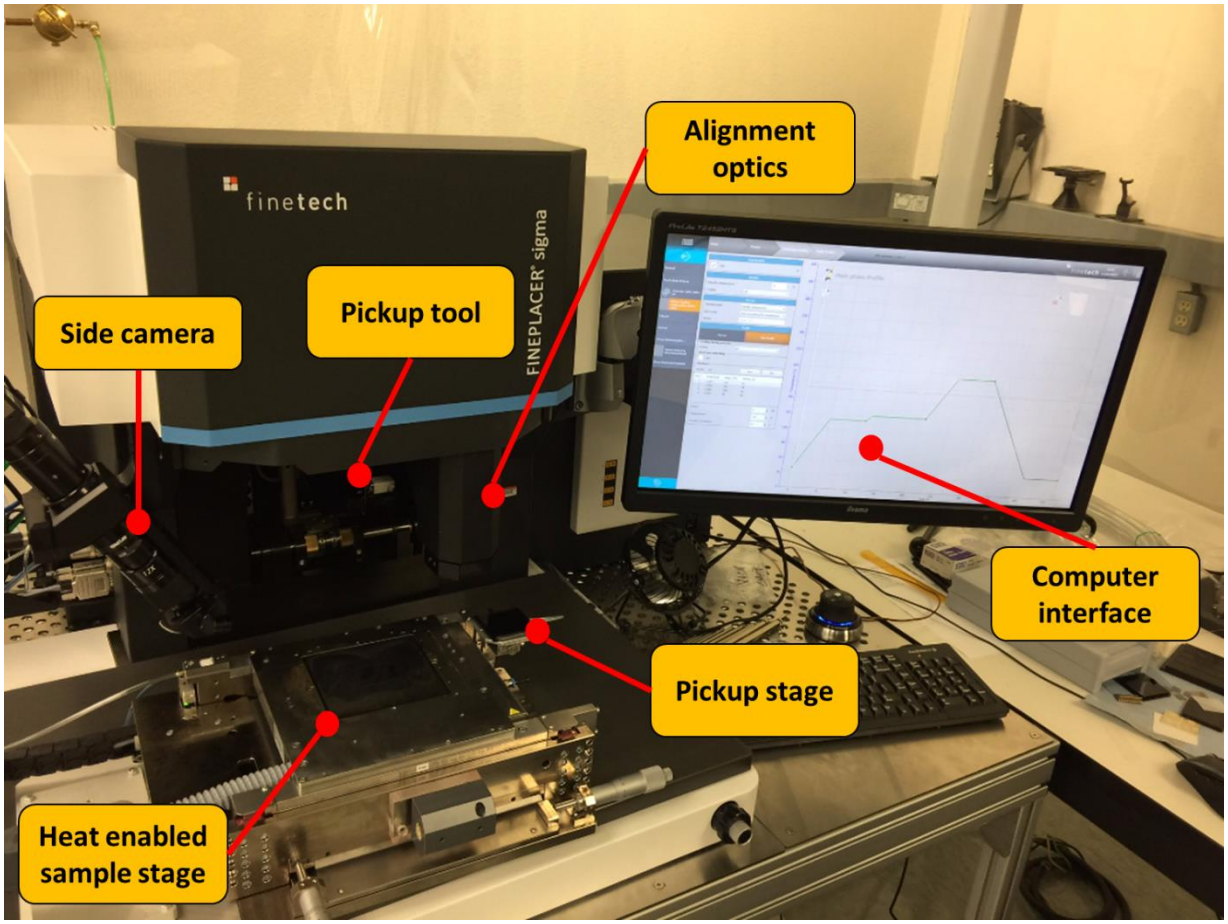


Figure 6.8: A labeled photograph of the Finetech Fineplacer.

Section 6.2: Process Qualification

There were three aspects of the re-metallization process which needed to be qualified before proceeding:

1. Adhesion of the newly applied metallization

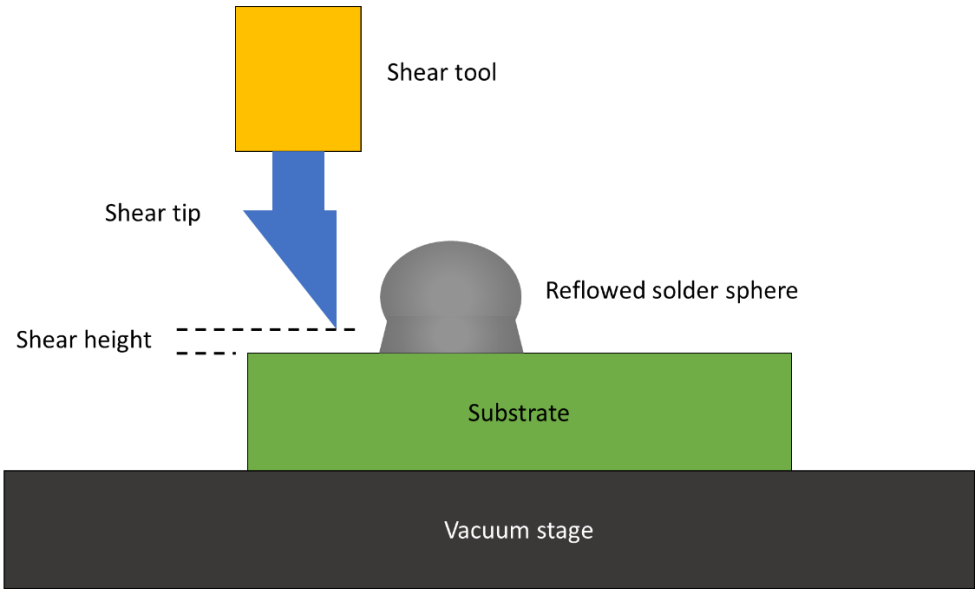
2. Strength of the flip-chip bond

3. Contact resistance of the newly applied metallization

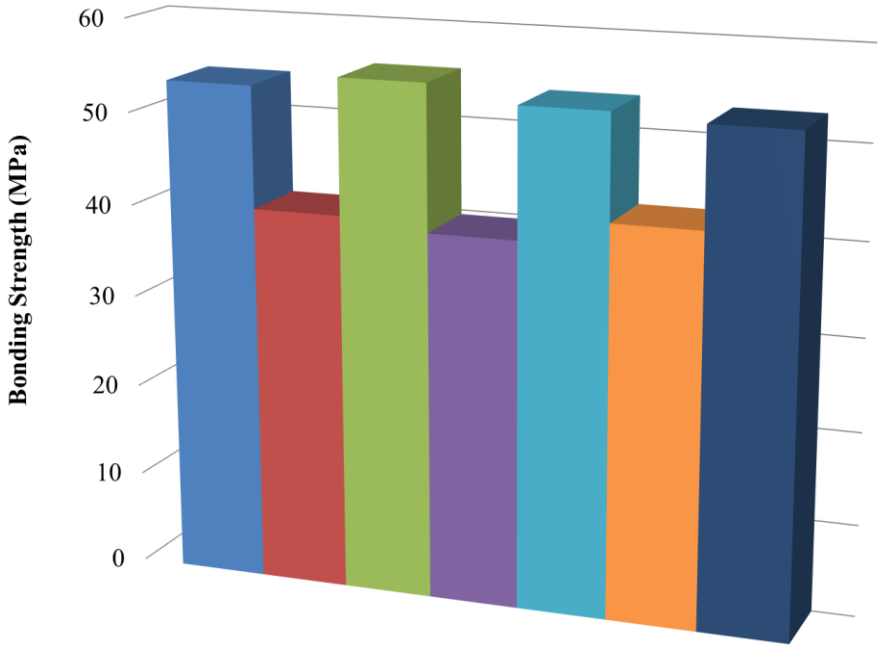
6.2.1: Qualification of metallization quality

To address the first concern, solder spheres were reflowed on multiple pad locations on a re-metallized power device as shown in Figure 6.9(a). A ball-shear test was conducted on the solder spheres to test the adhesion of the metallization, as well as the strength of the solder ball joint. This would give an indication of the metallization quality and whether solder was wetting the metallization adequately. The ball shear test process is described in the schematic shown in Figure 6.9(b). The results of the die shear test are presented in Figure 6.9(c). The principal failure mode in the solder spheres occurred as a result of the die-shear tip flattening the solder spheres. These observations were indicative of excellent adhesion for the metallization as well as the solder spheres. A photograph documenting a set of flattened solder joints after the test is shown in Figure 6.9(d).

(a)


Shear tool
Shear tip
Reflowed solder sphere
Shear height
Substrate
Vacuum stage

(b)



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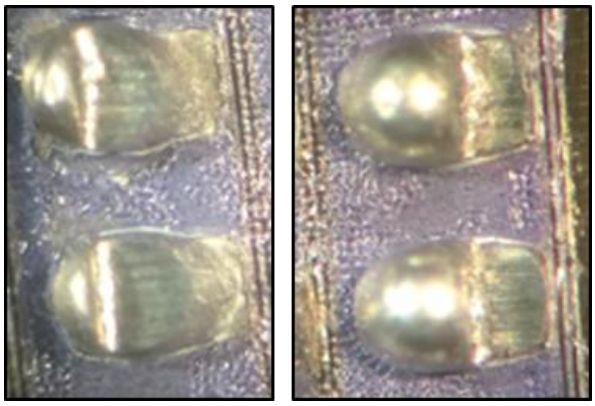
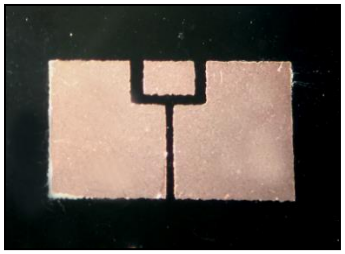


(d)

Figure 6.9: The metallization qualification tests showing (a) the solder ball bumped die sample, (b) a schematic representing the ball-shear test, (c) a bar graph documenting the bonding strength of multiple samples, and (d) a photograph showing the solder spheres in various location flattened by the die-shear tip.

6.2.2: Qualification of the bonding strength of the flip-chip bond

The second qualification was for evaluating the bonding strength for the flip-chip attachment. For this process, a set of silicon dummy die were fabricated. The copper metallization on the top surface of the silicon was patterned according to the gate and source pad pattern of a commercially available bare die from ROHM Semiconductor (S2301UCSF). The patterning was achieved through a combination of photolithography and chemical etching of copper. The resulting dummy die was solder masked and developed according to the procedure described in Section 6.1. The solder spheres were attached to the exposed pads using low temperature solder. The whole procedure leading to the solder sphere attachment has been described pictorially in Figure 6.10. The solder spheres were adequately spaced out so that they did not contact each other and coalesce during reflow. While designing the pitch within such constrained pads it must be noted that the solder spheres collapse into oblate spheroids during reflow.



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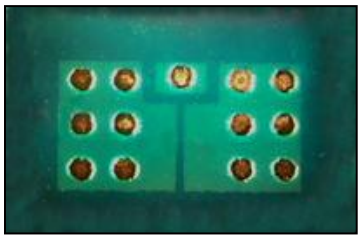

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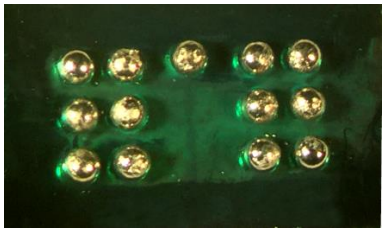
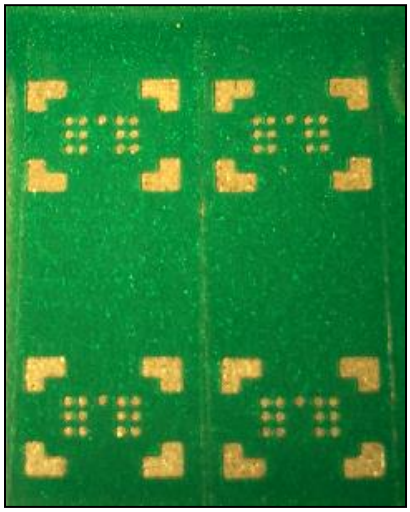


(c)

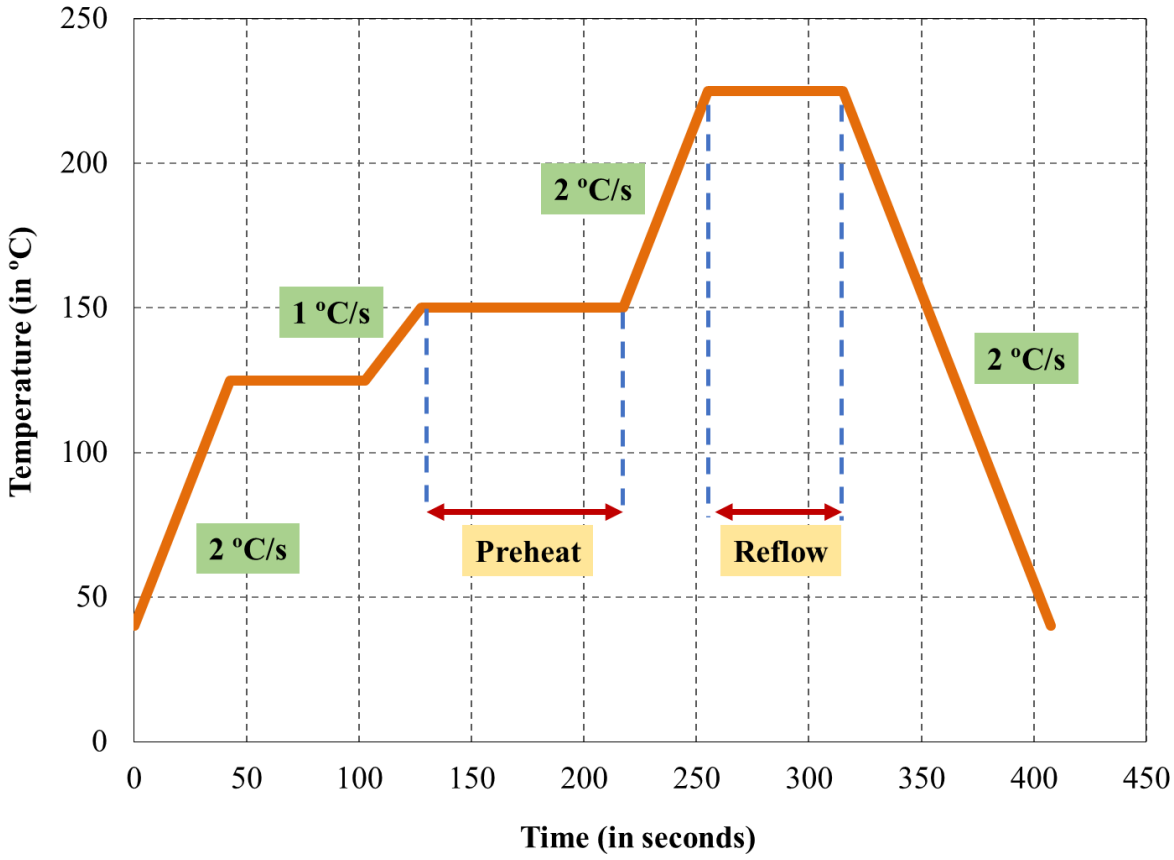
Figure 6.10: A pictorial representation of the ball-bumping process showing (a) the bare die dummy die, (b) The solder masked dummy die with bond pads exposed, and (c) the ball-bumped sample.

Flip-chip attachment was the next step in the process. Test substrates were fabricated by solder masking and patterning matching bond pads. Each test coupon contained pads for attaching multiple samples as shown in Figure 6.11(a). The ball-bumped samples were flip-chip bonded on to the substrates and reflowed according to the profile shown in Figure 6.11(b). A lateral view of the collapsed solder spheres and attached die is shown in Figure 6.11(c). It was observed that the die was parallel to the surface of the substrate and no electrical shorting was immediately apparent. To verify that the interior solder-spheres were not bridged, a scanning acoustic microscope (SAM)

was used. Figure 6.11(d) shows a SAM image of the assembly. It was observed that all the pads were distinct and there was no bridging between the interior spheres either.



(a)



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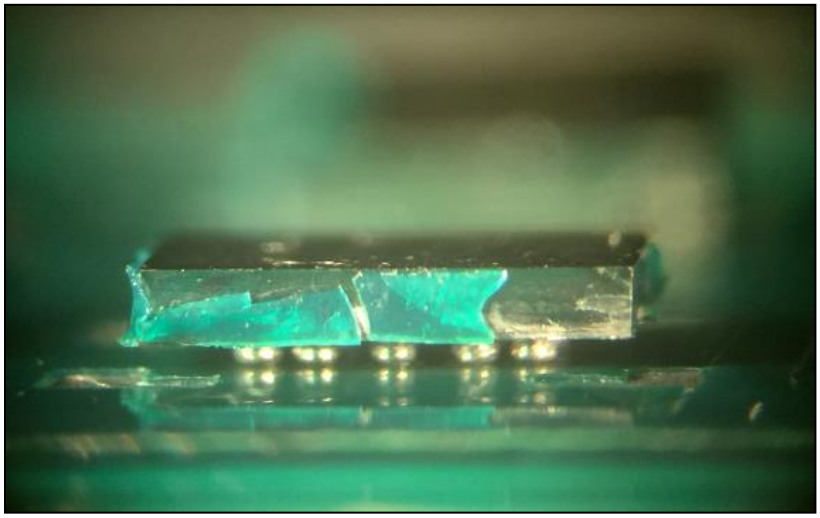

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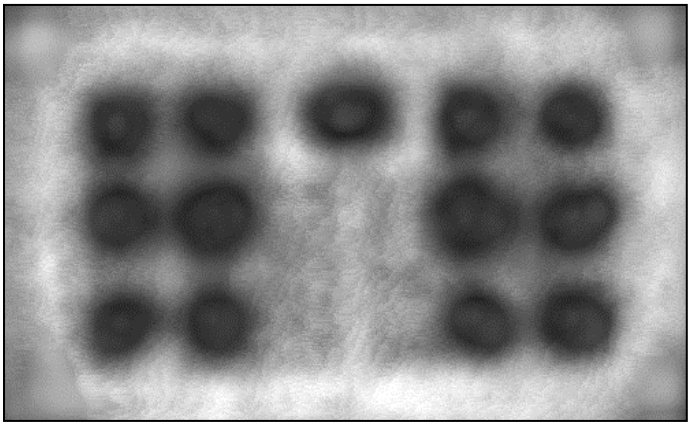


(d)

Figure 6.11: Photographs showing (a) a patterned test substrate, (b) the thermal profile used for reflowing the solder spheres, (c) a side-view of the flip-chip bonded sample, and (d) a SAM image of the same showing a short-free bond.

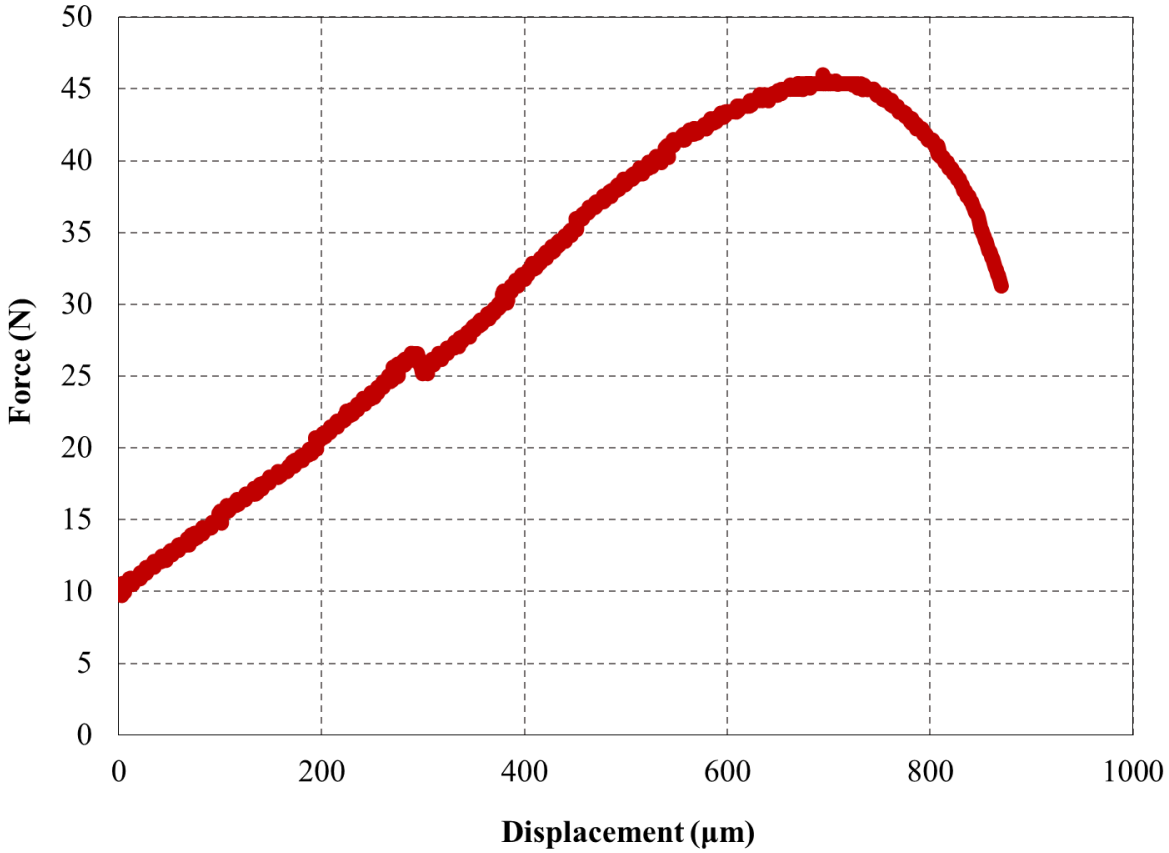
The bonded samples were subject to a die shear test to test the bonding strength. The result of the die shear test is presented in Figure 6.12. Figure 6.12(a) shows the force vs displacement curve of a typical sample. The peak force in the graph indicates the break point of the bond. The 45.992 N break point corresponds to a bonding strength of 48.51 MPa. This value was derived by dividing

the total bonding force by the total surface area occupied by the 13 solder spheres. The solder sphere array provided a distributed pillar-like effect in bolstering the bonding strength of the die to the substrate. A photograph showing the failed sample is shown in Figure 6.12(b).

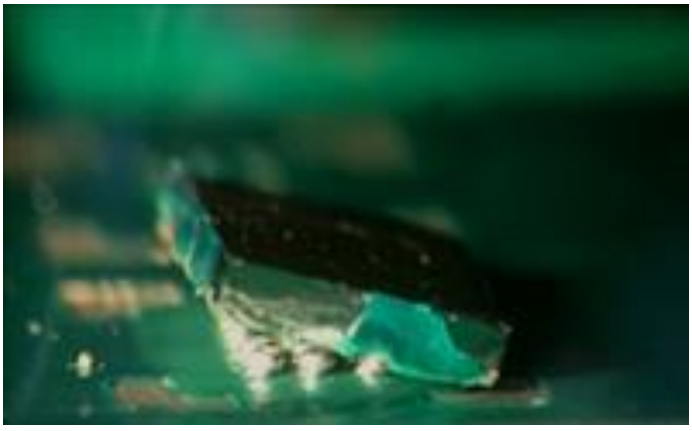
The bonding strength of the assembly was contrasted with the pull test result conducted in a wire bonded die. After the pull test was complete, the foot of the wire bond adhering to the die (or substrate) was also sheared. During the pull test it must be ensured that the feet of the wire bond remain firmly bonded to the die and substrate, while the bond wire breaks somewhere in between the feet. This is an indication of a well-bonded wire bond. Although a high bonding strength is not sufficient condition to prove superior long term reliability, it is one of the necessary conditions. Figure 6.12(c) shows a comparison of the strength of the flip-chip sample compared with the pull test strength and bonding strength of the foot of a wire bond. The bonding strength of the solder sphere array was found to be higher by 1-2 orders of magnitude. The pull test yielded an average strength of 0.328 N and the bonding strength of the wire bond foot was found to be 8.265 N on an average.

The bonding strength was also evaluated as a function of temperature by shearing off samples at set temperatures on the heated stage of the die shear tester. Elevated temperatures served to accentuate the CTE mismatch at the interfaces of the solder spheres. Figure 6.12(d) shows the result of this test. It was observed that temperatures up to 125 ºC had negligible effect on the bonding strength of the samples. However, the bonding strength showed a sharp decline at 150 ºC. The melting temperature of the solder spheres was 183 ºC according to the manufacturer's specifications, and it was likely that the solder had started softening at 150 ºC. If operation above 125 ºC is desired, the material of the solder must be reconsidered. A survey of solder sphere

manufacturers revealed that high temperature solder spheres were readily commercially available and would not be a limit in realizing a high-temperature variant of this packaging scheme.



(a)



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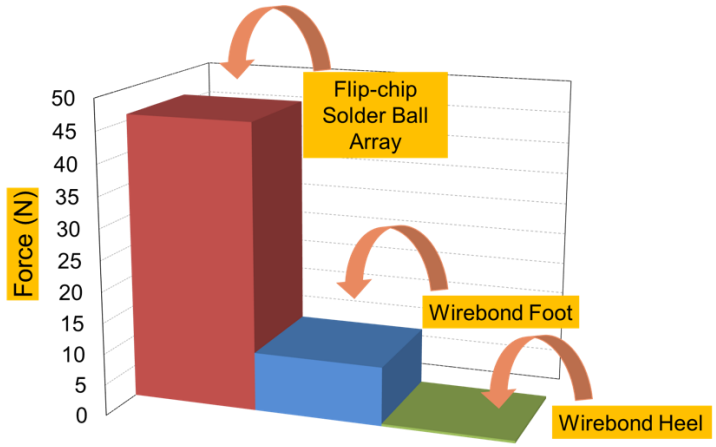

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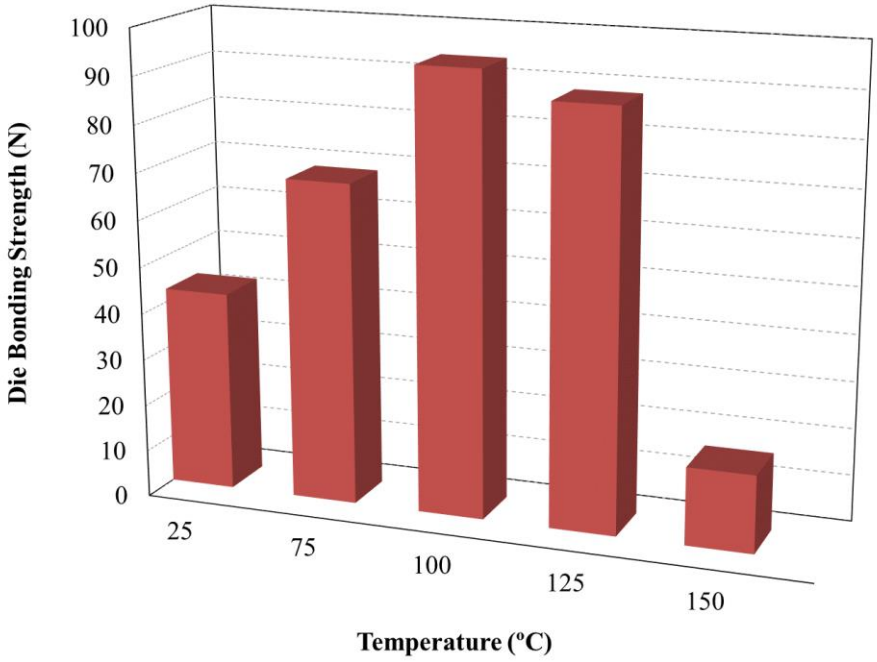


(d)

Figure 6.12: The results of the die shear test on the samples showing (a) the force-displacement curve and (b) variation of the bonding strength with temperature, (c) a comparison with the bonding strength of a wire bond, and (d) a photograph showing the chief failure mode.

6.2.3: Evaluation of the device contact resistance after plating

The third and final check was to ensure that the re-metallization process did not add electrical resistance to the top contacts of the bare die power device. For this purpose, the forward characteristics of two bare die power transistors were compared on a probe station using a curve tracer. One of the die was re-metallized using the processes described in an earlier section. It was observed the forward characteristics of the plated and pristine devices were identical. No significant increase in the contact resistance was observable as a result of the plating process. The forward I-V curves for the measured devices are presented in Figure 6.13.

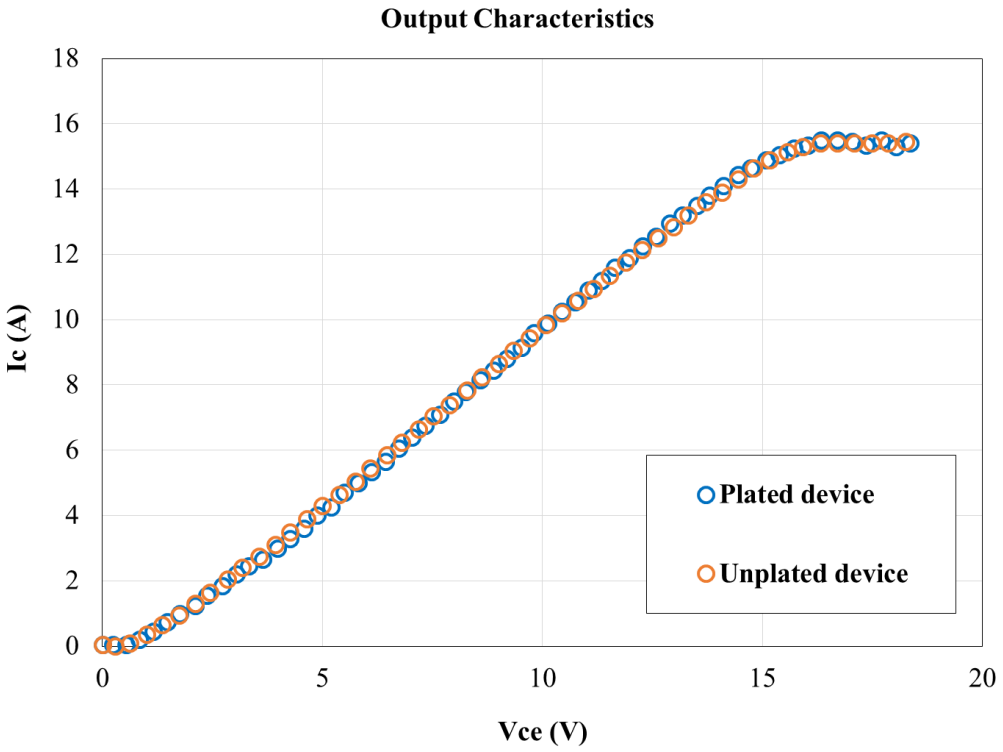


Figure 6.13: A plot comparing the I-V curves of a plated and un-plated power device.

In the previous chapter, the process flow and parasitic benefits for a flip chip power device was illustrated. In this chapter, a functional power device is subject to the process flow and electrical testing to verify the feasibility of realizing the proposed package architecture. The goal was to

develop a wire bondless flip-chip Schottky diode package starting with a bare die device. The manufactured package was evaluated for electrical functionality and compared with a wire bonded module.

6.2.4: The flip-chip Schottky diode package

A) Concept and parasitic estimation:

The device selected for this application was the 650 V-rated SBD from ROHM Semiconductor in bare die form. The part number of the device is S6203TCSF, and it measures 2.3 mm × 2.3 mm. As the simulation results predicted in Chapter 5, using a copper bottom connector and FR4 substrate was a viable approach for prototyping this novel architecture. The die was attached to a copper base connector, solder masked, and solder ball bumped in accordance with the processes described in Section 6.1. This enables the creation of a flip-chip capable component form a bare die power device, which was initially tailored for wire bonding. The major manufacturing steps are outlined in Figure 6.14.

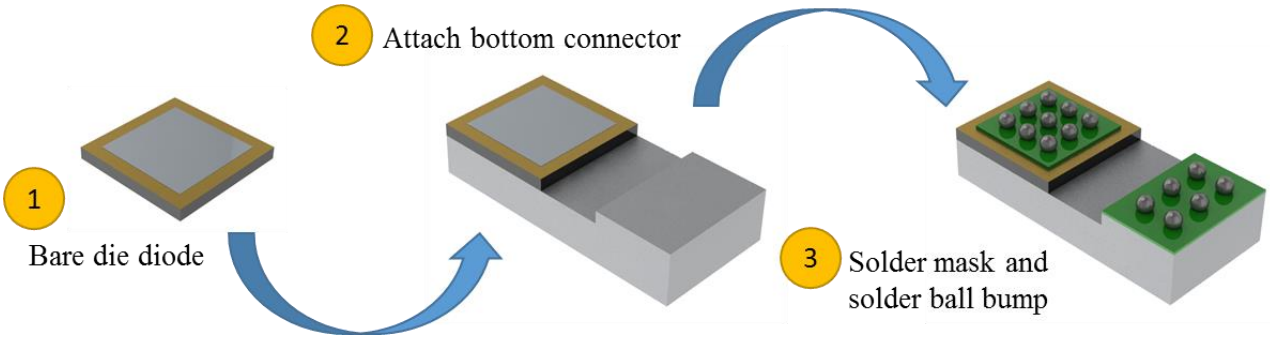
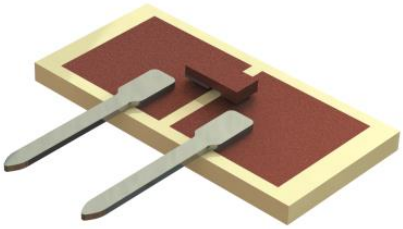


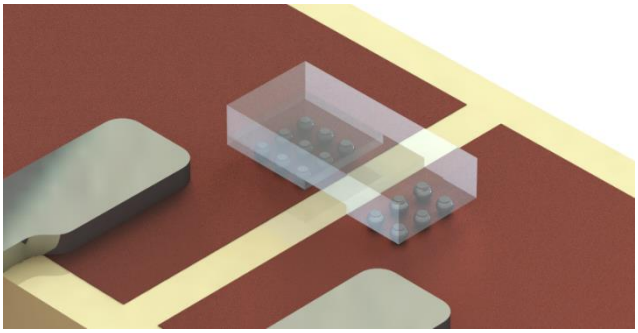
Figure 6.14: The major manufacturing process steps for obtaining a flip-chip capable SBD starting with a bare die.

The second step in the process was to pattern a matching substrate for the flip-chip SBD. This substrate was required to have a matching land pattern with the solder sphere array of the SBD and pads to facilitate electrical probing. The concept design of the test coupon is shown in Figure 6.15.

Figure 6.15(b) shows a close-up of the test structure the diode structure rendered transparent to easily view the solder sphere array. The substrate used was copper-clad FR4 lamina The solder mask is not shown in the renderings. TO-247-like terminals were attached to the test structures so that the devices could be evaluated on a curve-tracer. In addition tom the flip-chip module, a wire bonded SBD package was also fabricated and a rendering of the same is presented in Figure 6.15(c). Two wire bonds of 5 mil diameter were used for the top-side connection to the bare die device. It is to be noted that the same bare die SBD (S6203TCSF from Rohm Semiconductor) was used for both modules. The sizes of the packages and the lead lengths were identical, with the only difference being the interconnection scheme.



(a)



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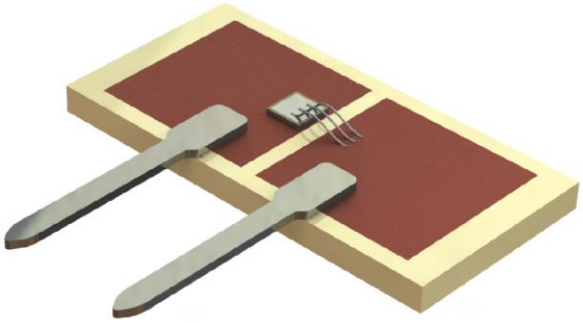
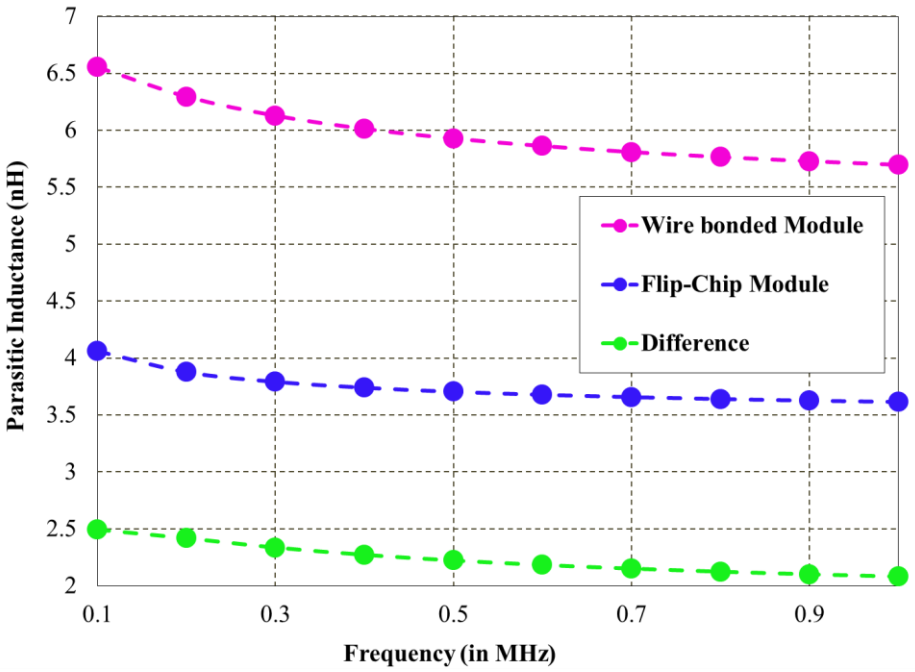


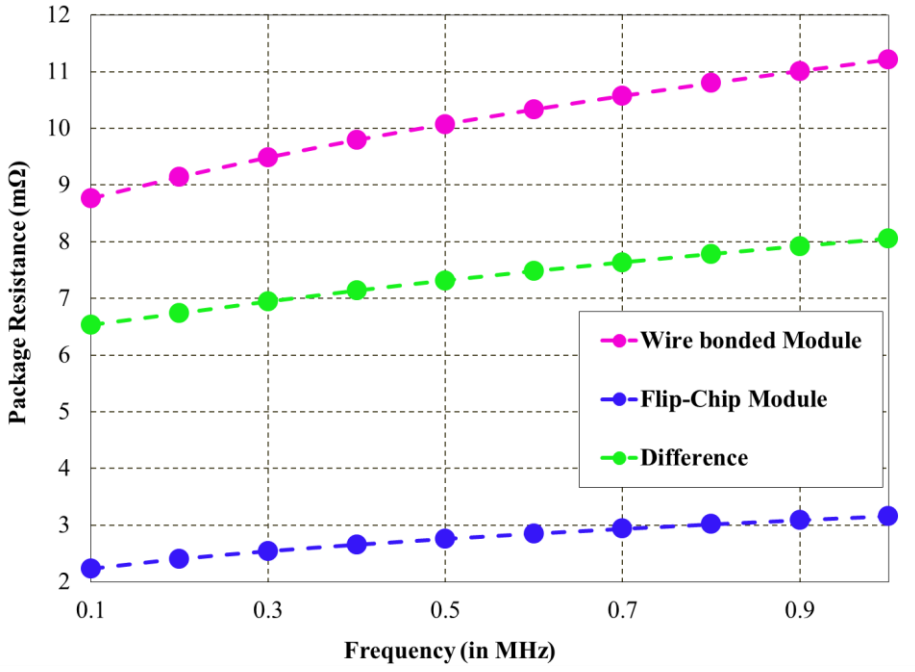
(c)

Figure 6.15: Renderings showing (a) the wire bondless flip-chip SBD package, (a) a close up view showing the placement of the solder sphere array, and (c) a control module containing a wire bonded SBD.

To gain an estimate of the scale of benefits achieved by a simple change to a flip-chip wire bondless package, parasitic simulations were conducted in ANSYS Q3D. A short segment of the package lead was considered since the device would be fitted in a through-hole pad and soldered as close to the body of the package as possible. This helps eliminate the effect of the lead as far as practicable. The parasitic inductance and resistance of the two packages were evaluated as a function of signal frequency, and the difference between the two was also plotted in the respective graphs. From Figure 6.16(a) it was observed that the difference in the parasitic interconnect inductance even for a single device package was over 2 nH. Though this may not seem like a significant difference, it must be note that this is a single-device package with a very short current loop. The effect is much more significant for systems containing multiple die and larger signal loops, as will be presented in due course. Similarly the parasitic resistance of the flip-chip module was up to 8 mΩ lower than the wire bonded module [Figure 6.16(b)]. The difference in the package resistance was significant since it implied that using a flip-chip device would lead to 24% lower conduction losses.



(a)



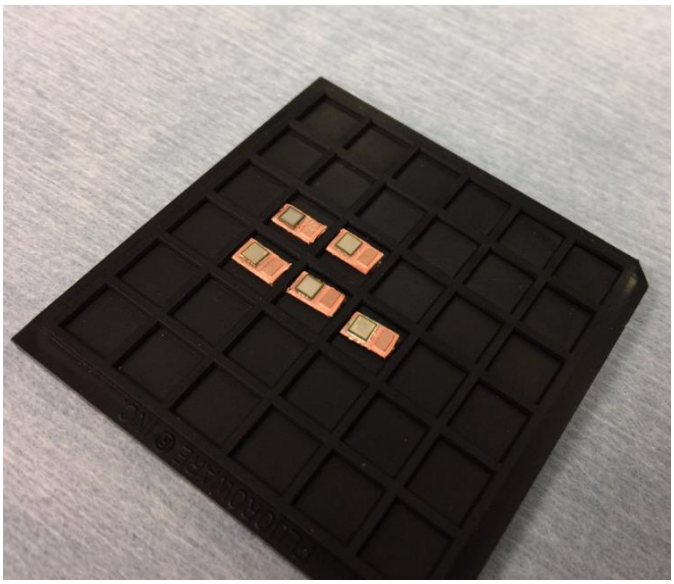
(b)

Figure 6.16: Estimation of the parasitic inductance and package resistance offered by the two packages showing (a) a plot comparing the parasitic inductances as a function of the frequency and (b) a plot comparing the package resistances as a function of the frequency.

B) Manufacturing of the samples:

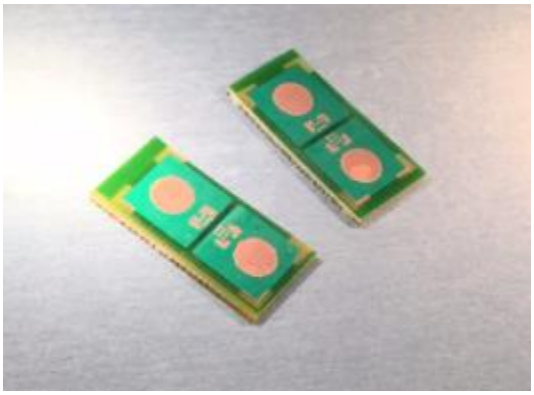
To verify the above predictions, a batch of flip-chip Schottky diode packages were manufactured in accordance of the processes described in Section 6.1. Photographs illustrating some of the process steps are presented in Figure 6.17. The samples were electroless-plated to have a solderable nickel surface finish, and soldered to a milled bottom metallic connector using SAC305 solder paste as shown in Figure 6.17(a). They were solder masked and solder ball-bumped as a next step. For the substrates, a copper-clad FR4 laminate board was patterned using a combination of photolithography and wet chemical etching of the unwanted copper areas in a Chemcut Spray etcher. The patterned coupons were then diced to form coupons as shown in Figure 6.17(b). The coupons were also solder masked and patterned using an identical process as the die. A photograph showing a batch of masked and patterned coupons is shown in Figure 6.17(c). Flip-chip bonding was achieved using a Finetech Fineplacer flip-chip bonder as shown earlier. The top vacuum enabled arm of the bonder was used to pick up the chip-scale SBD package, while the substrate was vacuum mounted on the bottom heated stage. The pads of the substrate were pre-wet with Pb63Sn37 solder paste prior to mounting to aid wetting. The flux present in the solder paste would also help remove any remaining copper oxide and impurities on the surface of the substrate pads. After the solder sphere array was aligned with the bond pads on the substrate, no clean tacky flux was applied on the surface of the land pattern. This would ensure that the placed part would not readily move with minor mechanical displacements and perturbations during the placement and reflow process. Figure 6.17(d) shows the placement process, where the top arm of the flip-chip bonder placed the chip-scale SBD securely on the land pads. The top arm was then disengaged and the reflow profile descried in the earlier section was run. During the reflow, it could be observed that the solder balls flattened and the profile of the part dropped slightly as a result [Figure 6.17(e)]. This is the sign of a good reflow process. This also served to verify that the

solder spheres were placed sufficiently apart and did not bridge during the reflow process. A photograph showing a batch of samples after the reflow process is shown in Figure 6.17(f). A good general practice for any flip-chip process is underfilling. It not only bolsters the mechanical strength of the flip-chip joints, but also aids voltage isolation. The samples were underfilled using Hysol FP4549 from Henkel. Figure 6.17(g) shows the photograph of a batch of underfilled flip-chip SBDs. A glob-top encapsulated wire bonded control package can also be seen in the photograph.

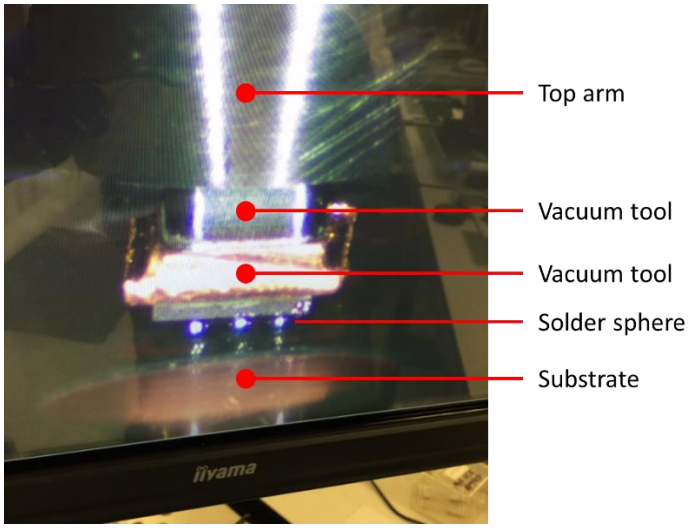


(a)

(b)

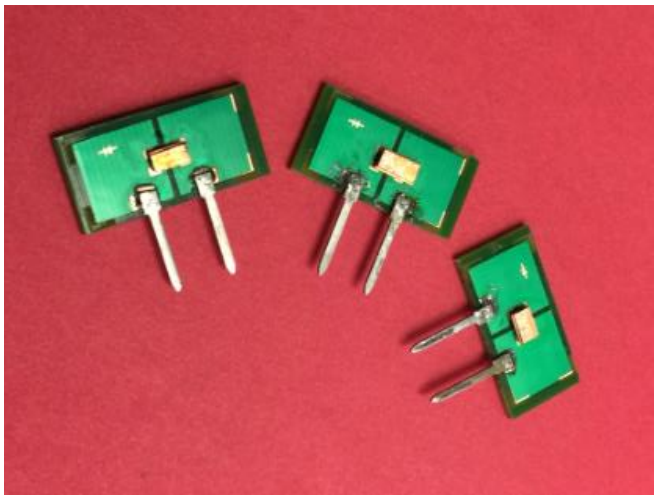


(c)

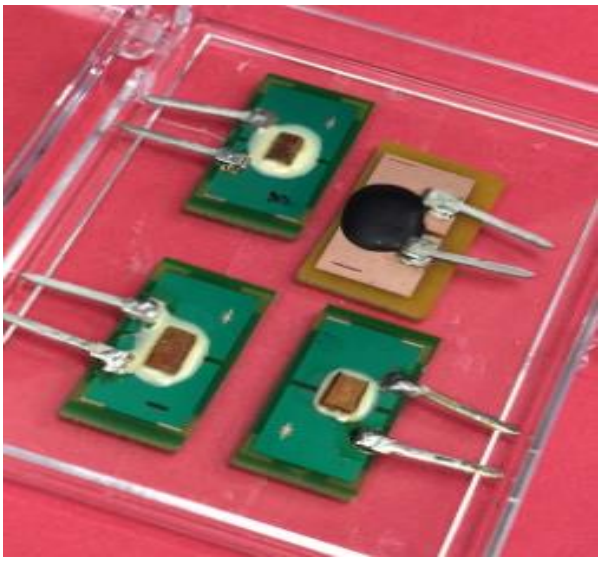

Top arm
Vacuum tool
Vacuum tool
Solder sphere
Substrate
iiyama

(d)

(e)



(f)

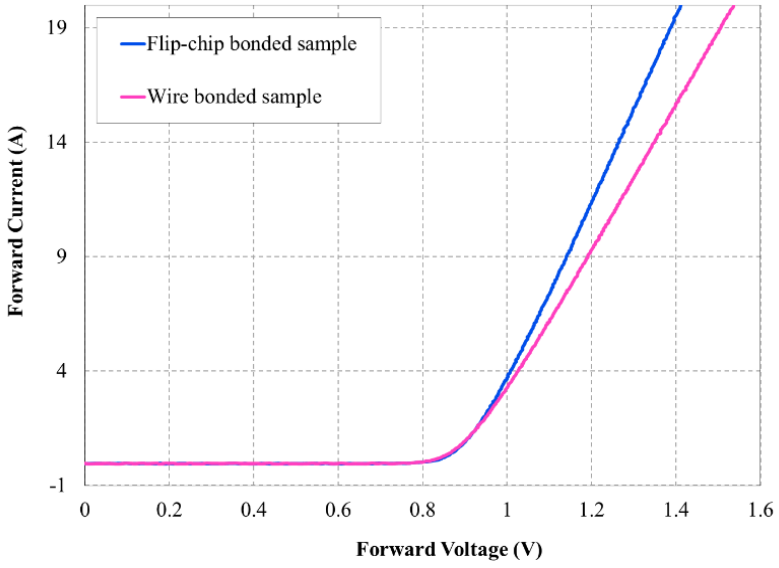


(g)

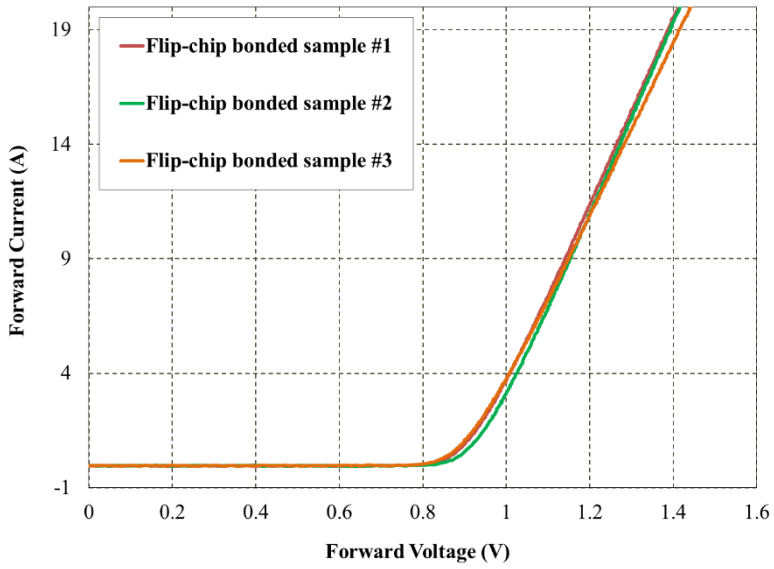
Figure 6.17: Photographs illustrating the process steps for the flip-chip diode package (a) the electroless-plated die attached to the bottom copper connector, (b) diced substrate coupons, (c) solder-masked substrates with land pads, (d) photograph showing the placement of the device on the PCB bond pad, (e) a close-up photograph showing the solder balls collapsing during reflow, (f) flip-chip bonded devices cast in a through-hole package, and (g) a batch of underfilled flip-chip SBD's alongside a glob-topped wire bonded SBD package.

C) Electrical testing:

The first electrical test was a curve tracer measurement. This test would provide evidence of the proper electrical functionality of the devices after they have been subject to the various manufacturing processes. The test would also serve as a measurement of the ON-state resistance from the slope of the forward I-V curve. The TO-247 like devices were mounted on a matching socket on a Keysight B1505A curve tracer. The results of the measurement are shown in Figure 6.18(a). It was clearly observed that the slope of the I-V characteristics were different for the flip-chip sample as compared with the wire bonded sample. However, when multiple flip-chip samples were measured, the curves were almost co-incident, as can be observed in Figure 6.18(b). As a result of changing the interconnection scheme from wire bonded, an average decrease of 6.4 mΩ was obtained. This matched the 6.53 mΩ value predicted by the simulation very closely and translated to a 20% decrease in the conduction losses associated with the package.



(a)

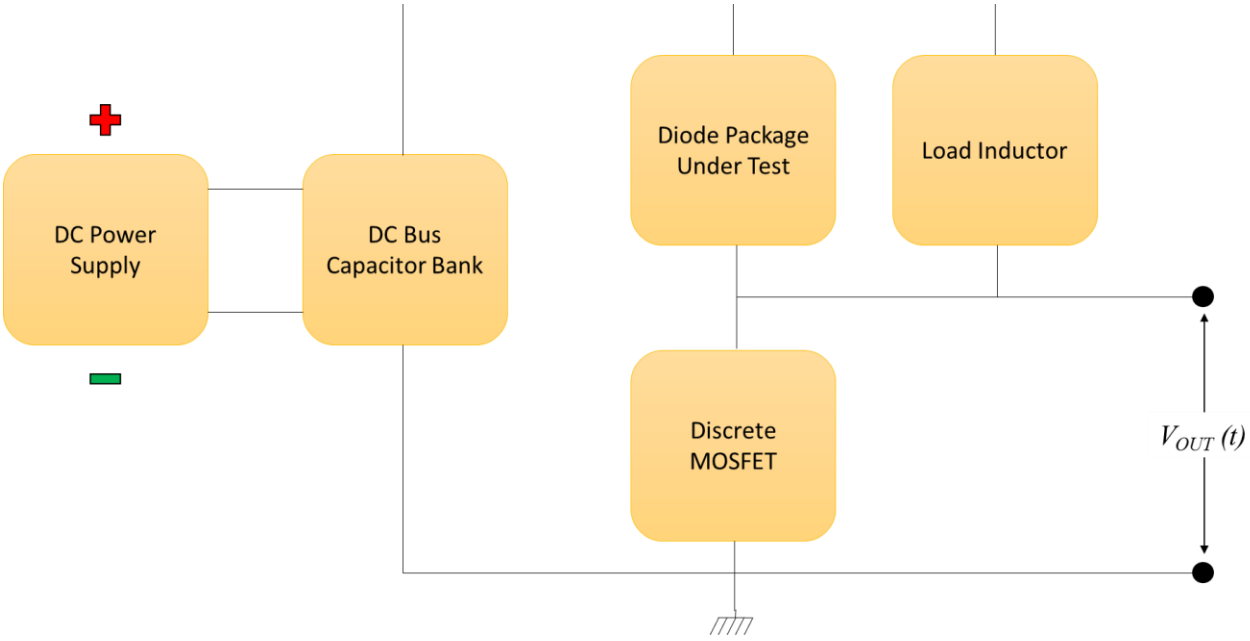


(b)

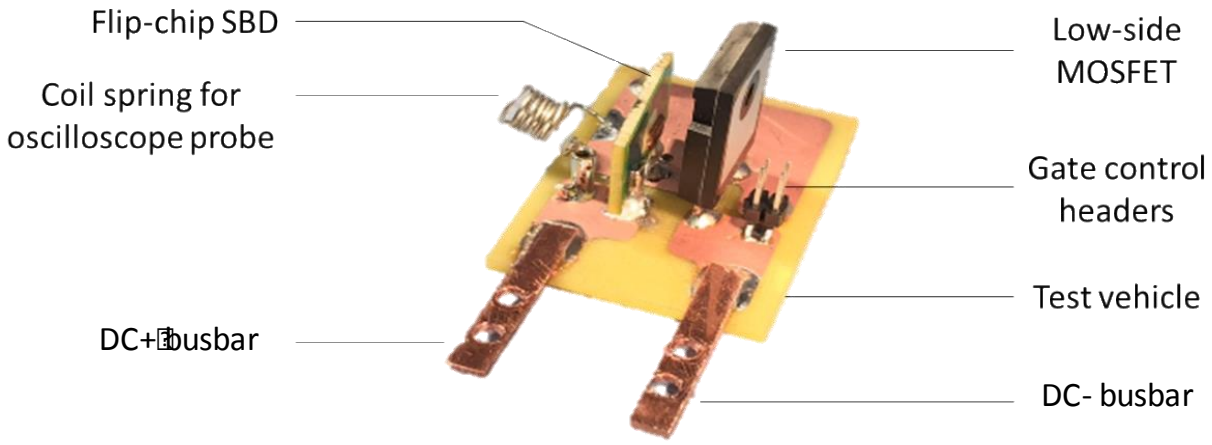
Figure 6.18: (a) A plot showing the forward I-V characteristics of the two types of packages and (b) a chart showing identical characteristics for multiple flip-chip packages.

It is not sufficient to evaluate only the static characteristics of a SBD to evaluate proper electrical functionality. The switching characteristics of the flip-chip SBD were evaluated and contrasted with the performance of the wire bonded control module. A double-pulse test is a standard known-good procedure to evaluate switching characteristics of power devices at a relatively low risk of damaging the device in the process. The devices may be run very close to the voltage and current specifications that they were designed for without requiring thermal management. The current pulses are of short-enough duration to bypass the requirement of a heat sink. The schematic of a double-pulse test setup is shown in Figure 6.19(a). A low-side MOSFET was driven using a series of two pulses from a gate driver circuit. The first pulse is usually of a relatively longer duration to help build current in the output inductor. The second pulse is much shorter, and the turn-off and turn-on characteristics of the circuit are measured at the transitions of this pulse. In order to evaluate the switching characteristics of the SBD packages, a double-pulse

test vehicle was designed and manufactured in-house. The low-side MOSFET was a discrete 1200 V-rated SiC power MOSFET from Wolfspeed with the part number C2M0080120. The fabricated SBD packages were used as the high-side freewheeling diode. A photograph showing the double-pulse test vehicle is shown in Figure 6.19(b), and Figure 6.19(c) shows the test-vehicle as part of the double-pulse test setup.



(a)



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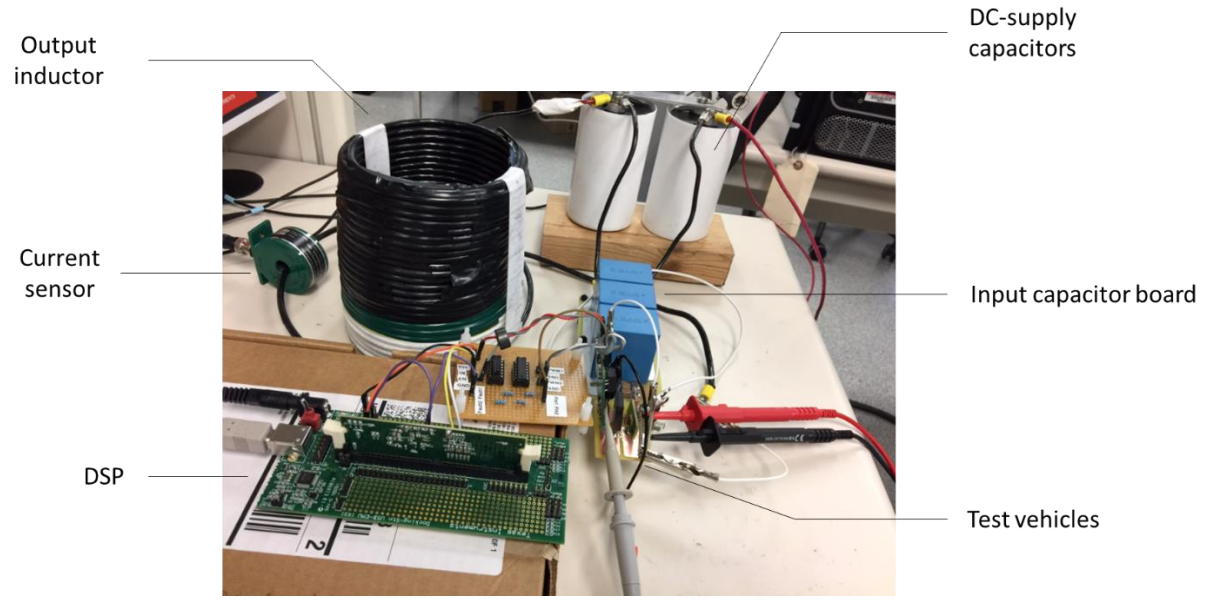


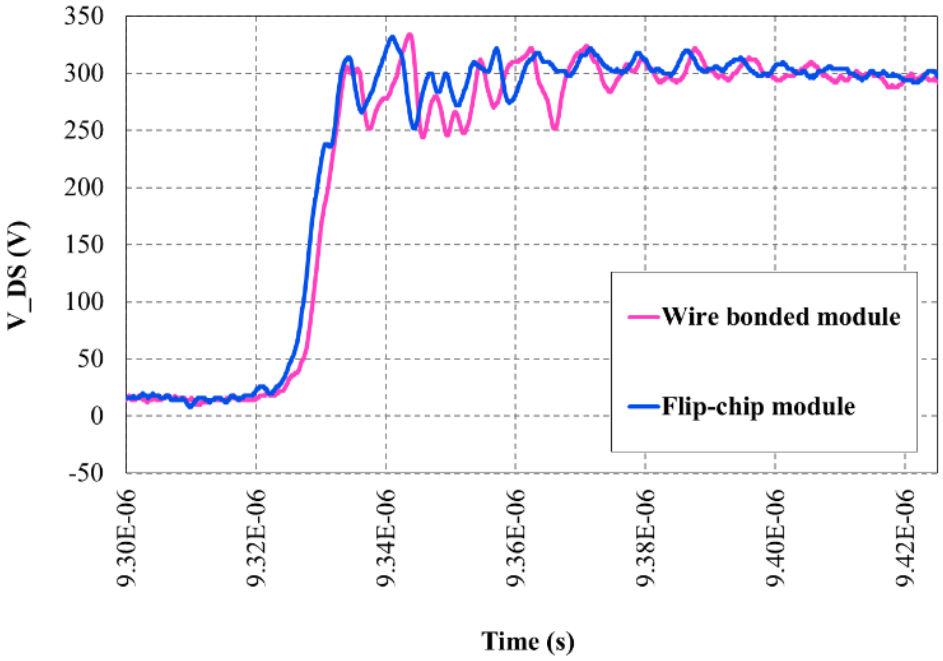
(c)

Figure 6.19: (a) A schematic showing a typical double-pulse test setup, (b) the test-vehicle for the double-pulse test, and (c) a photograph of the test-vehicle mounted on the double-pulse test setup.

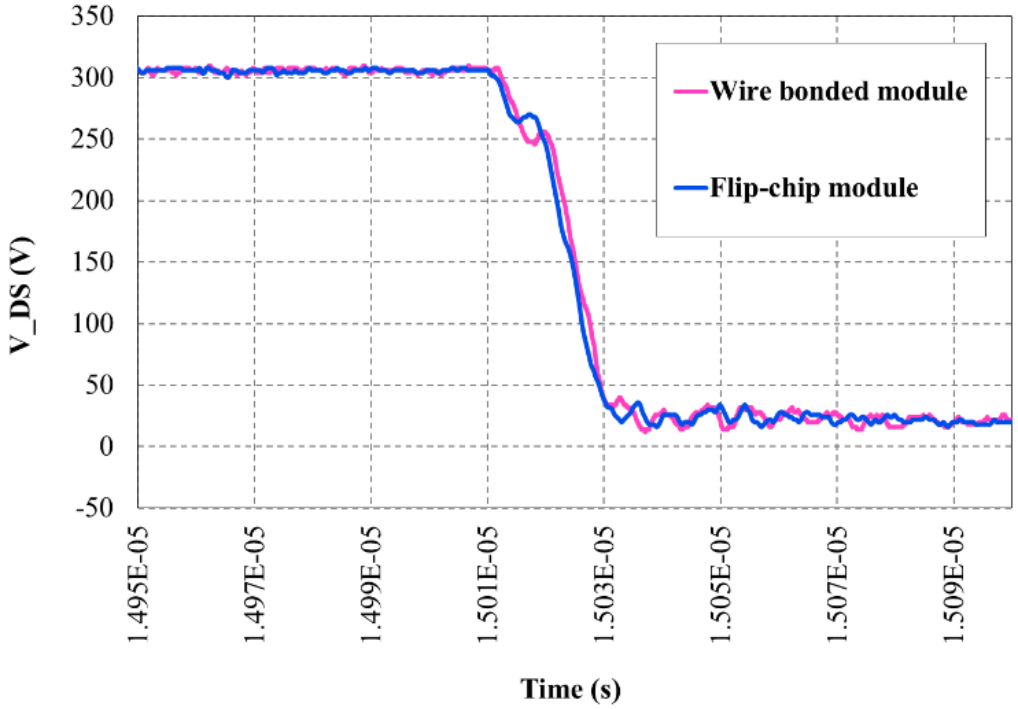
The results of the double-pulse test are presented in Figure 6.20. The first set of measurements were conducted at a DC-bus voltage of 300 V. The bandwidth of the 300 V-rated probes were 500 MHz and would be very sensitive to minor changes in the ringing and overshoot in the two cases

being compared. However, a higher voltage test was also conducted at 450 V DC-bus voltage to demonstrate functionality, and the output was measured using higher voltage rated differential probes with a 25 MHz bandwidth.

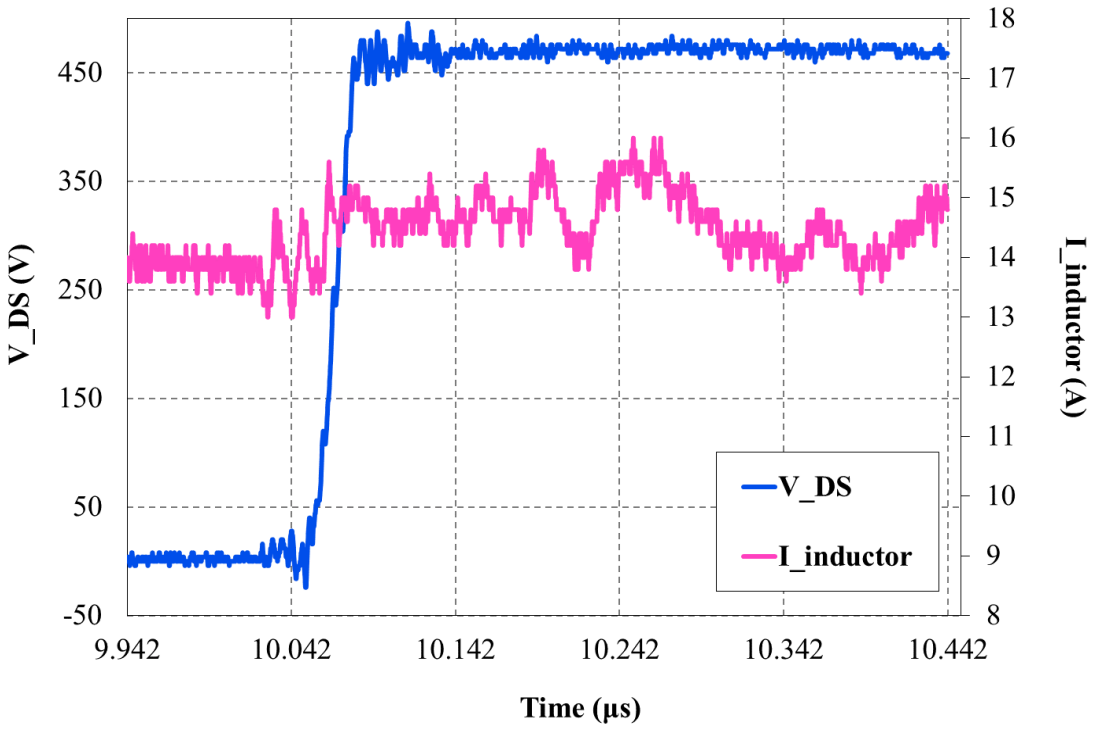
Figure 6.20(a) shows the waveforms of the turn-off event for the two cases at a load current of 15 A. Unfortunately, the parasitic loop inductance in both cases was heavily dominated by the large parasitics offered by the TO-247 leads of the packages under test and the TO-247 package of the low-side MOSFET. Hence, at first sight, there was little observable difference between the two waveforms, and both packages seemed to function perfectly well as SBDs. However, the parasitic loop inductances can be accurately estimated by measuring the time-period of the ringing. The ringing arises because of the resonance between the loop inductance and the output capacitance of the device. The calculation and comparison of the total loop inductance of the two cases are presented in Table 6.1. A 4 nH decrease in the total loop inductance was measured as a result of using the flip-chip package. Figure 6.20(b) shows the waveforms for two cases during the turn-on event. There was no perceivable difference in these waveforms. The calculated turn-off times amounted to 8.5 ns for both packages. The turn-on times were calculated to be 17.6 ns for the flip-chip module and 19.4 ns for the wire bonded package. The asymmetric turn-on and turn-off times were a result of using different gate resistors for turn-on and turn-off, and is considered good practice to minimize switching losses [2]. Figure 6.20(c) shows the output voltage and inductor current waveforms at 450 V and 15 A.


350
300
250
200
150
100
50
0
-50
V_DS (V)
Wire bonded module
Flip-chip module
9.30E-06
9.32E-06
9.34E-06
9.36E-06
9.38E-06
9.40E-06
9.42E-06
Time (s)

(a)


350
300
250
200
150
100
50
0
-50
V_DS (V)
Wire bonded module
Flip-chip module
1.495E-05
1.497E-05
1.499E-05
1.501E-05
1.503E-05
1.505E-05
1.507E-05
1.509E-05
Time (s)

(b)



(c)

Figure 6.20: Waveforms showing (a) the turn-off event, (b) the turn-on event, and (c) operation at 450 V, 15 A.

The calculation of the total loop inductances based on the measured time-period of the ringing is presented in Table 6.1, and the difference between the measured parasitics are contrasted with the predicted values from simulation in Table 6.2. The package resistances showed a very close match, while the match between the parasitic inductances were not as impressive. This was due to the fact that the inductance offered by the respective packages was far lower than the total loop inductance. The variability in the total loop inductance dominated the error in the measurements. However, both the simulation and the measurements verified that the flip-chip package offered a lower inductance.

Table 6.1: A table showing the estimated parasitic loop inductances of the two modules under test.

Output capacitance of the MOSFET (*Coss*)	**Time period of ringing (s) (Δt)**		**Parasitic Loop Inductance (nH) = $\frac{(\frac{\Delta t}{2\pi})^2}{C_{oss}} \times 10^9$**	
	Wire-bonded	**Flip-chip**	**Wire-bonded**	**Flip-chip**
110e-12	9.2e-9	8.2e-9	19.51	15.5

Table 6.2: A table showing the comparison between the estimated and measure parasitic inductance and package resistance for the two modules under test.

Difference in	**Predicted in ANSYSQ3D Simulations**	**Measured in Double-Pulse Test**
Parasitic inductance	2.1 nH	4.01 nH
Package resistance	6.53 mΩ	6.4 mΩ

Conclusions

This chapter provided a much required verification for the processes and concepts developed in the previous chapters. The metallurgical processes developed for converting a commercial bare die power device to a chip-scale package were verified from the standpoint of mechanical durability. The fabricated samples passed all the tests and outperformed a conventional wire bond in terms of bonding strength. The samples were evaluated for electrical functionality after being subject to the proposed fabrication process. The tests included measurements of the forward characteristics and switching performance using a double-pulse test. Both the on-state resistance and loop inductance was found to be reduced as a result of using the flip-chip bonded package, and the measured results agreed well with the simulated results.

References

[1] M. Datta, S. A. Merritt and M. Dagenais, "Electroless remetallization of aluminum bond pads on CMOS driver chip for flip-chip attachment to vertical cavity surface emitting lasers (VCSEL's)," in *IEEE Transactions on Components and Packaging Technologies*, vol. 22, no. 2, pp. 299-306, Jun 1999.

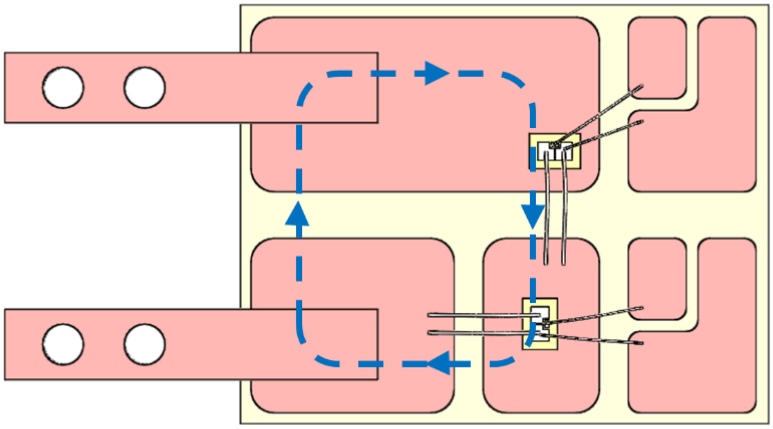
[2]http://www.st.com/content/ccc/resource/technical/document/application_note/7d/2b/9d/f0/88/07/4b/6f/DM00170577.pdf/files/DM00170577.pdf/jcr:content/translations/en.DM00170577.pdf

CHAPTER 7: The Flip-Chip MOSFET and its Implementation in a Half-Bridge Circuit

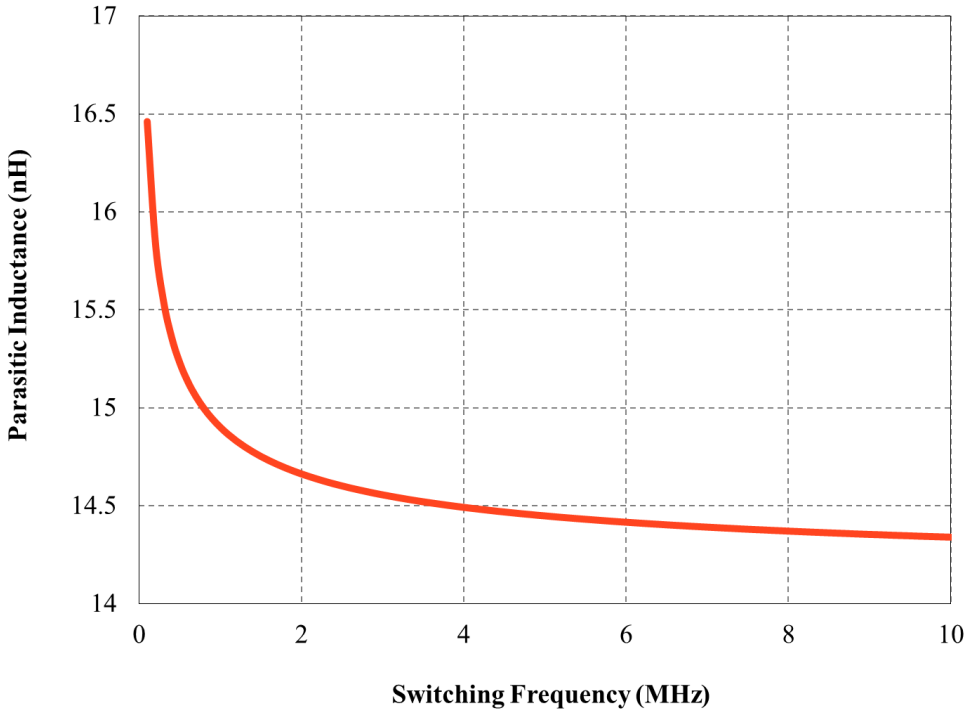
The performance of a flip-chip power device is demonstrated in a half-bridge power module in this chapter. The performance of the half-bridge is compared with control modules using wire bonded devices and discrete packages. The chapter begins with the description of the layout advantage while using a flip-chip bonding scheme alongside an evaluation of the parasitic loop inductances. The thermal management aspects of the flip-chip module are also presented and contrasted with that of a conventional wire bonded power module. Finally, the electrical switching characteristics of the flip-chip module are evaluated by way of a double-pulse test and contrasted with the performance of the control modules.

Section 7.1: The Wire Bondless Half-Bridge Module—Concept and Parasitic Evaluation

In a conventional wire bonded SiC module, the power loop is always lateral in nature. The loop inductance increases with the area of the loop. In order to adhere to recommended wire bonding and trace clearances in the layout of the power module, this loop results in covering a relatively large area even for a simple two-device module like a half-bridge. Figure 7.1(a) shows a schematic of the typical layout of a wire bonded half-bridge module. The area of the power loop is designated by the dashed blue line and measures approximately 14 mm × 14 mm. Contemporary wire bonded power modules also require a ground plane on the bottom DBC copper layer to minimize switching transients. The parasitic inductance of this minimum-area loop even for a simple two-MOSFET half-bridge module was estimated to be around 14-15 nH. The result of the simulation conducted in ANSYS Q3D is shown in Figure 7.1(b).



(a)

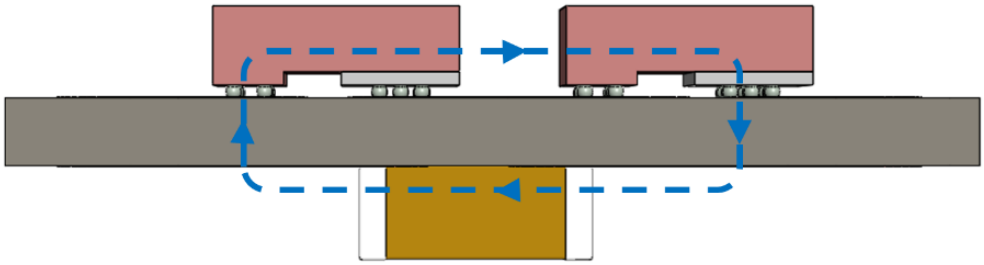


(b)

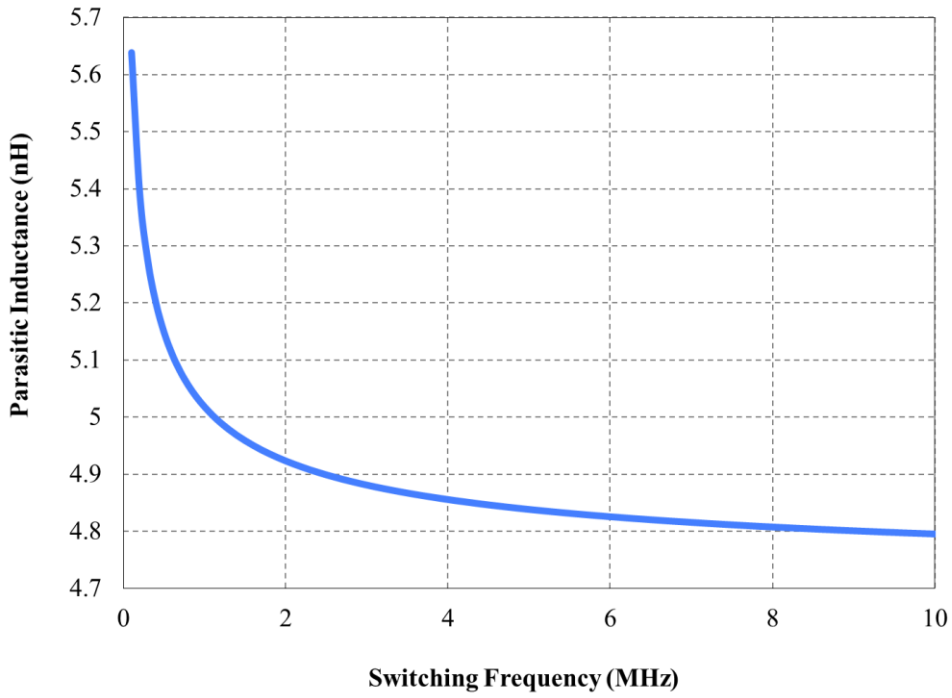
Figure 7.1: (a) A schematic showing a conventional wire bonded half-bridge module layout and (b) a graph showing the parasitic inductance variation of the same.

Let us briefly consider the case of GaN power devices. They are rated at relatively lower voltages as compared with their SiC counterparts. For most GaN applications, having an extremely low parasitic inductance is a requirement. It is not uncommon to find examples in the literature of GaN circuits operating at several MHz. At these frequencies, the overshoot must be extremely well-controlled by minimizing the parasitic inductance of the switching loops. This is the reason why many major GaN manufacturers have adopted a wire bondless chip-scale packaging approach. Even with greatly minimized interconnect inductances with wire bondless flip-chip interconnections, a lateral loop design was found to be detrimental to the switching characteristics of GaN circuits. This phenomenon has been documented great detail in the literature [1] and it has also been shown that a vertical loop design offers a much lesser parasitic inductance. Let us consider the power loop in the case of a flip-chip MOSFET based half bridge module.

A 3D view of the module is presented in Figure 7.2(a). The module consists of a patterned double-side metallized FR4 board with flip-chip MOSFETs on one side and DC-link decoupling capacitors on the other. This resulted in a small vertical power loop as illustrated in Figure 7.2(b) using a dashed blue line. Much like the GaN concept discussed in [1], the only significant contribution to the parasitic inductance are the vertical distances traversed by the signal. The lateral inductances are annihilated as a result of return-path cancellation. The thickness of a typical FR4 substrate is 1.62 mm, resulting in a very short parasitic loop. As mentioned before a short parasitic loop implies a small stray inductance, and this argument is verified through an ANSYS Q3D simulation. The frequency sweep showing the inductance variation of the vertical loop design is presented in Figure 7.2(c). It was observed that the inductance of the vertical loop design was reduced by an order of magnitude as compared with a conventional lateral loop design using bond wires.



(a)



(b)

Figure 7.2: (a) A 3D view of the top and bottom layers of a flip-chip wire bondless half-bridge using SiC power devices, and (b) an illustration of the vertical loop design for the power loop.

There are also a few other advantages of using a vertical design for routing. Power loop decoupling capacitors can be placed very close to the power devices. Many wire bonded power

modules have also been demonstrated using in-module decoupling capacitors, but it is not a standard practice yet. It is not feasible to use multi-layer ceramic capacitors (MLCCs) for decoupling on a power module. MLCCs are usually not as robust as the other components of a power module. The case is more complicated since several MLCCs are preferred to be connected in parallel to minimize the effective series inductance and resistance (ESL and ESR). Failure in any one of the MLCCs will require a replacement of the entire power module. MLCCs are delicate and very susceptible to damage under thermal stress or mechanical flexing [2]. This makes in-module decoupling capacitors a weak proposition.

The temperature capability of MLCCs is also limited. With SiC power modules moving toward higher operation temperatures, the other constituents of the power module have to keep pace. Currently, options exist for high-temperature die-attach materials, substrates and bonding schemes—and the maximum operating temperature of the module will be limited by the maximum rating of the decoupling capacitors.

These issues are efficiently circumvented using the design proposed in Figure 7.2. The design does not use a conventional power module. Power devices are instead treated like surface-mount devices. If an MLCC fails, it can be easily replaced on the FR4 board using standard methods. Similarly, if a power device fails, it can also be replaced easily. This flexibility greatly enhances the serviceability of the power module. The MLCCs are also thermally insulated from the heat of the power devices. The FR4 epoxy material has a typical thermal conductivity of 0.25 W/mK. Hence the waste heat generated by the power devices is not conducted laterally to the MLCCs. This is reinforced by the fact that the primary path of heat removal for the devices is through the bottom side of the power devices.

These concepts will become clearer when the thermal characteristics of the flip-chip module are investigated in detail in the following section.

Section 7.2: Thermal considerations

The bottom metallic connectors of the power devices are electrically active. Hence an electrically insulating thermal interface material was required to attach the heat sink to the chip-scale package. Thermal interface materials typically have a very low thermal conductivity, thus offering an increased thermal resistance. The flip-chip module also lacks a power substrate and a baseplate found in a conventional wire bonded power module.

The thermal analysis of the module was conducted assuming that one of the power MOSFETs dissipated 32 W of power. The on-state resistance of the power MOSFET used for this study was equal to 80 mΩ. Assuming an output current equal to 20A would result in a total conduction loss of 32 W in the MOSFET, which is principally dissipated as heat. This value of heat dissipation was assigned to one of the MOSFETs in the switching leg. A thin layer of thermal interface epoxy was also modeled between the bottom connector and the heat sink. The material properties were that of Loctite 3873 from Henkel. This particular epoxy has a thermal conductivity of 1.25 W/mK, which is very high according to the standard values for electrically insulating thermal interface materials. In keeping with the goals of achieving a high power density, the chosen heat sink was a unique integrated fan sink design. The part is available for purchase commercially at the Cool Innovations web store, under the name 4-202004UJFA. A photograph of the heat sink is shown in Figure 7.3. The surface area of the heat sink is 2.05 in × 2.05 in. It can be observed that the innovative sunk fan design effectively eliminated the additional height of the fan, whilst offering a satisfactory thermal resistance of 1.54 ºC/W. The total thickness of the assembly is only 10.9 mm. The fan is rated to produce 6.8 CFM of airflow. These heat sinks are also available in lower

thermal resistance variants of larger surface area and/or fan diameters to handle higher losses if required for an application.

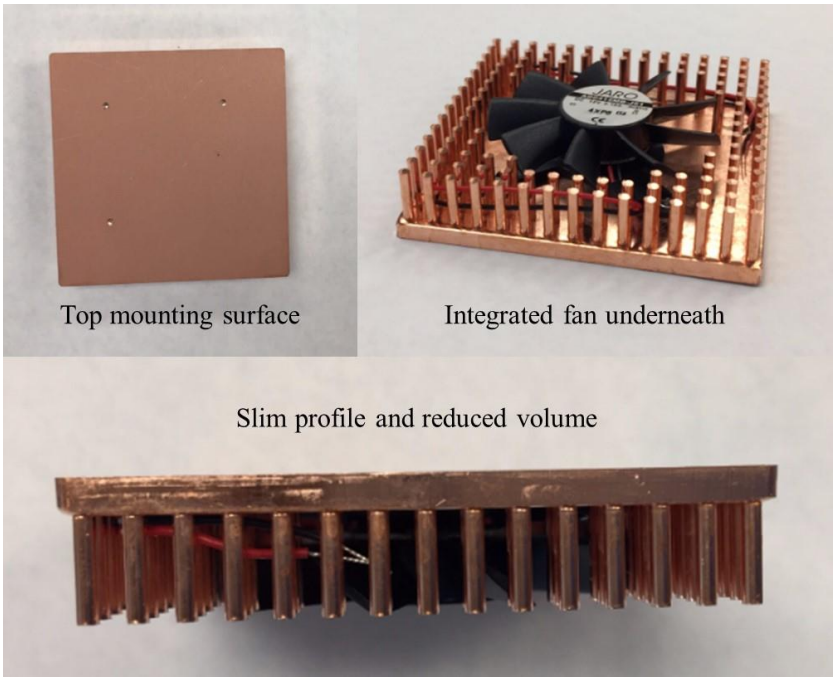
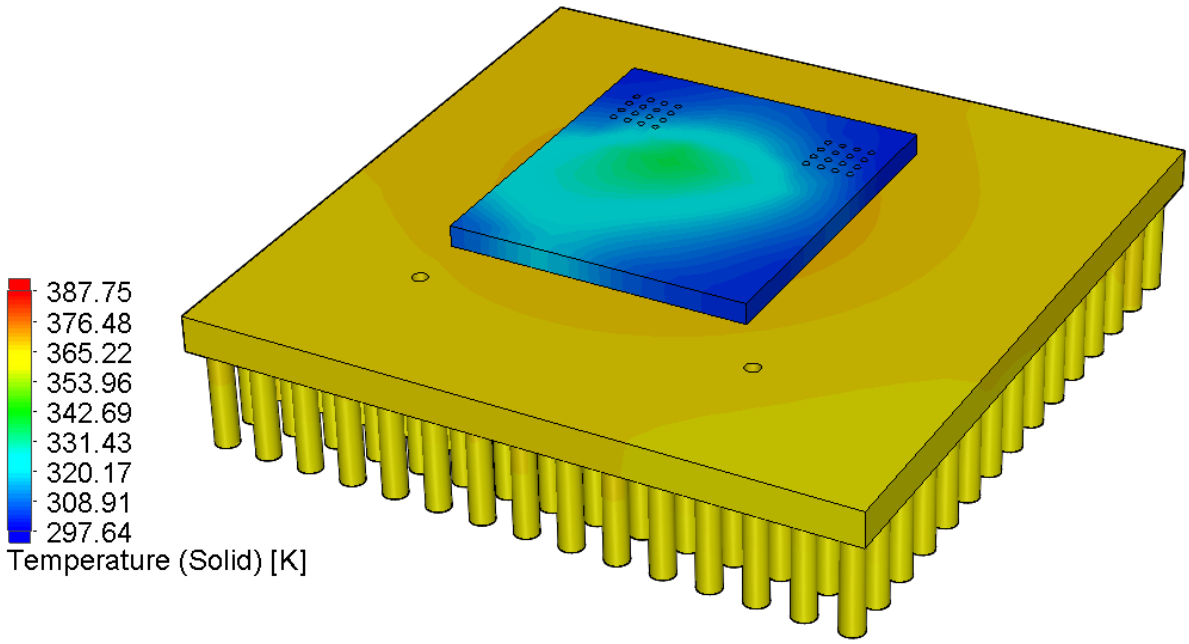


Figure 7.3: A photograph showing the integrated fansink used for thermal management.

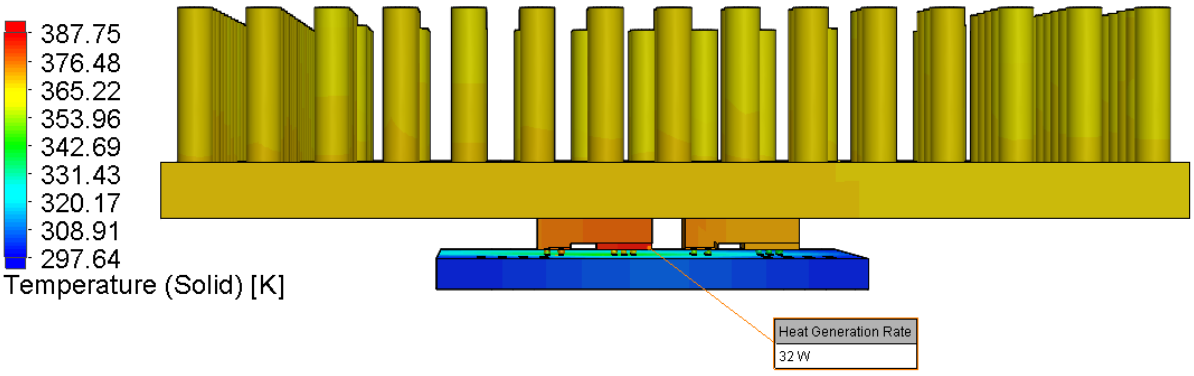
The results of the simulation is shown in Figure 7.4. The maximum temperature on the surface of the device as a result of using the reduced form factor heat sink was found to be approximately 114 ºC. A 3D view of the heat map is presented in Figure 7.4(a). It can also be observed that the FR4 interposer remains at a much lower temperature as compared with the power devices and heat sink. This had a few advantages. The low thermal conductivity of FR4 ensures that the temperature on the PCB stays well below the maximum allowable limit. Hence the capacitors on the PCB also experience a much lower temperature as compared with the power devices. Conversely, the heat sink temperature was found to rise readily implying a very low thermal resistance from the junction to the case. This was more clearly visible upon an inspection of the cross-section of the module presented in Figure 7.4(b). A zoomed-in view of the cross-section [Figure 7.4(c)] reveals that the

bottom side provides a much lower thermal resistance as compared to the top side, and this was the purpose of the design. The solder balls themselves were observed to be at maximum temperature of < 100 ºC. The heat sink temperature was very evenly distributed, and close to the temperature of the die [Figure 7.4(d)].

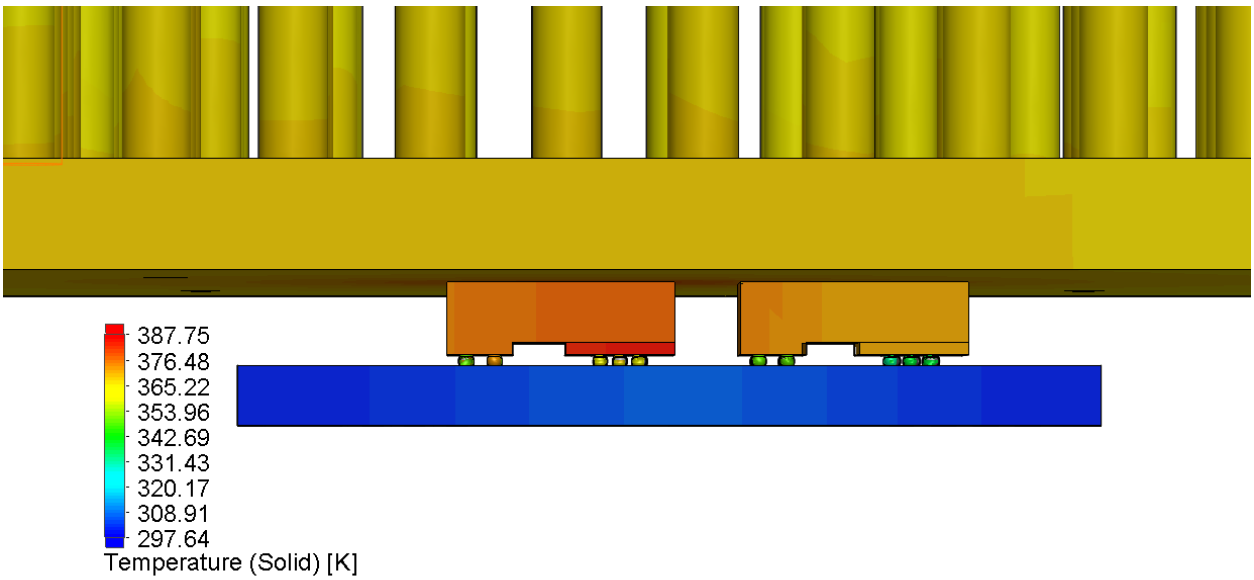
To evaluate the performance of the fan two parameters required careful inspection—pressure drop and air velocity, and the temperature of the air. An increase in air pressure through the pins would reduce the heat transfer capability of the system and bring about a decrease in the air velocity. A high air velocity as presented in Figure 7.4(h) alleviated these concerns. This was expected since the heat sink was a commercial product and presumably well-characterized with respect to these parameters. The fast airflow exiting the heat sink boundaries may also be utilized to cool inductors and capacitors in a system level design. The temperature of the air as shown in the contour presented in Figure 7.4(g), showed no observable heating. A cool fluid profile under thermal load is more efficient in heat removal.


387.75
376.48
365.22
353.96
342.69
331.43
320.17
308.91
297.64
Temperature (Solid) [K]

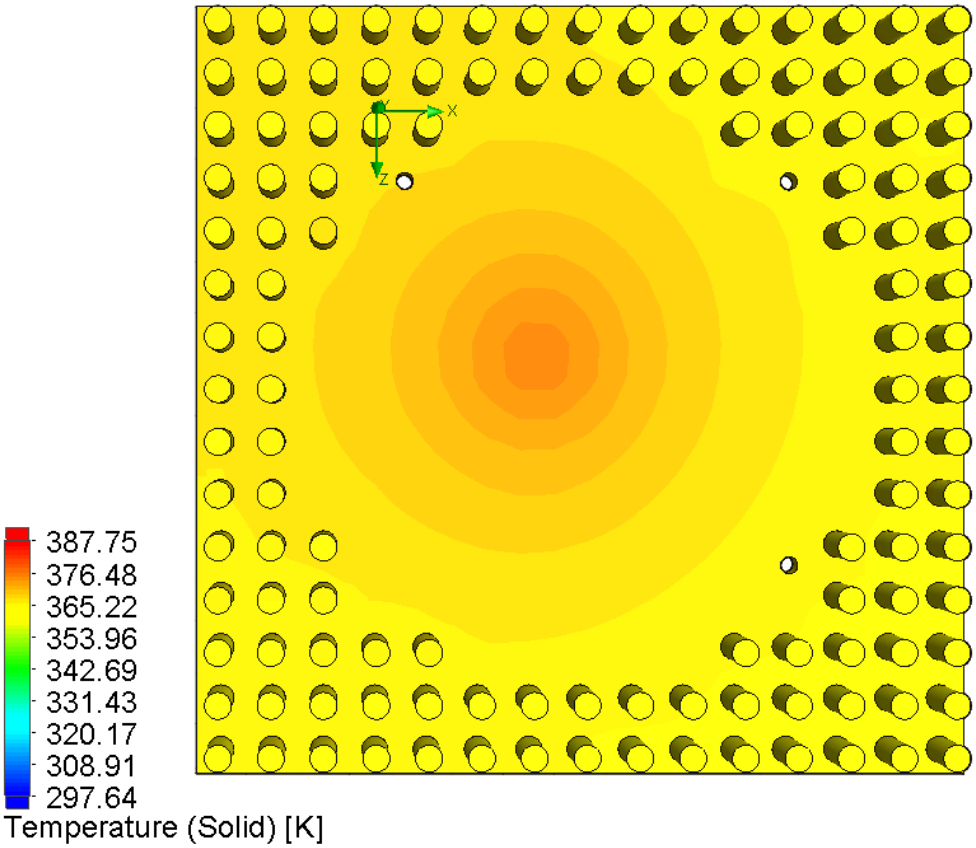
(a)


387.75
376.48
365.22
353.96
342.69
331.43
320.17
308.91
297.64
Temperature (Solid) [K]
Heat Generation Rate
32 W

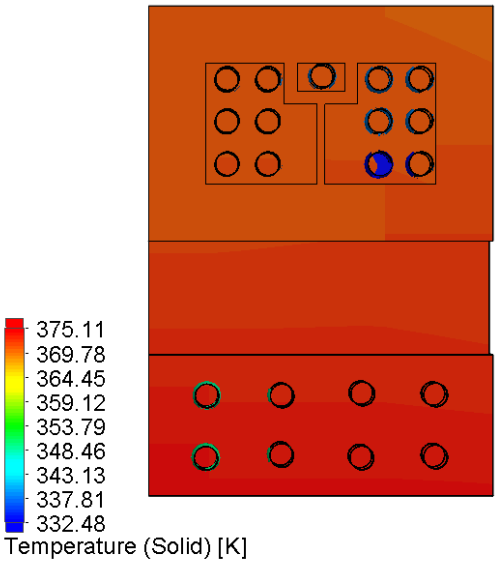
(b)


387.75
376.48
365.22
353.96
342.69
331.43
320.17
308.91
297.64
Temperature (Solid) [K]

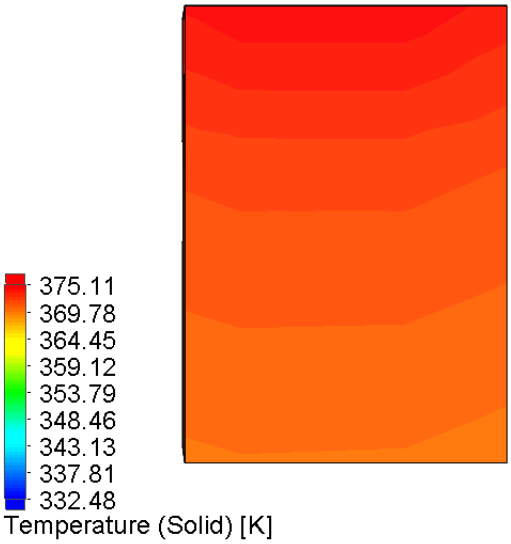
(c)


Y
X
Z
387.75
376.48
365.22
353.96
342.69
331.43
320.17
308.91
297.64
Temperature (Solid) [K]

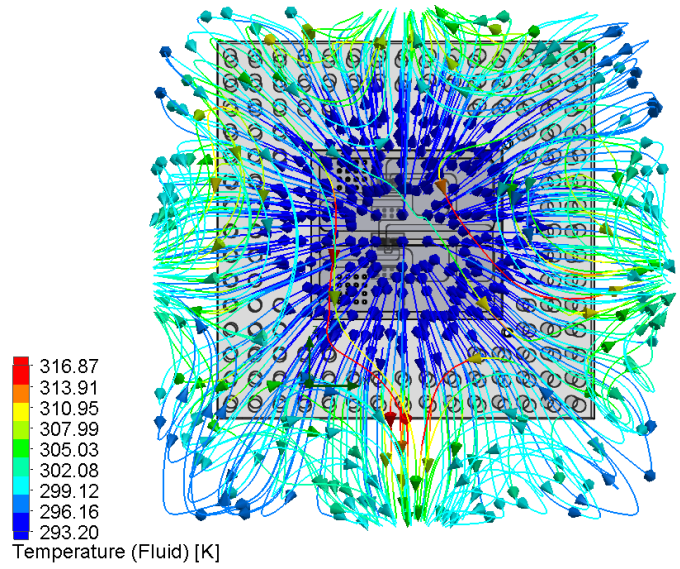
(d)


375.11
369.78
364.45
359.12
353.79
348.46
343.13
337.81
332.48
Temperature (Solid) [K]

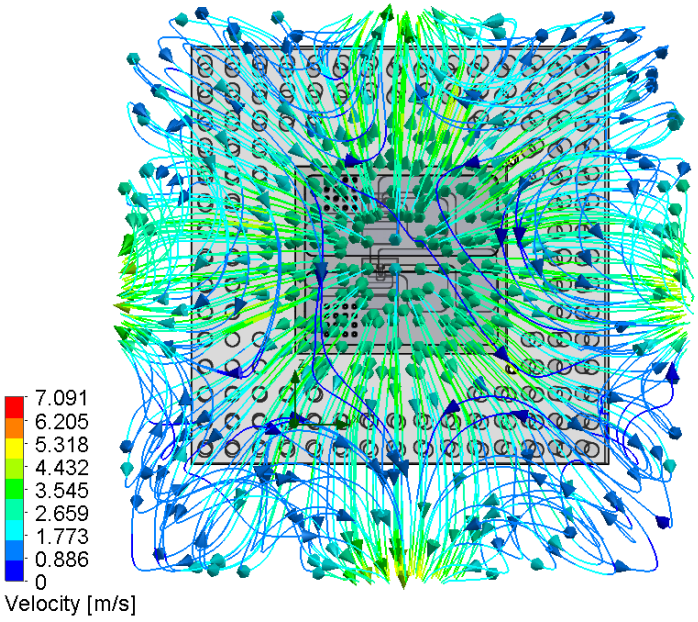
(e)


375.11
369.78
364.45
359.12
353.79
348.46
343.13
337.81
332.48
Temperature (Solid) [K]

(f)



(g)

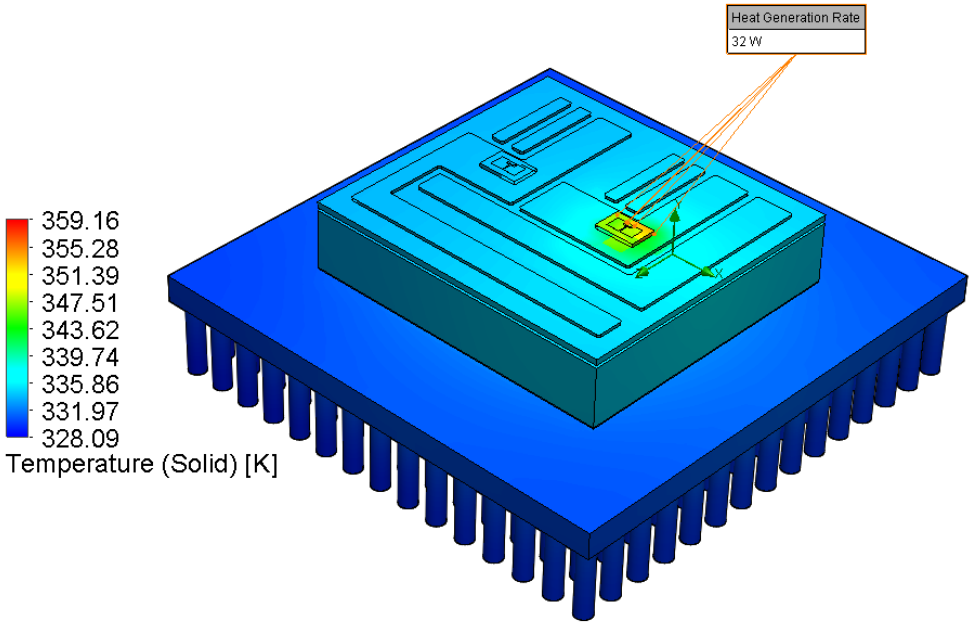


(h)

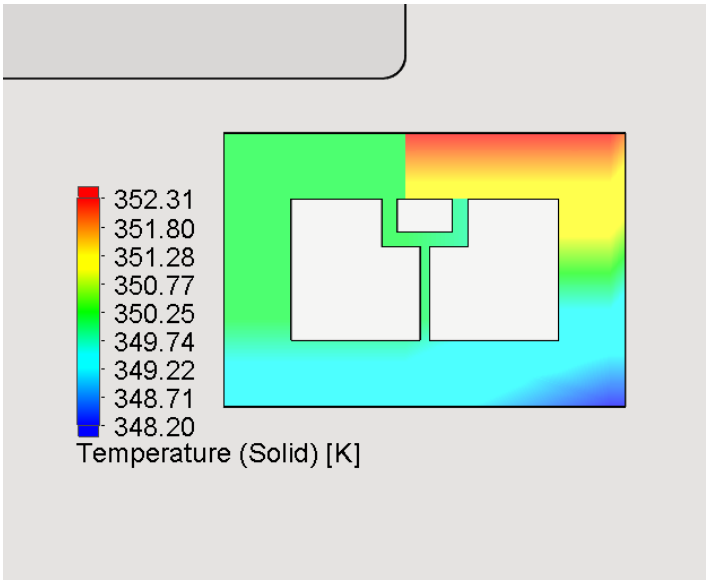
Figure 7.4: Thermal analysis results of the wire bondless half-bridge module showing (a) a 3D thermal plot for the entire module, (b) a lateral view of the thermal profile, (c) a zoomed-in lateral view showing the temperature of the solder balls, (d) the thermal profile on the heat sink, (e) the top view of the thermal profile on the MOSFET, (f) the bottom view of the thermal profile on the metallic connector, (g) a contour of the air temperature, and (h) a contour of the velocity of airflow.

A comparable wire bonded module was also analyzed to serve as a baseline for the observations for the flip-chip module. Figure shows a 3D model of the wire bonded module. The approach used for the thermal management of this module was standard practice in the industry. SiC devices were mounted in a half-bridge configuration atop a DBC substrate. Aluminum nitride (AlN) was defined as the ceramic layer because of superior thermal conductivity and close CTE match with SiC. Most commercially manufactured SiC modules have adopted this approach despite the higher cost AlN-based DBCs. The substrate was assumed to be soldered to a 0.25 inch thick copper baseplate. A baseplate is used for heat spreading and added mechanical support in wire bonded power modules. The same integrated fan sink was used for thermal management, and was attached to the baseplate using the same epoxy as the flip-chip model. A 32 W thermal load was assigned to one of the power devices, as before, and the result of the thermal simulation is presented in Figure 7.5.

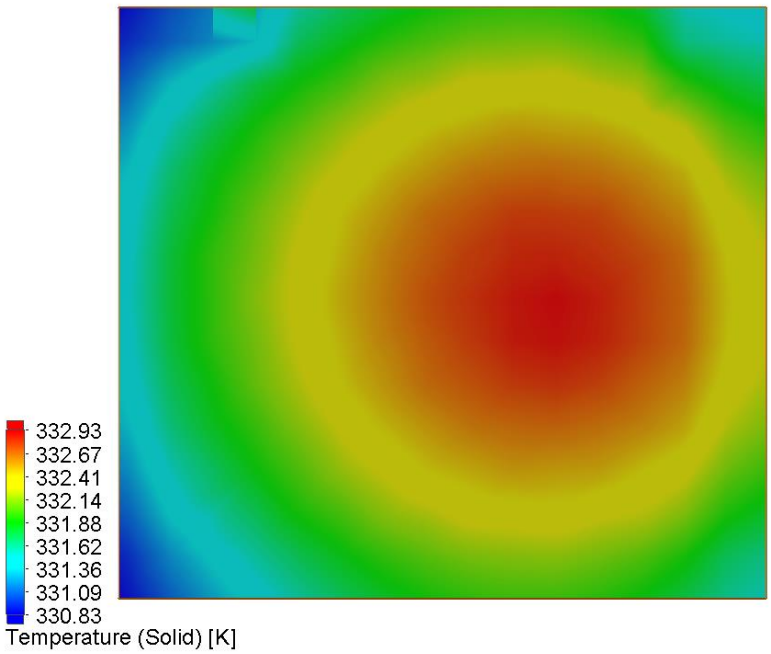
At first glance, the wire bonded power module seems a lot cooler than its flip chip counterpart. Upon closer examination, however, it was found that the maximum temperature on the die surface was only 14.74 ºC lower than the flip-chip module. An examination of the thermal profile on the surface of the chip and the bottom of the baseplate revealed a junction-to-case thermal resistance of 0.6 ºC/W. This was found to be typical of the specified value for most SiC power modules and discrete devices available in the market today. As observed earlier, the value for the flip-chip module much lower by enabling a more direct contact between the heat sink and the power device. The fluid temperature and airflow patterns for the wire bonded module were also plotted as shown in Figure 7.5(e), and were not found to be significantly different from the case of the flip-chip module.


Heat Generation Rate
32 W
359.16
355.28
351.39
347.51
343.62
339.74
335.86
331.97
328.09
Temperature (Solid) [K]

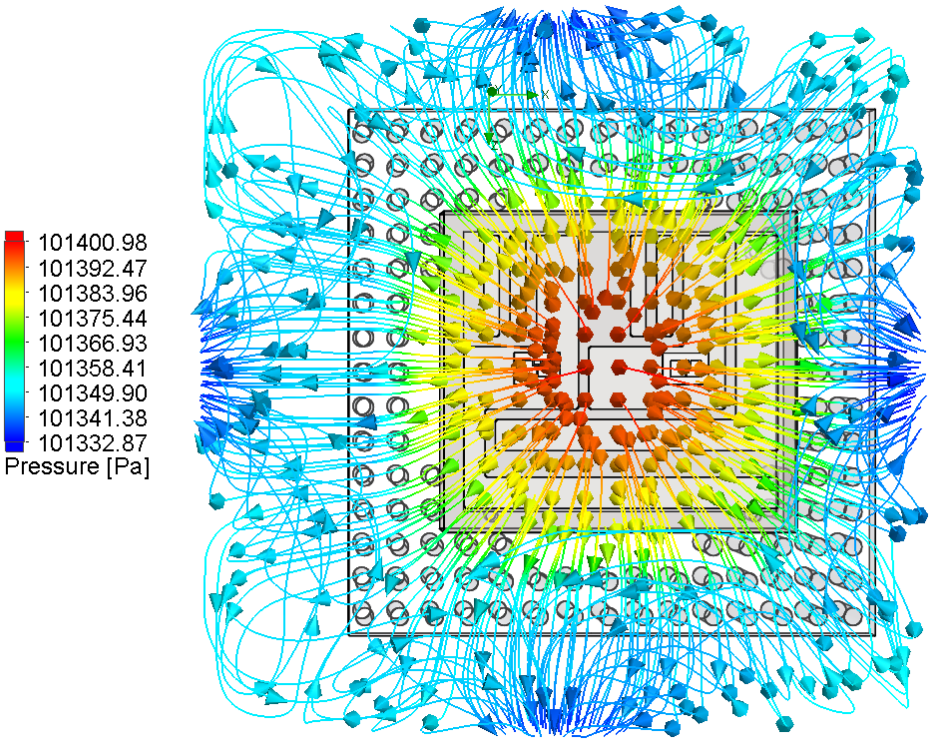
(a)


352.31
351.80
351.28
350.77
350.25
349.74
349.22
348.71
348.20
Temperature (Solid) [K]

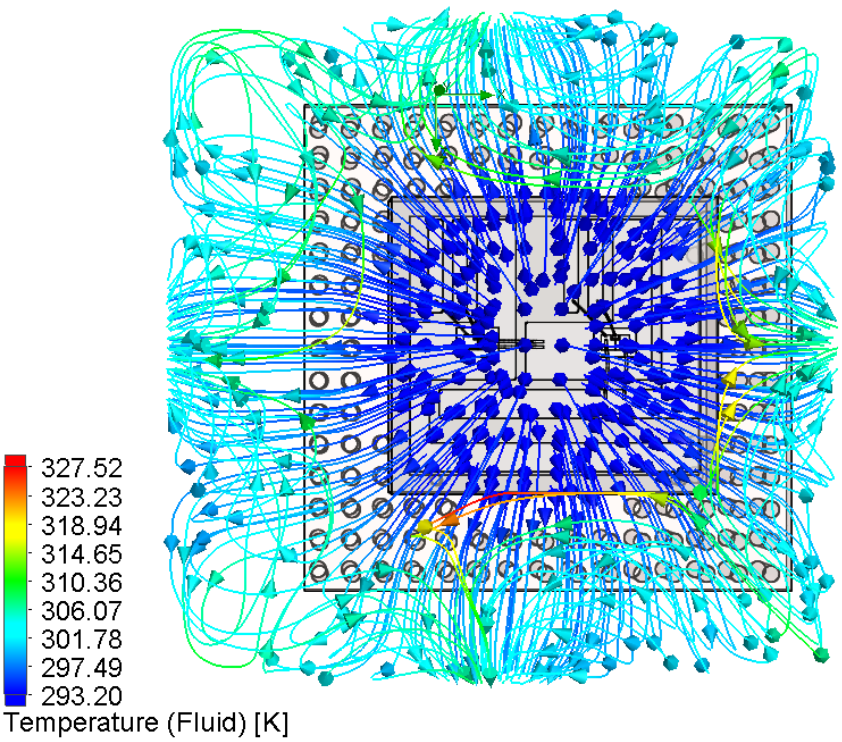
(b)


332.93
332.67
332.41
332.14
331.88
331.62
331.36
331.09
330.83
Temperature (Solid) [K]

(c)


101400.98
101392.47
101383.96
101375.44
101366.93
101358.41
101349.90
101341.38
101332.87
Pressure [Pa]

(d)

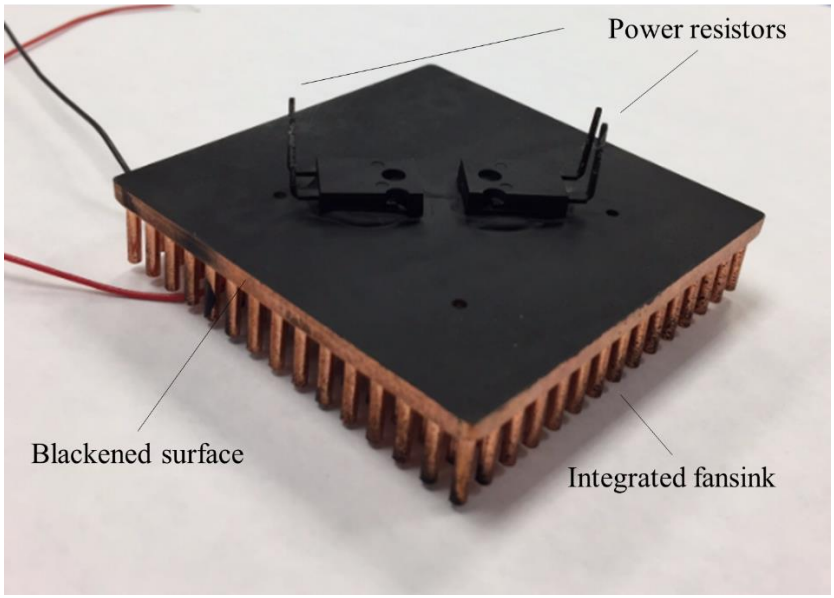


(e)

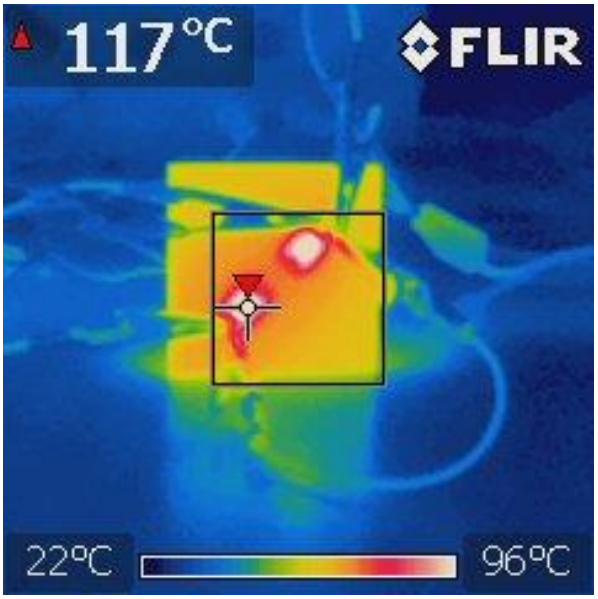
Figure 7.5: Thermal analysis results of a conventional wire bonded half-bridge showing (a) a 3D plot of the thermal profile, (b) thermal profile on the top side of the power MOSFET, (c) thermal profile on the bottom of the baseplate, (d) a contour showing the airflow pressure distribution, (e) A contour showing the air temperature distribution.

A well-defined thermal simulation can usually predict the maximum device temperatures to a great degree of accuracy. However, it is always good practice to compare the profiles observed in simulations with a thermal test designed to closely resemble a "real-world" situation. In order to achieve this, a test vehicle constructed, comprising a pair of power resistors mounted on a heat sink using a thermally conductive epoxy material—much like the heat sink was attached to the flip-chip MOSFETs with epoxy. The heat sink and epoxy were the same components assumed for the simulations. The power resistors were connected in parallel, and a voltage was applied across them. The level of this voltage was adjusted so that the resistors dissipated around 15 W of heat each, amounting to about 30 W combined. Figure 7.6(a) shows a photograph of the test vehicle for

the thermal test. Since an infrared detector was employed to make the observations, the surface of the heat sink was blackened to eliminate anomalies arising out of spurious reflections from regions of different emissivities. The thermal map is presented in Figure 7.6(b). The maximum surface temperature of the power resistors was measured as 117ºC, which was in agreement with the results of the simulations. Also, the temperature distribution on the heat source and heat sink are very close implying a very low thermal resistance. This was consistent with the prediction of the simulation for the flip-chip module.



(a)

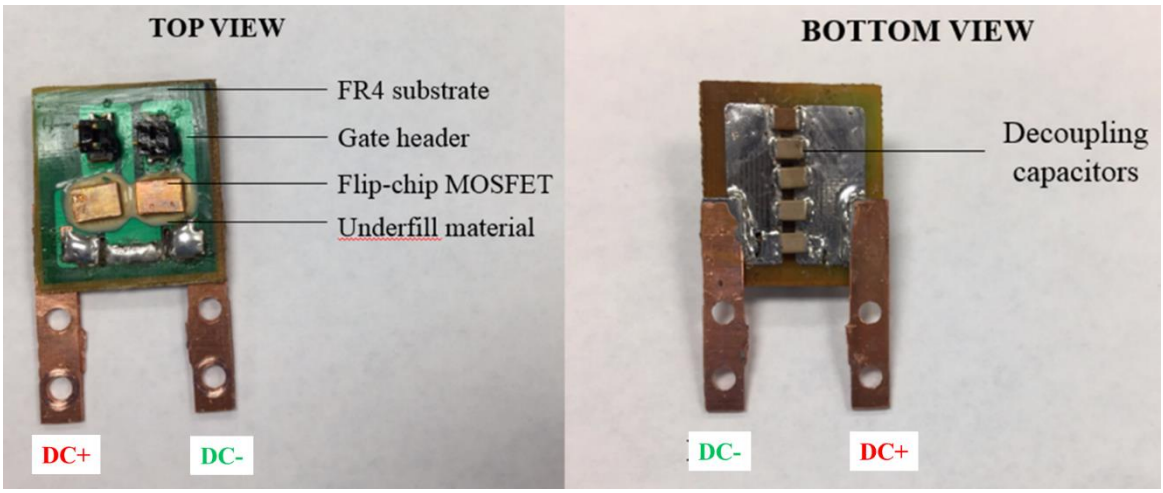


(b)

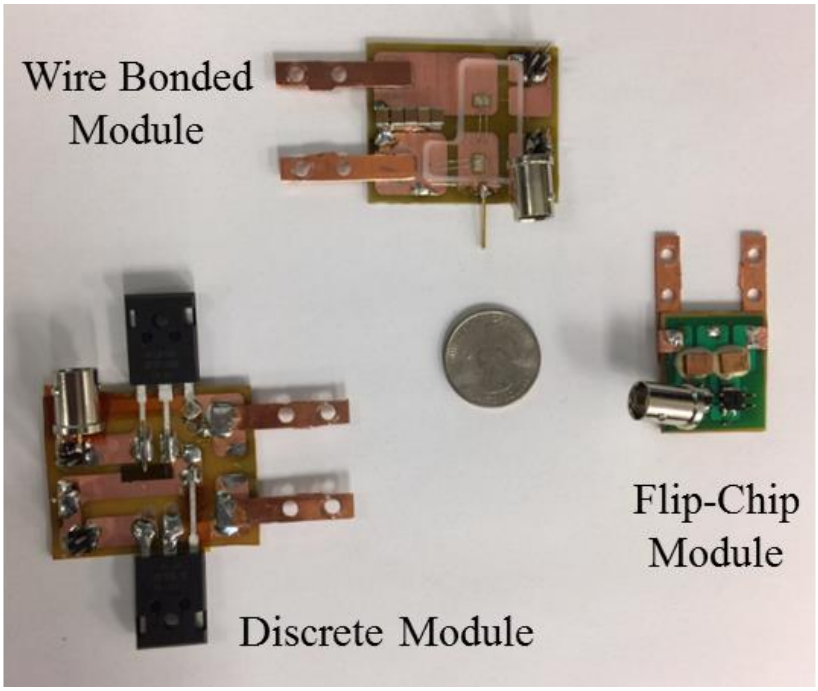
Figure 7.6: (a) A photograph showing the test vehicle for thermal verification and (b) a heat map showing the thermal profile of the same under 30 W of loss.

Section 7.3: Electrical Test Results

For the electrical test, three half-bridge modules were fabricated—using flip-chip MOSFETs, wire bonded MOSFETs, and discrete MOSFET packages. The MOSFET in all three modules were identical devices from the same manufacturer with the same ratings. This was an important step to ensure that any difference observed in the switching transients were a result of the difference in the loop inductances only. The fabrication details for the flip-chip module were identical to the procedures described earlier. The substrates used in all three cases were double-side metallized FR4 substrates. The modules would not be evaluated under continuous current and hence the thickness of the copper layer was not deemed a concern. The top and bottom views of the flip-chip module are presented in Figure 7.7(a). The underfilled flip-chip MOSFETs can be seen on the top side of the board alongside the gate headers for each device. On the reverse side of the interposer, five 10 nF decoupling capacitors were mounted. Multiple capacitors were employed to minimize the effect of the effective series resistance (ESR) and effective series inductance (ESL) associated with the capacitors. Figure 7.7(b) shows a photograph of the control modules alongside the flip-chip module and a US quarter for size comparison. Due to the small footprint of the flip-chip devices, it can be observed that the area of the flip-chip module is much smaller than the wire-bonded and discrete modules.



(a)



(b)

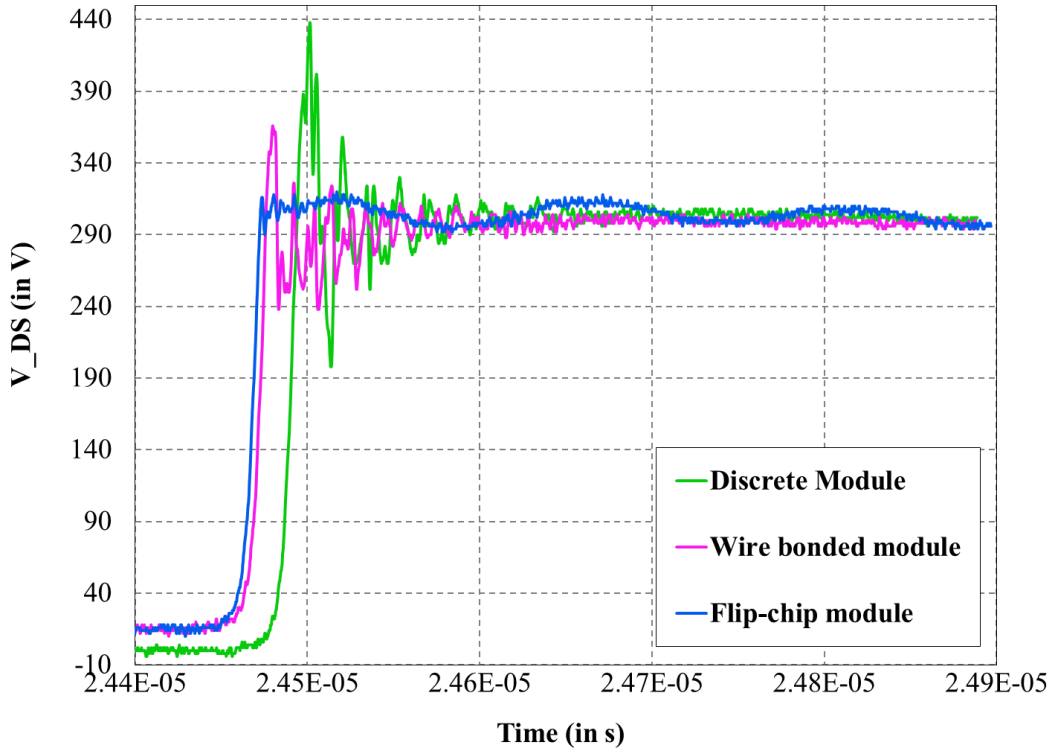
Figure 7.7: Photographs showing the (a) flip-chip module and (b) control modules.

For the electrical testing of the power modules, a double-pulse test setup was employed. The setup for the double pulse test has already been described in the previous chapter. The top switch in these modules was forcibly held in the off-state by electrically shorting the gate and source

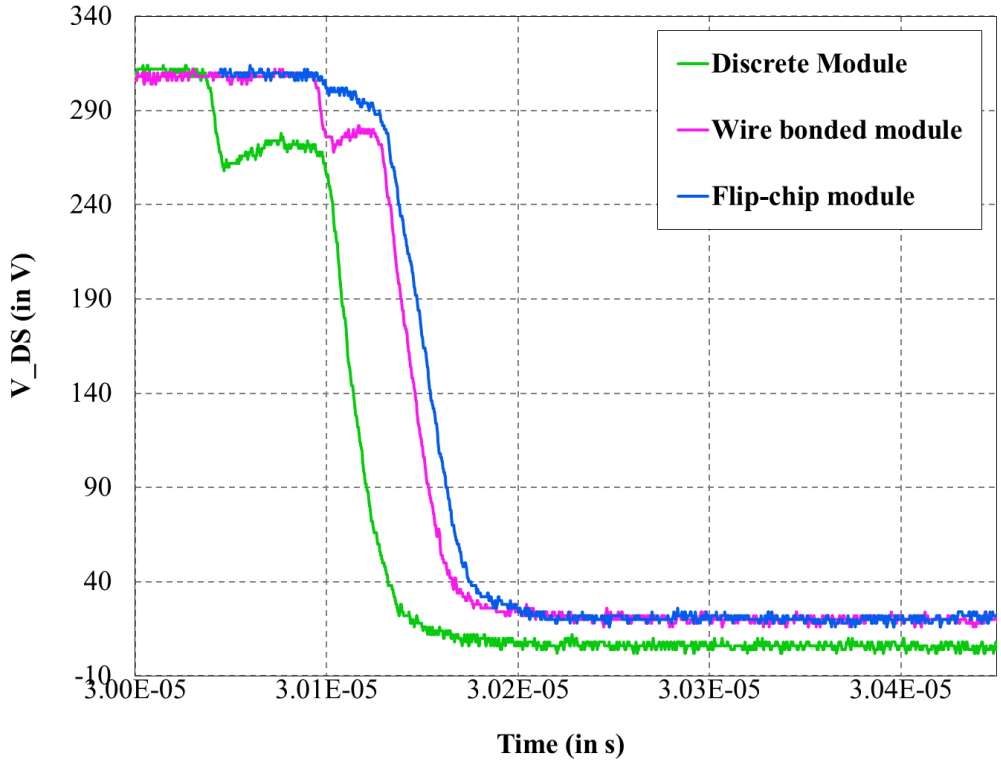
terminals using a jumper across the pin headers. The switching characteristics of the two modules would give an indication of the actual parasitic loop inductance values and *dv/dt* effects in the different modules. A DC bus voltage of 300 V was applied across the bus bars of each module and the width of the first gate pulse was adjusted to provide a current of 35 A through the devices which was close to the 40 A maximum rating of the devices. The bus voltage was limited to 300 V due to the probe voltage rating. A high-bandwidth probe of 600 MHz was used to measure the switching waveforms. Using a high-voltage differential probe rated at a bandwidth < 100 MHz would fail to capture the finer signal artifacts occurring in the span of a few nanoseconds. The results of the double pulse measurements are presented in Figure 7.8.

Figure 7.8(a) shows the waveforms across the output of the three half-bridge modules. The overshoot in the discrete module was expected due to the large loop inductance offered by the TO-247 device package. The loop inductance of the wire bonded module was significantly lower than the discrete devices, showing about 60 V of overshoot. However, in case of the flip-chip module, the overshoot was almost negligible. This was because of the highly-reduced loop inductance achieved using a vertical power loop. Turn-off time was calculated to be only 13.6 ns. Figure 7.8(b) shows the output waveform during the turn-on event. The difference in these waveforms were less drastic, since the turn-on process is comparatively slow due to the presence of a 5 Ω gate turn-on resistor. The load current was also monitored for the three modules and is shown plotted in Figure 7.8(c). The drain current waveforms could not be measured faithfully using a current transformer, since it added about 15 nH inductance to the loop. This would not only result in distorted current waveforms, but it would also cause perturbations in the output voltage waveforms due to the added loop inductance.

It is not sufficient to only measure the output switching waveforms of the modules. One of the major implications of an increased *dv/dt* is a corruption in the gate signal. Sever ringing in the gate signal can lead to a false turn-on event resulting in a shoot-through conduction. The gate voltage was also measured using a high-bandwidth probe to gain a clear insight into the voltage transients. Figure 7.8(d) shows a comparison of the waveforms for the three modules during the turn-event of the gate. From an inspection of the waveforms for the discrete and wire bonded modules, it was easy to understand the cause of the false turn-on risk. As for the case of the flip-chip module, the gate waveform was nearly transient-free with a much reduced overshoot and ringing. The turn-on event or the gate signal was nearly identical for all the three modules.


440
390
340
290
240
190
140
90
40
-10
V_DS (in V)
2.44E-05
2.45E-05
2.46E-05
2.47E-05
2.48E-05
2.49E-05
Time (in s)
Discrete Module
Wire bonded module
Flip-chip module

(a)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V_DS (in V)
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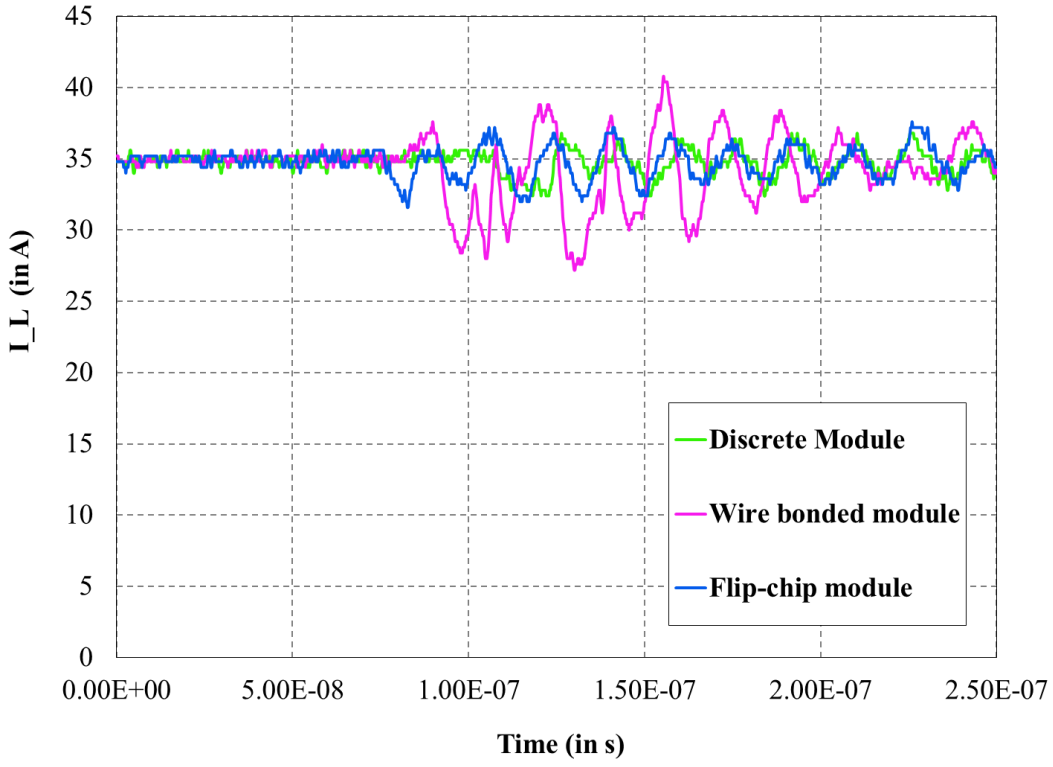
3.04E-05
Time (in s)
Discrete Module
Wire bonded module
Flip-chip module

(b)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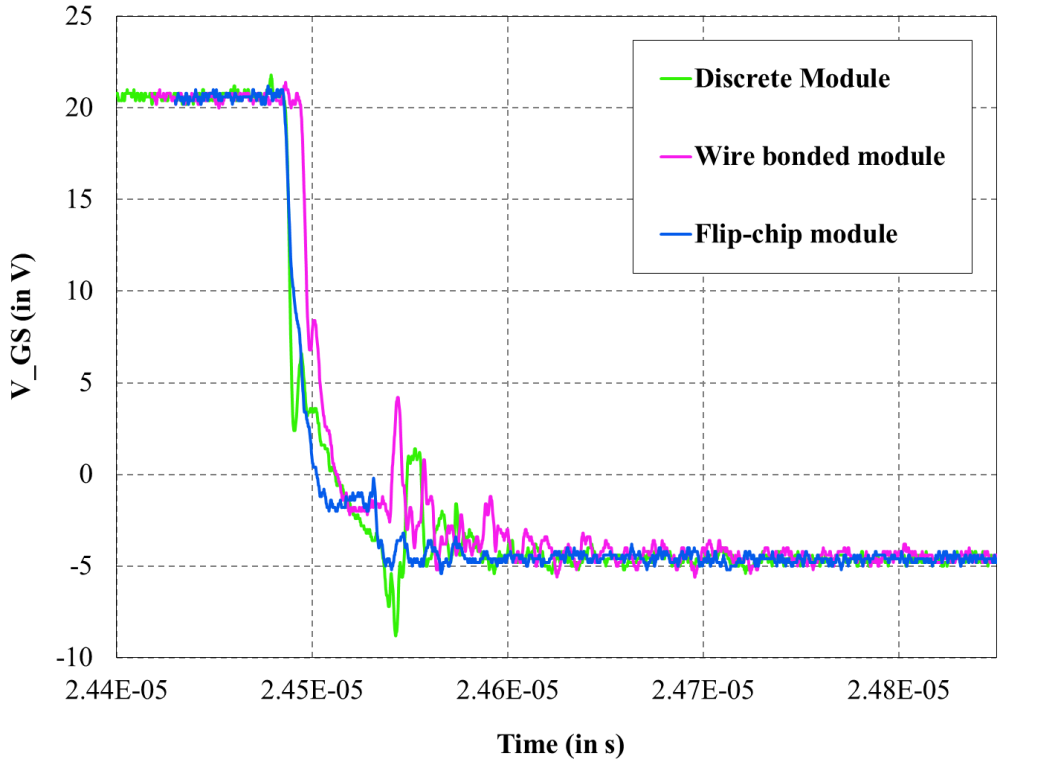
2.50E-07
Time (in s)
Discrete Module
Wire bonded module
Flip-chip module

(c)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V_GS (in V)
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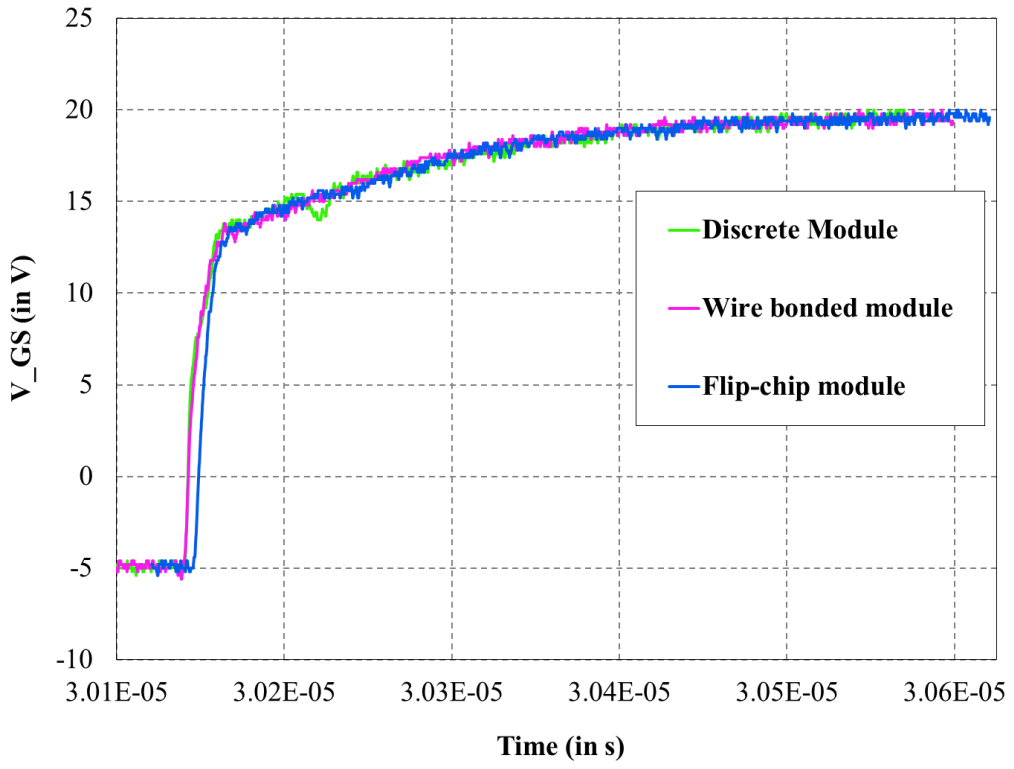
2.48E-05
Time (in s)
Discrete Module
Wire bonded module
Flip-chip module

(d)

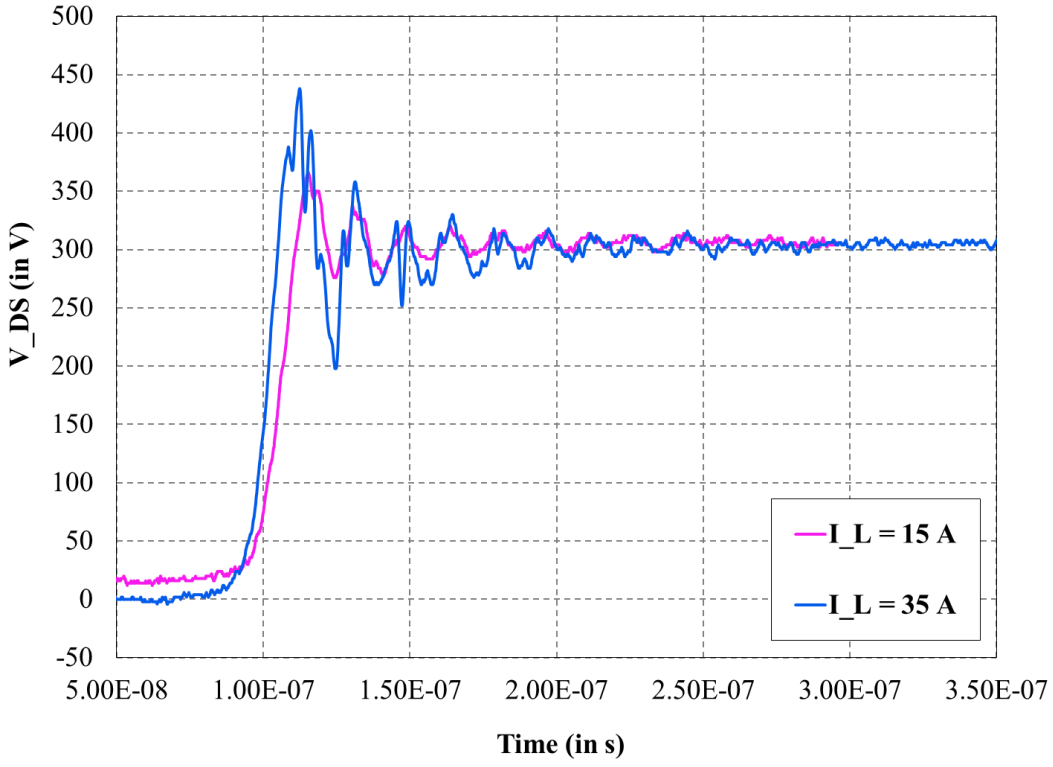


(e)

Figure 7.8: The double pulse measurement results for the three modules showing, (a) the voltage across the drain and source of the low-side MOSFET during the turn-off event, (b) the same during the turn-on event, (c) the load current waveforms, (d) the voltage across the gate and source of the low-side MOSFET during the turn-off event, and (e) the same during the turn-on event.

The effect of increasing the current level on the switching transients were explored next. The width of the first pulse was decreased to provide a current of 15 A. The overshoot and ringing in the voltage across the drain-source and gate-source were compared with the waveforms obtained for a 35 A load current. Figure 7.9(a) and (b) show the waveforms for the discrete module, illustrating the effect of the increased load current on the drain and source voltages respectively. An increase of nearly 100 V was observed in both the first overshoot and undershoot of the drain-source voltage. The gate voltage overshoot during turn-off was also found to increase significantly under the increased load current. Figure 7.9 (c) and (d) show the same set of waveforms for the wire bonded module. The increase in the drain-source overshoot is significant, but not as drastic

as the case of the discrete devices. The gate overshoot, however, does increase considerably. Driving the switch any faster may lead to a false turn-on event. The case for the flip-chip module is presented in Figure 7.9 (e) and (f). As can be observed from the drain-source waveforms, the overshoot does not show a significant increase even for more than 2× increase in the load current. The overshoot in the gate voltage waveform does in increase at 35 A from the flat-line at 15 A, but is still confined to a level below 0 V. This implies that the switching transitions may be even more aggressive before a false turn-on risk becomes imminent.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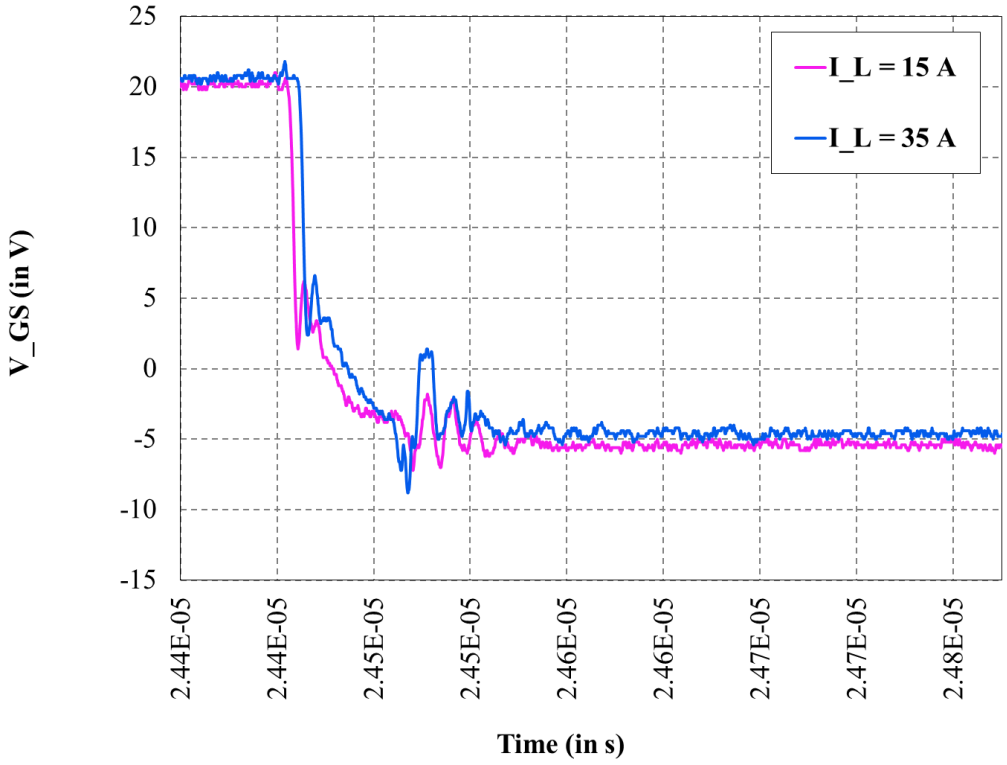
V_DS (in V)
5.00E-08
1.00E-07
1.50E-07
2.00E-07
2.50E-07
3.00E-07
3.50E-07
Time (in s)
I_L = 15 A
I_L = 35 A

(a)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V_GS (in V)
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2.45E-05
2.45E-05
2.46E-05
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2.47E-05
2.47E-05
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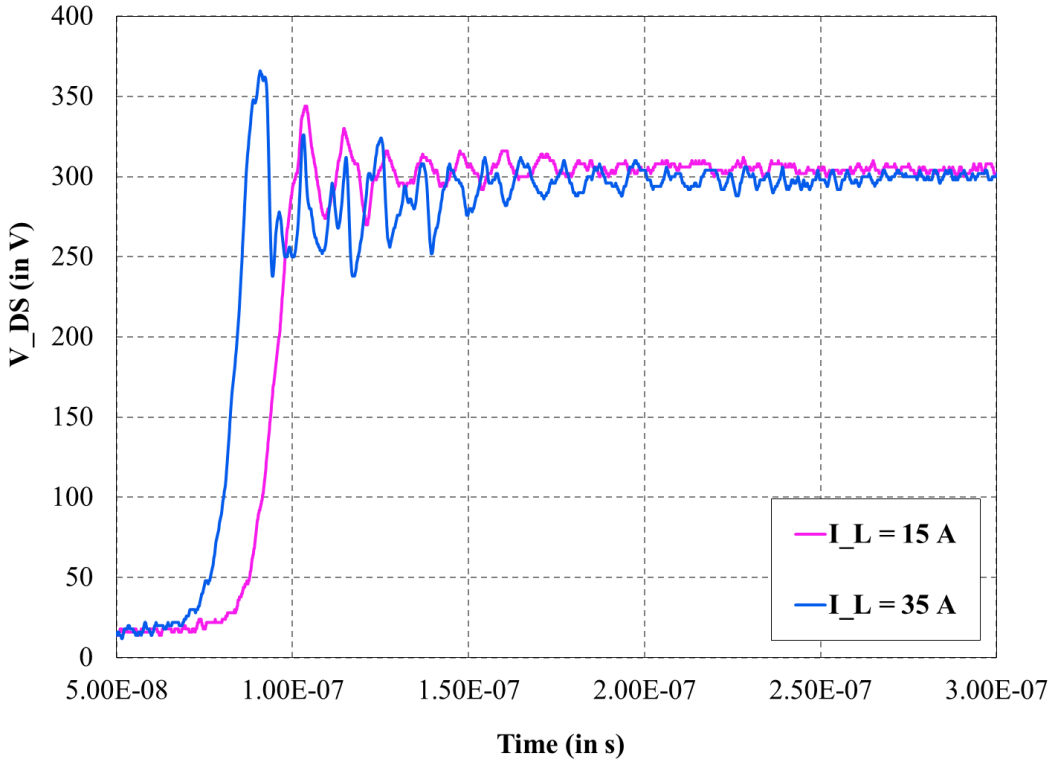
Time (in s)
I_L = 15 A
I_L = 35 A

(b)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V_DS (in V)
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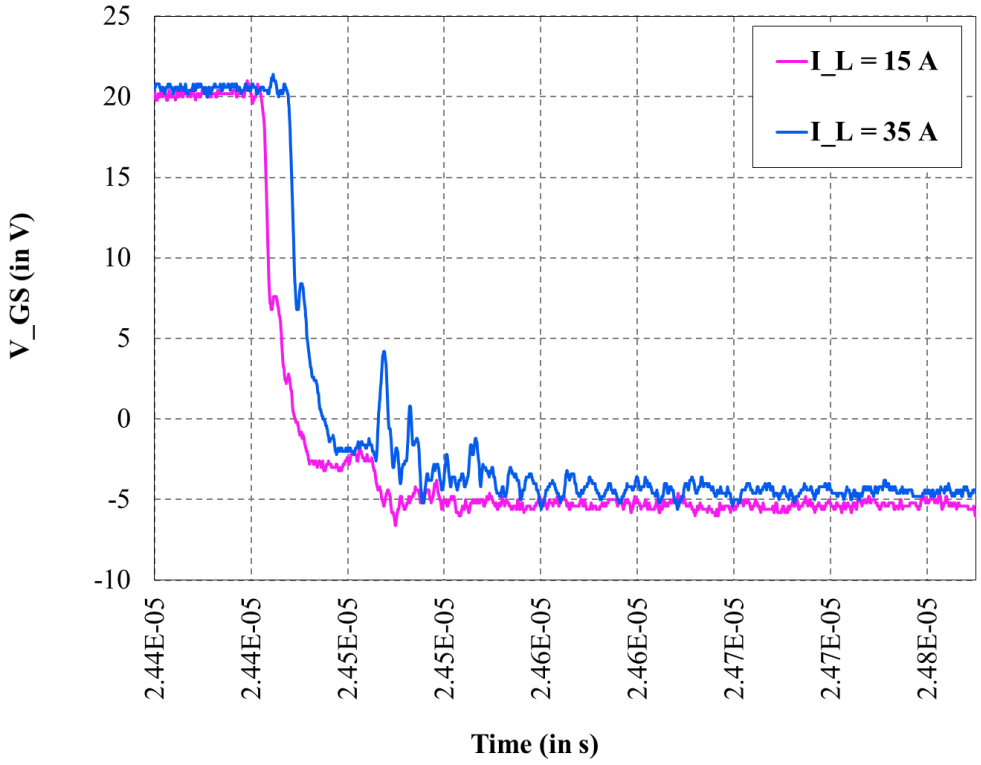
2.50E-07
3.00E-07
Time (in s)
I_L = 15 A
I_L = 35 A

(c)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V_GS (in V)
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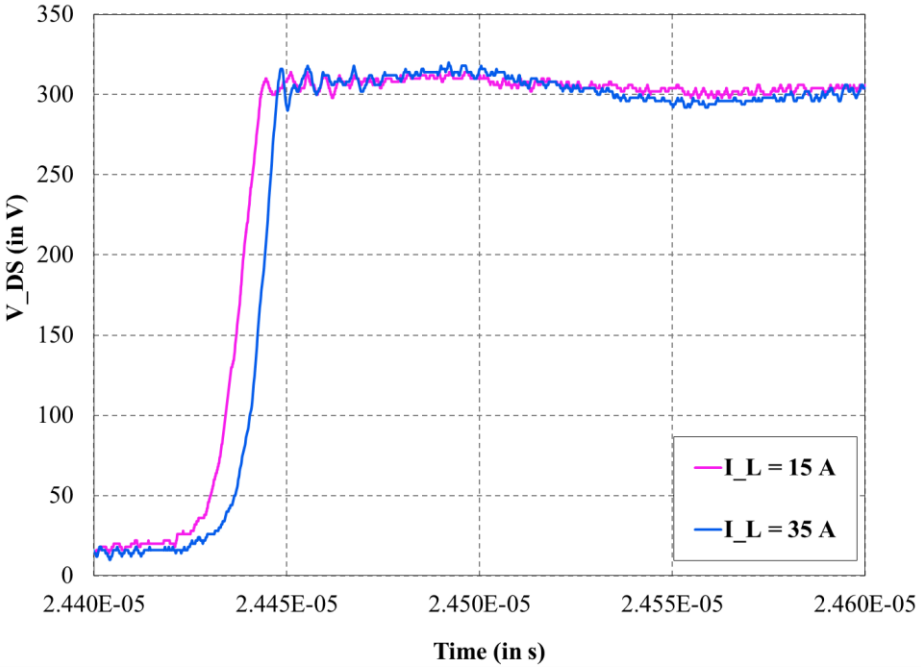
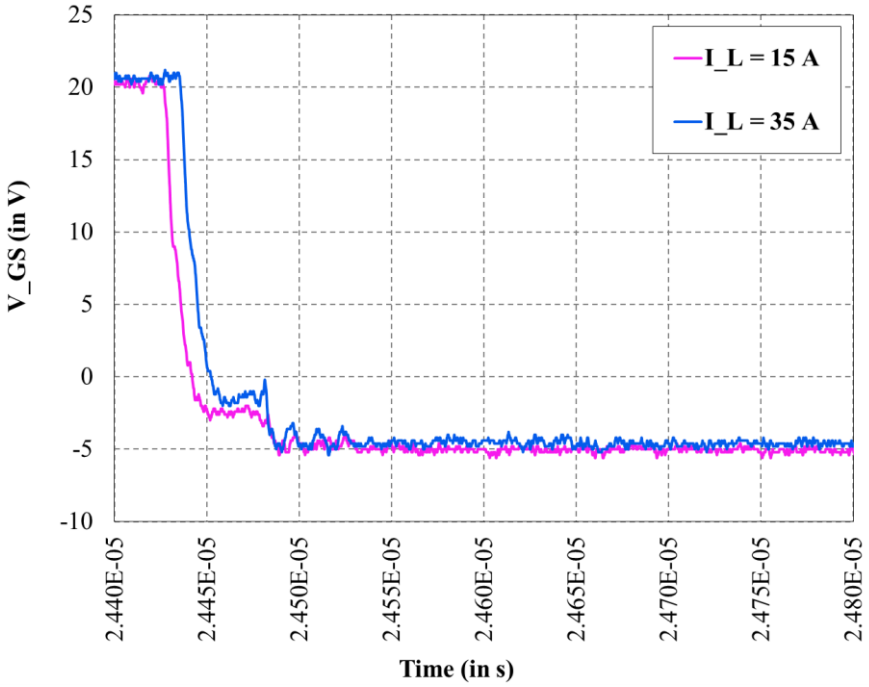
2.44E-05
2.45E-05
2.45E-05
2.46E-05
2.46E-05
2.47E-05
2.47E-05
2.48E-05
Time (in s)
I_L = 15 A
I_L = 35 A

(d)



(e)



(f)

Figure 7.9: Waveforms comparing switching characteristics for the three modules showing (a) the VDS for the discrete module, (b) the VGS for the same, (c) the VDS for the wire bonded module, (d) the VGS for the same, (e) the VDS for the flip-chip module, and (f) the VGS for the same.

The next investigation focused on extracting the actual parasitic loop inductances encountered by the switching currents. A very accurate method to estimate this is by the ringing frequency of the drain-source waveform during the turn-off event [3]. During this event, the parasitic loop inductance and the output capacitance of the device resonate to produce ringing. The output capacitance (C_{OSS}) of the device for a particular DC bus voltage is usually provided in the device datasheet, and the time period (Δt) of the ringing may be measured accurately using the oscilloscope cursors. The parasitic loop inductance (L_{loop}) may then be estimated using the following relation:

$$L_{loop} = \frac{\left(\Delta t / 2\pi\right)^2}{C_{oss}} \times 10^9 \; nH$$

Figure 7.10 shows the waveforms of the three modules at a DC bus voltage of 300 V. It was observed that the frequency of ringing for the flip-chip module was much higher than the discrete and wire bonded modules. This signified a highly-reduced parasitic loop inductance. To quantify this, the loop inductances for the three modules were calculated. The datasheet of the S2301UCSF from ROHM Semiconductor specifies an output capacitance of 110 pF at 300 V. Using this value the parasitic inductance of the flip-chip half-bridge was calculated to be only 4.88 nH. In comparison, the wire bonded module offered a loop inductance of 15.4 nH. Quite predictably, the discrete module offered the most parasitic inductance at 38.96 nH. The calculations are shown in Table 7.1.

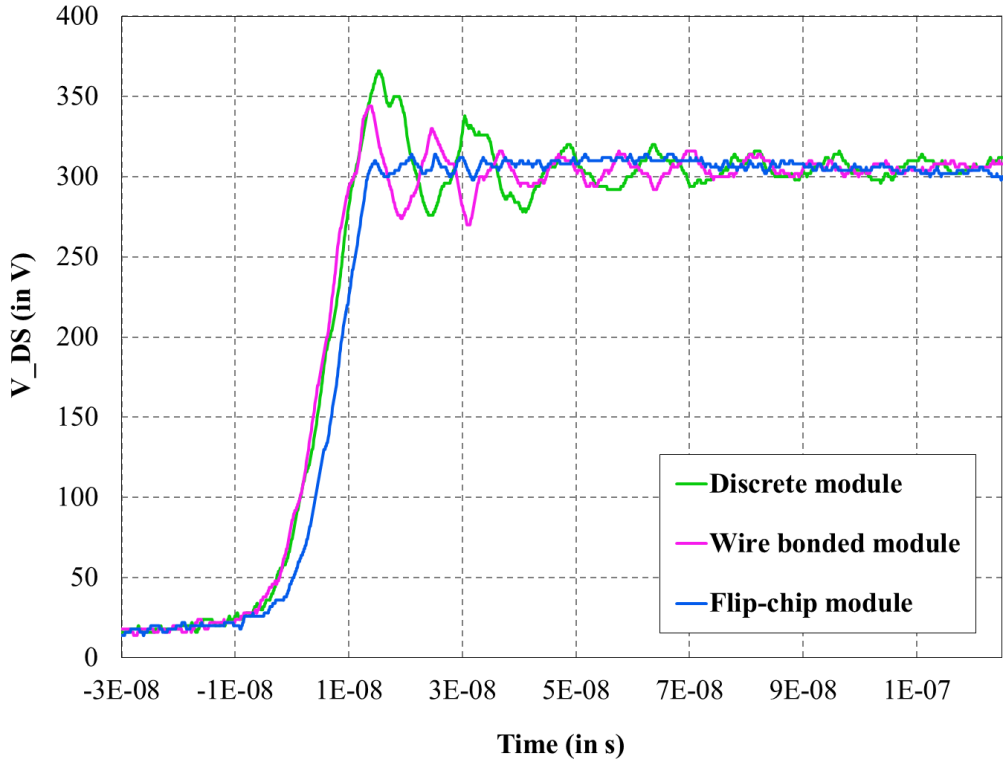


Figure 7.10: Waveforms for inductance estimation of the three modules, showing the turn-off waveforms for the drain-source voltage at a bus voltage of 300 V.

Table 7.1: A table showing the calculation of the parasitic loop inductances of the three modules under test.

Output capacitance of the MOSFET (C_{OSS})	Time period of ringing (s) (Δt)			Parasitic Loop Inductance (nH) = $\frac{(\frac{\Delta t}{2\pi})^2}{C_{OSS}} \times 10^9$		
	Discrete	Wire-bonded	Flip-chip	Discrete	Wire-bonded	Flip-chip
110e-12	13e-9	8e-9	4.6e-9	38.96	15.4	4.88

The low parasitic inductance offered by the flip-chip module was not only encouraging, but it also matched theoretical predictions closely. Figure 7.11 shows a comparison between the predicted and measured values of parasitic inductance for the wire bonded and flip-chip modules. The discrete module could not be simulated accurately in the absence of details regarding the

internal layout and wire bonding scheme. The comparison showed a very close agreement (within 5%) between the predicted and measured values.

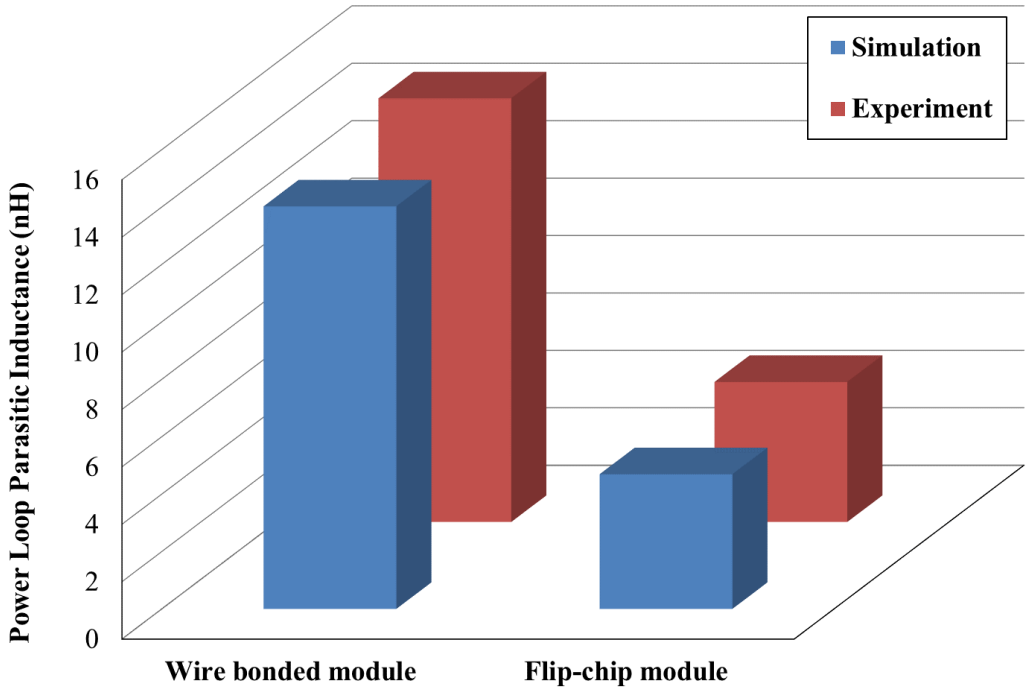


Figure 7.11: A bar graph showing a comparison between the simulated and measured values of the parasitic loop inductance for the wire bonded and flip-chip modules.

Conclusions

The system implementation of a novel flip-chip capable SiC power device was demonstrated. A GaN-like vertical power loop was realized using SiC power devices, and was estimated to yield a parasitic loop inductance of only 5 nH. Electrical testing of a fabricated half-bridge module confirmed this, producing very high quality switching waveforms. The measurements were compared with conventional half-bridge packages using discrete devices and a wire bonded module, and the parasitic inductance of the wire bondless module were found to be lower by at least a factor of 3. Despite the off-board gate driver, signal rise/fall times on the order of 16 ns

were measured. Finally, the actual parasitic inductance of the power loop of the modules was calculated from the ringing frequency of the output waveform, and there was very good agreement between the estimated and measured values.

References

[1] http://epc-co.com/epc/Portals/0/epc/documents/papers/Optimizing%20PCB%20Layout%20with%20eGaN%20FETs.pdf

[2] http://www.digikey.com/en/pdf/t/tdk/guide-flex-cracking-mlcc

[3] http://www.onsemi.com/pub/Collateral/AND9410-D.PDF

CHAPTER 8: A 3D Wire Bondless Half-Bridge Module using Flip-Chip SiC MOSFETs

Thus far, the superiority of wire-bondless flip-chip packaging of SiC devices has been clearly established. However, the developments so far have been aimed toward a larger goal—a 3D integrated power module. The flip-chip capable chip-scale packages will now be utilized to realize the 3D power module envisioned in Chapter 2. The module would be built around a central interposer, with gate drive and control inputs on one side and flip-chip power devices on the other. The passive devices for decoupling are also included within the module for cleaner switching waveforms.

The material of the interposer was chosen to be standard FR4 epoxy. The reason for choosing this over the initial LTCC proposition was explained in Chapter 2. The conductivity of LTCC thick film sintered metallization was not at par with the plated copper metallization available with printed circuit boards (PCBs). Also PCBs are able to provide large areas of copper for internal shielding planes for improving signal integrity. Attempts to co-fire thick internal planes in the LTCC process have resulted in warpage in previous experiences.

This chapter consist of three sections. The first section provides a description of the integrated power module and the layout details. The second section includes an estimation of the parasitic elements of the critical switching loops in the module. The third section provides description of the thermal management scheme of the module and also includes an estimation of the thermal profile under a typical thermal load. A final fourth section presents an evaluation of the switching characteristics of the module under double-pulse tests conducted across a range of voltages and load currents.

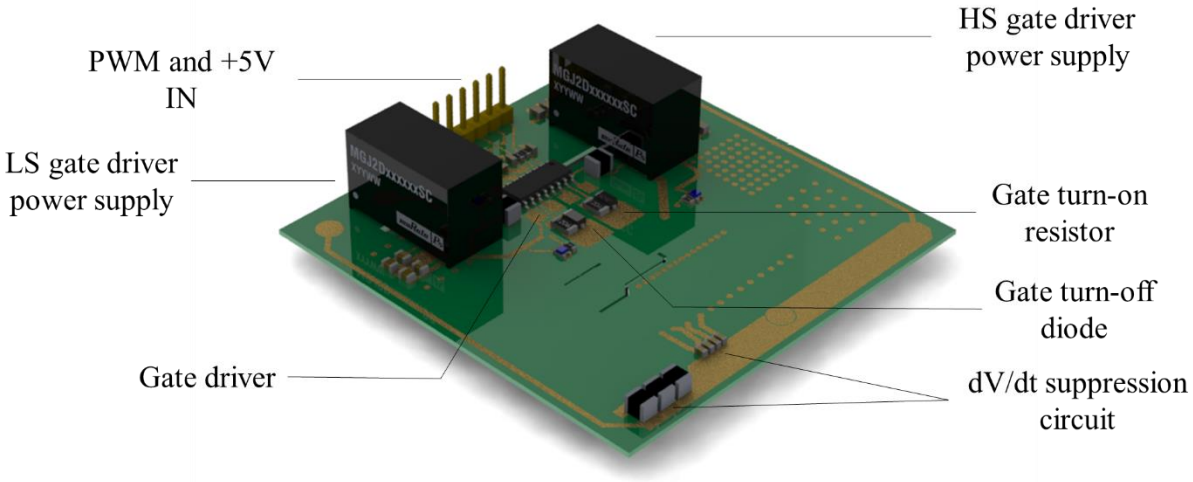
Section 8.1: The Integrated 3D Wire Bondless Half-Bridge

A concept of the proposed power module is presented in Figure 8.1. The electrical design of the module is a half-bridge, with a single MOSFET per switch position. In Figure 8.1(a) a 3D view of the power module is presented and shows the components on the top layer of the interposer. A 6-pin male header served as the entry point for the PWM signals and 5 V gate driver supply voltage from the DSP board to the module. Each of the signals—PWM1, PWM2, and 5 V—were provided with individual adjacent ground connections. Long connection wires are typically used to feed PWM signals from off-board microcontrollers to the gate driver. The stray inductance in the feed wire may cause undesired noise in the PWM signals. By providing adjacent ground connections and twirling the two wires tightly together, this stray inductance can be highly minimized due to a return-path cancellation effect. The gate driver for the module was the UCC21520DW gate driver from Texas Instruments. The gate driver had rated rise and fall times of 6 ns and 7 ns respectively, and a propagation delay of 5 ns. This half-bridge driver also had the provision for including a hardware dead time to prevent a shoot-through condition. This was a desirable feature for fast gate driver. The layout considerations for the gate driver provided in the datasheet were strictly adhered to [1].

In order to minimize the possibility of a false turn-on event under fast switching, there are a few recommended gate drive methods [2]. A combination of two of these methods were used in this module. First, a +20 V/ -5 V gate drive level was used for turn-on/ turn-off. The negative rail is usually recommended to ensure that the device is turned-off despite any possible gate voltage overshoots during turn-off. Secondly, an asymmetric turn-on and turn-off time was achieved by using different gate resistors during the two events. A common method used to achieve this is by using a gate resistor and anti-parallel Schottky diode between the gate driver output pin and the

gate of the device. From a survey of the literature, it was found that an on/off resistance ratio of about 2:1 was demonstrated to incur the least switching loss. This was achieved by using a series resistance of 5 Ω during turn-on. The internal gate resistance of the ROHM MOSFET was 6.8 Ω. During the turn-off event, the gate signal path would only experience this internal gate resistance, as opposed to 11.8 Ω during turn-on. Two separate DC-DC converters were used to provide the +20 V and –5 V voltage levels from the 5 V input from the microcontroller board. Through-vias were used to route the gate drive signals to the bottom layer of the board.

Figure 8.1(b) shows a rendering of the bottom side of the board. It shows the flip-chip type power MOSFETs bonded to a matching land pattern on the bottom surface of the interposer. The gate driver output was routed to the gate of the MOSFETs and a dedicated trace was also provided for the Kelvin source terminal. A Kelvin sense terminal was crucial to ensure that the gate loop does not encounter an increased loop inductance on the return path. This is a standard practice used routinely in the design of power modules [3, 4]. Decoupling capacitors were mounted in close proximity to the power MOSFETs in order to reduce the power loop parasitic inductance. It has been demonstrated previously in a flip-chip GaN half bridge module, that a vertical power loop has a much lower loop inductance as compared with a conventional lateral loop design. Instead of traversing the thickness of the board, the loop only extended from the bottom plane of the module to the next available interior plane. This resulted in a loop thickness of only 0.28 mm as compared to a 1.6 mm for a through-PCB vertical loop.



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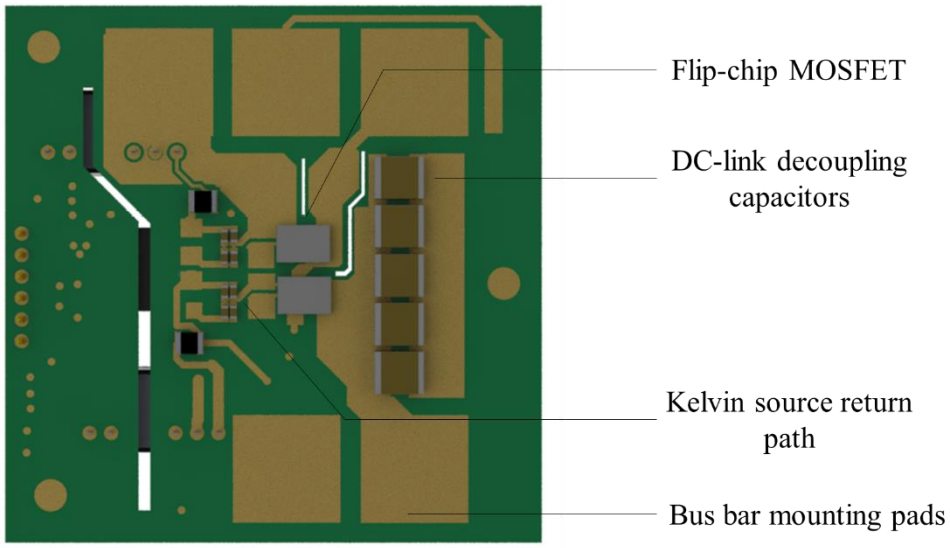


(b)

Figure 8.1: Artistic renderings of the 3D wire bondless integrated power module showing (a) a 3D view showing the top side of the module and (b) a bottom view of the same.

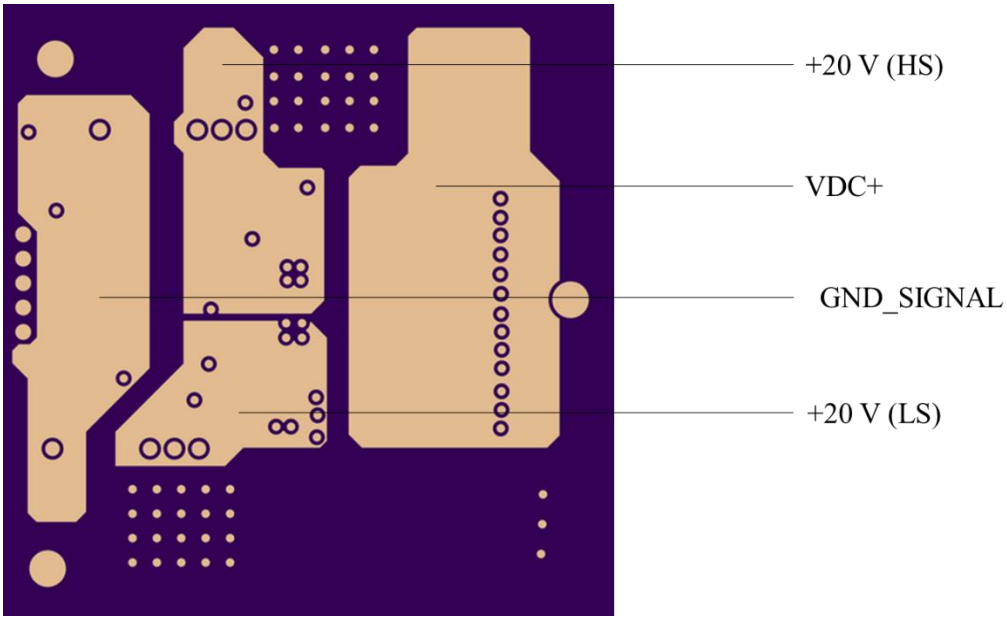
A *dv/dt* suppression circuit was also provided on the module. During high *dv/dt* switching events, current spikes ae injected into the heat sink through the parasitic capacitance between the

drain of the device and the heat sink. If the heat sink is electrically connected to the chassis of the power module enclosure, these current spikes could corrupt the gate driver circuit. An application note by Cree described a suitable procedure to prevent this conducted EMI from corrupting the gate signal [5]. In addition to isolating the heat sink from the chassis by floating it, any possible current spikes were coupled to the power ground through capacitors. The heat sink was also inductively connected to the chassis. If any high-frequency current spikes were accidentally injected into the heat sink, the inductors would prevent them from propagating to the entire system through the chassis.

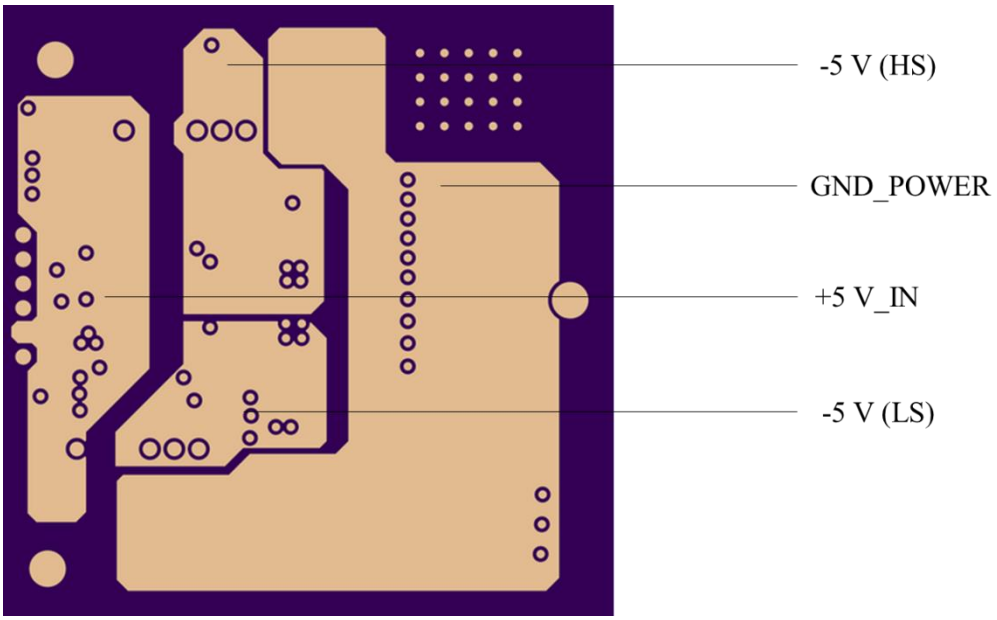
The interposer was a four-layer PCB. The routing in the top and bottom layers are visible in the rendering. The internal layers were principally used for power and ground planes. This is good practice for shielding and improving signal integrity. Figure 8.2 (a) and (b) show the copper plane designs for the first and second inner layers. The +5V input signal and the signal ground were allotted their own individual copper planes on separate layers. The same was true for the +20 V and -5 V rails from the DC-DC converters. Finally, the VDC+ and power ground were also routed to large copper planes beneath each other to minimize inductance and provide shielding. These large power and ground planes would also improve the current carrying capacity of the module.

The main current carrying traces were configured as surface traces on the bottom surface of the PCB. This was to provide a greater current carrying capacity as well. Surface traces do not get overheated as easily as embedded traces, and there are several PCB manufacturers that can provide up to 20 oz/ft^2 – 200 oz/ft^2 copper thickness for surface traces [6]. This significantly boosts the current capacity of the traces. In comparison, the internal conductor layer thickness of a PCB is confined to a few ounces of copper per square feet. The current routing was achieved using a minimum number of vias to lower the inductance. Wherever vias were required, a via-array was

used comprising multiple vias of 20 mil diameter. This ensured that the inductance was reduced to a fraction of a single via and that the current capacity was not compromised.



(a)

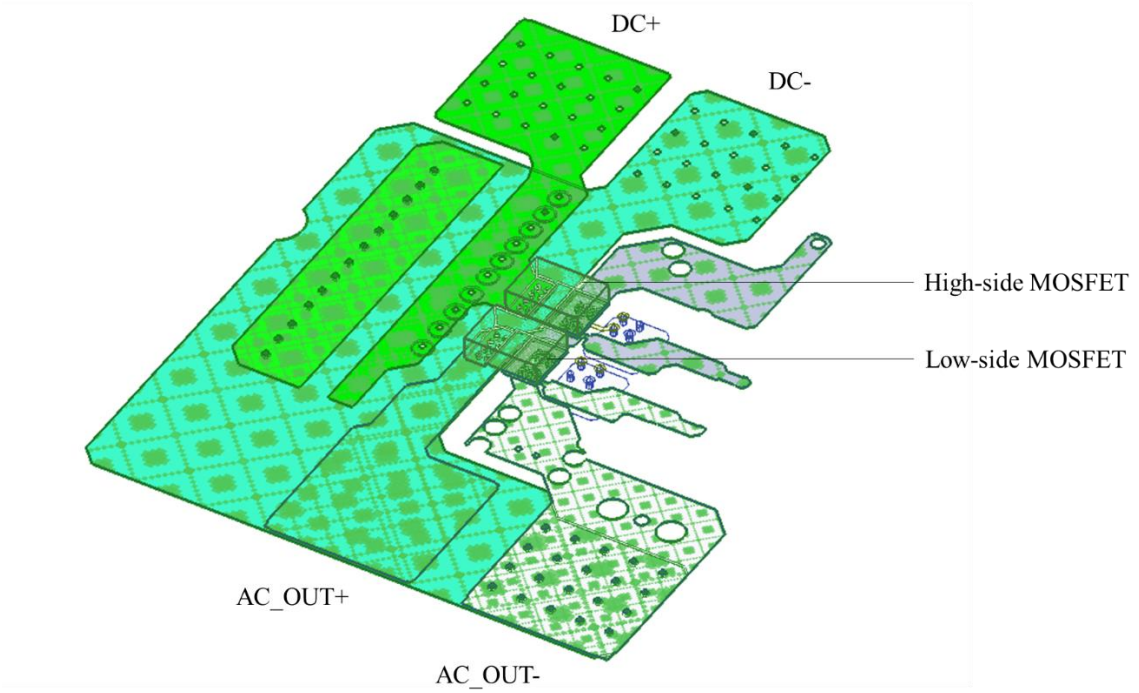


(b)

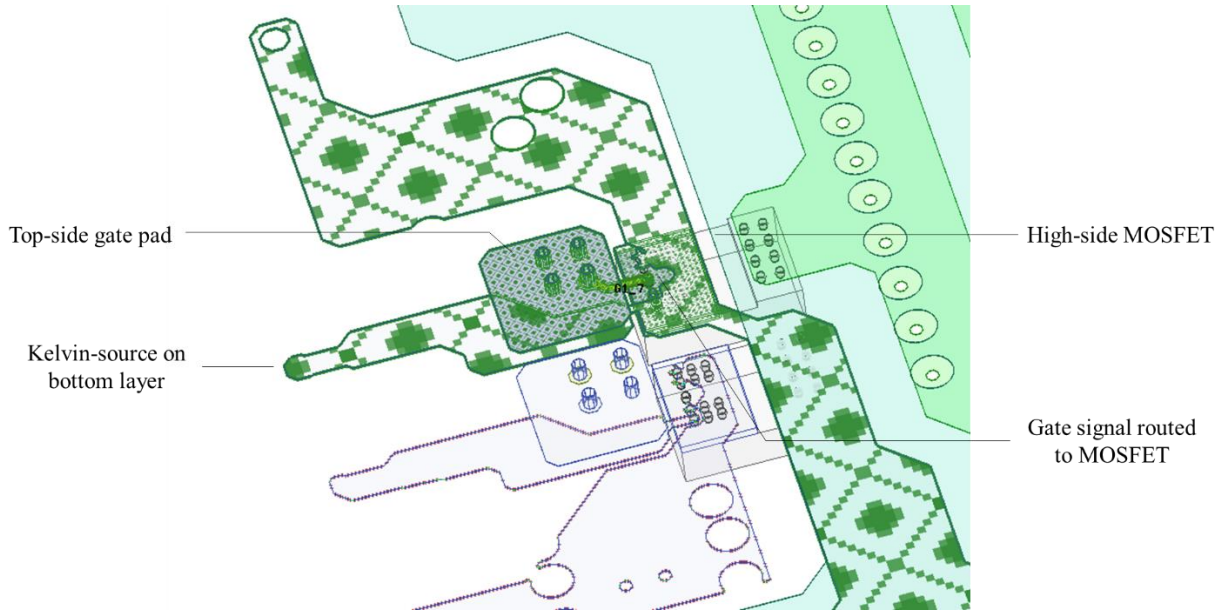
Figure 8.2: Renderings showing the copper areas of the (a) first inner conductor plane and (b) second inner conductor plane.

Section 8.2: Parasitic extraction

The reduced power loop and the close integration of the gate driver were the cardinal features of the proposed power module. However, an estimation of the critical loop inductances was required to verify the existing layout. A reduced model of the above layout was created and simulated in ANSYS Q3D to evaluate the parasitics. Figure 8.3(a) shows the power loop signal net for the module and Figure 8.3(b) shows the gate loop signal net for each power MOSFET. The solution frequency was configured to generate a sweep from 100 kHz to 10 MHz to study the nature of variation of the parasitic elements.



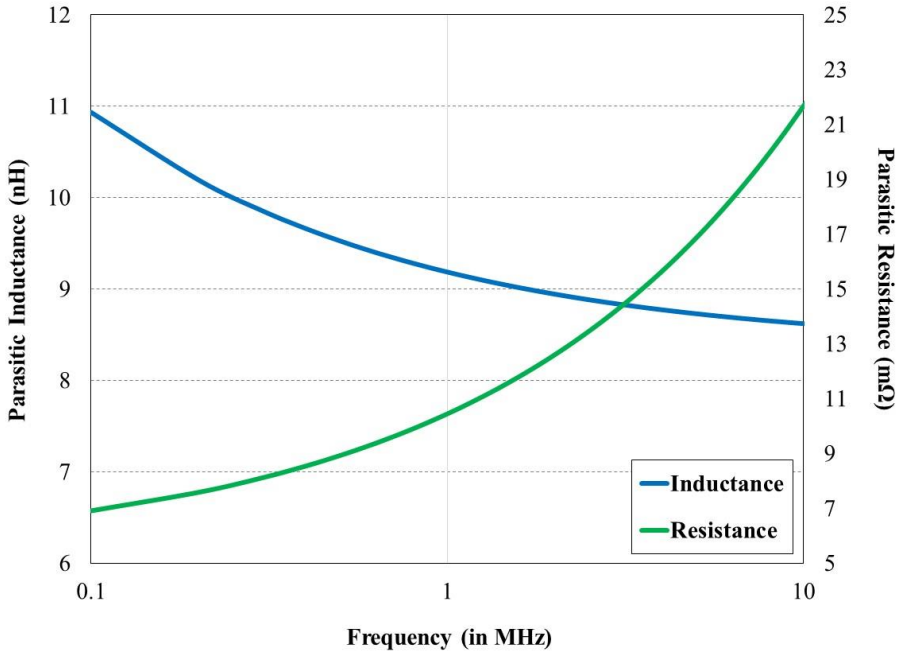
(a)



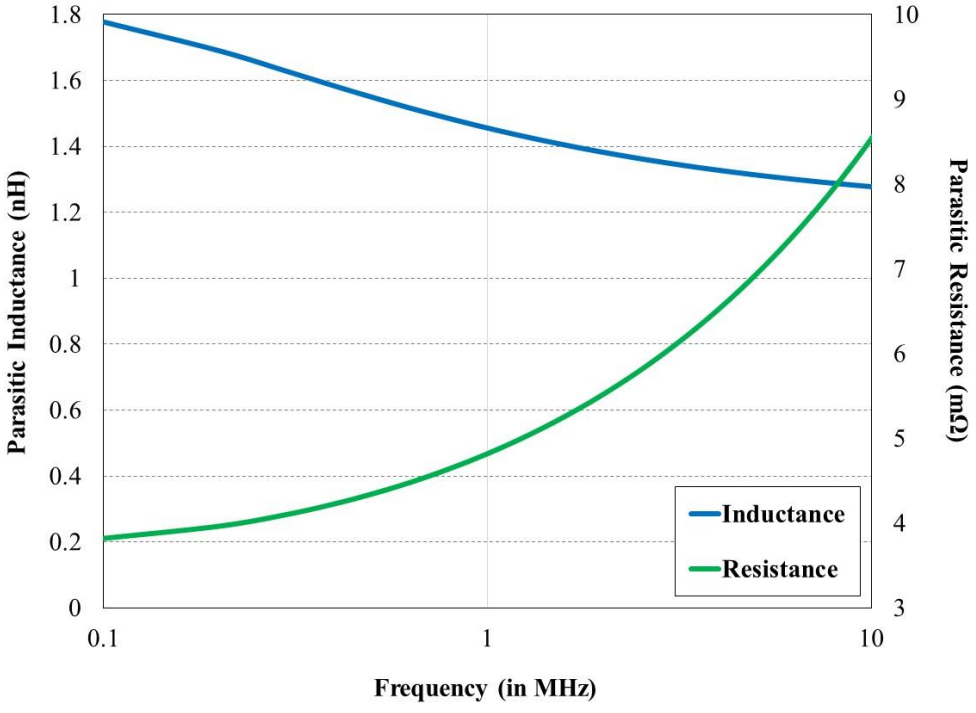
(b)

Figure 8.3: Parasitic analysis model in ANSYS Q3D showing (a) the power loop signal net and (b) the gate loop signal net.

The results of the analysis are shown in Figure 8.4. It was observed that both the power-loop and gate-loop parasitic inductances were very low. The low value of the gate-loop was expected because of the close coupling between the gate-driver output and the gate of the device. The estimated power-loop inductance was higher than the standalone wire bondless module demonstrated in the previous chapter. The main reason for this is the highly integrated nature of this module. While it is possible to place the critical components physically closer, it is difficult to route the wide power traces around them in a "smallest possible" loop. Also, it must be noted that the integrated module presented here is more of a system rather than a standalone module. When viewed from a system perspective, the slightly increased power-loop inductance was deemed acceptable. It was important to evaluate the variation of the loop resistances with frequency due to skin effect. The presence of through-vias in the system also runs the risk of adding resistance to the loops since the via plating thickness in standard PCBs is usually only tens of microns. This was a driving factor behind including via-arrays wherever applicable. From the parasitic analysis, however, any such concerns were mitigated. The parasitic loop resistances were negligible for both loops.



(a)



(b)

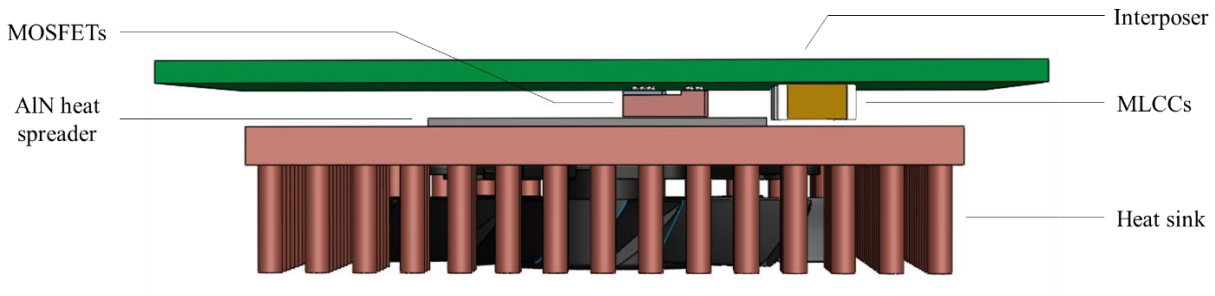
Figure 8.4: Results of the parasitic analysis of the integrated half-bridge showing (a) the variation of the power-loop parasitic inductance and resistance with frequency and (b) the variation of the gate-loop parasitic inductance and resistance with frequency.

Section 8.3: Thermal considerations for the integrated half-bridge

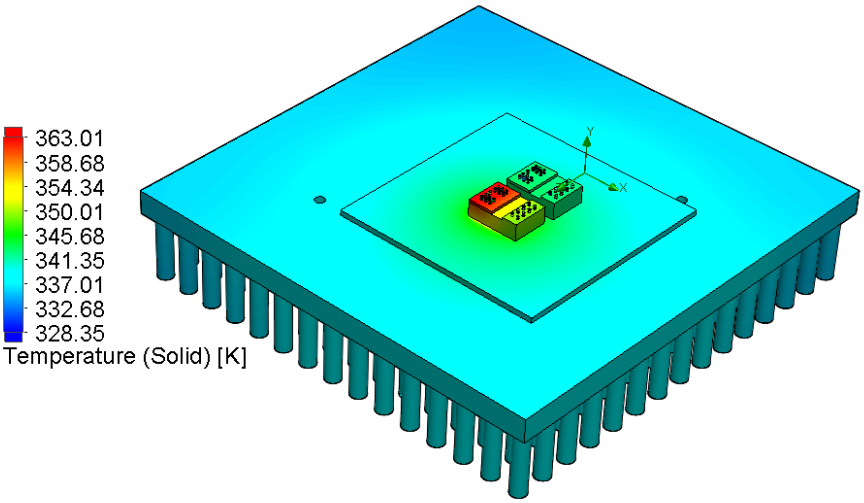
The principal means of heat removal for the integrated half-bridge module is identical to the standalone wire bondless half-bridge module described in the previous chapter. The bottom flat surfaces of the drain connector of the power MOSFET served as a low thermal-resistance interface to the heat sink. As before, one of the two devices were assumed to be conducting current at a given time, dissipating 32 W of heat. An identical integrated fan sink as was used as before in the interest of achieving a high power density.

The cardinal difference between the previous standalone module and this integrated module was the position of the DC-link decoupling capacitors. In this module, the MLCCs were placed very close to the MOSFETs on the same side of the board to have the greatest impact. This required that the height of the capacitors were lesser than or equal to the flip-chipped MOSFET packages. MLCCs with a high voltage rating and having a large capacitance value are typically quite thick. It is not feasible to have a bottom connector thickness of > 2mm, since it will be impossible to pass the chip-scale MOSFETs through a laminator for solder masking. At the same time, care must be taken to ensure that the heat sink did not contact the capacitor bank. Aside from the risk of developing an electrical short, there were two other factors to consider. Both factors are a consequence of the delicate nature of MLCCs. Firstly, MLCCs are usually not rated for high temperatures. It may be possible to run the SiC devices at a junction temperature of 150 ºC, but due to the ultralow thermal resistance of the flip-chip MOSFET, the heat may easily spread to the MLCCs. Secondly, thermal stress due to the heat and the mechanical pressure of mounting the heat sink may cause the MLCCs to crack. MLCCs crack relatively easily under the influence of seemingly inconsequential thermomechanical stresses like PCB flexure [7]. Hence, caution must be exercised to ensure that the MLCCs are not subject to additional stress.

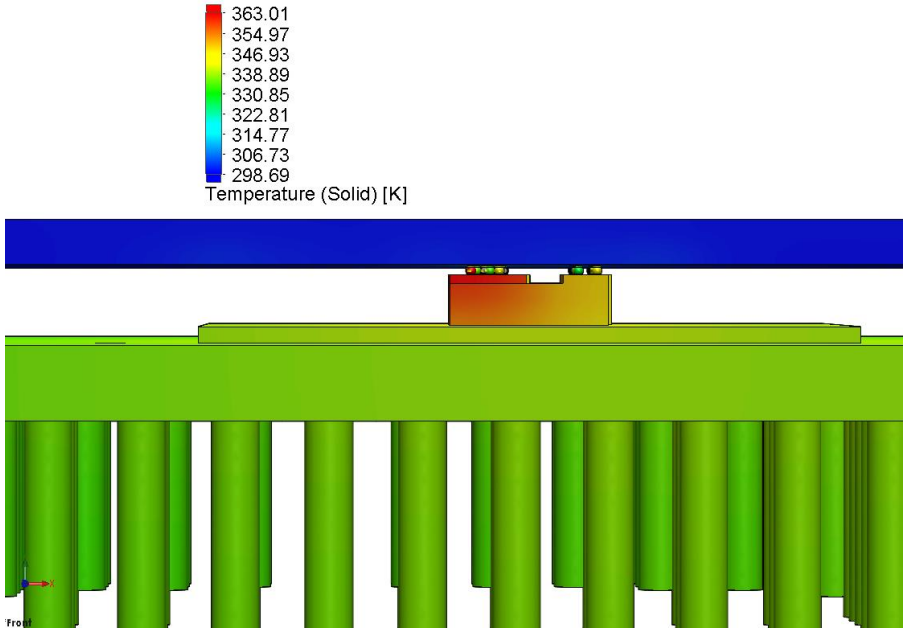
Fortunately, the thickness for 0.47 µF, 630 V (2220 footprint) MLCCs was almost equal to the mounted flip-chip MOSFETs. The heat sink was mounted on the bottom surface of the power devices using an AlN shim. The shim would also double as a heat spreader. This is represented in the schematic shown in Figure 8.5(a). The thermal profile across the power devices is presented in Figure 8.5(b). The maximum temperature on the device surface was found to be 90 ºC. Figure 8.5(c) shows a lateral thermal profile illustrating an ultralow thermal resistance despite adding the AlN heat spreader. The maximum temperature across the solder spheres was found to be 90ºC as well, thus justifying the choice of using inexpensive Pb62Sn36Ag2 material. Due to the inferior thermal conductivity of the FR4 material, the waste heat was not conducted to the passive devices and the gate driver IC. Thus, the junction temperature of the devices may be allowed to reach a high temperature without risking damage to the typically-lower-temperature-rated passive devices and ICs. The temperature across the capacitor pad area also remained cool, showing that the MLCC temperature would not rise under the influence of thermal load. Thus, in more ways than one, the inferior thermal conductivity of the FR4 material turned out to be beneficial in protecting the lower temperature rated components in the module from the risk of damage. A thermal plot of the interposer is shown in Figure 8.5(d) to illustrate this fact. Figure 8.5(e) and (f) show the thermal profiles of the top of the power device and bottom of the copper connector respectively, and the package thermal resistance was calculated as 0.34 ºC/W. Upon an inspection of the thermal profile of the AlN shim, it was observed that the temperature was very close to that of the bottom of the metallic connector. Hence, its inclusion added negligible thermal resistance to the system. As demonstrated earlier, the thermal resistance of contemporary wire bonded SiC modules is still larger than the calculated values for the integrated wire bondless half-bridge.


MOSFETs
AlN heat spreader
Interposer
MLCCs
Heat sink

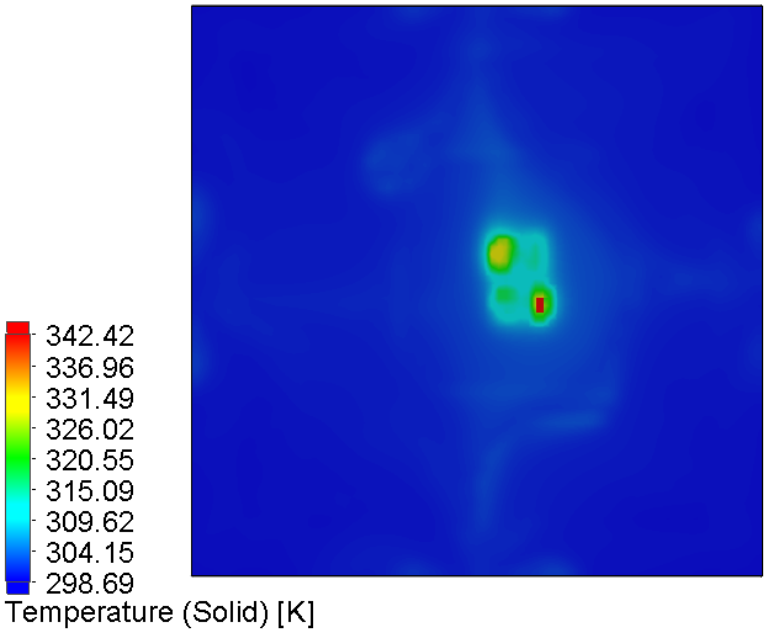
(a)


363.01
358.68
354.34
350.01
345.68
341.35
337.01
332.68
328.35
Temperature (Solid) [K]
Y
X

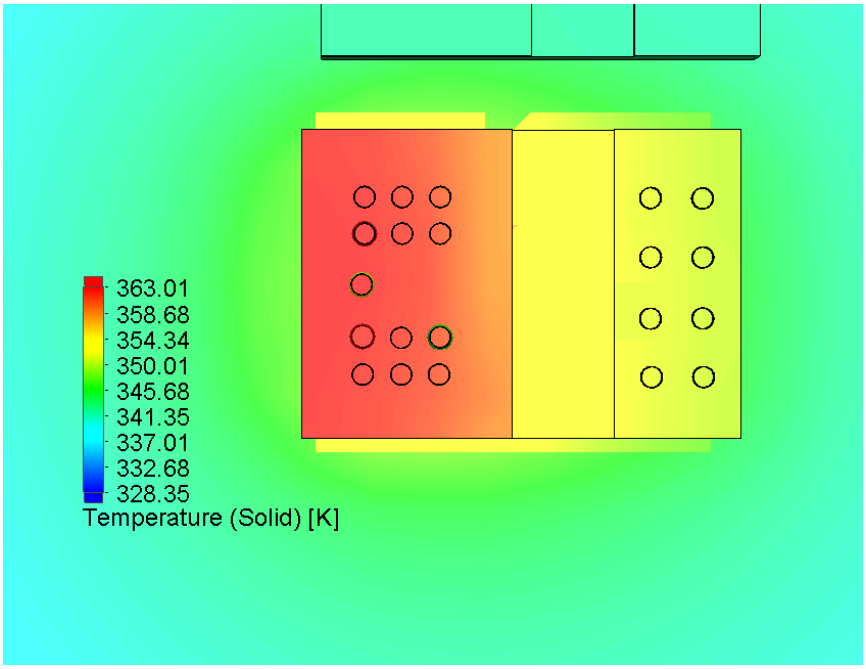
(b)


363.01
354.97
346.93
338.89
330.85
322.81
314.77
306.73
298.69
Temperature (Solid) [K]

(c)


342.42
336.96
331.49
326.02
320.55
315.09
309.62
304.15
298.69
Temperature (Solid) [K]

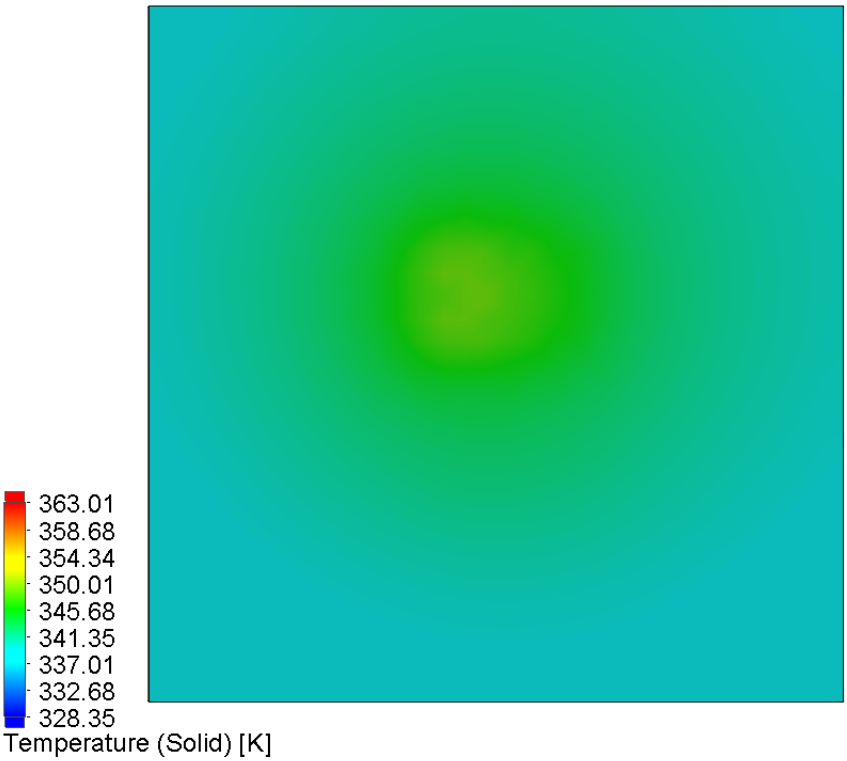
(d)


363.01
358.68
354.34
350.01
345.68
341.35
337.01
332.68
328.35
Temperature (Solid) [K]

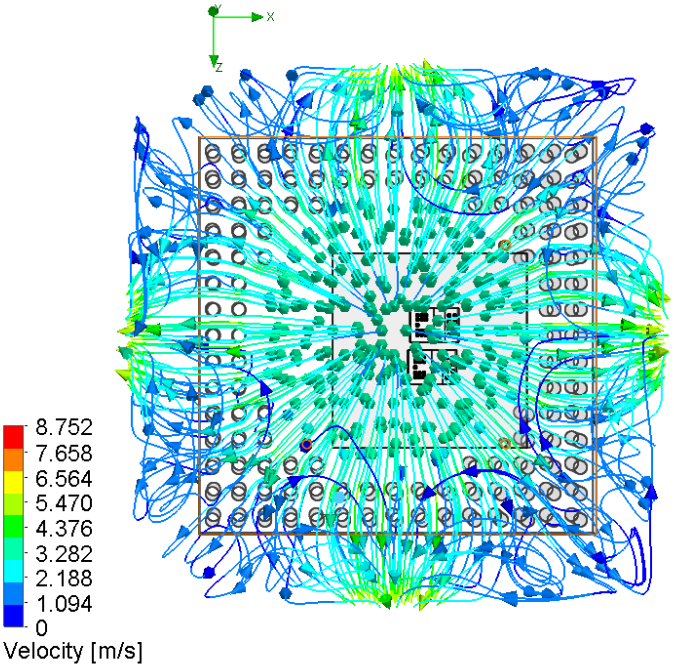
(e)


363.01
358.68
354.34
350.01
345.68
341.35
337.01
332.68
328.35
Temperature (Solid) [K]

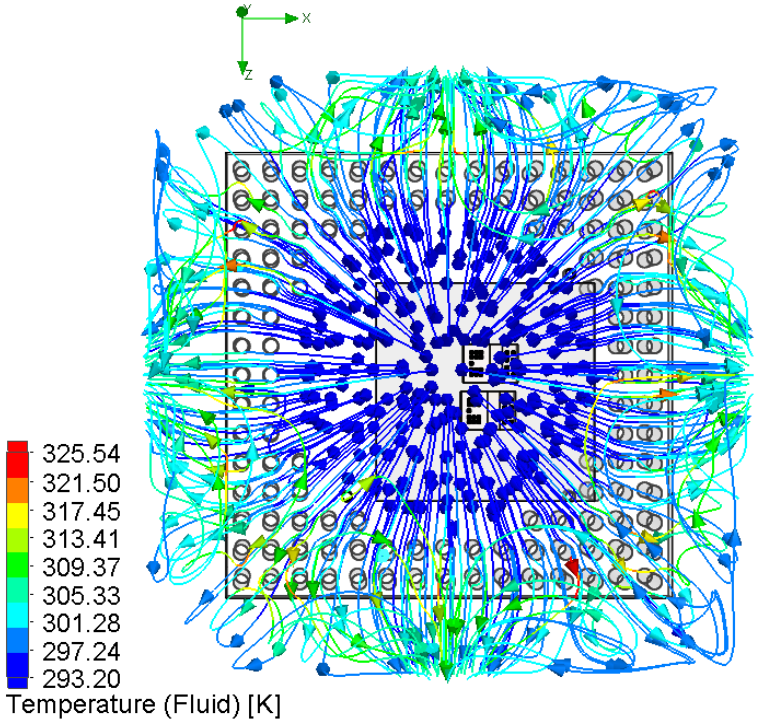
(f)


363.01
358.68
354.34
350.01
345.68
341.35
337.01
332.68
328.35
Temperature (Solid) [K]

(g)


X
Z
8.752
7.658
6.564
5.470
4.376
3.282
2.188
1.094
0
Velocity [m/s]

(h)



(i)

Figure 8.5: Thermal management in the integrated power module showing (a) the mounting of the heat sink on the flip-chip MOSFETs without contacting the capacitors, (b) a 3D thermal map showing the thermal profile across the power devices (interposer hidden from view), (c) a lateral view of the thermal map, (d) the thermal map on the bottom surface of the FR4 interposer, (e) a zoomed-in view of the thermal profile on the top surface of the power device, (f) a zoomed-in of the thermal profile on the bottom of the metal connector, and (g) a zoomed-in view of the thermal profile on the bottom side of the AlN heat spreader, (h) a contour map showing the velocity of air through the heat sink pins, and (i) a contour map showing the temperature of the same.

Section 8.4: Electrical test results

Double-pulse tests were conducted on the integrated wire bondless half-bridge to determine whether its performance was acceptable under high levels of *dv/dt*. The gate and source terminals of the high-side MOSFET were electrically shorted to reduce its functionality to a diode. The PWM input for the low-side MOSFET was supplied via an external DSP board. The 5 V signal for the gate driver was also routed from the same DSP board. The active status of the +5 V and the +20 V/-5 V rails, and the gate driver output was verified through observing the status of the blue

LEDs. All three LEDs were found to be active indicating proper functioning of the gate drive circuit. The gate resistor and diode were not placed to keep the devices protected from any possible anomalies in the gate signal. Figure 8.6 shows a photograph of the blue LEDS signifying proper operation of the gate drive circuitry.

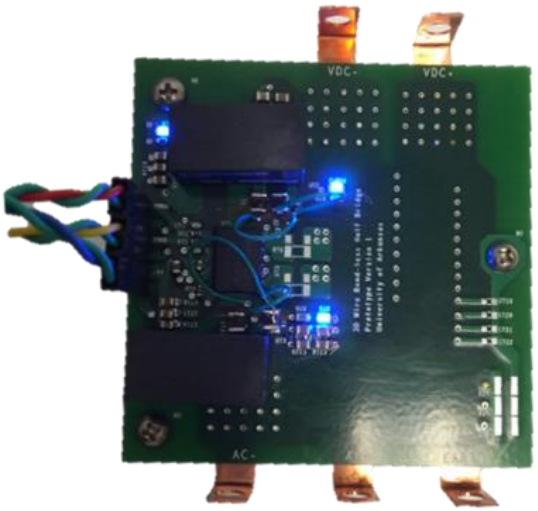
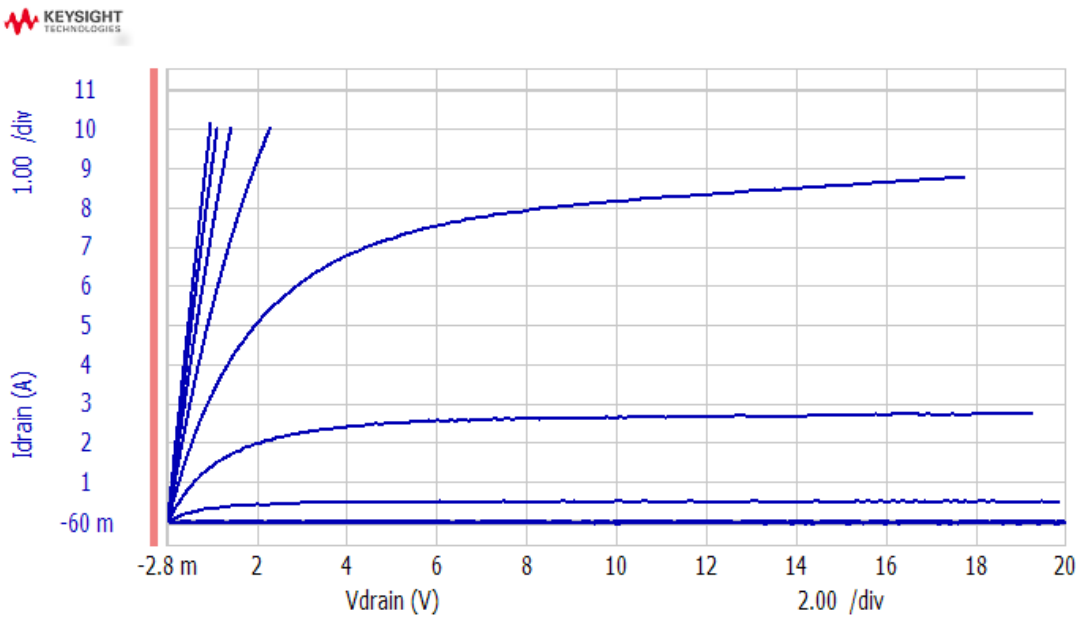
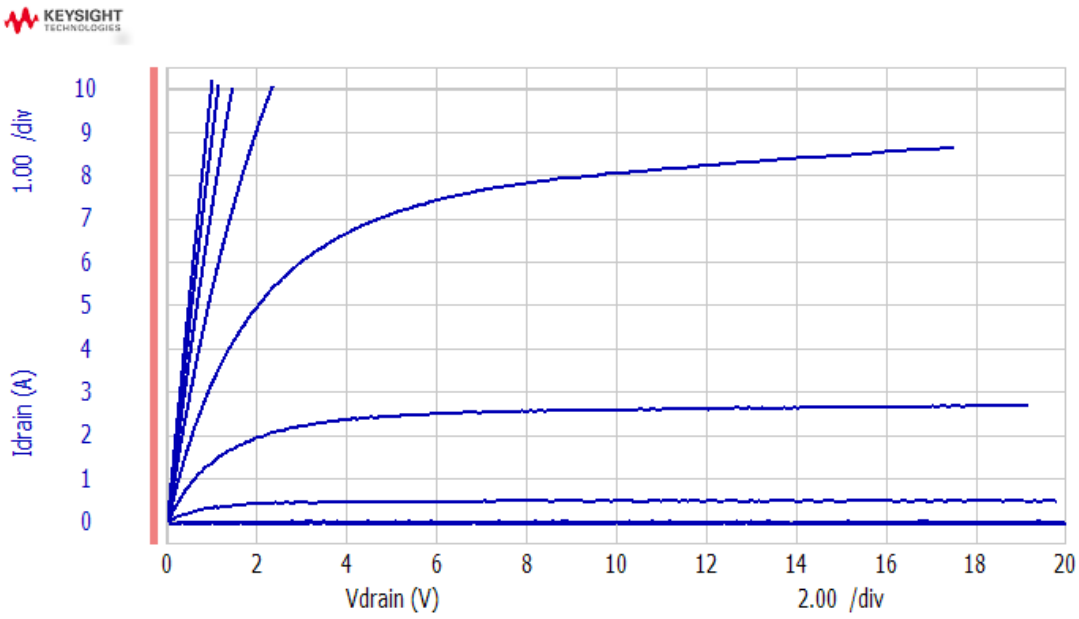


Figure 8.6: Photograph showing the status LEDs on the top side of the interposer.

It must be noted that the process flow for the assembly of the flip-chip MOSFETs on the interposer was identical to the processes described in the previous chapters. The remaining components were soldered on after assembling and under-filling the MOSFETs. However, before soldering the rest of the components, it was important to ensure that the MOSFETs were physically connected to the board and electrically functional. In order to verify this, the static characteristics of the two MOSFETs were plotted on a Keysight B1505 curve tracer.



(a)

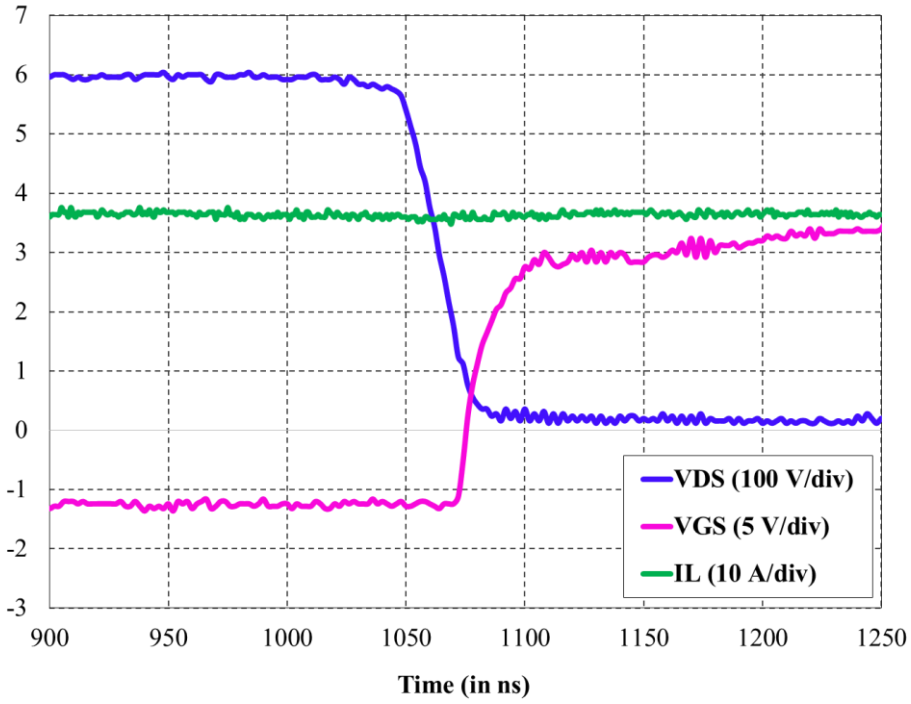


(b)

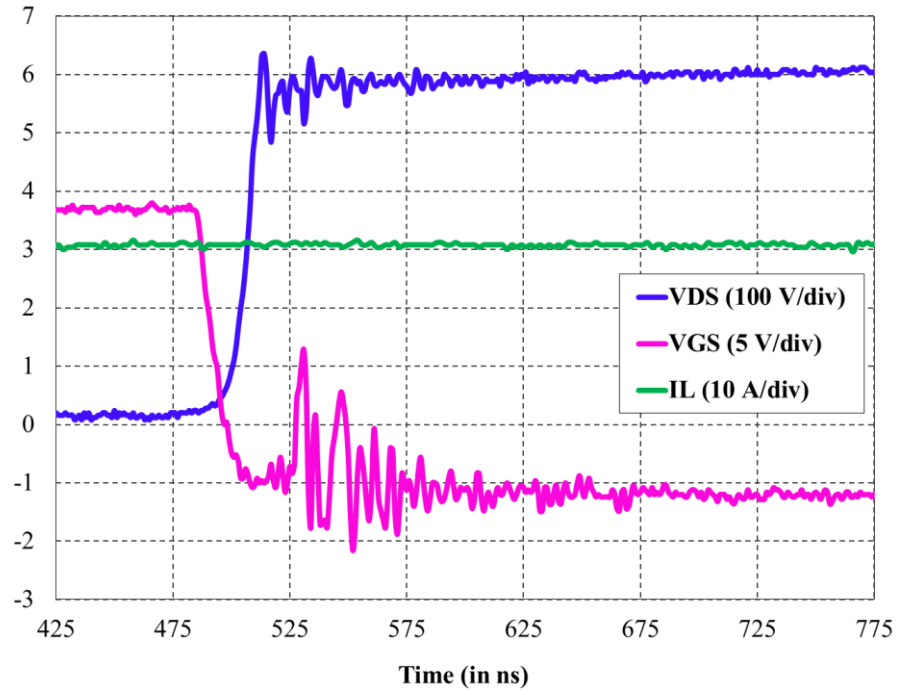
Figure 8.7: The static characteristics of the flip-chip bonded MOSFETs for the (a) high-side MOSFET and (b) low-side MOSFET.

The double pulse tests were conducted in an incremental fashion by increasing the DC-bus voltage gradually from 100 V to 600 V. At each step, a load current of 10, 20, and 30 A was drawn

in steps. The effect of the increasing *dv/dt* and di/dt will be presented in this section. Figure shows the waveforms of the circuit operating at 600 V, while supplying a load current of 30 A. The turn-on time for the MOSFET was only 28 ns, which corresponds to a *dv/dt* of 17 V/ns. It must be noted that the turn-on for the MOSFET was controlled by a 5 Ω gate resistor. The turn-off time for the drain-source voltage was measured to be 20 ns, corresponding to a *dv/dt* of 24 V/ns. The turn-off is quicker since the gate signal bypasses the gate resistor through the anti-parallel diode. As mentioned before, the asymmetric turn-on/off is good practice for minimizing switching losses in SiC MOSFETs. However, despite intentionally slowing down the turn-on event, there was no significant penalty in terms of time. It was very encouraging that the gate drive circuit remained stable under these aggressive *dv/dt* rates. The gate voltage did exhibit some overshoot during turn-off, however this was observed to be influenced by an increase in current levels rather than *dv/dt*. Also, the probes used for measurement were of 200 MHz bandwidth and were very sensitive to noise and parasitics in the measurement loop. The probes were fitted with a coil spring to form the shortest measurement loop possible. Most often, observed distortions were found to be manifestations of the inductive effect of the measurement loop, rather than the true signal itself. For example, in the gate-source waveform shown in Figure 8.8(b), a false-turn on would be observed if the overshoot of the gate was truly 5 V. The drain-source waveform at turn-off showed no signs of false switching. In fact, the maximum overshoot during the turn-off event was only 4.67%. Hence, it may be ascertained that the overshoot observed in the gate was a result of coupled noise from another oscilloscope channel during the switching transition.



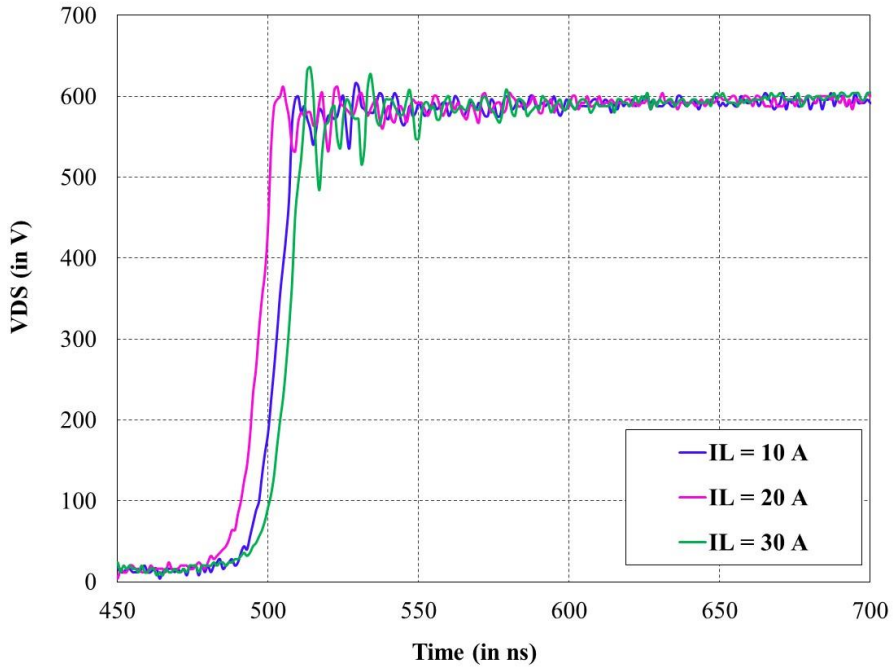
(a)



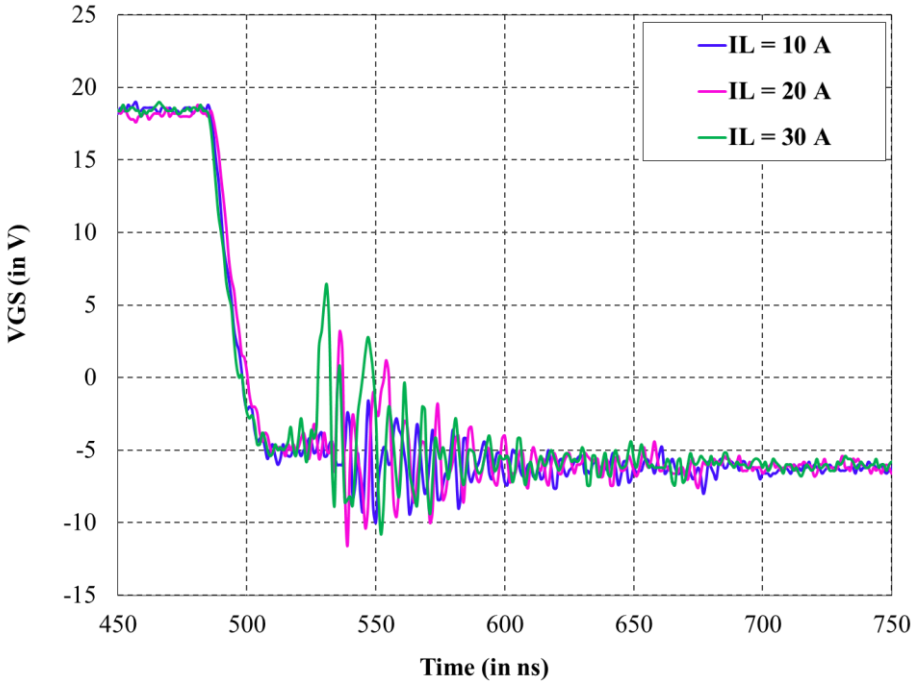
(b)

Figure 8.8: Waveforms showing the (a) turn-on and (b) turn-off switching events at 600 V, 30 A.

The variation of the drain-source voltage waveform and gate voltage waveform with increasing load current is shown in Figure 8.9. It was observed that the overshoot increased considerably as the load current levels increased. An increase in the VDS overshoot was expected due to an increase in the *di/dt* in the power loop. The increase in the overshoot of the gate waveform, however, was not intuitively apparent. As mentioned before, if the large > 5V overshoot between the gate and source of the MOSFET was indeed occurring, it would manifest itself as a false turn-on in the V_{DS} waveform. The stable off-state of the power device confirmed that the observed overshoot in the gate signal was either a possible artefact of measurement or an anomaly arising from the high *dv/dt* the output of the MOSFET. In the future, it may reap benefits to measure the gate voltage waveforms with all other oscilloscope channels disconnected.



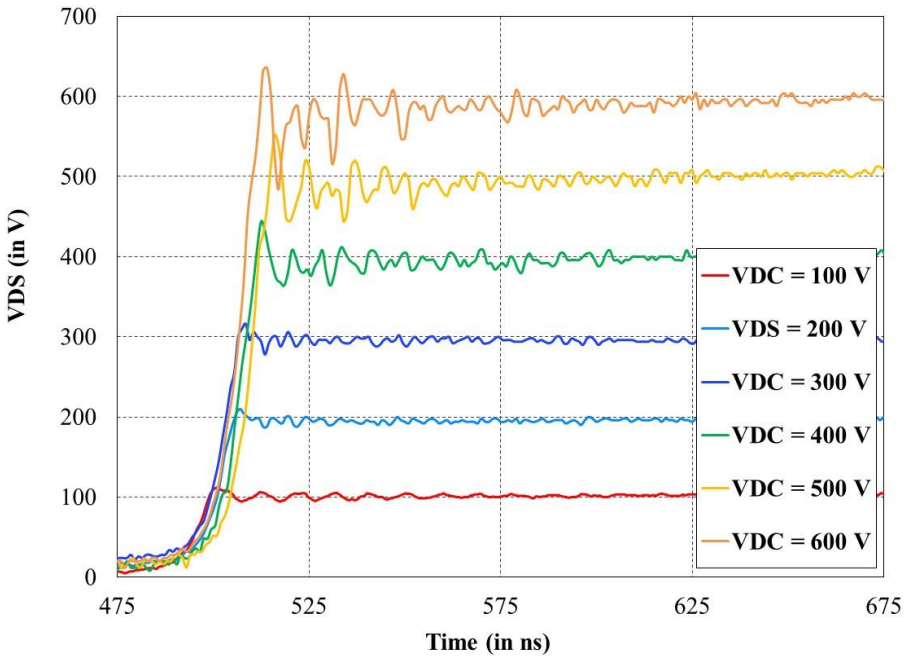
(a)



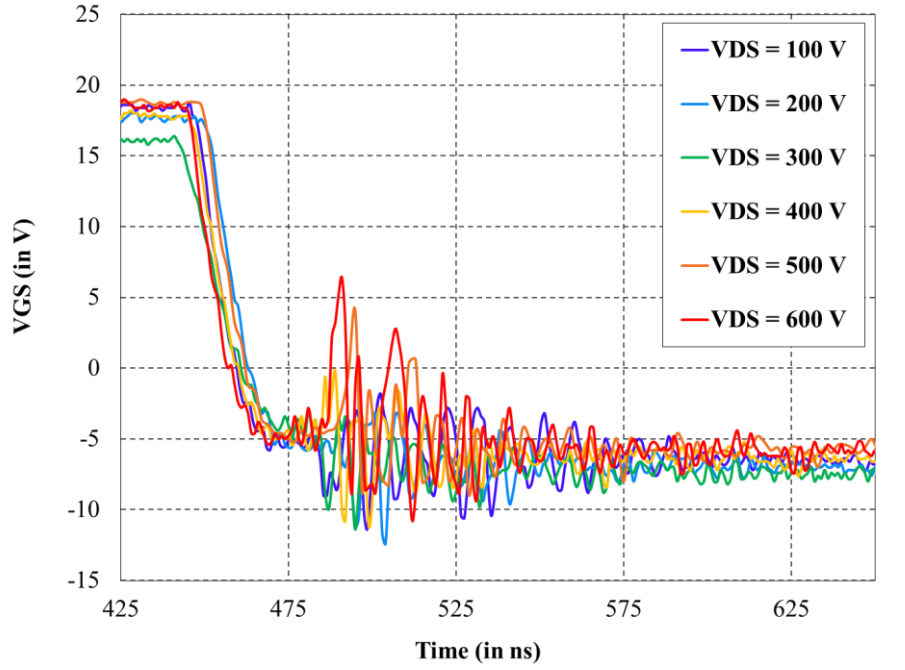
(b)

Figure 8.9: (a) The V_{DS} waveforms as a function if increasing load current and (b) the gate waveforms for the same.

The variation of the V_{DS} and V_{GS} with increasing DC bus voltage was studied as a next step. All waveforms were compared at a load current of approximately 30 A. It was observed that the overshoot in the VDS waveform increased steadily with increasing *dv/dt*. The ultralow parasitic inductance of the power loop ensured that the overshoot levels were insignificant even at the maximum DC bus voltage. The overshoot in the gate waveforms were confined to levels below 0 V during turn-off up to a DC bus voltage of 400 V, but the levels rose to 0-5 V when the DC bus voltage was increased beyond 400 V. This is shown in Figure 8.10(b). It is plausible that this is the result of the injection of spurious current spikes through the parasitic capacitances in the system due to increased *dv/dt*.



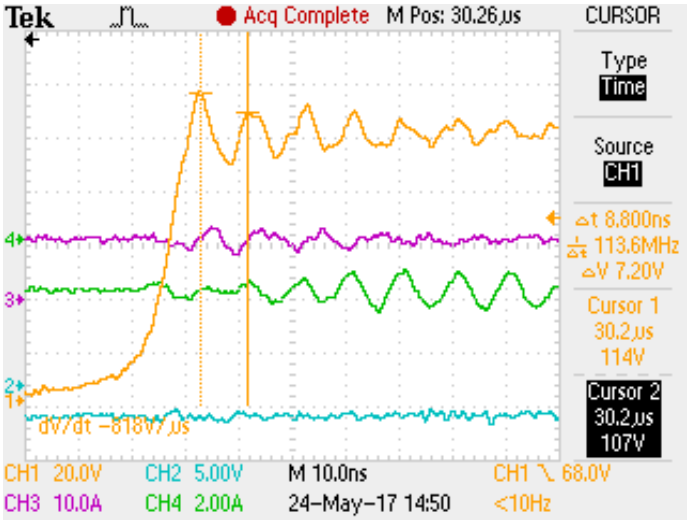
(a)



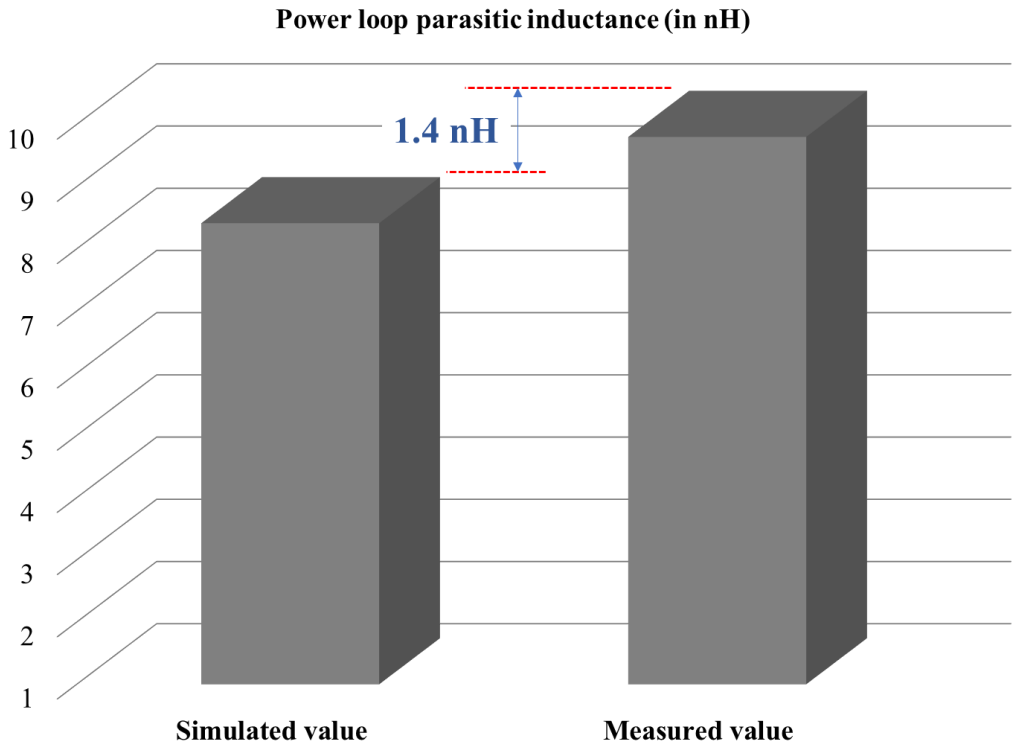
(b)

Figure 8.10: Waveform comparisons showing (a) VDS and (b) VGS as a function of increasing DC bus voltage.

Proof of the ultralow parasitic inductance offered by the 3D integrated half-bridge is clearly apparent from the highly reduced output overshoot. However, quantifying the parasitic inductance encountered by the load current is an important step. In order to estimate this inductance accurately, the time period of the ringing was measured at a DC bus voltage of 100 V. A relatively lower bus voltage was chosen for this measurement since the waveform is significantly less distorted at this bus voltage [Figure 8.10(a)]. The output capacitance of the S2301UCSF MOSFET at a bus voltage of 100 V is 200 pF. The measured time period of the ringing was 8.8 ns, and a screenshot of the oscilloscope during this measurement is presented in Figure 8.11(a). This returns a value of 9.8 nH for the parasitic inductance of the power loop and the calculation is shown in Table 8.1. As can be observed in Figure 8.11(b), this value differs from the predicted simulation result by only 1.4 nH. This re-iterated the significance of a well-defined finite element simulation in predicting the design and characteristics of innovative and novel power module designs. This not only improves confidence in proposed aggressive design approaches, but also reduces the need for expensive and time-intensive design re-spins.



(a)



(b)

Figure 8.11: (a) A screenshot of the oscilloscope waveform showing the measurement for the time-period of the ringing and (b) a bar graph comparing the simulated value of power loop inductance with the measured value.

Table 8.1: A table showing the calculation of the loop inductance of the integrated wire bondless half-bridge.

Output capacitance of the S2301UCSF MOSFET at 100 VDC (C_{oss}) (pF)	**Measured time-period of ringing (Δt) (ns)**	**Parasitic loop inductance (L_{loop}) = $\frac{(\Delta t/2\pi)^2}{C_{oss}} \times 10^3$ (nH)**
200	8.8	9.8

Conclusions

A novel 3D integrated SiC power module was demonstrated. The power device interconnections were completely wire bondless. The module was tested up to 600 V, and in excess of 30 A. The output switching waveforms demonstrated excellent stability despite recording slew rates of around 20 V/ns. The gate waveforms were very stable up to a DC bus voltage of 400 V. Beyond 400 V, the gate overshoot during turn-off was observed to increase. It could not be ascertained whether this was in fact true, or whether the high *dv/dt* was causing measurement artifacts to appear. Despite the observed overshoot, there was no observed false turn-on event at the output of the power device. The total power loop parasitic inductance was < 10 nH, and the predicted value matched the measured value to within 1.4 nH. It must be noted that the drain current switching waveforms were recorded using two separate methods—a Rogowski coil and a current transformer. However, both attempts resulted in a failure to produce usable waveforms due to the bandwidth limitation of the measurements. At the high slew rates observed in the module, perhaps a current shunt would produce reasonable results without adding inductance to the power loop.

References

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[3] Z. Wang, X. Shi, Y. Xue, L. M. Tolbert, F. Wang and B. J. Blalock, "Design and Performance Evaluation of Overcurrent Protection Schemes for Silicon Carbide (SiC) Power MOSFETs," in *IEEE Transactions on Industrial Electronics*, vol. 61, no. 10, pp. 5570-5581, Oct. 2014.

[4] H. Li and S. Munk-Nielsen, "Challenges in Switching SiC MOSFET without Ringing," *PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Nuremberg, Germany, 2014, pp. 1-6.

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CHAPTER 9: Conclusions and Future Directions

Silicon carbide is the only mainstream power semiconductor system to have never explored wire bondless integration. Ironically, it is perhaps the material that will benefit the most from its use. Without any complicated layout optimization, a simple change from a wire bonded to a flip-chip approach significantly benefited the signal quality in the modules demonstrated during the course of this work. 3D integration was also demonstrated by utilizing the flip-chip packaging approach to realize a condensed power module with integrated gate-drive.

The benefits of a three-dimensional and vertically routed system are intuitively apparent, and have been demonstrated to provide seminal benefits in GaN and Si-based power electronics modules alike. Based on this precedent, this dissertation started out with a vision for a SiC analog. To reap the reliability benefits associated with a near-perfect CTE match, the system was designed around an LTCC interposer. The concept was rigorously evaluated against thermo-mechanical and electrical feasibility using finite-element simulations. As expected, the system provided very low thermal stresses and parasitics as compared to the state-of-the-art. From a manufacturing standpoint and physical implementation perspective, however, there were a few concerns.

The standard thick-film sintered metallization for the LTCC process left a lot to be desired. While the low electrical conductivity offered by this metallization may be adequate for routing low power signals associated with the digital circuits, its fidelity and practicality for power traces and planes was deemed a major concern. A second concern was choosing an appropriate method for the flip-chip attachment of the bare die SiC power devices. Common solder and sintered silver are among the most common die-attach materials used in contemporary power modules. Sintered silver has already established its superiority over solder in terms of physical properties. However,

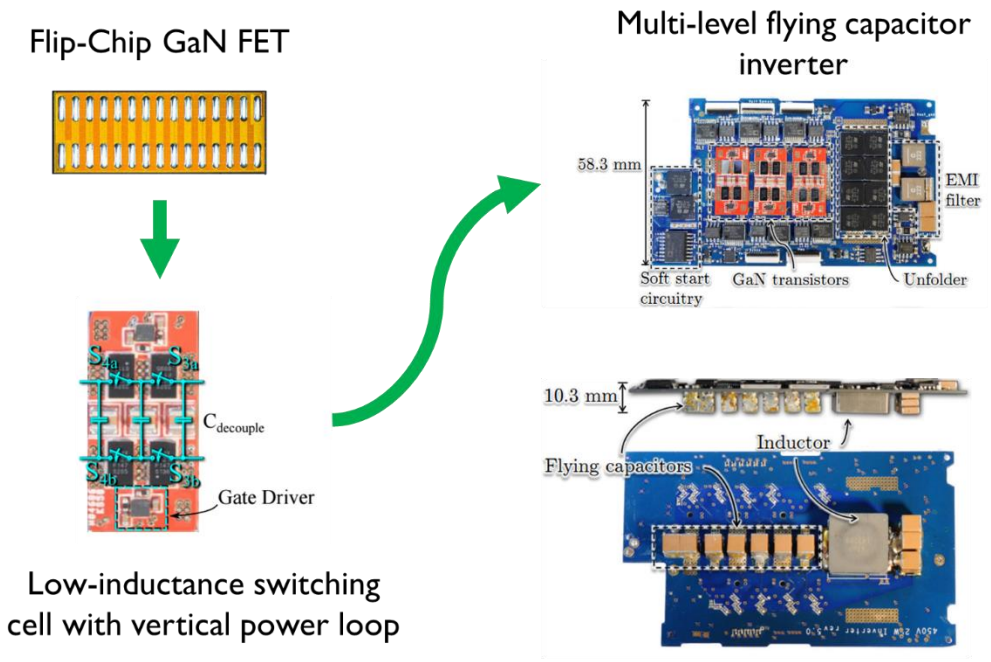
from the user's point-of-view, sintered silver processing is not consistent. The bond line is not flat, has inconsistent voiding and thickness, and there is significant extrusion of the paste out the side of the die and up its sidewalls. This makes it completely unsuitable for two-sided bonding in a 3D topology without risking an electrical short and/or breakdown. A process for controlled and defined bonding using sintered silver was explored through novel sintered silver preforms. The preforms were completely customizable—they could be tailored to fit the shape and size of the bond pads on any bare die power device with a chosen thickness. The preforms demonstrated a very high bonding strength that remained undiminished across hundreds of rigorous thermal shock cycles.

Owing to the aforementioned concerns with using LTCC as a multilayer interposer for routing vertical interconnections, FR4 was chosen as an alternative. FR4 technology is extremely mature, and is also available in a host of flavors targeted toward very specific high-demand applications. They do not have a limit on the voltage and current rating, and have a proven track-record in being highly reliable. Keeping cost, serviceability, and simple implementation process at the forefront—an ultralow inductance chip-scale power device package was proposed. It possessed a 14× smaller footprint than a discrete power device, and demonstrated a performance that exceeded a custom wire bonded module. The novel package was evaluated in software and was demonstrated to provide identical benefits as the LTCC scheme which was conceived earlier. All this despite a highly economical choice of materials. The proposed device was completely scalable, both in size and performance. A simple reselection from commercially available materials could tailor it toward more demanding applications. The same module may also be realized using an LTCC material system provided the metallization concern is addressed. LTCC is an extremely capable material system with certain properties that are much superior to FR4. They have proven benefits

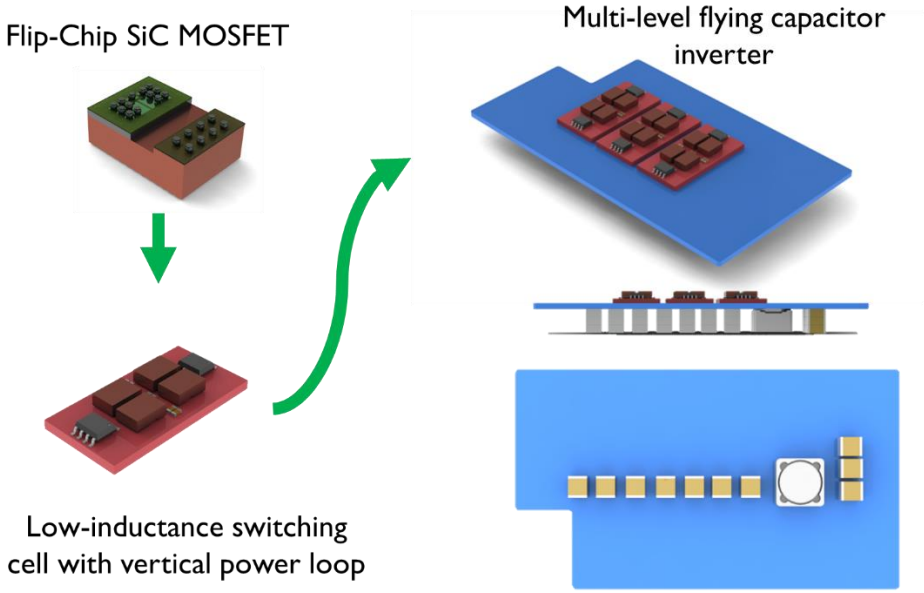
in RF and microwave circuits for a reason. However, remedies such as direct thick copper plating of vias and traces must be explored before the LTCC material system is power-electronic-ready.

The developed packages were used to construct two varieties of a half-bridge module—one with a vertical power loop with off-board gate drive and another with a semi-vertical power loop with an on-board gate drive. The vertical loop implementation produced textbook switching waveforms, with highly reduced overshoots as compared with a lateral power loop used in the state-of-the-art. Increasing the load current had a negligible impact on the fidelity of the signals. For the integrated module, the results were similar for the output waveforms. However, beyond a DC bus voltage of 300 V, the high *dv/dt* in the power loop resulted in some undesired overshoots in the gate signal. This was likely a measurement artefact resulting from spurious current spike injection into the oscilloscope ground during the switching events. The overshoot did not trigger a false-turn on event or cause any fault in the isolated gate drive circuits. This was an encouraging step, especially since the output voltage rise and fall times were of the order of 15-20 ns. This translated to *dv/dt* rates of the order of 20 V/ns. It is also important to note that this was achieved without using an external free-wheeling Schottky barrier diode.

The flip-chip power device gives the system designer the flexibility to be highly creative in conceiving novel low-inductance design topologies. Just like flip-chip GaN has inspired high density multi-level power converter topologies [1, 2], flip-chip SiC packages may usher in a wave of multi-level SiC converters for high-voltage applications. A concept representing this analogy is shown in Figure 9.1.



(a)



(b)

Figure 9.1: A concept showing the extension of a multilevel inverter concept to flip-chip SiC devices illustrating (a) the existing design for a GaN-based multilevel inverter and (b) the envisioned concept of the same using flip-chip SiC devices.

Flip-chip capable power devices also enable the scope of 3D stacking of power devices and enable double-sided cooling of the same. Without wire bonding tolerances to incorporate, it is possible to densely pack multiple devices in the space that one wire bonded power device would have occupied. Additionally, this can be done in multiple vertical tiers, thus further densifying the power capability. One such concept is shown in Figure 9.2.

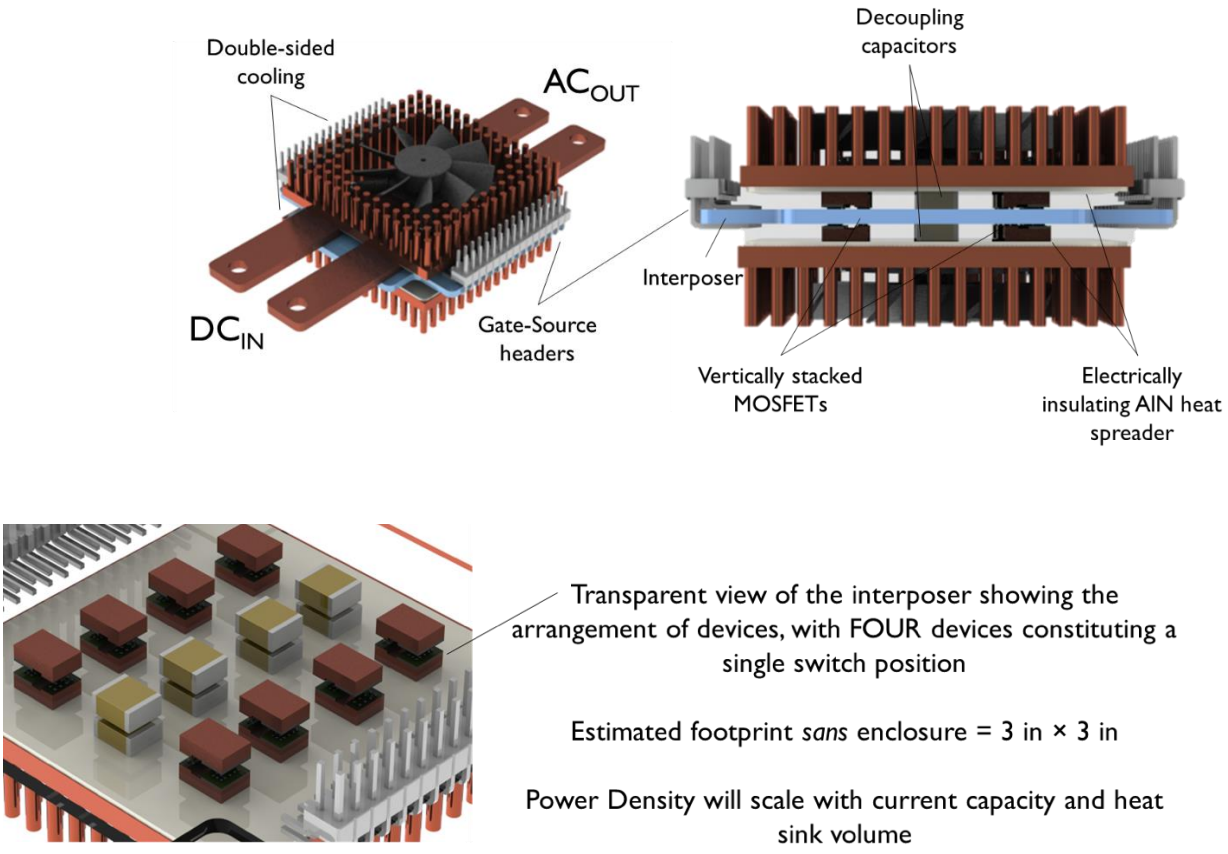


Figure 9.2: A two-tiered 16-device wire bondless SiC power module, featuring in-module decoupling capacitors and double-sided cooling.

This dissertation serves to introduce a crucial first step in the 3D wire bondless packaging of SiC modules. Using flip-chip MOSFETs will improve system power density in three fundamental ways—(1) it will enable higher switching frequencies leading to physically smaller passives, (2)

it will reduce the thermal management demand by distributing it vertically across multiple tiers, and (3) it increases the number of the power devices per unit volume. More power devices per unit volume implies a greater power output from a given volume. The result—a higher power density.

References

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