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Design, Fabrication, and Reliability Effects of Additively Manufactured First Level Compliant Interconnects for Microelectronics Application

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Design, Fabrication, and Reliability Effects of Additively Manufactured First Level Compliant Interconnects for Microelectronics Application

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by

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ABSTRACT

Semiconductor packaging and development is greatly dependent on the magnitude of interconnect and on-chip stress that ultimately limits the reliability of electronic components. Thermomechanical related strains occur because of the coefficient of thermal expansion mismatch from different conjoined materials being assembled to manufacture a device. To curb the effect of thermal expansion mismatch between conjoined parts, studies have been done in integrating compliant structures between dies, solder balls, and substrates. Initial studies have enabled the design and manufacturing of these structures using a photolithography approach which involves a high number of fabrication steps depending on the complexity of the structures and the masked approach may cause some structural alignment concerns during manufacturing. This research involves the fabrication of these structures using a different novel approach, utilizing additive manufacturing that reduces the number of fabrication steps required to obtain compliant geometries, eliminating the requirement for alignment tools, while also providing a platform for unique compliant structures. Additive manufacturing offers a solution to increasing fabrication concerns for electronics and additive manufacturing has emerged as a potential technology for improved customized and complex part fabrication. This thesis provides a review of common additive manufacturing approaches ranging from material development, process fabrication development, and applications that have been demonstrated in the electronics industry whilst also eliminating non critical process such as masking concerns, depending on geometry size. This thesis discusses two main methods of fabrication and analyzes the properties and effects of these interconnect structures on a die. Structural finite element thermal cycling simulations between -40 to 125^{o}C show about a 115% increase in the solder joint fatigue life. Additionally, fabricated test structures created directly on a PCB were experimentally characterized for compliance using a micro-indenter tester, showing a mechanical compliance

range of 265.95 to 656.78 μm/N for selected design parameters to be integrated into a test vehicle. This approach can accomplish similar thermomechanical stress alleviation to formerly reported methods, but with fewer process steps, and potential for new geometry manufacturing. Further validation of the finite element reliability has been done by integrating an in situ elevated temperature shear stress study. The compliant interconnect packaged device demonstrated enhanced electrical reliability performance when compared with the package without the interconnects.

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Firstly, I would like to express my sincere gratitude to my academic advisor, Dr. David Huitink, for his mentorship, professional advisory, knowledge, support, and motivation throughout my research and for helping me discover new skills within myself. I would like to thank Dr. Peng and Dr. Milkovjic for their additional contribution and advisory in my research. I would like to thank Mr. Errol Potter and Mrs. Kaoru Potter for their help in the usage of HiDec state of the art facility. I would also like to extend my thanks to my thesis committee member, Dr. Zhou.

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DEDICATION

I dedicate this thesis to my parents, Mr., and Mrs. Olatunji for their endless, love, support that has helped me through this phase of my career.

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1. INTRODUCTION

1.1 Background

Given the rapid development and miniaturization of already existing electronic devices and components, which causes reliability challenges for conventional organic packaging approaches due to the underlying limitation of machining and fabricating micro components sizes, it is paramount for researchers to investigate more effective methods of fabrication that can meet the industrial needs for miniaturized microelectronics fabrication. In recent times, researchers have investigated integrating additive manufacturing methods in electronics fabrication. Additive manufacturing is the layer-by-layer build-up of materials to form a part or component. This method of fabrication offers an effective way of fabricating complex design structures without the concern of machining from subtractive fabrication methods. Generally, additive manufacturing offers an easier path to fabricating microelectronics and also provides opportunities for the fabrication of unique customized designs for electronics parts and components whilst also reducing effective fabrication costs and reducing the number of process steps required to manufacture similar components in comparison to subtractive fabrication methods [1].

The overall set up, size designs, and assembly of microelectronics make it extremely difficult for conventional manufacturing approaches to be utilized in fabrication. Electronics components may consist of functional traces or interconnection structures such as compliant interconnects, conductive paths, chip substrates, etc. While conventional approaches have been enhanced through some processing techniques such as photolithography to aid in the miniaturization of the components' sizes, there are concerns with integrating multiples fabrication procedures such as difficulties in customization of designs for fabrication, increased number of process steps to

fabrication, low throughput turn out, exposure of materials to corrosive chemicals, etc. Just as predicted by Gordon Moore, the co-founder of Intel, the constant increase in the number of chips on substrates would inadvertently cause challenges in device size limitations requiring greater package integration technology approaches to aid the increasing development and power push on electronics and multi-chip integration [2].

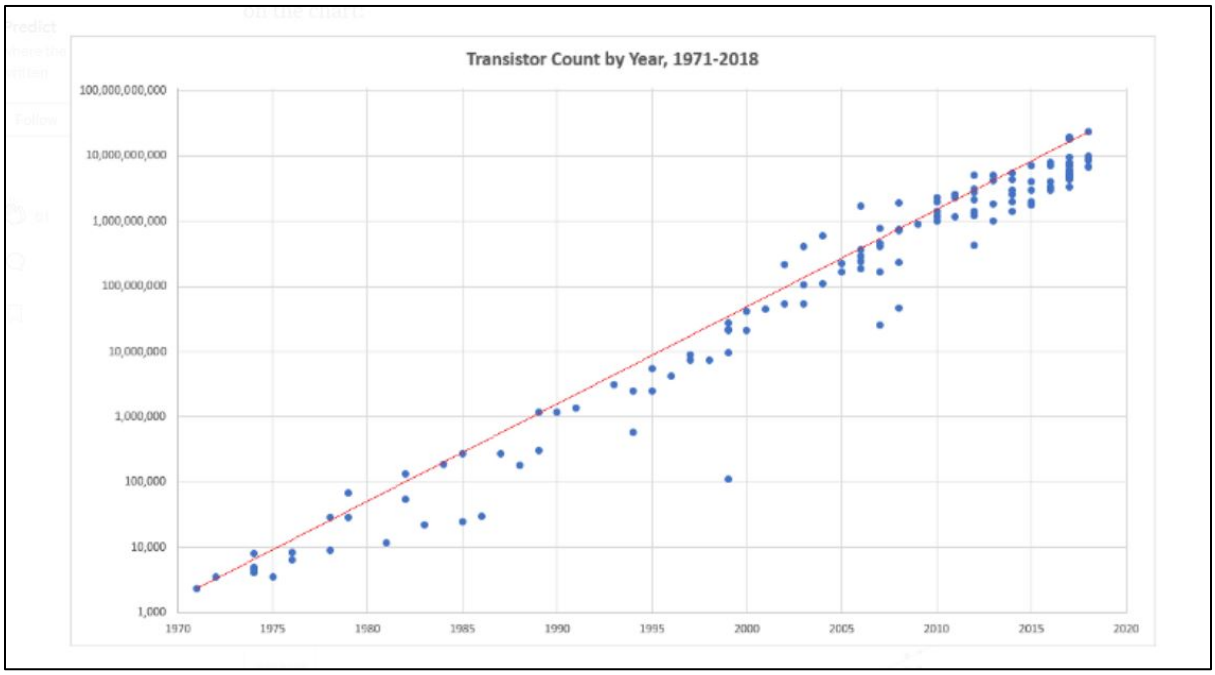


Figure 1-1 - Gordon Moore's transistor predictor chart [3]

Customization and complex geometry creation are made possible through additive manufacturing causing a paradigm shift in research and investigation of alternate complex geometry manufacturing methods, different from conventional subtractive manufacturing processes. Additive manufacturing provides numerous advantages such as aiding the fabrication of embedded functional elements during the step by step building of components enabling the integration of conductive circuit paths for electronics applications [4]. Salaoru et al. illustrate some of the advantages of additive manufacturing in the ease of design customization, low cost of production, etc. [5]. Additive manufacturing approaches have even been leveraged in the non-

electronics industry such as in the fabrication of human tissues and organs highlighting its vast industrial applications [6], [7], etc.

With the need for advanced integration methods and growing markets in customizable electronics, additive manufacturing offers a great opportunity in microelectronic packaging integration methods.

Electronic packages typically comprise multiple components that are mechanically assembled to form a singular working device and these assemblies are optimized for best mechanical and thermal performances. Electronic packages are constantly being improved for advanced performances and the increased performance expected from these devices is dependent on the reliability capabilities in geometrical designs, structural enhancement, and architectural and interconnect placements. Semiconductors are intricate components to most electronic devices and their reliability is paramount to the overall reliabilities of most power electronics. One of the major points of failure in a semiconductor device during device or system assembly and working conditions is at the interconnect level. Mechanical stresses that occur at these regions are caused by differential thermal contraction between dies, solder balls, and substrate for flip-chip devices [8]. There are many other ways of assembly a chip on a substrate such as a tape automated bonding and conventionally through wire bonds. Wire bonds have many demerits in optimizing the design space, mechanical and geometrical concerns, and even electrical disadvantages such as inherent crosstalk via parasitic inductances. Wire bonds pose concerns with thermal expansion mismatch between the substrate and the die, but most importantly the architectural design provides poorer thermal management control and consequently affects the reliability of these electronic packages as in a wire bond assembly, the heat generated region faces the die and thus prevents and/or reduces convective air cooling.

Experiments were done by Engl et al.,[9] comparing the effects of wire bonds and the flip-chip interconnect method validates the benefits and gives a better understanding of the industrial paradigm shift to the flip-chip method of assembly. They showed that with wire bonds, and increased power loss is expected, an increase in parasitic effects such as inductance is also observed when compared with solder balls-based assembly.

1.2 Research Objectives

Integration of high powered semi-conducting materials such as silicon carbide can push the working temperature of modules as high as 500 ºC [10]. Beyond the general obvious reason to shift from wire bond based assembly due to its mechanical unreliability, poor thermal conductivity, and architectural design causing a large footprint, but also electrically, wire bonds negatively impact the electrical performance of integrated circuits through parasitic self-inductances.

The numerous demerits of wire bonds have encouraged the integration of the flip-chip method as a first-level interconnect for die to substrate packaging that provides improved mechanical and electrical performance such as ball-grid arrays (BGAs).

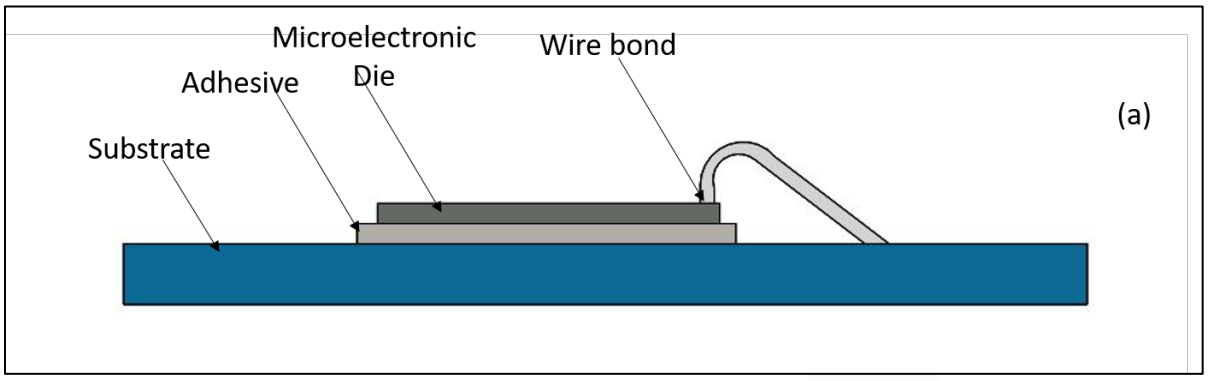


Figure 1-2: Wire bond assembled package [11], [12]

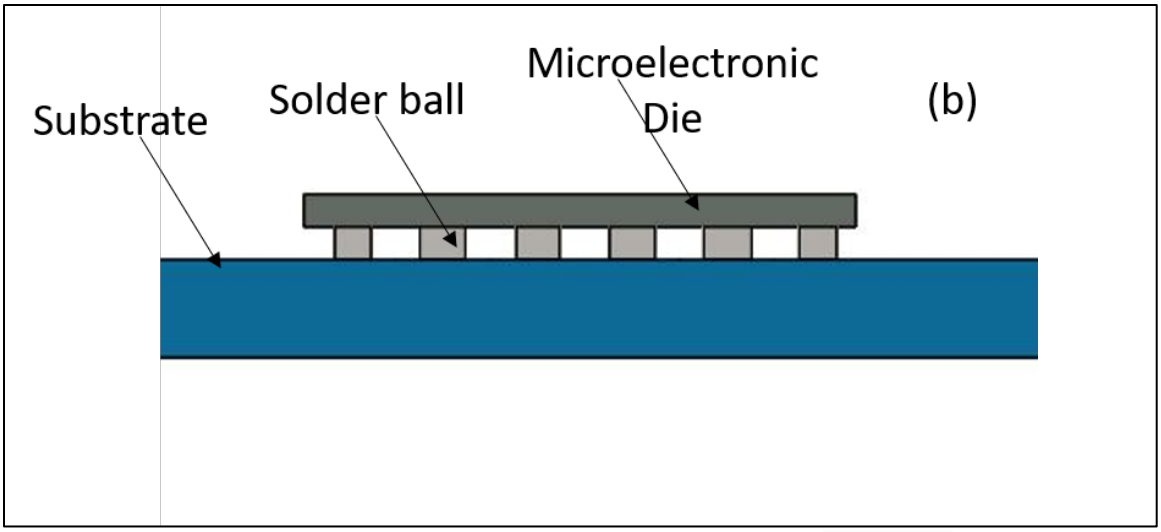


Figure 1-3: flip chip bonded assembled package [11], [12]

The working temperature of high-powered integrated circuits poses a great area of concern in the mechanical reliability of the conjoined parts due to the assembly and packaging of different materials with dissimilar coefficients of thermal expansion even with the flip-chip assembly method.

To improve the overall fatigue life of power integrated devices, this research focuses on developing a novel process to enable the fabrication of mechanical compliant electrical interconnect for power module assembly and to also improve solder ball thermomechanical reliability. Typically, electronic interconnect packaging can be subdivided into three (3) categories:

i. First level interconnect used to package an integrated circuit die to a substrate
ii. Second level interconnects used to package multiple integrated circuits die/chip to a systems board.
iii. Third-level interconnect is used to package multiple systems to a unified board creating a larger system.

These interconnects perform the following functions in a power device mechanical robustness through the underfill materials and solder balls, electrical conductivity for signal, and electrical connection, and they can even help in thermal conduction of heat away from the system.

This thesis also analyzes the certain properties of the manufactured device through mechanical, electrical, and reliability computational characterizations. Further experimental studies and tests are done to validate simulated results.

Some other objectives this research sought to improve includes:

- A cost-effective method of fabricating multiple compliant interconnect devices across the board by using readily available materials.
- Develop an easy to understand and use repeatable process for assembling power devices on these structures.
- Improve throughput for manufacturing of these structures by encouraging a wafer method of fabrication that can be diced afterward.

1.3 – Organization of Thesis

This thesis includes five chapters, and the content of each chapter is briefly described below.

Chapter 2: This chapter presents a comprehensive review of the existing literature of additive manufacturing applied in microelectronics fabrication. Here common additive manufacturing methods are highlighted and some examples of additive manufacturing applications into manufacturing components of electronics. Further review of structural enhancement techniques that have been integrated into chip substrate interconnects for mitigating stresses.

Chapter 3: The novel additive manufacturing approach of manufacturing this micro-compliant structure is presented, details in material selection and characterization are also highlighted including electroplating requirements for current and voltage. Further discussion includes

possible structural refinement of the structure and assembly methods of the dies on the compliant interconnect structure

Chapter 4: A complete step by step method of accurately modeling these structures for mechanical and reliability characterization is discussed with a process flow chart while also highlighting some of the boundary conditions that were applied to properly model operating conditions for testing and experiments

Chapter 5: Here the experimental characterization and validation process and challenges are accurately discussed. Validation and comparative study between experimental data and computational data are also presented generating an informed conclusion from both approaches. The sample is tested on a dummy MOSFET test vehicle and the experimental result is discussed.

Chapter 6: The final chapter discusses the main research findings gotten from this research thesis, highlighting the impact on microelectronics and presents areas for further studies.

2. LITERATURE REVIEW

2.1 Additive Manufacturing in Electronics

The concept of additive manufacturing is highly dependent on conjoining the matrix elements of the primary material of fabrication. Typically, the parent material is melted and fed to start the fabrication process usually at a specific feed or flow rate [13]. Many methods and printing technologies aid the fabrication of electronics components and some of the commonly used fabrication process steps for melting parent matrix materials ranging from electron beam melting, laser metal deposition, laser beam melting, and the use of a conventional heating block. However, more efficient ways to aid layer by layer fabrication should be explored and exploration of various fabrication approaches depends on the component application, some of the properties per application to be considered may consist of surface roughness concerns, size of embedded features in components, the strength of the component, and porosity effects [14]. Many additive fabrication methods exist that aid little or no change in material chemistry such as fused deposition modeling technology, inkjet printing, direct metal, and stereolithography-based printing like stereolithography apparatus, (SLA) and selective laser sintering (SLS) [5]. Additive based manufacturing technology is a step-based deposition of material to form a proposed designed structure. Here, some of the common methods of additive manufacturing incorporated for electronics application and fabrication is highlighted.

For example, inkjet printing technology is a common AM fabrication approach and offers a straightforward fabrication path for conductive paths in electronics by depositing ink droplets onto a substrate where the print head provides the driving force (thermal or piezoelectric) for accurate reliable material deposition see figure 2-1. This printing procedure can also be described as the powder bed printing method [15].

Numerous factors can affect the adoption of a printing method or selection and application of material for electronics. These factors may include but are not limited to the printability of material, extrusion pressure/temperature, dependent on the driving force, the diameter of the extruder nozzle, the viscosity of the material, the properties of the material [16]-[18]. One of the major drawbacks with using the inkjet printing technique is the limitation of the viscosity of the material that can be integrated into this additive manufacturing method, usually in the range of 20 – 40 MPa-s [19], [20]

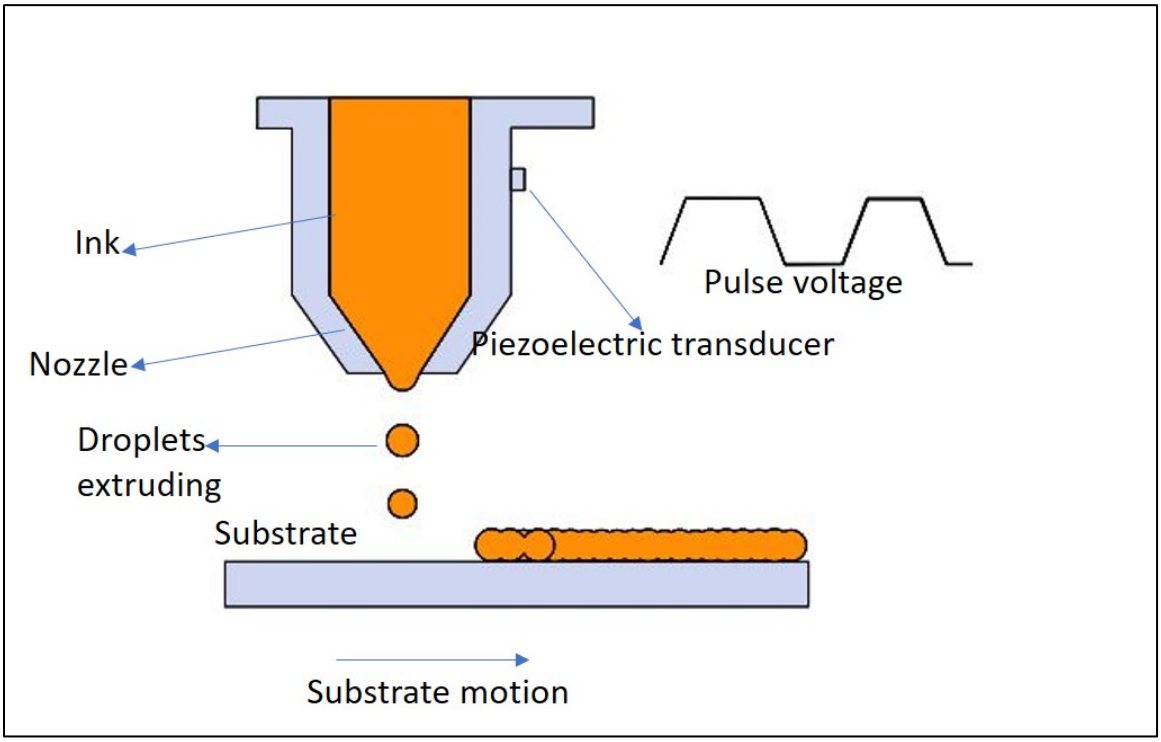


Figure 2-1: Inkjet printing and deposition technique on a substrate

Another common AM printing technique is aerosol jet printing which mode of operation that involves changing the material from liquid to vapor based on extrusion using a high – velocity nozzle. This printing technique provides a great advantage in reducing the cure time of the dispensed material during printing because the printing material is partially dried during phase change from liquid to vapor before the deposition is illustrated in figure 2-2.

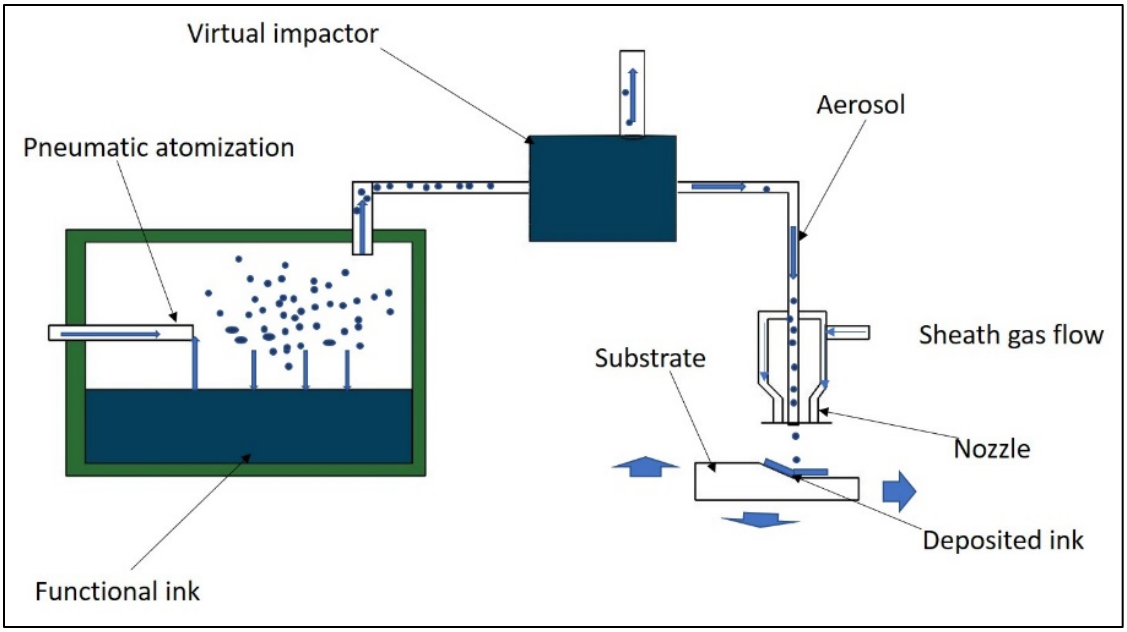


Figure 2-2: Aerosol printing and deposition technique adopted from [21]

There exist other types of 3D printing AM techniques such as stereolithography based printing method, fused deposition printing method, an extrusion-based 3D printing like syringes and pneumatic micro dispensing pump.

The stereolithography method utilizes the use of ultraviolet light to cure resins and metal powders in a systematic sequential arrangement to fabricate components and can be subdivided into Selective Laser Melting and Selective Laser Sintering. Stereolithography enables rapid prototyping and expedited testing of designs [22] and Maalderink et al. highlights various examples of integrating stereolithography-based 3D printing methods [23].

The fused deposition model or fused filament fabrication printing technology commonly abbreviated as FDM is another different and common type of additive based technique. This method does not integrate the use of curing ultraviolet light in its fabrication approach, but a gradual deposition of thermally induced thermoplastic material commonly called “filament” through an extruding nozzle. This gradual deposition is enabled by electric motors for multi-directional motions. This thesis research is based on the process development of compliant

structure mainly through FDM methods and provides a potential area of process enhancement and feature size refinement through stereolithography based methods.

Additive manufacturing is an emerging area of technology and numerous new research is currently ongoing to enable electronics industrial applications. Some of the benefits provided by additive manufacturing include:

i. Opportunities for 3D manufacturing of complex designs
ii. Opportunity for microstructural manufacturing
iii. Opportunity for cost and time effective methods of manufacturing by fabricating and prototyping high yield productions
iv. Opportunity and avenue for manufacturing light-weighted parts, particularly helpful in the Aerospace and Automotive industry

Table 2-1 below highlights some common additive manufacturing techniques, their working principle, and electronic fabrication applications. This table will provide references for applications that can be integrated into other electronics fabrication and give an insight into printing machine suppliers.

Table 2-1: 3D printing techniques and application in electronics fabrication

Common Additive manufacturing Technique	Printing resolution (µm)	Working principle	Examples of fabricated electronic components	Major supplier/ Manufacturer	Reference
Inkjet	≥20	Ink deposition based on a printing bed	Inkjet printing of high-performance transistors	Oasis 3DP	[24], [25]
Aerosol Jet	≥10	Atomization and vapor deposition on the target substrate	Aerosol jet printing of phased array antenna	Optomec	[24], [26]
Fused deposition model	50 -200	Forced filament extrusion via material melting	3D printing of electrical circuit on a substrate	Maker gear, Prusa, Ultimaker	[27], [28]
Stereolithography (SLA)	0.25 - 10	Ultraviolet light curing of liquid resins (thermoset plastics)	Embedded conductive wires and electronic components	Formlabs, Prusa	[29], [30]
Selective laser melting (SLM)	22	Ultraviolet laser-based curing of metallic powder	Direct metal laser sintered Flat finned heat sinks for electronics	SLM Solutions group	[31]-[33]
Selective laser sintering (SLS)	20 - 150	Ultraviolet laser-based curing of thermoplastic, glass, and ceramics	Laser sintered Ag lines for flexible electronics	3D systems	[34], [35]
Binder jetting	35	Liquid binds selected powder particles together	Fabrication of dielectric radio frequency filters and ferroelectric dielectric capacitors	Hewlett-Packard, Digital Metal	[36], [37]

Electronics comprises conjoined material parts to make a device and the components of the devices may range from different classes of electrical materials such as conductors to aid electrical and signal connection, insulators to act as a dielectric of the device, and semiconductors commonly used in the fabrication of integrated circuits. The flexibility offered by additive manufacturing in the fabricating of co-manufactured materials provides a unique ability to simultaneously create electronic interconnects and structural elements comprising of insulators, conductors, and semiconductors.

2.2 Electronics Packaging for Power Module Devices

Power device technologies include Silicon (Si), Silicon Carbide (SiC), Gallium Nitride (GaN) based transistors and they can be used to fabricate power Metal Oxide Semiconductor field-effect transistor (MOSFET) or Insulated Gate Bipolar transistor (IGBT) which are typically assembled and packaged on a substrate. Over the years, many requirements have influenced the research into the packaging of power modules, architectural assembly methods, and assembly materials.

Some of the concerns with module assembly and packaging are parasitic concerns and device reliability. Early methods of assembly power modules involved the use of wire bonds, which are the main causes of parasitic concerns, and they also cause poor thermal management schemes which inadvertently affect the overall reliability of devices particularly because of their architectural designs [10].

The main areas of focus for electrical and reliability improvements research can range between (1) improving cooling methods to curb extreme thermal conditions that pose structural and material property concerns especially at the interconnection points of the assembly and (2) implementing improved thermomechanical designs that can aid package withstanding extreme

stress conditions. This thesis focuses on the latter method of curbing these concerns albeit a manufacturing process is required to manufacture micro complex designs that can effectively meet the reliability requirements.

Development from wire bond methods of package and assembly for power modules have been improved by integrating flip chip technologies into power modules by Seal et al [10].

The flip-chip assembly method provides a great opportunity for enhancing electronics devices' capabilities but there are existing limits to power densification, improving switching frequency, etc. and this is hugely dependent on thermal management technologies. However, the architectural arrangement of components, material selection, and enhancement, structural designs, and integration are all important areas under emerging technologies curbing the effect of increased thermal energy generation and these areas of study are just as important as active and passive cooling and thermal management technologies and research.

One of the main areas of focus in flip-chip fatigue life is the solder joint fatigue that occurs primarily due to solder ball cracking [38] and other secondary reasons such as intermetallic area growth [39] etc. To improve the mechanical strength of solder balls and further curb the rate of cracking of solder balls, researchers have developed several solder balls enhancing technologies and features typically to improve mechanical strain compliance in the device ranging from polymer cored balls [40], compliant interconnect, etc. where polymer cored balls are polymers coated in solders and compliant structures are structures that accommodate volumetric expansion effects and warpages in the device.

Many first-level compliant structures and designs have been developed in the last decade highlighting the potentials of this technology.

2.3 Examples of Mechanical Enhanced Compliant Structure

i. Spring Based Interconnects

These are interconnects that particularly to reduce the impact of thermomechanical based interfacial stresses between assemblies by designing and developing microstructures with spring-like properties i: e properties that can deflect under mechanical induced load with some mechanical stiffness. Many structures have these properties like a micro spring, cantilever beams, etc.

For example, Sitaraman et al., [41] developed the J spring shaped compliant interconnects using the photolithography and selective etching approach of fabrication in the cleanroom and other interconnect designs such as flex connect, arc-fan interconnects [42], smart three-axis compliant interconnect [43], β-Helix interconnect [44], etc. Compliant interconnect studies have shown solder fatigue life reliability improvements exemplified in [45] and [46] etc.

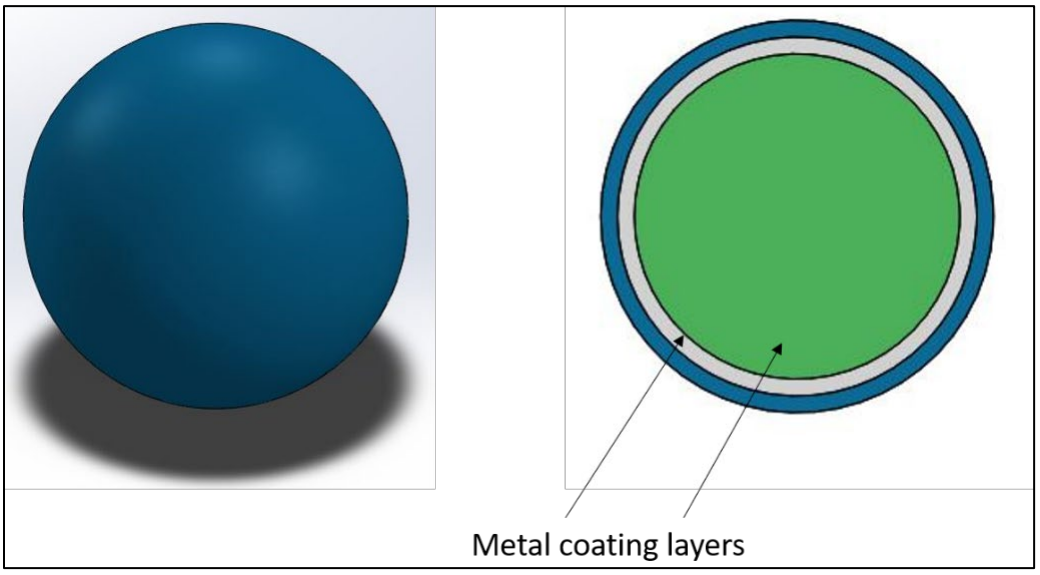


Figure 2-3: Metalized polymer spheres [47]

ii. Copper Bumps

Copper bumps as the name implies, made of copper, making it a perfect material for integration between semi-conductors and substrates because of their closely aligned coefficient of thermal expansion, 16.7 ppm/^{0}C for Copper and 14 – 17 ppm/^{0}C for printed circuit boards and its great mechanical and thermal properties.

Micro copper pillars represent some of the early research done on the power device's reliability enhancement. These interconnects decouple the substrate from the die and are developed as a slender structure. The design of these structures is based on mechanical strength due to their bulking property without any form of mechanical compliance. The method of assembly for copper pillars and bumps is the metal post solder chip connection (MPS-C2) [48].

Many inventions have been generated from this technology like Intel [49], IBM [50], Powertech technology inc. [48], etc.

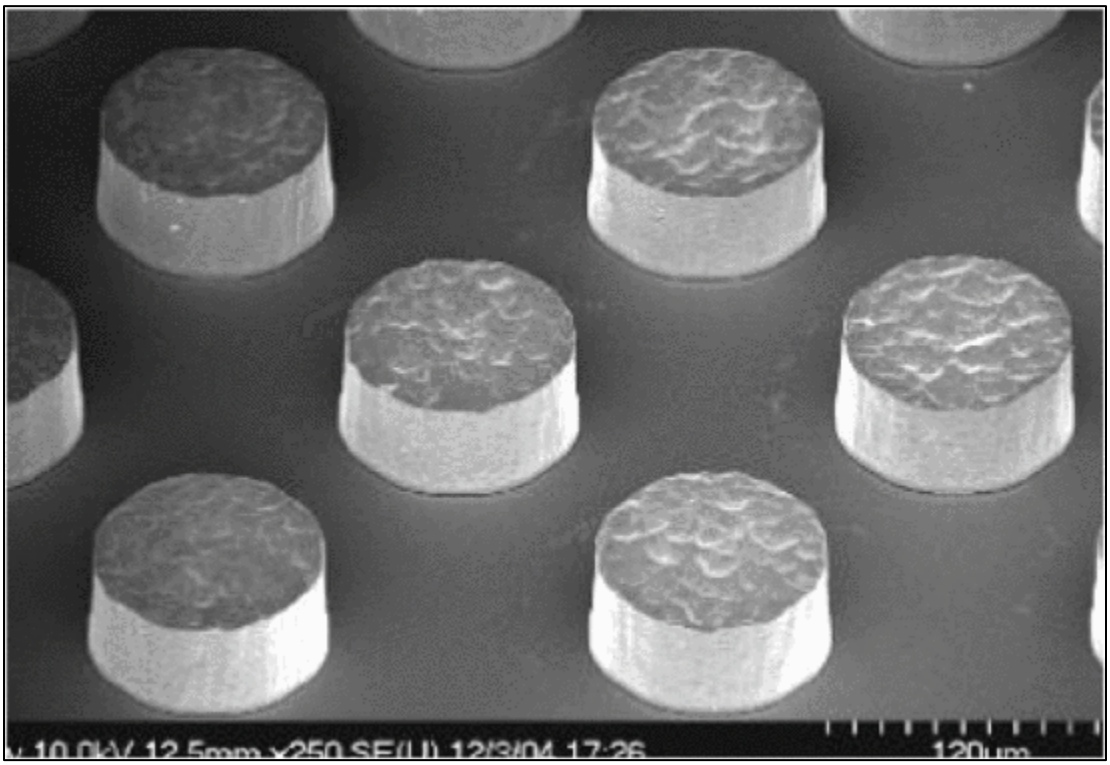


Figure 2-4: SEM images of copper bumps [51]

iii. Other Interconnects

Similarly, to copper bumps, there exists other interconnect bumps from other materials like carbon nanotube-based interconnects [52], copper nanowire bumps [53]. These other designs are a better alternative to compliance for copper bumps due to their design having a higher aspect ratio but they are inferior to copper bumps electrically due to their length, causing a higher self and mutual inductance in comparison to conventional copper bumps.

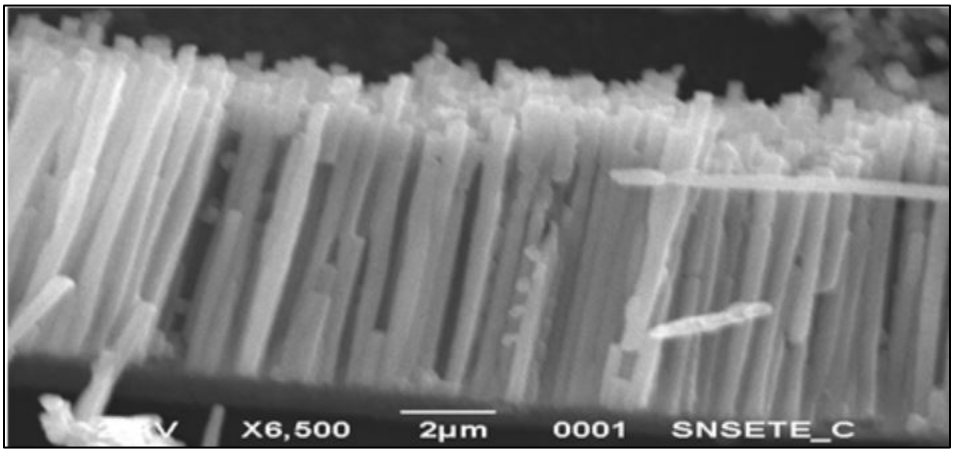


Figure 2-5: SEM images of copper nanowires [53]

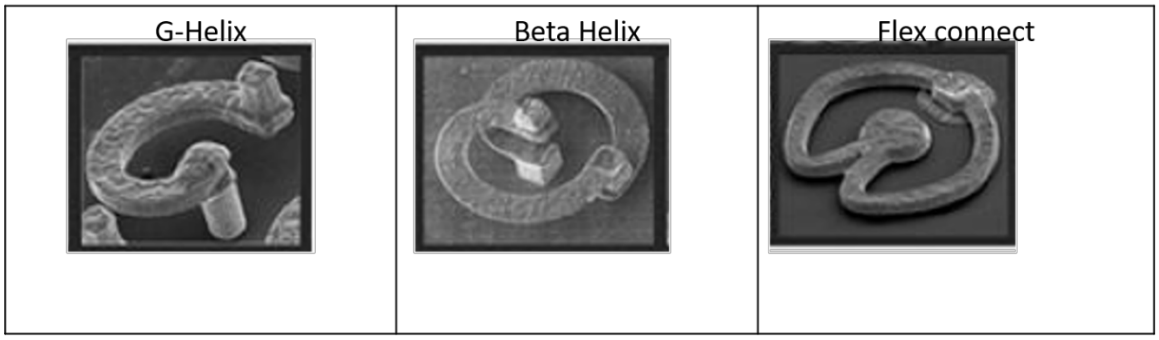


Figure 2-6: SEM images of different compliant interconnect geometries G-Helix [54], Beta Helix [55], Flex connect [56]

Various compliant interconnect structures have been pursued in academia and industry and compliant interconnects researches have demonstrated mainly semi subtractive and subtractive approaches for fabrication which may greatly limit industrial application, due to limitation in

complex compliant structures for improved reliability, manufacturing throughput, and adhesive stress regions, etc.

This work presents a novel additive fabrication approach directly on a printed circuit board and illustrates its mechanical properties and power module integration benefits, whilst also effectively improving device throughput and enabling complex structural fabrication. Complaint interconnects proposes a solution that reduces strain on solder joints but has its potential and advantages have not been fully harnessed due to current fabrication approaches, and throughput. This modal approach imitates casting [57] where the mold is removed after the development of the structures and components.

2.4 Working Principle of Compliant Interconnects

Interconnects significance in an electronic device includes electrical performance and not just the mechanical and thermal benefits. The major cause of device failures in electronic devices is at the interconnects and components joints caused by the mismatch in the coefficient of thermal expansion. The coefficient of thermal expansion of printed circuit board (PCB) substrates is 17 ppm/°C which is very close with the CTE of copper, 17 ppm/°C. Therefore, copper is used in the design because it has a closer coefficient of thermal expansion to printed circuit boards (PCBs). Compliant interconnects are generally designed to reduce the risk of failure of solder balls either by introducing a composite like metalized polymer spheres or designing a mechanical structure to improve support and create an allowance for thermomechanical expansion, shock, and vibrations. In theory, during the interfacial expansion of package components joined by solder balls, there is a limited area available for the deformation allowed in the volume of solder ball leading to creeping and fatigue behaviors. This expansion of the different adjoined materials induces different stresses on the whole package due to different rates of expansion causing the

package to warp and solder joint fracture or failure in the long term. The thermomechanical effect of coefficient of thermal expansion mismatch occurs during extreme temperature conditions i: e extremely hot temperatures and extremely low temperatures, ΔT, the effect of these values is dependent on the process temperature of the die attach during assembly typically the reflow temperature. Compliant interconnect designs curb the early failure susceptibility due to its thin cantilever design enabling the differential package expansion with lower stresses induced in the solder interconnects. This is evident as simulations (on Ansys®) show a lower maximum value of von mises stress in the overall device package for select designs. For the effective application of these components, some design conditions may be considered. Just as solder ball heights vary linearly across a die due to assembly conditions (warpage of the die during processing) and stress distribution reasons, we may adopt the same conditions during assembly of the interconnects. Interconnects can be designed on a board attachment to accommodate more stress at certain levels i:e interconnects close to the mid-region of a die can be designed to have low compliance while interconnects closer to the edges can be designed to have higher compliance [58] because the maximum shear and peeling stresses occur at the edges of a die [59]

3. DESIGN FABRICATION APPROACH, AND METHODOLOGY

Many efforts have been put into researching geometries and designs that can effectively meet the reliability challenges demands and 3D printing and additive manufacturing limitations. There are various design approaches such as 3-arc-fan compliant interconnect, micro j-springs, helix compliant, etc. [41], [60], [61].

The design chosen is a cantilever beam shaped compliant structure additively manufactured directly on a printed circuit board (PCB) for fabrication and testing. This structure is chosen to enable proof of concept and the ability to integrate the novel additive based fabrication approach. The accuracy of fused deposition model-based printers requires the integration of a design to provide compliance whilst also working within the constraint of size. The cantilever beams are designed according to various variables which may or may not involve curved shaped cantilever beams. The study in this research has integrated the use of curly shaped beams to utilize their effect of better compliance whilst also optimizing the design space ranging from 90 to 330 degrees to enhance mechanical deflection and improve compliance. The selection of a particular geometry and shape of these interconnects depends on the interconnect's application and die's dimension. The beam's mechanical stiffness is characterized and compared with other literature designs for compliance applications.[62]

3.1 Design Variables

The interconnects are designed as a cantilever beam comprising of a copper post and a beam. The post will be manufactured and connected on a substrate and the top of the beams will be bonded to the die through soldering. The figure below, figure 3-1 shows variations in the design of these interconnects. The interconnects final design is dependent on the following variables: copper beam width, copper pad dimensions, copper beam thickness, copper post diameter,

copper post height and subtended angle all determine the overall surface area and footprint of each singular interconnects.

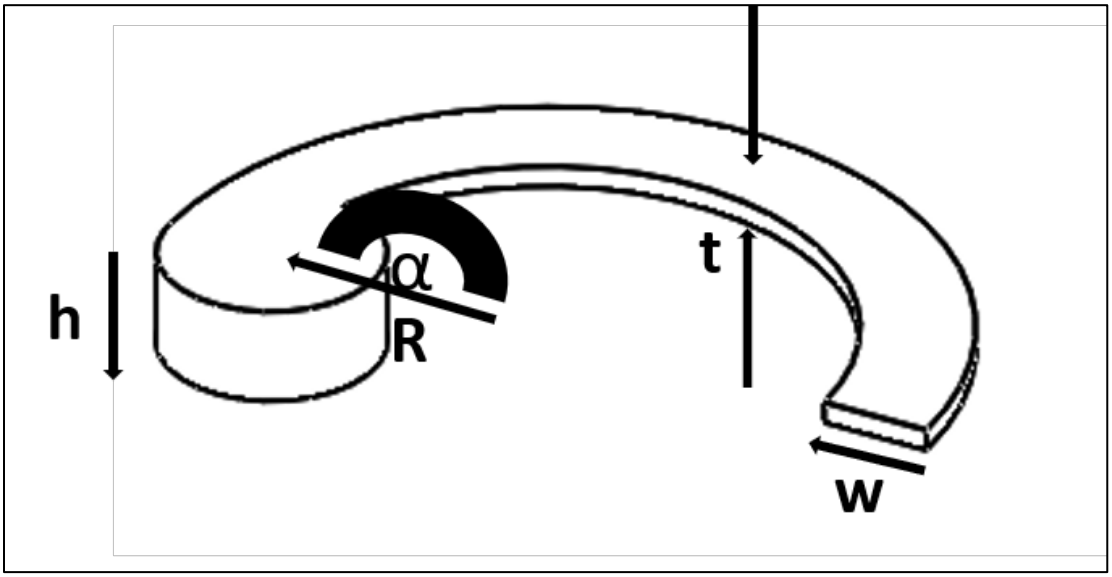


Figure 3-1: Additively manufactured interconnect model

3.1.2 Copper Post Variables

The copper post variables directly affect the standoff or decoupling height between the die and substrate and affect the extent of deflection i: e out of plane compliance.

The effect of size and proximity of electrical interconnections in an electronic assembly on electronics parasitics encourages influences design conditions such as small copper posts, in both diameter and standoff height but due to current limitation of fused deposition model printing techniques inhibiting effective minimizing of these variables as very thin mold prints where the application of electrodeposition manufacturing technique is prevented due to porous prints for thin molds visible in figure 3-2. Also, FDM prints have limited printability of small hole sizes typically 0.5mm radius when using the 0.4 mm nozzle.

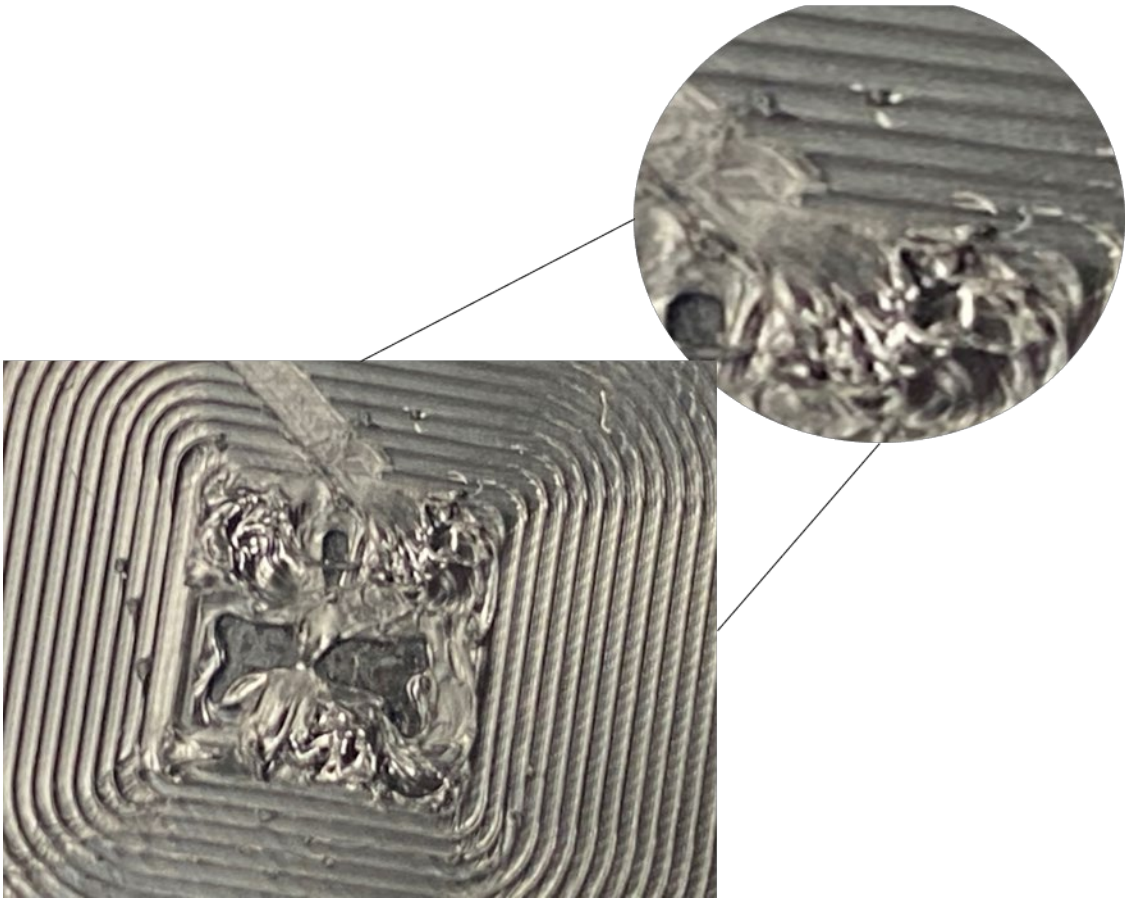


Figure 3-2: Image of a porous plot for thin molds

3.2 - Method of Fabrication

A new fabrication approach/ method which can reduce the cost of production of interconnects, reduce the number of steps and chemical processing required and effectively improve throughput is presented in this work.

Previous methods of fabricating compliant interconnects include the application of liquid photoresists and dry film photoresists which are essentially thin films. These thin films would require more than one in the fabrication of a microstructure consequently causing the addition of processing steps in the fabrication especially in the development of these films and concerns of film alignment, through UV light exposure and chemical development. Also, the application of dry films may not be very reliable as the films may undergo tear when being applied to the

substrate board. Beyond the concerns of dry films, a liquid photoresist even poses more concerns as the application substrate must undergo heat treatment before use, such as a soft bake for curing of the photoresist and a hard bake is done after development to enhance the physical and chemical stability of the photoresist. These additional process for liquid photoresist poses a risk of failure to the substrate such as cracking of the photoresist, thus, reducing the application of the resist. Also, the above-mentioned fabrication reduces the use of cleanroom facilities and makes it easier to fabricate in almost any makeshift lab with little or no use or exposure to any chemical processing techniques.

The use of additive manufacturing in the fabrication of compliant interconnects for electronic devices is demonstrated by using a 3D printed mold as a support fabrication and sacrificial material designed and developed to be removed after fabrication.

3.2.1 3D Printing Technique Selection

There are numerous printing techniques, and they all have their merits and demerits. In general, the stereolithography method of printing provides more accurate and precise microprint when compared to the fused deposition model printing techniques. However, the SLA based printing technique is considerably inferior in material selection because most of the SLA based materials do not offer a material removable method either through melting or solvent solution. Even more so, materials that do offer opportunities for etching require melting at very high temperatures > 200 C for some select materials which is not an ideal processing environment for FR4 printed circuit boards with ideal operating temperature -50 -110 C. Extensive study done on 3D printing materials and mode of printing enabled a decisive conclusion on using FDM based techniques due to the material etching requirement.

3.2.2 Material Selection

Establishing a 3D printing technique requires a material study on probable integrating materials to enable proof of concept and application. Many materials have been characterized and compared for application to the fabrication methodology across the two major 3D printing techniques and select material properties are highlighted in table 3-1.

Table 3-1: Comparison of common 3D printing materials

Material / **Properties**	Castable wax	Dental Resin	BVOH	PLA	ABS
Melting Temperature ^{o} C	46 - 68	41 - 48	200 - 230	185 – 205	220 - 250
Process Reversibility	Irreversible	Irreversible	Reversible	Reversible	Reversible
Solvent	None	None	Water	Sodium Hydroxide	Acetone
Copper Sulphate Reaction	No Reaction	No Reaction	Absorb solution	No Reaction	No Reaction
Print Method	SLA	SLA	FDM	FDM	FDM
Filament Cost	$$$	$$$	$$	$	$

After careful material study and characterization for this process development, few materials meet the process requirement and application development to manufacturing these interconnects, a water-soluble based material (BVOH) and an acetone soluble material (ABS).

These materials would enable the printing of a negative imaged print of the desired structures. A negative print or structure are structures that enable the development of a structure by providing an open path within itself for material deposition. The selected materials will aid the layer deposition of our select material to form the desired negative shape. Through the mold, copper will be deposited via electrodeposition/ electroplating and will be formed through the exposed negative mold. This method of gradually depositing copper is reliable because the properties of the deposited copper are consistent with the ideal properties of copper. Common problems faced in other metal additive approach includes porous deposition and poor density of the fabricated structures highlighting further this technique encourages better deposition through reduced porosity which can affect their material property.

Also, this technique is relatively cheaper because the whole process occurs within room temperature compared to other additive manufacturing techniques that have high manufacturing temperatures causing probable damage to a printed circuit board. In this approach, to arrive at a highly resolved and cost-feasible approach, the integration of two main technologies is observed, fused deposition model 3D printing and chemical electroplating.

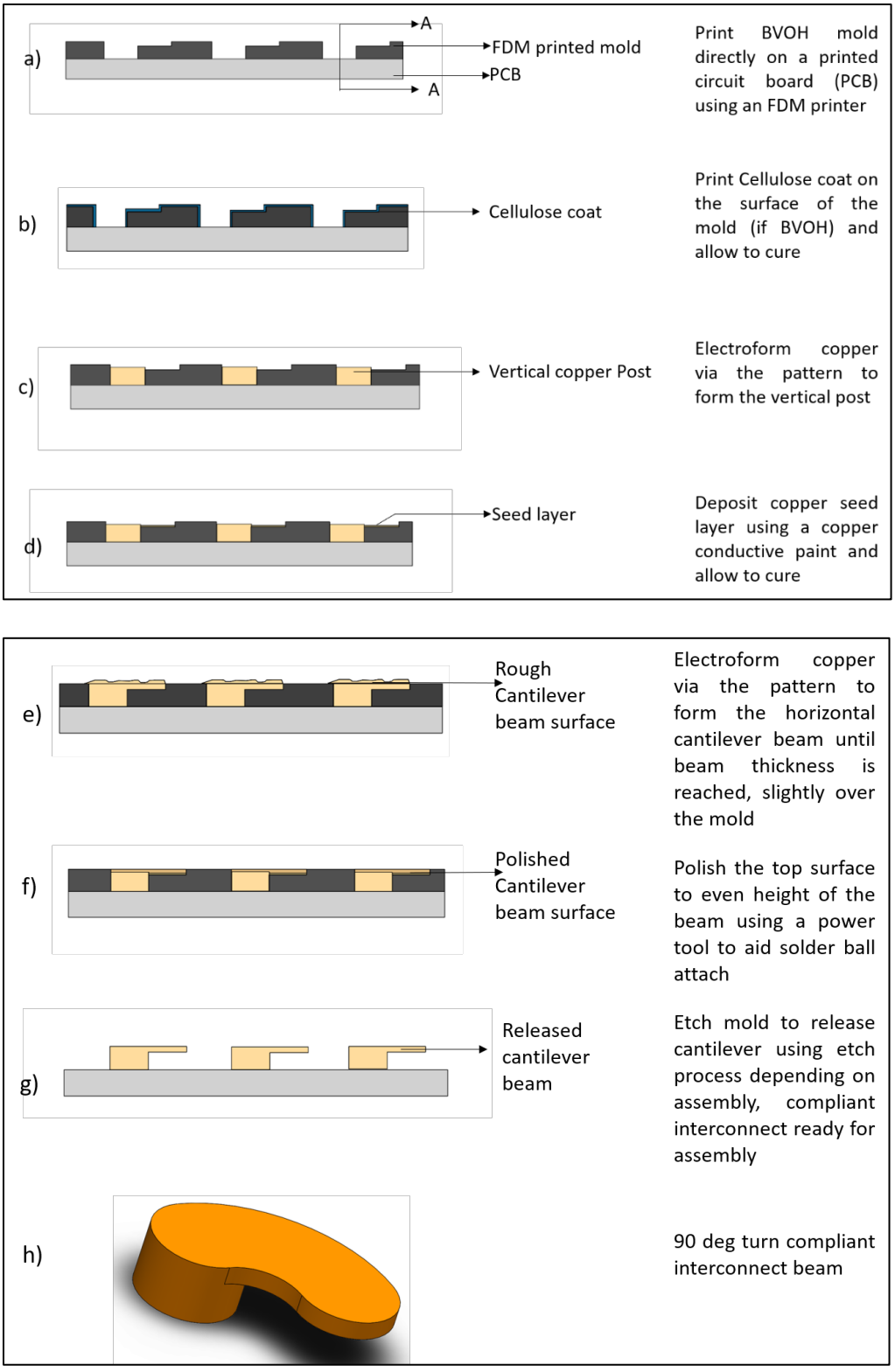


Figure 3-3: Process flow for additive manufacturing of compliant interconnects

3.2.3 – ABS Method of Fabrication Overview

The mold is printed with Acrylonitrile Butadiene Styrene (ABS) using a Prusa MK I3 fused deposition model printer at the normal printing requirements for ABS, 90ºC build plate, bed temperature, and 240ºC hot end/nozzle end temperature. To get better print quality and accuracy, the printer speed is reduced to 30mm/s and a 400µm diameter nozzle is installed.

a. The structures are designed in a negative mold using a solid modeling tool and the sliced .stl file is 3D printed directly on a printed circuit board. A negative image/mold of a structure is an inversed structure that aids the development of the proposed structure by filling the cavity in the negative mold, after which the mold is removed, identical to investment casting. The printer's offset z-height has been calibrated to accommodate the PCB.

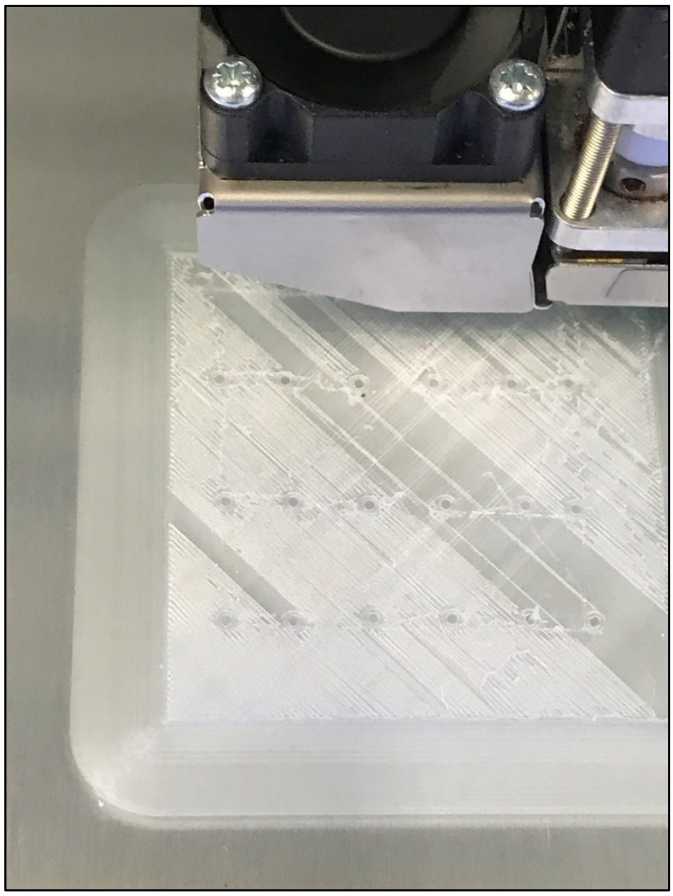


Figure 3-4: Pictorial image of 3D FDM printer printing on a PCB

b. The electroplating setup is prepared comprising of a Copper sulfate solution in a (500ml) glass beaker. A copper bar (155mm x 24mm x 1mm) is connected as the anode while the sample preparation from step a is connected as the cathode. A 30V tetronix PS821 DC power supply is used to provide a current of 0.01 ampere and 0.2 volts to the setup and the vertical copper bump is electrodeposited until initial post height is attained to enable electrical continuity for the horizontal beam. The electrical parameters are decided with the following equation below.

Following the rule of thumb of electroplating with optimum electroplating current at 0.2Amps/inch^2 translated to 0.00031 Amps/mm^2.

The current is determined by measuring the exposed surface area from the negative molds.

$$nA * 0.00031 = I_m$$

$$A = \pi r^2$$

Where n is the number of exposed regions for the copper post

A is the surface area of one exposed pad

r is the radius of the exposed area

I_m is the current recommended for electroplating the sample

Equation 3-1: Current calculating equations for electroplating

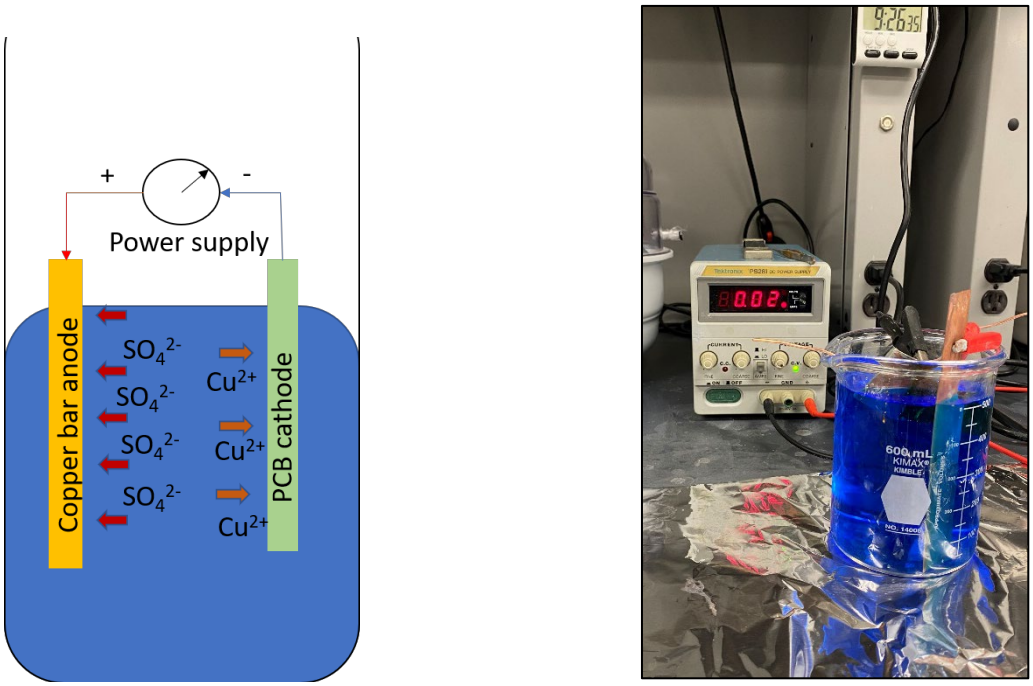


Figure 3-5: Electrical electrodeposition set up

c. The electrodeposition process is divided into two steps. The first step, b takes advantage of copper on the top surface of the PCB using that as step 1's seed layer. The second step involves the fabrication of the beam. To aid the electrodeposition of copper on the printed mold, the electrodeposition is stopped, and a Caswell-plating copper conductive paint is applied as the copper seed layer using a 200µm laser cut stencil and allowed to dry for 60 minutes to aid electrical continuity between the copper post to the mold.

Figure 3-6: Electrodeposited copper post

a

b

Figure 3-7: (a) stencil image after the printing of horizontal seed copper layer (b) Image of applied conductive paint

The electrodeposition process is restarted, and the horizontal beam is electrodeposited although at a much slower rate to the deposition of the copper post to help reduce the surface roughness of the pads

f. After the process and sample refinement, the mold is removed by placing the sample in a bath of Acetone as ABS is soluble in Acetone. After the complete dissolving of the ABS material, the free-standing interconnect can be seen and ready for assembly.

a

b

Figure 3-8: (a) Image of fabricated compliant interconnects within the mold (b) Image of compliant interconnects after mold removal

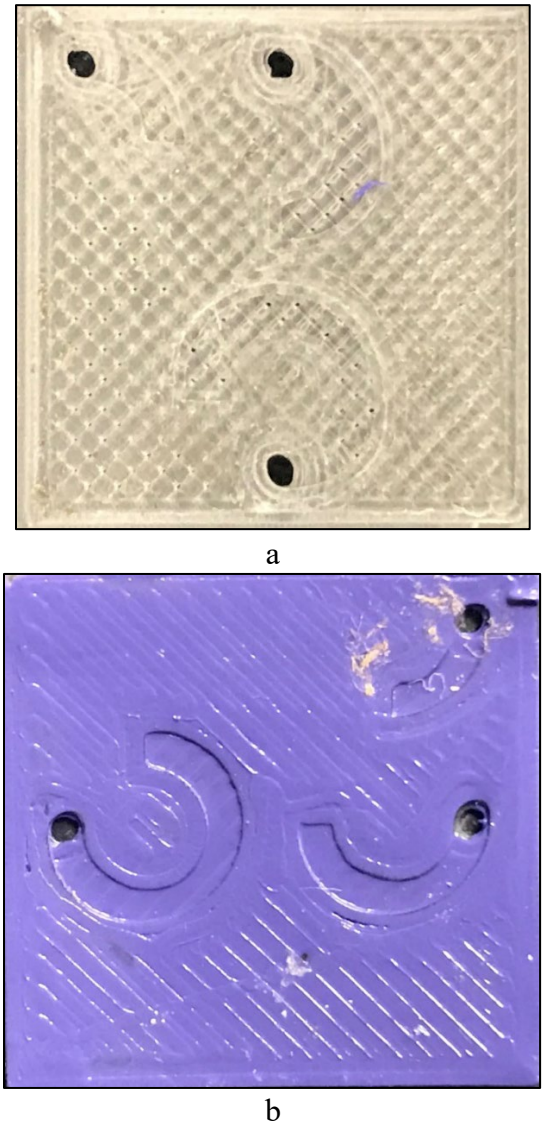
3.2.4 – BVOH Method of Fabrication Overview

Here we use a 3D printer (Creality Ender 3) a fused deposition modeling printer. The printer 180mm/s. The material used to print the mold is butenediol vinyl alcohol co-polymer (BVOH) which is majorly used as a support material for other 3D printing projects. The printing temperature of the BVOH is about 220ºC before extrusion begins, the printer is generally

equipped with a 0.4mm nozzle but to get improved resolution, a 0.2mm nozzle diameter is installed.

a. A .stl file of the mold containing a negative image of the compliant structure(s) is 3D printed directly on a printed circuit board after calibrating the appropriate offset distance between the print bed and the nozzle.

b. The mold is painted with a coating (Nitrocellulose), to prevent the copper sulphate absorption by the BVOH mold and allowed to dry.



a

b

Figure 3-9: (a) BVOH print without cellulose coat (b) BVOH print with cellulose coat

Just as the ABS method, the steps after b, is followed with a slight difference between the next steps of the BVOH and ABS discussed below

i. The degradation of the BVOH material makes the deposition process of this material considerably slower and the optimal growth rate is 5.85 x 10^{-4} mm^3/min for the copper post.

ii. The mold is dried at ambient room temperature before the next feature plating and before the application of the seed layer i: e Caswell-plating copper conductive paint. The paint is applied on the design path printed (horizontally) using a 200 μm thick laser cut stencil and allowed to dry for 1 hour.

iii. The setup is started again to allow the off-chip structure to grow for about 2 – 3 hours depending on the geometrical design. This has a slower growth rate of 2 x 10^{-3} mm^3/min to also help reduce the surface roughness of the pad

f. After the process and sample refinement, the mold is removed by placing the sample in a bath of Acetone to remove the cellulose coat and after complete removal of the cellulose coat, the mold is placed in a beaker of warm distilled water at about (40 – 60^0 C) and a sonicator may be used to agitate the water and consequently increase etching of the mold thus exposing the free-standing interconnect can be seen and ready for assembly.

3.3 – Process Refinement

At this stage, the interconnect has been fabricated but some post-fabrication process refinement, step e needs to be done before step f.

Some of the major concerns that are corrected with the post-refinement process are:

- Beam surface roughness for solder flux and reflow

- Design and fabrication dimension/shape accuracy for precise mechanical (in-plane and out-plane) and electrical characterization and prediction.

After step d, the cleanroom photo-etching process is done on the fabricated structures before removal of the mold.

1. The sample is polished using a Dremel power tool polisher until even surface height is visible and the surface is smooth enough for solder ball attach.

Figure 3-10: Power polishing tool

2. A negative photomask is printed used for ultraviolet light exposure of the photoresist on the beams and is laminated on the sample for etching.

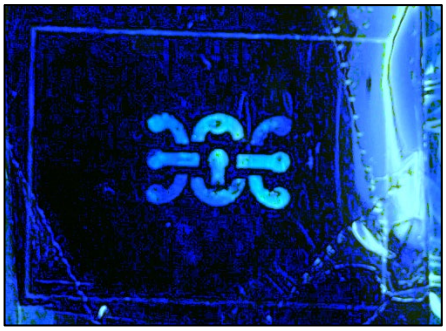


Figure 3-11: Printed negative photomask on a fabricated sample

3. After exposure, the photoresist is developed in a Sodium Carbonate bath and the sample is later placed in a conveyor Chemcut SA2315 spray etcher containing ferric chloride and ran for 2 cycles.

Figure 3-12: Exposed dry film on a fabricated sample

4. After the etching of the copper, the photoresist is removed using a bath of Isopropyl alcohol. In the cleanroom photoresist process, step 1 is repeated using a liquid photoresist on the interconnect pads to identify and earmark points for solder placement during assembly.

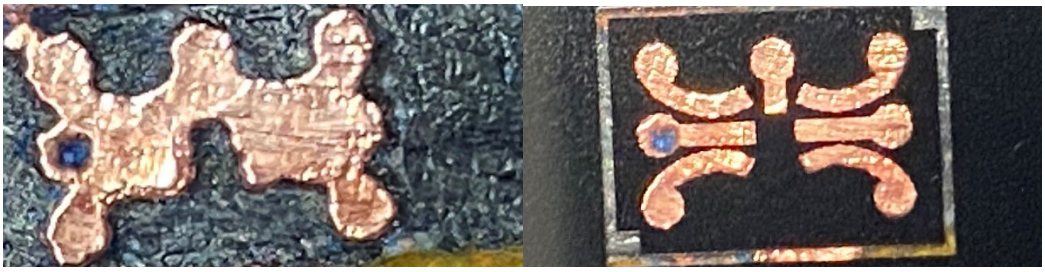


Figure 3-13: Optical images of interconnects (a) before polishing (b) after polishing

3.4 – Assembly

The assembly process is identical to the conventional flip-chip assembly method with the use of solder flux, a mechanical alignment fixture to prevent displacement from shock, and a reflow oven.

The Sikama falcon 5c reflow profile for SAC 305 was adopted from its preset temperature profile [63], [64].

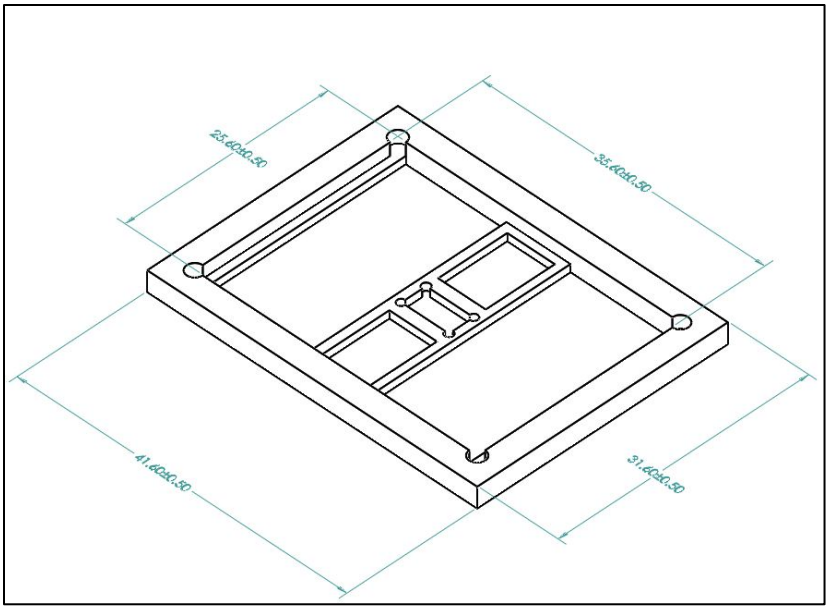


Figure 3-14: Die assembly mechanical fixture design

The fixture is designed with edge tolerance to allow proper placement in the design. The fixture has two designs and fixtures area, one to hold the die and the other to hold the substrate while also accounting for the height of the interconnect.

Firstly, the die is prepared in the cleanroom by attaching the solder mask for solder placement. Solder flux Kester TSF-6522 is then applied over the interconnect and allowed to dry and the solder balls, 305 mm in diameter are placed precisely with the aid of a solder mask, and a mechanical fixture is used to prevent the die from being displaced.

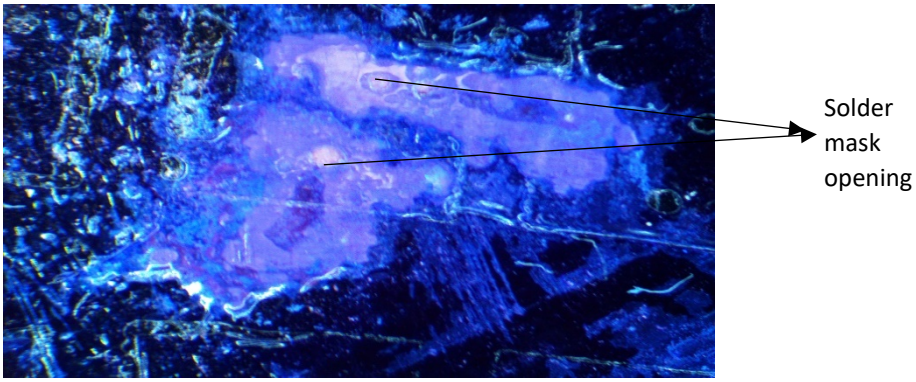


Figure 3-15: Solder mask opening on interconnect

The mechanical fixture is machined from graphite to aid effective heat transfer from the top end of the reflow oven through the die for solder reflow.

The SAC 305 reflow profile is selected for the solder reflow with reflow properties shown in table 3-2.

Table 3-2: SAC 305 solder ball reflow temperature profile

Time (sec)	**Temperature** (C)
0 – 90 (Preheat)	25 - 150
90 – 180 (Soak)	150 - 180
180 – 240 (Reflow)	180 – 220
240 – 270 (Cool down)	220 - 150

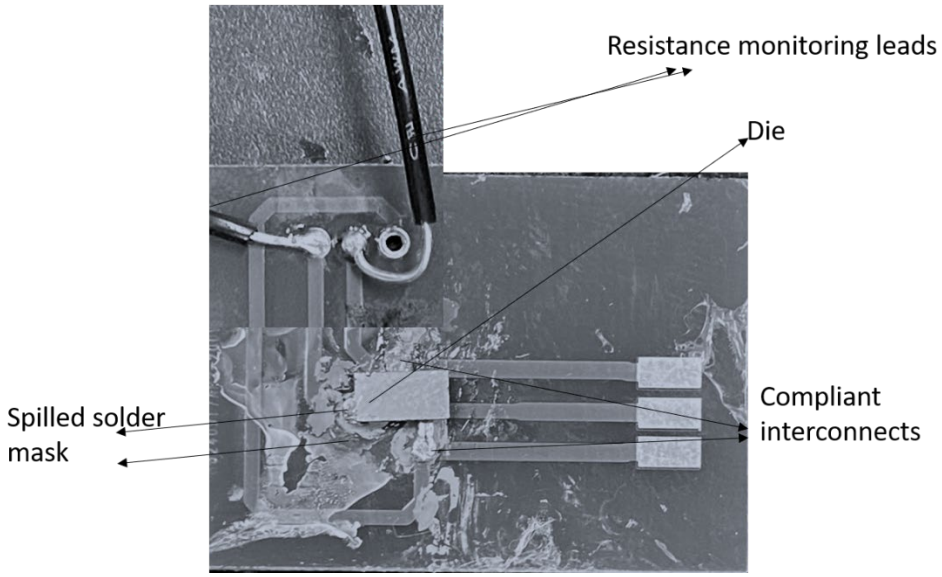


Figure 3:16 Assembled device for testing

3.5 Process and Material Characterization

The materials within the process are characterized to understand the interactions within the process and how these reactions can affect the reliability of the process, manufacturing parameters, or even design conditions to account for and if there are any material degradation such as swelling, etching, etc.

3.5.1 – BVOH Characterization

BVOH is a water-soluble material and therefore becomes unreliable when in contact with liquids and reacts differently to different solvents. Here, the study of how BVOH reacts in all the working fluids used in this process such as Acetone, Copper Sulphate solution, and deionized water is presented.

The BVOH is characterized to understand the standard degradation time per mass of mold which can be integrated to optimize the volume of the structure being fabricated and enable decision in electrical parameters for faster deposition within the mold's durable period and before degradation.

This process is characterized by weight measurement of a sample of BVOH before and after interval time in the various test solution

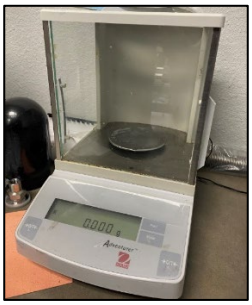


Figure 3-17: Weight measuring apparatus

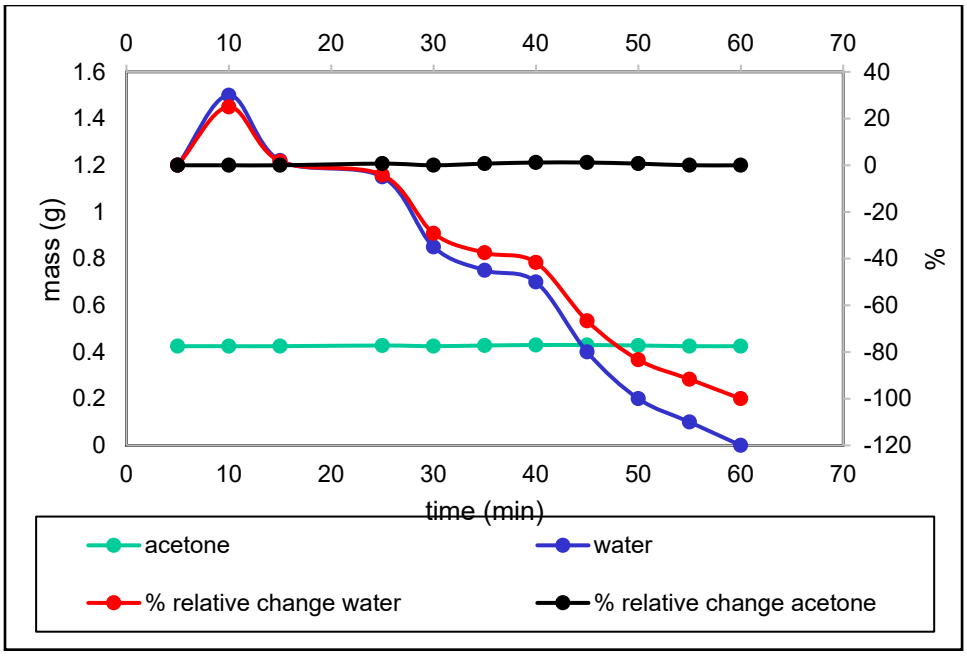


Figure 3-18: BVOH etch rate and reaction in acetone

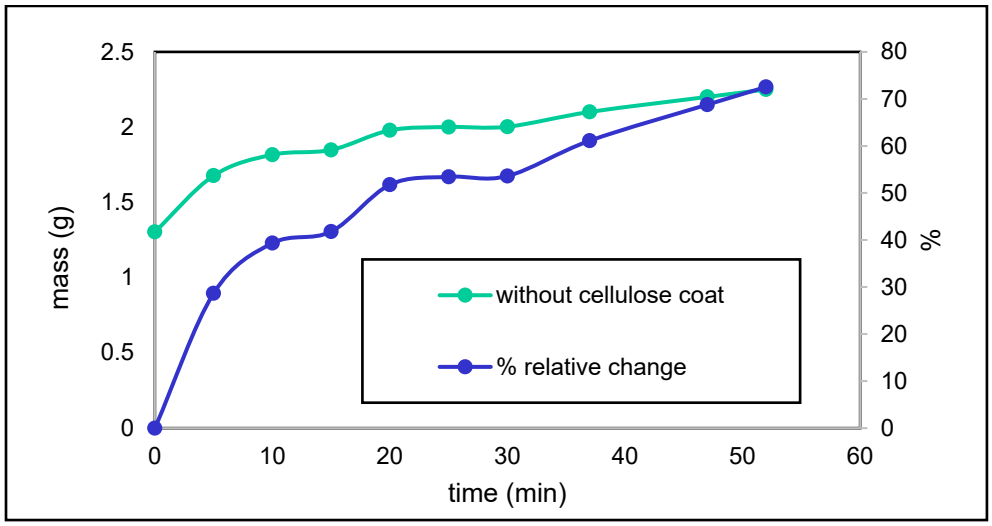


Figure 3-19: BVOH copper sulphate absorption rate without cellulose coating

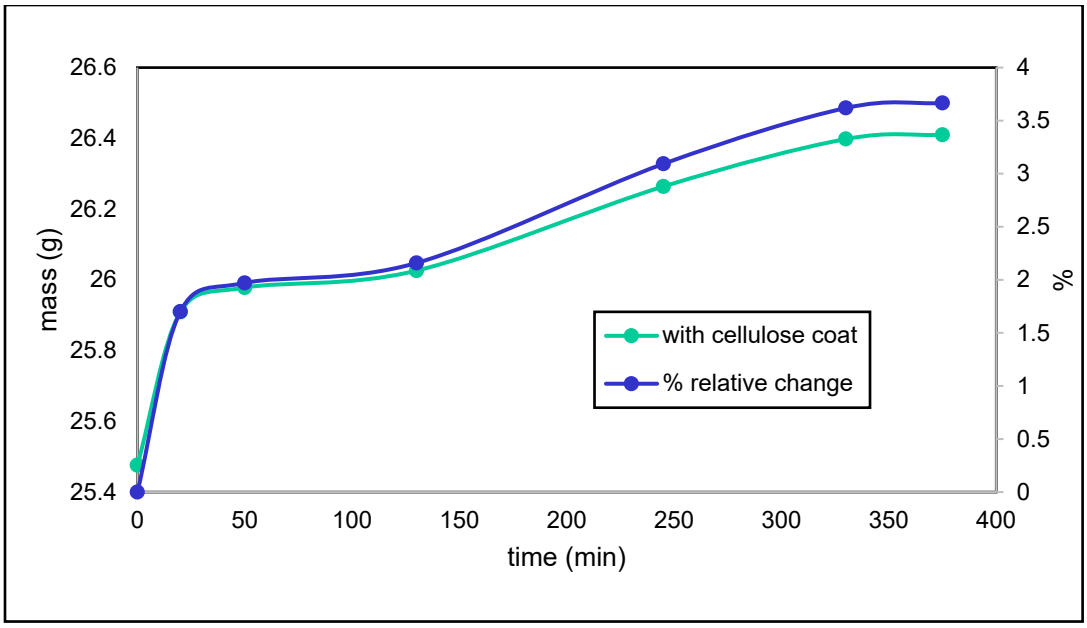


Figure 3-20: Partially coated BVOH absorption rate

As illustrated in the charts above, the BVOH absorbs the copper sulphate liquid and this is observed by the increase in the mass of the sample over time, hence the use of the cellulose coat to reduce the absorption rate of the BVOH. One of the major drawbacks of this solution absorption is the effect it has on the electroforming quality. Little or no copper is deposited through the mold when the BVOH expands due to solution absorption as the cavities printed in the mold would be blocked.

The application of the cellulose coat slows down the absorption rate and allows the integrity of the mold for the electrodeposition of the copper post for a couple of hours before swelling starts to occur.

BVOH is relatively stable in acetone and there is no significant mass change when left in acetone. In figure 3-15, we can see that the BVOH readily dissolves in water and can easily absorb moisture when left open without desiccants

3.5.1.1 BVOH Mold Negative Path Degradation

Here, a 3D printed mold is characterized for physical degradation by optical observation in the changes in the mechanical structural integrity of the mold, thus affecting the fabrication process. Although the cellulose coat can slow down material degradation, if electrodeposition is too slow, copper sulphate will eventually penetrate the mold. Figure 3-18 below shows a soggy coated and uncoated BVOH mold to illustrate the unreliability of this material.

Figure 3-21: Visible degradation during electrodeposition of BVOH (a) Without coating (b) With coating

3.5.2 – ABS Characterization

A concurrent study on ABS is also done by characterizing its reaction within the working fluids as a comparison to BVOH. The characterization of ABS is done to establish an understanding of material reaction and effect that can affect the design and electrodepositing parameters. ABS is readily soluble in acetone and copper sulphate does not have a huge impact on ABS.

The chart below shows that ABS does not absorb the copper sulphate solution evident from the little change in mass of the ABS material with time in fluid and thus the design and manufacturing conditions do not need to alter.

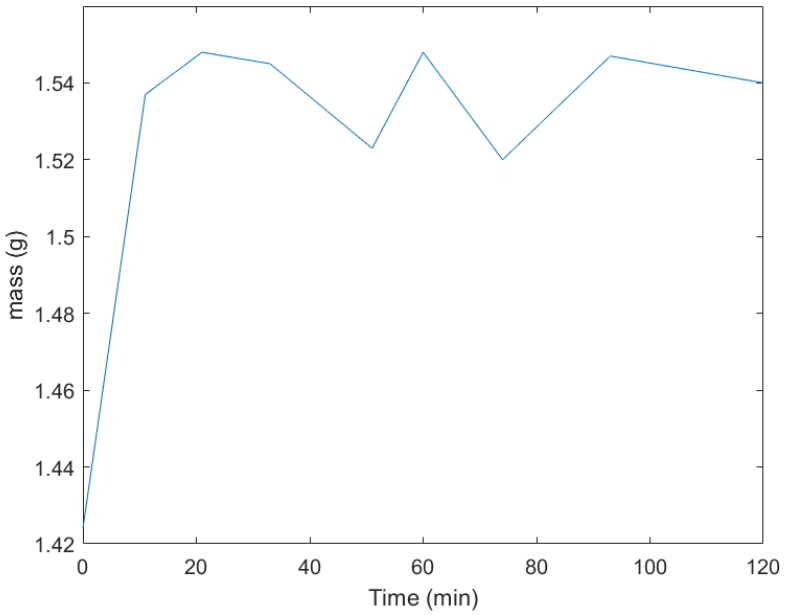


Figure 3-22: ABS reaction in copper sulphate solution

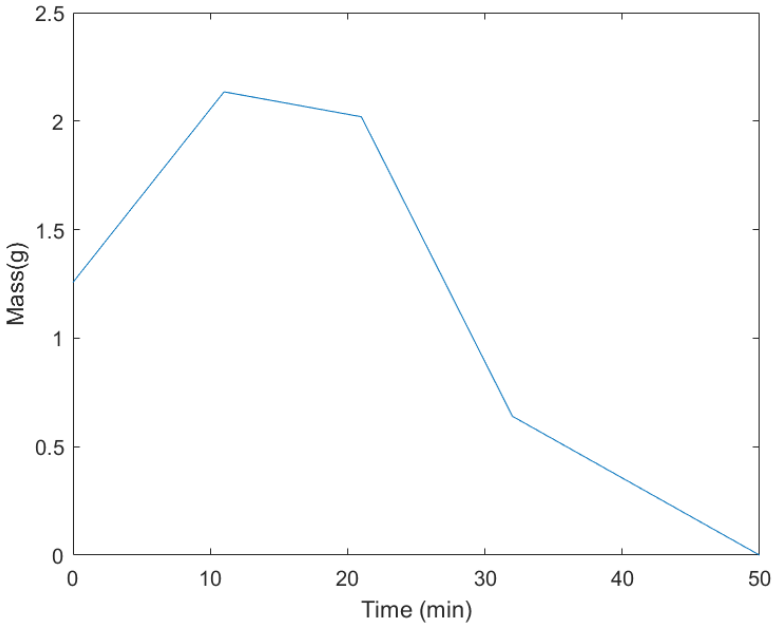


Figure 3-23: ABS etch rate in acetone

Since there is no visible mass change of the ABS material in the copper sulphate, the integrity of the material is thus stable for uninterrupted additive deposition of copper and thus, no further study of the material mold shape degradation is required.

4. INTERCONNECT MODELLING AND CHARACTERIZATION

(Modeling and Simulation)

Multiple arrays of interconnects have been fabricated and characterized for their compliance capability to determine their mechanical stiffness. Experimental test setups are validated by mechanical modeling and simulations.

The materials are modeled to match operating conditions and material behaviors including linear, nonlinear, elastic, and inelastic behaviors.

4.1 - Material Modeling

To accurately understand the overall impact of these structural enhancing technologies, there is a need to understand the fundamental behavior of the package during thermomechanical loading, representing real-life operating conditions.

Typically, mechanical loading may be linear and nonlinear. The materials used in the modeling of the packages include Flame repellant 4 printed circuit board (FR4), copper, lead-based solder, Pb37Sn63, and silicon carbide die.

4.1.1 - Solder

Solder is modeled as a Viscoplastic material due to its constitutive behavior under stress where solder behaves more linearly than linear causing an inability to go back to its original undeformed shape after loading describing its inelastic behavior.

To replicate the mechanical behavior of this material, Anand's model is used to model the solder ball's nonlinear behavior and the input parameters are illustrated in table 4 -1.

$$\frac{d\varepsilon_p}{dt} = Ae^{\left(-Q/Rt\right)}\left[\sinh\left(\xi\frac{\sigma}{s}\right)\right]^{\frac{1}{m}}$$

$$\text{Where } \dot{s} = \left[Signh_0\left|1-\frac{s_0}{\hat{s}}\right|^a\right]\cdot\dot{\varepsilon}_p$$

$$\text{And } \hat{s} = \hat{s}\left[\frac{\varepsilon_p}{A}e^{(Q/RT)}\right]^n$$

Equation 4–1: Anand's model of viscoplasticity

Table 4-1: Anand's parameters for Pb37Sn63

Anand's parameters for Pb37Sn63		
Poisson's ratio	v	0.38
The initial value of deformation resistance	S_O	1.241E+07 MPA
Activation Energy/ Universal gas constant	Q/R	9400 K^{-1}
Pre-exponential factor	A	4E+06
Multiplier of stress	ξ	1.5
Strain rate sensitivity of stress	m	0.303
Hardening/ softening constant	h_O	1.379E+09 MPa
Coefficient for deformation resistance saturation	ŝ	1.379E+07 MPa
Strain rate sensitivity of saturation (deformation resistance)	n	0.07
Strain rate sensitivity of hardening or softening	a	1.3

4.1.2 - Copper

Copper is modeled as a strain-hardening material model due to its material properties [61,62]. The strain hardening data used in computational modeling are highlighted in table 4-2 below. Chaboche's viscoplastic model is used in the nonlinear modeling of copper and includes the strain hardening effect of copper [65].

Table 4-2: Strain hardening parameters for nonlinear copper alloy

Chaboche's Kinematic Hardening parameters					
Temperature (C)	Yield Stress (Pa)	Material constant c1(Pa)	Material constant y1	Material constant c2 (Pa)	Material constant y2
20	4.5E+07	5.4041E+10	962	7.21E+08	1.1
50	3.8E+07	5.288+10	1000	7E+08	1.1
150	3.3E+07	4.576E+10	1100	6E+08	1.1
250	1.3E+07	3.804E+10	1300	4E+08	10
500	4E+06	2.8952E+10	1700	3E+08	35
800	2E+06	1E+10	2000	1.5E+08	50

4.1.3 - FR4

FR4 is modeled as a temperature-dependent linear elastic material and designed without the PCB internal connections such as plated through holes etc. and other electrical components commonly present within a PCB as illustrated in figure 4-1.

Figure 4-1: (a) Modeled shape of PCB (b) Actual shape of PCB highlighting internal components

4.2 - Mechanical Compliance

Mechanical compliance study involves studying the behavior of the interconnect when loading is applied in the vertical and lateral directions. The vertical compliance is the main determinant in the decoupling of the die and substrate z-axis displacement during thermomechanical expansion while the lateral compliance determines the surface displacement of the at the interconnection faces due to non-planarity after expansion.

An experimental study was performed to understand the effect of the dimensions of the design variables of the interconnect by applying a unit load at the edges of the beams. Experimental and simulated studies were done.

4.2.1 – Mechanical Stiffness and Compliance Study

To validate our testing approach, we conducted finite-element simulations. The underneath surface of the copper post is kept fixed in the simulations. An array of forces is were applied at strategic points highlighted in red in figure 4-2 below to help characterize vertical and lateral compliance. Vertical and lateral compliances are simulated by applying load in the out plane and in-plane direction, respectively. The deflection per load application is determined and the compliance is subsequently determined using the formula below and highlighted by the slope of the deflection (compliance) charts in figure 5-2.

$$C = \delta / F$$

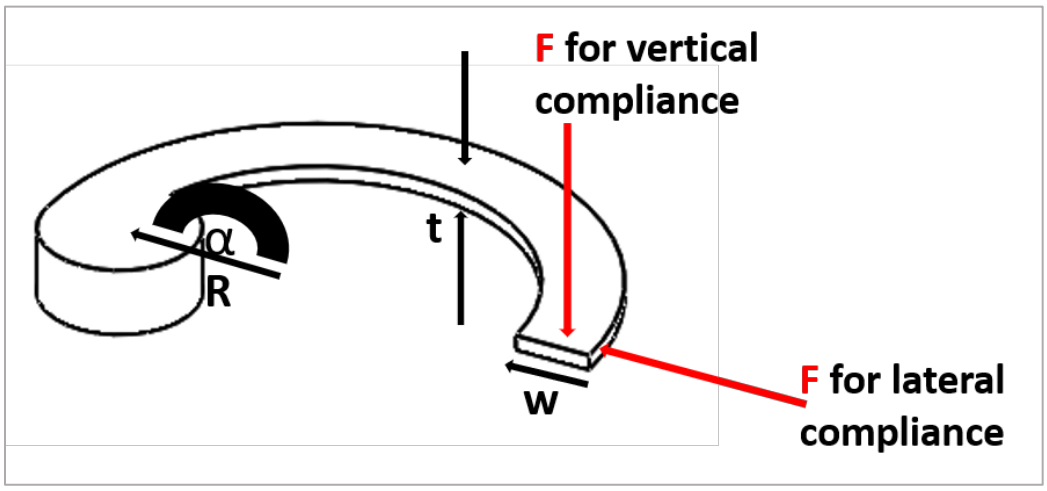


Figure 4-2: Directional application of force for lateral and vertical compliance measurements

The mechanical compliance is inversely proportional to the mechanical stiffness of a beam and for best deflection and beam sensitivity, a high compliant beam will be ideal typically influenced by the length of the beam but constrained by area mapping of the package for implementation. The effect of the subtended angle (α) from simulations is compared with the results from experiments and illustrated in Figure 5-2. Further study on the effect of other variables was done by simulations to reduce the error bound from experimental work and limitations in manufacturing and characterizing very small dimensional effects.

4.2.2 – Mechanical Characterization and Study

The Figures below explain the effects of the above-mentioned variables on mechanical stiffness, K. These variables have been studied closely and their effects have been reported and explained.

Mechanical stiffness and compliances can be calculated and characterized for each beam using the formulas below.

$$\delta = \frac{FL^3}{2EI}$$

where I and K is

$$I = \frac{wt^3}{12}$$

$$k = \frac{2EI}{L^3}$$

Where K is the Mechanical stiffness;

I is the moment of inertia;

δ is the deflection of the beam in distance

Equation 4–2: Beam deflection equations for a cantilever beam

4.2.2.1 – Experimental Effect of Subtended Angle (α) on Mechanical Stiffness

A study on the effect of the stated variables on compliance and mechanical stiffness was limited to the variable effects on the 270^0 subtended angle beam but the behavior of this beam is not limited to this structure type as this structure shape and type follows fundamental beam theory equations applicable to other structures. The increase in the subtended angle directly increases the length of the beam and studies show a drop in mechanical stiffness as the subtended angle is increased. This change and effect of the subtended angle are shown in figure 4-3.

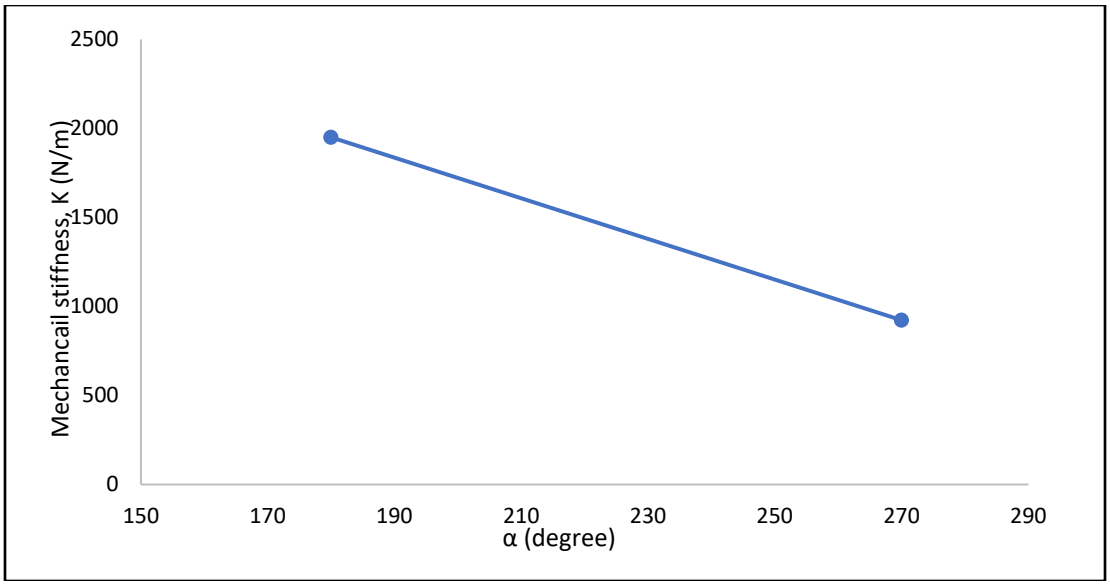


Figure 4-3: Effect of subtended angle (α) on mechanical stiffness and compliance of the beam

4.2.2.2 – Effect of Beam Width (w) on Mechanical Stiffness and Compliance

Computational studies have been done on the 270^0 cantilever beam and observed a significant increase in both in-plane (lateral) and out of plane (vertical) compliance with every decrease in the width of the beam. Here the moment of inertia reduces as the width of the beam reduces due to the inversely proportional relationship between them. Also, the average length of the beam reduces as the width of the beam reduces due to its geometry causing a reduction in length of the beam towards the inner arc. Therefore, the chart, figure 4-4 shows an increase in mechanical stiffness as the width of the beam increases, see figure 4-4.

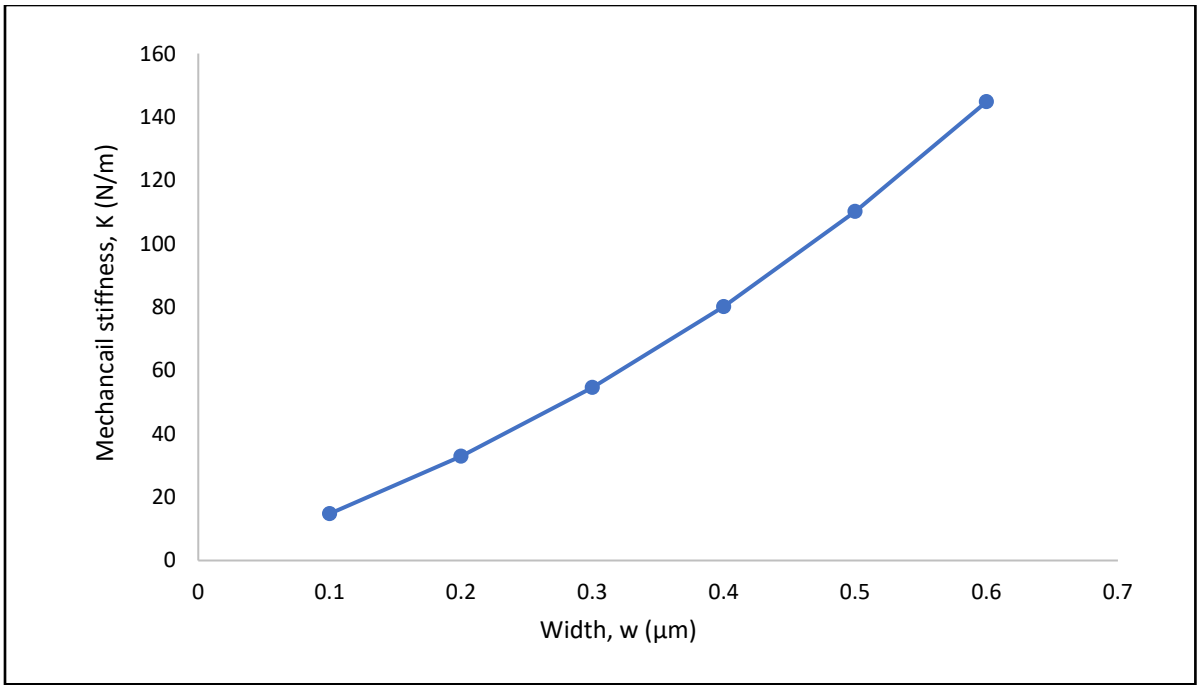


Figure 4-4: Effect of width (W) on mechanical stiffness and compliance of the beam

4.2.2.3 – Effect of Beam Thickness (t) on Mechanical Stiffness and Compliance

The increase in thickness also greatly decreases compliance in both lateral and vertical directions. By following the beam equation, the thickness of the beam is directly proportional to the moment of inertia and subsequently, an increase in the thickness of the beam increases the mechanical stiffness of the beam.

4.2.2.4 – Effect of Beam Length (L) from Center Radius (R) on Mechanical Stiffness and Compliance

Further study on the compliance effect with varying center radius, showed that the center radius is directly proportional to the length of the beam and directly proportional to the compliance and deflection of the beam. This causes a decrease in mechanical stiffness because of the increase in average beam length from both sides illustrated in figure 4-5.

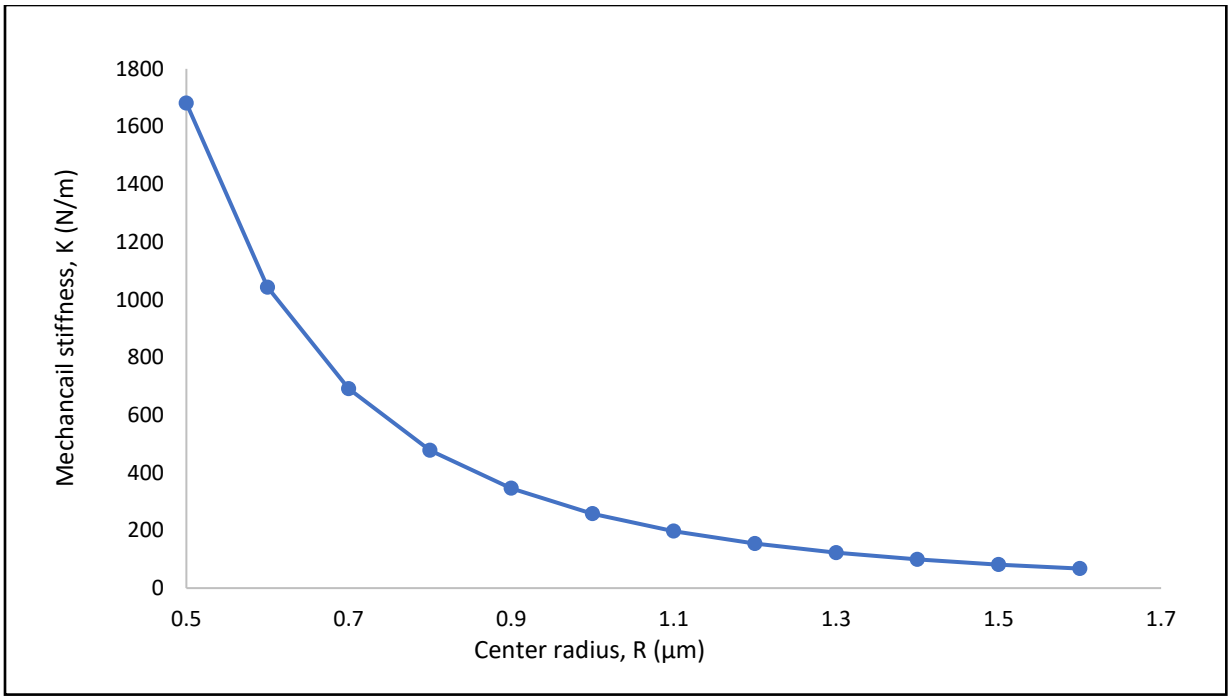


Figure 4-5: Effect of the center radius (R) on mechanical stiffness and compliance of the beam

4.3 - Interconnect Thermomechanical Fatigue Life

4.3.1 - Copper Compliant Interconnect Fatigue Life

Copper has a very close coefficient of thermal expansion (17 ppm/^{0}c) when compared to printed circuit boards (14-17ppm/^{0}c) and therefore the effect of cracking or fatigue will be reduced due to a lower CTE mismatch like between solder balls, SAC 305 (23.5ppm/^{0}c) and PCB for example [66].

Fatigue life simulation is done on varying design dimensions to understand which dimensions most affect the reliability of the structures. Thermomechanical simulations are used to determine the most strained element of the interconnects due to accumulated plastic strain and is typically the susceptible area for crack initiation and crack growth used to determine the life cycle.

To accurately predict the fatigue life of the interconnects after simulation and determining the accumulated plastic strain data across one thermal cycle, the coffin Manson equation is used to determine the fatigue life of the components.

The site with the maximum plastic strain is usually at the edge of the beam where the beam meets the copper post regardless of the geometry highlighted below.

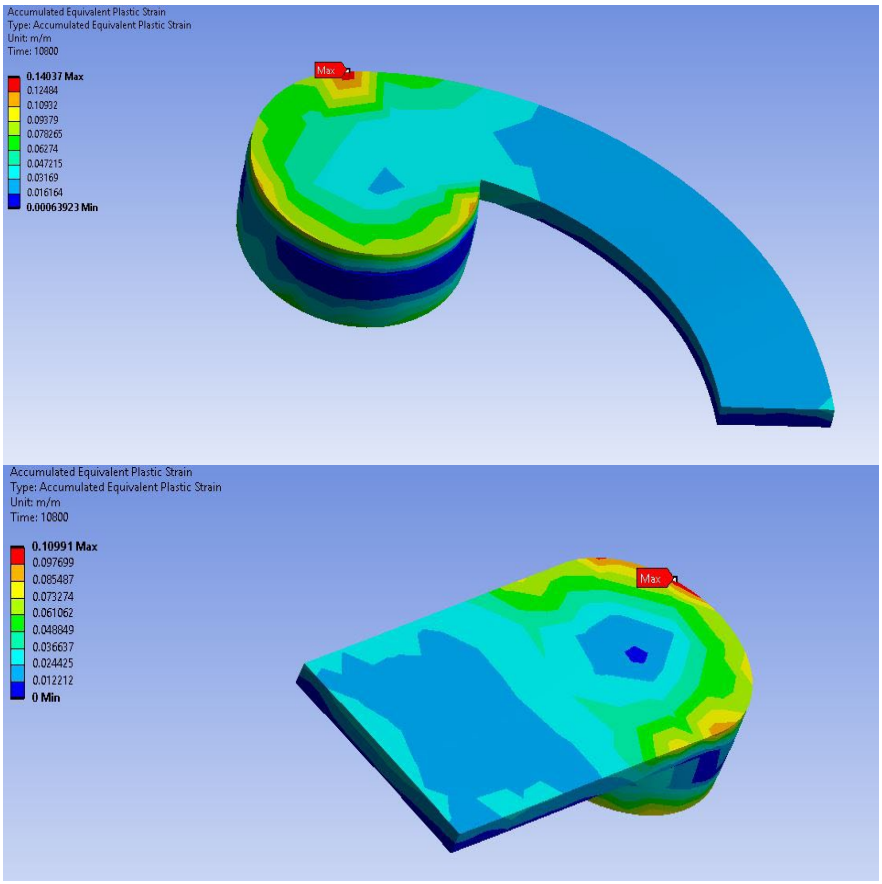


Figure 4-6: Maximum accumulated plastic strain for curved and straight beams

the Coffin-Manson based equation used is illustrated below.

$$\frac{\Delta \varepsilon p}{2} = \varepsilon f (2N)^{\mathrm{n}}$$

Where $\Delta \varepsilon p$ is the accumulated plastic work across a cycle.

N is the number of cycles to failure,

ε_f and n are numerical constants with value 0.56 and -0.6 for copper respectively [67]

Equation 4–3: Coffin Manson fatigue life equation

The result below shows a constant increase in the lifetime of the copper interconnects as the beam thickness increases highlighting an increase in mechanical strength of the beam causing the beam to withstand more yield. Also, the thermomechanical expansion of the beam is predominantly lateral, and the yield rate would be slower in the vertical direction because of the thickness of the beam. This is different for a change in beam width as an increase in width and could cause a probable increase in cracking due to shear as a larger area is susceptible to cracking.

Further study on the effects of these variables is discussed below and how the solder fatigue life (least reliable component) is affected.

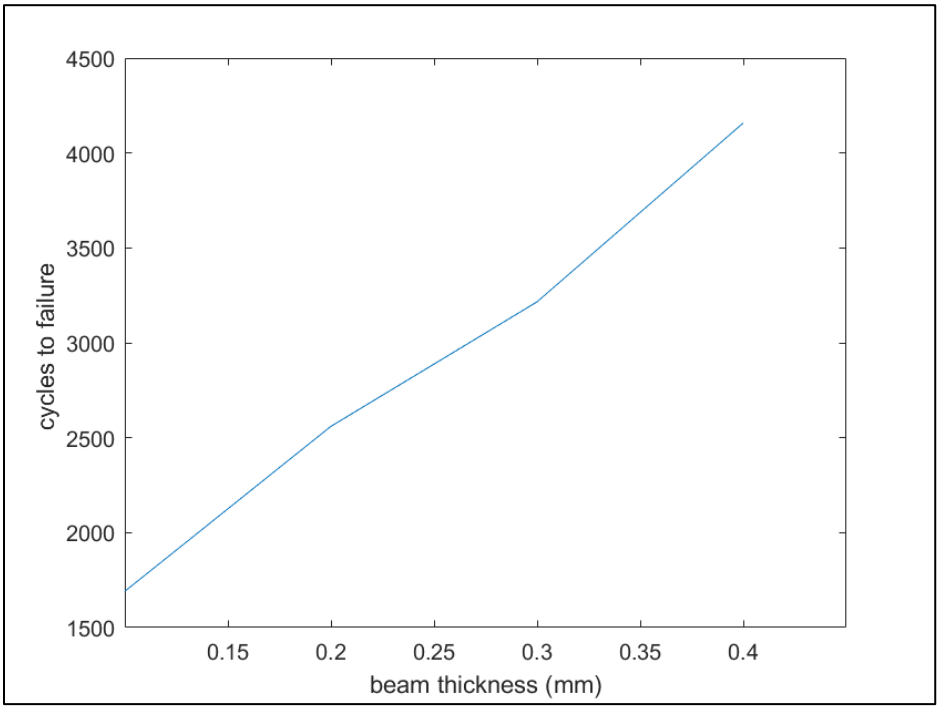


Figure 4-7: Effect of beam thickness of the beam on the lifetime of the compliant interconnects

4.3.2 - Solder Joints Thermo-Mechanical Fatigue Life

Thermocycling simulations highlight the maximum stress in a die package is commonly at the solder joint and this is expected due to the mismatch in CTE even with the aid of the decoupling interconnect structures, they are still suspect for failure and determine the overall reliability of the package.

A simulation was also done to understand the impact of the compliant interconnect structures on the fatigue life of the die and simulated across varying design variables. To simulate this model, other failure modes common with flip-chip technology will not be considered and only the thermomechanical effect of CTE mismatch will be considered and discussed.

Thermomechanical cycling simulation is done on the package with the same modeling input as the copper interconnect structure. The thermal condition data is represented in figure 4-8 below.

One of the major reliability challenges in power electronics is thermal cycling for die- substrate packages. Typically, extreme operating conditions cause mechanical fatigue and cracks in solder ball joints. Industrially accelerated testing is used to predict almost precisely the actual lifetime of components and in this case, solder balls fatigue. Thermal cycling one of the major approaches of accelerated testing usually ranging between -40^{o} C to 125^{o} C. Solder joint fatigue failures are characterized by measuring and observing for change in electrical resistance through the solder ball and interconnect.

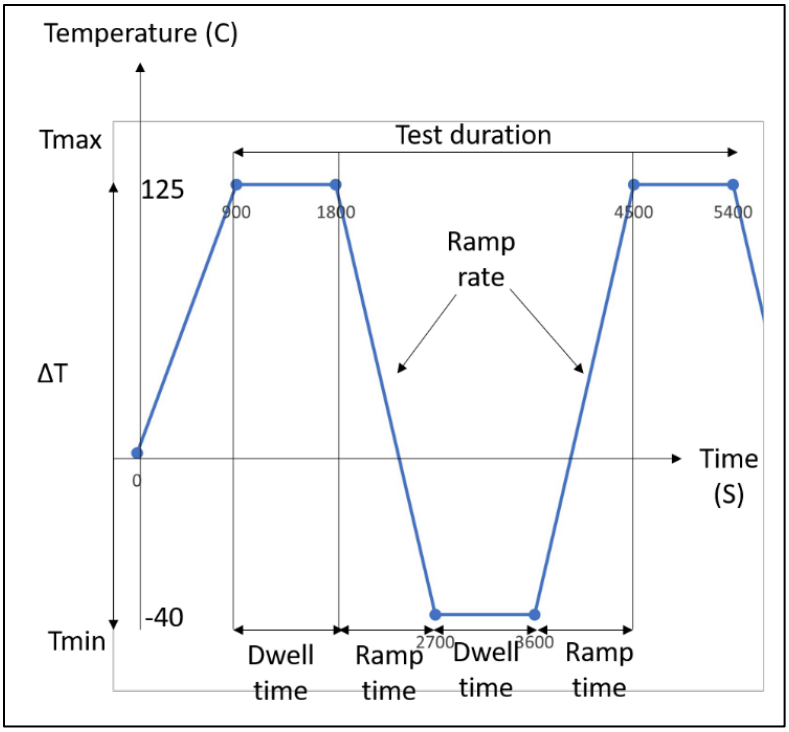


Figure 4-8: Schematic of thermal cycling profile for modeling and testing

An extensive reliability study on the dimensional effect is done via simulation prediction and the Darveaux model has been simulated on Ansys ® for reliability effects at the solder joints for the test vehicle model using solder balls alone and with help of the designed compliant interconnect.

$$N_0 = K_1 [\Delta w]^{k2}$$

$$da/dN = K_3 [\Delta w]^{k4}$$

$$N_f = N_0 + a/(da/dN)$$

Where; N_0 = cycles to crack initiation;

a = the joint diameter at the interface (final crack length); da/dN = crack growth;

Δw = Viscoplastic strain energy density accumulated per cycle of each element;

N_f = cycles to failure

Equation 4.4 – Darveaux model equations

Figure 4-9 below highlights the thermomechanical stress distribution and effects of these mechanical die-substrate decoupling compliant structures on the fatigue life of the solder joints. The maximum von mises stress is higher with the AM Cis integrated package, which occurs at the compliant interconnect and provides effective stress distribution from the solder interconnects and when compared without the AM CI, the package rates of propagation are significantly higher as illustrated in table 4-3 below.

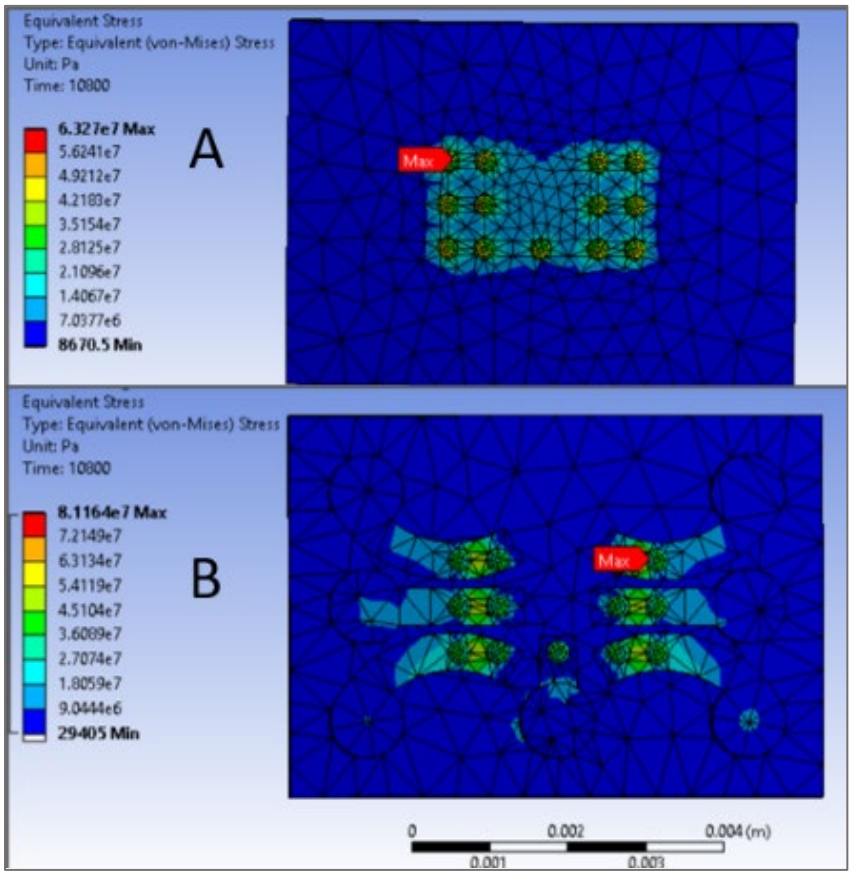


Figure 4-9: Top view of von- Mises stress mapping and distribution for (a) without compliant interconnects (b) with compliant interconnects

To validate the effect of the compliant interconnect in yield stress distribution on the solder joint, the accumulated plastic strain work density was studied and a larger accumulated plastic work value was observed at the solder ball without the compliant interconnect showing more stress is

induced on the solder ball and subsequently causing lower cycles to crack initiation. The strain distribution mapping is illustrated in figure 4-10.

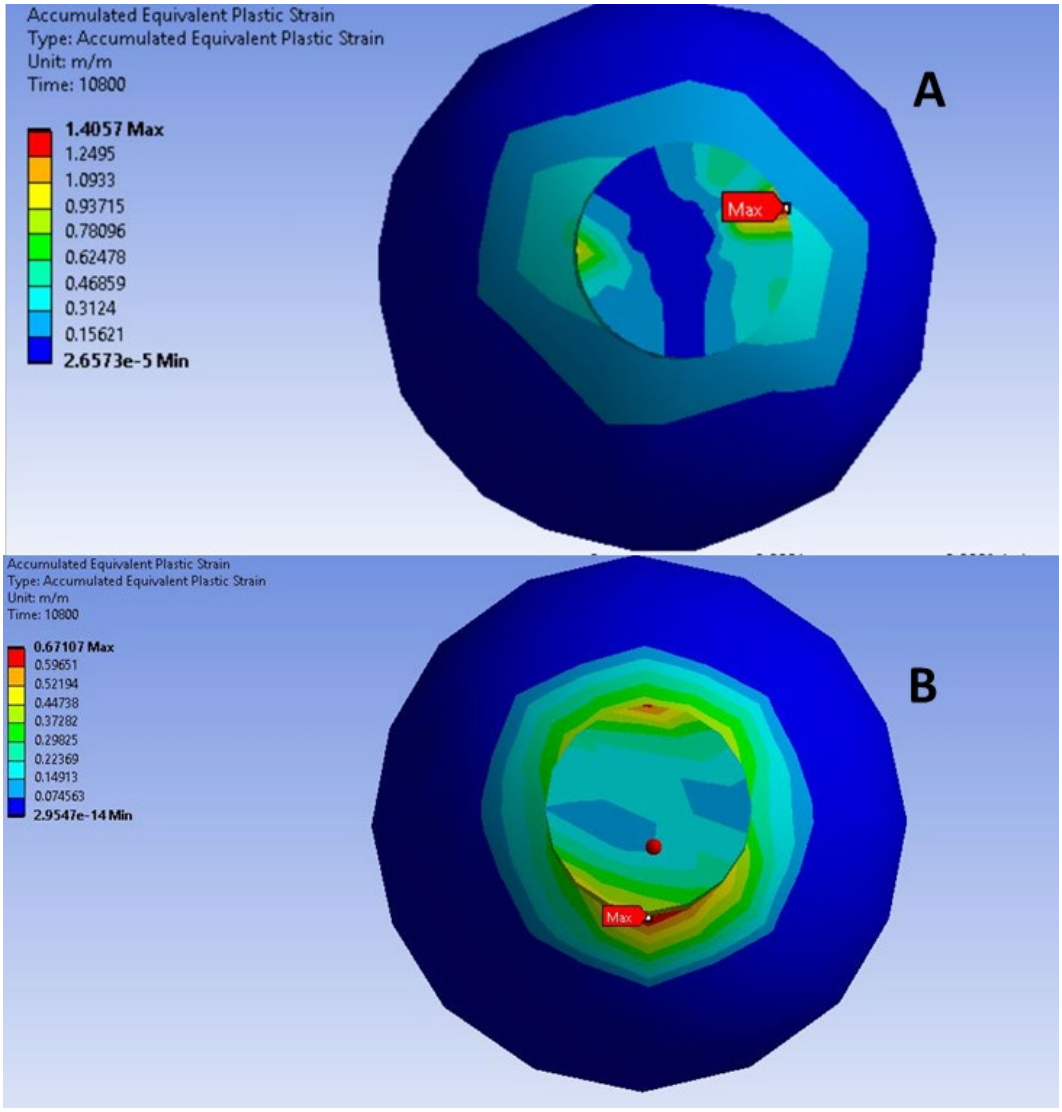


Figure 4-10: Maximum accumulated plastic strain distribution (A) Bare solder (B) Compliant integrated solder joint

Thermomechanical cycling simulations show an improved solder fatigue life on the AM CI integrated package shown in Table 4-3.

Table 4-3: Solder ball cycles to failure comparison of a package with compliant interconnects and package without complaint interconnects

Package type	Cycles to crack initiation	Number of propagation cycles to failure	Rate of crack propagation
Without CI	297	621	2.4
With CI	975	1336	1.1

The fatigue life of the solder balls was studied as a function of the beam width and beam thickness as any increase in the subtended angle or length of the beams will affect the size of the package defeating the concern of the device package miniaturization.

The fatigue life of the solder balls is directly dependent on the compliance of the beams. Figure 4-9 and figure 4-10 below shows a constant partially linear drop in the fatigue life as the thickness and width of the beam is increased. This means that a low compliant beam provides less decoupling area for the solder balls causing an increased stress and strain energy at the interconnect level due to expansion of the copper interconnects overall reducing the lifetime of the solder balls. Conclusively, it is best to select a thinner structure even though this affects the fatigue life of the copper, the copper still has a higher life cycle under the same thermal condition.

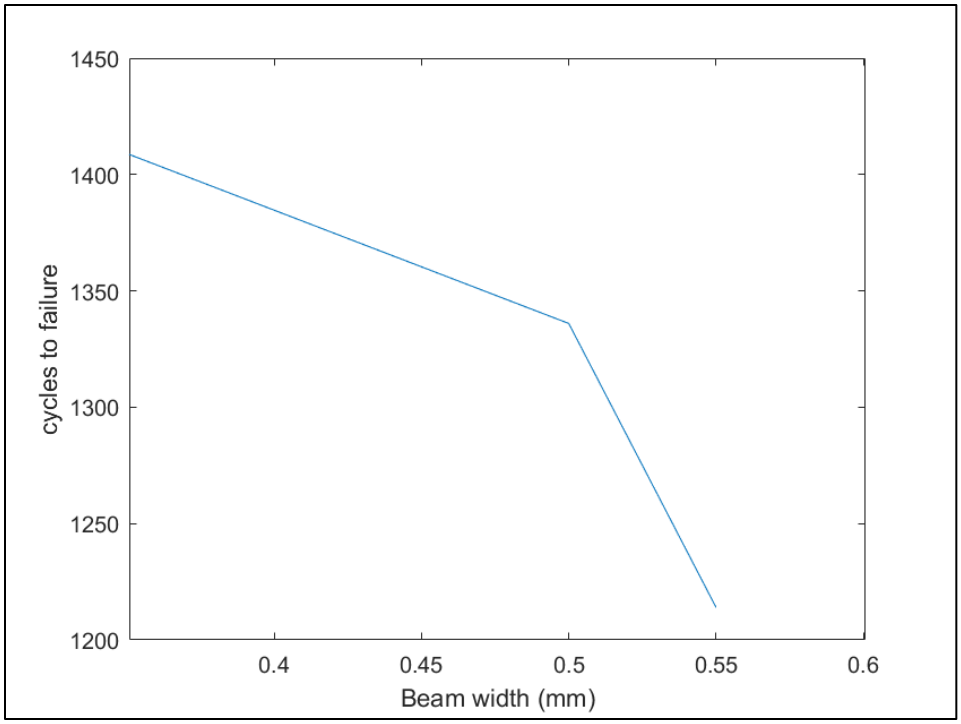


Figure 4-11: Effect of beam width on solder fatigue life

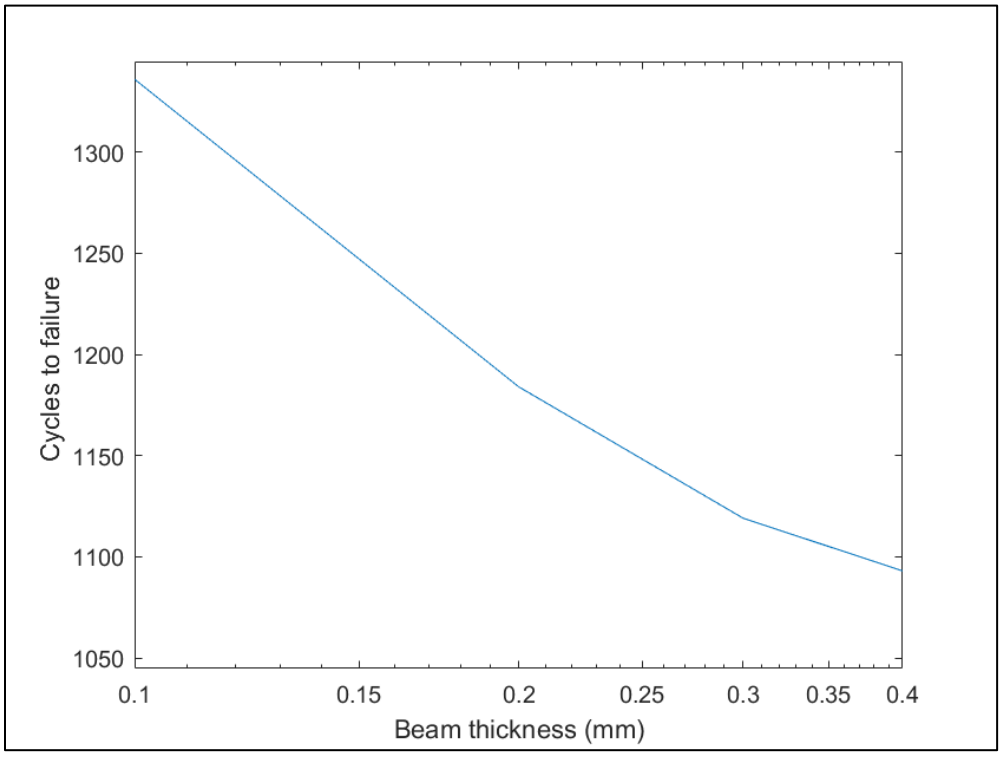


Figure 4-12: Effect of beam thickness on solder fatigue life

4.4 – Electrical Characterization

In addition to the impact of mechanical compliance on enabling improved solder joint reliability and its application, it is also important to consider the electrical properties, performance, and impacts. To study these interconnects, Ansys Q3D simulations for parasitic inductance prediction has been done to give an insight for comparison with other electrical interconnect methods shown in table 4-4. The parasitic inductance is simulated for extreme values for the longest beam length, 270^{o} beam length compliant interconnect presenting the worst possible scenario. The table highlights various interconnect parasitic inductance data. The compliant structure thus has an impact on the inductance of the assembly but is competitive with other interconnection and assembly approaches. Thus, a tradeoff has been achieved for the priority of the device between reliable concerns and electrical performance concerns.

Table 4-4: Electrical inductance comparison of common interconnects methods and compliant interconnects

Interconnection types	Inductance (nH) @ distance between components	Frequency	References
Plated Through Holes (PTH)	0.5 @ 1000µm	72 kHz – 320MHz	[68]
Core Via	0.3 @75 µm	1.6 – 530 MHz	[68]
Through Silicon Via (TSV)	0.2 @100 µm	160 kHz – 800MHz	[68]
Solder Balls	0.008097 @ 762µm	500kHz	[69]
Wire bonds	22.98 @5000µm	100MHz	[70]
Core Via	0.3 @75 µm	1.6 – 530 MHz	[68]
AM Cis with solder balls	0.653 @200 - 500µm	1MHz	**This work**

5. EXPERIMENTAL CHARACTERIZATION AND VALIDATION

5.1 – Compliance Experimental Testing

These interconnect structures and geometry have been designed, fabricated, and experimented with across different subtended angle to and validated with modeling and simulation discussed in chapter 4. Due to limitations in applied loading orientation and size of these structures, the forces are applied at the specified points F in figure 4.2 above. Since these are microstructures, accurate mechanical testing is somewhat difficult to measure. A known solution may be to fabricate the structure in an enlarged form and correlate the compliance. A testing procedure has been improvised using a microhardness tester to apply the varying load at specific points of the interconnect and using an optical microscope to precisely observe and measure the beam's deflection. Figure 5-1 shows the test setup used for deflection measurement.

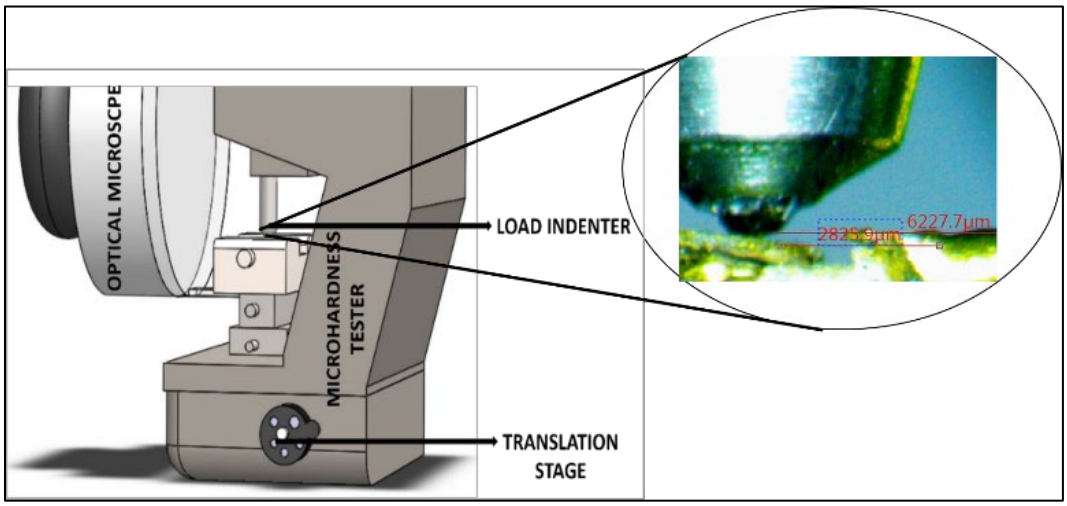


Figure 5-1: Mechanical compliance experimental setup

5.2 – Experimental Testing Comparison with Validation

Figure 5-2 shows a comparison of the simulated data of the deflection for 2 types of subtended angle, 180^{o} and 270^{o}, and data from the experimental test procedure. The estimated mechanical compliance value is highlighted at the top of the chart and we observed an increase in deflection/ compliance of the beam with an increase in subtended angle. The chart also shows the

percentage difference between the two data types by comparing the experimental data and simulation of the deflection of the beams. At some mass loading points, the data shows a close correlation, somewhat validating the mechanical compliance testing approach.

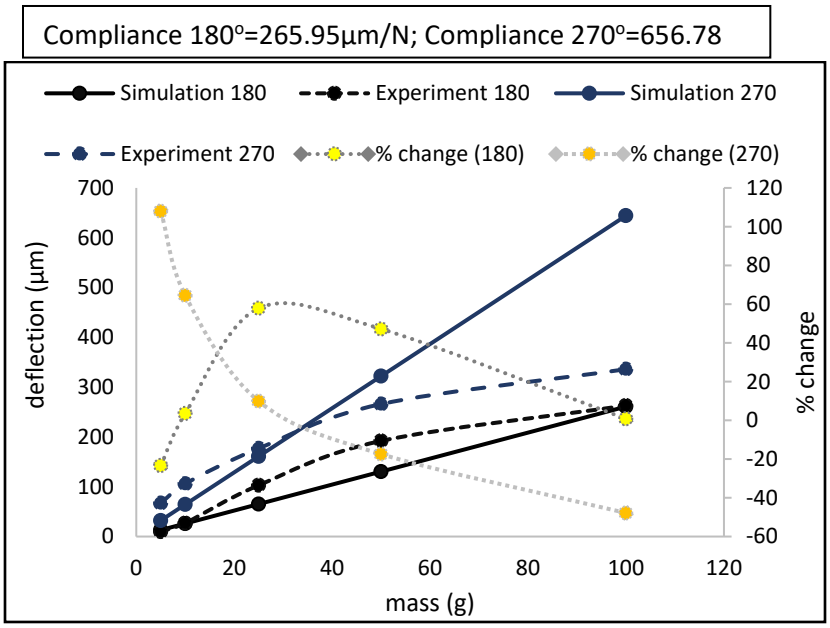


Figure 5-2: Effect of subtended angle (α) on vertical mechanical compliance (Simulation and experimental)

The compliance of multiple angled beams translating to change in length of the cantilevered beam is measured across 2 major angles, $180^{0,}$ and 270^{0}. As expected and visible in figure 5-2, the mechanical stiffness of the 270^{0} is lower evident from the increased deflection of the beam in comparison to the 180^{0} subtended angled beam.

Some of the errors that may have caused a difference in the trend lines between experimental and simulations have been highlighted and discussed below.

- The thickness of fabricated structures: The accuracy of the thickness of the structures after fabrication, may not be consistent with the design due to the inconsistency in electroforming,

across the whole package, where a section of the package may have more chemical/ionic deposition due to uneven current distribution across the surface of the printed circuit board.

- 3D printer dimensional accuracy: 3D printers are evolving, and the current FDM printer's resolution can affect the consistency of the dimensional accuracy of the negative beam print, which may alter the width or length of the beam in the negative print design.
- Etching accuracy: The accuracy of the etching process and accurate placement of the photomask and photoresist may also affect the width and length of the beam if etching is not accurate.
- Loading point consistency: During load placement and testing, the point of load application may not be consistent with the exact point of loading during the simulation.
- Error due to measurement: Errors may occur during testing either from parallax measuring error or error occurring due to the resolution and accuracy of the microscope.

5.3 – Design Strategy for Assembly on Test Vehicle

Due to limitations in 3D printing, the conventional approach of isolated interconnect designs and fabrication per solder ball cannot be readily achieved. FDM 3D printers have a limited negative resolution, and this affects the minimum size that can be printed for the copper post. Various die samples can be selected for this test and the Cree CPM2-1200-0080B Silicon Carbide Power MOSFET is the assembly vehicle chosen and is typically used with thirteen (13) solder points across the gate, drain, and source with one (1), six (6) and six (6) solder ball respectively.

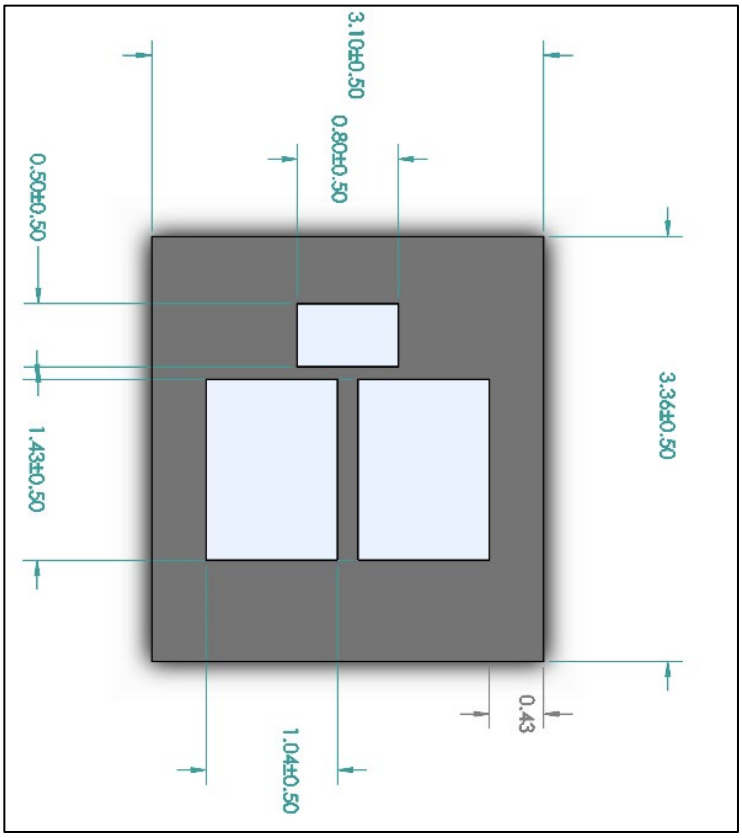


Figure 5-3: Dimensional representation of CREE MOSFET test vehicles

As commonly known and proven by [59] that the edge of the package is the point of the maximum stress (shear and peeling), the number of interconnect can be optimized and designed to accommodate all thirteen (13) solder balls whilst conforming to minimum feature size that can be fabricated. Ideally, it is recommended to follow this design placement approach which puts more compliant structures at the edges and the less compliant structures at the center of the package. The beam at the edges has a longer beam length than the other beams because they are curved to conserve surface area whilst also increasing length.

5.4 – Reliability Prediction Via Experimental Testing

Solder reliability tests span from multiple test types including power cycling PC, thermal cycling TC, highly accelerated life tests HALT, highly accelerated storage test (HAST), etc.

For this study, we have adopted the rapid solder interconnect fatigue life test methodology for predicting thermomechanical reliability developed by Cody J. Marbut, Mahsa Montazeri, and Dr. David R. Huitink [71].

Here an accelerated reliability testing approach was developed and involves the use of a shear testing method to simulate the behavior of shear stresses in an assembled package during thermal expansion/ conditions.

A controlled force is applied based on selected spring deflection to enable the application of shear force at room temperature. The shear force is applied in a lateral direction via the aid of a tribometer to emulate the real-life experience of stress mapping and distribution.

The tribometer used in this setup enables direct contact on the sample by applying load via the aid of mechanical springs which consequently deflects the spring enabling the measurement of the resultant spring force applied on the sample.

The average shear stress across the sample is calculated using the value of the measured spring force and the total cross-sectional surface area of the solder interconnects mechanically supporting the die.

A 3D printed clamp is used to restrict motion to only the interconnects structures (Copper compliant interconnect and solder balls) by gripping just the substrate and testing the dies highlighted by the free body diagram below.

An *in-situ* test is carried out to observe the change in resistance of the solder joint across shearing cycles.

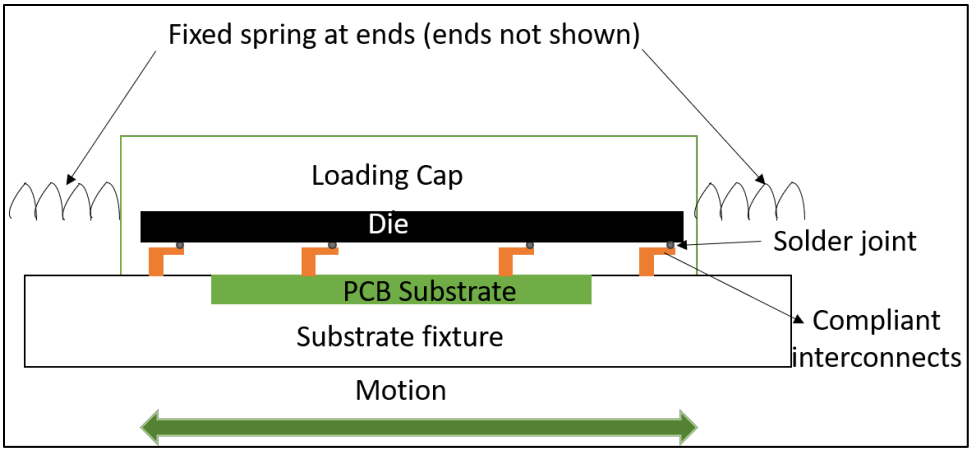


Figure 5-4: loading configuration for resistance in situ shear test

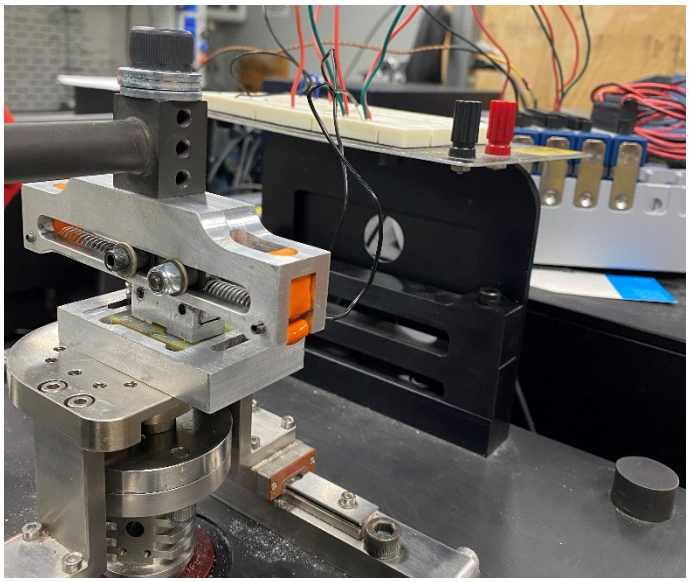


Figure 5-5: Mechanical shear stress test apparatus

5.4.1 - Preliminary Mechanical cycling effect on resistance

To accurately represent the stress-inducing factors and variables of the testing apparatus, data gotten from the tribometer adapted set up was used to determine the spring constant (k) of the setup, the number of cycles, and other stress-inducing factors.

The magnitude of the applied load in the tribometer is based on the set displacement of the input parameters in the setup. To predict the accurate loading values in the axial direction, multiple test calibration is carried out using a 3D printed prototype of the sample. The force values exported

from the tribometer are then used to calculate the spring constant of the springs in the system by dividing the average force by the input displacement in the tribometer.

After calibration, the spring constants were determined to be 300N/m.

$$k = \frac{F}{\delta}$$

Where F is extracted from the force plot in figure 5-6 below.

δ is the set input displacement

Equation 5.1 – Hooke's law equation

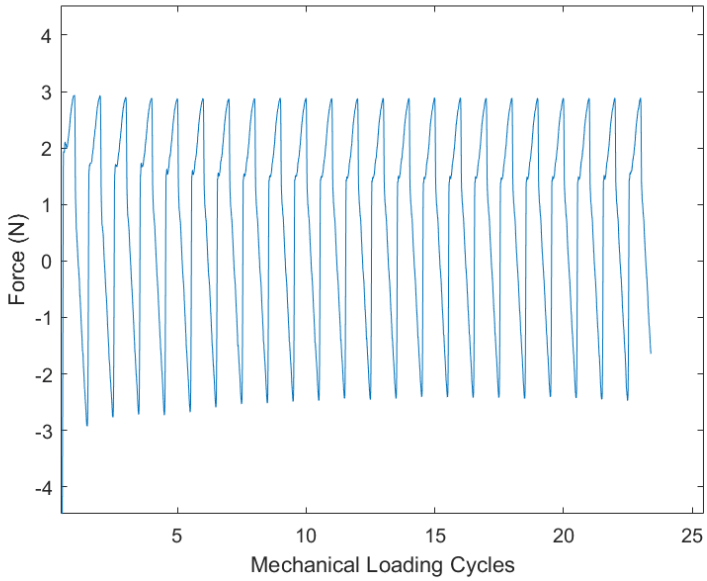


Figure 5-6: Force plot for the test sample

If the springs do not undergo plastic work deformation, any change in the trend of the force plot will translate to deformation of the test samples caused by shearing at the interconnect. The calculated spring constant can be used to calculate deflection/ deformation in the interconnects and other data can be calculated such as shearing stress, plastic work density, etc.[71].

The effective result from using this mechanical testing procedure can be leveraged for direct comparison between both package types, compliant interconnect integrated package and regular flip-chip integrated package under mechanical cyclic loading.

Elevated tests at 100 C were carried out coupled with an in situ resistance testing process to observe the effect of shearing on both packages which can be observed by the rate of resistance change of the package over the first 5000 cycles.

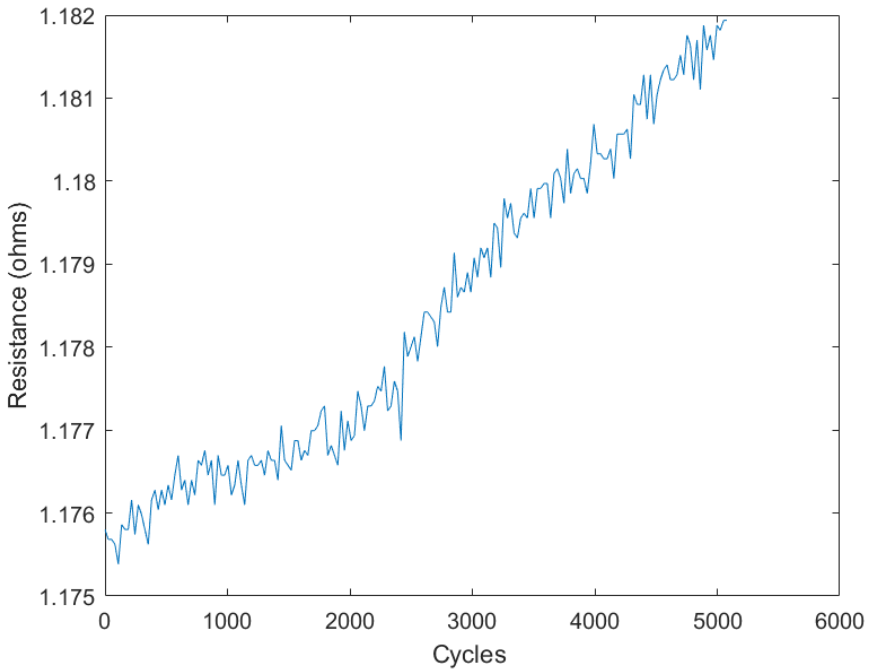


Figure 5-7: Effective resistance to cycle plot of a package without compliant interconnects @ 50 C

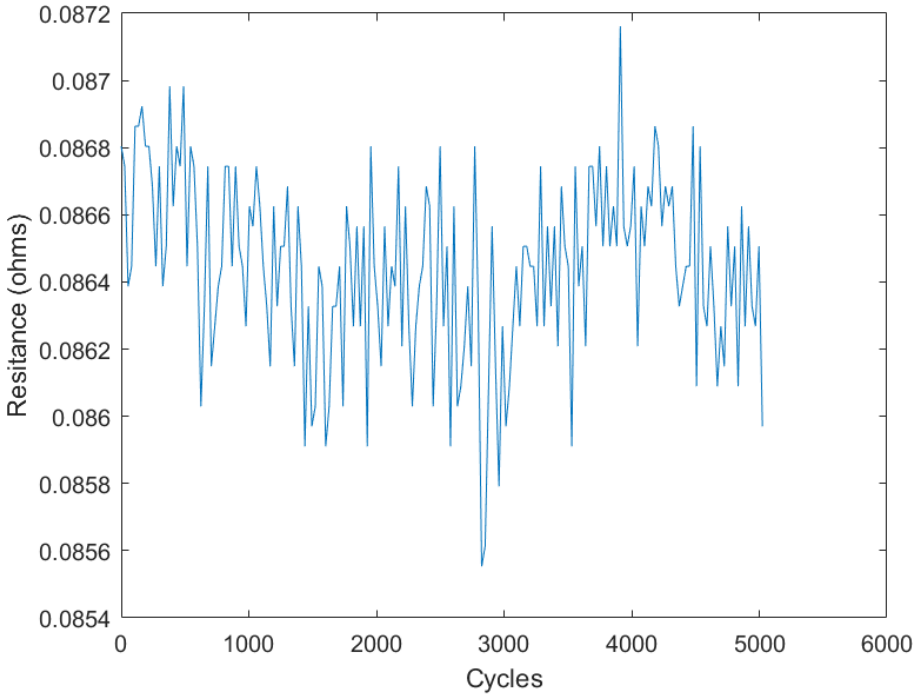


Figure 5-8: Effective resistance cycle plot of a package with compliant interconnects @ 50 C

Preliminary data gotten from this experiment highlights a constant trend line in the resistance plot on the compliant interconnect integrated package, over 5000 cycles while the package without the interconnects indicates constant resistance increase over time.

This rapid and constant change in resistance indicates solder cracking and plastic work deformation occurring at the solder interconnect region from the bidirectional deformation along the axial direction. A gradual increase in the resistance can also be caused by the shape geometry and length when the solder ball is deformed at elevated temperature causing the solder to operate in a molten manner illustrating potential for improved electrical reliability with the compliant interconnects

Other preliminary studies to use these test vehicles to complete failure and break down shows and analyze the mechanism of failures of these devices. The complete shear of the devices is

represented by the drastic reduction in the force from the spring-applied on the die. The drop in force represents the failure of the device and the complete shear of the solder joint.

It is observed that the lifetime of the devices before the complete shearing of the solder joints without the compliant interconnects are identical to the complete shearing of the device with the compliant interconnect.

Even though figure 5-10 and 5-11 have an almost identical lifetime, approximately 1000 cycles under the same cycling conditions, the mechanism of failure for the device with the compliant structures was not shearing of the solder balls entirely but shearing of the beam structures from the copper post illustrated in figure 5-9 below.

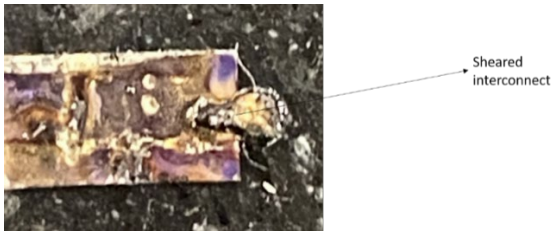


Figure 5-9: Mechanism of failure of the compliant interconnect

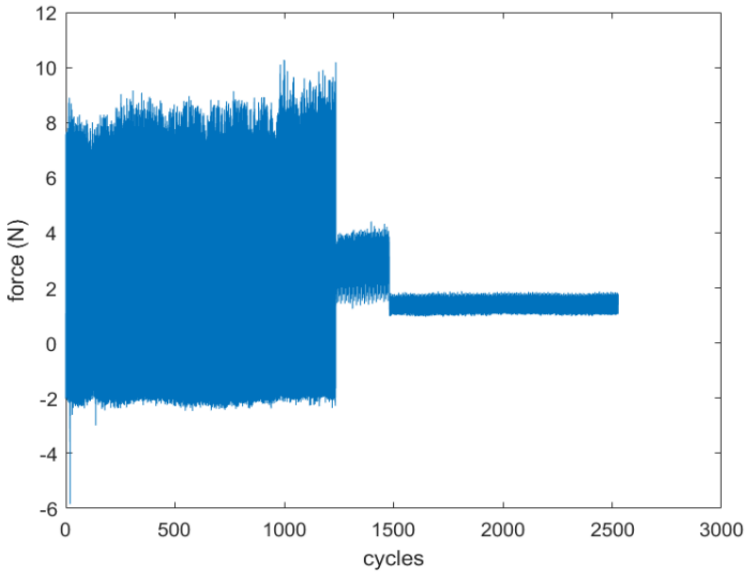


Figure 5-10: Lifetime of test vehicle without compliant interconnects @ 25C

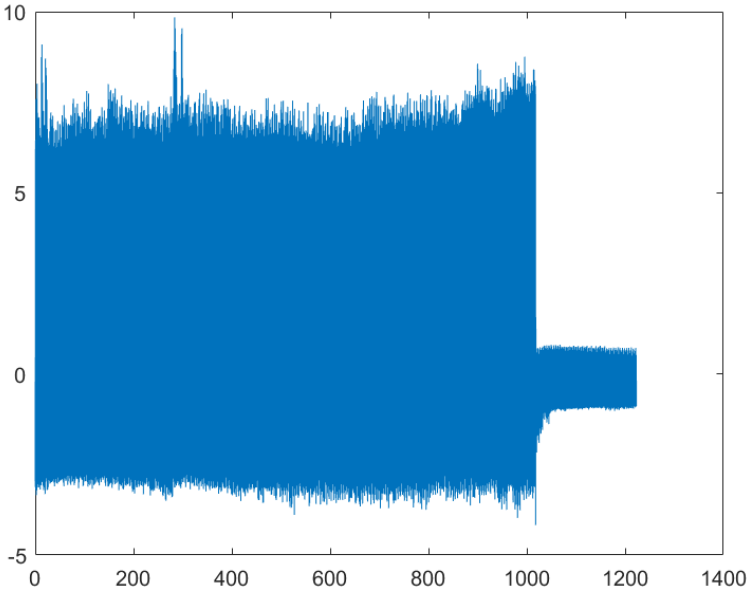


Figure 5-11: Lifetime of test vehicle with compliant interconnects @ 25 C

These results are preliminary and further study to enhance the reliability of these structures will be done by enhancing the integrity of the beam to post connections.

Potential enhancement of these connections may include a chamfer in the copper post to aid copper-to-copper bonding, reducing the surface area of contact between the copper conductive paint seed layer and the copper post, etc. These improvements in the fabrication of these interconnects can aid a more informed conclusion highlighting the direct advantage of these structures in a package. Further thermal-induced tests can also be carried out such as highly accelerated life test (HALT), thermal cycling tests, etc.

6. CONCLUSIONS AND FUTURE WORK

6.1 – Conclusion

A novel additive fabrication method of manufacturing compliant interconnects for electronics integration and assembly is developed, described, and characterized. This method of fabrication presents numerous advantages in encouraging the application of compliant interconnects by presenting a reduction in fabrication steps, increasing fabrication throughput, and presenting fabrication opportunities for complex interconnect designs consequently improving the overall reliability of power devices. A parametric study has been done on the fabricated structures with geometrical dimensions varied to understand their effects on the compliance and mechanical stiffness of the structures. It is observed that increasing the length (L) or subtended angle (α), center radius (R) will improve the vertical compliance and reduce the mechanical stiffness of the structures. Contrarily, increasing the width (w) or thickness (t) of the beam will decrease both lateral and vertical compliance and increase the mechanical stiffness. This study of compliance and mechanical stiffness can directly impact the lifetime of the solder interconnects and a careful design should be selected for this cantilever geometry beam that maximizes the lifetime of the solder interconnects. The additive fabricated interconnects present a great opportunity in electronic reliability interconnects eliminating industrial throughput concerns. Significant improvements were observed at the first level interconnect with the fabricated compliant structures causing an approximate 115% improvement in solder joint fatigue life from 621 – 1336 propagation cycles to failure when thermal cycling is simulated between -40^{o} C to 125^{o} C. The data from the experimental study also provides and highlights compliant interconnects contribution to mechanical shear with a less rapid change in resistance values under high-

temperature mechanical loading, fairly constant resistance over time when compared without the compliant interconnects, positive slope with increasing cycles.

Furthermore, additive manufacturing is a fast-emerging area in engineering and presents a remarkable opportunity in the electronics industry. Advances in 3D printing technologies present in resolution, in material printability for stereolithography printers and additive manufacturing, will most definitely improve the manufacturability of various micro components. The present AM CI approach may be improved at the copper post level with the help of a laser drill to drill smaller diameter holes which may further reduce the inductance parasitic effects of the package.

6.1.1 Major Research Findings

This work has developed a novel additive based compliant interconnect that presents a solution to some of the problems plaguing the integration of compliant interconnects into device packaging, majorly improving on already existing fabrication methods like photolithography. This method will improve yield for microelectronics fabrication and eliminate issues like multiple mask alignment.

- The developed interconnect has vertical compliance ranging between 265.95μm/N and 656.78 μm/N
- The compliant interconnects provide optimum stress distribution across the package reducing stress concentration on the solder joints.
- The compliant interconnects utilize the use of liquid photoresist to create solder pads to enable flip-chip applications.
- This work encourages the direct fabrication of compliant interconnects directly on the printed circuit boards reducing the processing of wafers and dies (electroplating)
- This work also illustrates a potential pathway for semiconductor device assembly

- The reliability enhancing capabilities of these interconnects have been simulated and experimental work has been done to the same effects to validate the real-life impact on a device, simulation, and modeling predicting a 100% increase in fatigue life.
- The developed interconnects can be done in a lab and may not include the use of cleanroom facilities, therefore reducing costs.
- The proposed interconnects do not require an underfill material for mechanical support, eliminating a probable mechanism of failure.

6.2 – Future Work

- This work presents sets of experimental data validated by some mathematical and computational analysis. An experimental study of the reliability effects has been done to demonstrate real-life impact through a shear test. Thermal cycling tests and the electrical measurement capability test needs to be done to understand the electrical impact on a working die.
- Sputtering of the path with a seed layer instead of copper conductive paint can improve the cleanliness of the process and accuracy of the beam dimensions.
- Vibration and drop-impact characteristics of the compliant interconnect study can be studied for more reliable characterization.
- This work is currently based on a first level interconnects development and further study for application and integration for second-level interconnect can be done.
- A more extensive electrical characterization study of the copper interconnects is recommended and other metal integration studies such as electromigration will be important to study.

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APPENDIX

Appendix A

Mechanical compliance testing procedure

1. Install sample in the clamp of the microhardness tester with the aid of the sample clamp wheel.

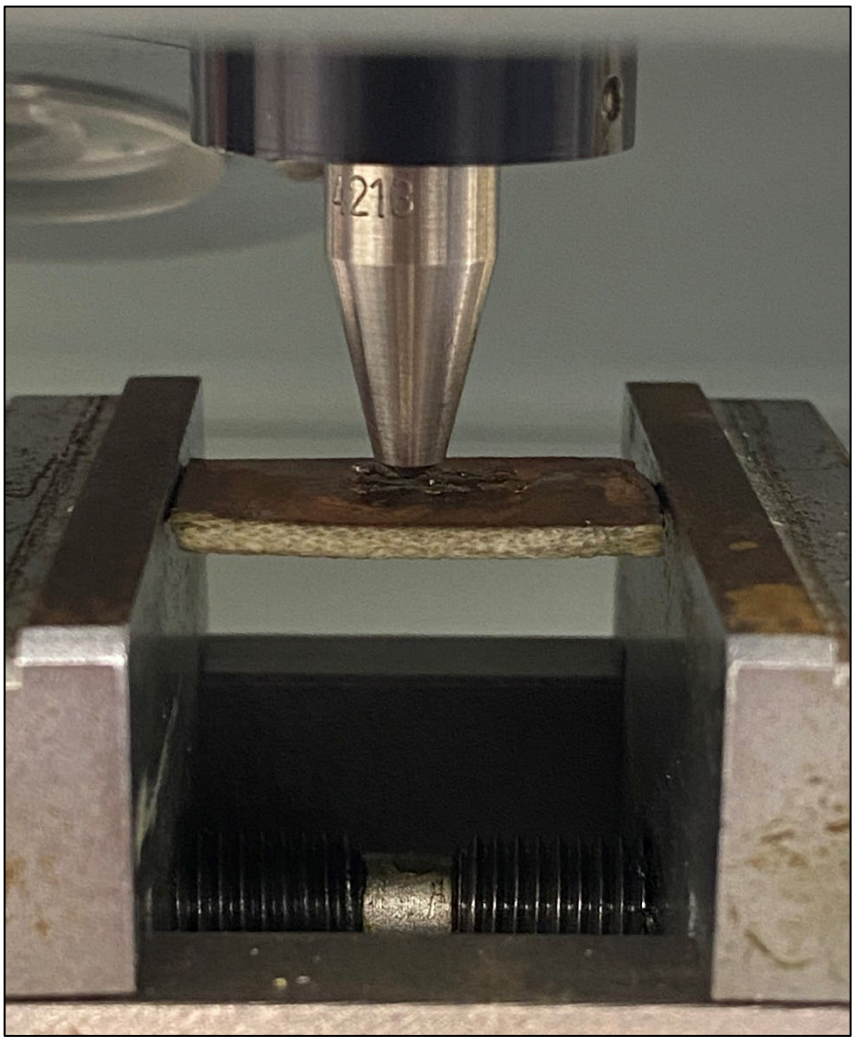

Figure A-1: Sample positioned in clamp for beam deflection measurements

2. Place loading mass in the mass loading area before calibrating the focus of the tester, this will enable accurate initial displacement for load application.

Figure A-2: Load placement area in microhardness tester

3. Use the crank wheel on the side to align the focus of the sample on the load indenter.
4. The AMscope optical microscope is positioned in front of the set up to enable visual display and motion of the cantilever beam during load application and deflection. The optical microscope is set for lighting and focus, a color temperature between 4000 and 6000, and a tint value between 500 and 650 is recommended/preferred as this reduces the reflection of light and gives a clear display of the samples.

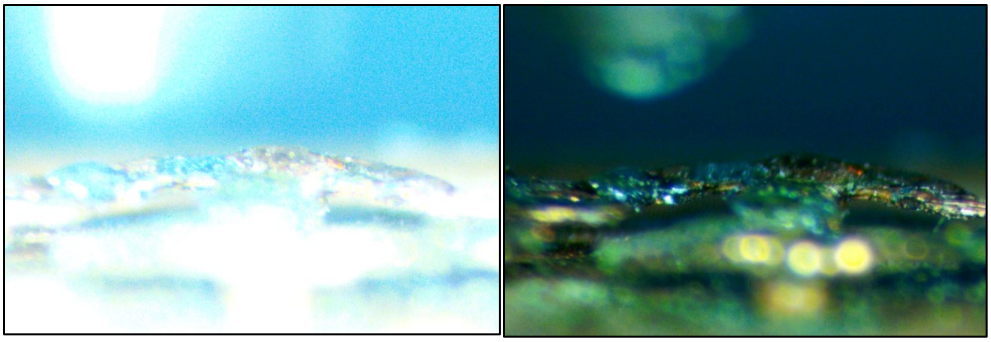

Figure A-3: Optical imagery of beams during load application (a) unclear image (b) clear image

Now that the sample is aligned, the mechanical deflection and compliance tests are started using the start button. The force is gradually applied to the sample and the deflection is measured using the measurement tool from the AMscope application.

5. Use a screen snipping tool to capture Jpeg images of the samples for reference

Appendix B

Interconnect PCB design for in situ reliability resistance testing

To closely observe cracks and reliability challenges, an in-situ lifetime approach is utilized. The testing methodology involves the use of a resistance changing approach to measure the change in electrical resistance of the samples throughout the mechanical cycles.

This test vehicle (PCB) was designed on the PCB design software, Allegro with a seed layer for interconnecting additive fabrication and copper electrodeposition. Copper pads were added to the design to enable electroplating and used as the anode in the fabrication process. Probes for electrical resistance testing were also added.

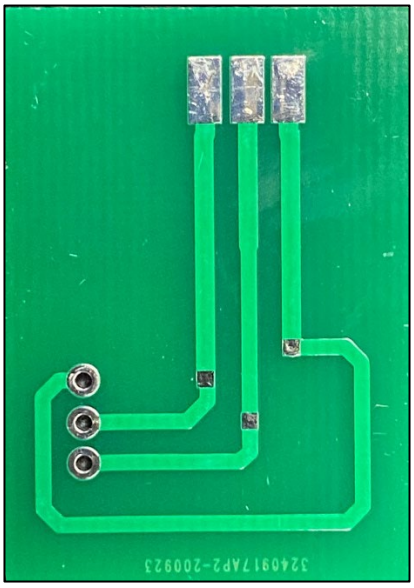

Figure B-1: Picture of designed and fabricated PCB for in situ resistance testing

The fabrication of the PCB was contracted to an external manufacturer for manufacturing.

The fabrication approach of the interconnects is the additive fabrication approach previously described in chapter 3 of this work.

Appendix C

Test vehicle wafer fabrication

A 4'' copper coated silicon wafer was used in the fabrication of the dummy die. The dummy die dimensions were adopted from CREE Silicon Carbide SiC MOSFET imitating a planar design where all source-drain and gates pad are on the same face of the wafer.

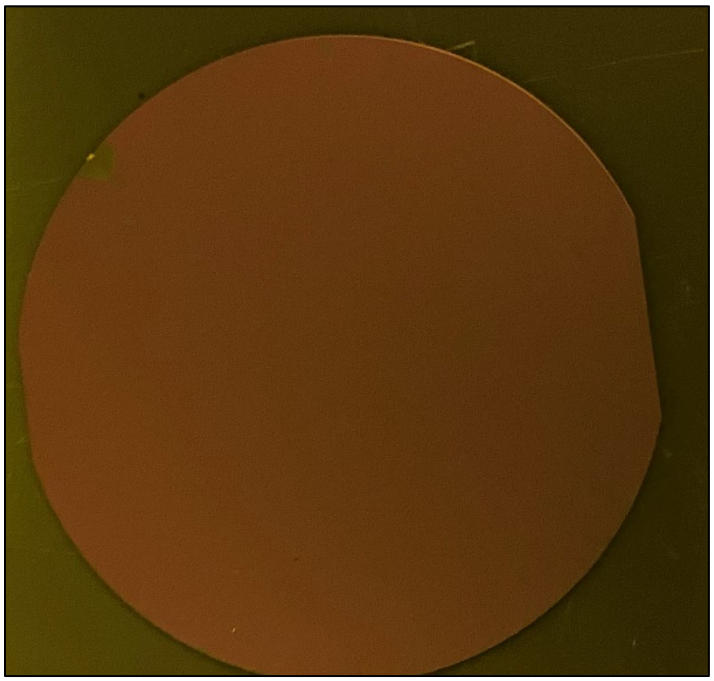

Figure C-1: Image of plane 4" silicon wafer before processing

A solder mask was used to pattern the wafer to enable openings for flip-chip bonding. The patterning was done using a dry film photoresist, and the photoresist was exposed to ultraviolet light was using a microcircuit engineering corp. exposure system. The wafer was then diced with an automated dicing saw from an external vendor.

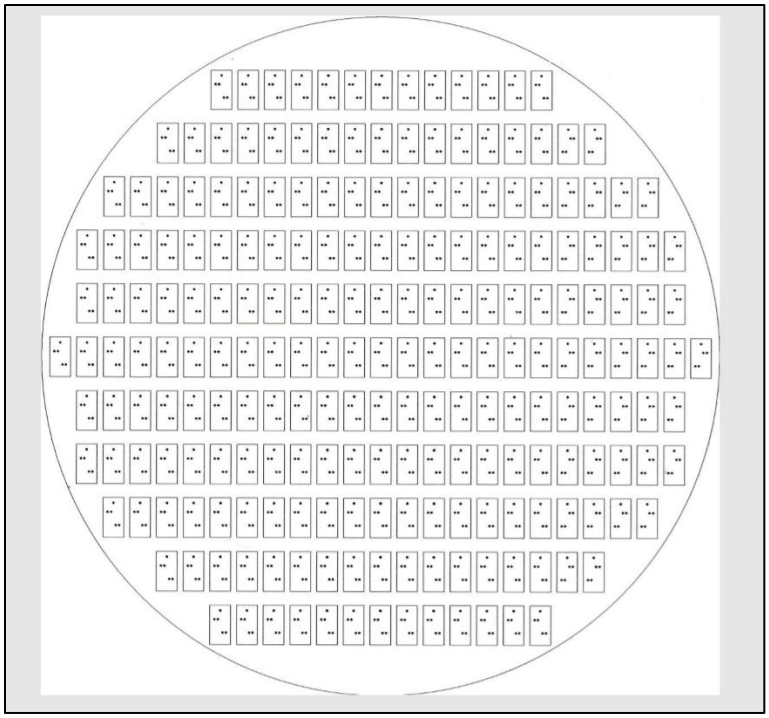

Figure C-2: Image of the solder ball design on a photomask

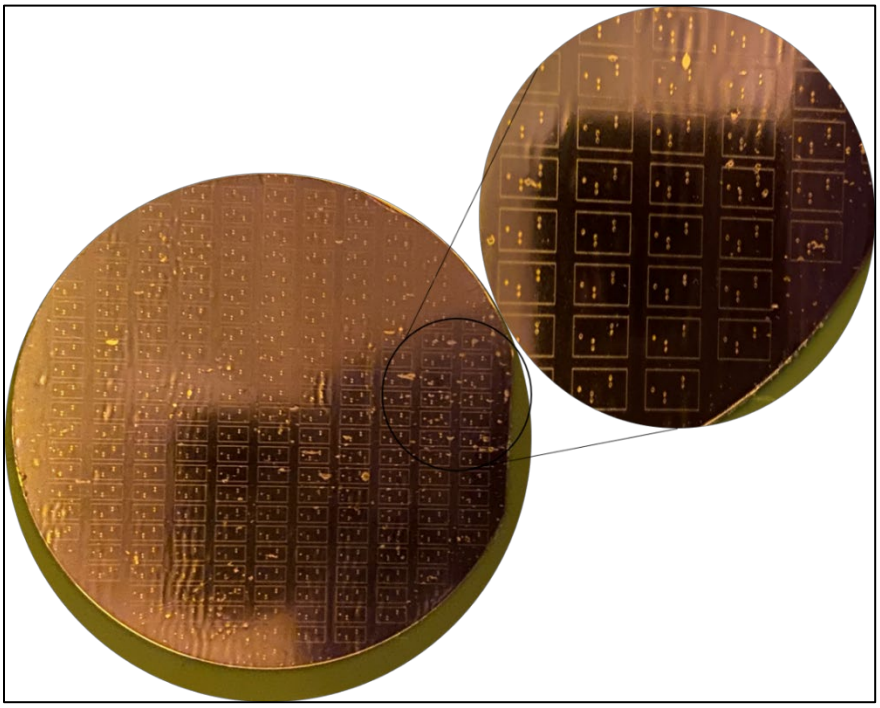

Figure C-3: Image of an exposed dry film on a silicon wafer

The dies are then prepared for assembly on the *in-situ* resistance PCB. The assembly was done using a manual method and passed through a reflow oven, Sikama 5C reflow oven.

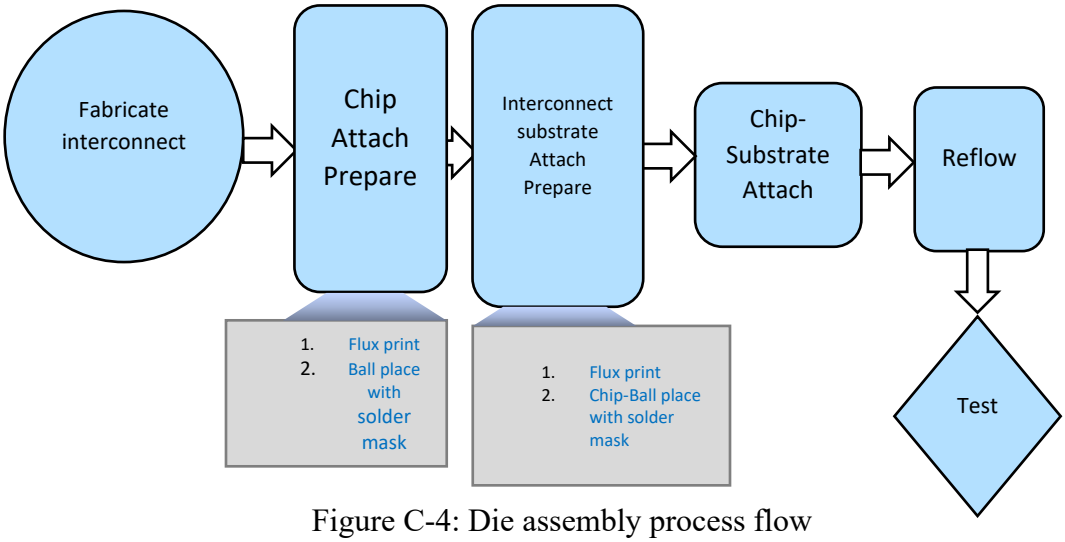

Figure C-4: Die assembly process flow

Appendix D

Tribometer in situ resistance testing procedure

Sample loading

1. 3D print sample carrier plate to hold a sample in place to enable stationary and fixed support.
2. Install sample into 3D printed plate and place plate into tribometer base plate acting as the bottom stage of the test.
3. Start force plotting on the Nanovea software by disabling coefficient of friction plotting from the view tab drop bar. Use the help button > diagnostic to enable stage motor motion controller and select manual control to move the stage to the center to set the zero point of the stage for bidirectional motion.
4. Lower the arm down until the upper cap assembly aligns perfectly with the die by also sliding the carrier base plate on the stage for perfect alignment. Depending on the type of test, the thermocouples may or may not be installed to monitor the temperature.
5. Zero the loading cell in the software and select the New Test tab. Set the input parameters like frequency and time of the test
6. Perform a calibration test with a 3D printed representation of the test vehicle before testing a device. This will help in determining the start and initial force. Start the calibration test and record the peak force in both directions (positive and negative), the force is used calculate the spring constant and this is done before and after testing to observe any change in spring force degradation

Device testing

7. Install the carrier base plate with the device on the stage and connect the wire leads to the resistance probe on your device. Connect the other parts of the leads to the breadboard and take note of the initial starting resistance of the connection.
8. Repeat steps 3 – 6
9. Start the oven for a high-temperature life test and let the device temperature reach a steady-state and allow airflow to the tribometer using the air compressor to ensure proper cooling of the bearings.
10. Before starting the test, enable data recording of resistance, temperature, and force simultaneously. Note the peak force at the start of the test to compare with the peak force during calibration and confirm force data is consistent with 3D printed set up.
11. Monitor resistance during testing and observe for resistance spike changes at least 30% of initial resistance and stop the test and allow to cool (If Highly accelerated test).
12. Save resistance, temperature, and force data in .csv files. Decouple the test set up, raise the arm, and remove the testing sample.

Appendix E

Fixture dimensions and machining

1. The dimensions (inches) of the fixture are presented below and are manufactured in aluminum.
2. The structural design is done to reduce the volume of the structure to account for the thermal expansion of Aluminum illustrated by the skeletal design of the fixture.
3. The structure is machined using a CNC tool.

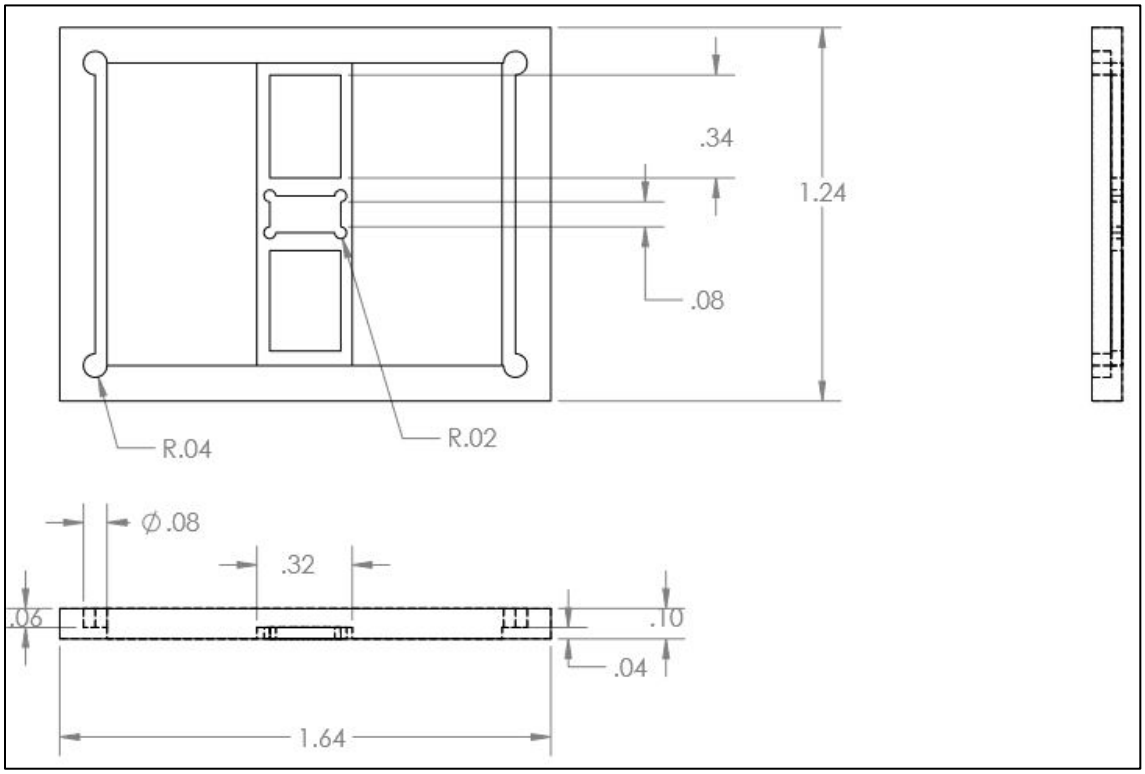

Figure E-1: Plan and elevation drawings with dimensions for the mechanical fixture