7-2020

Design and Optimization of Multichip GaN Module Enabling Improved Switching Performance

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Design and Optimization of Multichip GaN Module Enabling Improved Switching Performance

A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Science in Electrical Engineering

by

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Chittagong University of Engineering & Technology
Bachelor of Science in Electrical & Electronics Engineering, 2015

July 2020
University of Arkansas

This thesis is approved for recommendation to the Graduate Council

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Abstract

Wide bandgap semiconductors (SiC & GaN) due to their enhanced performance and superior material properties compared to traditional silicon power devices have become the ultimate choice for future high-performance power electronics energy conversion. GaN high electron mobility transistor (HEMT) offers very fast switching capability enabling the designer to push switching frequency to the MHz range. Traditional device packaging becomes a limiting factor in fully harnessing the benefits offered by these advanced power devices, and thus, improved and advanced packaging structures are a must to bridge the gap between GaN devices and their applications. A co-design, co-optimization method has been followed to develop two gate driver integrated GaN half-bridge phase leg power modules with optimized power loop inductance, improved thermal performance, and lesser EMI noise emission. The first design or baseline design is compliant with the commercially available easy 1B package and have a single-sided cooling feature. In the second or advanced design, a new design has been proposed with similar loop inductance but double-sided cooling feature and better EMI performance.

Moreover, to address the near field coupling issue in a high-density electronics system and to map the emission, an automated near field test setup using a six-axis robotic arm has been developed with very small step size and repeatability producing the desired map with refined resolution. An easy to use MATLAB based modeling approach has been proposed and validated using the ANSYS MAXWELL simulation and near field test.

Dedication

This work is dedicated to my parents Md. Ilias Shah and Hosne Ara Begum for supporting me throughout my life physically and spiritually. I am also thankful to my loving wife Fatema Tuz Zohara for constantly supporting me in this precious journey.

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1 Introduction

1.1 Overview of GaN and Comparison with Si & SiC

With the advent of Wide-band gap semiconductor devices, high-speed efficient power conversion is no longer a vision but reality [1-4]. Several materials have been tested to replace silicon in semiconductor industries, among them silicon carbide (SiC) and Gallium nitride (GaN) have superseded other candidates with their superior material property and relevance to the application [5-6]. Theoretically, GaN has an even higher figure of merit compared to SiC. The factors which are the basis of this comparison are: 1. Band Gap 2. Critical Electric Field 3. On state Resistance 4. Electron Mobility 5. Saturation Velocity and 6. Thermal Conductivity [7]

Bandgap refers to the energy difference between the valance band and conduction band. It is a yardstick to measure how strong the chemical bonds are between atoms inside the semiconductor lattice. Higher bandgap energy results in lower leakage current and higher thermal conductivity of the semiconductor.

A stronger chemical bond or higher bandgap also ensures a higher critical electric field to initiate impact ionization which causes avalanche breakdown. In brief, a higher critical electric field will enable the semiconductor to block higher voltage over smaller length or thickness. This property comes up with the opportunity to make smaller drift regions in semiconductor devices as low as 10 times compared to Si for SiC and GaN, as such, achieving lower on-state resistance.

Due to the unique device property of lateral GaN HEMT (High electron mobility transistor), the carrier mobility is very high compared to its Si and SiC counterparts. As explained earlier, due to the higher bandgap, the Critical electric field now superior electron mobility, very small on-state resistance is achievable for the same size of the semiconductor die in GaN [8].

$$R_{on} = \frac{4BV^2}{\varepsilon_s \mu_n E_c^3} \qquad (1)$$

As there is an advantage of having a smaller die size for the same voltage and current rating compared to Si, there is smaller input and output capacitance. So the device can be switched very fast. Due to fast switching speed, new applications such as bridgeless totem pool and so on can be realized using GaN. Even at hard switching applications, due to faster transition, switching loss can be minimized. So the cooling requirement can be relaxed.

In terms of thermal conductivity, Si and SiC have superiority over GaN. But most commercially available GaN HEMT's are now grown on a silicon substrate and by doing this, we can leverage the higher thermal conductivity of Si. In table 1, all these properties of GaN are juxtaposed with Si and SiC. Afterward, a spider chart has been drawn to show the figure of merit (FOM) graphically. The area dictates the overall performance of the device and the larger the area is, the better the devices are.

Table 1.1 Properties of Semiconductor Materials

Properties	Si	SiC	GaN
Band Gap, E_g (eV)	1.12	3.26	3.44
Critical Field, E_{Crit} (MV/cm)	0.30	2.00	3.80
Electron Mobility, μ_n (cm^2/V-s)	1400	950	1500
Saturated Electron velocity, v_{sat} ($\times 10^7$ cm/s)	1.00	2.00	2.50
Thermal Conductivity, λ (W/cm-K)	1.50	4.90	1.30

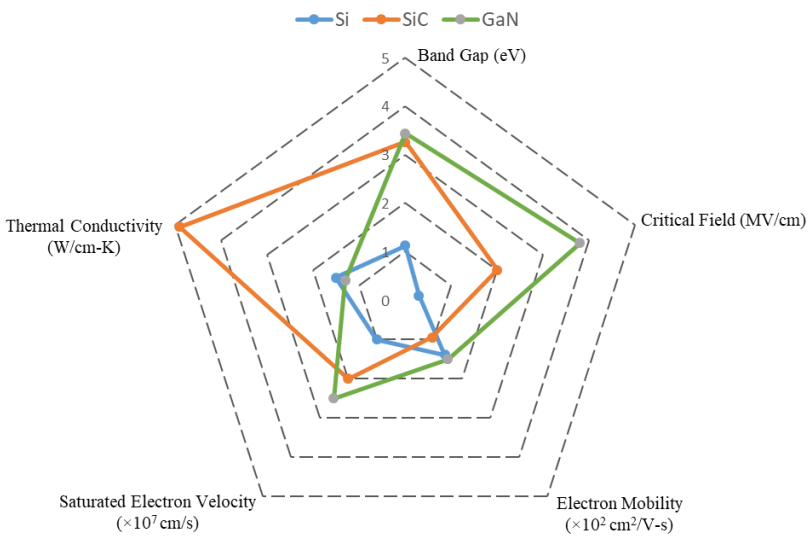
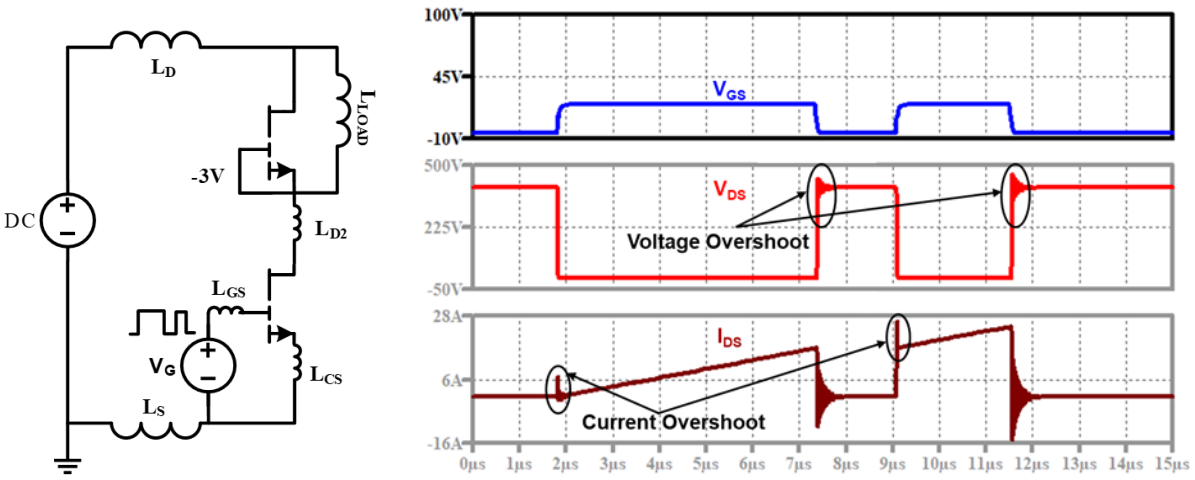


Fig. 1.1: Performance Matrix of WBG Devices

1.2 Impact of Switching Performance

Successful demonstration of any power stage relies on the efficient and robust switching performance of the transistors. Transistor level packaging of the bare die as well as the packaging of module or design of power loop has its significance in determining the matrix of switching performance. When a transistor switches or changes its state, current commutates and during this transient period. During this commutation process, due to inductances introduced by the package, several non-idealities happen which can be easily explained by a half-bridge phase-leg with clamped inductive load [9]. For the sake of explanation, during this test set up, the top device remains always turned off and its body diode is functioning as a free-wheeling diode.

When there is no switching action, the bottom device is blocking the bus voltage and the top device is shorted through the inductive load. At that period, the output capacitance of the bottom device is charged. When the bottom device turns on, the current will start to rise through its channel and the free-wheeling diode starts blocking the voltage.



a) DPT Schematic b) Switching Waveform

Fig. 1.2: DPT Schematic and Waveform

As soon as the diode starts blocking the voltage, its junction capacitor needs to get charged. This charging current gets added to the channel current of DUT. Due to that, we see a current spike in the channel current of MOSFET at the beginning of the switching action as shown in Fig. 1.2. The current will rise linearly through the channel of DUT. After a while when DUT will be turned off, the current will commutate from the DUT to the diode. During this transient, there will be additionally added voltage spike on top of the bus voltage. This spike is due to the commutation loop inductance and the change of current through the device and the peak of spike will be equal to:

$$V_{spike} = L_{stray}\frac{di}{dt} \qquad (2)$$

When the DUT is turning off, its output capacitance starts charging, and there will be a resonance between this capacitance and stray inductance of the commutation loop. This resonance frequency is often used to determine the loop inductance as the frequency can be related to L_{stray} using the equation:

$$f_{resonance} = \frac{1}{2\pi\sqrt{(L_{stray}C_{oss})}} \qquad (3)$$

Due to this stray inductance, the designer becomes constrained with switching speed (di/dt), otherwise, the voltage spike added to the bus voltage can exceed the maximum voltage blocking capability of the device leading to the damage of the transistor. This stray inductance can be controlled during packaging so the switching speed can be pushed to a higher value which will eventually decrease the overlapping area between voltage and current as such, reducing switching loss[10-15]. If the switching loss can be optimized, the power stage can be switched with higher frequency thus decreasing the filter requirement at the output stage. With lesser passives, the overall power density can be increased while reducing the volume and weight [16-20]. Again, now with the advantage, the designer is getting with the increased bandwidth of setting switching frequency, certain EMI standards can be easily met.

There are another two associated inductances named gate loop inductance (L_{GS}) and common source inductance (L_{CS}) which also has their effect on the switching performance. The gate loop inductance causes gate loop oscillation and can be easily controlled by calculating the necessary gate resistance value to damp this oscillation. It has been seen that the gate loop inductance does not have any direct impact on switching loss, but there is still a trade-off. If the gate oscillation is high, the higher gate resistance value will be required which in turn will slow down the device resulting in higher switching loss [21].

Common source inductance is the inductance that is seen by both gate and power loop. This inductance has a critical impact on device performance. When current flows through the channel of the device, there will be a certain voltage drop across the common source inductance depending on the gradient of the current. This acts as a local battery and reduces the effective gate voltage applied across the device gate. Hence the current available to be drawn by the device will be

smaller and the device won't be able to switch fast. This will result in higher switching loss [22-23]. Hence for the successful demonstration of any power stage, all these layout effects are needed to be considered. Half-bridge phase legs are building block of these converters and without the optimization of parasitics in its layout, the performance of the entire system will be affected.

1.3 Application of GaN Module:

Power electronics modules have been widely used to build the power conversion stage for the electric vehicle, more electric aircraft, motor drives, onboard charging, oil and gas, renewable energy, industry platform electrification, and so on [24]. Most of the power modules available in the market are mostly of Si IGBTs or SiC MOSFETs. Due to the theoretical constraint of these devices switching speed, many soft switching topologies such as bridgeless totem pole were not possible to realize using a silicon-based transistor. Cooling complexity introduces another layer of cost in traditional Si and SiC-based power module. The $R_{ds(on)}$ of GaN devices are much lower than Si and SiC due to higher electron mobility which will aid in lowering conduction loss substantially. Due to the physical property of channel (2D electron Gas), the absence of body diode is there in third quadrant operation so loss due to reverse recovery of charge is also can be diminished. Meanwhile, from the packaging point of view, the cost of an additional Schottky barrier diode is saved.

In the automotive application, the entire system can be divided into two-stage: 1. High power module and 2. Low and medium power modules. For driving the main motor a DC-DC boost stage is followed by an inverter stage. High power modules are used in this stage. For medium to low power applications such as in air conditioner and other utilities low to medium power modules are used. GaN-based module can be implemented for both of the stages [25].

For more electrification of future aircraft, power modules are being used for efficient power conversion. But at certain altitudes and lower temperatures, GaN has shown a better performance matrix compared to Si and SiC. With lowering the temperature, GaN's on state resistance decrease, breakdown voltage stays fairly constant, the gate threshold voltage ($V_{GS(Threshold)}$) increases linearly, and turn on speed increases [26-29].

Radiation in space is generated by many sources that come in the form of gamma rays, energetic electrons, protons, and heavier ions, which causes damage in semiconductors. GaN transistors have been tested under heavy ion bombardment and gamma irradiation. These devices demonstrate unparalleled performances in the most stringent of radiation environments and far exceed the capabilities of silicon power MOSFETs. The problem that engineers face with silicon MOSFETs is that they must choose between radiation tolerance and electrical performance. Commercial MOSFETs have thick gate oxides trapping a lot of charges, resulting in large shifts in the threshold voltage and eventual failure at relatively low total-dose exposure. In terms of the figure of merit (FOM), the radiation-hardened MOSFETs are several times worse than their commercial counterparts, leading to either low efficiency or large size (due to the low switching frequency). Enhancement-mode GaN transistors give designers a new capability with electrical performance superior to the cutting-edge Si MOSFETs, and radiation tolerance. So, GaN transistors come with a combination of electrical and radiation performance establishing a new state of the art [30-33].

1.4 Importance of EMI and Noise Immunity:

Electromagnetic interferences (EMI) is an inevitable part of the switch-mode power conversion system. The system itself can become either a source of EMI or a victim from the EMI generated in the nearby source. So electromagnetic compatibility and susceptibility are a must

check at the time of designing a power electronics system [34-40]. EMI noise can be conducted through the traces and cables of the system and get coupled to the different components. This type of EMI is called conducted EMI. EMI noise can also get coupled through radiation which does not require any physical connection of traces and cables between the source and victim. This type of EMI is named as Radiated EMI [41].

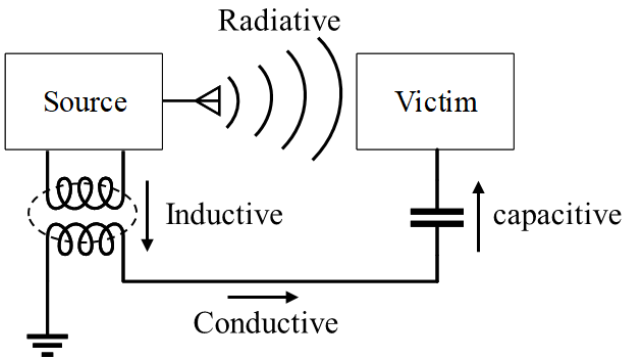


Fig. 1.3 Different methods of noise coupling

There are certain EMI standards specific to the country and application. Before commercialization, these standards must be met. The most traditional way of passing the standards and reducing the EMI is either through the implementation of a filter or applying shield. These solutions come with a price of cost, volume, and weight. In any particular system, 30% of space is occupied by EMI filters. None of these solutions kill the source but confine the noise close to its source. To reduce the overall emission or killing the EMI at its source, EMI aware design practice needs to be followed [42].

Again, for driving the transistor efficiently, numerous gate driving solution is there. To isolate the power stage and signal stage, an isolated gate driver solution is popular among designers. But due to the presence of small parasitic capacitance between the primary side and

secondary side of the isolator, in high dv/dt environment, there can be noise coupling and signal integrity will be violated which leads to spurious behavior during operation.

Depending on the distance from the source, the zone of Radiated EMI can be classified as near field and far-field. The most recent trend of power module packaging is to integrate the gate driver IC along with the power stage compactly. Radiated near field coupling has proven to be a bottleneck of such design space. This near field coupling can either be from the near electric field or magnetic field coupling. So, in a brief, to have a remedy against these problems, modeling the noise network and developing an understanding is a must [44].

Electromagnetic interference generates due to switching actions and associated parasitics of the system. A half-bridge topology has redrawn incorporating all the parasitics in Fig. 1.4

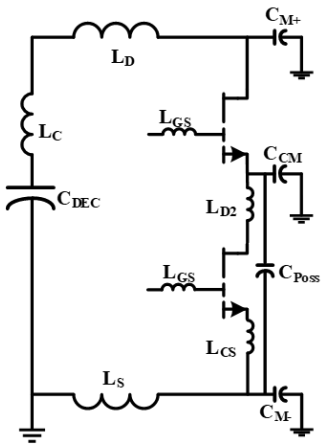


Fig. 1.4 Half-bridge topology with associated parasitics

Here L_C is the ESL of the decoupling capacitor. L_D, L_{D2}, $L_{CS,}$ and L_S are the power loop inductances. When device commutation is happening, the output capacitance resonates with all these inductance. Hence there will be a resonance peak at that particular frequency and DM noise coupling will increase due to that. C_{DEC} works majorly as a decoupling capacitance. The secondary

advantage of this capacitance is, it acts as x capacitor of the EMI filter and reduces DM noise. The effectiveness of filtering largely depends on the L_C (ESL) as it influences the insertion gain of the filter. Here L_{CS} is the common source inductance which will be present in both power and gate loop and deteriorate the switching performance. C_{CM} is the stray capacitance from the switching node to the ground while C_{M+} and C_{M-} is the stray capacitance between the ground and DC+ and DC- node. C_{CM} will induce the leakage current to the ground if it has a voltage gradient (dv/dt) across it which will give rise to the common-mode noise. On the contrary, C_{M+} and C_{M-} acts as C_y capacitor of the EMI filter which will constrain noise inside the module. So the larger value of these two capacitances is desirable. C_{Poss} is the stray inductance that comes in parallel to the device which will increase the output capacitance of the device. It will slow down the device and increase the switching loss. So lower C_{Poss} value is desirable.

1.5 The outline of the dissertation:

In the 1st chapter introduction to the wide band-gap devices, their superiority over traditional Si device, switching behavior of power MOSFET in hard switching topology, factors affecting switching performance of the device, and why module packaging is important to overcome the shortcomings due to package parasitics are explained.

In the 2nd chapter, a detailed review has been presented to understand the evolution of GaN technology over time along with the survey of recently available packages for discreet devices as well as available power module packaging techniques for GaN.

In the 3rd and 4th chapter, two half-bridge phase leg GaN module has been presented and detailed packaging philosophy and architecture of these packages have been discussed.

In the 5th chapter, a modeling technique for near field coupling is presented. To support that work, an automated near field scanner has been developed and magnetic near field of a planar module is scanned and modeled. Finally, the conclusion is drawn with a discussion of possible future exploration space.

2 Literature Review

2.1 Timeline of GaN

Though GaN HEMT first came into existence by Eudyna Corporation of Japan in 2004 as a depletion mode transistor for RF application, the HEMT structure phenomenon was observed and explained by T. Mimura et al. [44] and M.A. Khan et al. [45] in 1975 and 1994 respectively. T. Mimura et al. and M.A Khan et al. have found very high electron mobility described as 2-dimensional electron gas (2DEG) in the interface of AlGaN-GaN heterostructure. Later on, in 2005, Nitronex corporation 1st announced its GaN HEMT on Silicon for RF application. The next breakthrough came in 2009 when Efficient Power Conversion (EPC) came with the first enhancement-mode GaN devices. After that, Transphorm, Infineon, MicroGaN, GaN Systems, Fujitsu, Panasonic, International Rectifier, ExaGaN, VisIC, GaN Power International, Texas Instrument and many other companies have shown their intention to fill up space and started introducing their devices for a variety of application [46]. Most of the commercially available GaN devices are rated up to 650V and most of them are lateral devices. HRL has stepped on to make vertical GaN and demonstrated a strong effort to improve there especially with 1200V devices. In the meantime in 2018, GaN Power International brought 1st commercially available 1200V lateral GaN HEMTS. They have different discrete packages for different on-state resistance as such, current rating. Another major focus is given to monolithically integrating gate drivers with transistor die naming as GaN IC. GaN Power International, Navitas, Dialog Semiconductors, Texas Instruments, and EPC has announced their own GaN IC for different voltage and current ratings.

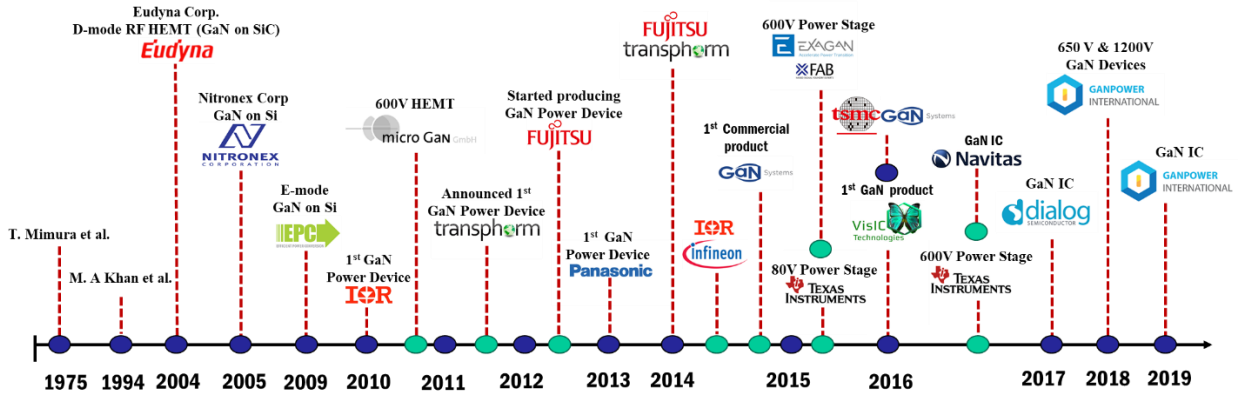


Fig. 2.1 Timeline of GaN innovation

2.2 Classification of GaN Devices

As seen from the list provided in the last section, many companies have already declared and sold their devices commercially while many others are about to announce their devices. All the devices that are now existing in the market can be classified into the following fashion:

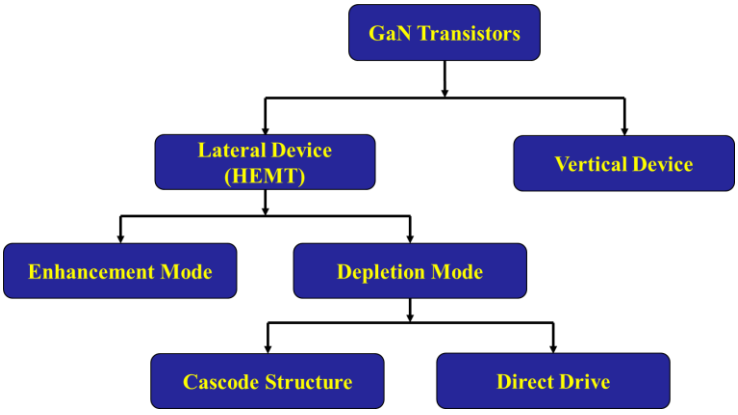


Fig. 2.2 Classification of available GaN devices

In this section, a brief introduction of GaN HEMT will be given mainly focusing on lateral GaN HEMT. Most of the commercially available devices are lateral GaN HEMT's as the vertical devices are yet to be commercialized. The terminology HEMT stands for high electron mobility transistor and this high electron mobility is achieved by the heterojunction structure. The principal

feature of lateral GaN devices is AlGaN-GaN heterojunction. The device is grown on Si or SiC substrate for their availability and mature technology as well as to take advantage of their higher thermal conductivity. This substrate is followed by a buffer layer and a GaN layer. On top of the GaN layer, a layer of AlGaN is formed. At the interface of the AlGaN-GaN layer due to the crystal polarity which is augmented by piezoelectric crystal strain induced by lattice mismatch of AlGaN-GaN, a very thin sheet of electrons are formed which is called 2D electron gas or 2DEG. This 2DEG works as a channel between the drain and the source of the transistor. As the channel is already formed due to the structure of the transistor, all lateral GaN HEMT's are inherently depletion mode or "normally on" device [47].

But from a design engineer's point of view, normally on devices are difficult to work with because of potential shoot-through events and loss of control, normally-off or enhancement mode devices are desirable [48]. So, to use the depletion mode devices as a normally-off device without changing device structure, cascode and direct drive configurations are there. In both cases, the GaN HEMT is connected in series with a low voltage enhancement mode device, especially Si MOSFET. For cascode devices, the gate of GaN HEMT is connected to the source of the low voltage MOSFET and the output voltage of Si MOSFET (Drain-Source) determines the input (Gate-Source) voltage of GaN HEMT. Low voltage MOSFET is driven in cascode structure where designers have the flexibility to choose a gate driver solution from a vast number of commercially available reference designs. The cascode configuration comes with a problem of potential avalanche breakdown of low voltage MOSFET due to C_{oss} imbalance between the series-connected device. It also has a limitation in terms of switching speed and higher reverse recovery loss. The direct-drive configuration solves this problem. Here low voltage MOSFET is always on and GaN

HEMT is directly driven by a negative voltage bias referenced to the ground which switches the combined device [49].

Instead of adding one more low voltage MOSFET to control the device, the device structure itself can be modified to shift threshold voltage positively hence making an enhancement mode device. Several techniques are adopted by companies to deplete the 2DEG channel beneath the gate when no voltage is applied. The channel can be reconstructed by applying a voltage greater than the threshold. The majorly known techniques are P doped GaN layer, P doped AlGaN layer, Recessed gate, CF_4 plasma treatment, Insulated Recessed gate, and so on [50].

2.3 Available GaN Devices in Market

Before going into the survey of the reported GaN power module, it is similarly important to shed light on the market scenario to see what are the available device options we have. Several choices are readily available varied by driving techniques, voltage and current rating, package outline, on-state resistance, and gate charge requirement. In the following table, comprehensive lists of available GaN power devices are presented with their characteristics matrix. A FOM (figure of merit) is also calculated for listed devices which will help users to choose among different options.

Table 2. 1: Available GaN Devices in Market

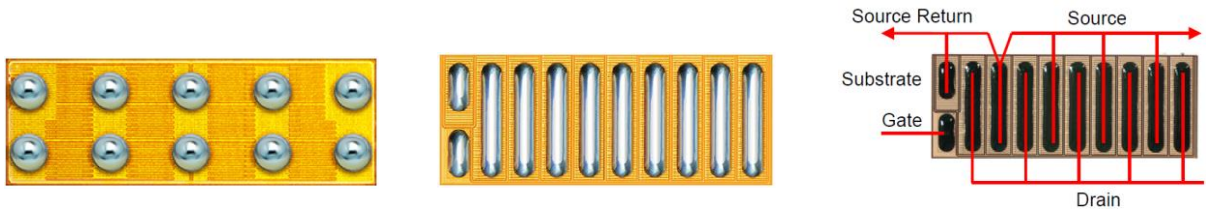
Voltage, V	Manufacturer	Current Rating, I	$R_{DS(on)}$, mΩ	Gate Charge Q_g, nC	FOM (R_{DS}*Q_g)	Driving Mode	Package
15	EPC	3.4	30	0.745	22.35	Normally off (E-Mode)	LGA
30		90	1.45	19	27.55		
40			1.5	18	27		
60			2.2	16	35.2		
80			2.2	15	33		
100			3.2	13.2	42.24		
	GaN Systems	38	16	3.3	52.8		GaNPx
		90	7	8	56		
200	EPC	48	8	11.4	91.2		LGA
500	Fujitso		100	14	1400	Cascode (D-Mode)	TO 220
600	Panasonic	26	70	5	350	Normally off (E-Mode)	DFN
	MicroGaN		320	Unknown	Unknown	Cascode (D-Mode)	TO 263
	Infineo CoolGaN	31	70	5.2	364	Normally off (E-Mode)	PG-DSO-20
	Sanken		50	Unknown	Unknown	Normally off (E-Mode)	Unknown
	TI	34	50	Unknown	Unknown	Direct Drive (D-Mode)	QFN
650	GaN Systems	30	50	6.1	305	Normally off (E-Mode)	GaNPX
		60	25	14.2	355		
		80	18	16	288		Die (E-Mode)
		150	10	33	330		
	Transphorm	47	35	24	840	Cascode (D-Mode)	TO 247
	ExaGaN	75	30	Unknown	Unknown	Normally off (E-Mode)	PQFN8x8
	VisIC	80	18	41	738	Cascode (D-Mode)	Customized SMT
	Navitas	24	180	Unknown	Unknown	Normally off (E-Mode)	QFN
	IGaNPower	60	25	16	400		TO 263
		30	50	5.5	275		TO 220
		30	55	5.8	319		DFN
1200	IGaNPower	15	95	4.15	394.25		TO 252
		30	65	8.25	536.25		TO 264
	ExaGaN	100	Unknown	Unknown	Unknown		Unknown

2.4 GaN Module Survey

To process the already manufactured die for specific applications so that maximum utilization of its capacity is ensured, further fabrication steps need to be taken. Power modules are the results of these steps. After the GaN dies become available, designers from industry and academia have already reported multiple application-oriented packaging endeavors. The reported GaN packaging efforts so far broadly fall under two categories: 1. Chip level packaging for devices and, 2. Module-level packaging for designing power stages.

2.5 Advanced Chip Level Packages for GaN Device

Packaging of GaN transistors bare die is done commercially by many manufacturers. In 2000, ball grid array (BGA) technology was introduced by Fairchild Semiconductor [51]. BGA eliminates the bonding wires and lead frames by applying solder bumps. It reduces the package's resistance and enhances heat transfer. These bumps can also enlarge the total contact area between the package and the printed circuit board (PCB) and reduce the length between the die pads. Available products of EPC was initially based on Ball grid array (BGA) and later on adopted Line grid array (LGA) technology [52].



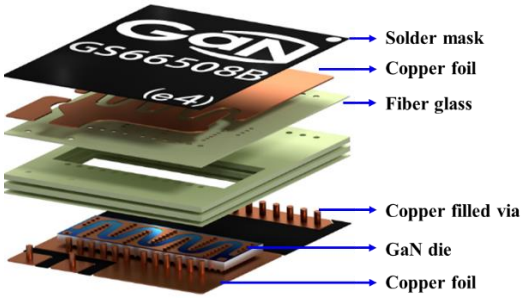
a) BGA solder bumps on EPC GaN b) LGA solder bumps on EPC GaN c) Intertwined current path on LGA

Fig. 2.3 BGA and LGA technology on GaN

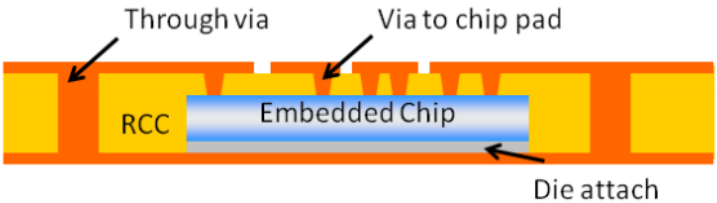
Fraunhofer IZM and TU Berlin worked together and came up with Chip in polymer package [53-55] to switch currents of 80 A or more. This technology embeds power chips into low profile

polymer package without using the DBC substrate. The chip is soldered by its drain contact to Cu foil. GaN Systems have introduced their island technology fused with the Chip-in-Polymer concept to reduce device level parasitics and increased current handling capacity. The concept of mutual cancellation of the magnetic field in adjacent traces with the opposite direction of current flow is implemented in this technology. GaN Systems has patented the GaNPx package for the near chip-scale version of their device enabling high thermal performance and low package inductance as well as resistance. The bare die is sandwiched in between two copper foils along with high-temperature fiberglass. Then patterning on the copper foil is done for accessing gate, drain and source potentials. Copper filled laser cut vias are drilled for making interconnection of patterned copper foil to the die. In the last step, solder masks and marking is done which provides further electrical insulations to the device [56].

a) Cross section of GaNPX package



b) Exploded view of GaNPX package

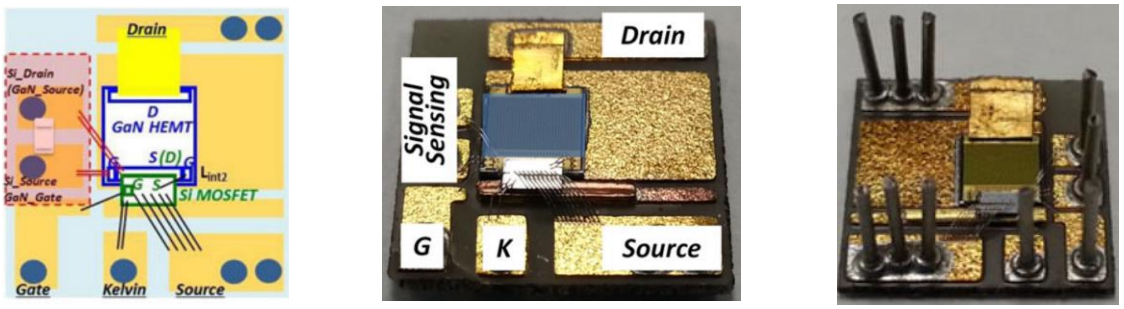


c) Chip in polymer concept

Fig. 2.4 GaN Systems GaNPX package

CPES has presented a package using a metal connection and stack-die structure for 650 V Cascode GaN devices and packaged it in a quad flat no-lead (PQFN) compatible format. Here,

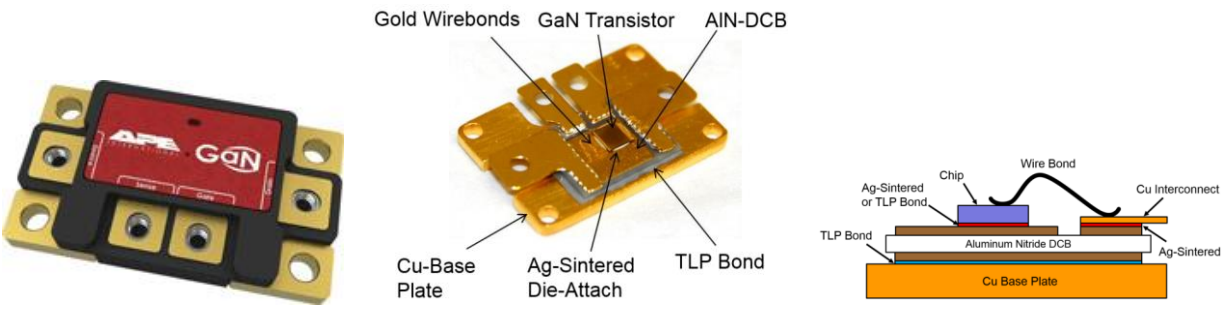
GaN Chip is attached to AlN substrate, and drain connection is done to the substrate through a copper plate. For cascade structure, required low voltage Si MOSFET is directly soldered onto the GaN HEMT and the copper space on the gate terminal. This design optimizes gate-loop and power loop inductances and reduces switching loss by 16% [57].



a) Outline of module b) Stacked die configuration c) Internal view of module

Fig. 2.5 Stack-die structure for Cascode GaN

With collaboration with GaN Systems, APEI (Now wolf speed) has developed a high temperature high current package. Inside this discrete package (named as X'6 power discrete package by APEI), for GaN chip attachment transient liquid phase (TLP) bonding was done to attach the die to the AlN DCB substrate while gold wire bonding was used for electrical interconnections between the chip and the copper interconnects. AlN DCB is mounted on the base plate using a TLP bond while the copper interconnects are attached to the DCB using Ag sintering process. The package is developed to be operated at 50-100A, 1200V, and 250°C temperature. The thermal resistance of the package is reported as 0.38 °C/Watt while the inductance is 7.83 nH [58].

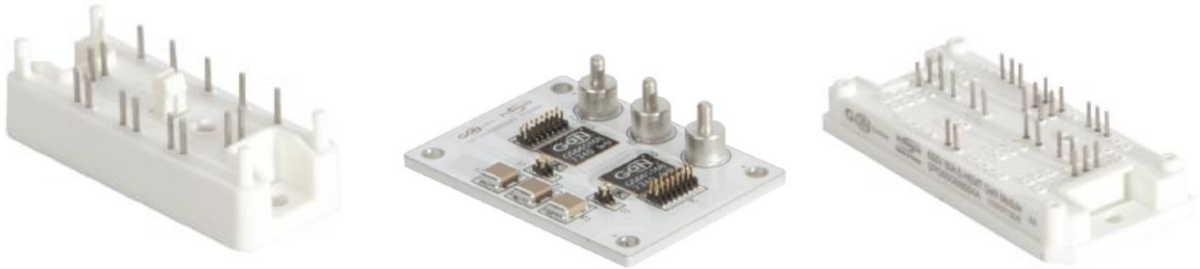


a) Completed module b) Internal view of module c) Cross-section of module

Fig. 2.6 APEI's high-temperature X-6 power discrete package

2.6 GaN Power Module

Semi-Powerex has demonstrated packaging solutions for GaN Systems prepacked devices into a commercially available module outline. They have available 650V full-bridge modules rated for 30A, 60A, and 120A respectively. They have used bottom side cooled GS66516B devices enabling wire bondless interconnection due to the structure of the prepackaged chip which has terminal pads and thermal pads located on the same side. Traditional DBC substrate has been used to in their module with single-sided cooling [59].

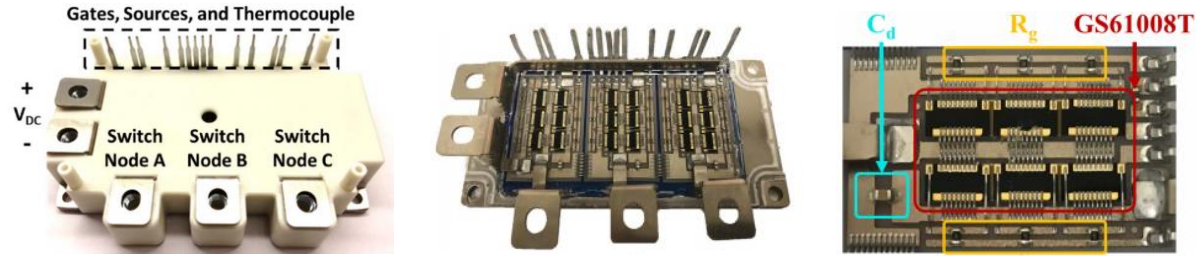


a) 650V/30A Power module b) 650V/60A Power module c) 650V/120A Power module

Fig. 2.7 Semi-Powerex commercially available GaN Module

Another single-sided cooled three-phase GaN power module was reported in the literature. It is based on GaN systems top side cooled prepackaged die (GS61008T) and rated for 100V/ 270A. GaN Systems top side cooled device has terminal pads and thermal pads located on the

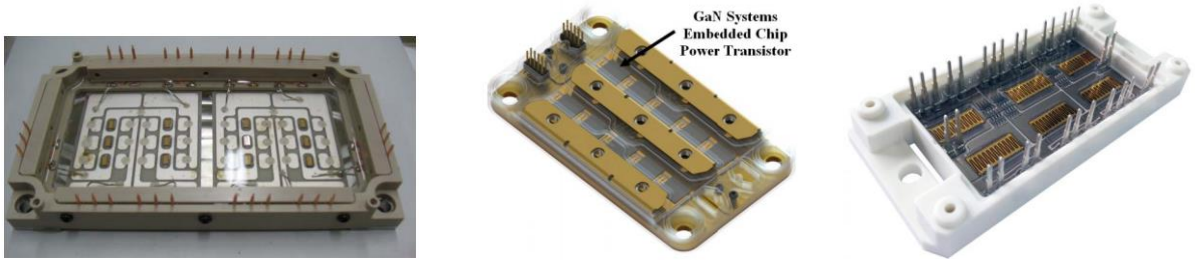
opposite side of the device. The thermal pad of the device is soldered on the DBC and electrical connection is made through aluminum wire-bond from the terminal pads of the device to the respective island of the etched DBC. Surface mount gate resistor and decoupling capacitors have been embedded inside the module by using the reflow soldering process [60].



a) Outline of three-phase GaN module | a) Internal view of the whole module | a) Zoomed view of single-phase

Fig. 2.8 100V/270A three-phase GaN Module

In reference [61], A 200V/45A half-bridge power module has been proposed using lateral GaN HEMT. Each switching position is comprised of three parallel GaN chip, while each chip has six 2.1 A GaN on Si cell. It shows a DBC based single-sided cooled design reporting 0.3252 °C/W thermal resistance.



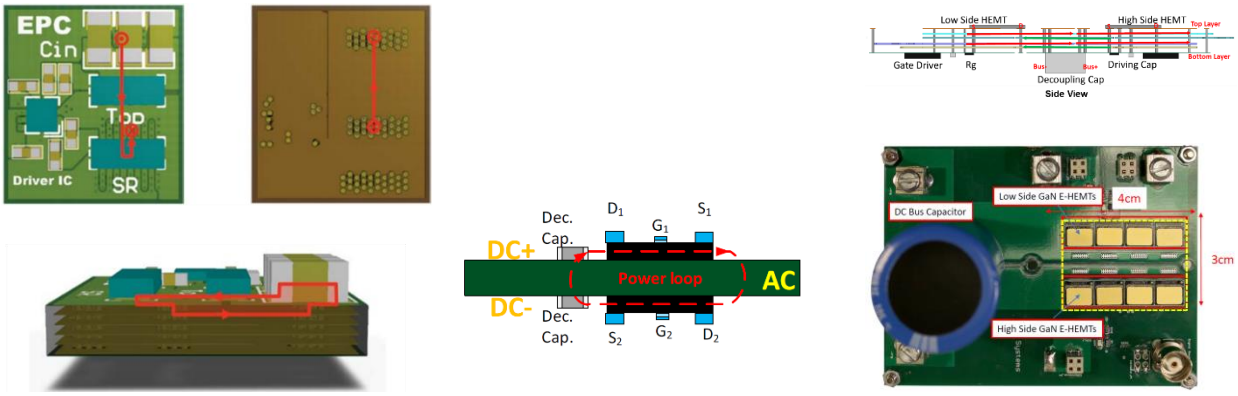
a) 200V/45A GaN module | b) 650V/150A APEI GaN module | c) 650V/150A die in module

Fig. 2.9 GaN power modules in conventional packages

APEI (now Wolfspeed/CREE) had worked with GaN Systems in 2012 to develop packages for high current and high-temperature modules. APEI modified its HT3000 module to build a

650V/150A GaN half-bridge module using GaN Systems 50mΩ device (GS66508P). They have paralleled five devices in each switching position and sintered them on DBC. Gate connection is realized by using wire bonds while the power loop is wire-bond less achieving 5.1 nH loop inductance [62]. GaN Systems has announced their 650V, 150A die which has the highest current rating in a single chip among the available devices in the market so far. They also have demonstrated a design for the reference module using this die which is a traditional DBC based wire-bonded module [63].

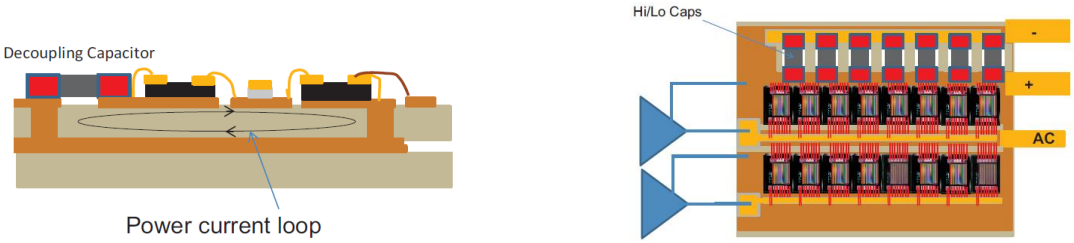
Having multilayer routing options for the power loop helps to reduce the stray inductance by mutual cancellation of the magnetic field, generated by current passing in the opposite direction in adjacent layers [64-66]. EPC has shown a detailed analysis of different routing techniques and suggested an optimized layout option for their LGA patterned chip [67]. J.L. Lu has optimized a layout for Gan Systems top side cooled device GS665108T in a six-layer PCB board [68]. Dushan et. al has also adopted this technique in one of his designs [69].



a) EPC vertical power loop b) Dushan et. Al vertical loop c) J.L. Lu et al. vertical loop

Fig. 2.10 Vertical power loop concepts to reduce power loop inductance

Fang Luo from CPES also demonstrated a 650 V, 15 A multichip GaN phase-leg module using this concept, as illustrated in Fig.2.11, which achieved very low power loop inductance (< 5 nH) for ten paralleled GaN devices [70].



a) Cross-section of multilayer multi-chip GaN Module

b) Top view of multilayer multi-chip GaN Module

Fig. 2.11 Multilayer ceramic GaN module

GaN systems themselves have an insulated metal substrate (IMS) power module where metal core PCB is employed. It gives flexibility to route the power loop with minimum inductance and metalcore features add better thermal performance as well. This design is optimized for GaN Systems bottom side cooled device. It comes with an external customized gate driver board dedicated to this design [71].

EPC has its PCB based half-bridge power module with an integrated gate driver. It features two 100V EPC 2045 e-mode GaN HEMT, attached to the PCB, achieving more than 1400 W/in^3 power density [72].

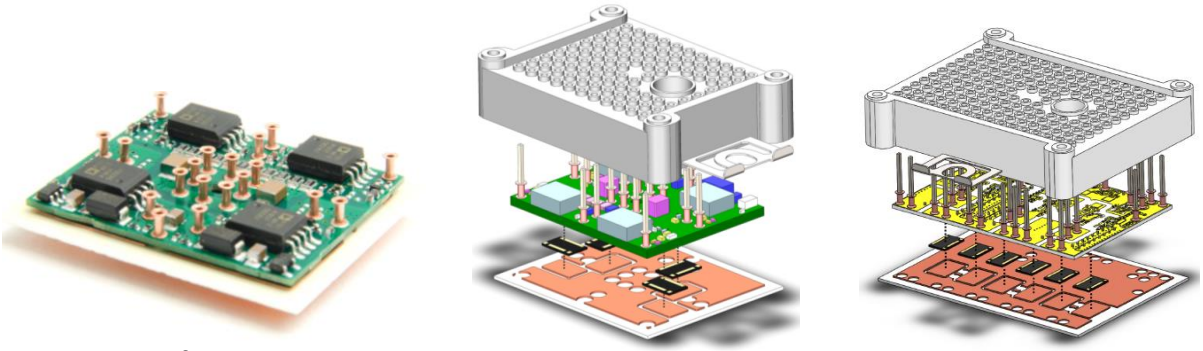
a) IMS GaN Module

b) Asssembled IMS GaN Module

c) EPC GaN Module

Fig. 2.12 IMS PCB based GaN module

A. B. Jørgensen from Aalborg University has shown a hybrid PCB-DBC based package for a full bridge module. This module is compliant with Infineon's commercially available Easy 1B package. GaN Systems GS66508T has been welded on the PCB using vacuum reflow soldering. A commutation loop inductance as low as 2.6nH has been reported. Topside of the die is attached to DBC for extracting heat. For external busing, surface mounted press-fit pins are used. Later a 3 phase voltage source inverter has been built using a similar principle which is compliant with Easy 2B package from Infineon [73-74].



a) Hybrid full-bridge GaN module

b) Exploded view of full-bridge GaN module

c) Exploded view of three-phase GaN module

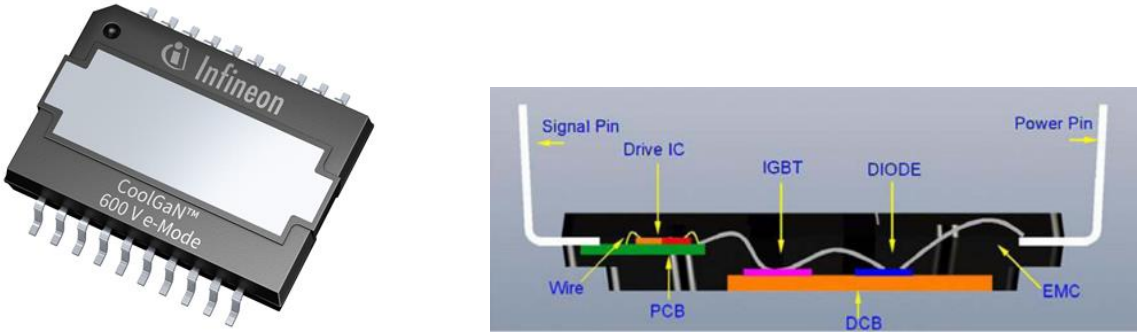
Fig. 2.13 Hybrid PCB/DBC GaN Module

VisIC has become the first company to commercially announce a 1200V GaN power module using its depletion mode device in direct drive configuration. As the highest voltage rated device they have is for 650V, for achieving 1200 V voltage blocking capacity, they have connected two devices in series. According to their datasheet, 40 mΩ on resistance and 80A continuous current carrying capability is achieved. Their package is an extended version of the Easy 1B outline with a 64mm*31mm dimension. A gate driving circuit is also embedded inside the package [75].

a) VisIC 1200V GaN module b) Internal view of VisIC module

Fig. 2.14 VisIC 1200V half-bridge module

Infineon has introduced its transfer molded package for its 600V e-mode CoolGaN series. The outline of these packages is very similar to their CIPOS package for the IGBT based intelligent power module (IPM). Bare dies are welded on top of a DBC substrate while driver IC is housed on a separate PCB. Wirebond is being used as interconnect inside the module and later the whole module with terminal pins is transfer molded together. The exposed surface of the DBC substrate is used for heat spreading as well as heat removal [76-77].



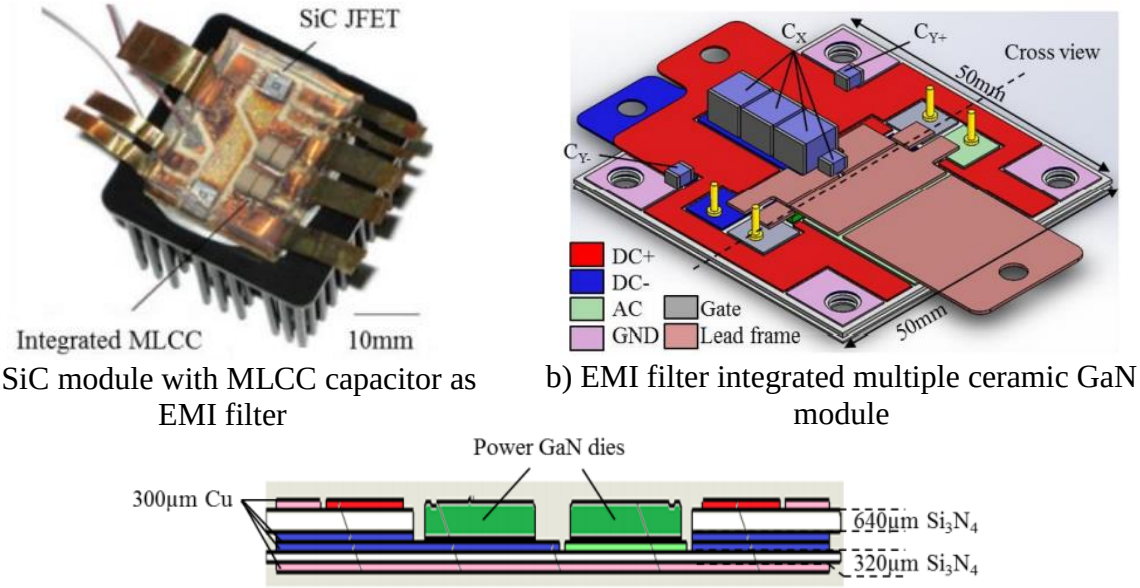
a) Infineon 600V CoolGaN module b) Internal structure of Infineon module

Fig. 2.15 Infineon transfer molded 600V GaN module

EMI is a concern in fast switching highly dense power electronics systems. The same truth goes as well for the power module. Integrating passives inside the module forms local common and differential mode filters and confine the noise inside the module. For filtering the DM noise, the parasitic inductance of the loop needs to be optimized as it resonates with the C_{oss} of the device

and brings DM noise spike. Integrating C_y capacitor for bypassing CM noise is a well-known practice. Remi Robutel et al have shown a SiC JFET module with integrated C_y capacitance [78].

Benoit Thollin et al. has built their GaN HEMT based half-bridge power module incorporating this concept. This module uses two Si3N4 ceramic substrate layers of different thicknesses. GaN HEMT dies designed and manufactured by CEA-LETI are attached to the bottom substrate and embedded in the cavity of the top ceramic layer so that the surface of the GaN chips are in the same height of the top ceramic layer's copper. A lead frame has been employed instead of wire bonding to reduce the interconnect inductance. C_x and C_y capacitance has been incorporated in this design to form a local EMI filter. C_x capacitors are the same as decoupling MLCC capacitors [79].



a) SiC module with MLCC capacitor as EMI filter

b) EMI filter integrated multiple ceramic GaN module

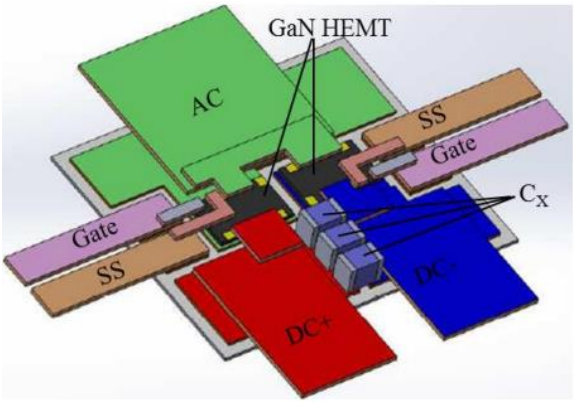
c) Side view of multi-layer ceramic GaN module

Fig. 2.16 EMI filter integrated power module

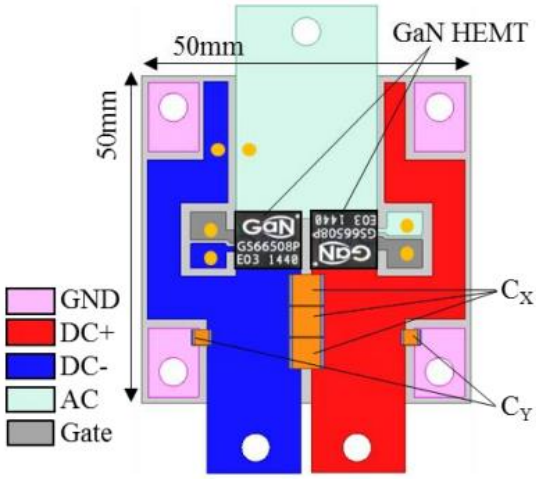
Using GS66516T from GaN systems, another EMI concerned design has been proposed where only one ceramic substrate has been employed. The top-side of the die which is dedicated to heat removal has been welded to the substrate. The interconnection between the substrate and

die has been realized by lead frames. C_{M+} and C_{M-} are balanced in the design so no mode transformation of EMI noise (from CM to DM or vise versa) will take place. No C_Y capacitance has been integrated into this design.

Using GaN systems GS66508P, another module has been built where a two-layer IMS with aluminum substrate has been used for efficient cooling. Devices are directly soldered on the top side of the substrate. It has both C_x and C_y capacitance integrated inside the module for constraining the noise inside the module.



a) EMI filter integrated GaN module using lead-frame



b) EMI filter integrated wire-bondless GaN module

c) Fabricated EMI filter integrated wire-bondless GaN module

Fig. 2.17 EMI filter integrated power module using GaN System chip

Using GaN systems GS66508P, another module has been built where a two-layer IMS board has been used for efficient cooling. Devices are directly soldered on the top side of the substrate. It has both Cx and Cy capacitance integrated inside the module for constraining the noise inside the module [80-81].

The knowledge gathered by surveying the existing package, available device, and their figure of merit, will be utilized in the next chapters where two half-bridge, phase leg GaN module has been developed.

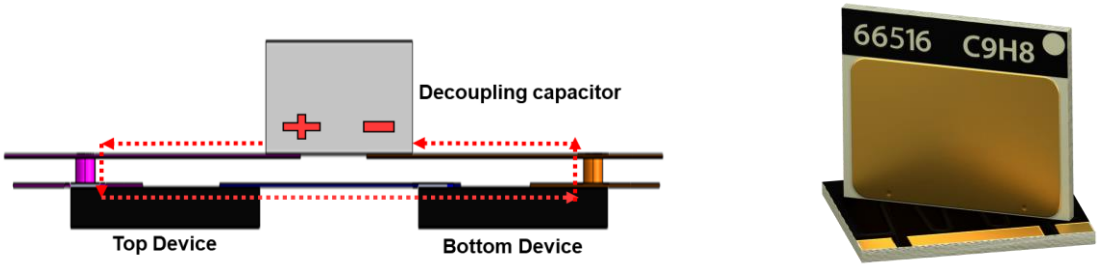
3 A 650V/50A Baseline GaN Module

3.1 Introduction

To develop the fabrication process and for comparison of the performance metrics of an advanced module which will be discussed in the upcoming chapter, a baseline module has been developed. The design procedure was guided by co-design, co-optimization philosophy from electromechanical performance, and reliability standpoint. Gate driver is integrated inside the package and been optimized for successfully driving paralleled GaN HEMT. The whole structure consists of a PCB for power routing as well as gate routing and a DBC for isolation and heat spreading. The design is compliant with commercially available Easy 1B package. Both the power and gate loop inductance has been optimized to 0.68 nH and 1.2 nH and verified using Ansys Q3D which is comparable to the result reported in the literature. As driving GaN with higher power density design comes with a challenge of handling noises from electromagnetic interferences (EMI), the design of gate driver and power routing is done carefully so that the signal fidelity is unharmed. In each switching position of the phase leg, two of GaN Systems prepackaged device (GS66516T) has paralleled to increase the power density in the bottom side of PCB. Isolated gate driver solution with miller clamping functionality for both top and bottom switch has been integrated at the top side of the PCB. Device placement and DBC have been optimized for maximum heat spreading and minimum thermal coupling. Low (70 pF) stray capacitance from switching node to the ground has been achieved by optimizing the DBC pattern to limit common mode EMI emission.

3.2 PCB Layout

As the device used in this module (GS66516T) comes with a dedicated pad on the top side for cooling, patterned DBC has been placed underneath the PCB. For optimization of the power loop, a vertical power routing loop has been achieved in the adjacent layers of a 4 layer PCB.



a) Implemented vertical power loop b) GaN Systems GS66516T chip

Fig. 3.1 Vertical power loop for reducing the stray inductance

As the module under discussion is a compact, high power density and gate driver integrated design, laying out of each layer of PCB was important to avoid any coupling between gate and power loop. Orthogonal gate and power loop to each other is desirable to minimize coupling through magnetic near field [82]. In this design, as the power loop is in the vertical orientation, the gate loop is laid out horizontally. When there is switching action happening during the operation of the module, the switching node will have voltage fluctuation or dv/dt. Any traces carrying logic signal can get contaminated by the noise current through the capacitive coupling from that switching node. So, the overlap of such traces with the switching node has been avoided.

For avoiding the thermal coupling between the GaN HEMT, a parametric sweep has been done to place the devices at the optimum location. From the trend of the result obtained in simulation, a safe margin of 4 mm between adjacent devices has been maintained. For easy

accessibility and flexible busing, input pins are placed on the same side while the output pins are placed on the other side. The layout of the PCB has been shown in Fig. 3.2

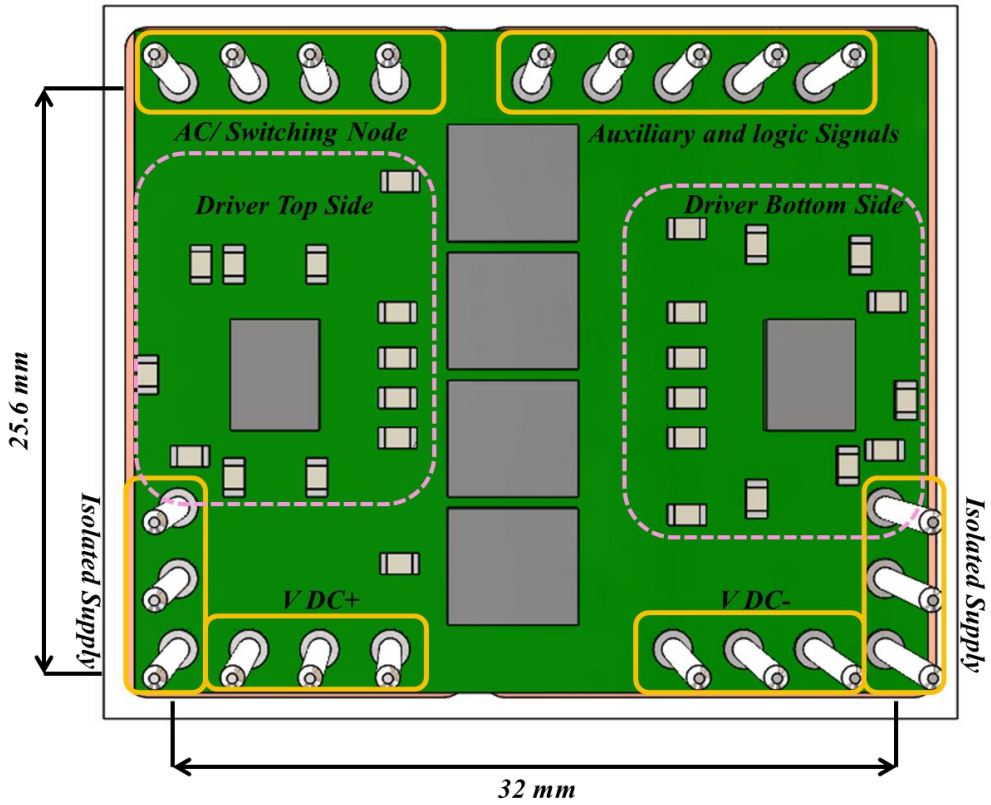


Fig. 3.2 PCB outline

After designing the PCB in Altium designer, its step file has been imported to ANSYS Q3D and its parasitics have been extracted. The lumped inductance of the power loop has been found equal to 0.68 nH. The equivalent circuit with the extracted parasitics of the power loop is shown in Fig. 3.3. The value of the coupling coefficient K_{D12} and K_{S12} is 0.714.

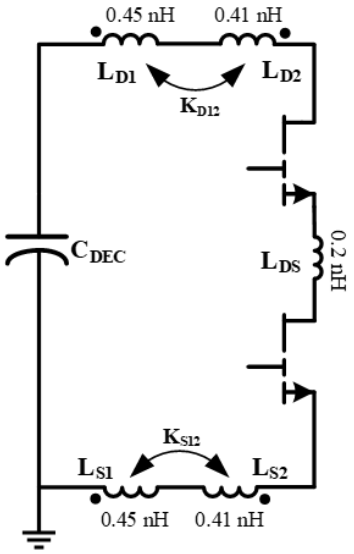


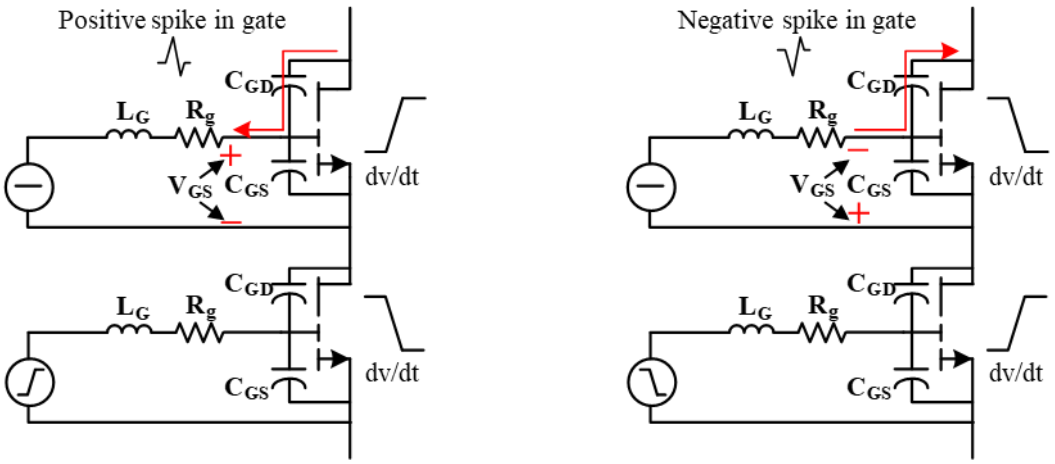
Fig. 3.3 Equivalent schematic of power loop with associated stray inductances

3.3 Gate Driver Design

A separate isolated gate driver solution for top and bottom switching position of half-bridge has been implemented. The isolated DC-DC power supply for powering the secondary side of the gate driver is external to the module. At the time of designing the gate driver for fast switching transistor, several considerations are needed to be accounted. The isolator's common-mode transient immunity (CMTI), withstand voltage per UL 1577, propagation delay and isolation capacitance are the key parameters to look at. For the isolated DC-DC power supply, withstand voltage capacity and isolation capacitance are important [83].

When switching action is happening, the miller capacitance or C_{GD} provides a path for the linkage between the power loop and gate loop and if necessary precaution is not taken shoot through event may occur. This is well known as the cross-talk phenomenon. Topologies that use half-bridge phase leg, transistors switch in a complementary fashion in them. So when the bottom switch is turning on, there will be a positive gradient of dv/dt across the top switch of the half-bridge. This positive dv/dt introduces a displacement current through C_{GD} and it needs to be sinked

in the gate driver IC. Due to this current, voltage drops occur across the gate resistance. If this voltage spike is higher than the threshold voltage of the gate, the transistor can be turned on inducing a shoot-through event. A similar phenomenon occurs during the turn off of the top device. In this case, a negative dv/dt appears across the bottom device so current flows in the opposite direction. This introduces a negative voltage drop across the gate resistor hence inducing a negative voltage spike across the gate. This does not introduce a spurious switching event but can cause a reliability problem for the transistor if this negative spike crosses the safe operating range of gate voltage [84].



a) A positive spike in the top gate b) A negative spike in the top gate

Fig. 3.4 Cross-talk phenomenon

To mitigate this problem gate driver with a small turn off resistance is recommended by taking into consideration that there is a separate gate path for turn on and turn off. Introducing external capacitance parallel to the gate might address this issue but it slows down the device and the advantage of using GaN is lost. Back to back connected TVS diode is another viable solution where the Zener action of diodes will keep the voltage to the set value and reduce the miller induced spikes at the gate. The selection of proper diode is important because if we parallel diode

to the gate with higher junction capacitance, the device will eventually get slowed down. Active miller clamp circuitry is another option where a transistor is connected in parallel to the gate to short it during the event of shoot through, but it comes with a relatively complex control. Moreover, it depends on the measurement of the gate-source voltage, but due to internal gate resistance, the actual measurement will be always less than the voltage appearing across the actual gate-source terminal.

Considering all the above-mentioned methods, a gate driver with a separate source and sink pin from silicon lab (Si8271) has been selected. It comes with a buffer and an isolator inside SOIC 8 package. It provides 2.5kV RMS voltage isolation, 200kV/μs CMTI, and very low primary-secondary stray capacitance (0.5 pF). For powering the secondary side of the gate driver, Isolated DC-DC power supply from RECOM power which comes with 3pF isolation capacitance has been chosen. As two devices have been paralleled in switching positions, a separate gate-source loop has been designed with individual Rg/Rs to reduce gate ringing among parallel devices. To reduce the imbalance in V_{GS} due to quasi common source inductance, the gate loops for parallel devices are kept symmetrical.

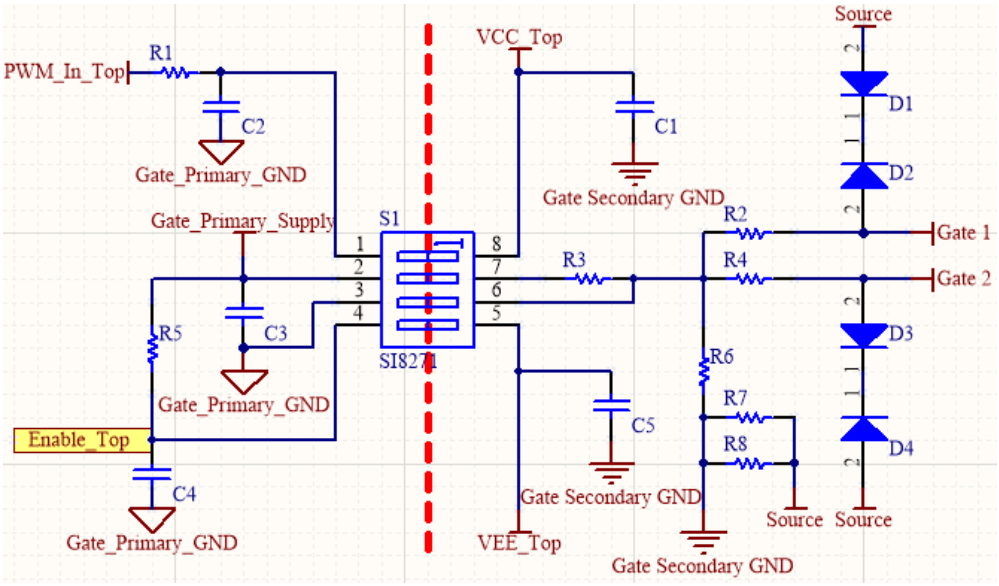
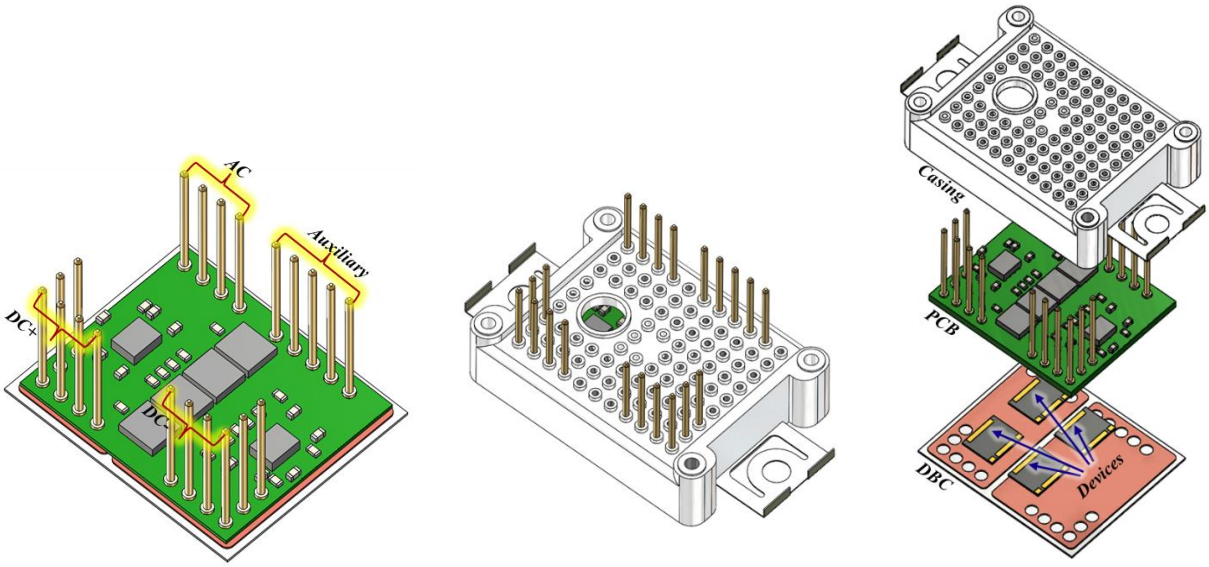


Fig. 3.5 Gate driver schematic for paralleled GaN device

3.4 Module Fabrication

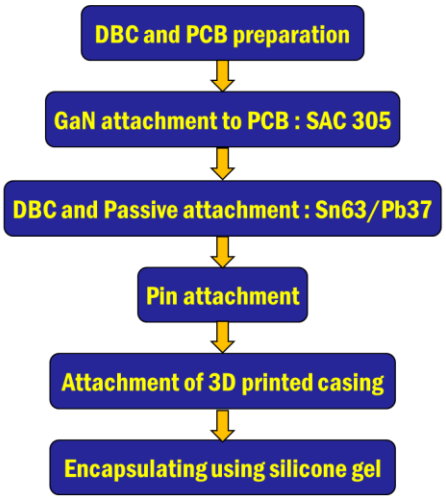
After designing the PCB for the gate and power routing, DBC design has been optimized for electrical isolation and heat spreading. Detailed CAD drawing of the module is shown in Fig. 3.6



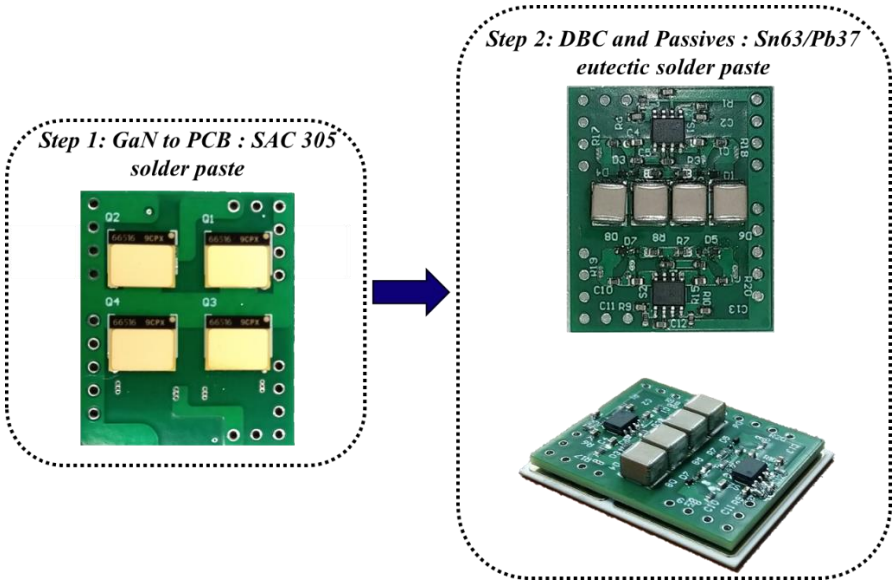
a) Module without casing b) Module with casing c) Exploded view Module

Fig. 3.6 CAD drawing of 650V/50A GaN module

A two-step process flow has been developed to assemble the module. Reflow soldering has been done to attach dies, gate driver chips, and passive components to the PCB and DBC. A graphite fixture has been fabricated to hold the boards during reflow. SAC 305 (220°C melting temperature) and Sn63/Pb37 eutectic solder (183°C melting temperature) pastes were chosen for two separate reflows. The assembly process goes as follows:



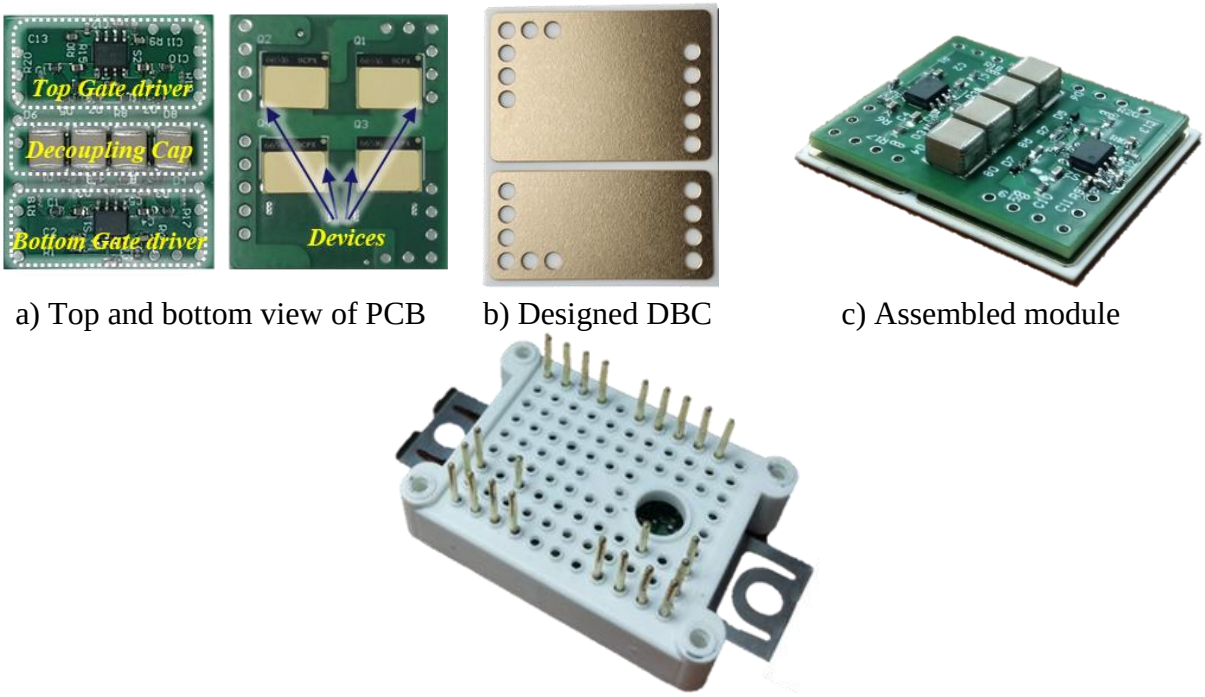
a) Process flow



b) Two steps reflow process to assemble module

Fig. 3.7 Assembly process of GaN module fabrication

After completion of the reflow soldering, connection pins and casing has been attached followed by pouring silicone gel for encapsulation. The entire module after assembly looks like as shown in Fig.3.8



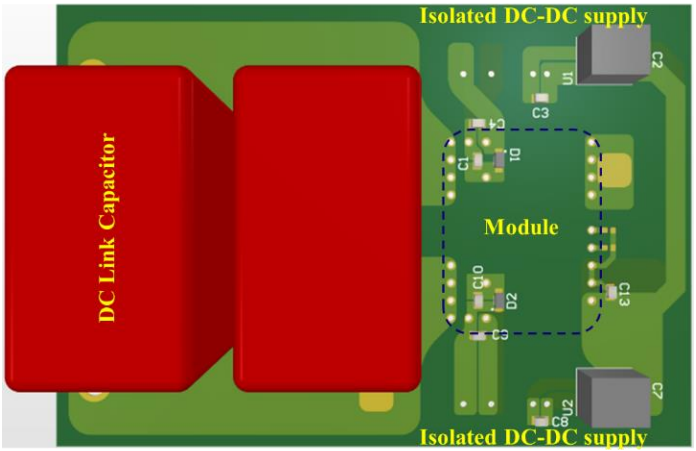
a) Top and bottom view of PCB b) Designed DBC c) Assembled module

d) Fabricated module with housing and pins

Fig. 3.8 Manufactured parts of the module at different stages of fabrication

3.5 Electrical Testing and Thermal Simulation

After finishing the fabrication of the module, a double pulse test has been performed to verify the electrical functionality. To interface the module with the external bus, an interface board has been developed which will also house the isolated DC-DC power supply for biasing the secondary side of the gate driver.



a) Outline of the interface board

b) Assembled interface board with module

Fig. 3.9 Test setup for electrical characterization

The test was performed at 400V/50A with a 131µH air-core inductor to clamp the top device. $R_{g(on)}$ (external turn on gate resistance) is chosen to 10 Ω and $R_{g(off)}$ is set to 1 Ω. In the waveform, only 7.5% overshoot at the turn off transient has been measured. Turn on speed equal to 35V/ns while turn off speed equal to 62V/ns has been recorded.

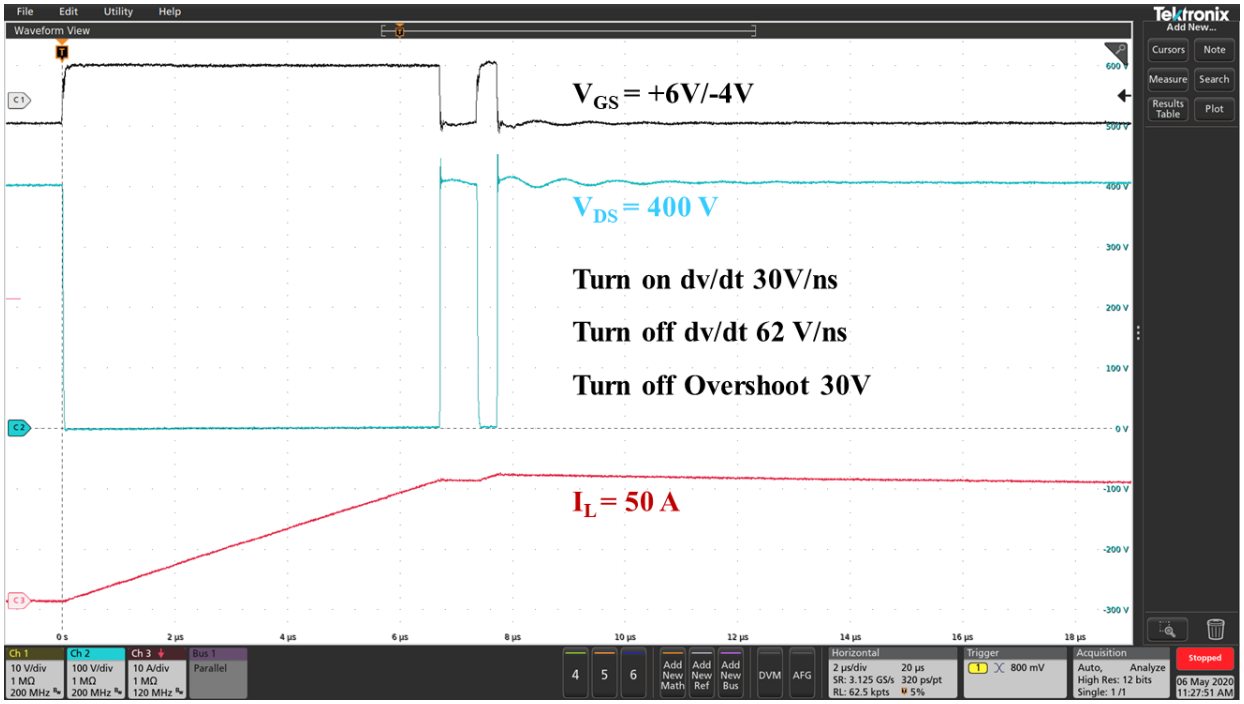


Fig. 3.10 Waveforms from DPT test

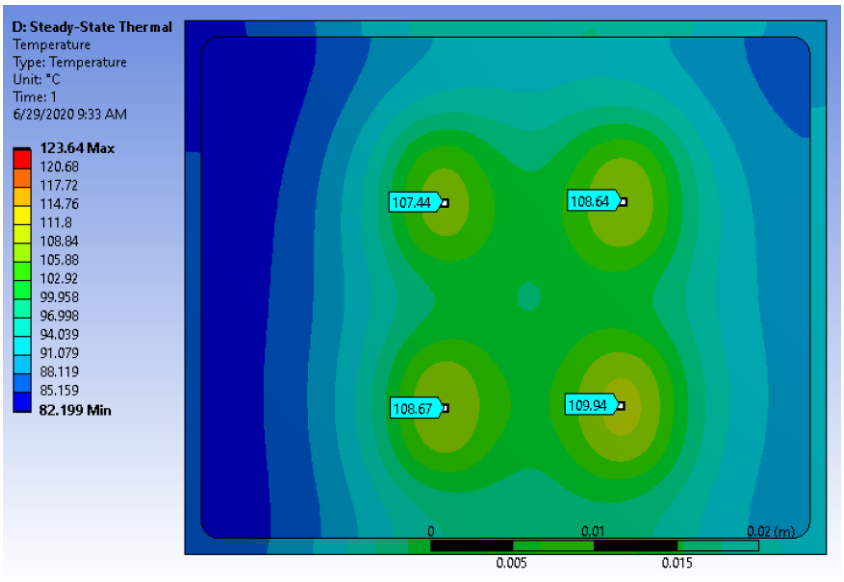
For validation of the thermal performance of the module, a steady-state thermal simulation has been done using ANSYS workbench. A thermal convection coefficient of 5000 W/m^{2}K has been set. Assuming the module is running in buck mode with a duty cycle of 0.5, 50A current and switching frequency of 200 kHz, the total sum of conduction loss and switching loss per die has been calculated to be 35W using equation (4-6).

$$P_{loss} = P_{Sw} + P_{Cond} \qquad (4)$$

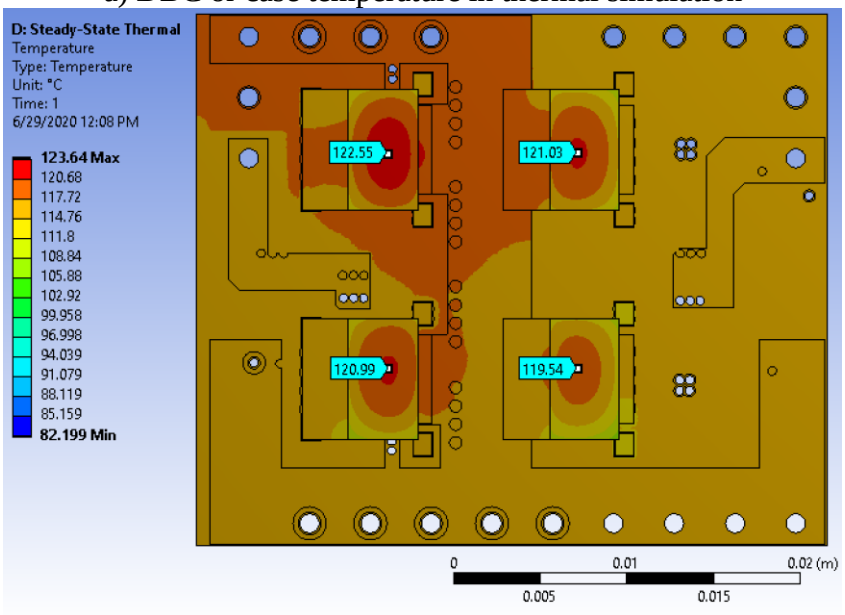
$$P_{Sw} = (E_{on} + E_{off}) * f_{sw} \qquad (5)$$

$$P_{Cond} = I^2 * R_{DS(on)} * Duty \qquad (6)$$

It has been seen that the highest junction temperature will be around 122.5°C while the highest case temperature is recorded to be 110°C. Junction to case resistance has been calculated to be 0.39°C/W per die. The result is shown in Fig.3.11



a) DBC or case temperature in thermal simulation



a) Zoomed view of the junction temperature of dies

Fig. 3.11 Result of thermal simulation

Most importantly, the temperature rise of both paralleled die in each switching position has only 1.5°C temperature difference and there is no thermal coupling between them. So dynamic current sharing will not be harmed due to imbalanced temperature distribution.

A half-bridge GaN module is designed, fabricated, and tested. This design sets a baseline for comparison of performance matrix and a new advanced design will be proposed in the next chapter comparable to the baseline design.

4 Double-Sided Cooled Advanced GaN Module

4.1 Introduction

With the emergence of GaN HEMT with superior device property, newly manufactured GaN HEMT's are superseding their Si counterparts in performance matrix such as lower on-resistance, faster-switching transient enabling higher switching frequency due to lower device input and output capacitance so that door to many new applications has become open. To effectively harness the advantages that the new devices offer, optimized packaging in the module level is important. A package should be designed with the consideration of optimizing electrical parameters such as low low commutation loop inductance to achieve lower voltage stress on device and having the flexibility to obtain fast switching speed, hence lowering switching loss, low gate loop inductances to robustly drive the device, minimum common-mode capacitance to minimize the common-mode leakage current, zero common source inductance in module layout and enough creepage and clearance distances to ensure electrical isolation and safety. At the same time, thermo-mechanical optimization such as low junction to case thermal resistance reduced interfacial stress and reliable interconnects are of the same importance for reliable operation and prolonged lifetime of the module.

When devices are being paralleled, the positive feedback phenomenon of $R_{DS(on)}$ with increased temperature in SiC and GaN balances the static current sharing. But when it comes to dynamic current sharing during the switching transient, the whole paradigm changes, and new factors come into consideration. Considering the gate and power loop is very symmetrical for the paralleled devices, dynamic current sharing may not be balanced as V_{th} (threshold voltage) has a negative feedback effect with the temperature that means with increased junction temperature, the

V_{th} will decrease. So ensuring equal junction temperature in each device that can be imbalanced due to thermal coupling between the devices is equally important to symmetrical gate and power loop implementation in layout.

A gate driver integrated, double-sided cooled, wire-bondless pseudo chip on-chip structure has been proposed and optimized with thorough electro-mechanical analysis ensuring all the above-mentioned parameters are optimized. The module employs a hybrid packaging approach using three separate PCBs and two DBCs. Power and gate routing has been done in the PCB while DBC provides electrical insulation and heat spreading functionality. A power loop inductance of 0.9 nH, and Junction to case thermal resistance of 0.2°C/W has been achieved. Customizing the DBC layout, the common-mode leakage current has been reduced by 15 dB. The module has been tested to its rated voltage and current after being manufactured to ensure the functionality of the fabricated module.

4.2 PCB and Gate Driver Design

The concept of this double-sided colled structure is inspired by the chip on chip structure. The design procedure started initially with a conceptual drawing shown in Figure where dies are placed on both sides of PCB in overlapping fashion ensuring a minimized commutation loop and mutual cancellation of flux generated by current flowing in opposite direction to achieve low power loop inductance. It also comes with the advantage of accessing the thermal pad of devices from both sides allowing a double-sided cooling feature for the entire module. To decouple the inductances introduced by the busbar terminals for powering the module, decoupling ceramic capacitors is decided to integrate inside the module itself along with isolated gate driver circuitry.

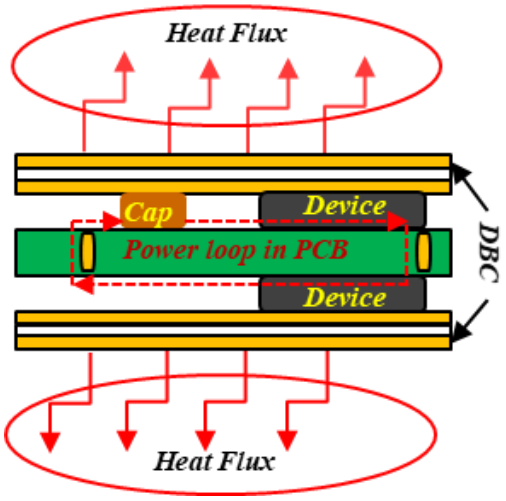


Fig. 4.1 Conceptual drawing of the double-sided cooled module

But the problem arises due to the mismatch of height between the device and the decoupling capacitor. GaN Systems yop side cooled prepackaged chip (GS66516T) has been selected to use. This chip comes with a thickness of 0.54 mm. Surface mount MLCC capacitor rated for 650V as well as selected gate driver IC does not have any available commercial package of that height. So, attaching DBC on the heat pad of the device is not possible in the provided architecture. Using a single PCB for housing all components also introduces reliability problem on GaN chips as well as manufacturing complexity as during manufacturing with existing architecture, it will need to go through at least 3 cycles of reflow.

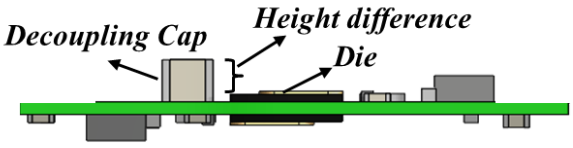
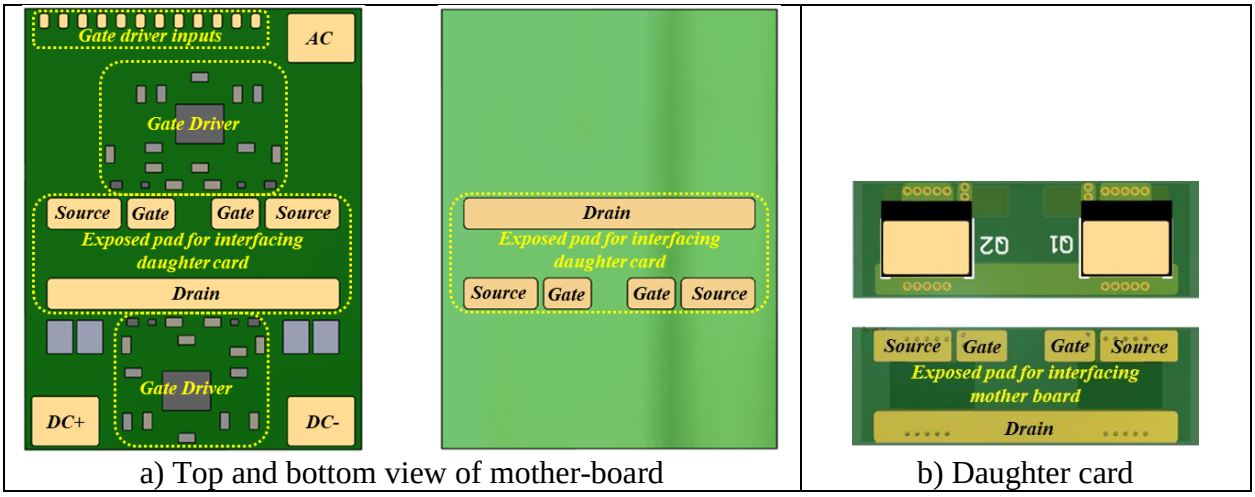


Fig. 4.2 Manufacturability problem in using a single PCB

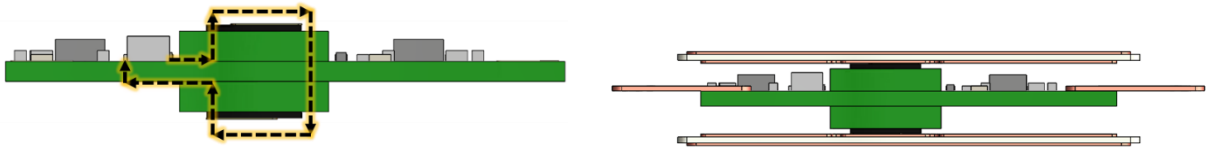
To address these problems, a mother board-daughter board concept has been proposed. The idea has been developed in a way that, no more than two reflow processes are not required during the fabrication of the package. In the daughter card, two parallel devices for each switching

position has been attached. The motherboard contains an isolated gate driver for top and bottom device as well as hold two daughter cards. The introduction of the daughter card solves the problem of height difference as that is compensated by the additional height of the daughter card PCB.



a) Top and bottom view of mother-board b) Daughter card

Fig. 4.3 CAD model of proposed mother-board and daughter-card



a) Achieved vertical commutation loop b) Side view of the module

Fig. 4.4 Vertical commutation loop with flexible manufacturability

The gate driver configuration is the same as explained for baseline design. So it is not repeated in this section.

After designing the PCB and defining the commutation loop, parasitics have been extracted using ANSYS Q3D software. A solution frequency of 10 MHz has been used considering the fast rise and fall time during switching transient. A total inductance of 0.9 nH has been achieved. Due

to increased height introduced by two additional dautghter-card, the mutual cancelation got reduced in this design.

4.3 DBC Design

As the gate and power loop are being routed inside the PCB, two DBCs are employed for electrical isolation and heat spreading. GaN Systems GS66516T is a top side cooled device and there is a large heat pad in the top side of the device which is also electrically connected to the source potential of the device. If we look at the half-bridge topology, the source of the top device is connected to the AC or switching node. Outer copper of DBC which has a direct interface with the heatsinks is recommended to be grounded for safety precaution. Stray capacitance is happened to form between the coppers of both sides of the DBC by following the physics of the parallel plate capacitor. Due to switching action, a voltage gradient (dv/dt) exists in the AC node which induces a displacement current through that parasitic capacitance and generates common mode noise from module to ground. Inadvertent designs lead to the requirement of a bulky EMI filter which reduces overall power and volume density of the system. If that issue can be solved at its source, the filter requirement will be less.

$$\mathrm{C} = \frac{A\varepsilon}{d} \qquad (7)$$

$$i_C = C\frac{dv}{dt} \qquad (8)$$

The thickness and the overlapping area are the two parameters that can be tweaked to reduce the capacitance as well as the CM current as changing the permittivity is limited by the available material options for the substrate. With the increase of thickness of the substrate, though the stray capacitance can be reduced, thermal resistance will go up. Commercially available DBC comes with standard thickness and customizing it will increase the cost. So playing with thickness is not

the best choice to go after. The methodical reduction of the overlapping area provides more design flexibility without increasing the thermal resistance. The DBC is etched in a way that can offer the capacitance reduction as well as uninterrupted heat spreading. A 45° heat spreading angle from the source has been assumed during the calculation. As the copper thickness in DBC is 0.3 mm in our design, in the die plane from the edge of the die, there should be copper pad more than 0.3 mm for uninterrupted heat spreading.

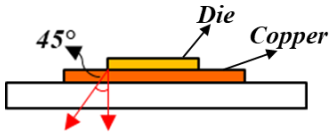
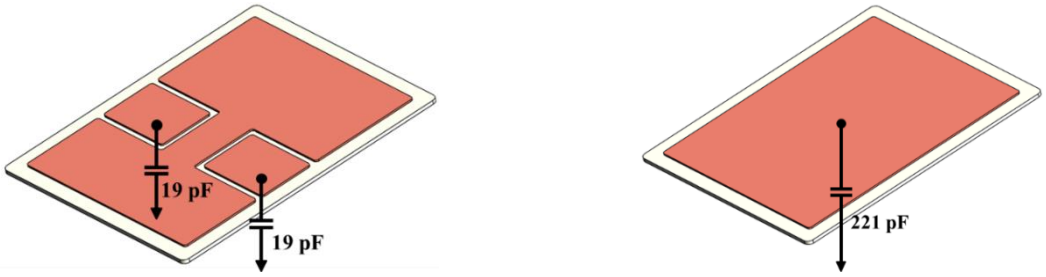


Fig. 4.5 Calculation of necessary copper for heat spreading

In the final design, a 1 mm margin is maintained. After developing the CAD model, parasitic capacitance has been extracted using Ansys Q3D. The developed pattern of the DBC shows around six times the reduction of parasitic capacitance.

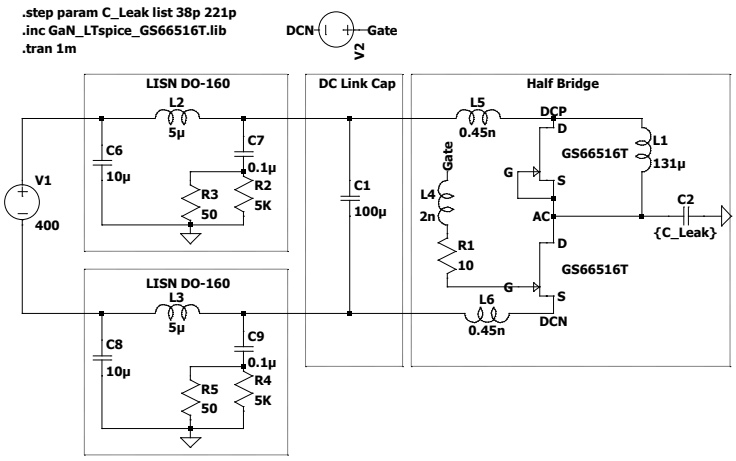


a) Etched DBC b) Non-etched DBC

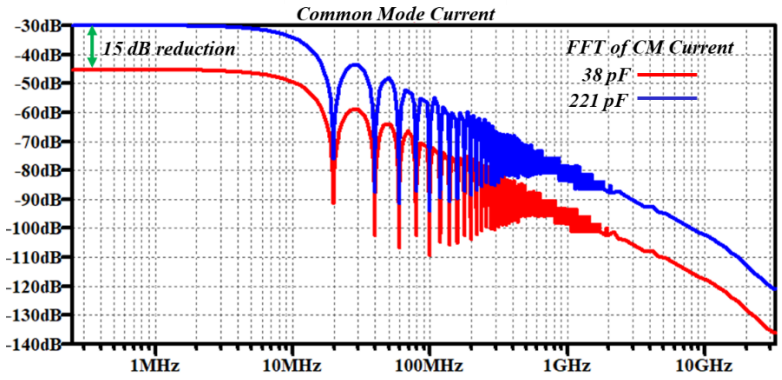
Fig. 4.6 Parasitic capacitance reduction

After doing the extraction, a spice model has been made with all the associated parasitics and LISN (Line Imbalance Stabilization Network). Gate pulses have been applied in the bottom switch of the half-bridge and top switch is clamped using an inductor. The noise current has been

measured and a fast Fourier transform has been done to show the results in the frequency domain. The result shows around 15 dB reduction of noise current using the proposed DBC structure.



a) Spice model for measuring common-mode noise



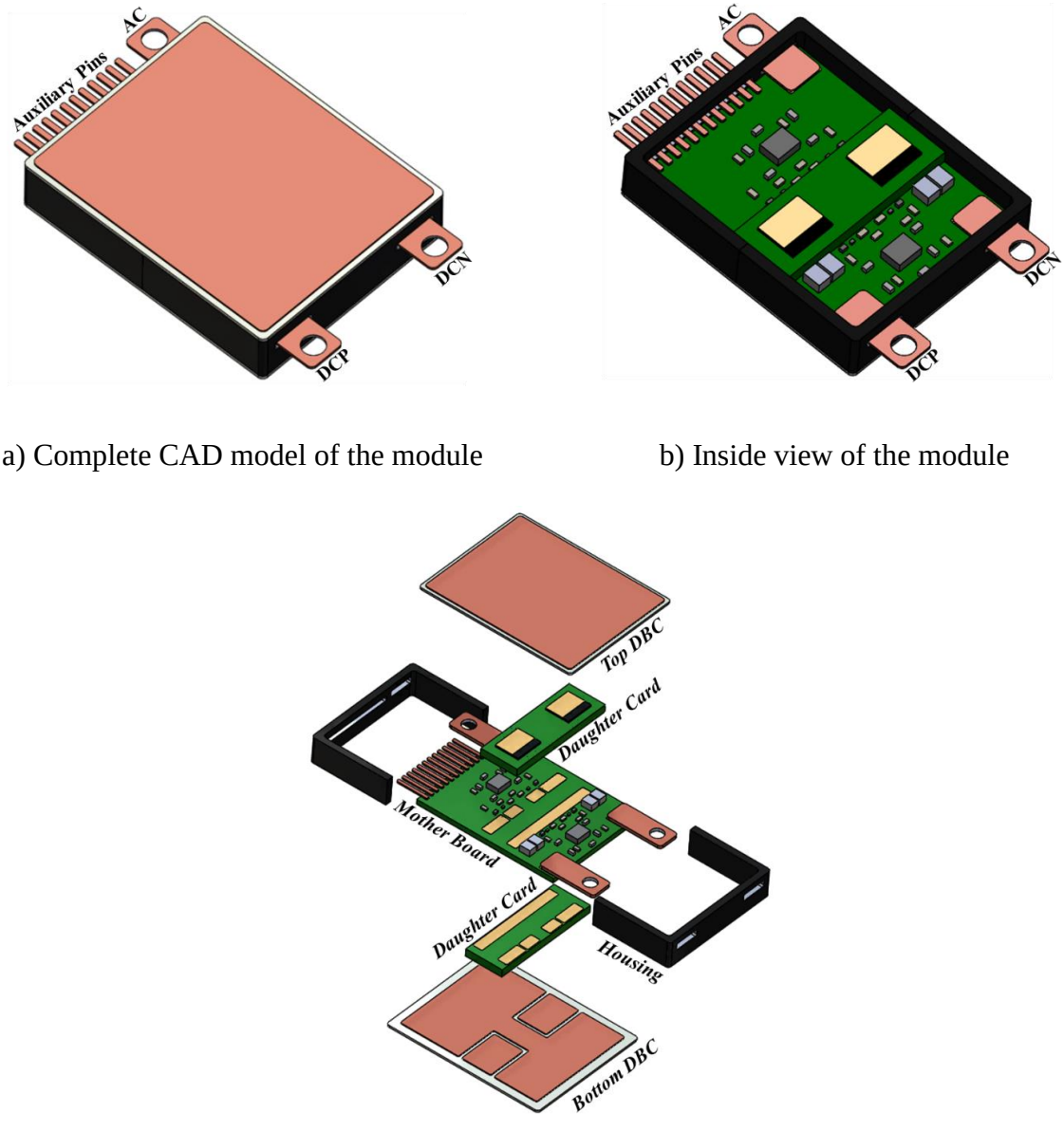
b) Simulation result of the Spice model

Fig. 4.7 Modeling the noise path to evaluate the effect of reduced parasitic capacitance

To verify that the DBC is not sacrificing its thermal benefits in the process of reducing the noise, a simulation has been done in para power. The simulation result shows only a 2° increase of case temperature compared to its unetched version.

4.4 CAD Model of Module

A detailed CAD model has been developed before starting the fabrication process. In module for external busing, custom made copper terminals have been used as a power terminal while surface mount male header with 2 mm pitch is implemented for auxiliary power and logic signals. The CAD model of the assembled module with an exploded view has been added in Fig. 4.8



a) Complete CAD model of the module

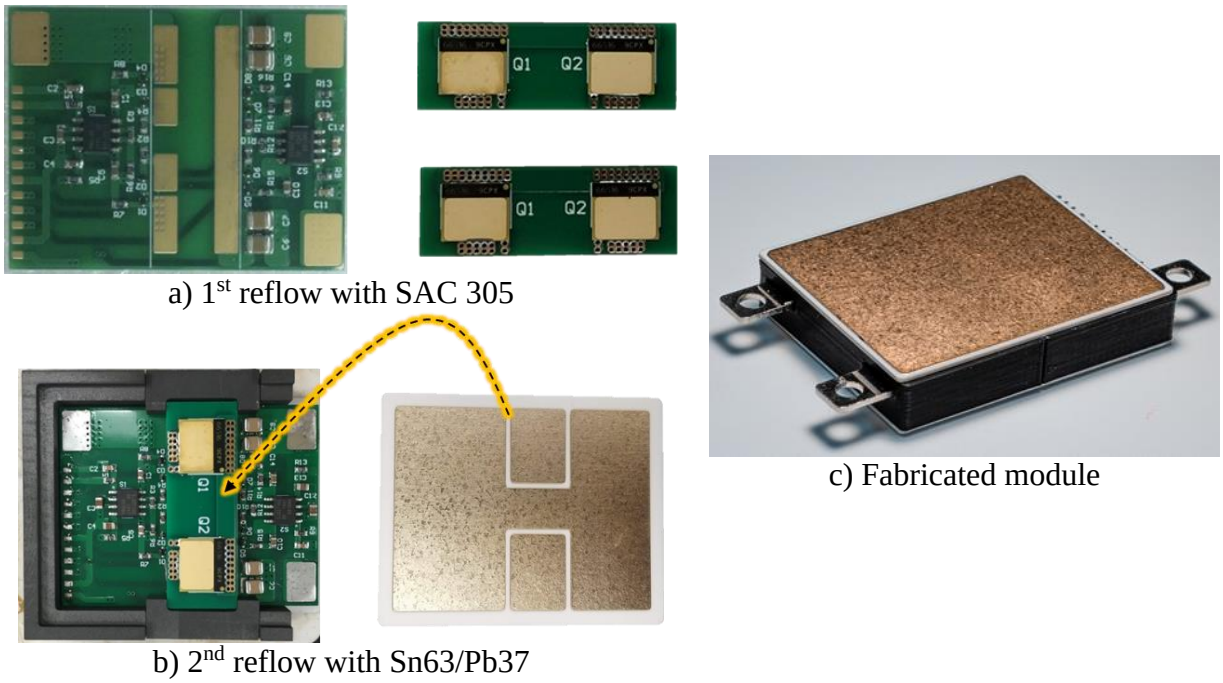
b) Inside view of the module

c) Exploded view of CAD model

Fig. 4.8 CAD model of the proposed module

4.5 Assembly Process

The assembly process of the module is done using two-step reflow soldering. At 1st reflow, gate driver components are attached to the mother-board. GaN chips are also soldered to daughter boards at the same time using SAC 305 solder paste. Then using a graphite fixture, mother-board, daughter boards, and DBC are soldered all together using Sn63/Pb37 solder paste. After the reflow process, 3D printed housing has been attached to the module which was poured with silicone encapsulant at the last step.



a) 1st reflow with SAC 305

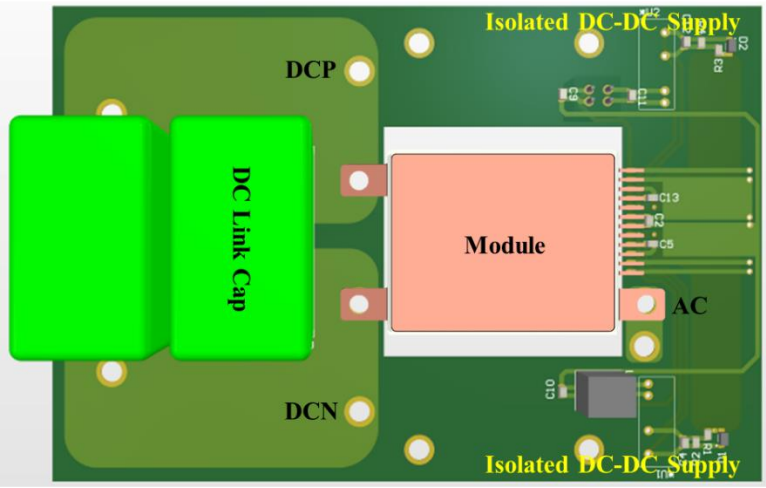
c) Fabricated module

b) 2nd reflow with Sn63/Pb37

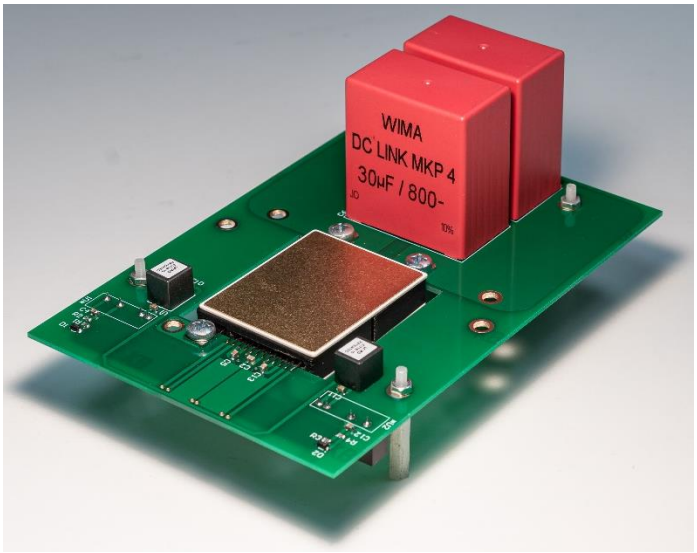
Fig. 4.9 Fabrication process of module

4.6 Electrical Testing and Thermal Simulation

An interface PCB is built afterward for testing the electrical performance of the assembled module. This interface board also holds an isolated DC-DC power supply for biasing the secondary side of the gate driver.



a) Outline of the designed interface board



b) Assembly with interface board for DPT test

Fig. 4.10 Interface board design and test setup with interface board

A double pulse test (DPT) has been performed on the module to test the electrical functionality of the module. An air-core inductor of a value of 131µH has been used to clamp the top device. The module was tested up to 400V/50A and the switching waveform has been shown in Fig.4.11

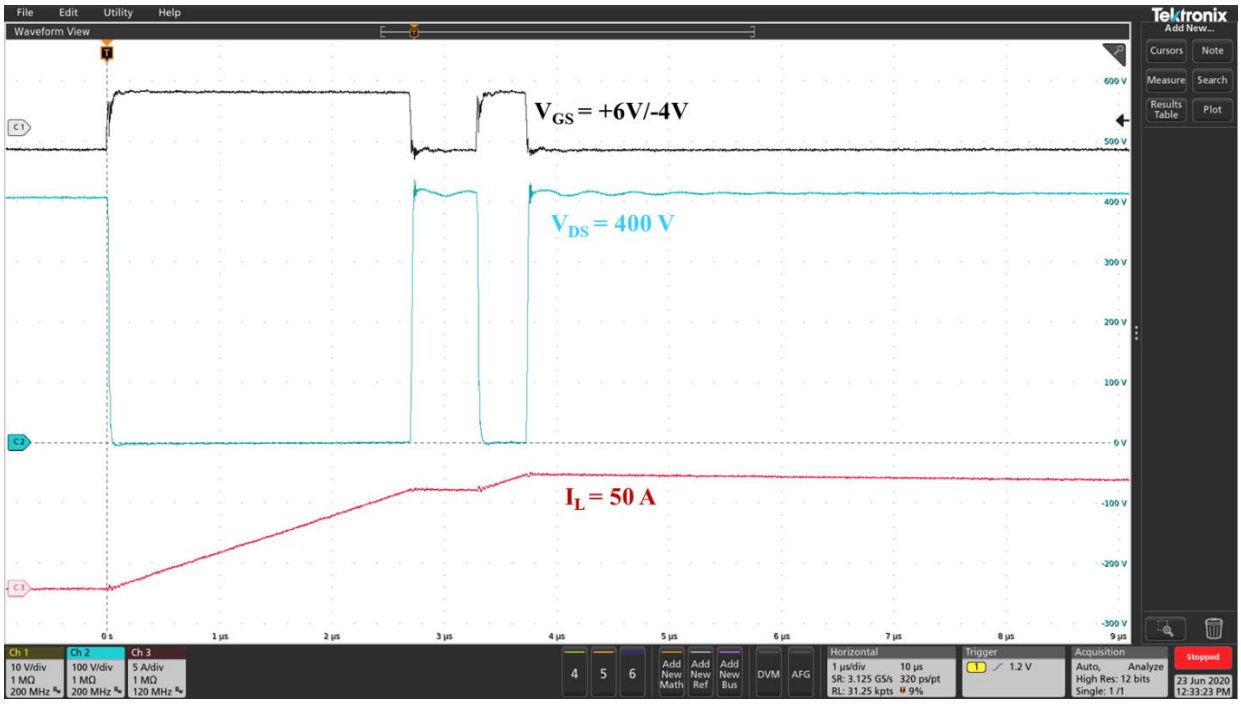
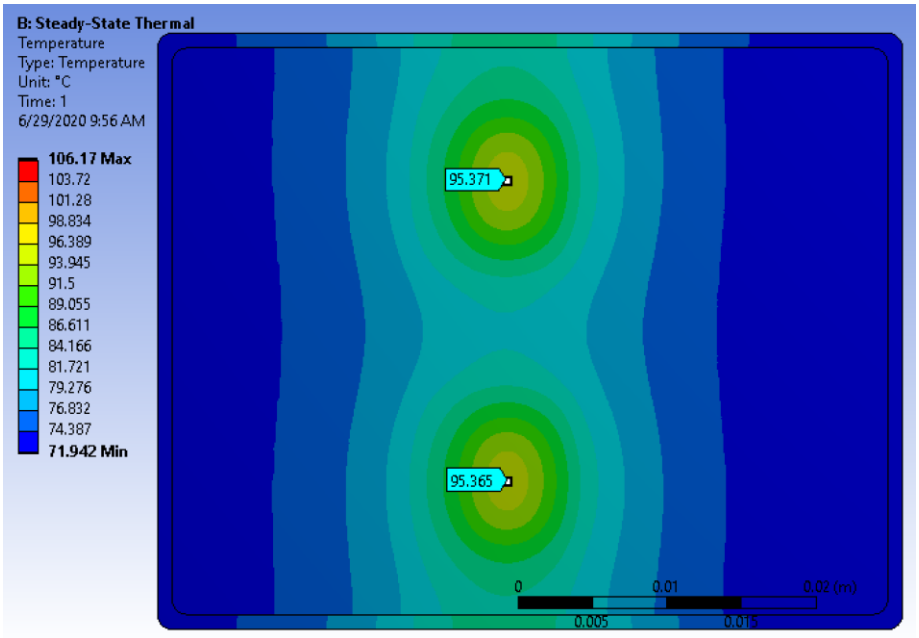
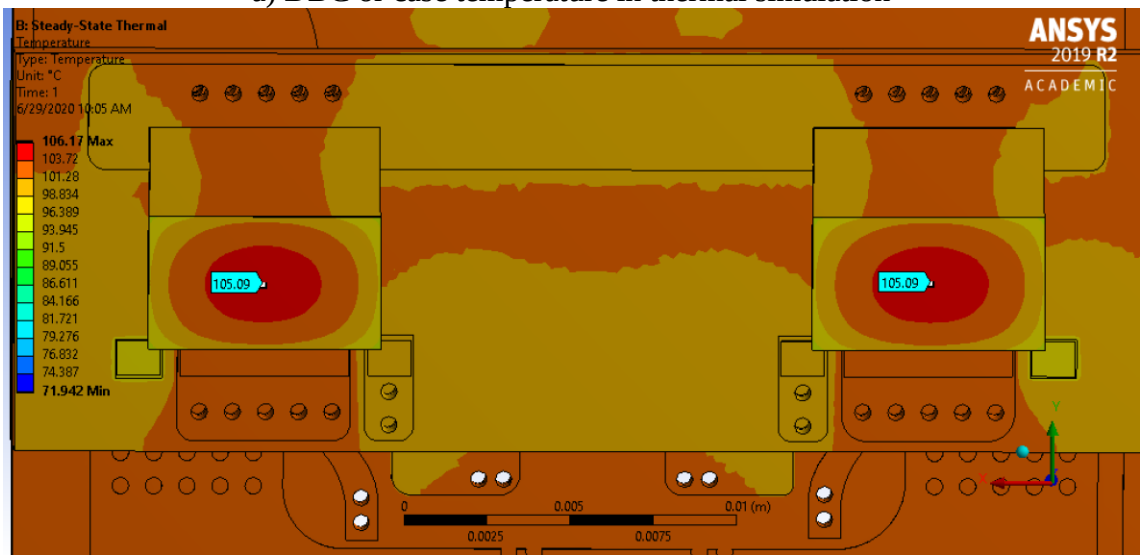


Fig. 4.11 Switching waveform at rated voltage and current

For evaluating the performance of the module, a steady-state thermal simulation has been done using Ansys workbench. Assuming the module is running in buck mode with a duty cycle of 0.5, 50A current and switching frequency of 200 kHz, the total sum of conduction loss and switching loss per die has been calculated to be 35W. A convection coefficient of 5000W/m^{2}k has been applied during simulation. It has been seen that the highest junction temperature will be around 106°C while the case temperature in DBC will be 95.3°C. That gives a junction to case thermal resistance of 0.31°C per die. Most importantly, the temperature rise of both paralleled die in each switching position is the same and there is no thermal coupling between them. So dynamic current sharing will not be harmed due to imbalanced temperature distribution.



a) DBC or case temperature in thermal simulation



a) Zoomed view of the junction temperature of two paralleled die

Fig. 4.12 Result of thermal simulation

A double-sided cooled design has been proposed, fabricated, and tested in this chapter. This design has improved thermal performance, dynamic current sharing and cooling space so more current can be pushed compared to the baseline module. Moreover, the way of noise reduction with DBC design and its impact has been explored. The reliability and lifetime expectancy of both designs will be evaluated in the future.

5 Near Field EMI Modeling

5.1 Introduction

Recent advances in wide bandgap power devices have resulted in increasing power density for power converters. Near field models of power modules are essential to design better packaging of other auxiliary circuits in a power converter. A simplified power module like structure is considered. The entire power module is then subdivided into simpler geometries and modeled separately. The overall map of the near field is then obtained from these simple geometries. The result from the simulation and measurement has been compared to the modeled map to validate the model.

Advances in wideband gap devices have enabled higher switching speeds and higher switching frequencies in power electronic converters which have led to higher efficiency and power density. To enable the next wave of advances in power density, it is essential to package the entire converter effectively. Among the challenges to high-density packaging, EMI is one of the most important. [85] The near-field radiated EMI from the switching power devices gets coupled to other auxiliary circuits such as the gate drivers and other control circuits [86]. There is a good understanding of the conducted coupling mechanisms due to the high dv/dt and di/dt of these devices [87]. The same cannot be said about radiated EMI. Having a good understanding of the near field EMI would facilitate more robust designs of auxiliary circuits and enable high-density packaging.

In the far-field ($D>\lambda/2\pi$), the electric (E) and magnetic (H) fields are proportionally related by the wave impedance Zw (377 Ω). This is not the case in the near field region. Instead, depending on the geometry of the object under consideration, either E or H field dominates. The dominance

depends on impedance offered by the geometry under consideration. If the impedance is high, the E field will be dominant and it can be modeled as a dipole antenna. If the impedance is lower, H field will be dominant and it can be modeled as a loop antenna [88-89]. Several authors have proposed modeling the E and H fields using different approaches. Leone, et al. [90] has developed an analytical closed-form expression using greens function for a microstrip line. Here radiated electric field has been calculated from current flowing through the trace and vias. Rogard, et al [91] has developed a model for a transmission line with different approaches such as: using greens function, Spice based circuit method, and modified Korn method and compared them with full-wave simulation results. These models are also built for evaluating radiation in far-field. Antonini, et al [92] has developed a model for the converter section of SMPS and built a lumped Spice model to evaluate the current distribution. Then using the Hertzian dipole model they evaluated E and H field in the near field region. The model was validated for up to 10 MHz

Some literature has focused on modeling conducted and radiated EMI. One of the most commonly exercised approaches is Spice based equivalent circuit modeling. Here the accuracy of the model depends on accurate extraction of parasitics and placing them in the equivalent circuit. This approach is tedious, and the offline impedance measurement yields results that have a good match only up to a few 10s of MHz [93]. Dutta et al. have measured the radiated EMI from a WBG power module. They used near-field probes to measure the field at a point in fixed elevation and ANSYS HFSS-Simplorer co-simulation to verify their approach. Their simulation approach is similar to Spice based modeling since they extracted the parasitic of system layout and included in the equivalent circuit, they built in the ANSYS Simplorer [94]

Tong et al. [95] have presented a method for modeling near field based on the measurement result from the near field scanning. In this method, the main layouts are replaced with equivalent

dipole which can create the same radiation in the measurement plane. The near field scanning using probes does not reveal the phase information. Again, this method for carried out only for a single microstrip line and was not validated when more than one geometry is placed in close vicinity.

Antonini et al. [96] presented another manuscript where involving modeled radiated EMI for industrial power drives. They used the PEEC model which predicts the surface current by developing an equivalent model circuit. This method provided a solution only for the electrically short traces. Sayegh et al. [97] presented a technique to overcome the limitation of electrically long traces. Here the model considered electrically long traces as a composition of multiple short traces which is further solved using transmission line theory and Hertzian dipole model. A closed-form expression E field for both CM and DM current developed by Paul et al. [98]. The model also works up to 200 MHz.

Zhang et al. [99] developed a model for Radiated EMI from an isolated power converter. Here the voltage difference between a two winding of a transformer is considered as excitation, which is driving the cable connected to the input and output side. The voltage source is modeled and the radiation resistance of the structure is determined by extracting S parameter with a VNA and determined maximum E field in the far-field region.

In a power module, the power loop is the main contributor to the radiation from the power module. The near field of the power modules depends on the switching state of the power devices. From the literature, there were no previous works that have developed models for near field prediction in power modules. This work aims to bridge this gap and develop simplified models that could be scaled for a multi-chip power module.

The organization of the paper is as follows. Section II describes the methodology for modeling. Section III describes the measurement setup. Section IV presents the preliminary experimental results. Section V presents the conclusion and future work.

5.2 Automated Near Field Scanner

To measure near field emission in close vicinity to the DUT, an automated system has been set up with high resolution and repeatability. A robotic arm is programmed using python-based GUI and interfaced with LABVIEW through Arduino UNO. Sniffer probe is attached to the robotic arm which can be moved with step size as low as 0.2mm.

RIGOL DSA815 spectrum analyzer has been used to acquire data that is controlled via LABVIEW for data acquisition. Bandwidth window, RBW and VBW is user-defined and can be defined at the program written in LABVIEW. Initial and final coordinates of the scanning object are also user-defined and given at the time of initialization along with altitude from the scanning surface and step size in the Python-based program that has been written to control the robotic arm. After making one step, robotic arm holds its position, LABVIEW acquires data of that position from spectrum analyzer and after completion of data storage, and LABVIEW sends a signal through Arduino to the Robotic Arm. This signal triggers the Robot control program to execute the next step. The robot moves one step ahead and so on.

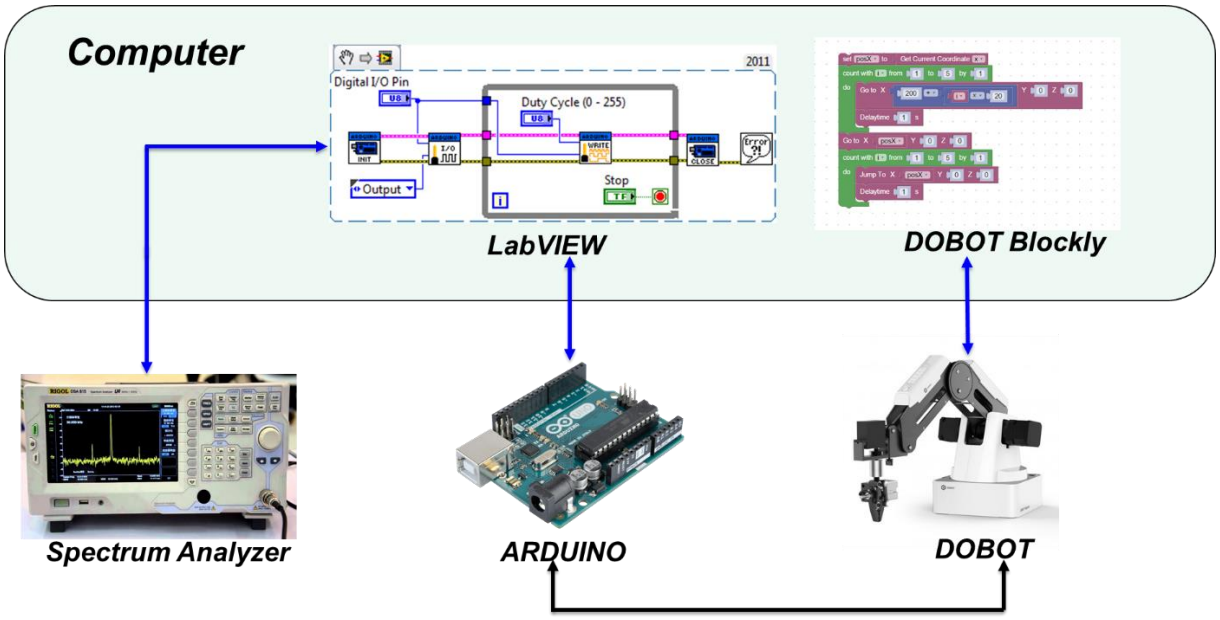


Fig. 5.1 Automated Near field Scanner

Stored data is plotted and post-processed using MATLAB. Sniffing probe from Tekbox is used which has both E and H field probe with different aperture size and rod length for being used in different applications. Those probes are calibrated up to 3 GHz. A pre-amplifier with +20dB gain has been used in conjunction with the sniffing probe. The system has four axes moving capability. The whole system architecture is shown in Fig.5.1

At the time of measuring E field, the orientation of probe is not a concern according to IEC TS 61967-3: 2014. During the measurement of the H field at a certain elevation, the probe should be oriented properly to get the reading of components of field data. The aperture of the probe should be placed orthogonally to the line of flux for better coupling as well as better measurement. Two different sets of measurements have taken for each mode of operation, in this case, to get the field-oriented in X and Y direction individually. Then both combined to project the total magnitude of the H field in a plane at a certain elevation.

For small-signal analysis, different structures have manufactured according to the commutation loop shown in Fig. 2 and excited with 10 MHz signals from HAMEG HM8131 signal generator. High voltage, low distortion op-amp TH3091 is used in non-inverting configuration between the signal generator and DUT to regulate the current flow.

The whole test setup and DUT is placed inside a grounded Faraday cage to mitigate the effects of noise from the environment. Fig. 5.2 shows the photo of the test setup.

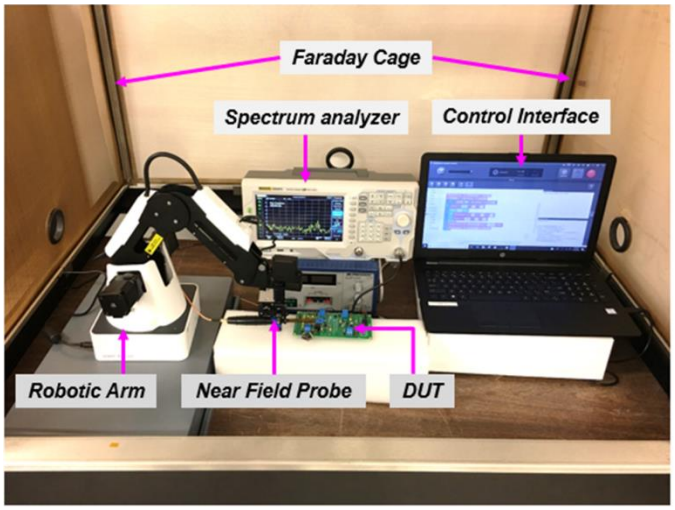


Fig. 5.2 Test setup for near field scanning

5.3 Modeling Approach

In literature, different methods have been described to model E and H fields analytically. Using microstrip model E field in near field can be modeled using below stated closed-form expression which is built on basic equations of a dipole antenna.

$$E_{D,max} = 1.316 * 10^{-14} * I_D * f^2 * ls * \frac{1}{r} \qquad (9)$$

$$E_{C,max} = 1.257 * 10^{-6} * I_C * fl * \frac{1}{r} \qquad (10)$$

Here, the equation for E field for both differential and common mode excitation has been stated where I_D and I_C are DM and CM current, *f* is the frequency of excitation/interest, *l* is length and *s* is the width of the microstrip line.

As stated previously, any structures with low wave impedance can be modeled as a loop antenna, and subsequent behavior can be predicted analytically using the below-stated equation in the spherical coordinate system.

$$H_r\ (A/m) = \frac{IA}{\lambda}\left[\frac{j}{D^2} + \frac{\lambda}{2\pi D^3}\right] \cos\sigma \qquad (11)$$

$$H_\sigma\ (A/m) = \frac{\pi IA}{\lambda^2 D}\sqrt{1 - \left(\frac{\lambda}{2\pi D}\right)^2 + \left(\frac{\lambda}{2\pi D}\right)^4}\ \sin\sigma \qquad (12)$$

Here λ is the wavelength in the frequency of interest; I is the current flowing through the structure, D is the distance of the point of measurement, A is the area of the loop under consideration and σ is the zenith angle.

H_r is maximum in the $+Z$ direction, but it vanishes rapidly due to its D^2 and D^3 term; hence it is of little interest. When σ is 90°, the maximum field is obtained for H_σ. So equation one is considered and modified with different zenith angles to get a map in a plane with fixed elevation. By ignoring term with lower exponent, equation (4) can be rewritten as:

$$H_{A/m} = \frac{IA}{4\pi D^3}\sin\sigma \qquad (13)$$

A very important observation here to make from the equations mentioned above are in the near field, though the H field is frequency independent, E field is not. E and H field always have a proportionality which is defined as wave impedance that also becomes frequency-dependent in the near field region.

A power module like structure with a half-bridge has considered and operated as a buck converter in CCM mode. The structure that is going to be modeled is shown in Fig.5.3

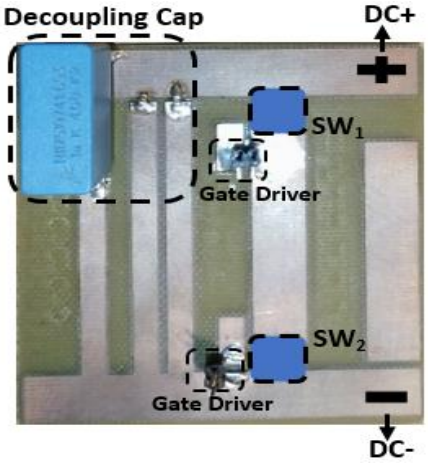
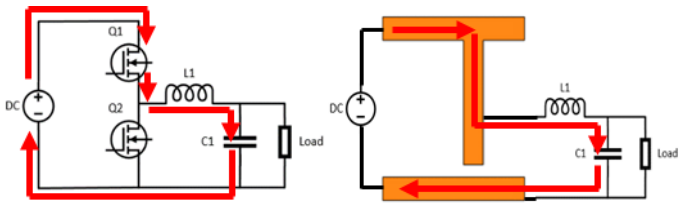
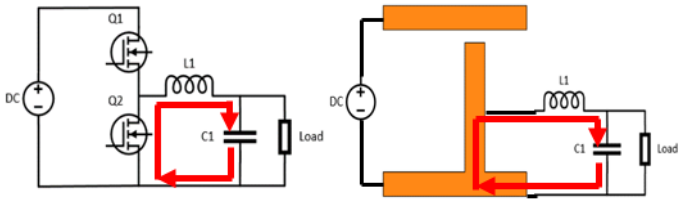


Fig. 5.3 Structure to be modeled

In this synchronous buck converter, two switching states will be there. For the very first instant, the top switch will be turned on, and the bottom one will be turned off. In the subsequent state, the bottom switch will be turned on, and the top switch will be commutated. Due to this switching, the path of current flow will change and so the near field map. The whole commutation process is shown in the below schematic:



a) 1st switching state & associated part of power module



b) 2nd switching state & associated part of power module

Fig. 5.4 Commutation Loop of a buck converter

In Fig.5.4, the associated part inside the power module through which current is flowing is shown. Radiation will solely be coming out of these parts will only be considered as the radiation from external interconnects, wire, and loads are beyond the scope of this research work.

So, these structures will be modeled separately after defining the commutation loop, the analytically developed equation is applied, and the derived map is matched with simulation and measurement result. An assumption is made that current is uniformly distributed on the outer surfaces of the structure and the same current is flowing through the entire structure under consideration. The deviation is taken into consideration and additional factors like fringing effect, the skin depth is incorporated to mitigate the mismatch. The total workflow is like:

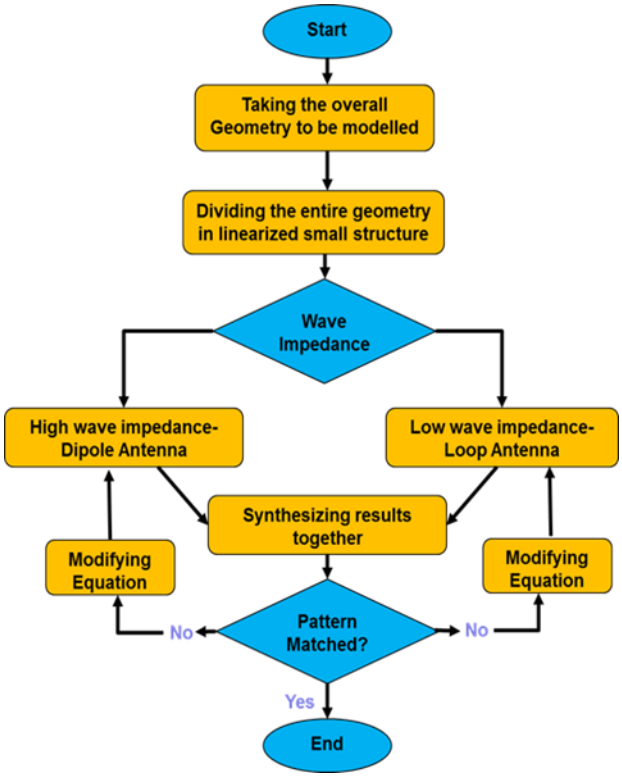
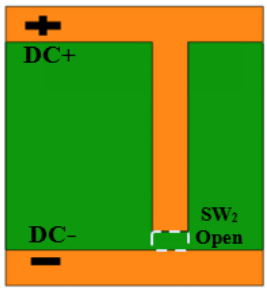


Fig. 5.5 Modeling algorithm

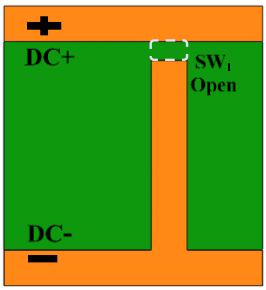
5.4 Validation of Model

A phase leg of a power module has been designed in the simplest structure with vertically integrated gate driver. Two surface-mount devices were placed separately to mimic the dies in switching positions. Initially, the phase leg was operated at synchronous buck mode.

The half-bridge during the synchronous buck mode behaves as two different types of antenna, loop, and dipole. For 1st switching instant, E field will be concentrated near the bottom switching device, and for 2nd switching instant, it will be around the top device. In the case of the magnetic field, the pattern will vary depending on the current commutation loop. As such, the pattern of the magnetic field will change accordingly.



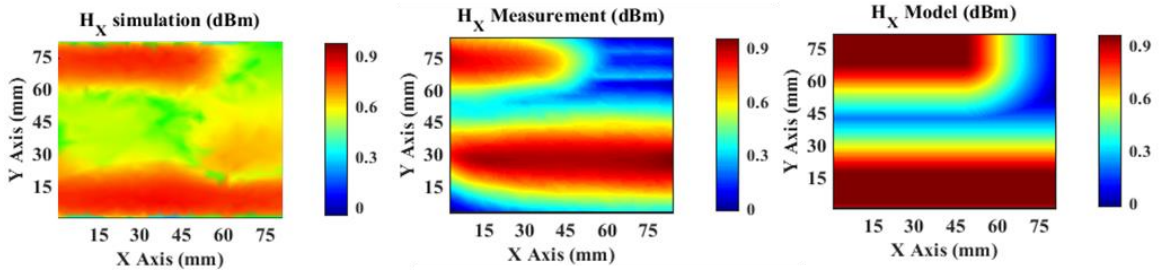
a) Equivalent physical structure for 1st switching state



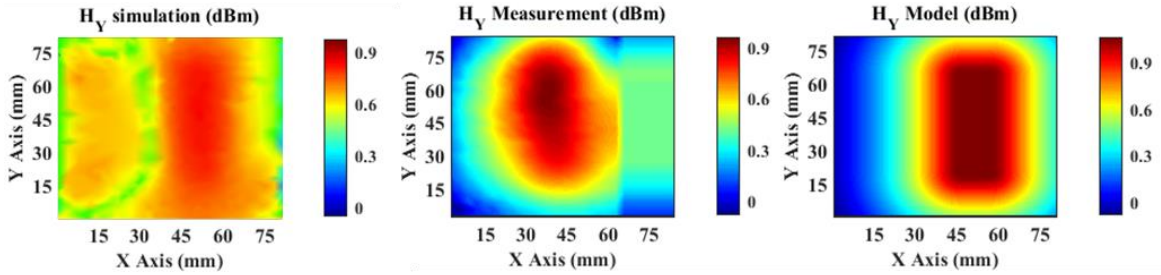
b) Equivalent physical structure for 2nd switching state

Fig. 5.6 Traces involved for the magnetic field in the different switching state

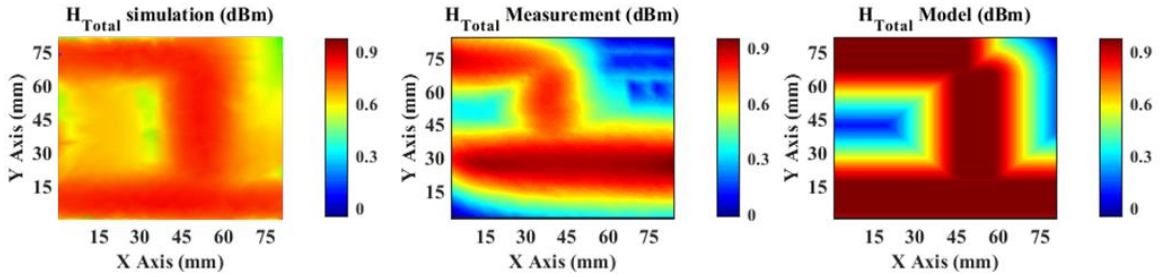
Using the previously described test setup, both the component of the magnetic field is measured, modeled, and shown side by side. As explained earlier, in the small-signal test we have measured the X and Y component separately by placing a sniffing probe in the required orientation. By combining two components of the magnetic field, we can get a full picture of an overall field in the plane of observation at a fixed elevation. Here the elevation is 20mm. Now the obtained results for 1st switching instant is shown below:



(a) Simulation, Small-signal measurement, and Model for H_X



(b) Simulation, Small-signal measurement, and Model for H_Y



(c) Simulation, Small-signal measurement, and Model for H_{Total}

Fig. 5.7 Validation of the proposed model for 1st switching state

Following the same steps, the small-signal model of the second switching state is also validated. Finally, the structure has been operated in buck mode at 10 kHz switching frequency with 50% duty ratio in the same layout. The power was pushed up to 250W with a resistive load. IXFA36N30P3 from IXYS with $R_{DS(on)}$<110mΩ was used in the switching position. The value of boost inductor and resistor was set to 330μH and 10Ω to ensure the converter is operating at CCM. Powder core with distributed air-gap(High Flux) has been chosen as core material so that the core can operate in the linear region. As the switching phenomenon will result in trapezoidal pulses

across the device; the current will not entirely be DC at a steady state. The time-domain waveforms are shown in Fig.5.8

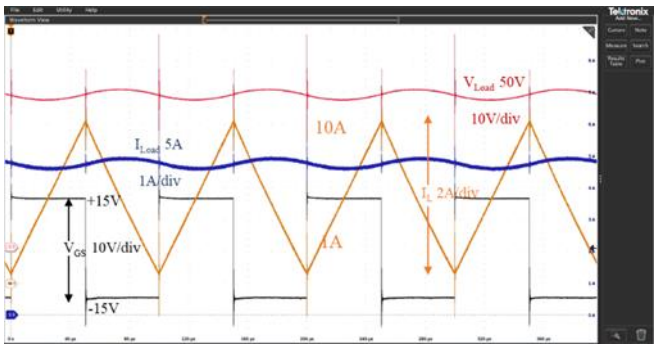


Fig. 5.8 Time domain waveshapes of V_{GS}, I_L, $I_{Load,}$ and V_{load}

Though the employed H field probe is capable of capturing all the harmonics of current ranging from 9 kHz up to 3 GHz, a fixed harmonic has been taken into account with the same frequency of excitation of the small-signal test. Now the whole converter has been scanned as mentioned previously and the surface plot has been generated for one particular harmonics. The continuous test result also shows a very close match to the small-signal model.

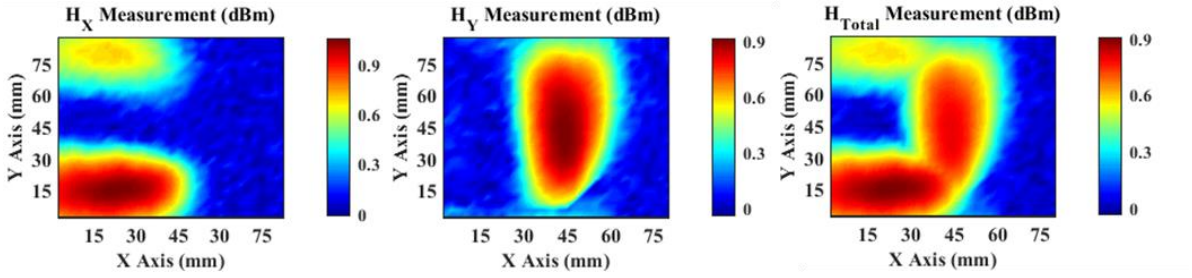


Fig. 5.9 H_X, $H_{Y,}$ and H_{Total} for buck converter

According to the discussion and modeling procedures shown with examples, a planar power module can be modeled in current capacity. The small-signal test and high power test shows coherence. At the time of the whole system layout, the digital circuitry where high signal fidelity is required can be placed wisely with the aid of the radiation pattern. Time-varying excitation with

higher frequency will have a skin effect and current crowding to the edge of the structure. Again in terms of E field when two traces will be closer, there will be effects from the fringing field and mutual coupling. If all these additional factors can be included, a lower deviated model with better matching can be achieved.

6 Conclusion & Future Work

Two GaN module has been designed fabricated and tested to their rated capacity. One of the modules has single-sided cooling capacity while the improved design has a double-sided cooling feature. In the future, a power stage will be built using those fabricated modules which will be helpful to evaluate their performance in continuous operation.

Reliability test will be done to see how the module respond to the thermal cycling, how good the joint in the interfaces are and what is the expected lifetime of the module.

For near field modeling, the existing model can only predict the planar power module with a 2D commutation loop. It will be further extended to predict the near field map of the vertical power loop.

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