OFFSET AND NOISE BEHAVIOR OF MICROFABRICATED ALUMINUM GALLIUM NITRIDE—GALLIUM NITRIDE TWO-DIMENSIONAL ELECTRON GAS HALL-EFFECT SENSORS

A DISSERTATION
SUBMITTED TO THE DEPARTMENT OF ELECTRICAL ENGINEERING
AND THE COMMITTEE ON GRADUATE STUDIES
OF STANFORD UNIVERSITY
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

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August 2019

This dissertation is online at: http://purl.stanford.edu/zf844xc3673

I certify that I have read this dissertation and that, in my opinion, it is fully adequate in scope and quality as a dissertation for the degree of Doctor of Philosophy.

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Abstract

Magnetic sensors are quite common in every day life, with a variety of uses in mobile devices, electric machines, cars, motors, navigation, and planetary exploration. They are incredibly useful due to their non-perturbing nature. For example, they infer information about position, velocity, and current in power systems. Silicon Hall-effect sensors are popular for many applications due to their low cost and ease of integration with silicon circuits. However, silicon Hall-effect plates cannot operate at extreme temperatures (below −100℃ or above 300℃) due to carrier freeze out or intrinsic carrier leakage, respectively. In addition, Hall-effect plates have challenges with thermal drift, offset, and flicker noise.

In this PhD thesis, I start with an in-depth focus on the fabrication of high aspect ratio trenches (18.5:1) in 4H-SiC for potential use in direct hot-spot cooling of GaN-on-SiC power devices as well as extreme environment SiC microelectromechanical system (MEMS) applications. I then switch gears and describe an AlGaN/GaN 2DEG Hall-effect plate with ~100 ppm/K constant-current sensitivity drift, 0.5 µT offset, and 200 Hz corner frequency. These metrics surpass state-of-the-art silicon Hall-effect sensors with a larger temperature operation range, stability of sensitivity, and lower offset and noise floor. I then describe the fundamental limits of offset in GaN devices and present an examination of the flicker noise of these devices. Through this work, I have achieved a record-low offset in GaN 2DEG Hall devices, presented the first framework for studying noise in GaN Hall sensors, and have demonstrated a world record aspect ratio in bulk 4H-SiC machining. These contributions will enable a future monolithically integrated GaN–on–SiC platform for extreme environment sensors and power electronics. I conclude with proposing future work, including a path forward for implementing these devices in extreme environment systems.

Acknowledgments

Several amazing people ought to receive gratitude for their contributions to this milestone in my life. First, I would like to thank all of my teachers—their guidance, encouragement, enthusiasm, and support have shaped the researcher I am today. In particular, I want to thank two members of my reading committee: Prof. Roger Howe, and Prof. Jim Plummer. Prof. Howe was my first point of contact at Stanford, and was incredibly supportive through the months of preparing for quals. I have also taken a few of his clean room courses and gained valuable knowledge in fabrication, and the value of a strong academic network. He also was the professor who introduced me to Prof. Debbie Senesky, who I was so lucky to have as my advisor. Prof. Jim Plummer holds a reputation as one of the best teachers on the Stanford campus, and I had the privilege of being a course assistant for his new course: Power Semiconductor Devices. This was one of the most valuable experiences I had in graduate school.

Next, I would like to thank my advisor, Prof. Debbie Senesky, and the XLab. When I first learned the group focuses on extreme environment MEMS, I was incredibly excited. Our first meeting was quite interesting—she was about to go on maternity leave and had an aggressive DARPA project which needed a student. Her trust in a new student like me, that early on, really helped me build my confidence as a researcher. In addition, the lab culture is very collaborative, creative, and intellectually stimulating. I was the fifth student to join the group, and I saw the lab grow to where it is today. I worked closely early on with Dr. Ateeq Suria, Ashwin Shankar, and Dr. Caitlin Chapin. I also really enjoyed sharing the office and lab outings with Dr. Ruth Miller, Dr. Minmin Hou, and our first post-docs Dr. Heather Chiamori and Dr. Helmut Köck. There are so many more colleagues to thank who have joined since then: Dr. Ananth Yalamarthy, Sambhav Jain, Hannah Alpert, Thomas Heuser, Ruiqi Chen, Savannah Benbrook, Dr. Hongyun So, Ricardo Peterson, Dr. Saleh Kargarazzi, Dr. Hoang-Phuong Phan, and many more visitors and students who recently joined. I would also like to thank the undergraduates who I directly worked with: Pengxiang Zhang, Daneille

Rocca-Bejar, Anthony Garcia, Andrea Ramirez, Lige Liu, you all did a great job and contributed significantly to my projects! XLab has a strong culture of family, and I am happy to have this one for the rest of my life.

I also need to thank many collaborators from Stanford and other Universities. We had work with the NSF Engineering Research Center for Power Optimization of Electro-Thermal Systems (POETS). I would like to thank the staff, professors, and students of POETS for such a great collaboration experience. Through Stanford SystemX I worked closely with Infineon Technologies on Hall-effect devices: Dr. Helmut Köck and Dr. Udo Ausserlechner, and took an internship through the Stanford Europe Center in Germany there with Dr. David Tumpold. I also want to the thank Barbara Plante and everyone at Boreal Space. We collaborated to get these sensors on a rocket flight, and it was a great team experience. I am also excited about the work starting with Prof. Makinwa at TU Delft. I've had many Stanford collaborators too: students of Prof. Goodson, Prof. Pops students, and Prof. Kenny. I have found the cross-talk between these groups to be one of the best experiences I have had during graduate school. Also special thanks to the staff and users at the Stanford Nanofabrication Facility and Stanford Nano Shared Facilities, their training and maintenance of the clean room facilities were critical for my research. Special mentions for Dr. Xiaoqing Xu, Dr. Usha Raghuram, Dr. Jim Provine, Dr. Astrid Tomada, Dr. Mary Tang, Dr. Jim McVittie, and Dr. Peter Griffin.

My communities at Stanford have also been a huge blessing. I would like to thank my friends and colleagues in the EE department. We have many great memories together studying for quals, playing ultimate frisbee, going dancing, seeing movies, singing karaoke, playing various video games, watching football games, and supporting each other along the PhD life. Also thanks to my friends through Women in Electrical Engineering (WEE). Special thanks to Dr. Mimi Yang—my oldest EE friend. I also need to thank everyone from the Catholic Community at Stanford—and all the amazing students I have metthere over the years. Stanford's Office of Religious Life is a special resource—their support for students of faith really supports inclusivity on campus. There I found several amazing opportunities for fellowship, including my womens group known as Doves, the rosary group, and the weekly dinner discussion series: they kept us well-fed! This is also a good spot to thank the undergraduates who ran Stanford Students for Life. I really enjoyed our advocacy for student mothers on campus and our visits to local non-profits that help expecting mothers in need.

I need to thank my family, who have shaped me from the beginning. My parents David and Cathy, who created a home of love and curiosity, and emphasized the importance of a strong education.

Our weekly phone calls are so helpful and refreshing and make me miss home all the more. Also my siblings—Mike, Ellen, Paul, Tommy, Susan, and Matthew. Thank you for your support from far away, and the fun we have when we are together. I also want to thank my extended family on the west coast, especially my grandmother, Alcyone Dowling. Also, many thanks to Raghav, who was incredibly supportive in this last year of school. The special food deliveries on late evenings in the lab, as well as our laptop cafés in Durand on button pushing and writing weekends made those final stretches easier. Hes like no one else I have ever met, and I am incredibly proud to be his fellow adventurer in this world.

Finally, I want to thank God; I am nothing without Him.

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Chapter 1

Introduction

1.1 Magnetic Field Sensors: Overview of Applications

While not obvious, magnetic sensing is crucial for the technology in our everyday lives. To start, let's consider two major trends in the automotive industry. There is a push for electrification—to reduce CO_2 emissions, reduce petroleum consumption, and improve efficiency of mobile systems [7]. This will require power electronic systems that push aggressive amounts of power through traction inverters as well as other DC–DC and AC–DC switching applications under the hoods of cars. These power systems will need to increase in efficiency and power density. These high power density layouts have less area to remove heat, which leads to increased temperature operation—which is more prone to failure. Thus, these new systems are monitored with various electro-thermal sensors for predictive health monitoring and failure prevention. Two key metrics to measure are temperature and current. Magnetic field sensors are primarily used to monitor the current outputs of these devices.

Another trend is autonomous driving. Cars will be able to transport people (and goods) more effectively with the removal of human drivers—for example, by mitigating traffic. However, autonomous driving will take time to earn the trust of consumers, and this must be accomplished by achieving extreme reliability. In order to do so, autonomous driving will require incredibly accurate sensor data to understand the environment as well as the state of the moving parts. A common method for sensing position, angle, and velocity in the car wheels (driving, steering, and internal gears) involves the use of small magnetic sensors to detect the passing of a permanent magnet on the edge of a gear, motor, or other mechanical mechanisms. Thus, the increased electrification and autonomy of the automobile demonstrates the need for high performing magnetic field sensors. This

is shown in the magnetic sensor market trends: automotive applications are driving the growth of these markets [8].

Beyond the car example, there are several more uses for magnetic sensors. Other mobile and autonomous systems also rely on these sensors (*e.g.*, drones, mobile phones, and airplane motors) for similar use in power and position sensing. Magnetic sensors also find uses in direct field sensing—compasses and geological investigations both on Earth and beyond (solar flares, Jupiter, Europa, etc). Figure 1.1 summarizes the broad areas of these applications.

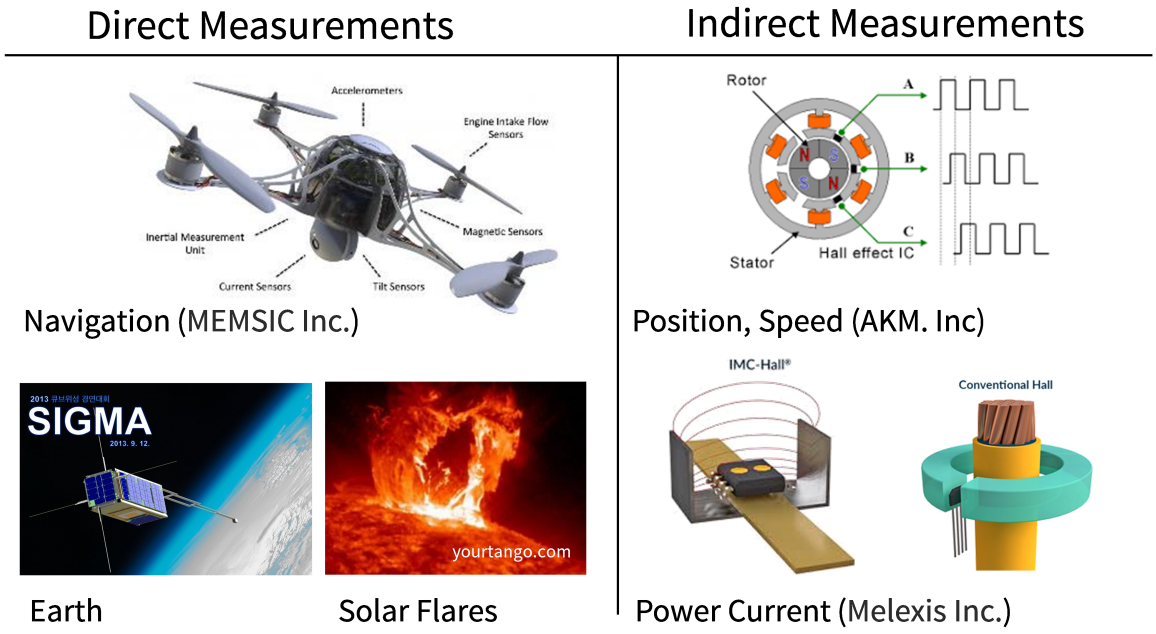
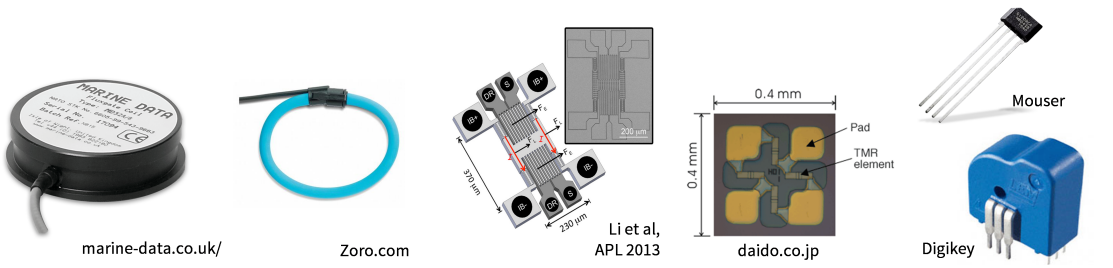


Figure 1.1: Overview of various magnetic field sensing applications. Direct measurements are used for magnetic field measurements. Indirect measurements are used to infer information such as position, sensing, and current.

1.2 Types of magnetic field sensors

Since there are various magnitudes and orientations of magnetic fields in practical applications, several different types of magnetic sensors have been developed to target them. This section will provide a brief overview of many magnetic sensor types and their main applications, summarized in Figure 1.2. It should be noted that some devices that operate via threshold detection or binary output, such as reed switches, are not covered here, because they target applications that do not



	Flux Gate	Rogowski Coil	MEMS	XMR (AMR, GMR, TMR)	Hall-effect
+	Accurate Low Drift	No Saturation Linear	Low noise Tunable Small	Sensitive Low power	Cheap Small + IC Low power
-	Expensive Complex Magnets	Low sensitivity AC only	Moving parts Complex fabrication Small fields	Small range Drift Offset	Offset Drift Temperature Range

Figure 1.2: Overview of various magnetic field sensor types. XMR corresponds to several types of magneto-resistance sensors (AMR, GMR, and TMR).

require analog magnetic data. First we will cover traditional, high-precision devices, and then we will cover some trends in scaling devices to be smaller and cheaper with the hope of maintaining precision.

1.2.1 Flux Gate Sensors

Navigation and geological studies are primarily done with flux gate sensors. These consist of two permanent magnetic cores with large permeability, wrapped with conductive wire around them. A periodic field is then generated with the coil, which causes a differential permeability between the two cores. In the presence of an external magnetic field, this differential permeability will vary and can be measured as an induced voltage in a second external coil. The differential measurement enables sophisticated high precision measurements with low thermal drift, but with tradeoffs based on the magnetic core choice and frequency of operation [9]. In addition, this solution is complex and quite expensive, but remains the gold-standard for high-precision field sensing.

1.2.2 Current Sensors: Rogowski Coil/Transformers/Hall-effect with Core

A specific subclass of existing current sensors operate through magnetic field sensing. These devices will measure a magnetic field which is induced through a wire. This is based on the Biot-Savart law:

$$\mathbf{B}(\mathbf{r}) = \frac{\mu_0}{4\pi} \int_C \frac{I d\boldsymbol{\ell} \times \mathbf{r}'}{|\mathbf{r}'|^3} \tag{1.1}$$

where $\mathbf{B}$ is the magnetic field, $\mathbf{r}'$ is the distance from the current element at $d\boldsymbol{\ell}$, μ_0 is the magnetic constant, I is the induced current, and $d\boldsymbol{\ell}$ is the unit of length of the wire that is being considered over the contour integral. This simplifies in 1D to Equation 1.2:

$$\mathbf{B}(\mathbf{r}) = \frac{\mu_0 I}{2\pi r} \tag{1.2}$$

Thus, one can measure the current going through a wire by detecting the magnetic field at a known distance $\mathbf{r}$ away.

When the current flowing is alternating (AC), the induced magnetic field will form with the same frequency. This changing magnetic field can be measured with a Rogowski coil. These coils are positioned around the current wire to be sensed, with a smaller coil shaped like a toroid, which will then have smaller current induced from the changing magnetic field. This principle leverages Faraday's law: An electric field will form in the presence of a changing magnetic field. A Rogowski coil has two key advantages: it is coreless (and is not limited by ferromagnetic material saturation principles) and relatively low-cost. As a result, Rogowski coils are commonly used in power systems. However, they are large devices with fairly low sensitivity and cannot operate in low frequency regimes, as the signal would be too small, or in very high frequency regimes, where the skin depth of the current carrying wires reduce the detected field. An improvement on the Rogowski coil involves the use of a ferromagnetic core to boost the magnetic field signal, which can improve the sensitivity of the current sensor by over 10×. This can also change the output signal from a current to a voltage, pending signal processing availability.

1.2.3 Chip-scale Magnetometers

To save on cost and size, there is a trend toward miniaturization of magnetic field sensors. Since the previous technologies have scaling challenges (coils are difficult to optimize at lithographic scales due to manufacturing limits), newer transduction methods are required to enable scaled devices. These are primarily studied in semiconductors and nano-materials with magnetic-dependant quantum behavior.

MEMS: Lorentz-Force Magnetometers Micro-electro-mechanical systems (MEMS) have been around for the last 50 years. They are micro-chips, traditionally made out of silicon, which involve moving parts on the micro-scale. Typically leveraged to create mechanical timing devices and accelerometers and gyroscopes, they can also be used to detect magnetic fields. They leverage the Lorentz force, described in Equation 1.3:

$$\vec{F} = q[\vec{v} \times \vec{B}] \tag{1.3}$$

where $\vec{F}$ is the Lorentz force, q is the charge of an electron, $\vec{v}$ is the velocity of the electrons, and $\vec{B}$ is the magnetic field. A suspended beam with current passing through it will deflect in the presence of a magnetic field. This deflection can be detected in several ways, including a strain measurement through piezoresistance, a resonant frequency shift, or a gap measurement through capacitance. This is still a fairly new technology compared to other devices, and it is starting to perform with better performance compared to other micro-scale sensors [10–13]. However, they still have limitations with respect to bandwidth, range, reliability, and yield due to the moving parts of the structure.

Magnetoresistance devices A popularly-studied transduction mechanism involves using semiconductor materials that change their conductivity in the presence of a magnetic field [9, 14–16]. Various methods exist to accomplish this, which loosely fall into three different categories. The first is the anisotropic magneto-resistive method (AMR), in which a material's resistance changes based on the orientation of the magnetic field. This effect is usually measured as a small percentage of the total resistance. Next, the tunneling magneto-resistive (TMR) method has been recently shown to have incredibly high sensitivities, where the resistance values have been measured to change by factors of 10–100 times [9]. These devices operate such that the ferromagnetic layers are separated by an insulator. An external magnetic field can change the magnetic polarization of one layer, but not the other, and this will change its ability to tunnel electrons. These devices are also known as magnetic tunnel junctions for the same reason. Finally, the giant magneto-resistive method was discovered (GMR). These are comprised of stacked films which separate two magnetic layers—one with fixed polarity and one free. The free layer changes its alignment in the presence of a magnetic field which then changes the device's electron scattering properties between the two films. These devices have the potential to be high-precision sensors with very low power and low footprint. However, they struggle with a small sensing range, poor linearity, and temperature sensitivity limitations, as

well as offsets in zero fields which require active calibration and resets. In addition, they are more challenging to integrate with electronics because of their costly magnetic materials.

Integrated Circuits: Hall-effect Devices The final miniaturized magnetometer to consider is the Hall-effect sensor. These are also based on the Lorentz force, but the Hall voltage is measured in a thin conducting sheet, instead of a mechanical deflection. Edwin Hall discovered the effect in 1879 with gold foil, and its physics have been studied extensively in semiconductors in the last century. This mechanism is popular because it has many advantages—it is solid state, easy to integrate with CMOS electronics, and thus incredibly cheap to produce at large scale. In fact, Hall devices dominate sales, comprising over 2/3 of the magnetic sensing market [8] However, these devices also come with some challenges, including temperature ranges limited to those of the semiconductor, offsets, and device noise. This thesis will address some of these challenges by focusing on Hall-effect plates for harsh environments.

1.3 Hall Sensors for Extreme Environments

1.3.1 Extreme Environment Applications for Magnetic Field Sensing

There are several applications for Hall-effect devices to operate in harsh environments. In the quest to explore other worlds, instrumentation will be required to operate in extreme environments. These harsh conditions will include large doses of radiation, chemical and mechanical corrosion, and extreme temperatures. For example, the surface of Venus reaches temperatures as high as 460℃ [17]. The longest a lander has operated on this planet was the Soviet Venera 12 in the 1970s, and it only lasted 2 hours on the surface. In other exploration, the Parker Solar Probe reached temperatures as high as 1300℃ when it approached the corona [18]. There are several compelling reasons to send scientific instruments to these places. For example, Venus's orbit is within the habitable zone (much like Earth) and it has a thick atmosphere, but it has no magnetic field. It is even theorized that Venus's thick atmosphere and geology could provide insight into our own planet's future. The sun has large solar flares which create magnetic pulses with incredibly high strength, and detecting these flares early will be crucial for spacecraft survivability, so that protection protocols can be deployed before the arrival of a solar storm. In addition, the large magnetic field of Jupiter has attracted large amounts of radiation, which provides challenges for electronics sent to study its moons or inner

structure [19]. Thus, there is a need for robust electronics that can withstand these factors in long mission times and effectively operate in these challenging conditions.

There are also several ground-based challenging environments as well, as summarized in Figure 1.3. Not only do magnetometers need to operate at cold temperatures like those found on Europa and Titan in order to be used on those worlds, but they also need to do so in order to monitor power electronics that are cooled with cryogenic rocket fuel based on liquid hydrogen and helium. Higher temperature electronics will enable power electronics to also run hot to push the most power density possible, and enable sensing of magnetic fields in fusion reactors, linear accelerators, cyclotrons, and the like [20].

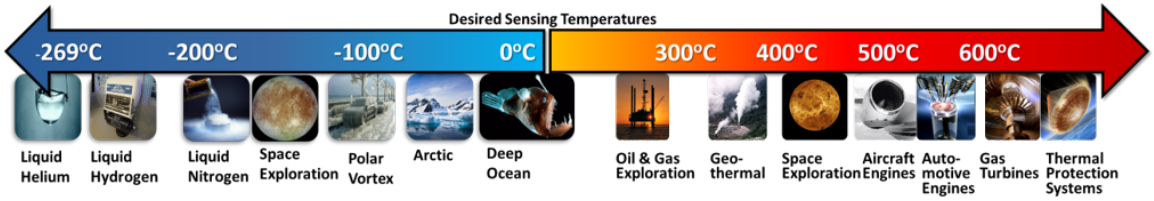


Figure 1.3: Extreme environment applications for magnetic field sensors. Adapted from [1].

1.3.2 Limitations of Silicon Devices

While Hall-effect devices are commonly made of out silicon, these devices have limitations when it comes to operating at extreme temperatures, due to the nature of the electric carriers in doped semiconductors. At low temperatures, electrons in silicon devices (with fairly low doping) will fall into the valence band of the semiconductor and become non-conducting, a phenomenon known as freeze out [21]. A silicon device doped with n-type carriers around $1 \times 10^{16}\,\mathrm{cm}^{-3}$ doping will reduce its carrier concentration by 50% at temperatures as high as -150°C, as shown in Figure 1.4. Silicon also struggles at higher temperatures: When silicon devices are heated above room temperature, the intrinsic carrier concentration ($1.45 \times 10^{10}\,\mathrm{cm}^{-3}$) will increase due to thermal activation (more electrons and holes are available to conduct), and these can actually overcome the intended doping in the material. This causes p-n junctions to cease and become simple resistors, no longer acting as the intended devices. Thus, there is a need to improve the temperature operation of Hall effect sensors.

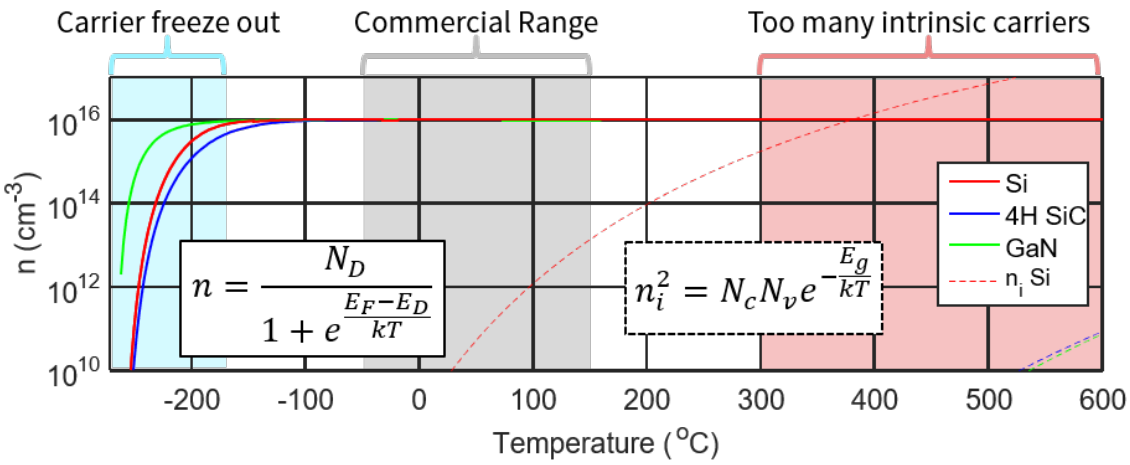


Figure 1.4: Behavior of carriers in 1×10^{16} cm^{-3}doped silicon and wide bandgap materials varied with temperature.

1.3.3 GaN's Potential for Hall Devices in Extreme Environments

Extended Temperature Operation Current strategies to enable electronics to operate in extreme environments include thick aluminum shielding from radiation and active heating and cooling to keep silicon electronics in the thermal operation regime of the device. This requires more power and adds to the payload of spacecraft or mobile systems. New robust materials can extend the operating temperature range and relax these requirements. Gallium nitride (GaN) and silicon carbide (SiC) are wide bandgap semiconductors; they are radiation hard [22] and can operate in extreme temperatures. In particular, GaN transistors (known as high electron mobility transistors) operate with a channel consisting of a thin electron sheet known as a two dimensional electron gas (2DEG). It has been shown that 2DEG mobility is extremely high (51700 cm^2/Vs) at low temperatures (13 K) [23], and can operate in regimes where silicon transistors freeze out (<100 K) [21]. In addition, GaN devices can operate at high temperatures where the silicon intrinsic carrier density is too high, as shown in Figure 1.4. In fact, InAlN/GaN transistors have operated up to 1000℃ for a duration of 25 hours [24].

Monolithic Integration GaN based electronics have potential to create several types of devices using nearly identical fabrication processing. In fact, recent work at Stanford University has led to the creation of several devices, including a high temperature transistor, UV detector, pressure sensor, micro-hotplates, Hall-effect sensors, and thermoelectric heat flux sensors (Figure 1.5) [4, 25].

The University of Michigan and Jet Propulsion Laboratory have recently led work in the creation of GaN based timing and acoustic devices with figures of merit competitive with quartz oscillators [26]. Finally, several commercial companies already have robust GaN power HEMTs and Radio Frequency (RF) devices available. Some sensor and power devices can also benefit from additional substrate machining steps to create mechanically sensitive structures, thermal isolation, and microchannels for direct liquid cooling of high power components. In order to create a temperature tolerant (>300°C), power efficient (<1 mW), small device (<25 mm^2), all these devices could be monolithically integrated together to create a single chip with multi-functional sensors, communication, and power management, such as the concept shown in Figure 1.5. This thesis covers two key themes for the this monolithically integrated GaN sensor node: substrate machining for GaN devices, and Hall-effect plates.

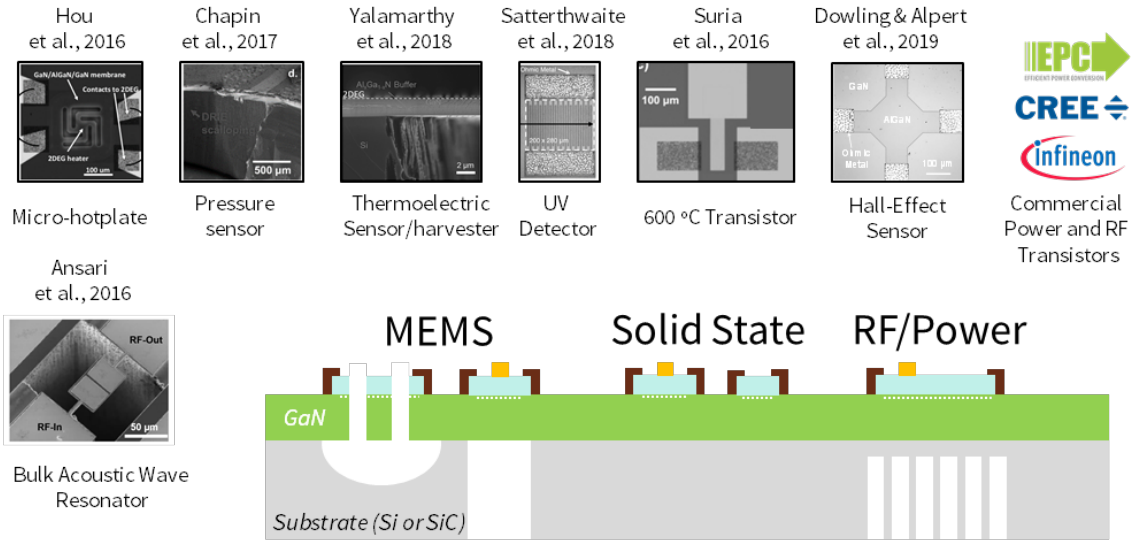


Figure 1.5: Various sensor concepts for monolithic integration of GaN devices.

1.4 Thesis Overview

This thesis will be consists of four key chapters. Chapter 2 covers the background material for micro-fabrication and Hall-effect sensor operation. Chapter 3 covers advances in micro-machining in silicon carbide and silicon. Next, the device development and characteristics of the Hall-effect GaN sensors is covered in Chapter 4. This will then be followed with Chapter 5, highlighting the

fundamental causes of offset and noise in these devices. The thesis will be concluded in Chapter 6 with suggestions for future research avenues.

Chapter 2

Background: Magnetic Field Sensors and Gallium Nitride

This chapter consists of the technical background information that is needed to understand the later thesis chapters. The first part will cover the selection of Gallium Nitride for magnetic field sensing over other available semiconductors with respect to material properties. Next, a summary of the microfabrication process of GaN devices will be provided, with in depth coverage of plasma etching, which will be covered in Chapter 3. This chapter will finish with an overview of the operation of the Hall device and key concepts will be explained, for later reference in Chapters 4 and 5.

2.1 Selection of Gallium Nitride

2.1.1 Wide Bandgap

Extreme temperature electronics can be achieved with wide bandgap semiconductors. This means the energy required to move an electron from the valence band to the conduction band of the semiconductor is three times that of Si. This is due to the higher covalent bond strength between atoms in these wide bandgap materials. The wide bandgap of GaN makes it beneficial for operation of extreme temperature electronics.

As described in Chapter 1, these materials also have much lower intrinsic carrier concentrations, as described in this equation:

$$n_i^2 = N_c N_v e^{-\frac{E_g}{kT}} \tag{2.1}$$

where n_i is the intrinsic carrier concentration, and N_c and N_v are the effective density of states for electrons and holes at the conduction and valence bands, respectively. E_g is the bandgap of the semiconductor, k is the Boltzmann constant, and T is the temperature. We can see that with a higher bandgap, the intrinsic carrier concentration is smaller. The effective density of states also depends on the effective electron and hole mass (m_e* and m_h*). We also see that an increase in T will increase n_i, which means wide bandgap semiconductors outpace typical materials. This presence of lower intrinsic carriers enables devices to operate at higher temperatures without the onset of high leakage currents, signal saturation, and non-detectable sensing.

The wide bandgap also allows these devices to operate in higher electric fields compared to their low field counterparts. Power electronics have leveraged this to create higher power density switches that block voltages 10–100× higher than equivalent devices in silicon. This enables higher efficiency power conversion systems with smaller footprint and mass. These novel, miniaturized power modules will be benefited by monolithic integrated sensors on the same chip.

2.1.2 The 2DEG: High Electron Mobility

Other wide bandgap materials are also used for high temperature and high power electronics, but GaN has an additional benefit—it can support a large electron mobility. In order to understand why this is case, we need to be able to understand how the electron carriers are available for conducting. Typical doped semiconductors have available electrons or holes: Atoms from column V or III replace silicon atoms in the crystal lattice, which require either the absorption of an electron to complete a covalent bond (making a hole) or the release of an electron to the conduction band. This process is both temperature dependent and leads to impurity scattering mechanisms in the crystal. This will cause the carrier concentration to have a temperature dependence, and limit mobility by the presence of these impurities.

Impurity scattering can be suppressed through the use of heterostructures. Through the fabrication of intricate combinations of layers with varied thicknesses, the electrons from a doped region diffuse to another region without any doping when lower energy states are available. Thus, impurity scattering is negligible. This concept was originally developed in AlGaAs/GaAs by Mimura et. al., in 1980 [27]. The confined area with a high electron density is referred to as a two-dimensional electron gas.

This concept has been extended to many different material platforms. For nitrides, AlGaN/GaN is the most popular and is the foundation for commercially available high electron mobility transistors, known as HEMTs. However, these devices do not require any doping to supply electrons to the quantum well. Instead, spontaneous and piezoelectric polarization in the GaN and AlGaN layers create a net polarization which is charge balanced with electrons that come from surface states (likely from defects or dangling bonds in the crystal surface) that fall into the quantum well to counter this polarization field.

High mobility is extremely beneficial for electronics—it allows higher switching speeds, which enables faster communication speeds (such as 5G) and smaller power electronics (passive capacitors and inductors can be smaller with higher frequency switching). This combined with larger blocking voltages is the reason GaN has such a potential to change the power electronics industry. As it turns out, this high electron mobility is beneficial for high performing Hall effect sensing, which will be seen later in this chapter.

Table 2.1 summarizes key comparisons between Si, SiC, GaAs, and GaN [28–31]. We can see that GaN has the high bandgap as well as the ability to support a large critical electric field. In addition, it has a high electron mobility compared to Si and SiC. GaAs systems may have the higher mobility, but GaN has an extended temperature range, so it is beneficial for use in harsh environments over a GaAs device.

Table 2.1: Key comparisons between Si, SiC, GaAs, and GaN.

Property	Si	GaAs	SiC	GaN
Energy Bandgap (eV)	1.12	1.4	3.2	3.4
Electrical Operation Failure (℃)	300	300	900	1000
Breakdown Field (MV/cm)	0.3	0.4	2	3.3
Electron Mobility (*2DEG)	1400	8500*	1020	2000*
Johnson Figure of Merit	1	2.7	20	27.5
Melting Point	1414	1238	2830	2500
Sensitivity / Carrier Drift (ppm/K)	300–800	160	−500–75	100–200
Seebeck Coefficient (*2DEG)	300–1500	200–300	40–100	115*

2.1.3 Micro-fabrication for GaN Sensors

Substrates for GaN

GaN has been grown on several different semiconductor substrates. Originally, GaN was deposited on sapphire substrates using an AlN interface layer to enable lattice matching between the materials, which led to the Nobel prize for the blue light emitting diode LED [32]. The GaN crystal quality is fairly high with this material system, but there are thermal issues with high power heating due to the low thermal conductivity of sapphire. Next, GaN was successfully grown on hexagonal silicon carbide, which has a very good lattice mismatch. This led to high power GaN HEMTs being commercially available, but the cost was quite high. This led to the focus of epitaxial growth of GaN on silicon (111) wafers. Silicon is a cost-effective substrate, and 6-inch wafers are readily available with decent material quality. However, the large lattice mismatch between Si and GaN (17%) means the material has a higher defect density than other mechanisms. GaN is also grown on diamond (or grown on another substrate and transferred) to increase the cooling output. However, there are several challenges with grain boundaries and thermal interfaces that are still being addressed. This thesis will discuss experiments that involve both GaN-on-Si, and 4H-SiC substrates.

Table 2.2: Summary of available substrates for GaN.

Substrate	Lattice constant (a)	Mismatch to GaN	Benefits	Challenges
GaN	3.188 Å	0%	Power electronics Vertical devices	Wafer size limitations
Sapphire	Rhombohedral (N/A)	16%	High quality Cheap	Heating issues
SiC	3.0798 Å	3%	High quality Effective Cooling	Expensive
Silicon (111)	3.83 Å	17%	Cheap Machinable	Non-CMOS Defects
Diamond	CVD (N/A)	--	High cooling	Expensive Interface issues

2.1.4 Fabrication process for GaN Devices

Micro-scale GaN devices are made using similar fabrication techniques to those of CMOS and MEMS fabrication in silicon. For GaN Hall-effect plates, this fabrication includes 2 major lithography steps (and a few more for added features).

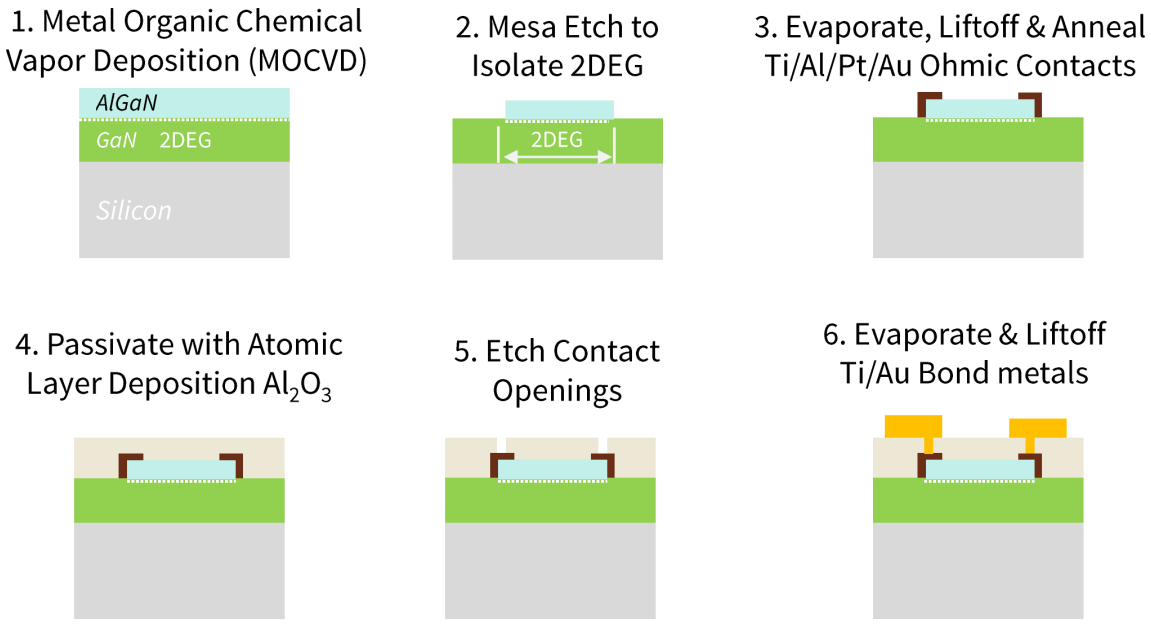


Figure 2.1: Schematic image of the fabrication process used to create AlGaN/GaN Hall-effect plates.

The general steps of the process are shown in Figure 2.1. GaN is first deposited onto a silicon wafer (or other substrate) through a process known as metal organic chemical vapor deposition (MOCVD). Next, the device conductive area is defined by the removal of AlGaN via an etch. Next, lithography is done to define the liftoff area for Ohmic metals (in our case, Ti/Al/Pt/Au), which is then annealed at high temperature to activate the Ohmic metals. Next an Al_2O_3 passivation layer is deposited using Atomic Layer Deposition (ALD), to provide protection for the device surface. This passivation doubles as a gate oxide for metal-on-insulator HEMTs (MISHEMTs), which can also be fabricated using this process. After this, openings are etched to access the Ohmic metal, and another metallization step is done to apply bond metals for the devices. These steps are described in more detail in prior work [5, 6, 33, 34].

2.1.5 Micro-machining for Si and SiC

The previous section covered a standard GaN process for creating Hall-effect devices. Even more fabrication technologies exist besides this for the creation of micro-electro-mechanical systems (MEMS). Primarily, structures that can be mechanically and electrically coupled and manipulated rely on various methods of etching. There are several techniques for etching substrates, as summarized in Figures 2.2 and 2.3.

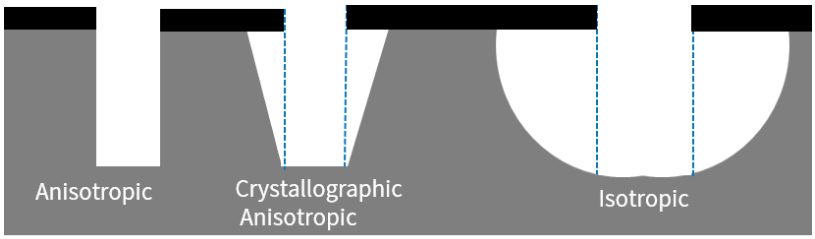


Figure 2.2: Etching types in substrates

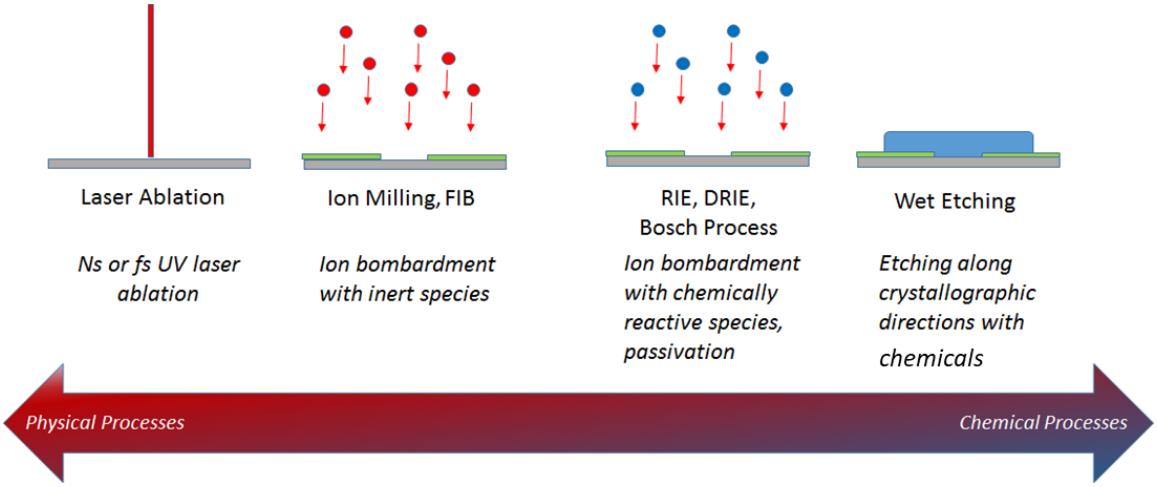


Figure 2.3: Etching processes for Silicon and Silicon Carbide, Image credit: Elliot Ransom.

Isotropic. Etchants which have no directional preference for material removal create isotropic etching processes. Several types exist for various materials. For silicon, this is done via chemical reactions, such as XeF_2 or low powered SF_6 plasma. This can be used for releasing mechanical features from the surface. This has been used to create suspended GaN microheaters, such as Hou et. al. [35]. However, these chemical reactions are much more difficult to attempt in wide

bandgap materials—so SiC processing has to be done at extremely high temperature using molten salts or with the assistance of photo-chemical etching processes. [36]

Crystallographic anisotropic. There are chemical processes which have some crystallographic preferences for etching. Based on the crystal structure, this can show preference for certain crystal planes. This is used to create structures in silicon MEMS devices that etch <100> and <110> crystal planes, but etches the <111> plane much more slowly. This was originally used to create membranes in silicon which would be useful for pressure sensing or optical uses like SiN membranes. Crystallographic etching also exists in GaN devices, but it requires high temperature acidic etching and is challenging to control.

Anisotropic. MEMS and modern 3D memory structures really took off when processing for anisotropic etching was introduced. The ability to preferentially etch vertically into a substrate with respect to the lateral direction enables many different features, such as narrow gaps for capacitive fingers, trenches for on-chip heat sinks, and vertically stacked elements for flash memory. The primary process for anisotropic etching is done with plasmas—and there are several different kinds. Silicon can be etched vertically using various plasma techniques: reactive ion etching (RIE), deep reactive ion etching (DRIE), as well as inductively coupled plasma (ICP) etching. Laser ablation can also be used to create vertically etched cavities, but it does not benefit from scaling the way wafer-level processing can achieve.

2.1.6 Inductively Coupled Plasma Etching

ICP etching operates with a few key principles. A schematic of an etcher is provided in Figure 2.4. The wafer to be etched is placed in a pressure- and temperature-controlled chamber between two electrodes. Gases (for SiC etching we use SF_6 and O_2) are fed into the gas inlet and are ionized by an RF coil. Once the plasma strikes on, ions will bombard other particles to sustain the plasma. The electrodes are then powered up to drive the ions towards the substrate and etch the wafer. Designing the plasma process takes a lot of care—every etch tool has different temperature, power, and flow rate parameters for stable processing. Once a stable process is created, it is possible to tune the plasma settings to optimize the etch process.

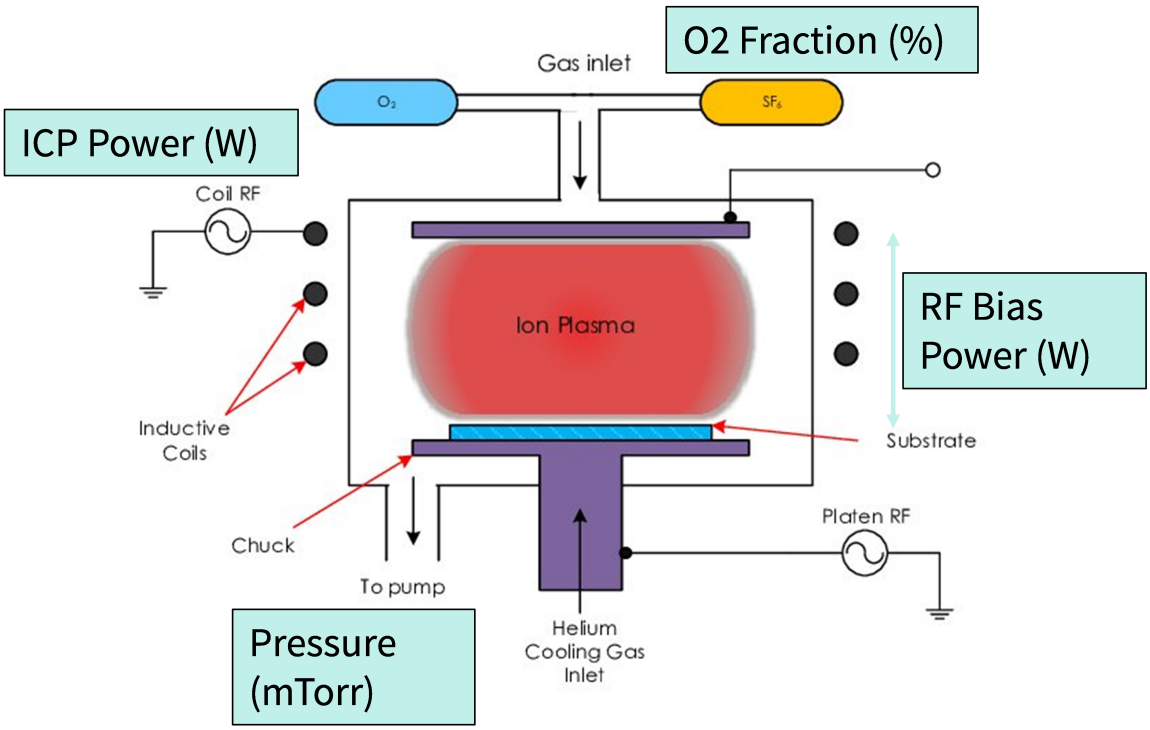


Figure 2.4: Schematic of an etcher. Image Credit: Plakhotnyuk et. al., 2016 [2].

Etch Terminology

Several characteristics can be considered in characterizing etch processes, with key ones covered in this list:

1. *Etch Rate:* This corresponds to the rate material is removed. In most cases, this rate is desired to be very fast (for bulk etching), or very slow for precise control. It is calculated using equation 2.2.

$$Rate = \frac{Depth}{Time} \tag{2.2}$$

2. *Mask:* This is the material that is patterned on the substrate, so as to protect the non-etched areas from the plasma etchants. Most masks also have an etch rate, ideally slower than the substrate.

3. *Etch Stop:* This is a material that is a barrier from the etched material—some etches terminate on this material. For example, GaN serves as an etch stop in Si DRIE for the creation of a GaN on Silicon pressure sensors. [34]

4. *Selectivity:* This is the ratio of etch rates between two materials. Usually, it is written as the ratio of the etched material to its mask or etch stop, as shown in Equation 2.3

$$Selectivity = \frac{rate_{SiC}}{rate_{mask}} \tag{2.3}$$

5. *Aspect Ratio:* This is used to understand the depth of an etch with respect to the opening width. This is usually written as depth:width, normalized for the width. For example, a 2 µm opening that is 40 µm deep will have an aspect ratio of 20, or 20:1.

Non-ideal Etch Features

There are also terms related to non ideal features that develop in plasma etching processes. These are summarized in Figure 2.5. Micropillars (also known as grassing and micromasking) can form when the mask is redeposited by the plasma (from sputtering). In addition, some etch chemistries form polymers which can deposit on the sidewalls and contribute to sidewall roughness. There are also non-ideal features that can form at corners of etched trenches, known as microtrenches. These features will be discussed more in Chapter 3.

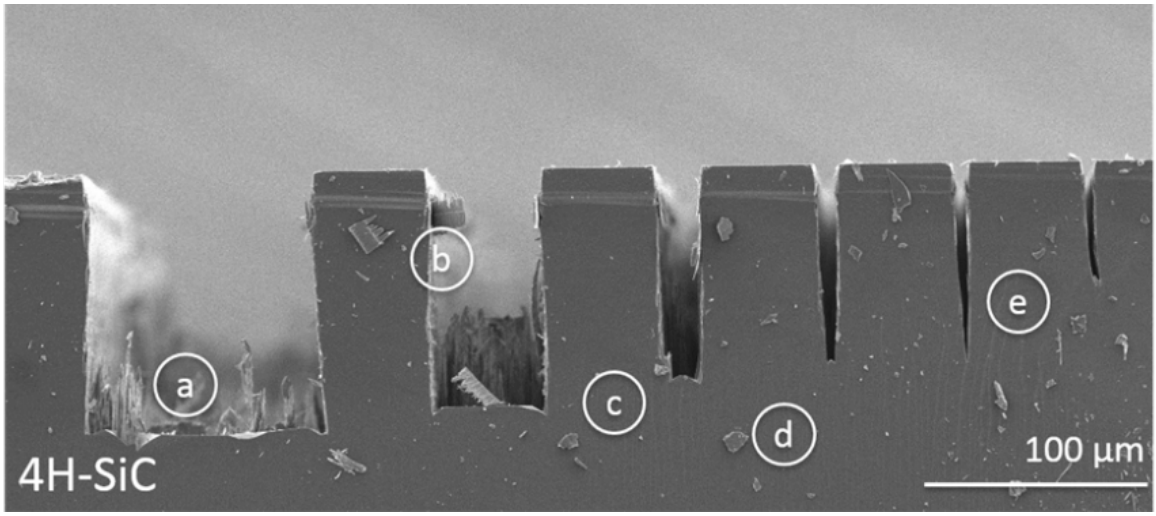


Figure 2.5: Overview of non-ideal features made in plasma processing. Image credit: Dowling et. al. [3] (a) Micropillar formation (grassing/ micromasking). (b) Polymer deposition & sidewall roughness. (c) Microtrenching. (d) Dicing debris (n/a). (e) Aspect ratio dependant etching, recognized by pinching shape "V".

2.2 Hall-effect Magnetometer Overview

The magnetometer presented in this thesis operates via the traditional Hall effect. The device has four electrodes, which are alternating sides of an octagon. When current is applied across the sensor in the presence of a magnetic field, the electrons experience the Lorentz force (Equation 1.3). Due to the presence of the magnetic field, the carriers will drift orthogonally and create another electric field, which can be measured as a voltage between the two other electrodes (V_{Hall}), shown in Figure 2.6.

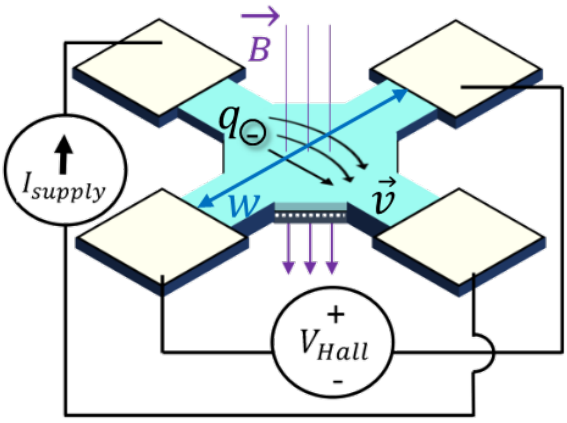


Figure 2.6: Operation of a Hall-effect plate.

When B is one dimensional and perfectly orthogonal to the Hall plate, the relationship between (V_{Hall}), and magnetic field (B) can be described in Equation 2.4:

$$V_{\text{Hall}} = vBw \tag{2.4}$$

where the velocity of the electron is v and w is the distance between the sense electrodes. The electron velocity depends on the supplied electric field E and mobility μ, such that $v = \mu E$, as long as $v < v_{sat}$. The velocity of the electrons is related to the input supply current I_s through the following relation in Equation 2.5:

$$I_s = vQg \tag{2.5}$$

where Q is the charge density of the material (C/cm^2), and $Q = n_{2\text{DEG}}q$, and g is the width of the current path. V_{Hall} can be improved through material choice (higher μ) and geometry design by changing w and parameters which alter the electric field E. E comes from an input current I_S,

associated with a supply voltage V_s. We can combine Equations 2.4 and 2.5 to create an expression for V_{Hall} with respect to input current, B field, and material constants:

$$V_{\text{Hall}} = \frac{I_s B w}{n_{\text{2DEG}} q g}. \tag{2.6}$$

In general, this expression includes the scattering factor r and shape factor G, which accounts for short circuit effects near the contacts and accounts for a reduction in V_{Hall} [6],

$$V_{\text{Hall}} = I_s \frac{B}{n_{\text{2DEG}} q} r G. \tag{2.7}$$

In these studies, r and G are neglected, since geometry factors are investigated more systematically elsewhere [6]. The experiments included in this thesis instead focus on variables which impact the Hall voltage due to inherent material properties.

Equation 2.7 can also be written with respect to the supply voltage V_s, by considering the resistance R of the structure:

$$R = \frac{1}{n_s q \mu} * (L/W)_{\text{eff}} \tag{2.8}$$

where $(L/W)_{\text{eff}}$ is the effective length-over-width ratio for a non-rectangular geometry [37], and since $I = \frac{V}{R}$ for Ohmic devices, we get

$$V_{\text{Hall}} = \mu V_{\text{supply}} \frac{B r G}{(L/W)_{\text{eff}}}. \tag{2.9}$$

2.2.1 Sensitivity

The sensitivity S of the device is defined as the change in Hall voltage with respect to the change in input magnetic field:

$$S = \frac{\Delta V_{\text{Hall}}}{\Delta B}. \tag{2.10}$$

However, as we can see in Equations 2.6 and 2.12, the sensitivity can be increased with an increase in supply current or voltage. In order to benchmark this material against others, we need to understand how μ and n_{2DEG} impact sensitivity. We can do this by normalizing S by I_s and V_s. Thus, voltage-scaled sensitivity (S_V) is described in Equation 2.11.

$$S_V = \frac{\frac{V_{\text{Hall}}}{B}}{V_s} = \mu \frac{rG}{(L/W)_{eff}} \tag{2.11}$$

To improve sensitivity for a given V_s, high electron mobility is desired. Similarly, current-related sensitivity (S_I) is described in Equation 2.12:

$$S_I = \frac{\frac{V_{\text{Hall}}}{B}}{I_s} = \frac{rG}{n_{\text{2DEG}} q} \tag{2.12}$$

In other words, low n_{2DEG} is desired to improve sensitivity when operated with a constant current. Equation 2.11 and 2.12 follow physical intuition from Equation 2.4. For a given device geometry (constant w, g, G, and $(L/W)_{eff}$), we can increase the magnetic sensitivity by increasing v. There are two ways to accomplish this velocity increase.

1. Choose high mobility materials. For a fixed electric field, electron velocity can be increased by increasing μ. This intuition can be seen in Equation 2.11. A constant V_s corresponds to constant E, so μ can be increased to improve S_V.

2. Increase electric field. The electrons flow through the device by the electric field applied to the Hall plate through V_s and I_s. When the current and mobility is fixed, V_s and E can only be increased by higher sheet resistance. This can only be accomplished by reducing the carrier concentration n_{2DEG} of the material. Thus, the intuition of Equation 2.12 holds. However, the resistance increase corresponds to higher power consumption, a common tradeoff with sensors.

Sensitivity is prone to changes of temperature. Thus, an ideal material candidate for Hall devices will have both high mobility μ, low carrier density n_{2DEG}, and low drift. GaN is a promising because candidate because of the high electron mobility in the heterostructure, the 2DEG concentration can be controlled with varied material thicknesses or voltage modulation (Figure 2.7), and because it has a very low drift in carrier concentration with temperature due to the polarization scheme for the 2DEG. While higher mobility materials exist such as GaAs (Table 2.1), GaN shows potential for high mobility operation in extreme environments with lower drift.

2.2.2 Offsets and Current Spinning

Ideally, a sensor's readout would be "zero" when the stimulus has no value. However, sensors typically measure a "false" reading in small or zero fields. Figure 2.8 depicts a typical example of signal readings with and without offset.

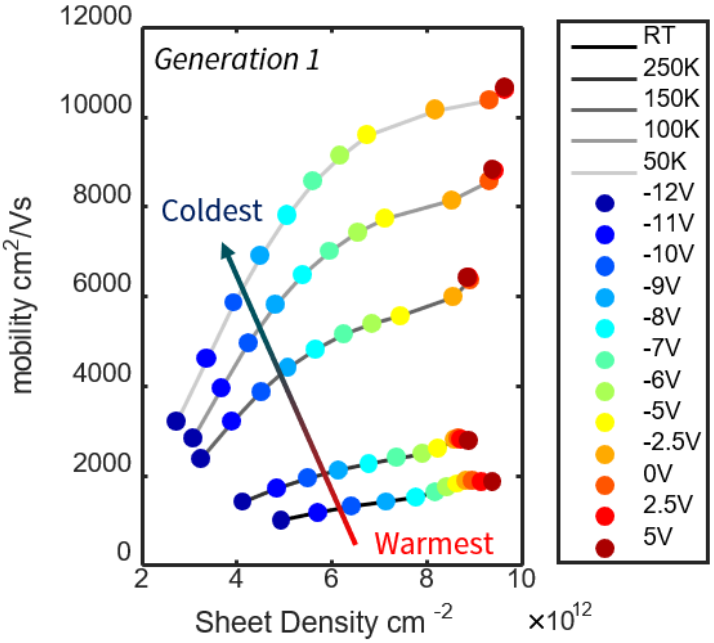


Figure 2.7: Voltage-dependant sheet density and mobility of a modulated AlGaN/GaN Hall-effect plate measured from 300K to 50K. A larger negative gate voltage V_g reduces $n_{2\text{DEG}}$. Mobility is also reduced due to scattering mechanisms. Sheet density around $V_g = 0V$ remains quite constant with changes in temperature.

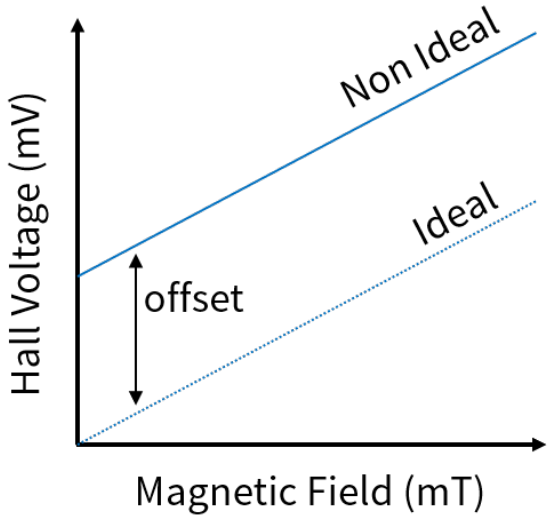


Figure 2.8: Drawing of a signal with and without offset.

Static Resistance Asymmetry and Current Spinning

Hall devices in particular suffer from large raw offsets due to asymmetries developed in fabrication and nonlinear effects that are challenging to compensate. These offsets will be referred to as raw offsets in this thesis. Raw offsets can be reduced through current spinning (also known as the spinning current method). Current spinning was first introduced by Munter in 1989 [38] to reduce offsets in silicon devices. Several techniques have been demonstrated taking advantage of device symmetry to subtract small defects and create a Hall signal with near-zero offset [39–43].

To understand how current spinning works, we can represent the device as a Wheatstone bridge with an asymmetric resistance (represented as ΔR) on one branch. In reality, all four branches will be non-equivalent, but this analysis can be superimposed in the general study. This scheme assumes a constant current supply, and voltage is measured for the offset. Through Kirchoff's voltage and current law, we can calculate the offset voltage from this resistance asymmetry.

Consider the circuit in Figure 2.9. The offset voltage corresponds to $V_3 - V_1$ for this configuration, Phase A. This will give the following:

$$V_3 = I_{supply}\left(\frac{R_{eq}}{2R}\right)R, \quad V_1 = I_{supply}\left(\frac{R_{eq}}{2R+\Delta R}\right)R, \text{ where } R_{eq} = \frac{2R(2R+\Delta R)}{4R+\Delta R}. \tag{2.13}$$

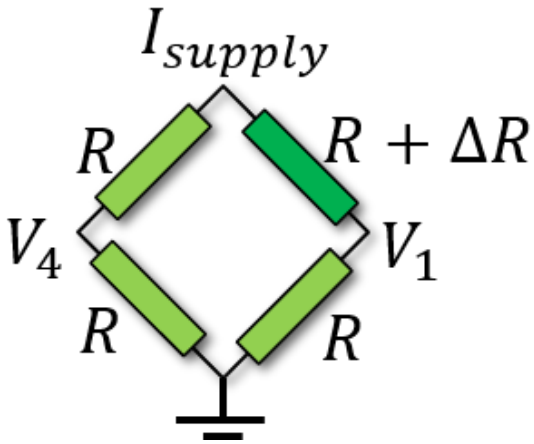


Figure 2.9: Phase A of Wheatstone bridge model for Hall plate.

So we get:

$$V_{offset_A} = I_{supply} R_{eq} \left(\frac{2R + \Delta R}{4R + 2\Delta R} - \frac{2R}{4R + 2\Delta R} \right) = I_{supply} R_{eq} \left(\frac{\Delta R}{4R + 2\Delta R} \right). \tag{2.14}$$

The same device can be measured with the contacts for source and sensing configured by 90°on the same device, shown in (Figure 2.10). The offset in Phase B will correspond to $V_4 - V_2$.

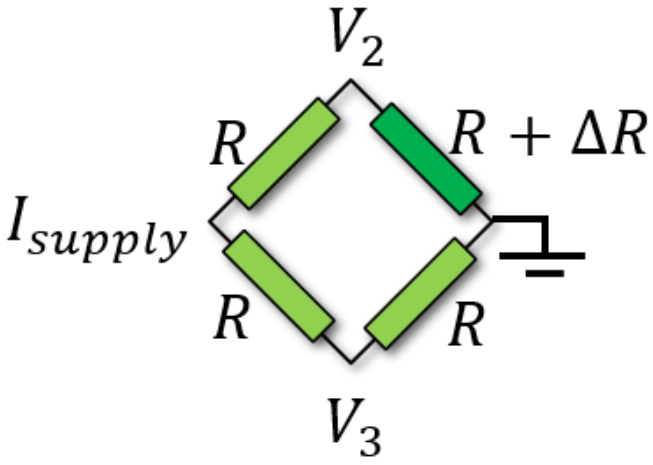


Figure 2.10: Phase B of Wheatstone bridge model for Hall plate

This will give the following:

$$V_4 = I_{\text{supply}} \left(\frac{R_{eq}}{2R}\right) R, \quad V_2 = I_{\text{supply}} \left(\frac{R_{eq}}{2R+\Delta R}\right)(R+\Delta R), \text{ where } R_{eq} = \frac{2R(2R+\Delta R)}{4R+\Delta R}. \tag{2.15}$$

Which leads to:

$$V_{offset_B} = I_{supply} R_{eq} \left(\frac{2R+\Delta R}{4R+2\Delta R} - \frac{2R+2\Delta R}{4R+2\Delta R}\right) = I_{supply} R_{eq} \left(\frac{-\Delta R}{4R+2\Delta R}\right). \tag{2.16}$$

In this simple bridge model, it is clear that V_{offset_A} and V_{offset_B} have equivalent magnitude, but opposite sign. This means static and linear resistance asymmetries can be canceled with current spinning in an Ohmic device. In our work, these raw offsets are on the order of mT in magnitude. Current spinning removes these offsets, and offsets on the order of 0.5–11 µT remain afterwards.

The 4-phase spinning scheme used in this thesis is shown in Figure 2.11. Eight configurations are used, each 90° rotated from the previous, with the last 4 phases identical to the first four with the hall voltage polarity measured in a new direction, as summarized in Table 2.3. This method does increase measurement time and power consumption by 4 to 8×, but the offset reduction is typically improved by 100 to 1000times. Modern CMOS circuits can implement current spinning without the need for substantial power and speed budgets [44].

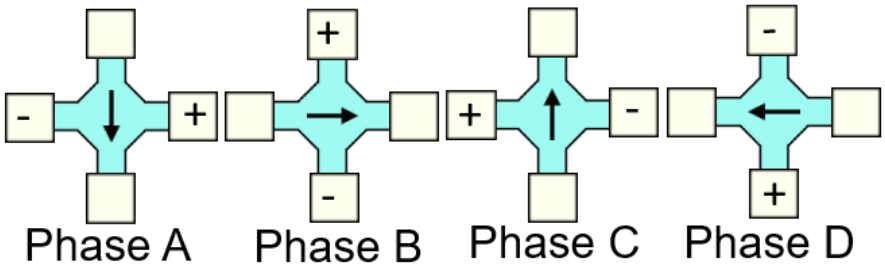


Figure 2.11: Schematic of current spinning. One 4-contact device is measured in 4 unique configurations, and the results are averaged to remove offset.

Equation 2.17 dictates the computation to average all 8 configurations:

$$V_{Hall} = \frac{1}{8}\left(\Sigma_{i=A+}^{D+} V_{Phase_i} - \Sigma_{i=A-}^{D-} V_{Phase_i}\right) \tag{2.17}$$

Table 2.3: Current spinning phases for all 8 configurations

	I+	I−	+Meas	−Meas
A+	N	S	E	W
B+	W	E	N	S
C+	S	N	W	E
D+	E	W	S	N
A−	N	S	W	E
B−	W	E	S	N
C−	S	N	E	W
D−	E	W	N	S

This removes offsets from the device as well as the measurement equipment. In Chapter 4, only 4-phase current spinning is mentioned, but it follows this 8-phase sequence. Fundamentally, only 4 phases are needed if the offset of the measurement equipment is properly considered [45]. Equation 2.17 can be used to remove the raw offsets and keep only the magnetic induced Hall voltage. In the presence of no magnetic field, this computation measures residual offsets.

Equivalent Magnetic Offset

Raw and residual offset voltages can be expressed as magnetic offsets through a simple conversion shown in Equation 2.18:

$$B_o = \frac{V_o}{S} = \frac{V_o}{S_I I_s} = \frac{V_o}{S_V V_s} \tag{2.18}$$

Essentially, if the magnetic sensitivity is known, the equivalent magnetic offset can be calculated. This is useful to compare various magnetic sensing technologies against each other. Similarly, noise floors can be estimated as a magnetic field through a similar computation.

Residual Offsets

Current spinning is a well-established method for removing raw offsets in Hall-effect plates, but the residual offsets remain challenging to remove from measurements. While residual offsets are small, they limit the measurement detection of sensors without careful calibration. The key sources of residual offset are as follows:

1. External Causes: Stray fields in measurement setups and packages will be read as an offset measurement. These can be constant fields or vary as a function of the supply current. Measurement equipment noise and induced voltages from switching can also cause offset errors.

2. Intrinsic Causes: Residual voltages which do not cancel with current spinning due to their mobile nature. This can include thermal gradients from self-heating and resistance asymmetries related to input supply power.

Chapter 4 presents residual offset data from two different device generations, and Chapter 5 will go in depth into several sources of residual offset.

2.2.3 Noise Sources in Hall effect devices and systems

During these measurements, system noise can interfere with the offset measurements. Thus, several repeated offset measurements are taken and averaged to find the true offset. This is shown in Figure 2.12. In this example, 300 current spinning measurements are taken and averaged to find the true offset voltage. Since this value is close to zero, the standard deviation of these measurements is much higher than the mean. Thus, a confidence interval is calculated for the samples by taking the standard deviation and normalizing with the square root of number of measurements. The number of samples N needed for statistically confidence measurements is dictated by the noise of the system (2.19).

$$C = \frac{\sigma(V_{offset})}{\sqrt{N}} \tag{2.19}$$

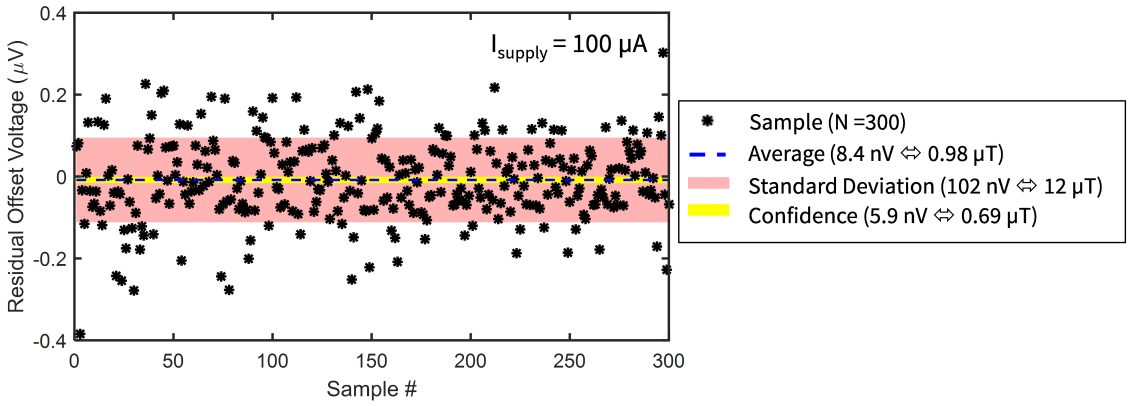


Figure 2.12: Example of current-spun measurements on the same device. Noisy measurement equipment leads to the need to average 100s of measurements for one device under the same conditions.

Thus, when it comes to magnetic field sensors, noise is very important to understand. Noise can come from many different sources in a system. Electronics fundamentally have challenges with noise, and so any processing circuit, measurement amplifier, and wiring can contribute.

There are several sources of noise in semiconductors. First, thermal noise is known to be a uniform power spectrum. This noise is due to thermal fluctuations in carriers. It is also known as Johnson noise, and sometimes referred to as white noise. This noise cannot be removed and represents a fundamental limit of electronic measurements. The power spectral density can be represented by this equation:

$$PSD_{\text{thermal}}\left(\frac{V^2}{Hz}\right) = 4k_bTR \tag{2.20}$$

where k_b is the Boltzmann constant, T is the temperature, and R is the resistance of the device. Second, there is noise known as generation-recombination noise. This is due to carriers falling into and out of energy traps in the semiconductor. Electrons can occupy and vacate these traps with a measurable time constant related to the energy level of that trap. These G-R traps thus follow a power spectrum which is related to the time constant [46].

A third noise source is known as flicker noise, or "$1/f$" noise, due to the power spectral densitys inverse relationship with frequency. This noise is known to empirically exist, but it is still not clear what the fundamental physical mechanism behind it is. Frederik Nicolaas Hooge (F.N. Hooge) developed the first empirical model to describe the $1/f$ behavior [47,48], which follows this equation:

$$PSD_{\text{flicker}}\left(\frac{V^2}{Hz}\right) = V^2\frac{\alpha_H}{N}\frac{1}{f^\gamma} \tag{2.21}$$

where f is the frequency, V is the input voltage, N is the total number of carriers (which can also be expressed as a carrier density multiplied by the volume or area, unit pending), γ is the logarithmic slope of the $1/f$ portion of PSD, and α_H is a unitless scalar known as the Hooge parameter. The Hooge parameter was initially believed to be a constant regardless of semiconductor materials of 2×10^{-3}, but it was later shown to vary drastically with materials. Hooge wrote a response to his original findings in the early 1990s to address this [48], but did not update his model. Others have also worked to quantify $1/f$ noise behavior through models involving things such as traps and trap distribution in silicon CMOS devices [49]. However, there is still little consensus between models and experiments—several experiments can point to either theory. Others have tried to unify these models with coupling, but these models have little benefit over the separate approaches [50].

Figure 2.13 shows a sketch of the noise power spectral density seen in sensors. There is a low frequency portion with a slope related to γ from the flicker noise, and a frequency-independent portion at higher frequencies, which is known as the thermal noise floor. The corner frequency is the crossing point between these two regimes. The Hooge parameter can be extracted with the y-intercept of the log graph. These noise parameters computations will be described in detail in Chapter 5.

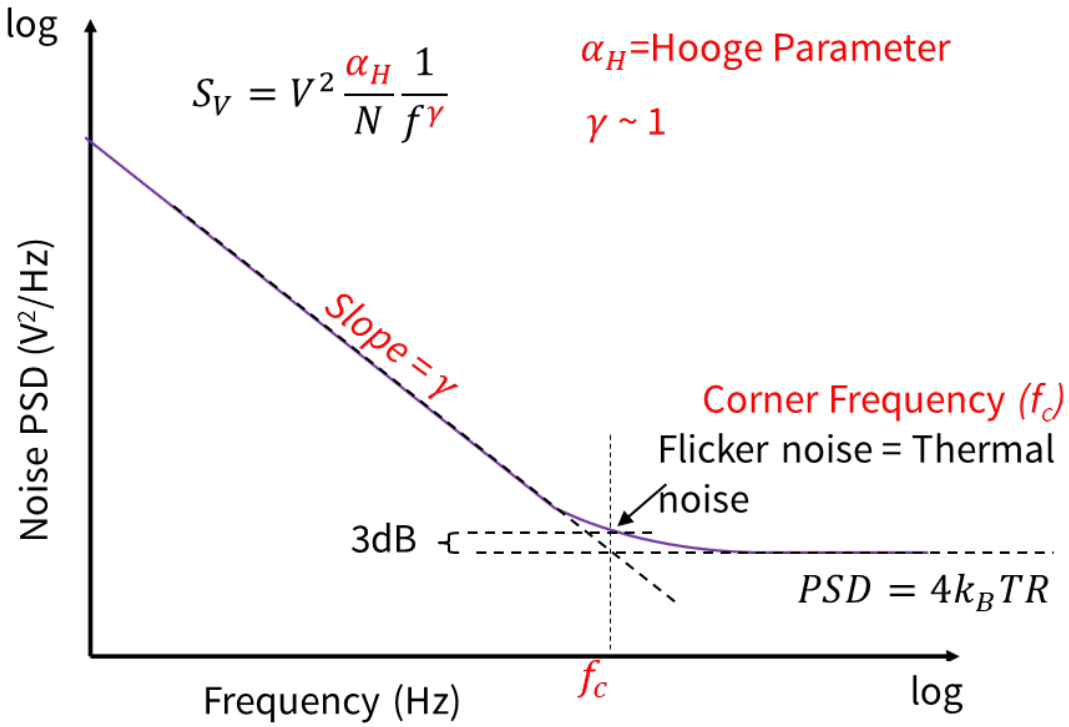


Figure 2.13: Parameter extraction methods for $1/f$ noise characteristics.

Several integrated circuit techniques exist to remove $1/f$ noise from circuits, and it is less of a concern for commercial products. Chopping and averaging are two popular methods [51]. Our standard current spinning approach actually does both (we flip the multimeter sign in phases 5–8 to correct for multimeter noise, and we take several measurements and average to remove noise). However, current spinning works best when the spinning frequency is higher than the corner frequency of the devices. Thus, the $1/f$ components can also be canceled through spinning [44]. Devices thus with a low thermal noise floor and low corner frequency are thus ideal for simplified Hall device

operation. (Low spin frequencies are easier than higher ones.) The noise characteristics of the GaN-based Hall-effect sensors will be covered in Chapter 5.

Chapter 3

Machining Substrates for Gallium Nitride: SiC and Si

3.1 Overview

This chapter will cover progress in micro-machining of substrates for Gallium Nitride in both ICP etching and laser ablation. As described in the second chapter, there are several substrates which GaN is deposited on through MOCVD. This work was previously published in the proceedings of the IEEE International Conference on Microelectromechanical systems in 2015 [52], the ASME Technical Conference and Exhibition on Packaging and Intergration of Electronic and Photonic Microsystems (InterPACK in 2015) [3], and IEEE Journal of Microelectromechanical Systems in 2017 [53], and Microelectronic Engineering Journal in 2017 [54].

3.1.1 Introduction

Complex 3-D microstructures (sensor, actuator, and microfluidic devices) made from Si, Ni, and polymer materials (e.g., PMMA) have been fabricated using deep reactive-ion etching (DRIE) [55, 56], lithography, electroplating, and molding (LIGA) [57]. This is enabled through the high selectivity (above 300:1 for Si to SiO_2) and fast etch rates (up to 10 µm/min) of DRIE, as well as the high aspect ratio (1.5 µm x 350 µm) of LIGA processes [56, 57]. However, Si, Ni and polymer materials are limited to benign operating conditions due to their low melting points, fatigue under high cycles

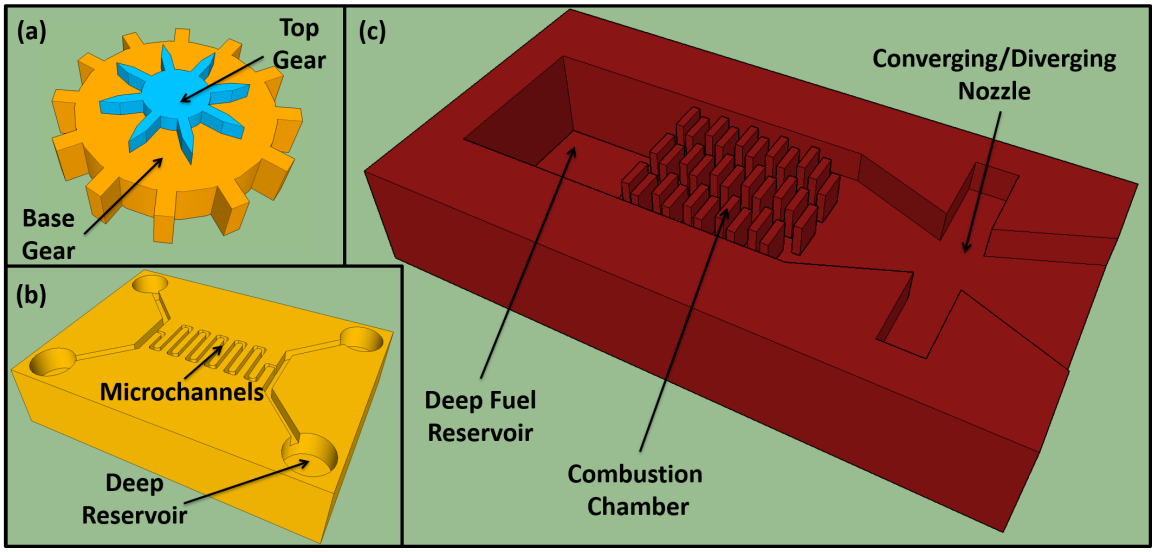


Figure 3.1: Schematic image of robust 3-D SiC microstructures that are enabled through a multilayer mask process: (a) stacked mechanical gears, (b) bio compatible, heat-tolerant, and transparent microchannels, and (c) robust microthrusters.

of wear, and susceptibility to chemical corrosion. Thus, SiC has been investigated for microstructure design due to its inherent thermal stability, chemical inertness, and wear resistance [36]

3-D features have been previously made in polycrystalline SiC using a 3-D patterned Si mold and high rate atomic pressure chemical vapor deposition (AP CVD) [58]. However, it is desired to bulk micromachine single-crystalline SiC to leverage its electrical properties and high thermal conductivity. 3-D fabrication techniques for single-crystalline SiC have yet to be demonstrated and will aid in the realization of robust microstructures that can operate within extreme harsh environments such as micro-scale combustion systems, microchannels for hot fluids, and wear-prone mechanical structures (Figure 3.1).

Previous efforts in bulk SiC micromachining have focused on development of inductively coupled plasma (ICP) based etches using fluorine, chlorine, and bromine chemistries [59–62]. In addition, photoelectrochemical etching has been used to etch n-type 3C-SiC and has reached etch rates as high as 100 µm/min [63] but shows poor directionality, which is required for many MEMS components [61]. Femtosecond laser irradiation has been shown as a maskless technique to pattern deep (up to 350 µm) via holes [64]. In addition, tremendous work has been done in improving the via hole plasma etching of SiC, but these efforts have been for sub-1:1-aspect-ratio features [65]. G. Beheim et al. have carefully characterized the effects of etch rates with respect to many plasma etch parameters with an indium tin-oxide mask to obtain etch depths over 100 µm [66]. Large depths ($>$ 200 µm) and

high aspect ratio (> 10:1) features have also been demonstrated using an electroplated Ni mask, and opening widths of 10 µm and 50 µm up to 250 µm [67]. Recently, new mask candidates have been considered such as AlN [68]. This work demonstrates a multilayer mask etch process to create 3-D microstructures in 4H-SiC substrates. The fabrication process for three experiments is described and the results are presented. First, the SiC etch rate and mask selectivity for three materials (Ni, SiO_2, and Al_2O_3) are studied at varying plasma bias powers. Additionally, aspect ratio dependent etch characteristics are presented with 5 µm to 110 µm opening width variation. Finally, a gallery of high resolution images of fabricated 3-D structures (mechanical gears, Lego®-like bricks, and poker chips) on a transparent and robust 4H-SiC substrates is shown for the first time. The use of 4H-SiC as a structural material enables such microstructures to be utilized under high cycles of wear, within elevated temperatures, and within chemically corrosive environments unlike common MEMS structural materials [36].

3.1.2 Fabrication

A 4H SiC substrate (Cree Inc.) was used for this experiment. Due to the high cost of the SiC substrates, dies of 1 cm by 1 cm were used for the experiments. Before processing, SiC samples underwent a piranha clean (H_2SO_4:H_2O_2, 9:1). Next, the samples were rinsed sequentially in deionized water, acetone, methanol and isopropanol. The samples were processed with one or two stages of standard 1:1 contact photolithography to perform the etch selectivity study, observe the aspect ratio dependent etch rate, and create the 3-D structures. The SiC plasma etch (PlasmaTherms LL-ICP Metal Etch System) baseline recipe selected for this work used 1000 W ICP power, 50 W of RF bias power, 5 mTorr of pressure, 9:1 ratio of SF_6/O_2 gas chemistry, and a total flow rate of 60 sccm.

Etch Rates and Mask Selectivity

Three types of etch masks were used for this study: evaporated Ni, plasma enhanced chemical vapor deposition (PECVD) SiO_2 and plasma atomic layer deposited (ALD) Al_2O_3. Ni (200 nm) was evaporated and lifted-off from photoresist patterned 4H-SiC. ALD Al_2O_3 (60 nm) was deposited at 250℃on 4H-SiC using a plasma ALD process (Ultratech/Cambridge Nanotech Fiji System). It was then patterned with photoresist and plasma etched (PlasmaTherms LL-ICP Metal Etch System) with BCl^3 chemistry comprising a total flow rate of 50 sccm, at an etch rate of 45 nm/min. PECVD SiO_2 (2 µm) was deposited at 350℃on 4H SiC, photoresist was patterned, followed by an etch in an ICP etch system (PlasmaTherms LL-ICP Oxide Etch system) with an O_2/CHF_3 chemistry at

an etch rate of 0.2 µm/min. Once all the etch masks were patterned, the 4H-SiC was etched with the selected SiC etch baseline recipe and then etch rates for RF bias power values of 25, 50, 100, 150 and 200 W were investigated. The selectivity is obtained by calculating the ratio of etch rates of 4H-SiC to the etch masks for the same parameters. Using a stylus-based profilometer (Tencor Alphastep 500), the SiC etch depth was determined for a given time with the mask. The Ni mask was removed and the sample re-measured, to calculate the final thickness of the mask. The difference of this provides the etch depth of the Ni mask from which the Ni etch rate is determined. This technique was previously used by K. Williams et al. in 1996 [69]. The SiO_2 selectivity was measured by processing a Si wafer with 2 µm deposited in the plasma etch for 1 minute, and the SiO_2 film thickness was measured before and after using an optical profilometer (Nanospec 010-180). The ratio of the SiC etch rate to SiO_2 etch rate gives the SiC:SiO_2 selectivity. The thin Al_2O_3 film was completely removed within 1 minute of plasma etching and as a result, the selectivity was estimated using the ratio of SiC etch depth to the starting thickness of Al_2O_3 [70]. Etch rate and selectivity were measured in three to five consistent locations across the 1 cm^2 SiC die, and data is presented with the average and standard deviation of those measurements.

Aspect Ratio Dependent Etch Rate

To investigate the effect of opening dimensions on the etch rate of 4H-SiC, the dies were patterned with a mask design that had several opening dimensions using standard lithography. Ni (200 nm) was evaporated as described earlier with a 10 nm Ti adhesion layer. Next the same sample was evaporated with an additional 500 nm of Ni and 10 nm Ti adhesion layer, making a total mask thickness of approximately 750 nm. This metal was lifted off to serve as the etch mask for this investigation. PlasmaTherms ICP Metal etch system was utilized to etch the 4H-SiC 3 D structures. The recipe used a 1000 W ICP power, 50 W of RF bias power, 7 mTorr of pressure, 9:1 ratio of SF_6/O_2 and a total flow rate of 60 sccm. The sample was etched for 90 minutes with an average large opening etch rate of approximately 0.6 µm/min. The sample was then imaged using variable pressure scanning electron microscopy (Hitachi S-3400N SEM) to characterize the aspect ratio dependent etch rate.

3-D Etching using Multilayer Etch Masks

The fabrication process used for the development of 3-D microstructures is presented in Figure 3.2. Post dehydration (hot plate at 115°C for 10 minutes), the sample was coated with a 2 µm thick PECVD SiO_2 film at 350°C. Following this, the sample underwent a standard lithography process.

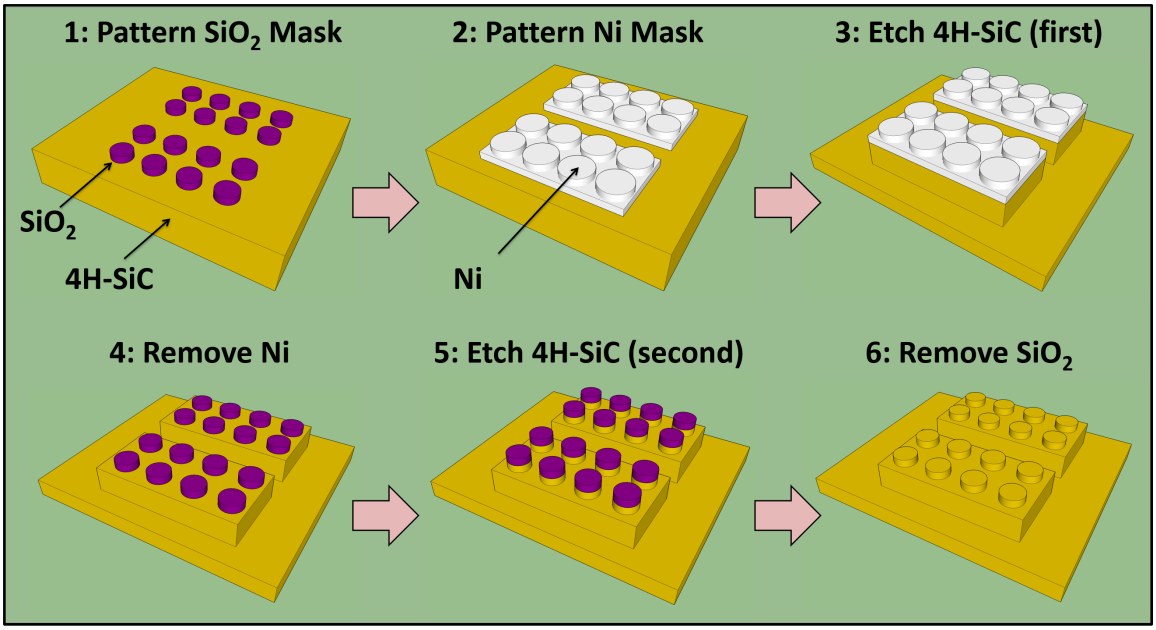


Figure 3.2: Schematic image of the plasma etch process with multilayer masks (Ni and SiO_2) used to create 3-D microstructures in 4H-SiC.

The SiO_2 thin layer was patterned using photoresist as an etch mask. ICP etching was used to etch the 2 µm PECVD SiO_2 layer. Another iteration of standard lithography was performed onto which 200 nm of Ni is evaporated and lifted-off.

To perform the first level of the complex SiC etch patterning, SF_6/O_2 chemistry was used. The baseline ICP etch recipe was used to etch the 4H-SiC 3-D structures to 10 µm. The sample was then dipped in a nickel etchant (Transene Company, Inc.) to remove the leftover Ni mask. Next the sample was etched for a second time to 1 µm, using the patterned SiO_2 as the mask. The remaining SiO_2 was stripped using a wet etch with hydrofluoric acid (49% HF). The samples were then imaged using SEM.

3.1.3 Results

Etch Rates and Mask Selectivity

As mentioned previously, three etch masks were used in this investigation: evaporated Ni, PECVD SiO_2, and ALD Al_2O_3, and were chosen due to their high etch selectivity. Figure 3.3 shows the etch rate of 4H-SiC and the SiC to hard mask selectivity values for varying plasma bias power. A SiC etch rate as high as approximately 1 µm/min was observed at a bias power of 150 W and a lower end

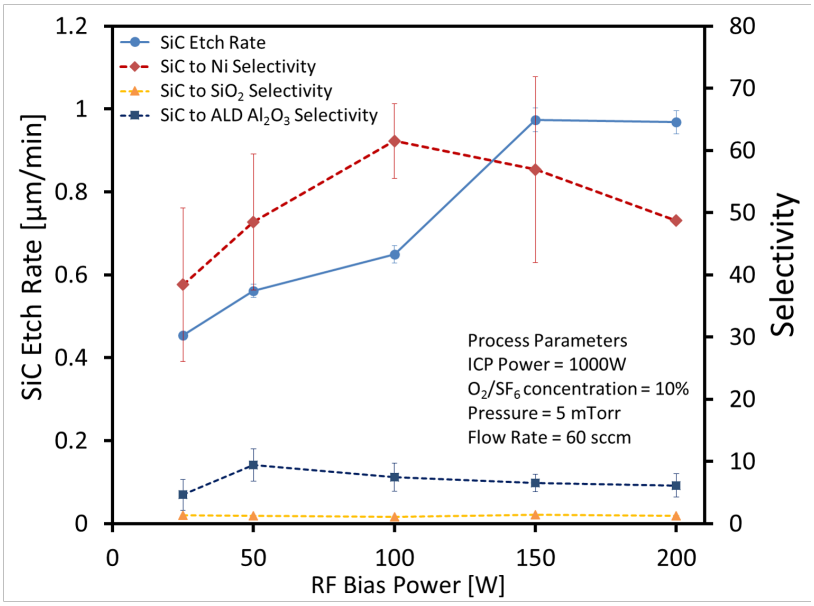


Figure 3.3: Measured 4H-SiC etch rates and mask selectivity with respect to RF bias power for three etch masks (evaporated Ni, PECVD SiO_2 and ALD Al_2O_3

etch rate of about 0.45 µm/min at a bias power of 25 W. In addition, a SiC to Ni etch selectivity of 60:1 and an etch rate of 1 µm/min were obtained at a RF bias power of approximately 100 W and approximately 150 W, respectively. Furthermore, a decrease in selectivity is observed at higher bias power. These results agree with previous SiC etch studies [66, 71]. A SiC:SiO_2 selectivity ratio of 1:1 was observed, which is near the expected selectivity [66]. In addition, the etch characterization showed SiC to ALD Al_2O_3 selectivity values between 5:1 and 10:1, surpassing typical selectivity values for SiO_2 ($<$ 3:1). These preliminary results show that ALD Al_2O_3 is promising as a mask for multilayer SiC etching. The moderate selectivity can be leveraged when a diversity of masks are needed for complex microstructures.

Aspect Ratio Dependant Etch Rate

An aspect ratio dependent etch was observed for feature openings between 5 µm and 110 µm. Figure 3.4 shows the SiC etch rate dependence on opening width, and a SEM of trenches with opening widths varying from 7 µm to 50 µm. As expected, there is a decrease in etch rate (and overall etch depth) with a decrease in starting opening feature. This trend has been widely reported in Si etching literature [56] and SiC etching literature [67]. Additionally, there is an open area saturation value of etch rate, where larger openings will etch nominally at the same rate. To obtain high aspect ratio

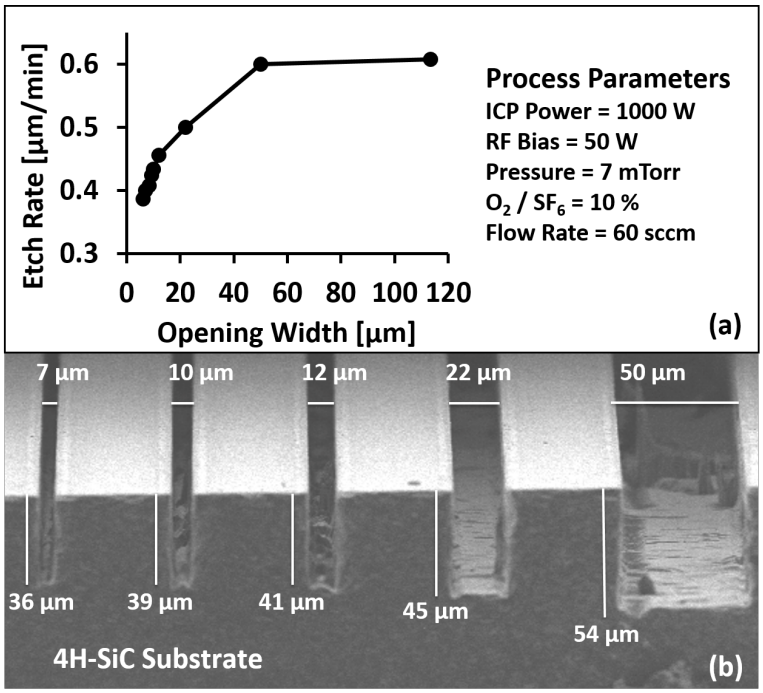


Figure 3.4: Measured 4H-SiC etch rates and mask selectivity with respect to RF bias power for three etch masks (evaporated Ni, PECVD SiO_2 and ALD Al_2O_3

trenches, the modified etch rate must be considered for starting mask feature size. Additionally, there are observable pointed features in the corners of each channel due to microtrenching [66], and these features converge in narrow trenches over longer etch times.

3-D Etching using Multilayer Etch Masks

The examination of the selectivity and aspect ratio dependent etch rates enable a set of etch recipes to realize 3-D etch structures using multilayer masks. An array of structures (stacked gears) micro-fabricated in a transparent, 1 cm^2 4H-SiC substrate is shown in Figure 3.5. Figure 3.6 presents an image gallery of the first complex microstructures (mechanical gears, a Lego-like brick, and a poker chip) created in 4H-SiC using multilayer mask etching. The base features of these structures have a height of 10 µm and the top features are 1 µm tall. The structures in Figure 3.6a to Figure 3.6c were etched using the baseline SiC plasma etch recipe shown in Figure 3.3 with a bias power of 50 W. Figure 3.6d, the poker chip, was etched using a 100 W bias power, and shows rough artifacts on the etch surface due to micromasking [62]. The nickel mask is sputtered and redeposited on the etch surface creating non-desired roughness. This roughness can be avoided by using reduced bias

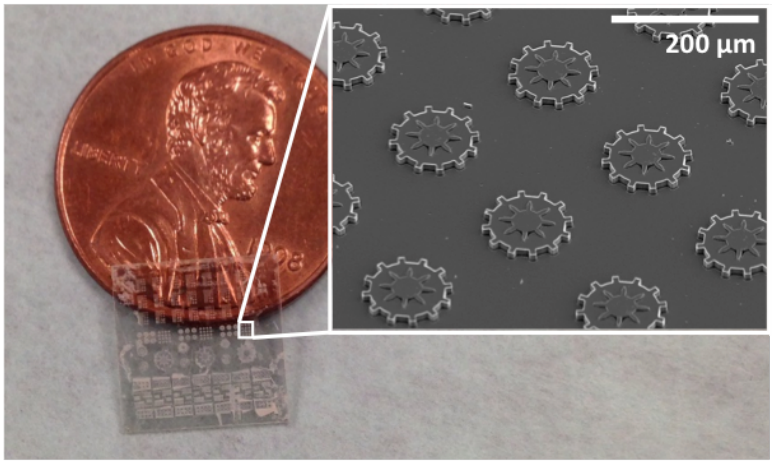


Figure 3.5: Image of a 1 cm^2 4H-SiC die (optically transparent) that was used to microfabricate a variety of microstructures with inset showing SEM of gear array with minimal micromasking.

powers. Overall, these results demonstrate the potential to create 3-D structures in SiC from use of multilayer masks.

3.1.4 Conclusions

This work shows the effect of plasma RF bias power on the 4H-SiC etch rate and selectivity to various etch masks including evaporated Ni, PECVD SiO_2 and ALD Al_2O_3. A SiC to Ni etch selectivity of 60:1 and an etch rate of 1 µm/min were obtained at a RF bias power of 100 W and 150 W, respectively. These results agree with previous SiC etch studies [66,71]. In addition, we observed an aspect ratio dependent etch, with a maximum depth achieved of 54 µm. Finally, we presented the first 3 D structures made in SiC using this multilayer mask etching technique. It is suggested that future work be performed to create 3-D features using multilayer etch masks including ALD Al_2O_3 and to demonstrate ultra-deep (above 100 µm) 3-D features in SiC.

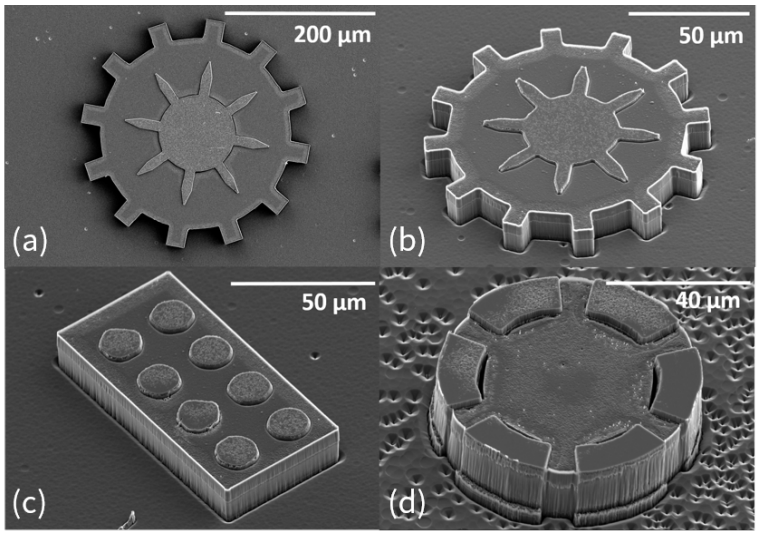


Figure 3.6: SEM gallery of various 4H-SiC 3-D microstructures created using this multilayer mask technique: (a) top-view of 300-µm-diameter gear stack, (b) 100-µm-diameter gear stack, (c) Lego-like brick, and (d) poker chip.

3.2 Inductive Coupled Plasma Etching of High Aspect Ratio Silicon Carbide Microchannels for Localized Cooling[†]

3.2.1 Introduction

Gallium nitride (GaN) transistors used in high power and high frequency electronics generate power densities as high as 10 W/mm during operation which leads to temperature rises as high as 200°C and can decrease reliability [72–74]. As a result, a reduction in the peak temperatures of hot spots generated on-chip is required to increase operation lifetime. Silicon carbide (SiC) substrates are often used in the design of GaN-based electronics due to its high thermal conductivity (370 W/m-K), and can be leveraged to reduce device channel temperatures. The thermal conductivity of SiC drastically reduces with an increase in temperature [75], so the use of SiC alone is not sufficient to reduce hot spot temperatures. As a result, one vision is to locally integrate microchannels and cooling fluid into the SiC substrate to decrease device channel temperatures during operation. This allows the use of both convective and conductive heat transfer to reduce overall temperature of the

[†]© The American Society of Mechanical Engineers. Originally published as Karen M. Dowling, Ateeq J. Suria, Yoonjin Won, Ashwin Shankar, Hyoungsoon Lee, Mehdi Asheghi, Kenneth E. Goodson, and Debbie G. Senesky. Inductive Coupled Plasma Etching of High Aspect Ratio Silicon Carbide Microchannels for Localized Cooling. In *Volume 3: Advanced Fabrication and Manufacturing; Emerging Technology Frontiers; Energy, Health and Water-Applications of Nano-, Micro- and Mini-Scale Devices; MEMS and NEMS; Technology Update Talks; Thermal Management Using Micro Channels, Jets, Sprays*, page V003T07A006. ASME, 7 2015.

system and increases local cooling [76]. It is approximated that channel temperatures can remain below 110°C using this integrated cooling architecture [77]. However, advanced manufacturing and packaging techniques are required to realize such an on-chip cooling system.

Silicon (Si)-based microchannel heat exchangers have been demonstrated in the past with various geometries to perform thermal cooling [78–82]. However, Si has low thermal conductivity which limits power density and generation of material defects in the thin film device layers (due to large lattice mismatch) causes increased leakage currents. In addition to Si, SiC substrates, although costly, have been utilized in the development of SiC-based and GaN-based power electronics devices. However, creating fin-like, high aspect ratio features in SiC is challenging due to slow plasma etch rates (0.2 µm/min to 1 µm/min) and poor selectivity to etch masks in comparison to well established plasma etch techniques for Si substrates. In addition, previous work in plasma etching of SiC has primarily focused on the manufacturing of large via holes and feature sizes greater than 50 µm [66]. There are reports of 10 µm width trenches with depths of 110 µm, creating a 11:1 aspect ratio [67] and trench widths of 13 µm and 7.6:1 aspect ratio in 6H-SiC [83]. However, there is little reported on etching features with narrow opening widths below 10 µm and large depths (higher aspect ratios) in SiC. This work focuses on the development of high aspect ratio features in SiC with narrow openings widths as low as 4 µm.

This paper presents numerical analysis of the thermal behavior of high aspect ratio 4H-SiC microchannel heat transfer properties and experimental results of microfabrication of high aspect ratio SiC microchannels. First a finite element model is presented to approximate expected hot spot temperatures generated for various aspect ratio microchannel geometries. In addition, the impact of inductively coupled plasma (ICP) etch parameters on etch rate, selectivity and topography are investigated to assist in the realization of deep, high aspect ratio microtrenches in SiC. Finally, a gallery of SEM images of SiC microchannels with varied aspect ratios (13:1 to 5:1) is presented to observe aspect ratio dependent etch features. The integration of SiC microchannels for hot spot cooling (Figure 3.7) could enable high power density platforms and improve device reliability.

3.2.2 Fin Efficiency Analysis

Fin efficiency is a common metric to analyze microchannel arrays used in thermal management applications. We analyzed multiple fin array geometries that were then fabricated in bulk 4H-SiC. The model assumed rectangular and long ($>$ 400 µm) channels. The efficiency of a single fin is

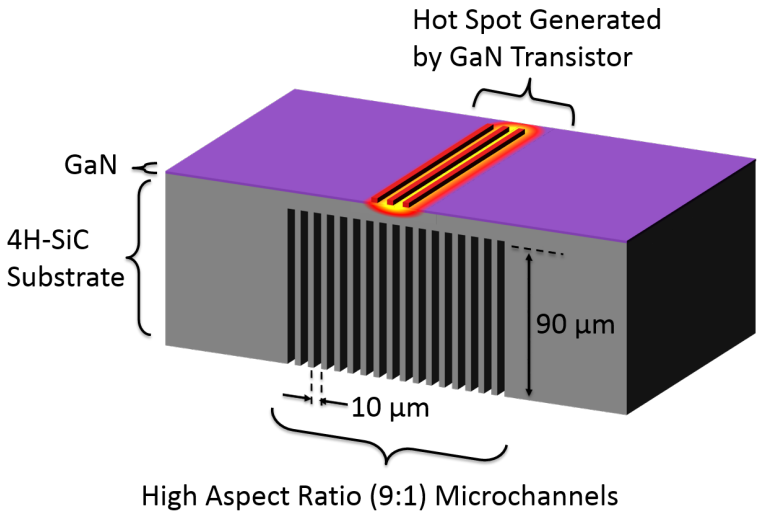


Figure 3.7: Schematic illustration of high aspect ratio 4H-SiC trenches used for localized cooling of hot spots generated by high power operation of GaN transistors.

commonly known to be [84]:

$$\eta_{fin} = \frac{\tanh(mL)}{mL} \tag{3.1}$$

as described by Equation (3.1), where L is the lenght of the fin plus half the fin thickness, and m is defined as:

$$m = (\frac{2h}{kt})^{\frac{1}{2}} \tag{3.2}$$

in Equation (3.2), h is the heat transfer coefficient, t is the fin thickness, and k is the thermal conductivity of the SiC substrate. In additon, the overall fin efficiency of an array of microchannels is expressed as:

$$\eta_o = 1 - \frac{NA_{fin}}{A_{total}}(1 - \eta_{fin}) \tag{3.3}$$

where A_{fin} refers to the surface area of one fin, N is the number of fins, and A_{total} is the total surface area of the heat exchanger. Equation (3.3) can be expressed as a function of fin spacing g, in-plane fin length l and A_{fin}:

$$\eta_o = 1 - \frac{NA_{fin}}{N(A_{fin} + gl)}(1 - \eta_{fin}) \tag{3.4}$$

Thus, it becomes clear that smaller spacing between fins leads to higher fin efficiency, and therefore higher improvement in thermal cooling. Detailed hot spot temperatures presented in the following

section are obtained based on a simple 1D analysis using the overall fin efficiencies which can be expressed as shown in Equation (3.5):

$$T_{hotspot} = Q(\frac{1}{\eta_o h A_{total}} + \frac{t_{base}}{k A_{base}}) + T_{inlet} \tag{3.5}$$

where Q, t_{base} and A_{base} are the input power, thickness of SiC substrate and the total channel base area, respectively.

3.2.3 Hot Spot Temperature Computation

A simulation was performed using COMSOL® Multiphysics software to account for the thermal resistances associated with the heat source, spreader, and heat exchanger. COMSOL® Multiphysics software solves for the temperature field as the solution to the steady-state heat conduction equation. The device in the simulations includes 1.5 µm GaN, 10 µm SiC substrate, and 90 µm height SiC fins (see Figure 3.8a). An array of 20 transistor gates in the quarter device is modeled as the hot spot generator. As boundary conditions, heat fluxes are given to the gates (2 µm x 175 µm x 20 in the quarter device). A range of heat transfer coefficients from 100 to 600 kW/m^2-K is imposed to the fin walls. Symmetry boundary conditions are used to account for the quarter device. The fluid temperature is 25°C and total power to the system of 50 W is used for the hot spot temperature simulation. The simulation accounts for the material properties and device dimensions for each layer to solve the conduction equations where the thermal conductivity of GaN and SiC is the function of temperature. (i.e. $GaN(T) = -0.1623T + 214.17$, T (in K); $SiC(T) = 0.0038T2 - 4.1734T + 1259$, T (in K) < 600 K). The grid size is about from 1 to 10 µm depending on the fin width. It should be noted that the convergence error is set to 10^{-4} for 210,000 elements.

Figure 3.8b compares the junction temperature using two different methods of 3D COMSOL Multiphysics for four different channel widths of 4, 10, 20, and 30 µm with 90 µm channel depth and the 1D conduction model using fin analysis for the corresponding channel configurations. Here we imposed a constant heat transfer coefficient of 450 $kW/m^2 - K$ for difference channel sizes of 4 to 30µm in COMSOL simulation. In reality, the effective heat transfer coefficient is larger for a smaller channel, which will improve the impact of small hydraulic diameter. This finite element modeling has confirmed that smaller channel and fin widths leads to lower hot spot temperatures and improved device cooling. Also, the 3D COMSOL simulation shows good agreement to 1D solid conduction model with fin analysis for corresponding channel size.

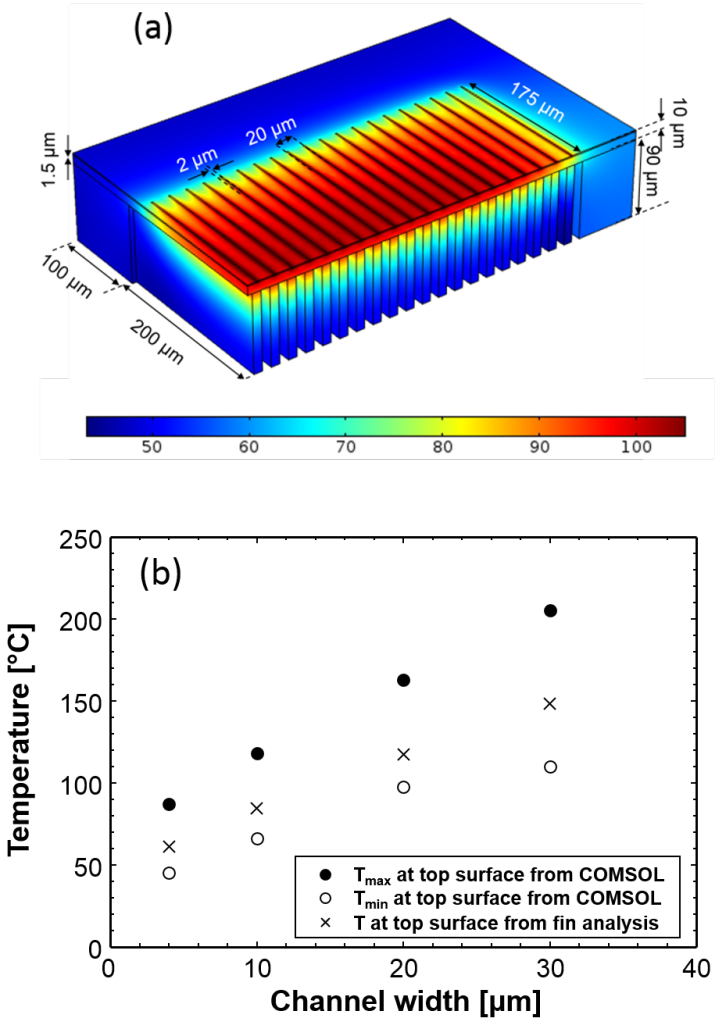


Figure 3.8: (a) An example of the conduction simulation result using 3D COMSOL® Multiphysics. The color map shows the temperature distribution (°C) of SiC heat exchanger with a power to the system of 50 W and heat transfer coefficient of 450 kW/m^2-K. The fin width is 10 µm and fin pitch is 20 µm. (b) Hot spot temperature (maximum and minimum) variation with respect to fin width for an array of GaN High-electron-mobility transistors (HEMTs) being cooled with SiC microchannels.

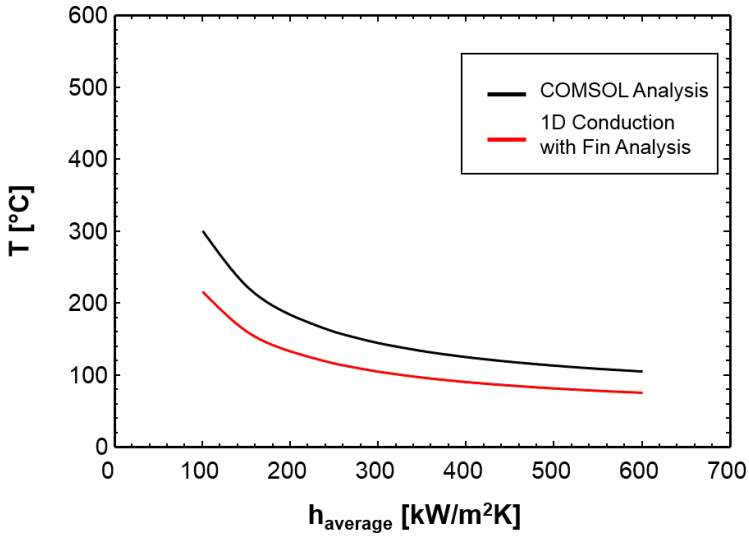


Figure 3.9: Maximum hot spot temperature for 10 µm channel width, 10 µm fin width and 90 µm channel depth with varying convective heat transfer coefficient.

In Figure 3.9, the hot spot temperature from the simulation and overall fin efficiencies are evaluated for an appropriate range of constant heat transfer coefficients, h = 100 to 600 kW/m^2-K. These heat transfer coefficients are obtained from both single-phase conjugate computational fluid dynamic (CFD) simulations and relevant two-phase boiling correlations using methanol as a working fluid [76]. The channel geometry analyzed is an array with 10 µm channel width, 10 µm fin thickness and 90 µm channel depth. The hot spot temperature significantly decreases with increasing heat transfer coefficients. For example, the hot spot temperature is about 300°C with an h of 100 kW/m^2-K where the hot spot temperature decreases to 100°C with an h of 600 kW/m^2-K. The averaged hot spot temperature is also obtained using 1D solid conduction with fin analysis for a heat transfer coefficient range of h = 100 to 600 kW/m^2-K. The temperatures from fin analysis are under-predicted compared to hot spot temperatures obtained from COMSOL simulation because two-dimensional effects are not considered in fin analysis. However, the difference is weakened as the heat transfer coefficient increases and the temperature reaches asymptotic point because fins are no longer effective at very high heat transfer coefficients.

3.2.4 SiC Microchannel Fabrication Process

To experimentally verify the predicted increase in fin efficiency and decrease in hot spot temperatures due to high aspect ratio SiC microchannels, fabrication of actual high aspect ratio microchannels

with similar geometries in 4H-SiC is required. In this work, microchannels were fabricated using a double-sided-polished, high purity semi-insulating 4H-SiC substrate with a resistivity above 105 Ω-cm (Cree Inc. supplier). Samples with a size of 1 cm by 1 cm were used for experiments due to the high cost of 4H-SiC substrates. To clean the 4H-SiC samples, a 30 minute immersion in piranha (H_2SO_4:H_2O_2, 9:1) followed by a rinse in deionized water and acetone, methanol, and isopropanol was performed. Next, a standard 1:1 contact photolithography process was used to pattern photoresist and print features of various opening widths (4 µm to 100 µm).

To perform the etch characterization experiments, a 200 nm Ni film was thermally evaporated and patterned using a lift-off process to serve as an etch mask. The bare SiC substrates were then etched in 10 minute cycles using PlasmaTherms LL-ICP Metal Etch system. A baseline recipe with an ICP power of 1000 W, RF bias power of 100 W, chamber pressure of 5 mTorr, SF_6/O_2 gas chemistry with 9:1 ratio, and total flow rate of 60 sccm was utilized. In this investigation, the RF bias power was varied between 25 W and 200 W. The etch rate and SiC:Ni etch selectivity were also observed. In addition, the etch rate was characterized between the pressures of 4.7 mTorr and 10 mTorr. Each 10 minute etch was measured using a stylus-based profilometer (Alphastep 500) on a 1 mm by 1 mm etch area. The etched Ni film was calculated from the difference in step heights before and after Ni removal by a wet etchant. The selectivity of SiC:Ni was calculated using a ratio of SiC etch rate with respect to Ni etch rate.

To create high aspect ratio microchannels, a thick (> 200 nm) Ni mask is required to maintain masking during the relatively deep etch. The microfabrication process is described in Figure 4. To microfabricate the thick Ni mask, a 50 nm gold film was evaporated and patterned using a lift-off process. Etch opening features between 4 µm and 100 µm were utilized to study the impact of narrow features on etch rate, selectivity, and profile. Ni was then electroplated with a thickness of approximately 1.5 µm using a Watt's bath chemistry [85] to create the etch mask. It should be noted that the conformal nature of the electroplating process causes further narrowing of the etch opening. To create the high aspect ratio features, the 4H-SiC substrate was then etched using the baseline recipe and RF bias power of 50 W. Since narrow trench openings require an increased etch time due to reduced mass transfer into trenches during the plasma etch process [52], these samples were etched in the range of 2.5 to 4 hours to reach depths from 50 to 100 µm for mask opening widths of 4 to 100 µm.

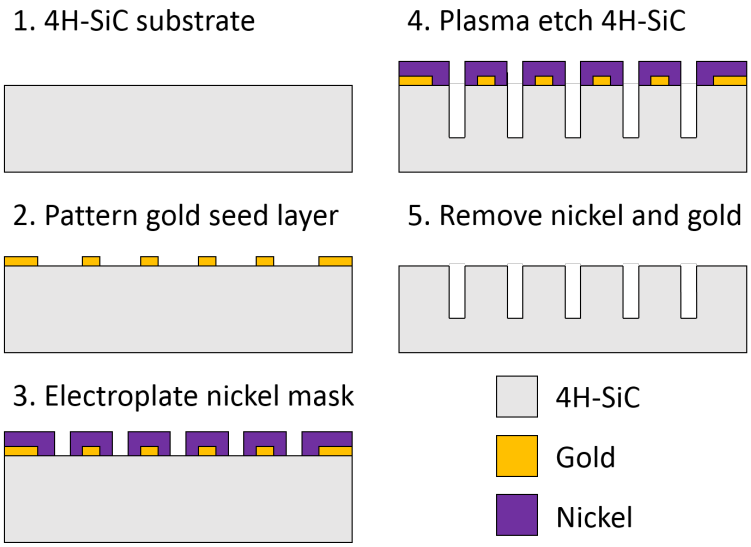


Figure 3.10: Microfabrication process used to manufacture high aspect ratio SiC microchannels using an electroplated Ni mask.

3.2.5 Plasma Etch Characterization Results

To obtain high aspect ratio channels, it is important to first characterize the etch rate and selectivity obtained from the plasma etch recipe with respect to various plasma conditions. While there are many important plasma parameters (e.g. ICP power, gas chemistry, temperature, etc.), RF bias power and chamber pressure are of particular interest for the realization of deep channels with narrow (<10 µm) opening width. A high SiC:Ni selectivity is desired in addition to high SiC etch rate. The effect of RF bias on etch rate and selectivity is shown in Figure 3.11a. A SiC:Ni selectivity of approximately 60:1 (highest value for this study) and an etch rate around 0.6 µm/min was observed at an RF bias power of 100 W. Figure 3.11b shows the effect of etch chamber pressure on the SiC etch rate. For the range of pressures studied in this work, the highest etch rate (0.72 µm/min) was obtained at lower pressures (approximately 5 mTorr). To create the high aspect ratio features in SiC the baseline recipe with a pressure of 5 mTorr and an RF bias power of 50 W were utilized. It should be noted that an increase in chamber pressures (10 mTorr) can also lead to higher etch rates due to higher plasma density, but this should be further investigated to observe the limits in the high aspect ratio regime. In addition, the limits of mass transport in narrow areas [62] may require etching at reduced pressures (increased mean free path).

It is well known that the feature opening size (i.e. aspect ratio) also affects the etch rate of the substrate. Figure 3.12 shows the effect of trench opening size on the overall depth of the microchannel. The results show that narrower openings result in a reduced etch rate (44% decrease from 100 µm to 4 µm openings). This is due to a reduction in mass transfer. In addition, in the wide opening sizes (above 10 µm) etch artifacts are observed. For example, the micromasking effect caused by sputtering and re-deposition of the Ni etch mask [62] caused grass-like structures in large open areas. However, at etch openings below 10 µm (Figure 3.12), no micromasking is observed. Sidewall roughness is another feature that was observed in the SiC microchannels, which may have been caused by organic polymer growth on the sidewall during etching [66]. In addition, micro-trenching (increased etch rates at the corners of the trenches) was observed and may have been caused by sidewall ion bombardment [66].

3.2.6 High Aspect Ratio SiC Microchannel Results

This microfabrication process developed in this work aims to investigate the etch behavior of narrow features with opening widths below 10 µm to support integrated microchannel technology in SiC. The etch topography of the microchannels in Figure 3.12 (varying widths between 100 µm to 4.5 µm) resulted in aspect ratio dependent etch depths and etching artifacts, as well as aspect ratio dependent micro-trenching. Low aspect ratio trenches ($<$ 9:1) show two distinct micro-trenches at the trench edge: a "W" shaped channel. On the other hand, the high aspect ratio trenches ($>$ 9:1) narrow to a"V" shaped channel. This aspect ratio dependent micro-trenching appears in repeated arrays of microchannels, shown in Figure 3.13a. In addition, the high aspect ratio channels ($>$ 12:1) in Figure 3.13b have narrower width at the bottom of the channel versus the top opening. This is due to changes in the etch behavior at deeper etch depths. As the channel gets deeper, the etch rate decreases due to limited mass transport of the plasma to the bottom of the narrow trench. It should be noted that these narrow channels show some sidewall curvature, which may be due to the cleaving and SEM imaging process or isotropy effects from the low bias plasma

Large arrays of SiC microchannels have been microfabricated using the ICP etching processes studied here. Figure 3.14a shows an array of 25 microchannels that are 47 µm deep, 800 µm long, with an aspect ratio of 5:1. These channels show similarity in shape, depth, and overall appearance in comparison to previous DRIE etching in Si [55]. The array of 12 high aspect ratio channels (8:1), shown in Figure 3.14b are 38 µm deep and greater than 1000 µm long demonstrating that the features from this process are scalable even at high aspect ratios. The manufacture of actual SiC

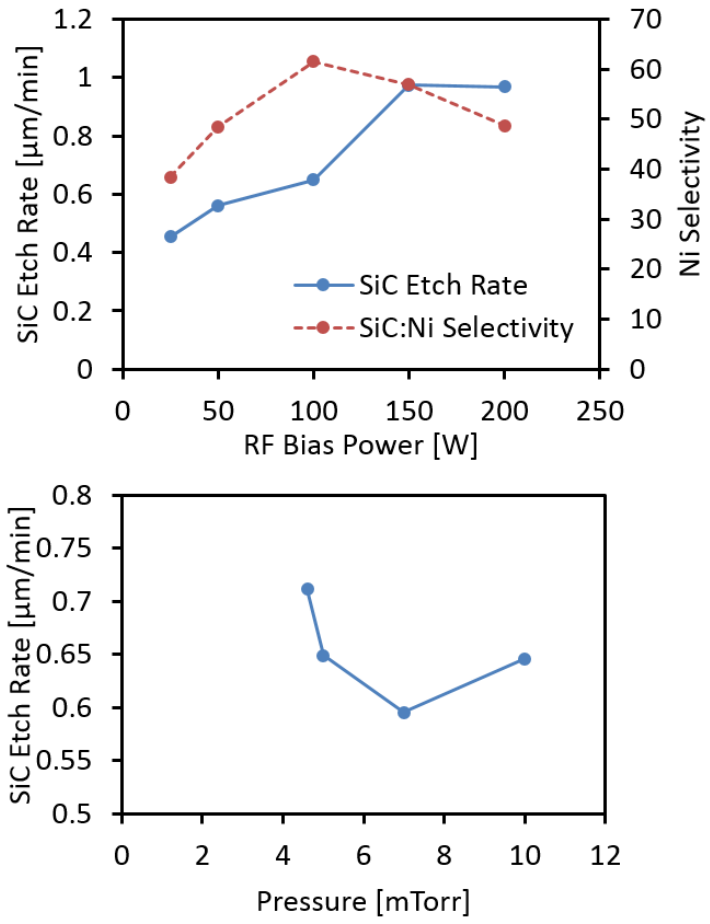


Figure 3.11: SiC etch rate versus varying plasma parameters. (a) SiC etch rate versus RF bias power and (b) SiC etch rate versus etch chamber pressure. The baseline plasma etch parameters used are ICP power of 1000 W, RF bias power of 100 W, chamber pressure of 5 mTorr, O_2/SF_6 ratio of 10% and total flow rate of 60 sccm.

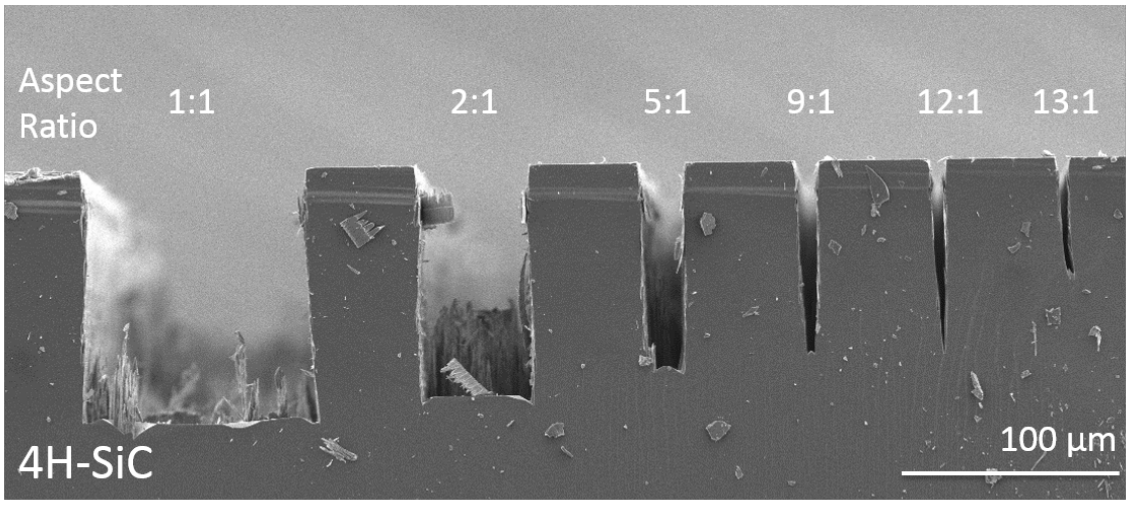


Figure 3.12: SEM image of ICP etched 4H-SiC microchannels with various mask opening widths.

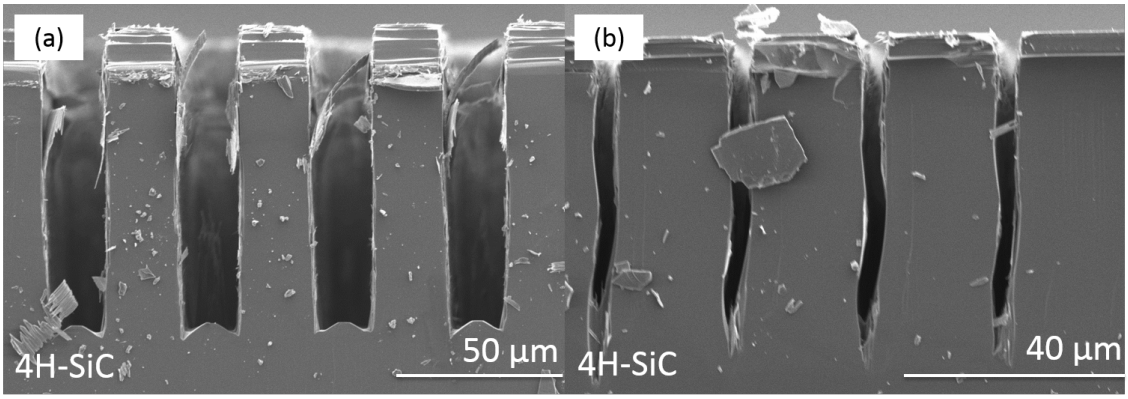


Figure 3.13: SEM images of ICP etched 4H-SiC microchannel arrays. (a) Wide channels (20 µm) have lower aspect ratio channels (4:1) and show microtrenches at channel corners in a "W" shape. (b) High aspect ratio SiC channels (12:1) with narrow opening widths (4.7 µm) have reduced etch depth and thinned profiles in a "V" shape.

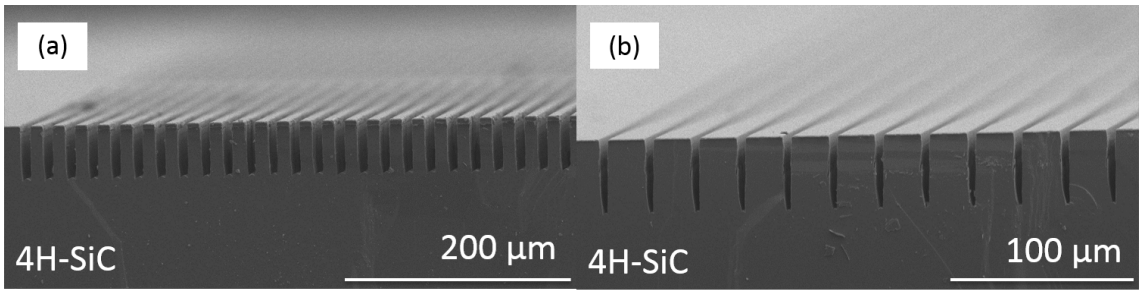


Figure 3.14: SEM images of high density arrays of high aspect ratio SiC microchannels. (a) 8.5 µm wide, 47 µm deep microchannels with aspect ratio of 5:1. (b) 4.5 µm wide, 38 µm deep microchannels with aspect ratio of 8:1.

microchannel arrays with high aspect ratio features supports the development of future micro-scale cooling architectures in SiC substrates.

A summary of the microchannel arrays fabricated in 4H-SiC substrates and estimated hot spot temperatures are shown in Table 3.1. As mentioned previously, the resulting hot spot temperatures were estimated using the fin efficiency analysis. However, it should be noted that these approximations do not take the aspect ratio dependent features (e.g., the "W" and "V" etch bottom shapes) into account. Heat transfer coefficients at the channels are assumed to be constant at 450 kW/m^2-K and the averaged hot spot temperatures are obtained based on a 1D conduction model with fin analysis (Equations 3.1–3.5). The high aspect ratio channels (geometries #2 and #3) have higher hot spot temperatures in comparison to low aspect ratio channels (geometries #1 and #4) because they have larger fin widths. Therefore, thin fin widths, in addition to high aspect ratios, are desired for integrated microcooling technology.

Table 3.1: Summary of SiC microchannel dimensions fabricated and hot spot temperature analyzed with fin efficiency calculations. Device surface cooling area is assumed constant at 1.5 µm long, so number of fins varies.

Geometry #	Depth (µm)	Width (µm)	Fin Width (µm)	Aspect Ratio	Hot Spot Temperature (°C)
1	47	8.5	10	5:1	102.5
2	38	4.5	19.5	8:1	139.8
3	58	4.7	21.5	12:1	115.6
4	90	20	20	4:1	119.1

3.2.7 Conclusion

Fin efficiency of thermal heat exchangers increases with high aspect ratio geometries and if such features are realized in SiC, through advanced manufacturing, they can improve power device reliability. Finite element and numerical computation showed a reduction in surface hot spot temperature with decreased fin and channel widths. In addition, the microfabrication of high aspect ratio microchannels in 4H-SiC with dimensions that are suitable for microcooling of on-chip hotspots has been reported. More specifically, this work demonstrated SiC microchannel fabrication with aspect ratios as high as 12:1 with depths of 51 µm. In addition, low aspect ratio features with depths as high as 110 µm were obtained. Furthermore, fabrication and topography of high density arrays of over 20 microchannels with aspect ratios of 5:1 and 12 microchannels with aspect ratios of 8:1 were shown. In the future, this high aspect ratio, SiC-based microfabrication process could be implemented to create convective heat exchangers for on-chip cooling of high power GaN and SiC electronic devices, as well as robust microfluidic systems.

3.3 Profile Evolution of High Aspect Ratio Silicon Carbide Trenches by Inductive Coupled Plasma Etching[†]

3.3.1 Introduction

Silicon carbide (SiC) has been developed into a microelectromechanical systems (MEMS) and power electronics platform for use in a variety of harsh environment applications where traditional silicon (Si) based platforms must be heavily packaged or actively cooled [36, 61, 86, 87]. When compared to Si platforms, bulk SiC and thin film SiC materials provide increased radiation hardness, temperature tolerance, and chemical inertness [36]. In addition, the wide bandgap (3.2 eV) and high breakdown field (>1 MV/m) of SiC-based devices make them well suited for high-power applications where Si devices are limited by reduced breakdown voltage levels and generation of thermal carriers [88]. However, these robust properties also mean that SiC is far more difficult to micromachine [36] compared to Si substrates. Si processing for MEMS through deep reactive ion etching (DRIE) and similar techniques has created features with aspect ratios as high as 250:1 [89] at etch rates as fast as 20 µm/min [90]; there is no directly comparable process for SiC substrates.

[†] © 2017 IEEE. Reprinted, with permission, from K.M. Dowling, E.H. Ransom, and D.G. Senesky. Profile evolution of high aspect ratio silicon carbide trenches by inductive coupled plasma etching. *Journal of Microelectromechanical Systems*, 26(1), 2017.

SiC microsystems require a diverse set of geometric features for different device components to function (Figure 3.15). For instance, low aspect ratio features with large depths (100's of µm) have been fabricated for through-wafer interconnect vias in power electronics [66,91–93] and diaphragms in MEMS pressure sensors [94–96]. Most MEMS components require high aspect ratio (HAR) features to reduce footprint and increase sensitivity. For example, narrow gaps (<1 µm) between boss and spring structures in accelerometers and gyroscopes enable higher sensitivities and active area with respect to device footprint. In addition, HAR etch holes (30:1) enable sacrificial release paths, and ports for epitaxial seals [97,98]. HAR components are also useful for periodic structures in photonics, such as gratings and photonic crystals [99–102]. Furthermore, HAR channels have higher surface area, and the reduced thermal resistance is leveraged to decrease the hotspots of power electronics [3], [103]. HAR trenches (5:1) have also been filled with epitaxial deposited SiC to create electrical super junctions, which are deep columns of alternating p and n type SiC [104]. HAR geometries of 50µm in depth have also been used in the manufacturing of monopropellant microthrusters, where exothermic decomposition of a monopropellant is achieved [105]. The corrosion resistance of SiC makes it an attractive candidate for use with harsh monopropellants such as hydrazine; hydrazine microreactions have been demonstrated in a 600 µm deep SiC microreactor for 3-hour periods [106].

Various manufacturing methods (plasma etch, laser ablation, imprint, and molding) have been developed to realize HAR features (>3:1) in SiC and each method supports a variety of MEMS and electronics applications (Figure 3.15). For example, laser ablation using small wavelength femto- and pico-second lasers [92], [93], [94], [64, 107–111] has been shown to create reliable SiC wafer vias at a rate of 870 µm/min [92], and has also shown AR features as high as 40:1 with a depth of 200 µm for use in optical gratings [64]. However, laser ablation is challenging to scale for manufacturing purposes, and the residual particles and depths are challenging to control for small (<5 µm) features in the nanoscale regime. In addition, molding techniques where a secondary substrate is etched and coated with SiC films have been used to create atomizers with critical dimensions of approximately 75 µm and AR 3.5:1 [58]. Molding techniques have so far been limited to polycrystalline and amorphous forms of SiC. Isotropic chemical etching through electro-chemical etching or molten salts has also been used but is limited to isotropic features and doped substrates [36]. Also, nanoimprint technology has been used, where a hard mask is created using a grating press on photoresist to get ultra-narrow (<400 nm) features, but these are limited to very small etch depth features [112].

ICP etching is attractive for MEMS SiC processing due to its potential for wafer-level scalability, high throughput, compatibility with Si processing equipment, and high precision compared to other

machining technologies. However, a common effect in SiC ICP etching is microtrenching, where the edges of the trench etch faster than the center of the trench [113]. This effect is negligible in large area etching, such as that of a 1000 µm diameter pressure sensor [94]. However, at high aspect ratios, microtrenching can cause undesirable effects in MEMS devices such as stress concentrations [96]. Previous work has characterized the effects of different ICP parameters on the etch process [114]. Other work has focused on characterizing etch rates of SiC in low aspect ratio bulk processing. L. Evans et al. at NASA Glenn [83] have reported trenches with aspect ratios as high as 13:1 to date with a modified deep reactive-ion etch [55]process for SiC, and Tanaka et al. have reported channels of 11:1 aspect ratio with 10 µm opening width [67].

This section presents a detailed examination of HAR SiC trench formation and evolution with an SF_6 and O_2 ICP etch process. We have observed that HAR trenches etched in SiC have an observable side wall angle from the vertical (Figure 3.16a) [3]. We found that this shape occurs through the progressive microtrench formation in the channel. We characterized the evolution of the microtrench topology as it advances from low AR with small corner variations to HAR with larger microtrenches, to extreme AR with converged trenching (Figure 3.16b). We also studied the effect of ICP bias power, gas mixture (O_2 by flow rate), and ICP chamber pressure on etch rate with respect to various aspect ratios. This work presents the highest aspect ratio fabricated with ICP etching reported to date at 18.5:1 (Figure 3.15 & Figure 3.16a). The HAR etching of SiC will help enable the next generation of SiC MEMS for extreme environment and micro-cooling applications [52].

3.3.2 Microfabrication

To perform microfabrication, we used double-sided polished, n-type 4H-SiC samples with a resistivity of 1.15 Ω-cm (CREE Inc.). Due to the high cost of this substrate, the samples were singulated into 1cm1cm dies when used for etch experimentation. An overview of the fabrication process steps is shown in Figure 3.17. To create the seed layer for the electroplated etch mask, a 50 nm evaporated gold layer was patterned with a multilayer lift-off process to improve metal removal. The multilayer photoresist was composed of photoresist (Shipley 3612) coated on an inert, non-UV-sensitive polymer (Lift-off-Layer 3000) and was soaked in a solvent (MF-26A) to develop features. The samples were coated with gold and then soaked with a solvent (Microposit Remover 1165) to create the patterned features. The Ni mask was electroplated using a Watt's bath recipe [85] at room temperature for 15 min. The mask thickness varied from 1 to 4 µm due to non-uniformity in the electrodeposition

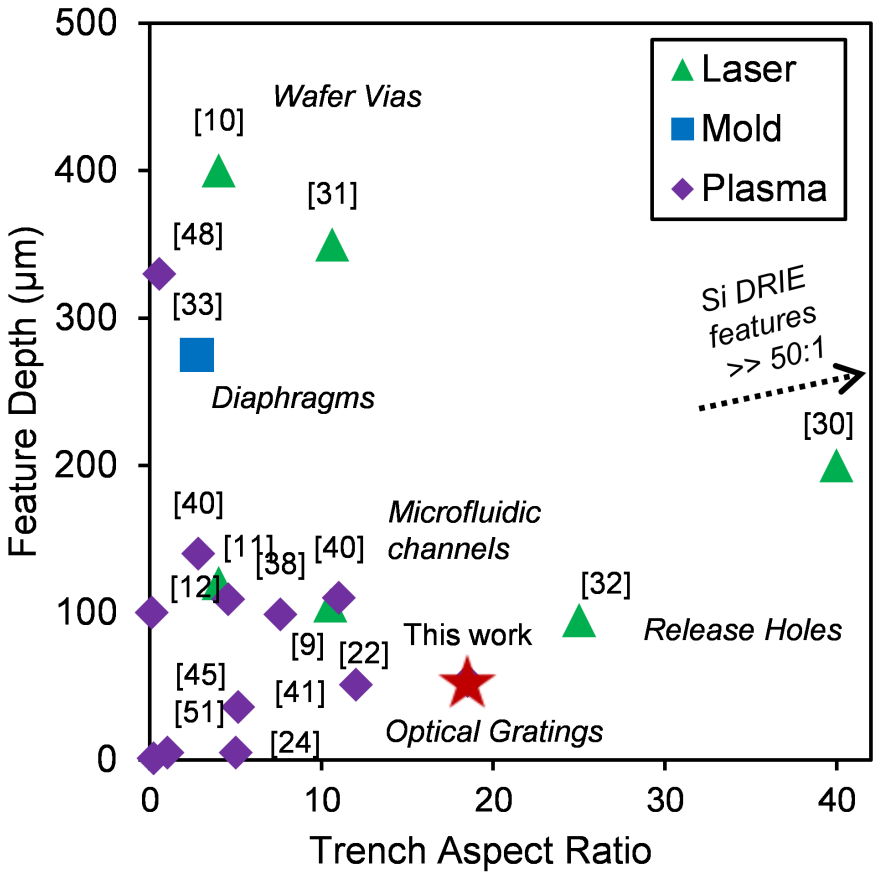


Figure 3.15: Previous work in SiC micromachining for plasma etching, laser ablation, and other mold techniques.

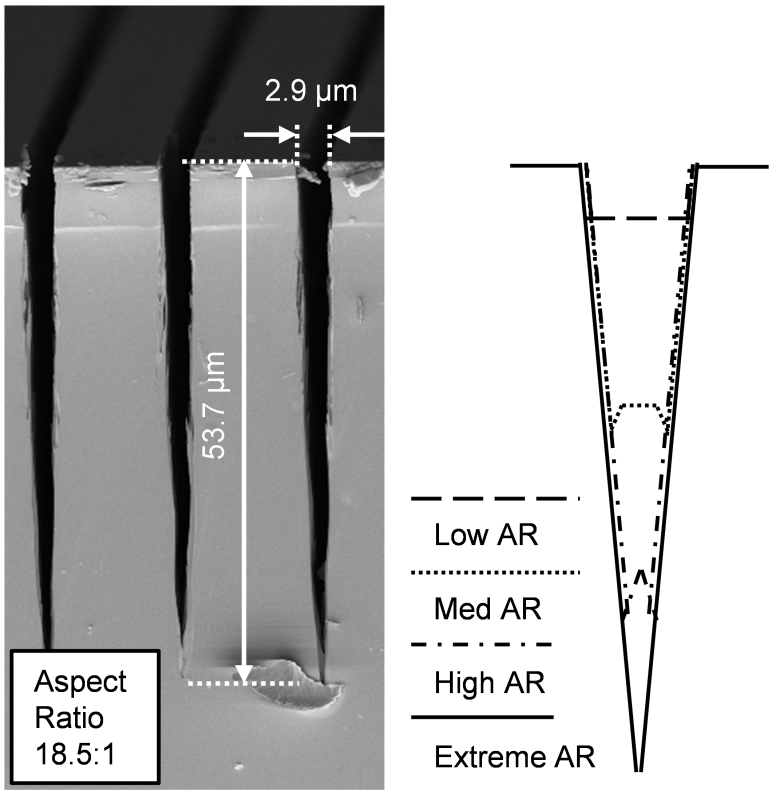


Figure 3.16: (a) High aspect ratio trenches machined in 4H-SiC. The sample was etched as sample E in Table I. (b) Sketch of the typical topology of a narrow SiC trench at different aspect ratios. Empirical values from our study showed a low AR < 1 with negligible microtrenching, medium AR > 3 with resolvable microtrenches, high AR > 5 with converging microtrenches, and extreme AR > 7 with non-resolvable microtrenches.

process. The lithography mask contained arrays of 3.5 mm long channels with widths ranging from 2.5 to 100 µm. Since the conformal electrodeposition process decreased the final channel width by approximately 1 to 5 µm, the actual opening width was measured using Scanning Electron Microscopy (SEM) after processing. After bonding the samples with thermal release tape to a 4-inch wafer carrier (sapphire), the SiC dies were etched in a metal etcher (PT-MTL, Plasma-Therm LLC, 2 MHz ICP RF and 13.56 MHz bias). Samples were etched in an SF_6 and O_2 plasma, with specific process parameters summarized in Table 3.2. After the SiC etching was complete, the Ni, Au, and Ti metals were removed using standard wet etch chemistries. The etched samples were then cleaved with a diamond scribe, cleaned with isopropyl alcohol, and imaged with SEM. To examine the etch profile as it evolved through the depth of the substrate and the effect of ICP etch process parameters, we performed two types of experiments: time-evolution and parameter variation. Table I summarizes all experiments run and measured for this study. In the time-evolution study, five SiC die were etched in the chamber. One sample was removed at each time stamp between 15, 30, 60, 90, and 180 minutes. During the parameter variation experiment, the parameters were varied from a set baseline (sample H in Table 1). Pressure, O_2 fraction, and RF bias power were varied in this study. The ICP coil power was set to a constant of 1000 W, which is near the upper end (1200 W) of the tool, to ensure a study of more practical etch rates (> 0.3µm/min). Each of these samples was processed for a total etch time of 60 min. Each etched SiC trench cross section was imaged using a SEM (Carl Zeiss AG). The depth and width of each trench was measured using image processing software (ImageJ, Inc.).

Selectivity of SiC to Ni was calculated through a ratio of SiC etch rate to Ni etch rate [69, 70]. We used a stylus-based surface profiler (Alphastep 500) to measure the step heights of the initial Ni mask, the etched SiC with remaining mask, and the etch SiC with Ni mask removed completely, to approximate the amount of Ni thickness etched. It should be noted that the selectivity was within an approximate range of 20 to 90 and is in agreement with previous reports [66, 67]. These experiments were studied at the die level due to the high cost of materials. Should wafer-level processing be performed, one must consider wafer-level etch effects. These include, but are not limited to, loading effects (the amount of exposed material to etch) and wafer-level variation due to processes such as diffusion of the plasma gases [115, 116].

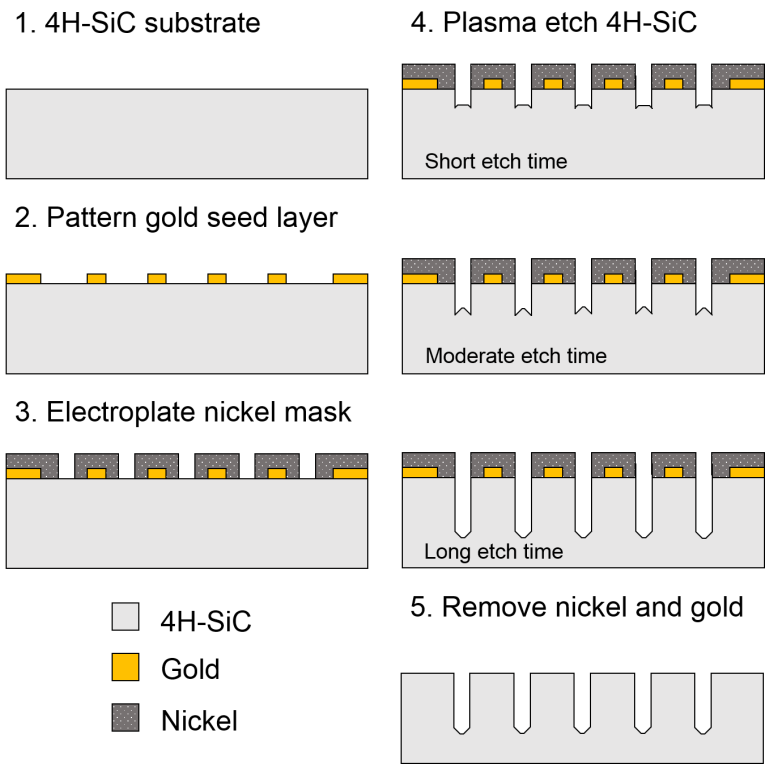


Figure 3.17: Schematic of fabrication process used to create high aspect ratio trench features in n-type 4H-SiC.

Table 3.2: ICP Plasma Parameter Conditions for each Test Sample. Note: The total flow rate of SF_6 and O_2 was 60 sccm. The ICP coil power was 1000 W

Sample	Etch Time (minutes)	Pressure (mTorr)	O_2 Fraction (% Total Flow Rate)	RF Bias Power (W)
A	15	5	10	50
B	30	5	10	50
C	60	5	10	50
D	90	5	10	50
E	180	5	10	50
F	60	10	20	50
G	60	15	20	50
H	60	5	20	50
I	60	5	40	50
J	60	5	20	25
K	60	5	20	100

3.3.3 Results and Discussion

Time-Evolution of High Aspect Ratio SiC Trenches

Etching of HAR SiC trenches is characterized, in part, by the formation of microtrenches at the bottom corners of the trench. Figure 3.18 shows the observed trench profiles over time for an opening width of 6 µm. At low aspect ratios (AR 1:1 at 15 min), the trenches were observed to be mostly uniform square shapes with approximately 90° sidewalls. As etching progressed, microtrenches began to form at the trench corners (AR 2:1 at 30 min), increasing in size (AR 3.5:1 at 60 min). Eventually these microtrenches converged (AR 6:1 at 90 min) causing a "W" shape to be observed. At very long etches and HARs (such as 13:1 at 180 min) the microtrenches fully converged to a "V" shape. In our experiments, the microtrenches were observed to converge at an aspect ratio of about 7:1 as seen in Figure 3.19a. The anisotropy had also decreased to 88° sidewalls over 180 minutes. These behaviors were observed in trenches fabricated up to an aspect ratio of 18.5, the largest aspect ratio obtained during this experiment (Figure 3.16a). Extreme HAR structures in SiC will have this narrowed "V" shape if the plasma parameters are kept constant. The observed formation of microtrenches in the SiC trenches is complex, and results from a combination of mechanisms. Throughout the experiment, the sidewalls were shown to have a small divergence angle (2°) from the vertical as is

generally observed during dry etching of SiC [113], [117], [83], [59]. Previous work has shown the formation of microtrenches in Si, SiC and other substrates due to various effects at the sidewalls of trenches [113] [118], [119], [120]. When the depth of a trench increases, the ion flux distributes over the bottom and the sidewalls. For anisotropic plasma, the ions encounter the sidewalls at small angles of incidence, and this causes reflection of ions onto the bottom surface. The increased scattering of etchant characters yields higher bombardment at the corners of the trench [114], [121], [122]. At higher plasma powers, a sheathing effect [114], [119] has been studied where the charging of the substrate surface during etching creates a bend in the etching bias, which causes more plasma ions to bombard at the corners.

These SEM images at different etch times also provide evidence of decreasing etch rate as total trench depth progresses. Figure 3.19b and Table 3.3 show the dependence of the etch time (and trench depth) on the etch rate, with the etch rate getting slower as the trench evolves. The calculated rate to etch 5 µm deep is 40% faster than the calculated rate at 55 µm deep. As the depth (and thus aspect ratio) of a trench increases, there is limited mass transfer [65, 123, 124] of radical etchants to the bottom of the channel, which thus reduces the etch rate. This shows a time-averaged reduction of etch rate. The time-dependence of the etch rate is estimated by taking the slope between each pair of points in Fig 3.19b. These values are tabulated in Table 3.3. The time-average etch rate is higher than the time-dependent etch rate as high as 21%. For the highest aspect ratio trenches, this decreasing etch rate increasingly affects the total etch time of the trench. If one is to design an extremely HAR etch, one must consider the long term etch rate reduction of a process, and go beyond linear assumptions (time-average) to determine the target etch time.

It should be noted that the data presented in Figure 3.19 and Table 3.3 applies to features with narrow (<20 µm) mask openings. Larger area features, such a pressure sensor diaphragms with AR <1, will typically result in microtrenching [96], but these features do not influence the bulk etch rate as they do in these narrow regimes. The appearance of irregular artifacts such as secondary trenching (located at the top of the trench) and etch asymmetries (lop-sided microtrenches) are also observed (Figure 3.18). Asymmetry of a microtrench has been reported in the past, which results from the sample placement in the etch chamber being farther away from the center [114].

The Effect of Pressure

The ideal pressure at which to etch SiC using an ICP is dependent on a number of variables including equipment model and bias voltage [123], [125], [126]. The etch rate as a function of pressure is

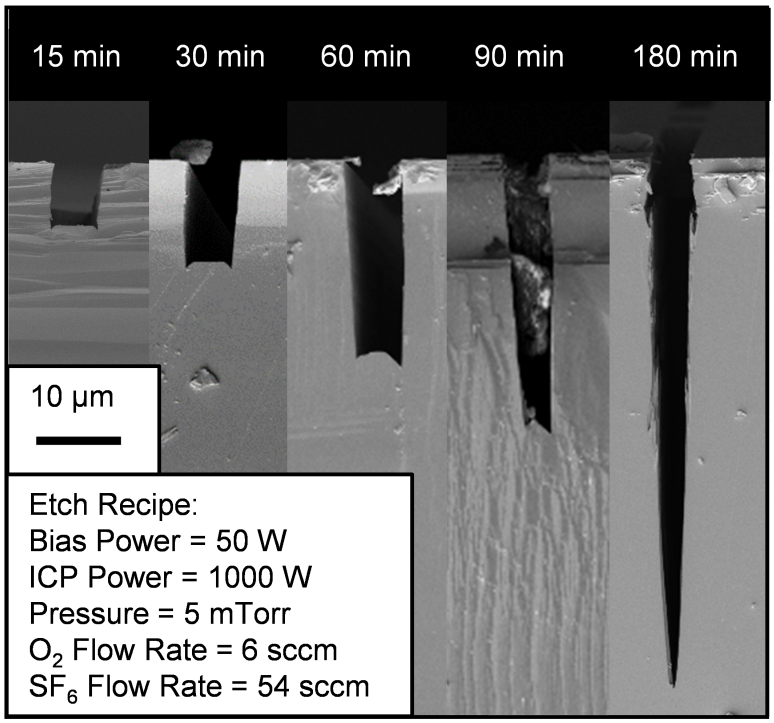
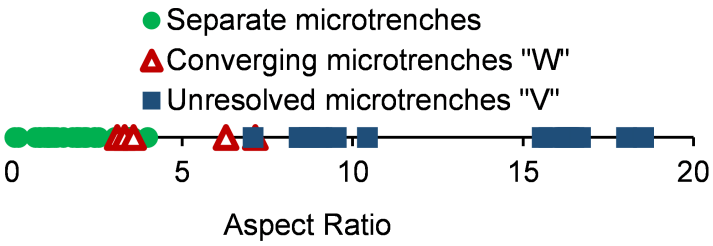
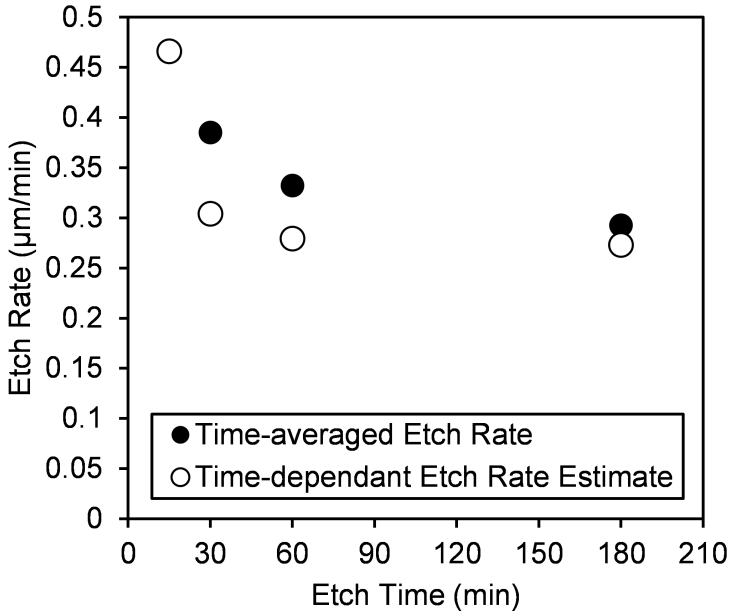


Figure 3.18: Cross-sectional SEM images of 6 µm wide trenches from samples A-E from Table 3.2. Each sample was etched for a varied amount of time, and the microtrenches dictate the evolution of the trench geometry.



(a)



(b)

Figure 3.19: (a) Plot of the trench aspect ratios observed in 60 SiC trench samples (A–E from Table 3.2), sorted by microtrench topology. (b) Time-average etch rate of narrow features ($<$ 10 μ opening) and Time-dependent etch rate with respect to current etch depth. As the trenches are etched deeper, the current etch rate reduces greatly.

Table 3.3: Summary of Trench Depth and Etch Rates. Note: Trenches analyzed had widths < 10 µm

Sample from Table 3.2	Trench Depths (µm)	Time-average Etch Rate (µm/min)	Time-dependent etch rate (µm/min)	Difference in Etch Rates (%)
A(15 min)	6.99 ± 0.26	0.47	0.47	–
B(30 min)	11.55 ± 0.83	0.39	0.30	21
C(60 min)	19.93 ± 2.85	0.33	0.28	16
D(180 min)	52.70 ± 4.73	0.29	0.27	7

characterized by considering two competing plasma effects that occur in the 1 to 100 mTorr pressure range [125]. In general, increasing the chamber pressure results in an increase in the number of neutral radicals available for ionization, increasing the number of ions etching the plasma in a given unit time. We found that this effect was dominant in the <10 mTorr pressure range. At higher pressures, however, the mean free path of the particles in the plasma decreases, decreasing the energy of the etchant ions and increasing their rate of recombination with free electrons [123]. We observed that at chamber pressures higher than 10 mTorr, the etch rate began to decrease from the 10 mTorr value.

It has been suggested by previous reports that increasing the ICP bias voltage increases the optimum chamber pressure for etching [123]. At higher bias voltages, the ions become more energetic, combatting the effects of reduced mean free path and ion recombination [126]. Our experiment examined the effects of varied low pressures. We etched samples at 5, 10, and 15 mTorr pressures (holding other plasma etching parameters constant), and the sampled etched at 10 mTorr had the highest etch rate at approximately 0.5 µm/min. The sample etched at 15 mTorr had the lowest etch rate at approximately 0.3 µm/min, and the sample etched at 5 mTorr had an etch rate near 0.45 µm/min, as shown in Figure 3.20a. These samples also showed a small decrease in etch rate at higher aspect ratios. These samples were all etched in a plasma with 50 W bias power, and so the ideal pressure (for range of parameters studied here) for these trenches is around 10 mTorr due to the competitive effects described previously.

The Effect of ICP Bias Power

ICP etch rates are strongly affected by bias power. Our SiC etch rate measurements, as shown in Figure 3.20b and 3.20e, follow trends previous researchers reported [65, 66, 123]. As we increased in

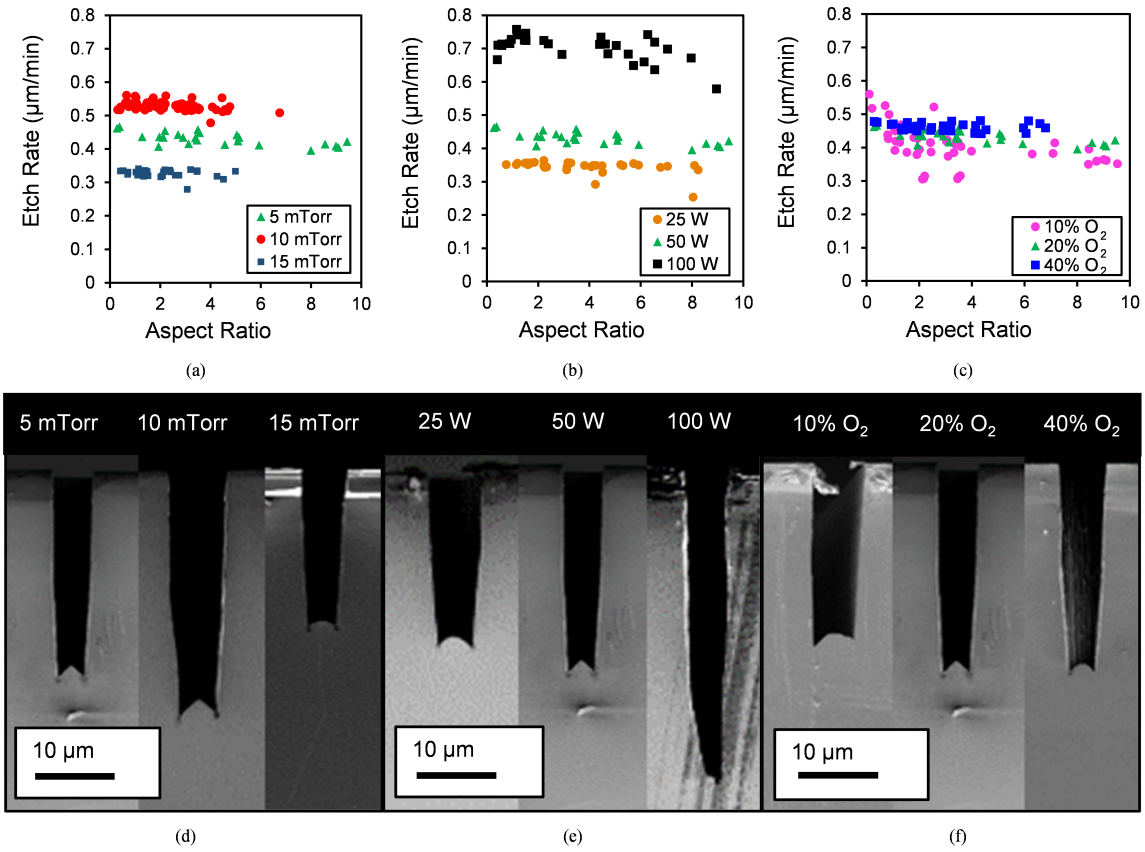


Figure 3.20: Etch rate of SiC trenches as a function of aspect ratio from samples listed in Table 3.2. (a) Varied pressure with samples F, G, and H. (b) Varied bias power with samples H, J, and K. (c) Varied oxygen fraction with samples A-E, H, and I. SEM images of trenches with opening widths of approximately 6 μ from samples in Table 3.2. (d) Varied pressure with samples F, G, and H. (e) Varied bias power with samples H, J, and K. (f) Varied oxygen fraction with samples C, H, and I.

bias power from 25 W to 100 W, we observed an increase in the SiC etch rate from 0.36 µm/min to approximately 0.7 µm/min, respectively. Additionally, the etch rate did not vary much with feature aspect ratio until around the 8:1 regime. We also observed an increase in sidewall trench angle at higher bias powers (Figure 3.20e). When the vertical bias field is stronger it maintains higher anisotropy. This creates more vertical sidewalls, less incident reflections off these sidewalls, and thus less bombardment at the corners of the trenches. High bias power recipes are desired to increase the etch rate, but the drawback is an increase in micromasking, where the etch mask redeposits on the etch surface [65]. We observed micromasking phenomena similar in our previous study of wider SiC trenches [3], but not in narrow regions. This has also been reported by others [67]. However, Khan et al. have shown that increasing the bias power as the etch progresses can improve the etch rate of high aspect ratio trenches (and mitigate micromasking) [124].

The Effect of Oxygen Flow Ratio

Previous work has demonstrated the effect of ICP SF_6/O_2 ratio on etch rate and microtrench profile of SiC [66], [114], [120], [68, 127, 128]. SF_6 is the dominant etchant in the SF_6/O_2 mixture, so at high O_2% (and thus lower ratio of reactive particles), the etch rate decreases. Higher O_2% has also been reported to cause SiO_2 passivation [114, 128], which also slows down the etch rate and creates micromasking. However, O_2 presence has also been reported [129] to create highly volatile products and thus improve etch rates. Thus, there are competing effects; the literature tends to show that a low O_2 concentration (20%) is beneficial to reduce sidewall passivation without significantly reducing the etch rate [68,120,127]. The measurements of SiC etch rate dependence on aspect ratio at varied O2 percentage are presented in Figures 3.20c and 3.20f. The etch rates at 10% O_2 (90% SF_6) varied from 0.55 to 0.3 µm/min, from lowest to highest aspect ratio features. Similarly, the etch rates at 20% O_2 (80% SF_6) varied from 0.47 to 0.40 µm/min, and the etch rates at 40% O_2 (60% SF_6) varied from 0.48 to 0.44 µm/min.

The range of experimental parameters used in our study did not yield a resolvable effect of O_2% on etch rate. However, it was observed that the etch rate was less sensitive to aspect ratio at increased O_2 fraction. In the lowest 10% O_2 case the high presence of SF_6 amplified the etch rate in low aspect ratio features the mass transport limitation is clearly shown at higher aspect ratios. The HAR features (>9:1) etch 40% slower than low aspect ratio features (<1:1). At higher O_2 concentrations there is less SF_6, and thus lower sensitivity to mass transport effects. The 20% O_2 case shows a 10% etch rate reduction between high and low aspect ratio, and the 40% O_2 case

has 5% difference between high and low aspect ratio. Higher O_2 concentration plasmas have less etch rate variation with varied aspect ratios.

3.3.4 Conclusion

We performed an extensive study of HAR ICP etching of SiC with SF_6 and O_2 using time-evolution and ICP parameter variation. We observed a profile evolution of the microfabricated trenches from an AR of 1:1 to 13:1. No microtrenching was observed for aspect ratios less than 1:1, after which microtrenches were seen to develop at the trench corners creating "W" shapes. These trenches converged at aspect ratios greater than 7:1, forming a characteristic "V" shape that was observed in trenches with aspect ratios as high as 18.5:1. This feature has the highest aspect ratio reported for an ICP etched SiC trench to date. Our analysis of the time-dependent and aspect-ratio-dependent etch profiles showed a reduction in etch rate at higher aspect ratios by over 40%. In addition, dependence of etch rate on a variety of ICP parameters was also observed resulting in an etch rate as high at 0.75 µm/min. An optimal plasma chamber pressure for improved etch rate was observed to occur at approximately 10 mTorr for our chosen plasma conditions, with competing physical effects reducing etch rates at higher and lower chamber pressures. The fraction of O_2 flow had a negligible effect on the observed etch rate. But the increased presence of oxygen (>20%) reduced the aspect ratio dependent etching. The increase in RF bias power increased the etch rate and anisotropy of the trenches.

This study of ICP processing of HAR SiC trenches allows advancement in micromachining technology for this durable wide bandgap semiconductor. The ICP etch process examined here can be used in the fabrication of SiC-based microelectromechanical devices and systems such as accelerometers and gyroscopes as features in the range of 20 to 75 µm deep with opening widths as small as 1 µm and aspect ratios as high as 18.5 were achieved. In addition, this process is suitable for manufacturing other interdigitated geometries, embedded cooling or fin-like structures, and microcombusters. The application of SiC in these application areas has the potential to realize microsystems for operation within harsh environments that are not suitable for Si platforms.

3.4 Lithography-free microfabrication of AlGaN/GaN 2DEG strain sensors using laser ablation and direct wirebonding[†]

3.4.1 Introduction

Microelectronics based on aluminum gallium nitride (AlGaN) and GaN heterostructures have gained interest for various sensing applications such as strain [130–132], pressure [133, 134], inertial [135], chemical [136], and optical sensors [137–139] due to their sensitivity and extended operation temperature by wide bandgap properties. Among such devices, AlGaN/GaN-based mechanical sensors have particularly emerged because the conductive two-dimensional electron gas (2DEG) formed at the AlGaN/GaN interface is highly responsive to external stimuli [140, 141]. The majority of AlGaN/GaN mechanical sensors typically use suspended membranes [133, 134, 142]or cantilever [130] elements with metal alloys for Ohmic and Schottky contacts. In general, such devices' scheme requires multiple microfabrication steps including thin film deposition, lithography, dry/wet etching, metallization, and annealing [130, 133, 142]. In addition, fabricated devices need to be packaged separately on ceramic chip carriers. However, this multiple microfabrication steps and packaging process leads to high cost, large time commitment, and complexity of overall process. Consequentially, the development of simple and rapid microfabrication/packaging techniques is required for the fabrication of various microelectronics. In this work, we demonstrate a facile, rapid, and reliable microfabrication technique using direct laser ablation and direct wire bonding as reported in our former study [139,143] to create AlGaN/GaN strain sensors (suspended membrane type) in less than 5 min. The silicon (Si) substrate was quickly etched away using the laser ablation, which is much faster etching process compared to conventional Si dry/wet etching, to release membrane structure. The backside Si etching was achieved without any photolithography processes including photoresist coating, baking, photoresist development, and backside alignment. In addition, the direct bonding between suspended AlGaN/GaN membrane and chip carrier enables simultaneous metallization and packaging processes that eliminate tedious metallization process (i.e., lift-off) [139, 143].

[†]Originally published as K.M. Dowling, H. So, A. Toor, C.A. Chapin, and D.G. Senesky. Lithography-free microfabrication of AlGaN/GaN 2DEG strain sensors using laser ablation and direct wire bonding. *Microelectronic Engineering*, 173, 2017.

3.4.2 Experimental method

A schematic of our simple fabrication process is shown in Figure 3.21. AlGaN/GaN-on-Si wafer (DOWA, 25% Al content in AlGaN, 2DEG mobility of ~1400 $cm^2/V \cdot s$) was singulated into 5 mm×5 mm die (Figure 3.21a). Then a circular diaphragm (3.5 mm diameter) of the underlying Si substrate was etched using laser ablation (DPSS Samurai UV Laser) (Figure 3.21b). The laser was operated at 3 W at 30 kHz pulses, 30 passes, 200 mm/s scribe speed, 25 µm scribe spacing, and cross hatch cut path, completed in 200 s. The etched die was rinsed with acetone and isopropyl alcohol to remove chip debris. The die was then attached with polyimide tape to a ceramic leadless chip carrier (LCC, Spectrum Semiconductor Materials Inc.) and directly wire-bonded (7476E, West Bond Inc., ultrasonic power of 460 mW for 30 ms) using aluminum bonding wire (25.4 µm diameter) [139] (Figure 3.21c). The fabricated device was tested under various displacements using a micromanipulator (Signatone S-M40 micropositioner) with a small tip, centered over the diaphragm. Force was applied through vertical displacements at 1/48th turn of the knob (~13.2 µm). Figures 3.22a and b show the experimental testing setup and optical image of packaged AlGaN/GaN die on the LCC used in this study, respectively. A small tip on the end of the micromanipulator was centered over the packaged AlGaN/GaN strain sensor. The tip was slowly moved down towards the center of the membrane while measuring the current-voltage response in a range of voltage (V_{bias}) from 0 to 2 V. We added 1/48th of a turn and took sequential current-voltage measurements until the displacement reached approximately 106 µm. To characterize the sensors transient and reliable response, the change of current with respect to time was also monitored with varied bias voltages. This measurement was conducted by alternatively applying and releasing displacement.

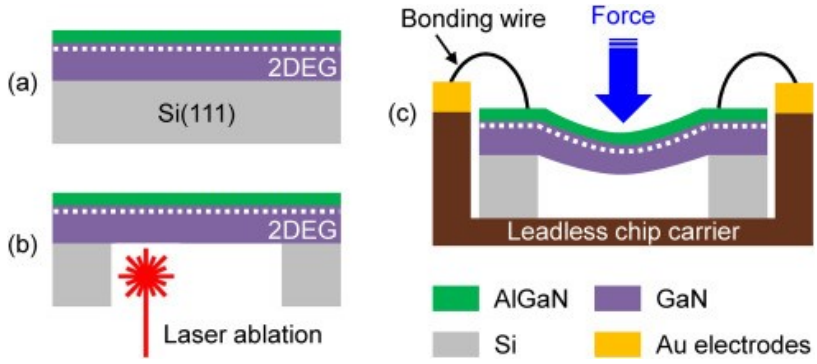


Figure 3.21: Schematic of AlGaN/GaN strain sensors using a combination of laser ablation etching and direct wire bonding architectures. (a) Singulation of AlGaN/GaN-on-Si die, (b) membrane suspension using laser ablation, and (c) aluminum wire bonding between sensor surface and leadless chip carrier.

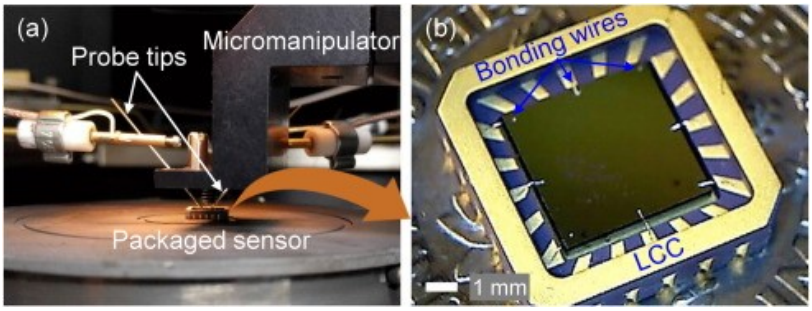


Figure 3.22: (a) Image of experimental setup for strain transduction measurements and (b) optical image of packaged AlGaN/GaN die on ceramic leadless chip carrier (LCC).

3.4.3 Results and discussion

Figure 3.23a shows an optical image of 3.5 mm diameter cavity etched by laser ablation of the underlying Si substrate. To characterize the surface roughness, etched surface was visually investigated using 3D non-contact confocal microscope (S-neox, Sensofar) and it showed RMS surface roughness of ~21.34 µm, as shown in Figure 3.23b. Figures 3.23c and d show a cross-sectional scanning electron microscope (SEM) image of suspended AlGaN/GaN diaphragm (thickness of ~190 µm) and Al wire directly bonded between the LCC and the GaN capping surface on top of the AlGaN barrier layer, respectively. The physically stable and electrically reliable metal contact was achieved using a direct wire bonding between the LCC and sensor surface [139, 143]. This simultaneous fabrication and packaging process took only approximately 5 min (with 1 h of preparation time) whereas several hours and photolithography masks are needed in conventional microfabrication and packaging methods.

To characterize the fabricated strain sensors, we applied different displacements with a micromanipulator and measured the current-voltage response. Figure 3.24 shows the change in current passing through the 2DEG with respect to applied displacement (i.e., strain). External tensile strain through applied displacement induces additional piezoelectric polarization of the 2DEG and increases the sheet carrier concentration [130, 133, 139, 144–147]. Therefore, there was an increase in current when the membrane was gradually deflected from 13.2 µm to 105.8 µm. It should be noted that the current came back to the base current (i.e., the dashed line in Figure 3.24) when the strain was completely released, indicating a stable and reversible sensor's operation. Figure 3.25 shows the change of current (ΔI) with respect to applied strain under different operation voltages. To estimate the sensitivity of the sensor, a linear fitting curve was employed on each data. The measured data

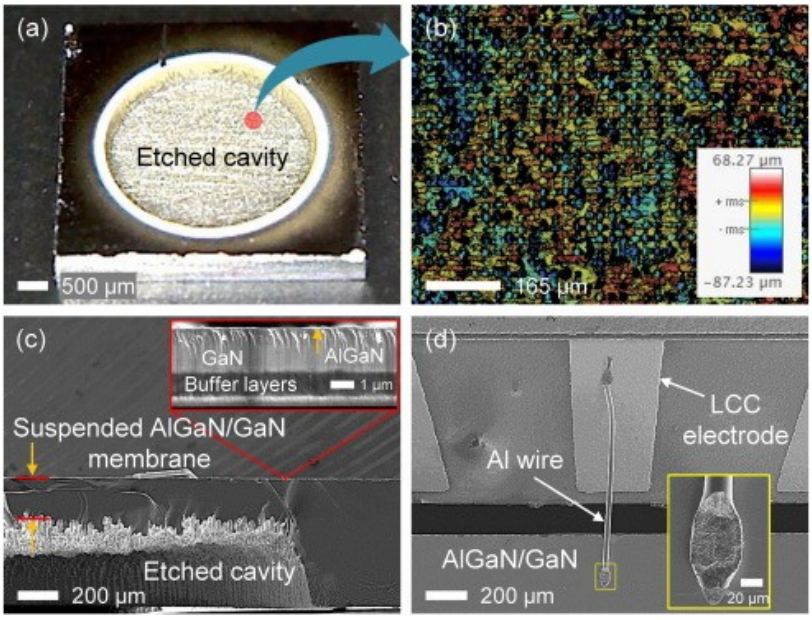


Figure 3.23: (a) Optical image of a 3.5 mm diameter cavity etched by laser ablation of the underlying Si substrate, (b) confocal contour of etched surface indicating RMS surface roughness of ~21.34 µm, (c) cross-sectional SEM image of suspended AlGaN/GaN membrane after laser ablation etching, and (d) aluminum wires directly bonded between LCC and GaN surface (i.e., capping layer on top of the AlGaN barrier layer) for electrical connection.

are in good agreement with linear fitting curves, as seen in Figure 3.25. Table 4.3 summarizes the calculated sensitivity (in nA/µm units) with the coefficient of determination (R^2) values of linear fitting curves. The R^2 values around 0.96 to 0.99 for four different linear fitting curves showed the proportional (linear) trend of current change with respect to the applied displacements. In addition, the sensitivity increases with an increase in V_{bias}, which has also been observed in other GaN based devices [148, 149].

Table 3.4: Calculated sensor's sensitivity and coefficient of determination values using linear curve fitting method.

Applied bias (V)	Sensitivity (nA/µm)	R^2
0.5	5.4	0.966
1	18.7	0.991
1.5	49.3	0.994
2	102.5	0.994

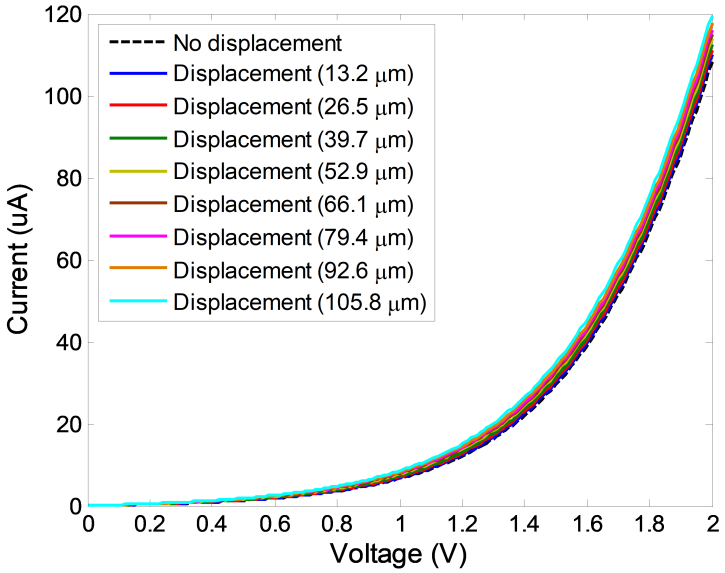


Figure 3.24: Current change of the fabricated AlGaN/GaN strain sensor under different applied displacements.

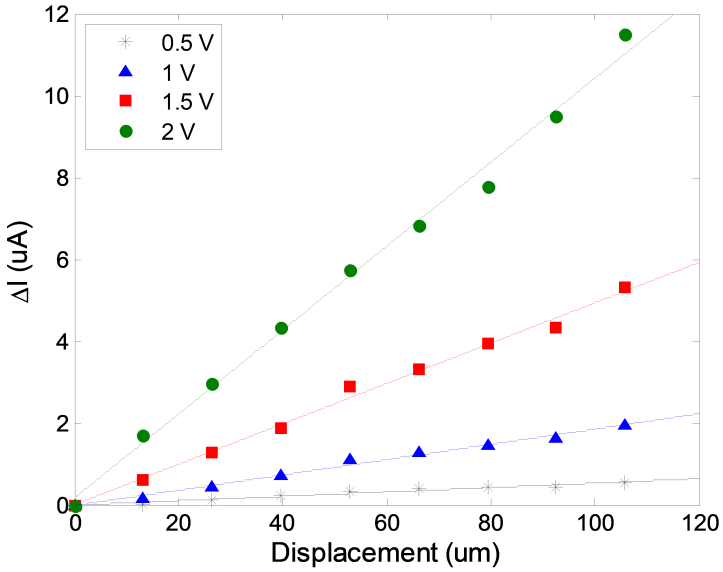


Figure 3.25: Change of current and linear fitting curves with respect to various displacements under different operation voltages.

To characterize transient response of the fabricated sensor, the real-time current change was monitored with different levels of displacement applied and released alternatively, as shown in Figure 3.26. It should be noted that the base current at high V_{bias} (i.e., 2 and 3 V) was drifted at

the beginning because of initial discharging from transients when device was first turned on. Once these transients were settled (stable), the current-voltage response was returned to the original base level upon release of the displacement, as shown in Figure 3.26, demonstrating stable and reversible operation of the fabricated AlGaN/GaN strain sensor. There was some variation in the base current due to the manual placement of wire bonds [139] and AlGaN/GaN membrane thickness variation due to laser focus during the ablation etching process. Nevertheless, this prototyping method enables low cost testing for studying 2DEG transduction properties and rapid customization for GaN-on-Si microelectronics products without cleanroom infrastructure.

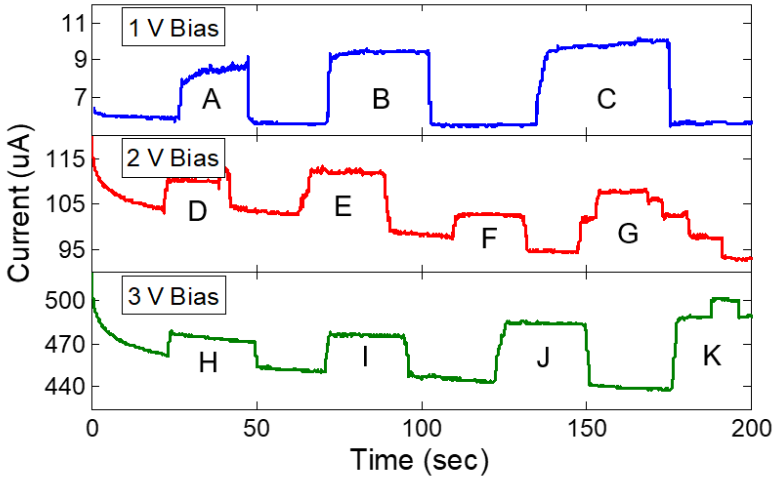


Figure 3.26: Transient current response for the strain sensor under different bias voltages (1, 2, and 3 V) with different levels of displacement applied and released alternatively. Qualitative amplitude of applied displacements: A < B < C (at 1 V), D = F < E = G (at 2 V), and H < I < J < K (at 3 V).

3.4.4 Conclusions

In summary, this study reports the facile and rapid microfabrication technique for AlGaN/GaN strain sensors. The laser ablation was used for etching Si substrate and release AlGaN/GaN membrane within a short period time. The direct bonding of Al wires on sensors surface was achieved for simple electrical connection between the LCC and sensors. The overall fabrication process was

completed within 5 min, which is significantly faster than conventional microfabrication processes. This prototyping method enables testing GaN-on-Si microelectronic devices before investing in a costly wafer-scale process, and studying GaN in laboratories without cleanroom facilities.

Chapter 4

Characteristics of Gallium Nitride Hall Plates

4.1 Overview

In the next two chapters, several fundamental studies involving Hall-effect plates will be covered. Results from three different fabrication runs are presented and compared to understand how the differences effect offset and noise. The devices presented in each of these studies is summarized in Table 4.1. In addition, cross sectional drawings are provided in Figure 4.1 to distinguish the differences between each of these studies. The devices are fabricated using standard lithography techniques, presented in Chapter 2.

This chapter will cover the development of AlGaN/GaN 2DEG Hall plates from two different fabrication runs. The first section will cover work previously published at the Solid-State Sensors, Actuators and Microsystems Workshop at Hilton Head in 2018 [150], which discovered the influence of large bias conditions on the Hall plates. The second section will cover a Hall device from a later fabrication run, which showed much lower residual offsets and temperature stability, previously published in the IEEE Sensors Letters [151].

Table 4.1: Summary of fabrication runs

Gen 1 (SNF MOCVD AlGaN)	Gen 2 (DOWA AlGaN)	Gen 3 (InAlN and SNF MOCVD AlGaN)
200 µm octagon [4]	2×200 µm Octagon with Mesa extension to contact and long traces[2,3]	200 µm point-like contacts, narrow contacts, octagon, and wide contacts [4]
100 µm octagon [1,4]	2×200 µm Octagon with Mesa extension to contact and extra long traces[3,4]	100 µm point-like contacts, narrow contacts, octagon, and wide contacts [4]
50 µm octagon [4]	2×200 µm Octagon with Mesa extension to contact and short traces[3]	50 µm point-like contacts, narrow contacts, octagon, and wide contacts [4]

[1] Section 4.2.

[2] Section 4.3.

[3] Section 5.2.

[4] Section 5.3.

4.2 The effect of bias conditions on AlGaN/GaN 2DEG Hall Plates[†]

This section describes the operation of the first generation AlGaN/GaN two-dimensional electron gas (2DEG) Hall plates under various supply conditions (0.026 V to 1.27 V). The 100-µm-diameter octagon-shaped devices were microfabricated using metal-organic chemical vapor deposition of AlGaN/GaN on <111> silicon wafers and traditional photolithography techniques. Upon device characterization at various Hall supply voltages, we observed an increase in the residual offset from 0.1 mT to 1.4 mT (from 9% of measured signal to over 60% in a 1 mT magnetic field). In addition, the sensitivity (scaled with bias voltage) was constant at 76 ± 2.5 mV/V/T (stable within 3%) with

[†]Karen M. Dowling, Hannah S. Alpert, Pengxiang Zhang, Andrea M. Ramirez, Ananth Saran Yalamrthy, Helmut Köck, Udo Ausserlechner, and Debbie G. Senesky. "The effect of bias conditions on AlGaN/GaN 2DEG Hall plates." 2018 Hilton Head Workshop on Solid-State Sensors, Actuators and Microsystems, Hilton Head 2018 Technical Digest, reprinted with the permission of the author and the Transducer Research Foundation.

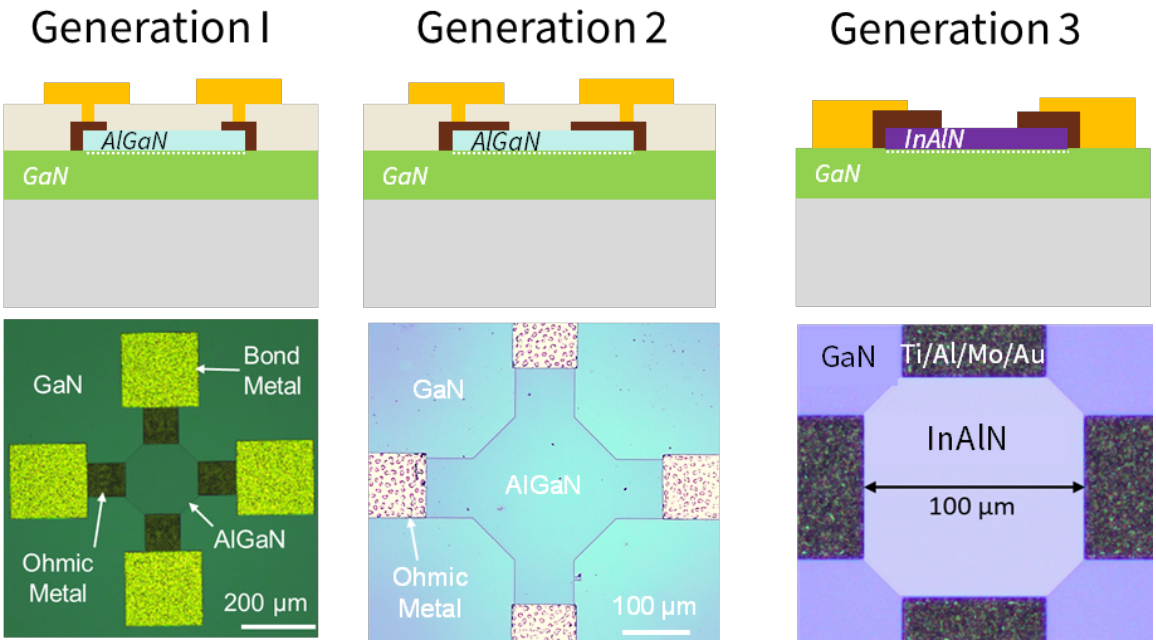


Figure 4.1: Summary of different fabrication runs to be described in Chapters 4 and 5. Generation 1 follows a standard AlGaN/GaN process from previous work [4] but with narrow overlap of contacts with AlGaN/GaN sturcutre. Generation 2 follows the process from [5]and was designed with longer contact overlap, and extended mesa structures for the contact area. Generation 3 follows the process from [6] and uses an InAlN layer instead of AlGaN. Geometries are varied in each fabrication process, summarized in Table 4.1.

high linearity ($R^2 > 0.99$) across the tested operating conditions. This work demonstrates improved understanding of AlGaN/GaN sensor elements that may be monolithically integrated with power electronics, as well function within extreme environments.

4.2.1 Introduction

Hall-effect devices are used in diverse sensing applications such as position and velocity sensors in automobiles and current sensing in power electronics [152]. However, silicon-based Hall-effect sensors have limitations in extreme environments because of the influence of temperature on intrinsic carrier concentration—low-doped materials ($< 10^{16}$ cm^{-3}) become saturated with carriers around 300°C. Recently, two-dimensional electron gas (2DEG) material systems, including AlGaN/GaN, have gained high interest for power electronics monitoring and extreme environment sensing due to their durable nature, wide bandgap, and potential for monolithic integration with electronics [153]. Additionally, piezoelectric and spontaneous polarization create a stable 2DEG carrier concentration across a wide temperature range [154], which enables robust Hall-effect sensing [155, 156]. However, sensing low magnetic field signatures (< 10 mT) under high bias conditions has not been investigated with AlGaN/GaN 2DEG Hall plates.

The Hall-effect can be leveraged for sensing magnetic field signatures through a 4-probe scheme. Constant current is applied across two contacts, and the induced electric potential from the external magnetic field is measured by a Hall voltage reading on the other two contacts. AlGaN/GaN 2DEG plates are promising candidates for Hall-effect sensing because of their high mobility (2000 $cm^2/V - s$) [155] and high temperature stability.

In applications with low magnetic field levels, sensors are required to have high signal accuracy to overcome issues with background fields such as Earth's field or from electromagnetic interference. Hall devices generally have high raw offset values (larger than Earth's magnetic field of 50 µT) when no external magnetic field is applied due to inherent material defects or from various steps in microfabrication [38, 157]. This limits the minimum detectable signal to inconvenient ranges and reduces sensor accuracy. To overcome this issue, current spinning [38] and orthogonal layouts [158] have been adopted in practice to remove these "raw" offsets for silicon devices. These techniques can reduce the raw offset to a "residual" offset below 10 µT under various conditions [38, 157, 159, 160], corresponding to an improvement by a factor of up to 4,000.

In addition to low residual offset values, sensors are also required to have high sensitivity in many applications. Sensitivity is defined as a ratio of the change in Hall voltage (V_{Hall}) due to an

external magnetic field (B). It is well known that the Hall voltage scales with supply voltage (or current), so most reports show either sensitivity scaled with supply current (S_I) or sensitivity scaled with supply voltage (S_V). However, in most applications, Hall plates are operated with a constant supply voltage to enable ease of integration with interface circuitry.

In this section, we present the methodology for Hall-effect sensor microfabrication and characterization with a current spinning technique to study offset values in low magnetic fields (<5 mT). We also examine the sensitivity and residual offset in AlGaN/GaN 2DEG Hall plates as influenced by supply voltage. We observed that the sensor exhibited large residual offset values (60% of the signal in a 1 mT field) under high supply voltage conditions, as well as a constant sensitivity of 76 ± 2.5 mV/V/T. A discussion on the leading contributions to residual offset in these high bias schemes is provided. It should be noted that the AlGaN/GaN Hall-effect sensors have higher sensitivity values compared to silicon-based Hall plates and with proper offset calibration can be used over a large temperature range for extreme environments.

4.2.2 Methodology

Fabrication

To study the effect of bias conditions on AlGaN/GaN 2DEG Hall plate performance, we examined two devices (4-contact van der Pauw structures) from different chips. Figure 4.2 shows a cross-sectional schematic of the 2DEG Hall plate (Figure 4.2a). To microfabricate the device, AlGaN/GaN films were grown on <111> silicon using metal-organic chemical vapor deposition (MOCVD). Then, a 100-µm-diameter octagon mesa with Ti/Al/Pt/Au Ohmic contacts and a 50-nm-thick alumina passivation layer was microfabricated (Figure 4.2b) [4]. The Hall plate device was then bonded to a printed circuit board (PCB) with epoxy and electrically connected with aluminum wirebonds. The packaged device is shown in Figure 4.2c. The two tested devices have lateral resistances (R) of 867 ± 22 Ω and 896 ± 30 Ω (variation among bias conditions) and the operating power rose from 0.83 µW to as high as 1.91 mW (Figure 4.3).

Experimental Set Up

The sensor's principle of operation is shown in Figure 4.2d. To characterize the sensitivity of the device, current was applied with a Keithley 2400 current source from 30 µA to 1.5 mA, which correspond to average supply voltages of 0.026 V to 1.2 V. The Hall voltage was then measured with

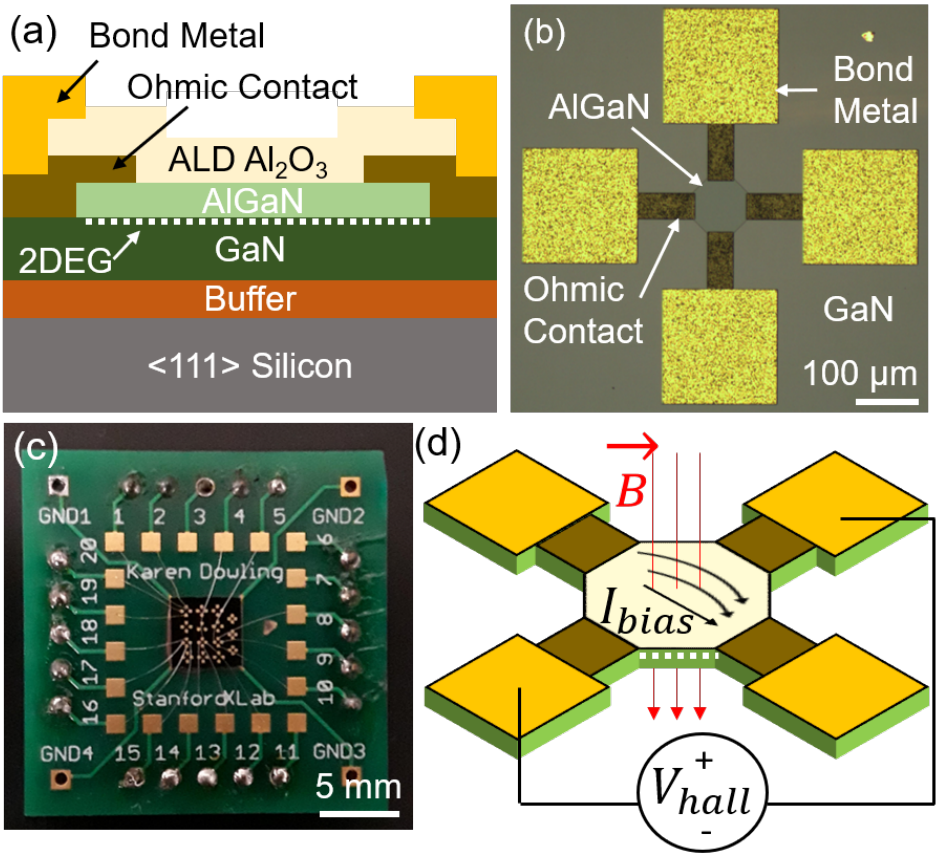


Figure 4.2: (a) Cross sectional schematic of the AlGaN/GaN 2DEG Hall plate. (b) Optical image of the 2DEG Hall plate with 4 contacts (no top plate). (c) Packaged Sensor #1 for testing with floating substrate. (d) Device operation. Constant current is applied across a 4-contact van der Pauw structure and the Hall voltage is measured across the other two contacts. Reprint of Figure 1 in: Karen M. Dowling, Hannah S. Alpert, Pengxiang Zhang, Andrea M. Ramirez, Ananth Saran Yalamrthy, Helmut Köck, Udo Ausserlechner, and Debbie G. Senesky. "The effect of bias conditions on AlGaN/GaN 2DEG Hall plates." 2018 Hilton Head Workshop on Solid-State Sensors, Actuators and Microsystems, Hilton Head 2018 Technical Digest, reprinted with the permission of the author and the Transducer Research Foundation.

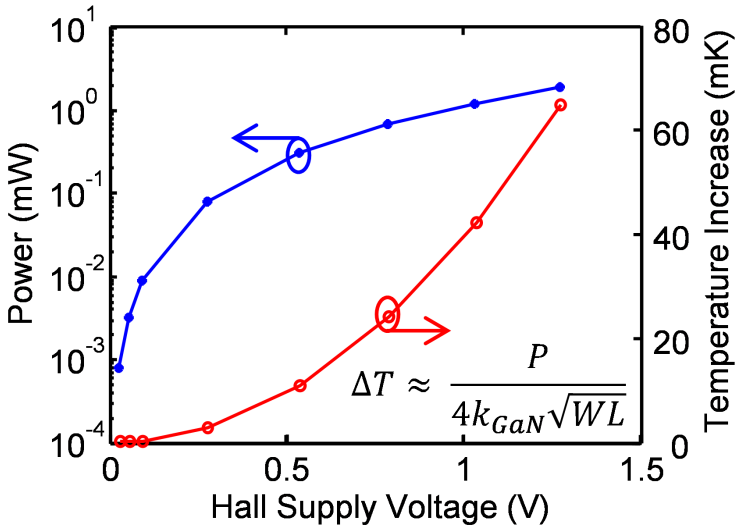


Figure 4.3: Average operating power of 2DEG Hall plates under various supply voltages, and expected average temperature increase along current path from thermal resistance approximation. Reprint of Figure 2 in: Karen M. Dowling, Hannah S. Alpert, Pengxiang Zhang, Andrea M. Ramirez, Ananth Saran Yalamrthy, Helmut Köck, Udo Ausserlechner, and Debbie G. Senesky. "The effect of bias conditions on AlGaN/GaN 2DEG Hall plates." 2018 Hilton Head Workshop on Solid-State Sensors, Actuators and Microsystems, Hilton Head 2018 Technical Digest, reprinted with the permission of the author and the Transducer Research Foundation.

a multimeter (Agilent 34401A). Current spinning was used to suppress offset errors [157] with an Agilent U2715A switching matrix (1 s/measurement).

A magnetic field was applied using a home-built and calibrated Helmholtz coil (up to ±5 mT) inside a zero-field Mu-metal chamber. Finite element modeling (FEM) with COMSOL(R) was leveraged to design a compact Helmholtz coil system to apply magnetic fields from −5 to 5 mT within 1 A of supply current (Figure 4.4a). Once the design was selected, a 3D-printed scaffold was made to support the hand-wound coils. Each coil pictured in Figure 4.4b is 250 turns of copper wire in a 1x1 cm cross-section. The Hall sensor is placed in the center of the coils through the top of the scaffold with a custom sample holder (not pictured). Since the fields being measured are relatively small, the entire setup was placed within three concentric magnetic shielding canisters made of MuMetal. This shielding reduced the background field to 6 µT, checked with a gaussmeter (1 nT resolution) from AlphaLab, Inc. The vertical coil pair, which was used in this study, was calibrated with another Gaussmeter (1 μT resolution, ±80 mT range) from AlphaLab, Inc. Once assembled, the entire set up was controlled using LabView (National Instruments) to control the current spinning, measurements, and magnetic field (Figure 4.4c).

4.2.3 Results

Hall Voltage

The net Hall voltage after current spinning is plotted with respect to magnetic field in Figure 4.5a and the residual offset was calculated from the x-intercept of the linear fit of these curves. Ideally, the x-intercept should be near zero, which would indicate a high accuracy sensor. However, the increased supply power seems to cause an additional offset that cannot be canceled with current spinning. Visualizing the data from another perspective (Figure 4.5b), the Hall voltage is compared to the supply voltage directly. It can be clearly seen that the data is skewed with a positive Hall voltage, especially at higher supply voltages as indicated in Figure 4.5b. When this offset voltage is removed from the measured data, the resulting calibrated data show Hall voltages linear with supply voltage. This further confirms the need for Hall calibration at high supply bias on the devices.

Sensitivity

Voltage-scaled sensitivity (S_V) for the two devices is shown in Figure 4.6. S_V was constant at 76 ± 2.5 mV/V/T, which is within 3% and has high linearity with respect to magnetic field. The small variations are subject to the power supply variation and slightly non-Ohmic nature of some

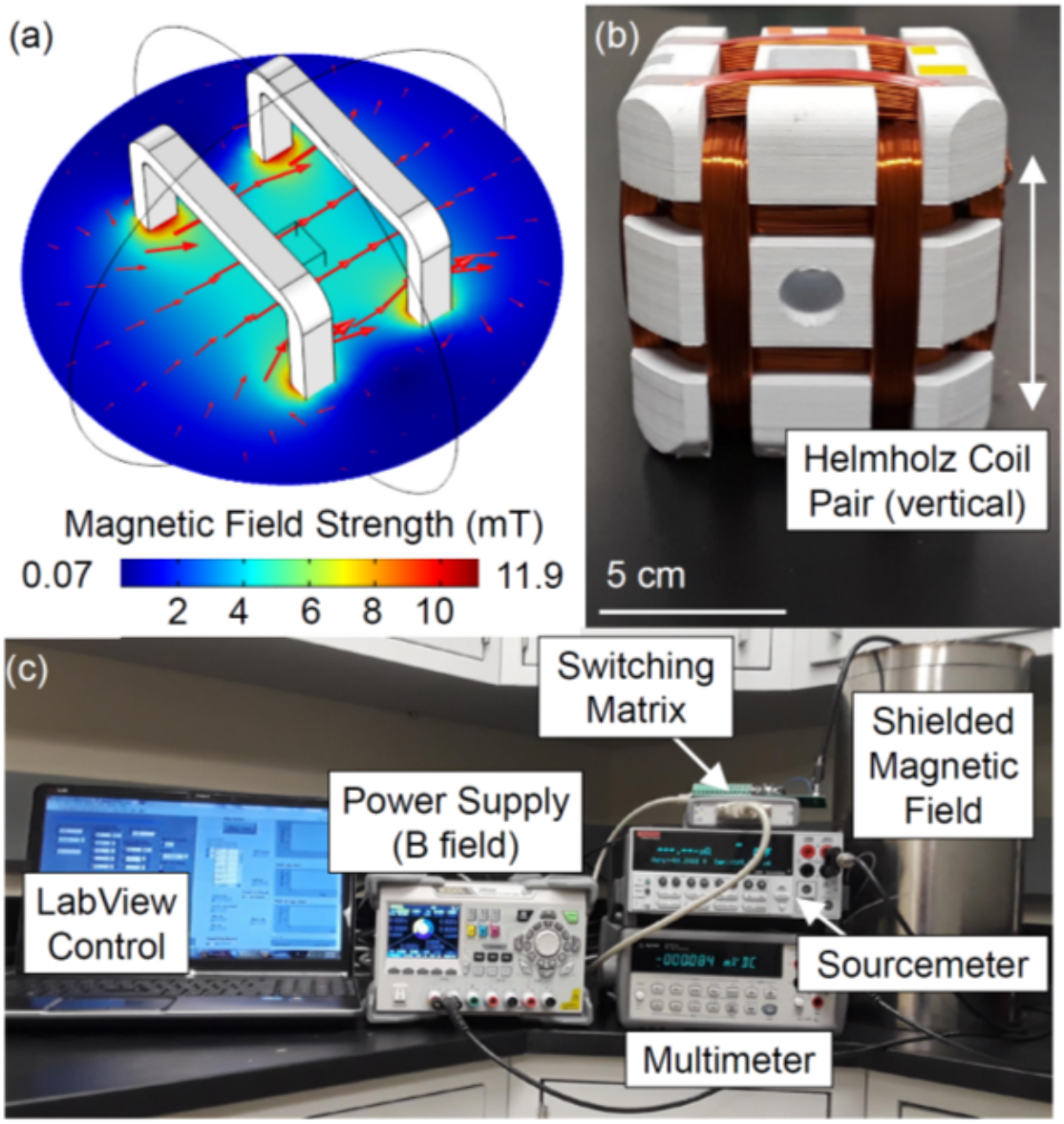


Figure 4.4: (a) Finite element model of the magnetic field profile from a Helmholtz coil with 250 turns of 9 x 9 cm of copper wire powered at 1 A. (b) Home-made Helmholtz coil pair using a 3D printed scaffold. (c) Complete test setup, the Helmholtz coil scaffold sits inside the shielding canisters. Reprint of Figure 3 in: Karen M. Dowling, Hannah S. Alpert, Pengxiang Zhang, Andrea M. Ramirez, Ananth Saran Yalamrthy, Helmut Köck, Udo Ausserlechner, and Debbie G. Senesky. "The effect of bias conditions on AlGaN/GaN 2DEG Hall plates." 2018 Hilton Head Workshop on Solid-State Sensors, Actuators and Microsystems, Hilton Head 2018 Technical Digest, reprinted with the permission of the author and the Transducer Research Foundation.

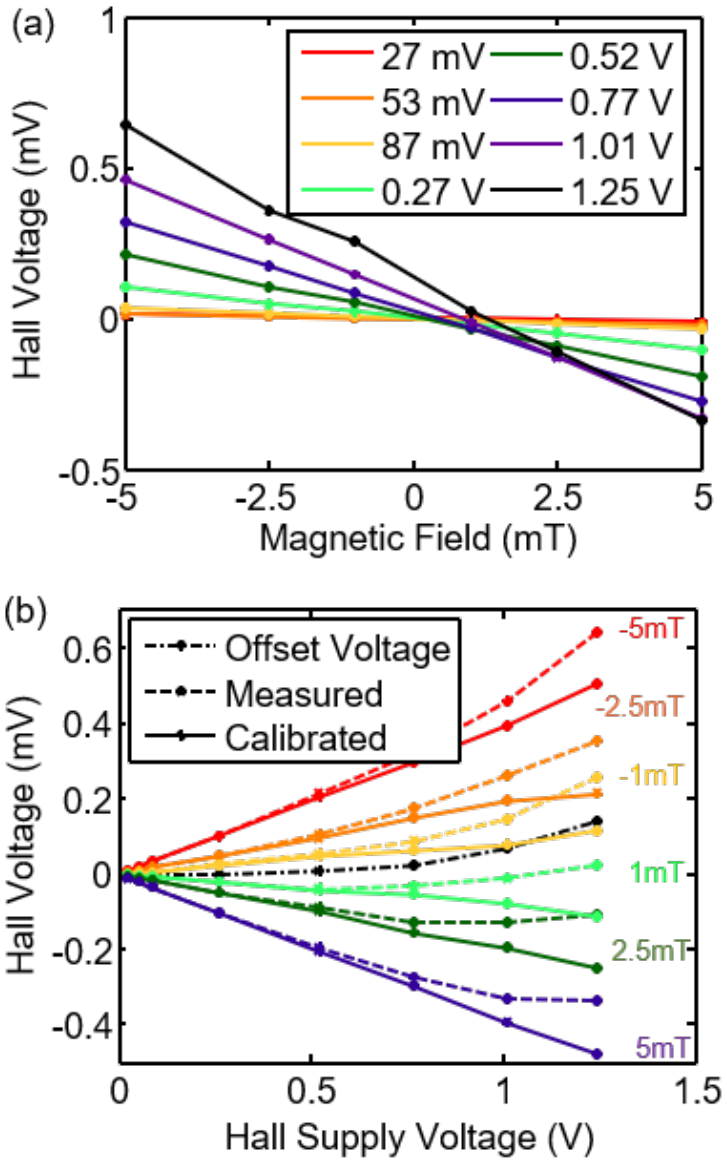


Figure 4.5: (a) Hall output voltages under varied magnetic fields and Hall supply current of sensor #1. (b) Hall output voltages before and after calibration by removal of residual offset voltage at each magnetic field condition. Reprint of Figure 4 in: Karen M. Dowling, Hannah S. Alpert, Pengxiang Zhang, Andrea M. Ramirez, Ananth Saran Yalamrthy, Helmut Köck, Udo Ausserlechner, and Debbie G. Senesky. "The effect of bias conditions on AlGaN/GaN 2DEG Hall plates." 2018 Hilton Head Workshop on Solid-State Sensors, Actuators and Microsystems, Hilton Head 2018 Technical Digest, reprinted with the permission of the author and the Transducer Research Foundation.

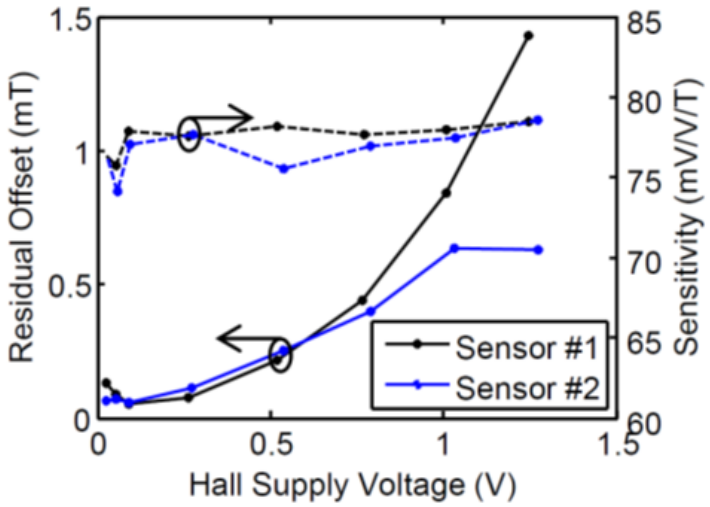


Figure 4.6: Residual magnetic offset of two AlGaN/GaN 2DEG Hall plates under varied bias voltages. Sensitivity (scaled with Hall supply voltage) under various supply voltages on the secondary axis. Reprint of Figure 5 in: Karen M. Dowling, Hannah S. Alpert, Pengxiang Zhang, Andrea M. Ramirez, Ananth Saran Yalamrthy, Helmut Köck, Udo Ausserlechner, and Debbie G. Senesky. "The effect of bias conditions on AlGaN/GaN 2DEG Hall plates." 2018 Hilton Head Workshop on Solid-State Sensors, Actuators and Microsystems, Hilton Head 2018 Technical Digest, reprinted with the permission of the author and the Transducer Research Foundation.

sensor contacts, which would affect the average supply voltage. Current-scaled sensitivity (S_I), similarly measured, is around 68 V/A/T ± 1.3 V/A/T. From these values, the sheet density was calculated to be 9.3 x10^{12} cm^{-2} and the mobility was calculated to be around 1635 cm^2/V-s. These values agree with similar 2DEG characteristics from previously reported values for AlGaN/GaN Hall plates [155, 156, 161]. Since the sensor shows relatively stable sensitivity, the residual offset must be addressed to enable AlGaN/GaN 2DEG Hall plates for extreme environment sensing.

Residual Offset

The residual offset is defined as the magnitude of magnetic field that is read in a zero-field. The x-intercepts from Figure 4.5a are shown in Figure 4.6. Here, the 2DEG Hall plates have residual magnetic offset values that are quadratically proportional to the supply voltage. Figure 4.6 shows that a residual offset as high as 1.4 mT is present at 1.25 V, which is over 60% of the measured signal at B = 1 mT. These results will be further examined in the discussion section below.

4.2.4 Discussion

The residual offset increases with supply voltage as a function of V^2. There are many possible physical mechanisms that contribute to the increase in residual offset with supply voltage. The potential contributions to the nonlinear offset are summarized in Table 4.2 [4, 38, 157, 162–164] and are discussed in this section in detail.

Table 4.2: Possible contributions to increase in residual offset with high bias conditions.

Offset Source	Explanation
Seebeck Voltage	Increase in residual offset directly proportional to input power, combined with inhomogenous current density around defects and contacts causes localized heating [4, 162, 164]
Buffer effect	Underlying GaN substrate induces Hall voltage prominent at higher bias conditions. [157]
Packaging	Packaging Thermal and mechanical stress in substrate and packaging from high bias operation [38]Also induced magnetic fields from bond wires [164]
Asymmetry	Linear imbalance due to geometrical asymmetries is removed with current spinning, Nonlinear effects remain [38]

The first contribution is due to thermoelectric effects from self-heating. The increase in supply voltage (and supply current) corresponding to an increase in operating power of the Hall plate. Power (P) increases with V^2/R (and I^2R), which causes the device to increase in temperature (ΔT). The device is an octagonal Hall plate, but the highest current concentration is across the supply contacts, so the majority of heating occurs across the octagon length (L) and contact width (W). Using Equation 4.1,

$$\Delta T = \frac{P}{4k_{GaN}\sqrt{WL}} \tag{4.1}$$

an estimated average temperature rise of at least 65 mK in the current path is expected, assuming an in-plane thermal conductivity (kGaN) of 115 W/m-K [4]. AlGaN/GaN 2DEG devices have been recently reported to have a lateral Seebeck coefficient of 120 µV/K [4] at room temperature. Thus, the thermal gradients generated in the Hall plate from high supply voltages could be generating an additional voltage measured on the Hall contacts, regardless of measurement orientation or external magnetic field direction.

The second potential contribution to residual offset could be due to underlying material buffers. Larger supply voltages (and currents) could start to cause a portion of the current to flow through underlying buffer structures (Figure 4.2a). When the current values get large enough, this buffer could be causing an additional contribution of Hall voltage to the sensor. However, the Hall plate still has constant S_V at high supply voltage, and a buffer component would alter the sensitivity, which is not seen here.

A third potential source of the residual offset could be from packaging. Strain has been reported to cause an increase in residual offset in silicon devices, due to the directional change in resistance from its asymmetric piezo-resistive components. Analogously, the AlGaN/GaN 2DEG forms from a combination of spontaneous and piezoelectric polarization, so any strain from packaging could cause local changes in the 2DEG concentration, and thus would contribute to resistance asymmetry. In addition to packaging stress, these sensors were electrically connected using wirebonding with different wire layouts. At higher supply power, the induced magnetic field of the wirebonds could interfere with the device measurement. However, simple finite element modeling predicts this additional external field to be around 12 µT when supplied with 1 V, much smaller than the measured conditions.

The final contribution mechanism considered here is the linear imbalance from fabrication. Current spinning successfully removes linear offsets in contact resistance from lithography misalignment. However, nonlinear differences in contact resistance from misalignment remain (ΔR is not constant between measurement phases). Our sensors had up to 60 Ω difference between the orthogonal current paths in the sensor, which is around 7% change between lateral and longitudinal directions of current spinning. This could contribute to a nonlinear offset in V_{Hall} that scales with increased current. This could be improved with tighter fabrication tolerances in future work.

4.2.5 Conclusion

Here, we presented work on AlGaN/GaN 2DEG Hall plates with high, stable sensitivity values, which match results of Si-based Hall plates found in the literature and even slightly better sensitivity due to higher electron mobility. Current spinning was used to reduce the offset voltages, but there were large residual offsets when biased with a large supply voltage. This is particularly problematic when operating to sense small magnetic fields (<5 mT). While AlGaN/GaN sensors are of interest for extreme environment applications, these electrical operation conditions need to be further understood for proper calibration and use. We discussed some key factors that cause residual

offsets, including self-heating and nonlinear contact resistance asymmetry. Future work should focus on reducing the causes of large signal offset to enable improved sensing capability. Regardless, this work confirms that AlGaN/GaN 2DEG Hall plates could be used as magnetic field sensors and offers a monolithically integrated sensing solution for GaN power electronics, as well as harsh environment operation

4.3 Micro-Tesla Offset in thermally stable AlGaN/GaN 2DEG Hall Plates[†]

This section describes the characterization of the second generaion, low-offset Hall plate using the AlGaN/GaN 2-D electron gas (2DEG). A four-phase current spinning technique was used to reduce the sensor offset voltage to values in the range of 20 nV, which corresponds to a low residual offset of 3.4 ± 2 µT when supplied with low voltages (0.25-1 V). These offsets are 30× smaller than the values previously reported for GaN Hall plates, and it is on par with state-of-the-art current-spun silicon (Si) Hall plates. In addition, the offset does not exceed 10 µT even at a higher supply voltage of 2 V.Current spinning was done with a relay matrix at a switching frequency of 1 Hz to enable an offset reduction. The sensor also shows stable current-scaled sensitivity over a wide temperature range of 100℃to 200℃, with a temperature coefficient of ∼ 100 ppm/℃. This value is at least 3× better than the state-of-the art Si Hall plates. Additionally, the sensor's voltage-related sensitivity (57 mV/V/T) is similar to that of the state-of-the-art Si Hall plates. Because of the low offset values enabled by current spinning, these AlGaN/GaN 2DEG Hall plates are viable candidates for low-field current and magnetic sensing in high-temperature environments.

4.3.1 Introduction

Magnetic field sensing is widely used for both direct purposes such as navigation using the Earth's field and for indirect purposes such as motor position or current monitoring. In most applications, the ideal magnetic field sensor would exhibit a high sensitivity to maximize the output signal, and low offset to accurately detect small fields. While giant magnetoresistance (GMR) and tunnel magnetoresistance (TMR) sensors have the highest sensitivities, they suffer from hysteresis, behave non-linearly, and have large offsets in DC applications [165]. Hall plates have better linearity than

[†]

such devices and are easily fabricated in integrated circuit (IC) device technology. Current spinning can further mitigate raw offsets in Hall plates without the need for external calibration [38,39,43,166] [158, 167, 168] [40, 41, 157, 160, 169]. This strategy takes advantage of device symmetry to subtract small nonidealities and create a Hall voltage with near-zero offset. Current spinning in devices with bulk-film doping was popularized by Munter in 1989 [38], leveraging complementary metal-oxide-semiconductor (CMOS) analog technology. Recent work shows that this approach can also be used to reduce offsets in two-dimensional electron gas (2DEG) structures, such as those based on GaAs [45, 170]. This same technique can also benefit GaN devices, enabling low offset, highly sensitive Hall plates that could be monolithically integrated with power devices for in-situ current monitoring and eventually GaN IC's [161, 171–173], as well as high temperature operation.

In this section, we examine the offset with current spinning of 2DEG Hall plates for the first time. We implemented a 4-phase current spinning technique to significantly reduce sensor offset from milli-tesla to the order of micro-tesla. Our measured offset values are comparable to the lowest obtained values for Si Hall plates using similar spinning methods [39, 43, 158] and are much smaller than those previously published for GaN [161,174,175](and that in the preivous section). Our sensor also exhibits sensitivities similar to that of previous GaN and Si Hall plates [155,156,161] [159,176]. Finally, we characterized the device in a temperature range of 100℃to 200℃. This device is therefore competitive with silicon (Si) Hall plates on all considered metrics, as summarized in Table 4.3.

Table 4.3: Calculated sensor's sensitivity and coefficient of determination values using linear curve fitting method.

Material	S_I[a] (V/A/T)	S_I TC[b] (ppm/℃)	S_V[c] (mV/V/T)	Residual Offset[d] (μT)
Si [158, 159, 164, 167, 168, 176]	107	300–800	33–72	2.5
AlGaN/GaN 2DEG [150, 155, 156, 161, 174]	15–113	102	76	100
This Work	89	100	57	3.4 ± 2

[a] Current-scaled sensitivity.
[b] Temperature coefficient
[c] Voltage-scaled sensitivity
[d] Supply voltages range from 0.1-2V across literature

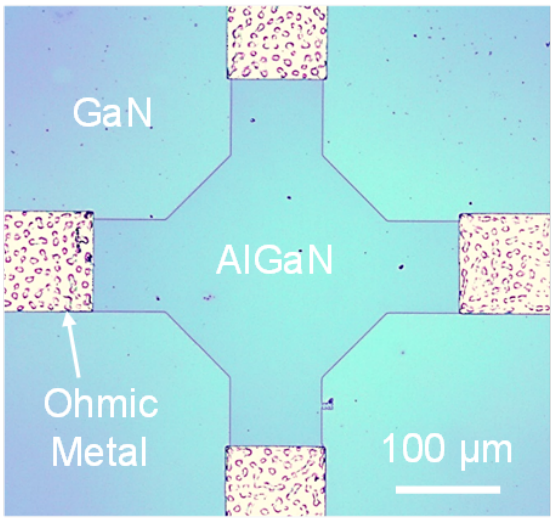


Figure 4.7: Optical image of the AlGaN/GaN 2DEG Hall plate.

4.3.2 Background

The AlGaN/GaN sensor operates via the Hall-effect [169]; supply current is applied across the sensor pictured in Figure 4.7, and in the presence of a magnetic field a Hall voltage is measured across the other two electrodes. Two metrics of interest for Hall sensors are sensitivity scaled with supply current and voltage (S_I and S_V). S_I has an inverse relationship to the sheet density of the 2DEG, and S_V is directly proportional to the electron mobility in the 2DEG. S_V and S_I are also related to the geometrical shape of the plate, which is the focus of other recent work [6].

In addition to sensitivity, offset is a key metric of interest for low field magnetic sensors. Key sources of measured Hall-effect offset voltages are from resistive asymmetry due to device fabrication and material defects, asymmetric self-heating, and packaging effects [150, 164]. This diverse set of contributions leads to a varied offset voltage in different measurement configurations. In particular, measurements taken with 90° rotated source and sensor electrodes will have offset voltage with opposite polarity, as shown in Figure 4.8 (Phase A, B, C, and D). Offset reduction with current spinning is possible due to this switching polarity (from static offset sources such as resistance asymmetry), and one can calculate the true Hall voltage from these 4 unique Hall voltage configurations ($V_{\text{A–D}}$). This can be understood by a simple Wheatstone bridge representation of a Hall plate, described elegantly by Bilotti et al. in 1997 [39]. Static, linear offsets are removed with 4-phase current spinning using (4.2),

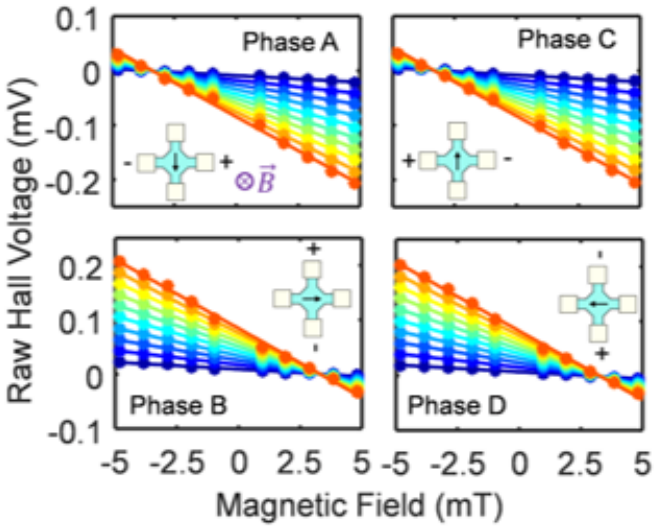


Figure 4.8: Raw Hall voltage with respect to magnetic field under varied supply current (30 µA to 300 µA) for the 4 different current spinning phases. Insets show measurement configuration used for each phase: arrow indicates supply current, and "+" and "−" indicate Hall voltage measurement terminals.

$$V_H = \frac{V_A + V_B + V_C + V_D}{4} = S * B + V_{O,res} \tag{4.2}$$

When applying this calculation, only the induced voltage from the product of the magnetic field (B) and sensitivity (S), as well as the residual offset voltage ($V_{O,res}$) from imperfect cancellations between the different measurement phases remain. After Equation 4.2 is implemented with the raw voltages in Figure 4.8, near-zero offsets can be achieved as shown in Figure 4.9.

4.3.3 Methodology

Fabrication

Devices were fabricated with a metal-organic chemical vapor deposited AlGaN/GaN on <111> Si substrate purchased from DOWA, using the same process of that of Satterthwaite et al. in 2018 [5]. The wafer has a manufacturer-specified mobility of 1400 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$, and sheet density $>9 \times 10^{12}\,\mathrm{cm}^{-2}$. We obtained a sheet resistance of 430 $\Omega/\square$ and contact resistance of $1 \times 10^{-5}\,\Omega\cdot\mathrm{cm}^2$ as indicated from transfer length method [177] measurements using dedicated structures fabricated on the same wafer. The device was then wire-bonded with bond pads far from the active sensor to a printed circuit board (PCB) for testing. An image of the Hall plate is shown in Figure 4.7.

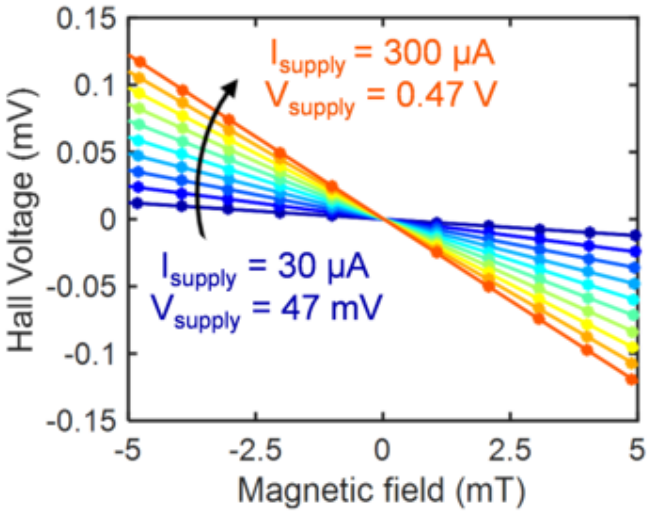


Figure 4.9: Hall voltage (via current-spinning) with near-zero offset with respect to magnetic field under varied supply current (30 µA to 300 µA).

The device is a modified 200-µm-diameter octagon with 70-µm-long legs extending from 4 sides for electrical contact. These legs are meant to eliminate the effect of contact alignment on the active device area [150]. The device can also be thought of as a Greek cross with chamfers to reduce electric field spikes at sharp corners. The longitudinal resistance was $1560 \pm 3\,\Omega$, which is only 0.2% asymmetrical.

Test Set-up

Our test apparatus implements current spinning using the same procedure described previously. The device was tested in constant-current operation (30 µA to 1.5 mA) using a Keithley 2400 current sourcemeter connected across the plate. An Agilent 34401A voltmeter was used to measure the generated Hall voltage across the other contacts. A switching matrix (Agilent U2715A) was used to alternate the connections across the contacts to create 4 unique phases (Figure 4.8). The offset of the voltmeter was cancelled out by reversing its polarity once per voltage measurement and subtracting both values and dividing by two, thus eight total configurations (switched at 1 Hz) are used as previously described in literature [45]. These measured voltages are then averaged to calculate the low offset signal. Residual offsets were measured in a near-zero magnetic field chamber composed of 3 concentric canisters made of MuMetal® shielding. To determine the background voltage from

measurement equipment (thermal emf and multimeter offset), measurements were repeated with a Wheatstone bridge of 1 kΩ resistors, which should ideally have zero offset, and showed a maximum average current spun signal of only 20 nV (shaded region in Figure 4.10). The magnetic field was applied via a home-made Helmholtz coil apparatus from −5 mT to 5 mT, calibrated with a high-sensitivity gaussmeter probe (GM2, AlphaLab, Inc). We also examined the influence of temperature on sensitivity from −100℃ to 200℃, in a similar unshielded test apparatus. All measurements were done with supplied constant current, but we display our results with the averaged measured supply voltage for simpler comparison between device technologies.

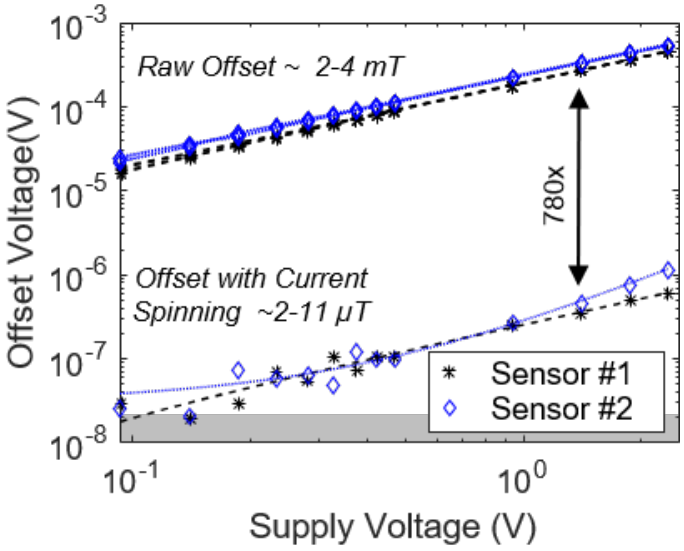


Figure 4.10: Magnitude of average offset voltage (raw and residual) with respect to measured supply voltage under constant-current scheme. Residual offset voltage is fit with second order trendlines. Shaded region refers to the measured electrical measurement limit.

4.3.4 Results and Discussion

Residual Offset

Figure 4.10 compares the magnitude of the raw offset voltage of the 4 unique phases measured, to the residual offset voltage after applying current spinning. The average residual offset voltage varied from 36 nV to 1.12 μV as supply voltage increased from 92 mV to 2.34 V (60 μA to 1.5 mA supply current). Across this bias range, the overall attenuation of raw to residual offset voltage is ~780, a significant improvement in minimum resolvable signal.

Typically, offsets voltages between different sensor technologies, are translated to magnetic offset values for comparison. Magnetic offset is then calculated by dividing the average offset voltage with the sensitivity. In Fig 4.11, the residual magnetic field offset for two different sensors is shown. Magnetic field offsets are as low as 3.4 µT and increase to only 11 µT at a measured supply voltage of 2.34 V. Differences in offset between sensors are likely due to varied wire bond placement from the assembly process and resulting magnetic field induced from the wire.

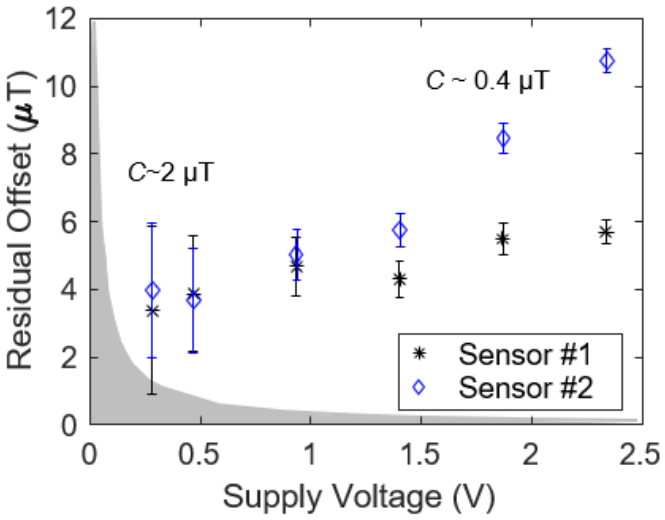


Figure 4.11: Magnetic residual offset with respect to measured supply voltage under constant-current scheme, with 1-σ confidence (C) scale bars. Shaded region corresponds to the electrical measurement limit.

Due to limitations in the measurement equipment, the standard deviation of residual offset voltage is ~0.63 µV regardless of supply conditions, which implies larger errors at lower supply voltages. We repeated offset voltage measurements 300 times at each supply condition and averaged the final offset value to reduce stochastic noise. We then calculate the confidence of the offset measurement by taking the standard deviation of the magnetic offset divided by the square root of repeated measurements. When the measured supply voltage was as 0.28 V, the confidence value was 2 µT then decreased at higher supply conditions to 0.4 µT. One could operate the device at these higher voltages (1 to 2 V) to have lower thermal noise in a practical measurement application.

Magnetic field offset values in current-spun Si Hall plates have been reported as low as 2.5 µT with similar improvements in ratio with raw offset [38–40, 160, 167]. The lowest offsets resolved here were comparable ($3.4 \pm 2.0\,\mu T$). Thus, GaN Hall plates benefit from current spinning methods in a similar fashion to that of Si Hall plates.

Sensitivity

At 25℃, the voltage and current-scaled sensitivities measured for the AlGaN/GaN 2DEG Hall-effect plate are 57 mV/V/T and 89 V/A/T, respectively. These values are respectively slightly lower and higher than previously reported GaN 2DEG Hall plate sensitivity values [150, 155, 156, 161]. This discrepancy is due to the device geometry—this design has additional resistance from the contact legs. This lowers S_V by reducing the voltage drop across the active region and increases S_I with the higher resistance. The sensitivities have since been increased in AlGaN/GaN 2DEG Hall Plates through optimized design of the Hall-effect plate geometry [6].

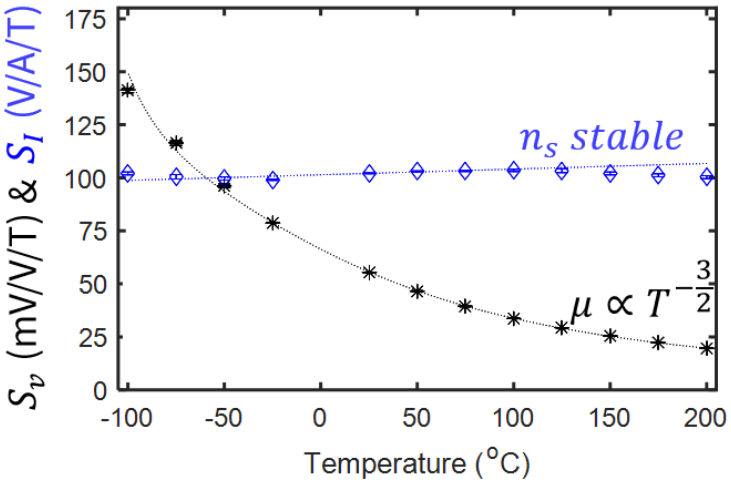


Figure 4.12: Hall plate sensitivity scaled with voltage (S_V) and current (S_I) averaged over supply voltages from 0.3 V to 1 V, across various temperatures. S_V has fit with $T^{-3/2}$, and S_I remains fairly constant.

The voltage and current-scaled sensitivities measured from 100℃ to 200℃ are shown in Figure 4.12. S_V increases by 180% from 25℃ to 100℃ and decreases by 60% from 25℃ to 200℃, because it is directly related to electron mobility. The sheet resistance, inversely proportional to mobility, increases by 130% from 430 Ω/□ at 25℃ to 1 kΩ/□ at 150℃. S_I, however, remains fairly stable with measurement drift within 1.8% of its room temperature value. The measured temperature coefficient (TC) of the average S_I of this 2DEG Hall-effect plate is approximately 100 ppm/℃, consistent with previous reports [155,156]. This is an advantage of AlGaN/GaN in extreme environments: the 2DEG sheet density formed by the crystals spontaneous and piezoelectric polarizations, is invariant in this temperature range [154, 178]. However, the sheet density in Si-based devices is from external ionizing dopants, so its S_I TC is larger (336 ppm/℃ to −800 ppm/℃) [37,159]. There

is at least 3x stability improvement for the AlGaN/GaN Hall-effect plate due to lack of thermally induced intrinsic carriers. Thus, when temperature stability is required in an extreme environment, 2DEG Hall plates should be implemented with constant-current interface circuits.

4.3.5 Conclusion

In this section, we presented a 2DEG GaN Hall plate with record low offset of 3.4 µT (~7% of Earth's magnetic field), which is on par with the best reported silicon Hall plate offsets. We accomplished this by using a 4-phase current spinning technique to reduce the raw offset in AlGaN/GaN 2DEG Hall plates by 3 orders of magnitude. We also confirmed robust sensor operation at extreme temperatures from −100℃ to 200℃. Since current spinning enables quality low-offset GaN Hall plates on par to those of silicon, it is ready for next steps towards system level integration. Future research should create the proper on-chip AlGaN/GaN amplification and current spinning circuits to enable a low offset, monolithically integrated solution for magnetic field sensing in harsh environments. Once achieved, GaN magnetic-field sensors may be a competitive sensor solution for power systems, autonomous position sensing, and novel space exploration applications.

Chapter 5

Fundamental Limits of AlGaN/GaN Hall Plates

5.1 Overview

The previous chapter showed how the use of current spinning reduces raw offsets by a factor of 1000 in AlGaN/GaN devices. However, some residual offsets remained in both the Gen 1 and Gen 2 devices. This chapter will cover the fundamental sources of residual offset and provide recommended practices to reduce offset in AlGaN/GaN devices. The final section in the chapter will then go over fundamental sources of noise in these Hall-effect plates, which can educate current spinning and sensor systems for practical deployment.

5.2 Small, Stable Offsets at High Bias Conditions in AlGaN/GaN Hall Plates

The previous chapter showed an AlGaN/GaN 2DEG Hall plate with residual offsets on the order of 3 to 11 µT, which we later found to be the limits of that measurement set up. With an improved test apparatus (stronger MuMetal® Shielding verified with calibrated milligaussmeter), the residual offsets of four different AlGaN/GaN devices from 2nd generation (including the two from the previous study) were confirmed to be 0.5–3 µT. In addition, key factors that contribute to offset in GaN

2DEG Hall plates were identified and mitigated. This section will summarize the key factors that were identified and mitigated to improve the offset.

5.2.1 External Causes of Residual Offset

Stray magnetic fields from unexpected sources are known as external causes of offset. For example, non-shielded sensors will detect Earth's magnetic field (50 µT), which will register as an offset during device measurement. Thus, care to shield these devices is crucial for accurate zero-field measurements. Overall, three sources of external fields were identified: poor shielding, magnetized packaging, and wirebond placement. These are addressed in the following subsections.

Shielding

MuMetal® is a commercially available magnetic shielding material which has a high permeability. The initial test apparatus was made with another (more affordable) shielding material with similar properties, but it had a lower shielding capability. This was confirmed with multiple measurements with the same sensor in both cannisters (Figure 5.1). This was also confirmed with a calibrated milligauss meter: the old chamber measured fields on the order of 5–10 µT, and the new chamber had stray fields only from 30–70 nT.

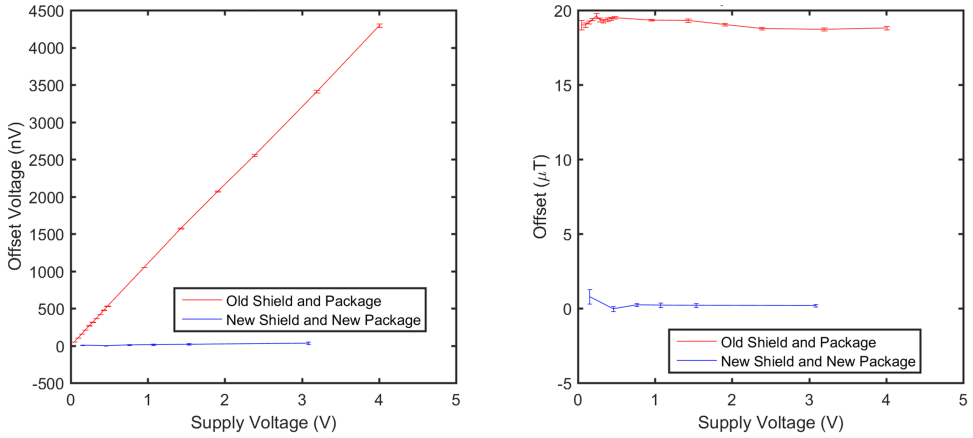


Figure 5.1: Residual offset measurements with a Gen 2 Hall sensor in the old cannister and the new ones. It is clear that the sensor was not properly shielded before and a stray field was being detected. (a) Residual offset voltages of Gen 2 AlGaN/GaN Sensor #3 (b) Equivalent magnetic offset of Gen 2 AlGaN/GaN Sensor #3 calculated from $S_I = -85$ V/A/T.

In addition, Gen 2 sensor #1 and #2 were also measured in upward and downward configurations in the new shielding. This meant any measured offset which flipped polarity corresponded to influence of a stay field. We saw mirror images of measured offset for the same device flipped in both orientations, as shown in Figure 5.2.

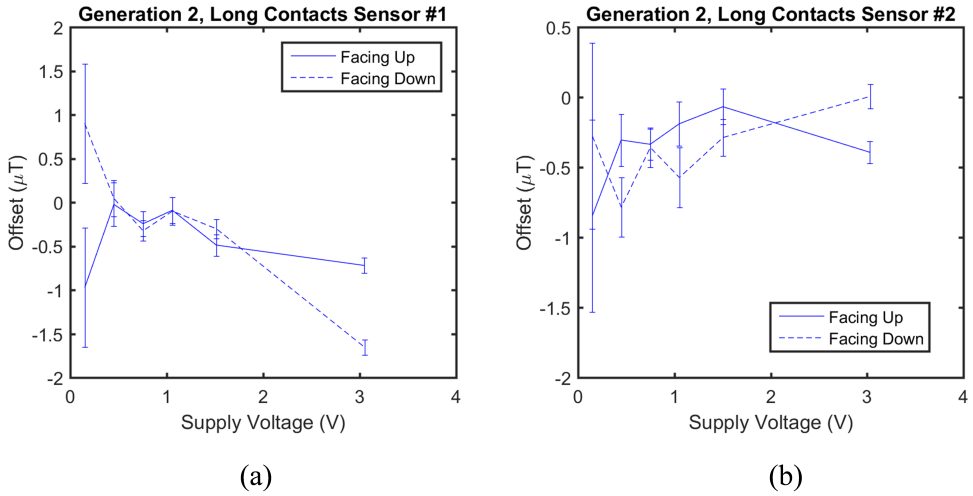


Figure 5.2: (a) Gen 2 AlGaN/GaN sensor #1 from (Figure 4.10, measured in the newly shielded setup, facing both upward and downward in the system. (b) Gen 2 AlGaN/GaN sensor #2.

Magnetized Packaging

The sensor package was also stored in the laboratory near the wall, by a power line. In addition, the sensor packages contain ferromagnetic materials—nickel, in particular. Thus, improper storage can lead to a small magnetization in these packages which was measured to be on the order of 10–40 µT. This can be reduced through mindful storage of packaging materials in shielded areas away from large magnetic fields. Figure 5.3 shows some of the offset measurements which led to this finding.

Wirebond Placement

Previous work has shown the influence of wires on Hall-effect sensors [164]. Current flowing through a wire will induce a magnetic field which is perpendicular to that wire. The field induced is related through the Biot-Savart law, which was described in Chapter 1, Equation 1.2. When in air, this corresponds to a 1 mA current flowing through a bond wire 100 µm away will induce a magnetic

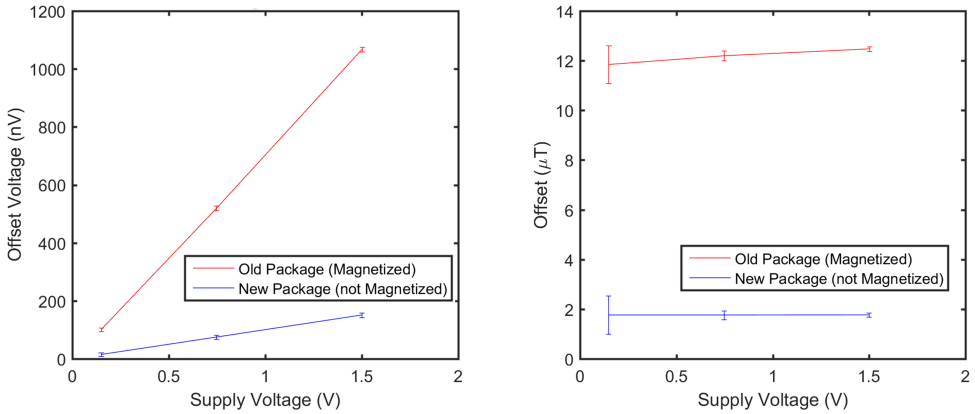


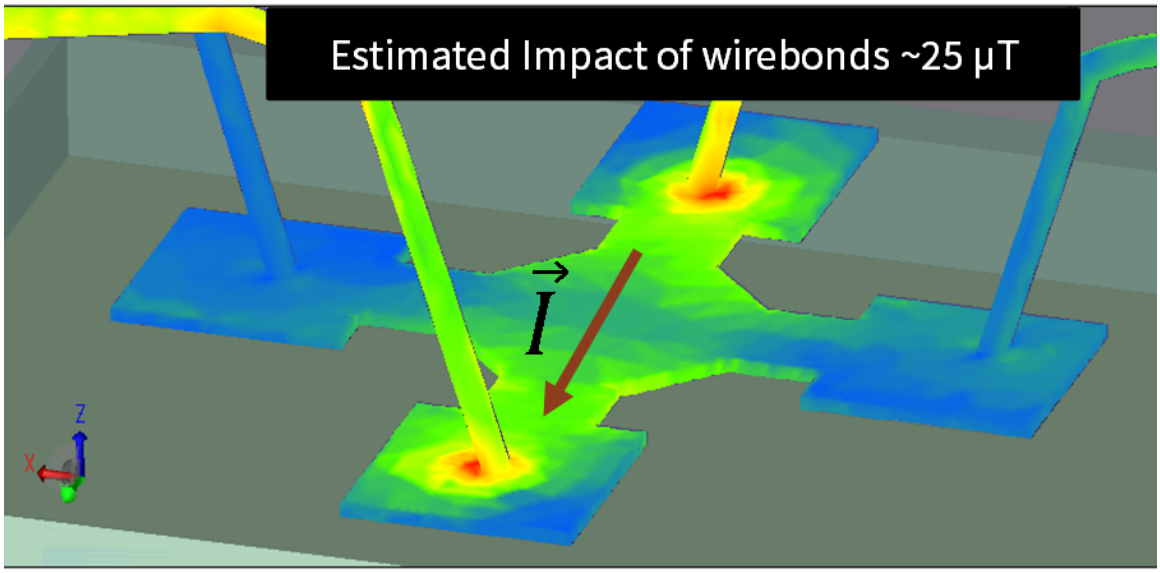
Figure 5.3: Sensor #1 from Figure 4.10, measured with an older PCB and a new one. The old board was magnetized, which was removed and the sensor remeasured with a new PCB package.(a) Residual offset voltages (b) Equivalent magnetic offset calculated from $S_I = -85$ V/A/T.

field of 2 µT. The wire distance changes, but its distance is approximately between 100 µm and 1 mm. Figure 5.4 compares the recent best Hall data to this 1D limit.

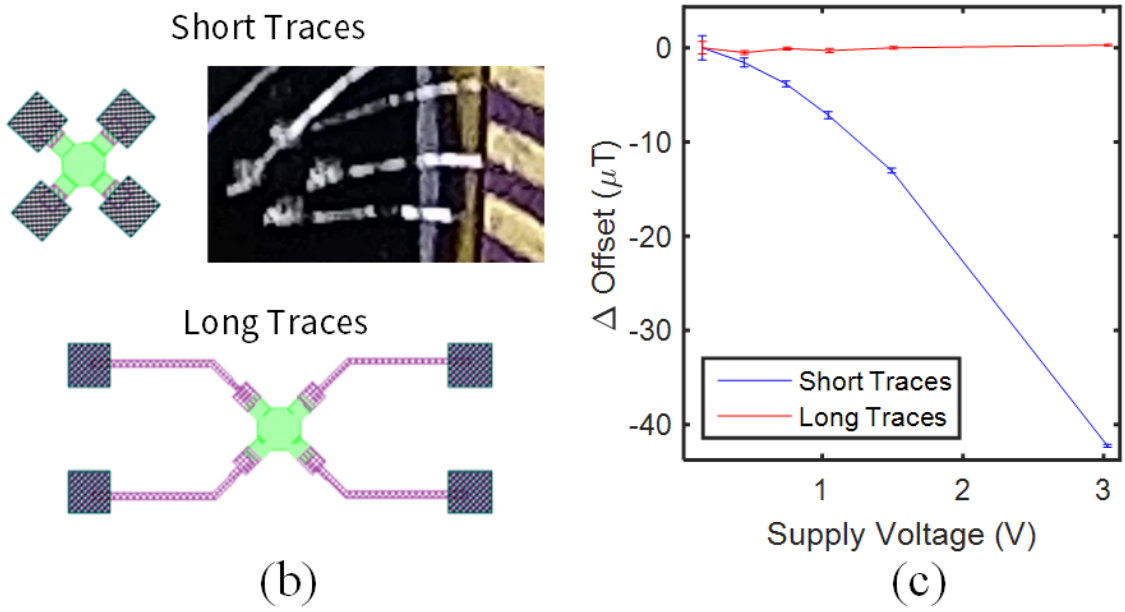
This effect is easiest to see between devices with varied placement of bondpads. Bond pads close to the device will have more wires cross over the device, which will induce measurable fields. This was consistent between devices on the same chip longer traces (bond pads farther away) devices had lower offsets than devices with shorter traces (bond pads adjacent to device), as shown in Figure 5.4.

Measurement Equipment Limitations

Another source of external offset comes from the equipment for the offset measurement. Unlike the other sources, this one is not directly a magnetic field. Switching relays generate a thermal electromagnetic interference voltage (quoted up to 3 µV in the the switching matrix datasheet), which will contribute to the measured signal. In addition, the multimeter has a large noise floor of 1.5 µV (according to spec). This means residual offsets smaller than 1 µV will be drowned in measurement noise. This can be confirmed with testing a non-magnetic Wheatstone bridge, which should have an ideal measurement of 0 V after current spinning. In our work, we found the measurement limit to be closer to 20 nV for the Wheatstone bridge (Figure 5.5).



(a)



(b) (c)

Figure 5.4: (a) Finite element simulation showing approximate magnetic field strength due to induced magnetic fields from wirebonds. EMP Pro. Image credit: Max Holliday. (b) Drawings of two Hall device designs with short and long metal traces. Longer traces move wirebonds away from active area of device. (c) Residual offset data from long and short trace devices from Generation 2.

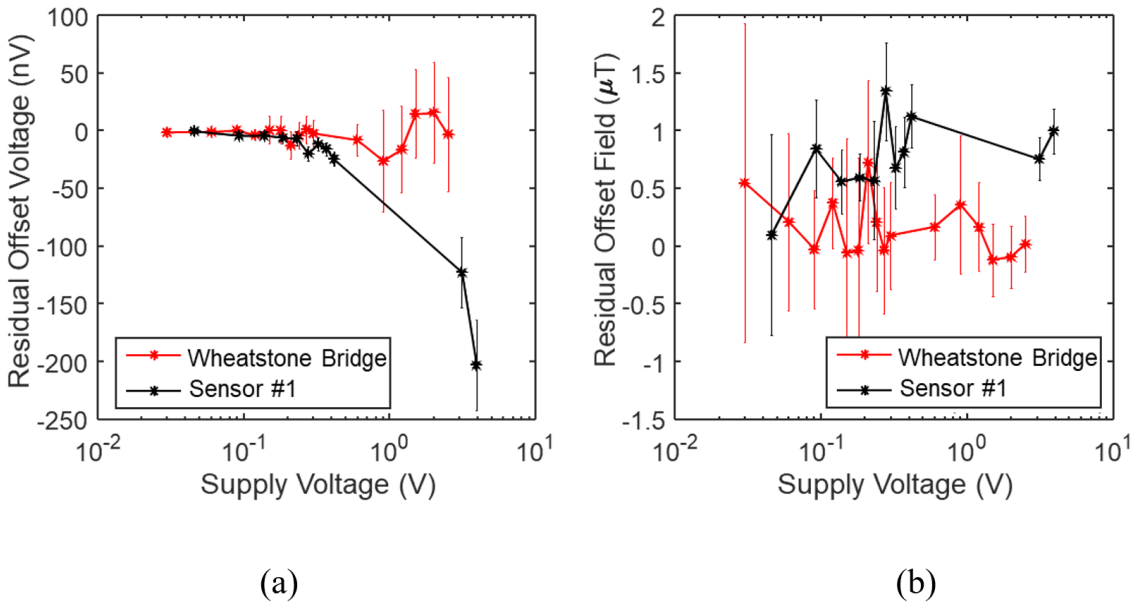


Figure 5.5: Wheatstone Bridge measurements compared to Sensor #1 from Figure 4.10.

5.2.2 Internal Causes of Residual Offset

There are also intrinsic offset sources. These correspond to offset voltages generated due to properties of the Hall-effect plate or its inherent material quality. In particular we identified that resistance asymmetry and self-heating are major offset contributions. Other sources not covered in this study are summarized at the end of this section.

Dynamic Resistance Asymmetry (Residual) Silicon vs. GaN

Current spinning can remove static resistance asymmetry, as we saw previously, but this cannot remove effects that are due to the bias conditioning, as we saw in Chapter 4. For example, the wirebond magnetic field cannot be removed because the activation will vary between phases a different wire will create the parasitic field in each phase of the circuit. Internal device behavior will also suffer from these dynamic switching changes.

Silicon devices suffer from dynamic resistive asymmetry. The conduction layer is formed through doping the silicon substrate thus a p-n junction exists between the device layer and the substrate. P-n junctions are known to have a depletion region in equilibrium. When the device is turned on, a reverse bias forms at the high voltage node, described in Figure 5.6a. This constricts conduction

paths in the Hall device, which causes an asymmetric resistance with respect to supply voltage. This will further increase offset voltage during operation, and will propagate through the current spinning scheme, as shown in previous work on silicon plates [179]. In our commercial Si samples from Infineon, we measured a resistance change of 5%/V and offsets ranging from 3µT to 15 µT, shown in Figure 5.6b .

The 2DEG is the main conduction layer in GaN Hall-effect plates, and has less resistive influence from substrate bias. The lowest energy state for the electrons is in the quantum well of the 2DEG, and it takes a large bias voltage to overcome this potential. Previous work has shown substrate leakage in GaN-on-Silicon systems does not occur until much larger potentials (>100 V), due to the low doping in the GaN, buffer layers, and the silicon substrate [180]. The junction voltages in the silicon device (up to 3V) are much smaller than these potentials, which do not alter the device layer in the GaN devices. Our samples measured a resistance change of 0.5%/V, which is likely due to self-heating in the structure, and not a 2DEG concentration variation. This likely explains the much lower offset measurements we saw of 0.5–3 µT. Figure 5.6 shows a direct residual offset comparison between this silicon and AlGaN/GaN devices from Gen 2.

Seebeck Effect

We also observed thermal gradients in Gen 1 GaN devices. The power density of device operation can cause Joule heating in devices, which will create thermal gradients within the device. These thermal gradients can generate a thermoelectric voltage through the Seebeck effect. Thus, a moving hotspot (due to a moving current source) will generate a moving thermal gradient, which will not perfectly cancel in an asymmetric device, and will lead to large thermal-generated offset voltages. These large offsets were shown earlier in Chapter 4.

We confirmed the presence of thermal gradients with an infrared microscopy measurement technique. The device was measured on a heated chuck at 45°C, and live video was taken while the device was being current spun at a large power (3-9 mA were input as current supply). These screenshots are shown in Figure 5.7. As we can see, devices from the earlier generation had current crowding issues that led to generation of large hotspots, which varied in the 8 measurement phases. However, the later generation devices, show some heating between phases but no noticeable thermal gradients. This hints that the wider contact design Gen 2 onward reduced current crowding and mitigated this effect.

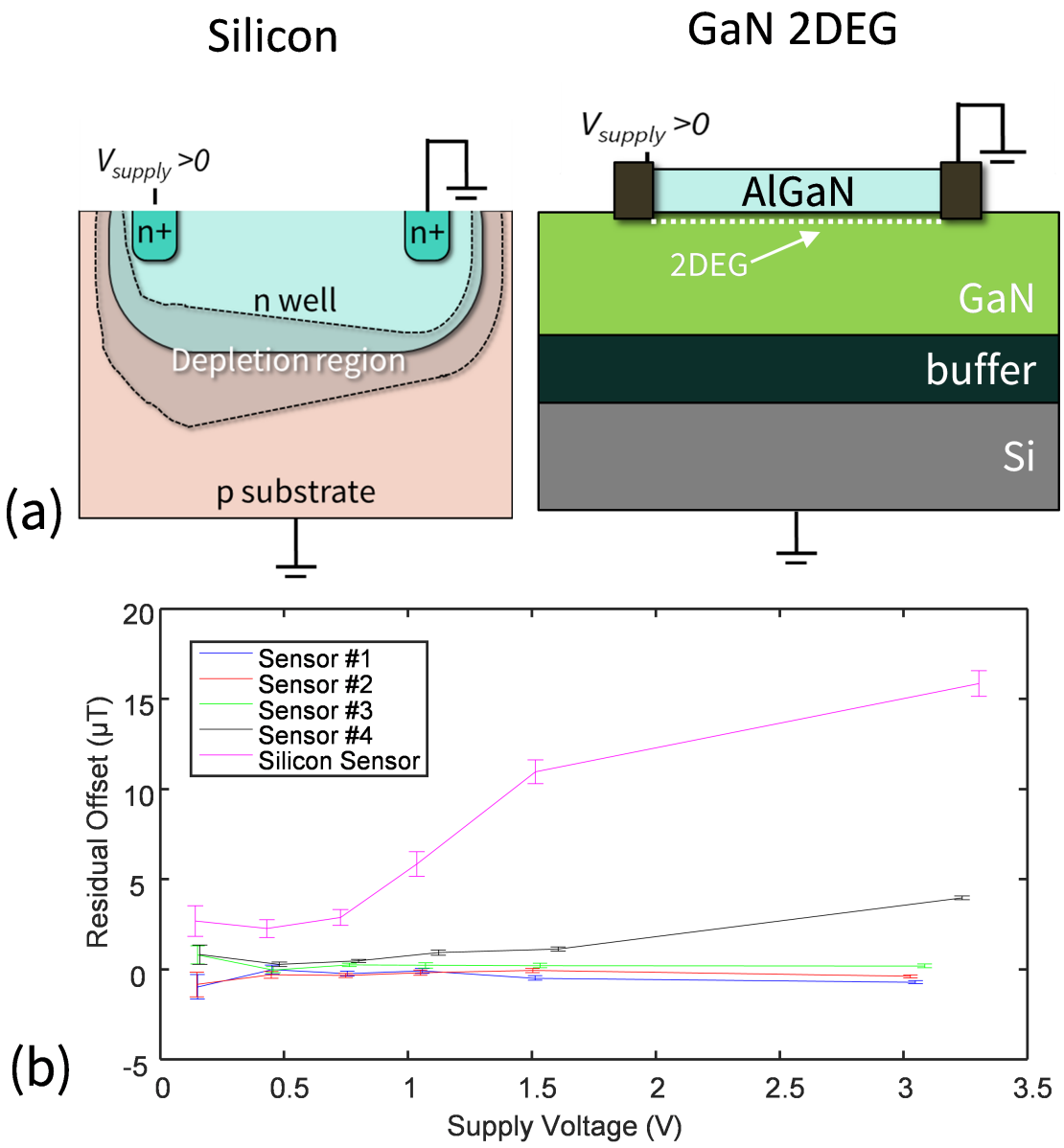


Figure 5.6: (a) Drawing showing comparison of Silicon device in operation to 2DEG. (b) residual offset measurements of Si Hall-effect plate and AlGaN/GaN 2DEG Hall-effect plates with high bias voltage.

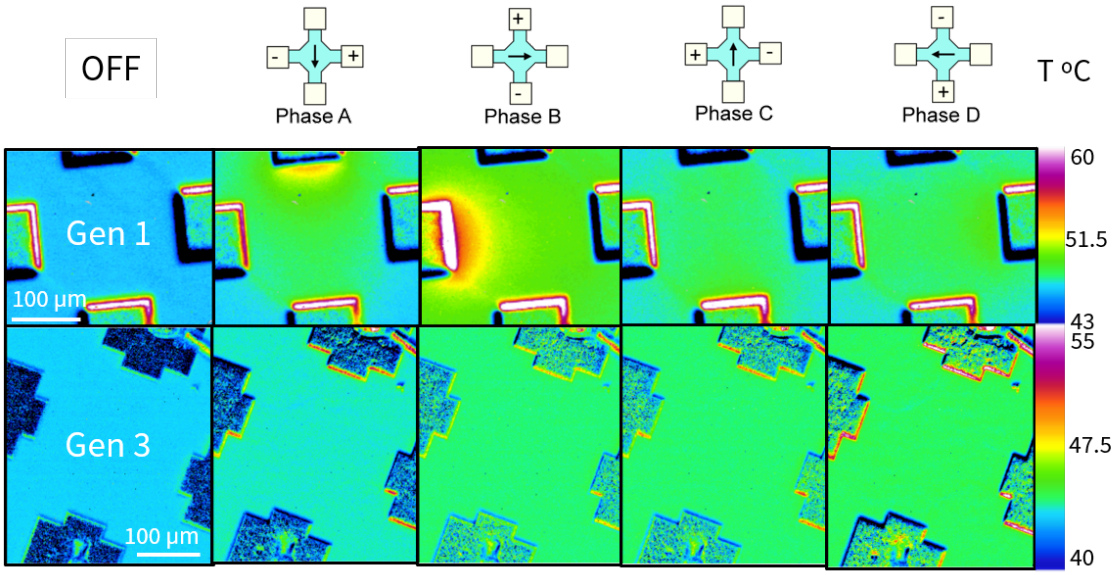


Figure 5.7: Infrared microscope image of GeN 1 device at 9 mA, on and off, showing self heating at the contact.

Other Sources of Offset

Other offset sources have been reported in the literature. First, mechanical stress has been reported in Si Hall-effect plates to cause asymmetric resistances which cannot be canceled in current spinning [38, 158]. Another source is self-magnetic fields. Similar to wired fields, the Hall device can generate its own magnetic field around the sourced current, which could locally fringe the devices. However, this will only occur when there are drastic asymmetries in the device current path with respect to the sense contacts (such as in vertical devices) and the opposing fields cannot cancel out. Another intrinsic offset source is nonlinear contacts. Schottky-like contacts will not have symmetric operation in a poor fab run, and this will create nonlinear offsets which cannot fully cancel. Another proposed offset source is due to localized electric field stress in devices due to sharp corners in geometries. While these effects were not directly studied in this work, they would be valuable contributions in future work.

5.2.3 Best Practices for Low Offset

To summarize the findings for offset measurements, the following practices are recommended in device design and testing:

1. Design Hall plate with bond pads placed far from active device area. This can be done with long contact traces.
2. Design Hall plate with contacts which overlap longer than the transfer length, to avoid current crowding in the contact.
3. Shield device from non-desired fields. Suggestion to use high magnetic permeability materials to accomplish this.
4. Package device with low stress—avoid encapsulations without proper thermal characterization
5. Avoid materials with doping to avoid the dynamic resistance change with voltage. This is best accomplished with 2D materials or 2DEGs.
6. Use package materials which do not contain ferromagnetic materials (Ni, Co, and Fe).
7. Process sensor with low noise measurement equipment (to be discussed in the next section).

5.3 Noise Contributions in GaN 2DEG Hall Devices

In addition to offset, sensor measurements are also limited by the background noise. There are a vast number of noise sources in a measurement system. The block diagram shows the standard current spinning measurement set up (Figure 5.3), and the data sheet specifications for noise of each portion.

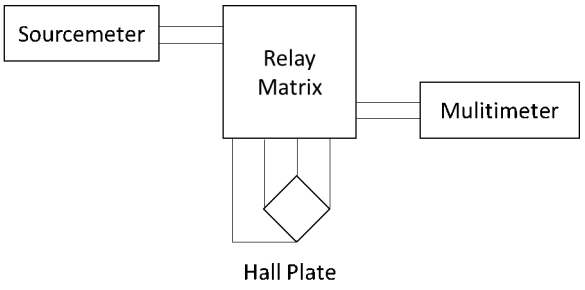


Figure 5.8: Block diagram of current spinning benchtop setup.

Component	Noise levels
Current Source	500 nA (0.1–10 Hz)
Relay Matrix	3 µV emf
Hall Plate	Varied (Resistance and flicker noise)
Multimeter	0.5 to 3 µV

Similarly, this can be seen in the prototyped CubeSat payload (Figure 5.9 and Table 5.1). An example measurement from the CubeSat payload is now shown in Figure 5.10. This was taken

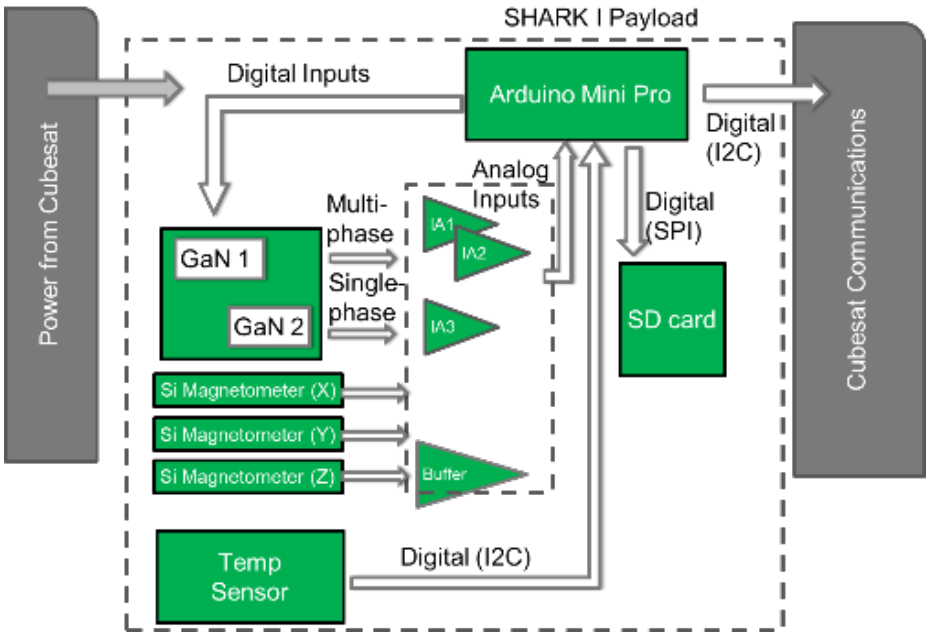


Figure 5.9: Block diagram of cubesat payload from Appendix A.

Table 5.1: Summary of noise sources in demonstrator payload of GeN 1 Hall devices for suborbital CubSat. A

Component	Noise levels
Voltage Source (Arduino Mini Pro)	Unknown
Bias Resistors	Varied (Resistance and flicker noise)
Instrumentation Amplifiers (AIA188, Gain =500)	Input: 10 nV/$\sqrt{\text{Hz}}$, Output: 5 µV/$\sqrt{\text{Hz}}$
Hall Plate	Varied (Resistance and Flicker Noise)
Digitization (Arduino Mini Pro)	10 bits, 5 V range, LSB = 4.8 mV (~0.13 mT)

during a sounding rocket flight in the Mojave dessert in June 2018. The payload is documented in Appendix A. Unfortunately, the readout of the data was too noisy to resolve any behavior from the flight itself.

To improve measurement systems, several factors can be addressed. Low noise circuits are a popular topic in the silicon integrated circuits research [51]. With proper component selection, system noise can be mitigated to levels such that the sensor limits will be the only ones that

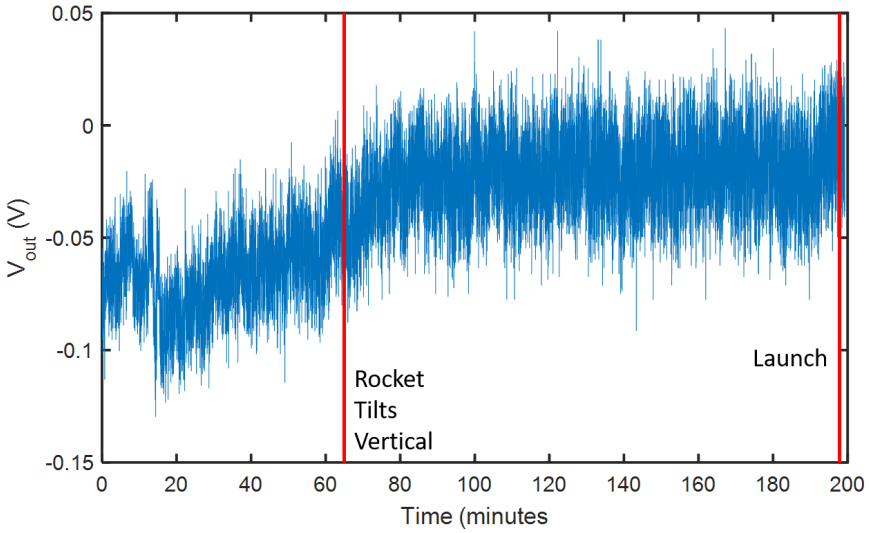


Figure 5.10: Logged data from CubeSat flight on sounding rocket for Gen 1 Hall device. This measurement is incredibly noisy and the signal of earth's field is not resolvable.

remain [181]. The ultimate limitations will derive from the sensors noise characteristics. In this section, we quantify the noise characteristics of these AlGaN/GaN and InAlN/GaN Hall plates.

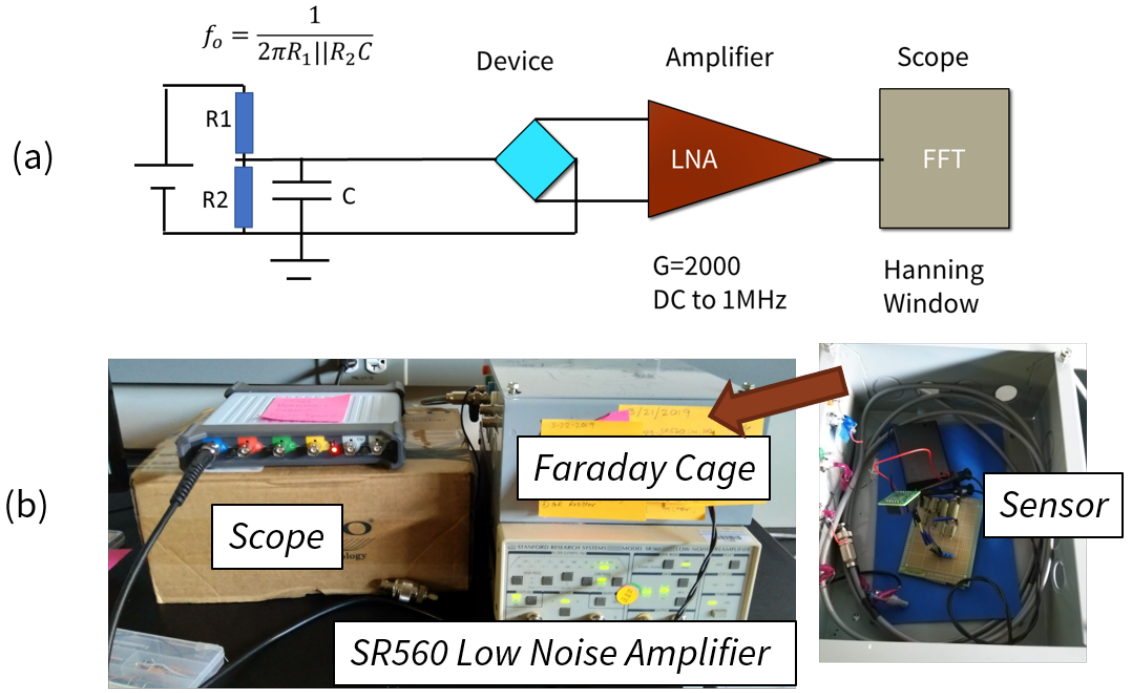


Figure 5.11: (a) Block diagram for noise measurement. (b) Photograph of noise measurement setup.

5.3.1 Methodology

The measurement set up was based off of noise measurement setups documented in the literature. [46, 182, 183] The measurement block diagram and set up is shown in Figure 5.11. The device is biased with a nominal 1.5 V alkaline battery, low-pass filtered with foil resistors and attenuated to vary input voltage. The device and bias circuit are placed in a metal box to shield from stray electromagnetic noise. The sensors output is then measured with a low noise amplifier (Stanford Research SR560). This amplifier is set with an AC filter and low pass filter at 100 kHz and 6dB/octave slope (20 dB/decade). The gain is set as high as possible without railing the amplifier, (G=2000). It should also be noted, the amplifier was updated with critical modifications– which is documented in Appendix D. The amplifier output connects to a computer-programmable oscilloscope (picoscope 5444B), where several time-domain measurements are taken, converted to the frequency domain via a fast Fourier transform (FFT) using a Hanning window, and averaged with several samples. The background noise was measured (Figure 5.12) with the probe cables connected as a short, and this was subtracted from subsequent measurements with the same settings. The sensor noise spectrum (v_{hall}^2) can thus be calculated with Equation 5.1:

$$V_{out}^2 = G^2(v_{hall}^2) + v_{LNA,G=2000}^2 + v_{pico}^2 \tag{5.1}$$

where V_{out}^2 is the output noise spectrum measured, G is the gain of the LNA, $v_{LNA,G=2000}^2$is the output noise of the LNA at the gain setting of 2000, and v_{pico}^2 is the detected noise of the picoscope. The picoscope resolution needs to be selected such that the noise of interest can be detected and smaller range allows this, and 500 mV was selected for this purpose. The gain, G, must be large enough so that the sensor noise is comparable, ideally larger, than the noise of the LNA to be detectable. After several iterations with hardware settings, the following parameters in Table 5.2 were used in these studies.

Once the input referred noise was collected, the $1/f$ noise parameters were calculated. A linear fit was done between 10 and 100 Hz in the log-log scale to calculate from the slope and α_H from the intercept of this fitted line (f = 1 Hz). Some assumptions were made about device carrier concentration and area, summarized in Table 5.3. A diagram of the parameter extraction method can also be found in Chapter 2 with Figure 2.13.

Devices from all three fabrication runs were measured and compared as summarized in 4.1. Due to large number of devices, these are compared in different sub-studies for ease of understanding.

Table 5.2: Hardware settings for measurement. Software for measurements and computation will be described in Appendix D

Bias Circuit	SR560 LNA	Picoscope
1.5 V Battery	AC Coupled Input	AC Coupled Input
R_1 = 50, 100 Ω	100 kHz Low Pass @ 6 dB/oct	16 bit resolution, single channel
R_2 = 100, 50 Ω	G = 2000	T_{meas} = 1 second
C = 300 µF	Low Noise Mode	N = 500–6000 (1000 nominal)
V_{min} = 0.1 V	Battery Powered	Timebase = 65
V_{max} = 1.436 V	Replaced front end FET	Range 500 mV (1 Vpp)

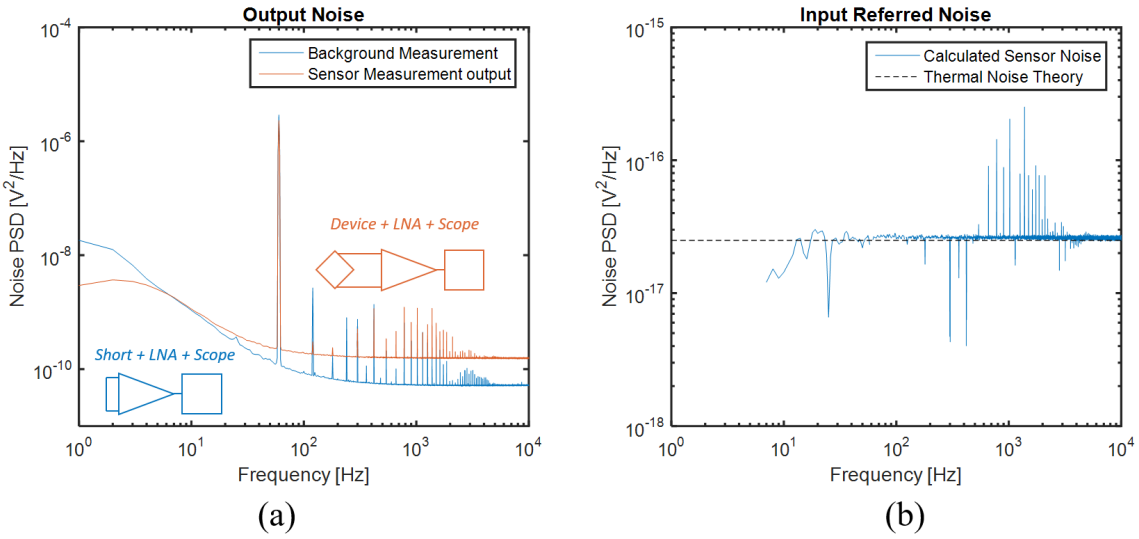
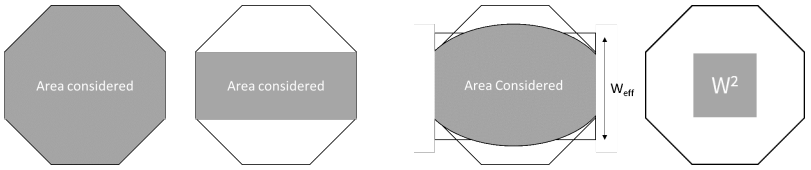


Figure 5.12: (a) Raw output data from noise measurements (b) Remaining signal after background subtraction and scaling for gain to get input referred noise.The spikes are 60 Hz its harmonics due to power line noise.

5.3.2 Noise Characteristics in Generations 1 and 2

It was confirmed the first device fabrication study had issues with contact resistance. Several indications showed this. First, the device resistance varied heavily with an increase in voltage (-5%/V), which resulted in a large residual offset on the order of 2-4 mT. Previous work had shown that

Table 5.3: Hooge parameter calculation assumptions for N. Sheet density values are taken from publications in which the fabrication is documented. Four methods are suggested for calculating area (A) in the octagonal Hall device.

$N = n_s \times A$	n_s (cm^{-2})	Full Area	Width × Length	W_{eff}× Length	W^2
Gen 1 (SNF MOCVD AlGaN)	9×10^{12} [4]				
Gen 2 (Commercial AlGaN)	9×10^{13} [5]				
Gen 3 (InAlN)	2×10^{13} [6]				

a measured Hooge parameter has a volume-dependency with noisy contacts [184]. While it is unclear the role these contacts play, it should be considered when estimating the Hooge parameter. Equation 5.2 is the starting point to analyze for better understanding:

$$S_V^2 = S_{V,Hall}^2 + S_{V,Contact}^2 = \frac{V^2 \alpha_H}{N f^\gamma} + \frac{V_{contact}^2 \alpha_{Hc}}{N_{contact} f^\gamma}. \tag{5.2}$$

Thus, the contacts could contribute more to the noise should the ratio between these terms change.

The noise measurements from octagon shapes in Gen 1 devices confirms that the Hooge parameter of the GaN 2DEG material stack is over estimated with the presence of noisy contacts larger devices calculate to have larger Hooge parameter (fig 5.17). This means there is probably a component in the noise which does not proportionately scale with area. This theory is better explained in [184]. Regardless, the improvements in noise characteristics can be seen in a comparison between noise data from a Gen 1 and Gen 2 device, found in Figure 5.13.

5.3.3 Generation 3—Geometry Variations and Noise

The next fabrication process (Gen 3) had more area available for Hall devices, so we designed structures with several geometries. A few differences still exist compared to Gen 1. For example, the contact overlap regions is still extended in Gen 3, even for the octagonal structures. The geometries and sizes included in this study are listed in table 4.1, similar to those from Alpert et. al 2019 [6]. The geometries are varied from wider contacts to very narrow, point-like contacts. These were previously studied to understand the influence of geometry on current and voltage-scaled sensitivity, but they were also designed with signal to noise ratio optimized (for thermal noise). However, 1/f

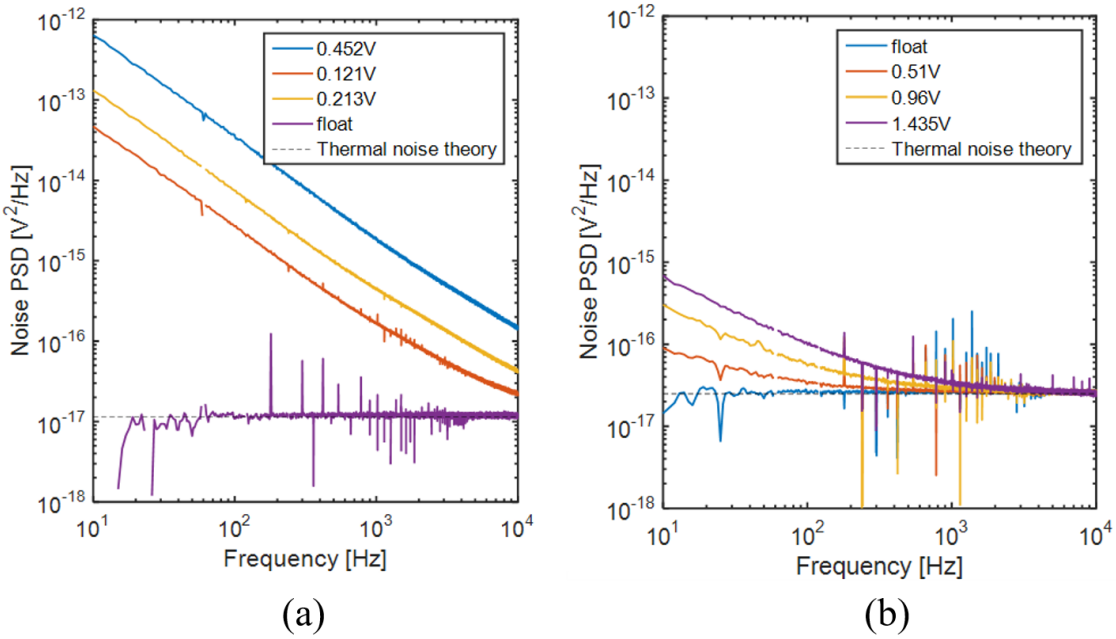


Figure 5.13: (a) Gen 1 noise characteristics, showing large corner frequencies. (b) Gen 2 noise characteristics, showing much smaller corner frequencies.

noise characteristics should also be considered to realize ideal structures for given applications. (To account for spinning frequency system parameters).

The 1/f parameters for the varied geometry study are thus summarized in figure 5.14. We can see right away, the widest contacts show the largest Hooge parameter and the larger corner frequencies.

There are several possibilities that influence this trend:

1. *Geometry vs. N*: We saw in Table 5.3, that there are several ways to approximate the area of these devices and each method modifies the output Hooge parameter calculated. However, when this is considered, we would see that the overlying trends stay the same. Ideally, the Hooge parameter for a given material should be constant, and thus the proper normalization terms need to be identified for these different device geometries. Also, we should consider what is the best way to calculate the total number of carriers (N). It can be approximated that the carriers that influence noise must be in the captured section of the Hall device. Carriers at the contacts orthogonal to sense contacts will not be as much of influence of carriers at the equator, where the device will pick up the potential and activated carriers. We also should consider the differences between these geometries, which is related to $(L/W)_{eff}$. Figure 5.15

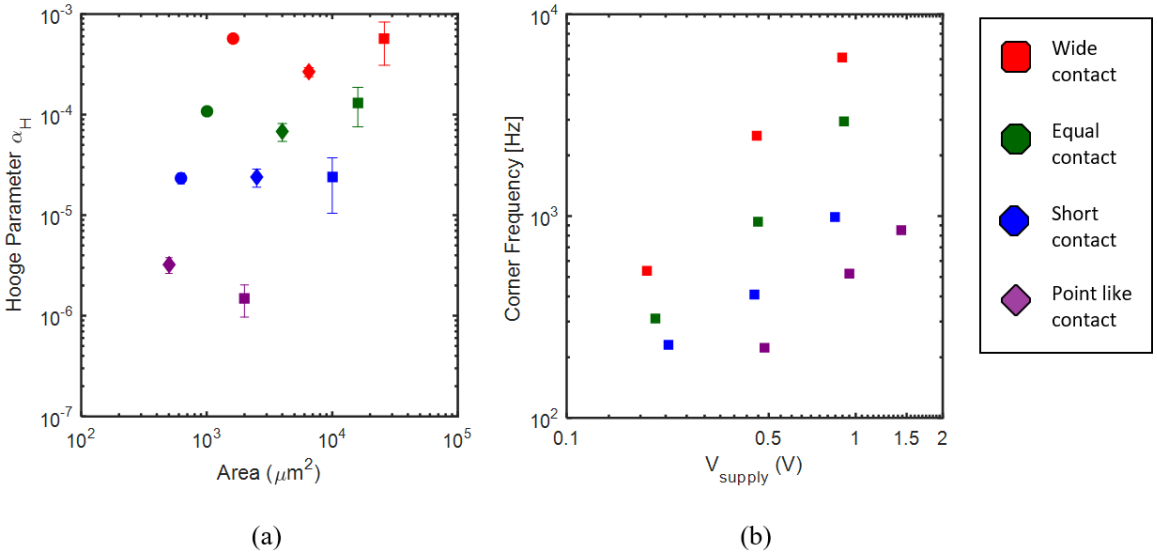


Figure 5.14: 1/f noise parameters with respect to geometries for Gen 3 samples. (a) Estimated Hooge parameter using L*W with respect to Area (L*W). (b) Extracted corner frequencies with respect to bias supply voltage for the largest devices in each geometry.

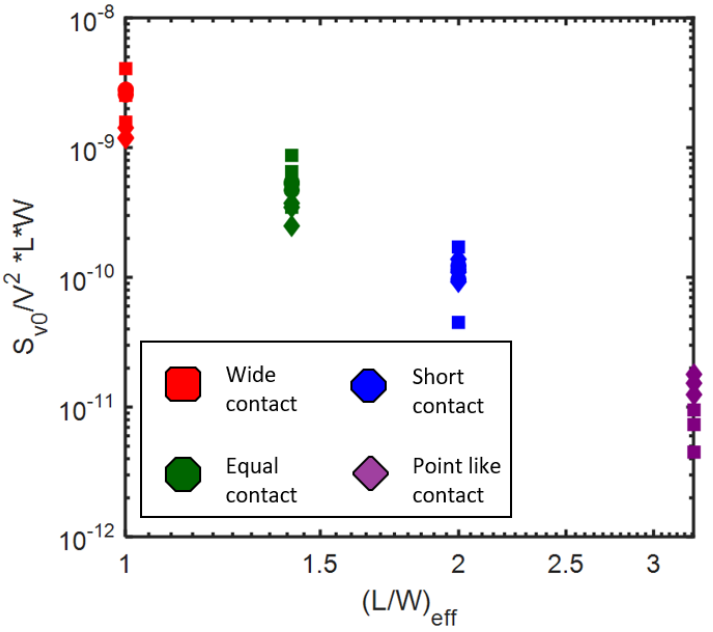


Figure 5.15: A simplified look at the effect of the geometry on the noise power spectral density, normalized by input power and multiplied by L*W.

shows the Noise power spectral density normalized with input Voltage and W*L, vs $(L/W)_{eff}$, and the trend isolates the influence of $(L/W)_{eff}$ on the noise parameter.

2. *Power or Current Density*: Another possible explanation is to understand the influence of power density. We see the large contact device utilized more area for conduction than the narrower contact devices (regardless of area calculation method). This means the power density is higher in these devices (more current flow for a given voltage). When we compare power density to corner frequency, we see Figure 5.16a. It is possible that the higher power density relates to higher vibrational energy of the available electrons, could cause larger fluctuations in a similar device area, and thus lead to calculation of a larger Hooge parameter in the same material.

3. *Electric Field*: Similar to power density, the electric field varies with different devices sizes, and could reveal some differences with geometry and corner frequency. We see in Figure 5.16b, the corner frequencies do fit linearly with respect to electric field. However, we still see a shift in those curves with geometry.

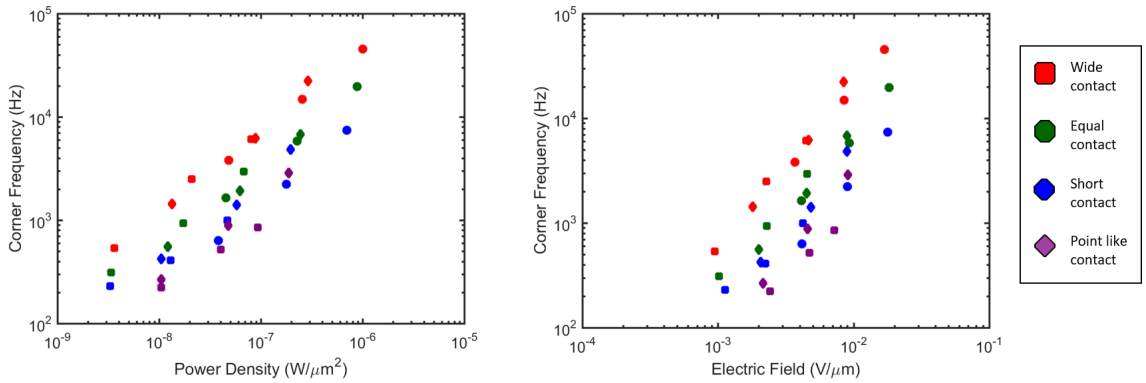


Figure 5.16: Corner Frequencies of Gen 3 devices with respect to (a) power density and (b) electric field.

5.3.4 Summary of noise studies

While it remains unclear what exactly about the device geometry influences the noise parameters, it is quite clear that these devices have competitive noise figures compared to state-of-the-art silicon and InAs devices. Figure 5.17 shows a final comparison between all generations of devices and

the control samples. While the Hooge parameter is not completely approximated for the unknown volumes of commercial devices, we can still conclude via corner frequency measurements that the GaN 2DEG Hall plates from Gen 2 and Gen 3 are competitive with state-of-the-art semiconductor Hall plates motivating further advancement in GaN Hall-effect sensor products.

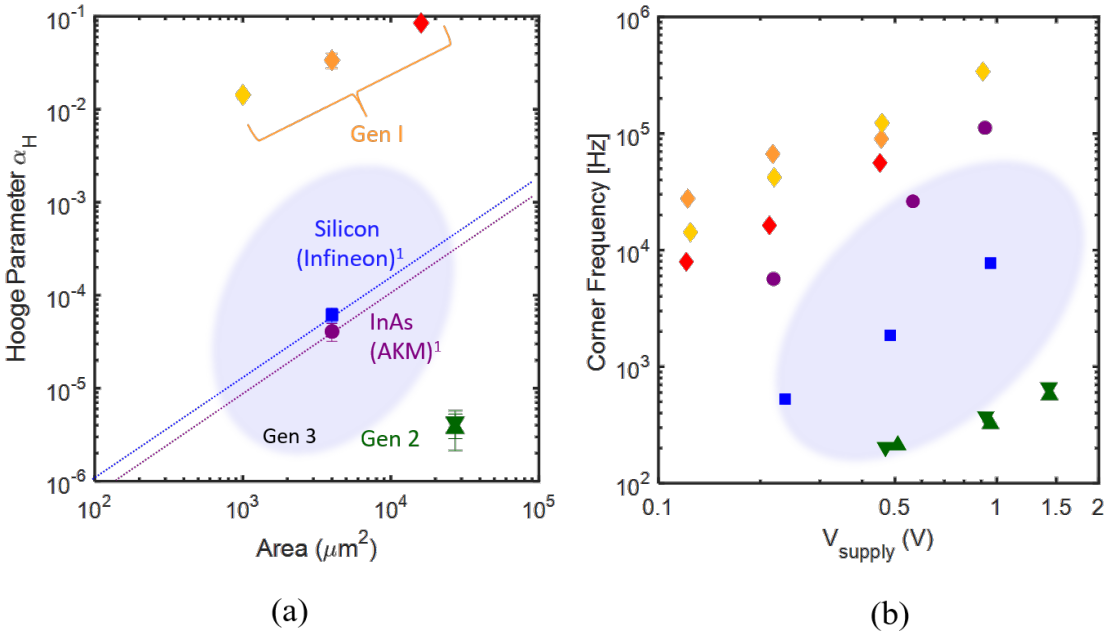


Figure 5.17: Overall summary of the improved noise characteristics of GaN 2DEG Hall plates compared to Silicon and InAs devices. The Gen 3 devices are represented as a light purple cloud. The dashed lines refer to devices with unknown area, so an estimate was made. (a) Estimated Hooge paramter vs. Area (W*L). (b) Corner frequencies vs. supply voltages.

Chapter 6

Conclusions and Future Work

6.1 Key Contributions

The following summarizes the technical contributions made through the research as described in this thesis.

1. Created high aspect ratio trenches in bulk 4H-SiC (record 18.5:1) and multi-layered mask process for 2.5-D features to support SiC MEMS for Harsh Environments and cooling highly power dense electronics.
2. Identified key factors that cause offset in GaN 2DEG Hall Plates (%R/V, Seebeck, noise)
3. Measured record-low offset in GaN 2DEG Hall devices (0.5pm0.7 μT)
4. Investigated and examined noise in AlGaN/GaN Hall-effect plates for the first time.

6.2 Thesis Summary

This thesis covered the development of a thermally stable, low offset, and low noise two dimensional electron gas Hall-effect plate, as well as improvements in micro-fabrication of silicon carbide and silicon substrates to support the advancement of wide bandgap devices. These key developments support several new applications moving forward for monolithic integrated sensor and power electronic circuits.

In Chapter 1, we saw there are several magnetic field sensing applications, which various types of magnetic sensing paradigms have been developed to address those applications. We saw in particular

Hall-effect plates have several advantages due to their ease of integration with CMOS circuitry, and low power, low footprint operation, with decent sensitivity and reliability. We then saw that there are temperature limitations with traditional Hall-effect devices made with silicon and GaAs films. In addition, we saw that GaN and wide bandgap materials show promise in novel extreme environment applications outside of their traditional use for LED lighting, RF, and power. In Chapter 2, we reviewed the terminology and concepts which Hall-effect devices operate, how they are micro-fabricated, and reviewed a critical technology for MEMS and micro-cooling GaN and SiC devices.

We saw in Chapter 3 several in-depth studies in inductive plasma etching of bulk silicon carbide. First, we investigated the selectivity of different mask candidates with a goal for creation of multi-layered structures, as a proof of concept for future MEMS concepts in SiC. Then, we investigated the creation of high aspect ratio arrays with a particular interest in micro-cooling GaN power transistors. We saw hotspot temperatures were effected both by the channel width as well as the fin thickness - and both need to be considered when designing micro-channels and fabrication processes. We also saw interesting aspect ratio dependant etching features: "W"-shaped microtrenches and "V"-shaped pointed trenches. This was further studied to understand how the microtrenching profiles of high aspect ratio features evolve throughout the process. In addition, plasma conditions were varied and their influence on high aspect ratio etching and features also considered. This work culminated in a world-record aspect ratio in inductive-coupled plasma etched 4H-silicon carbide at the time of publication in 2017. Since then, multiple studies have been published which have pushed the aspect ratio, depth, and channel tapering to more ideal applications for both micro-fluidic cooling and MEMS. [185, 186]

We then switched gears and investigated the operation of Hall-effect plates made with AlGaN/GaN on silicon in Chapter 4. The first generation devices showed higher voltage-scaled sensitivity than silicon hall plates, but undesired large residual offsets. We identified this was due to self-heating in the devices and a resistance asymmetry issue later shown in Chapter 5. In addition, with a few changes in the Hall sensor design, we were able to show a silicon-competitive device with offsets on the order of 3-10 µT. Later in Chapter 5, it was realized this offset was actually even lower, at 0.5 µT, which was found with several test setup and packaging improvements. Finally, we investigated the noise contributions from both thermal and flicker noise in these Hall devices, and saw they had better performance to typical silicon and InAs devices in both merits of corner frequency and noise floor. We finished with an intensive study on the effect of geometry on flicker

noise characteristics- and devices with narrower contacts showed improved flicker noise behavior over the wider contact shapes. Thus, typical silicon devices are outperformed by AlGaN/GaN Hall-effect plates in terms of temperature operation, offset, and noise.

Table 6.1: AlGaN/GaN Hall Plates Bench-marked with Silicon Devices.

Material	Silicon	AlGaN/GaN [151]
Current-Scaled Sensitivity (V/A/T)	300	90
Voltage-Scaled Sensitivity (mV/V/T)	60	57
Temp Coeff Drift (ppm/K)	300	100
Max Temperature (℃)	150	600
Resistance Drift (%/V)	5	0.5
Offset (μT)	3	0.5
Corner Frequency (Hz) at 0.25V	600	200
Noise Floor (nV/$\sqrt{Hz}$)	9.7	4.99

6.3 Recommended Future Directions of Research

There are several directions this line of work can take, because of the potential impact for a diverse set of applications. Here are a few key paths ranging from fundamental studies to applied system studies.

1. *Fundamental 2DEG studies* Since the Hall effect primarily uses Van der Pauw structures, it is a great platform to study the effect of stimuli on mobility and sheet density of thin films. This could be done to study the effect of strain on the 2DEG, and finally decouple the 2DEG's conductance change due to a local change in mobility (from straining the lattice) or sheet density (due to the change in piezoelectric strain). In addition, this could be studied in both AlGaN/GaN and InAlN/GaN, since the top film in each has a different spontaneous and piezoelectric polarization ratio, and so this effect should be different in both films. A pressure sensor with a Hall plate would be a good starting point for this study [187]. In addition, optical effects could be studied to understand the effect on the GaN 2DEG or material. An ultraviolet light coupled with a Hall set up could be used to characterize the efficiency of the UV absorption, through a direct measurement of the sheet carriers in the material [5]. Finally,

work has also been done with gated Hall devices, which can dynamically change the 2DEG concentration, and show various scattering mechanism which are present in a depleted 2DEG. This work was published elsewhere in the study of phonon drag on AlGaN/GaN 2DEGs [188] and was also shown in Chapter 3 (Figure 2.7). Many more avenues of study can be considered, using modified Hall measurements as the platform of study.

2. *Noise Studies in modern GaN devices* There are no measurements of direct noise of AlGaN/GaN Hall-effect plates in the literature, and many things could still be studied in these devices. For example, the influence of traps and defects on the 1/f noise curve could be studied between different material sources, as well as the influence of temperature on these measurement outputs. This would inform future system level implementations and circuit specifications. In addition, other GaN–based devices should also be considered to understand the noise parameters in those structures. Transistors and diodes seem like a good place to start, which will influence the design of low-voltage digital and analog circuits for sensor integration. Amplifiers, in particular, need to be designed with low-noise parameters to enable the best sensor node. Regarding device geometry, it would be advised to analyze the geometry effects in a finite element tool to further understand carrier fluctuation pockets, and possibly integrate over the nonuniform conducting surfaces or identify peak electric fields and their correlation with 1/f noise. High electron concentrations likely vary 1/f noise locally in the material.

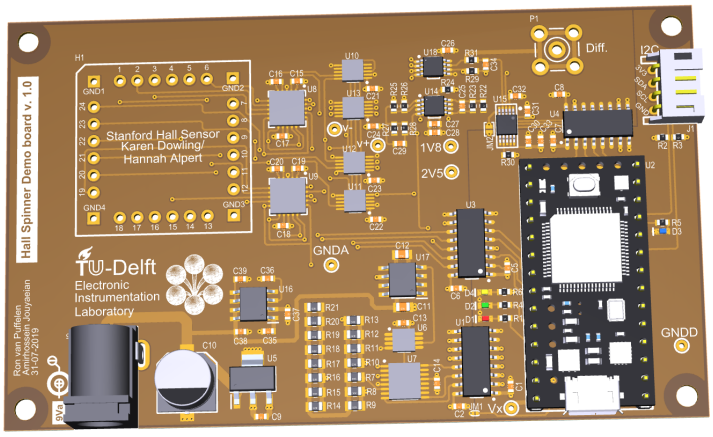


Figure 6.1: First draft of current spinning in collaboration with TU DELFT.

3. *Digitization* Microdevices are great due to their small size and low power, but they rely on analog-to-digital signal processing to be useful in embedded systems and instrumentation.

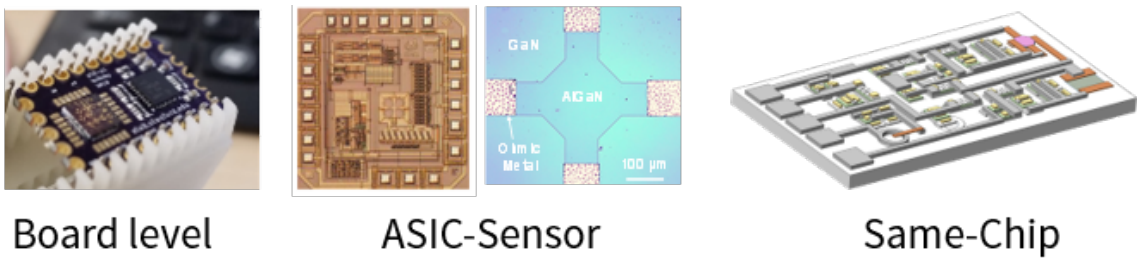


Figure 6.2: Progression of digitizing Hall sensors from board level, to a two chip asic-sensor solution, then longer term: monolithic integration.

Thus, it is important to effectively convert the Hall voltage to a digital stream. This would include the development of a circuit which can handle low noise amplification, current spinning, and digitization in real time. Several strategies are currently in progress, including direct amplification with a programmable analog-digital converter, as well as a low noise spinning board in collaboration with Prof. Kofi Makinwa at TU Delft (Figure 6.1). Eventually, smaller and low-parasitics solutions can be implemented with a high-quality silicon ASIC similar to previous work [158], and eventually done with monolithic integration all on one chip. This progression is shown in Figure 6.2.

4. *Sensor Deployment* Once these devices have a reasonable readout scheme, they can be used for magnetic measurements in various systems. Power electronics is a good starting point. We currently have ongoing efforts in the NSF-funded research center for Power Optimization of Electro-thermal Systems (POETS) to use these sensors to study both currents in a traction inverter, and position sensing in a air-core motor which operates at 1 MW. Demonstration of successful operation and deployment in these environments will give the momentum needed to push this technology further.

5. *Extreme Environments* Once deployment is successful in near-room temperature systems, these sensors should be leveraged for the applications with most promise: extreme environments. Preliminary was done with an Arduino to current spin a Gen 1 Hall device and interface the data telemetry with a CubeSat developed by BOREAL Space. This sounding rocket was a launch into system level experiments in the lab. Last year, Stanford collaborators worked with NASA KickSAT (Prof. Manchester and Max Holliday) to deploy some Gen 3 Hall devices in orbit. Current work is underway to develop a mission concept as part of MagSense to profile Earth's magnetic field in Low Earth Orbit at a resolution far better than before. Future work

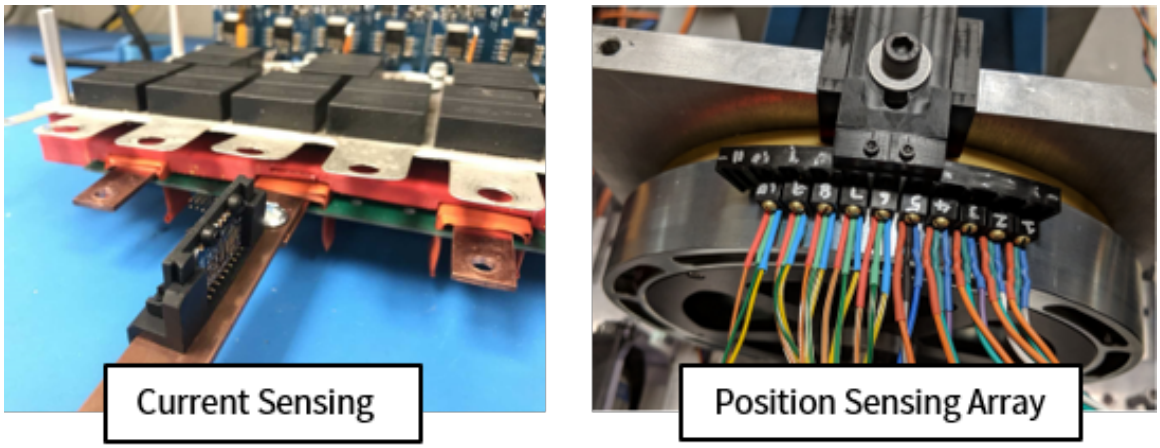


Figure 6.3: Power electronics environments for magnetometer applications. Image credits: Prof. Juan Balda and Prof. Yue Zhao at Univ. of Arkansas, Prof. Haran at UIUC.

can consider the recent noise characterization to optimize these devices for the best performance to detect earth-like fields in challenging temperature ranges and radiative environments.

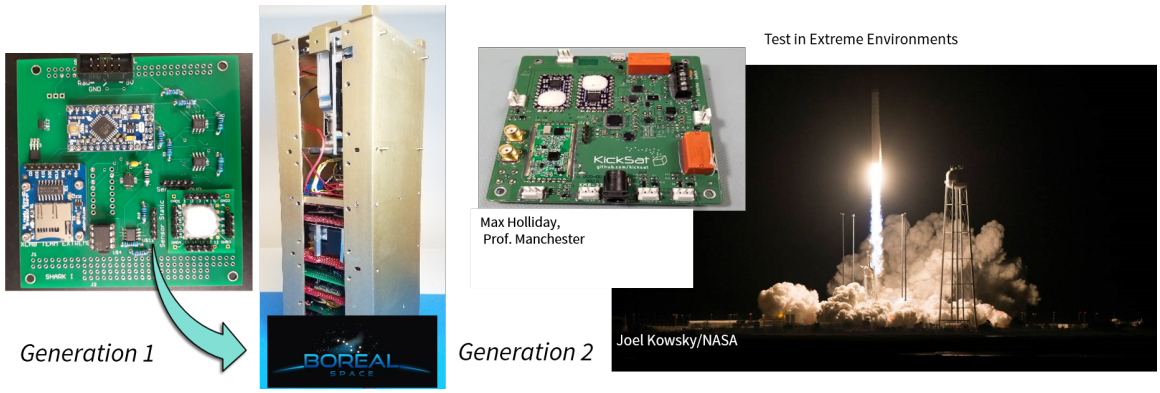


Figure 6.4: Efforts in CubeSats with magnetic field sensors in extreme environments micro-systems laboratory. Generation 1 devices were deployed on a CubeSat in collaboration with Boreal Space. Generation 2 devices deployed on a Cubesat in collaboration with NASA KickSAT.

6.4 Final Remarks

The future is bright for wide bandgap semiconductors. The last 20 years has brought to fruition the use of GaN and SiC in power electronics, radio frequency communication, and opto-electronics. These materials typically are leveraged at their extremes in power density, speed, and blocking voltage, yet still have much to offer in extreme environment electronics (i.e. temperature, radiation,

and chemical corrosive environments). Through the use of microfabrication advancements in etching of SiC presented in this dissertation, power electronics can be pushed to higher power densities with localized microcooling, and novel MEMS devices for high temperature environments can be fabricated. This dissertation concluded with a highlight of GaN's potential as a magnetometer for high temperature, low offset, and low noise which out perform state-of-the-art Si devices. GaN and SiC have paved a path for novel wide bandgap research which will change sensing, power, and communication in coming decades.

Appendix A

Rapid Development of Hall Sensor Payload for Suborbital Flight

Some work with Gen 1 Hall plates to integrate them with a cubesat payload was perfomed in the summer of 2017. This abstract was presented as a poster at the Interplanetary probe workshop (IPPW) at CU Boulder in June 2018. Later that same week, the payload actually flew in the Mojab dessert and survived the flight. The board was still operating when retrieved from the sounding rocket.

GALLIUM NITRIDE MAGNETIC FIELD SENSOR PAYLOAD FOR SUBORBITAL FLIGHT.

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Introduction: Miniaturized electronics enable the design and engineering of compact, low-cost instrumentation payloads used in space experiments. However, most silicon-based electronics are not suitable for long term space operation due to various mechanisms such as threshold voltage shifts, single event effects, and freeze out. As an alternative to silicon, wide bandgap semiconductor devices have been developed for operation under extreme environments, such as cryogenic temperatures and high levels of radiation [1, 2]. These emerging electronics often require rigourous advancement in Technology Readiness Level (TRL) for deployment on commercial satellites and other space missions. Novel device technologies, therefore, take years of reliability testing beyond academic research before they fly. CubeSats enable rapid and affordable flight testing to validate these new technologies.

Methods: Here, we present the development and implementation of a gallium nitride (GaN) based magnetic field instrumentation payload for a suborbital launch. The key payload interface choices were dictated by a rapid (< 2 months) delivery timeline. The board is affectionately named SHARK-I in honor of the team that contributed to it.

The sensor: GaN devices were manufactured with a previously reported microfabrication process [3]. To summarize, AlGaN/GaN was grown by metal organic chemical vapor deposition (MOCVD) onto a (111) silicon wafer. A stack of titanium, aluminum, platinum, and gold was evaporated and annealed to create Ohmic contacts. Finally, the devices were passivated with alumina through thermal atomic layer deposition (ALD). The sensor is shown in Figure 1. The magnetic sensors were packaged with wirebonding on a FR4 printed circuit board (PCB) and encapsualted with low-outgas resin (Masterbond® EP37-3FLFAO). The sensor was characterized in a home-built Helmholtz coil setup (Figure 2) and current spinning was leveraged to reduce the offset [4]. Figure 3 shows the measured Hall voltage with respect to various tested fields and bias currents from -5 mT to 5 mT. This sensor was then integrated into the payload SHARK-I for Boreal Space's Wayfinder II CubeSat.

Payload Sensor Amplification: The payload's biasing sheme for the device was set by the Arduino's digital pins for current spinning [4]. The sensor operates via the Hall-effect, so its differential output was amplified with an instrumentation amplifier (INA188) using a gain of 500. SHARK-I stores the hall votaltage multiplied by the amplifier gain (~500), shown on the secondary axis of Figure 3. This calibration will be important for analyzing recorded data after the flight.

Data Handling/ Payload Control: The analog signal was then digitized to 10 bits (Arduino mini pro), and was sampled at a rate of 5Hz. Two custom GaN sensors were included for redundancy. Reference silicon Hall sensors (Infineon Technologies) were also equipped on the payload. The Arduino interfaced with an Intel Edison on-board computer (OBC) via standard I^2C data communication protocol for telemetry data acquisition, and Serial Perpheral Interface (SPI) for on-board data storage in a micro SD card. The final payload's block diagram is shown in Figure 4, and Figure 5(a) shows the final payload design before integration into a 3U Cubesat (Wayfinder II from Boreal Space-Figure 5(c)). To examine the payload's signal conditioning with the sensor, a longer test duration was completed with the SHARK-I board using the magnetic test set up in Figure 2, with the data was recorded in the SD card on board. Various fields were applied, and the recorded Hall voltage (with current spinning) over time is displayed in Figure 6. This flat-sat test shows promise regarding future operation on flight – sensors are operating and data is transmitting as expected.

Future Work: Wayfinder II is scheduled to launch later this year via an Interorbital Systems launch vehicle. SHARK-I will provide important insights(e.g. launch load survival, signal integrity) into future CubeSat oribital missions with GaN-based sensing technology. Challenges discovered (e.g., signal conditioning, magnetic interference, noise reduction and radiation-hard electronics) will be addressed in future flights. Ultimately, this prototyped instrumentation payload paves the way for low TRL microdevices to be readily tested in space and launch conditions, bringing future technologies to space exploration at a rapid pace through the use of CubeSats.

References:

[1] Son, K., et al. (2010) *Nanoscience and Nanotechnology Letters 2.2*, 89-95; [2] Smorchkova, I. P., et al. (1999) *Journal of Applied Physics, 86.8*, 4520-4526; [3] Yalamarthy A.S. et al. *Advanced Materials* (2018); [4] Dowling, K.M. et al. *Hilton Head Workshop*, Accepted (2018)

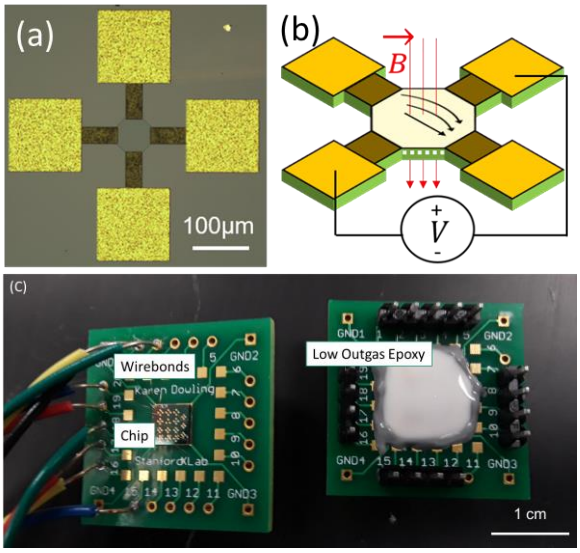


Figure 1: (a) Optical image of GaN-based Hall Sensor. (b) Sensor operation – current sourced and Hall voltage measured. (c) GaN sensor chip packaging, first wiredbonded on a PCB, then encapsulated with low-outgas epoxy.

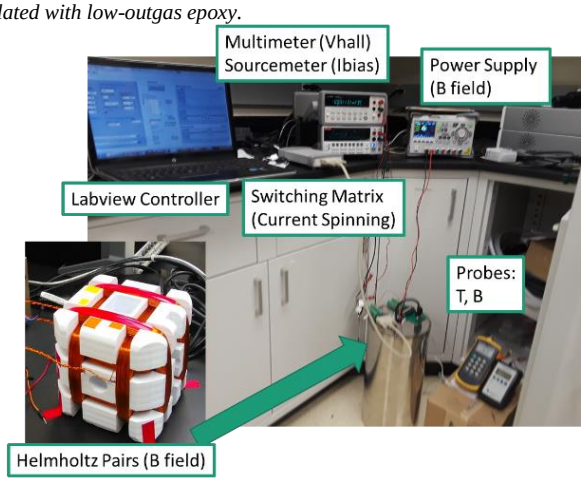


Figure 2: Experimental setup for characterizing the response of the magnetic field sensor.

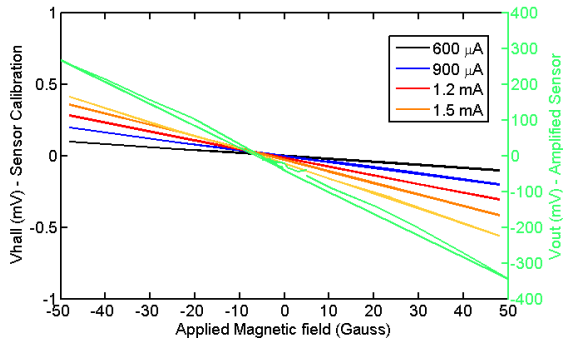


*Figure 3: Sensor voltage output from GaN-based sensor at various magnetic field value and bias currents. Secondary axis shows output voltage from amplified GaN magnetic field sensor (~Vhall *500).*

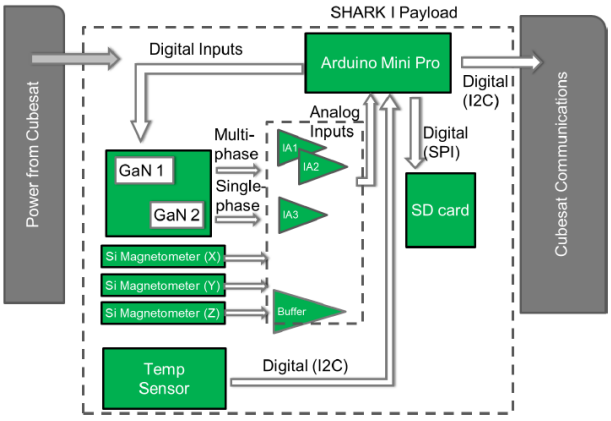


Figure 4: Schematic image detailing the block diagram of magnetic field sensolr payload.

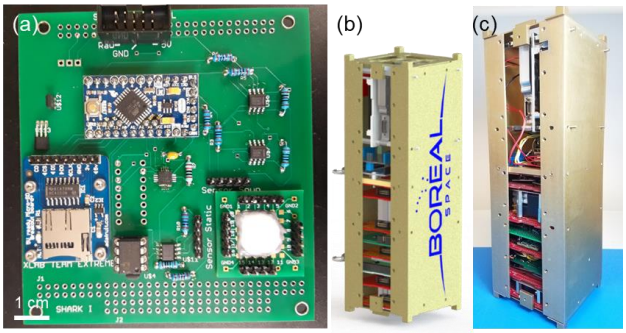


Figure 5: (a) Image of the SHARK-I payload that was implemented on Boreal Space's Wayfinder II.(b) CAD rendering of Wayfinder-II by Boreal Space (Image by Richard Casas) (c) Finaly assembly of 3U CubeSat Wayfinder-II with SHARK-I included.

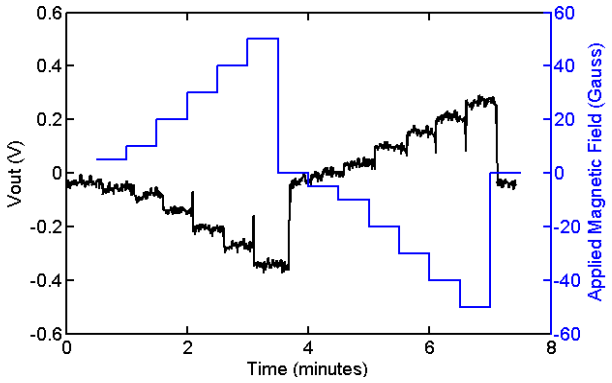


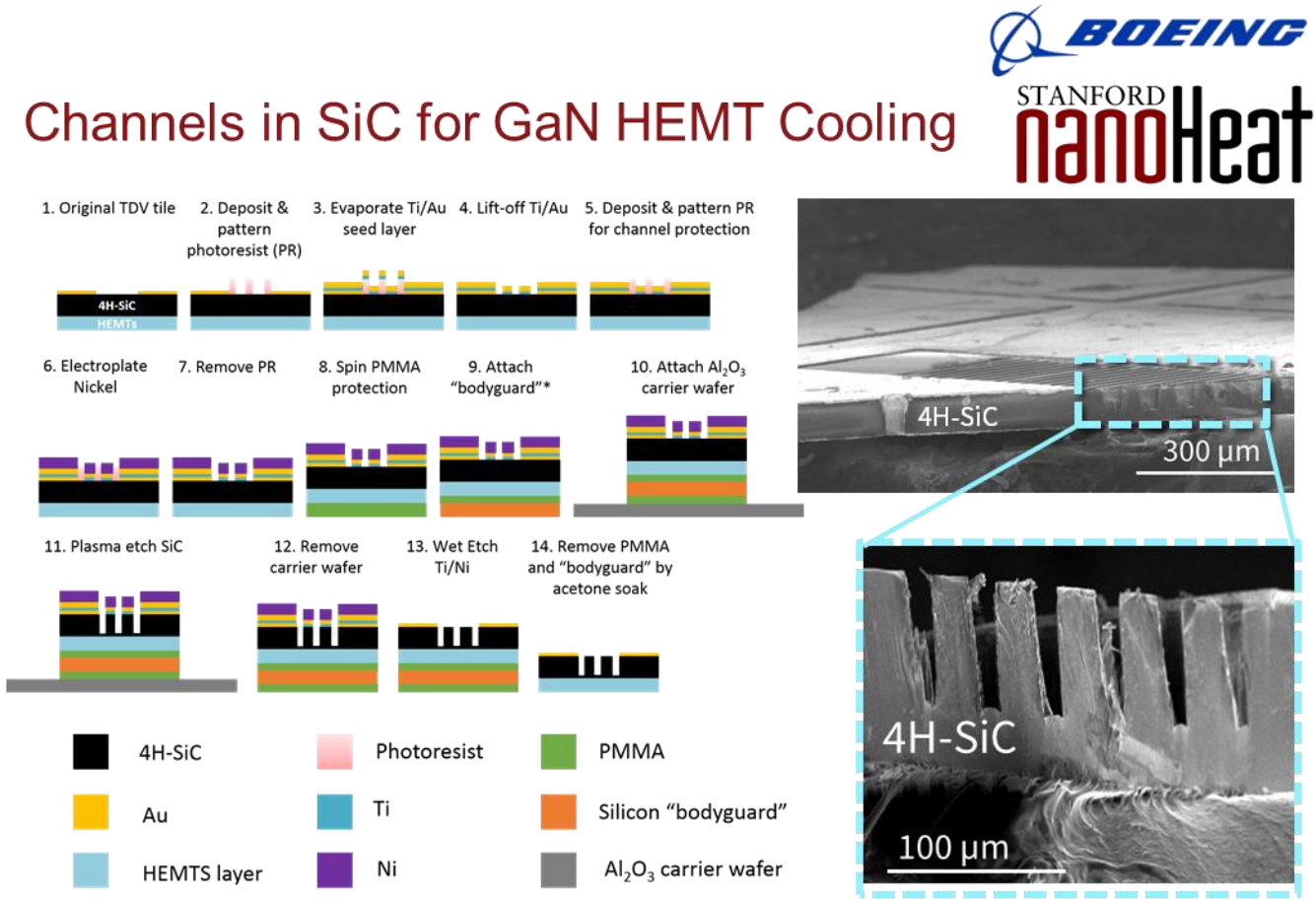
Figure 6: Data logged in SD card vs. time for GaN sensor while in magnetic field testing chamber.

Appendix B

Silicon Carbide Etch Run Sheet

The SiC etching work was sponsored by Darpa and Boeing in the ICECool program. During this work, a process was developed to directly integrate SiC channels on the back of GaN chips.

Process for backside SiC Channel etching on GaN HEMTS.



	Description	**Tool Name**	**Notes/Comments**
1	Dehydration for 20 minutes	110 C oven	Aluminum foil holder
2	HMDS deposition on Back	Yes oven	Back = side to be etched Front = TDV devices side
3	Spin Lift-off-Layer (LOL) at 3000 rpm for 60 seconds on Back	Headway	Protect Front with blue tape
4	Bake LOL at 170 C for 5 minutes	Hotplate	
5	Spin Shipley (SPR) 3612 at 5000 rpm for 60 seconds on Back	Headway	Protect Front with blue tape
6	Bake 3612 at 90 C for 1 minute	Hotplate	
7	Tape Aligner Chuck for pieces	Karlsuss	
8	Clean Mask with acetone/methanol/IPA and mask cleaner	Wetbench litho solvent	Spray Acetone/Methanol/IPA, air dry, spin dry and

		& mask spinner	clean with mask cleaner and spin dry **Repeat for every TDV exposure**
9	Attach TDV tile to taped chuck and align	Karlsuss	
10	Expose for 3.9 seconds	Karlsuss	
11	Post Exposure Bake for 60 seconds at 115 C	Hotplate	
12	Develop for 60 seconds with MF-26A	Wet bench misc.	Characterized for TDV features
13	Hard Bake for 90 seconds at 115 C	Hotplate	
14	Descum for 2 mins 50 W O_2 plasma	Drytek	
15	Tape to Si holder with kapton tape		Limit tape at corners
16	Evaporate 5 nm Ti, 50 nm Au	KJL in SNC	Faster than SNF tool
17	Remove tape and TDV tiles from Si holder		
18	Overnight soak in RemoverPG	Wet bench solvent	1165 can also be used, multiple days is better
19	Rinse w/ Acetone/Methanol/IPA until liftoff complete	Wet bench solvent	inspect with optical microscope, repeat as needed
20	Dehydration for 20 minutes	110 C oven	
21	HMDS deposition	Yes oven	
22	Spin SPR 3612 at 5000 rpm for 1 minute, bake at 90 C for 1 min	Headway Hotplate	Protect front with blue tape
23	Tape Aligner Chuck & align TDV	Karlsuss	Same mask as before
24	Expose for 1.2 seconds	Karlsuss	
25	Post exposure bake at 115 C for 1 min	Hotplate	
26	Develop with MF-26A for 1 min	wbmisc	
27	Hard Bake for 90 seconds at 115 C	Hotplate	
28	Transfer samples to electroplating lab		
29	Kapton tape on front side of TDV		
30	Set up electroplating bath and electrodes		Red – Ni source, Green – TDV sample, white – reference electrode
31	Electroplate for 15 minutes with bias = -1V	Nanoheat lab potentiostat	
32	Rinse in water		
33	Soak in acetone for 20 minutes	XLab wetbench	
34	Remove kapton tape		
35	Rinse in IPA, dry with air hose	XLab wetbench	

36	Prepare Si “bodyguard” - Cleave Si - Rinse Si in IPA, dry with air gun		Si may be changed to sapphire
37	Spin PMMA on Front	Headway	Special tape system to not damage patterned Ni on Back
38	Spin PMMA on “bodyguard”	Headway	
39	Bond TDV to “bodyguard” using 170 C and weighted pressure for 1 min	Hot plate	5 min on plate before and after
40	Prep sapphire carrier wafer by depositing 25 nm Chrome on back	Innotec	Many can be prepped at once
41	Bond TDV/ “bodyguard” to sapphire wafer using 170 C and weighted pressure	Hot plate	5 min on plate before and after
42	Clean PT-MTL using Cl-Clean	PT-MTL	
43	Season PT-MTL with SiC-KD recipe	PT-MTL	
44	Etch TDV’s using sapphire wafer for 3.5-4 hours	PT-MTL	Plasma will shut off after 8-12 mins, let chamber cool and repeat
45	Remove from PT-MTL	PT-MTL	
46	Tap TDV+ “bodyguard” off sapphire wafer		
47	Wet etch Nickel using Ni Etchant TFB for 45 mins, rinse with water	Wbflexcorr	
48	Wet etch gold using gold etchant (KI based) for 30 seconds, rinse with water	Wbflexcorr	
49	Wet etch titanium using Peroxide and 49% HF	Wbflexcorr	This step is sometimes ignored
50	Overnight soak in acetone to separate TDV from “bodyguard”	Wbsolvent	
51	Rinse in Acetone/Methanol/IPA and air dry		
52	Place TDV carefully in gel packs & Vacuum seal	Vacuum sealer	
53	Ship to RFHIC		

Appendix C

GaN Pyramidal Run Sheet - Kleopatra

Several attempts were made to create pyramidal structures similar to that of Dr. So's work in 2016 [138], to create a new platform for sensing. A disclosure was filed with the Stanford Office of Technology Licensing on a particular concept, but the fabrication was challenging to attempt. This section will cover the most recent fabrication run of these devices, and some images of the finished structures. A key challenge, which needs to be be overcome or mitigated, is that the GaN growth on a sloped 111 Silicon surface is not uniform in our MOCVD reactor at Stanford. Thus, the 2DEG does not form in the bottom of the device. It is recommended to try this process with a heavily doped GaN layer to prove the concept. Figure C.1 shows some results from this fabrication run.

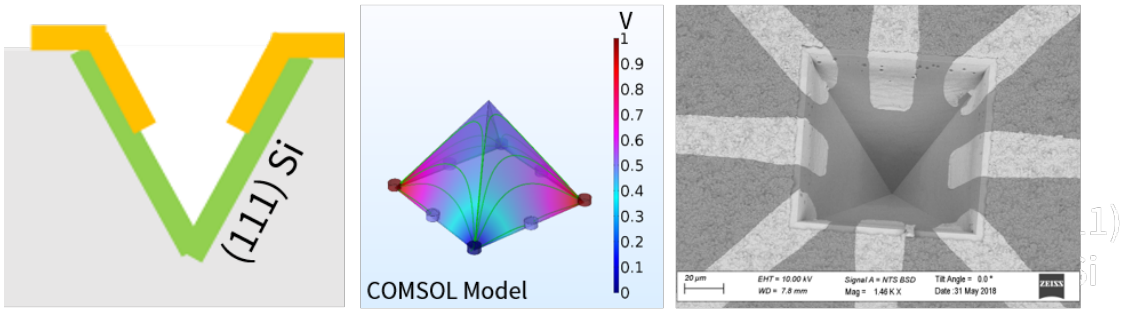


Figure C.1: (left) drawing of GaN on Silicon in V groove concept (middle) COMSOL simulation of 3D Hall device (right) SEM image of GaN on Silicon V groove from fabrication

Master Run Sheet

Date	Step	Tool	Wafers	Time	Temp	Notes
05/03/2018	0: Sample Prep	New Diamond Scribe	25 x L Prime (10-20 Ohm-cm, p type)	10 mins		
05/03/2018	0: Sample Prep	wbclean_res_piranha + SRD	K1-15, T1-10	20 mins	120C	30 min to heat up pot (mixed by previous user)
05/03/2018	1: Diffusion	wbclean1 + SRD	K1-15, T1-10	10 min, 30 sec, 10 min	50C, RT, 50C	SC1, 50:1 HF, SC2
05/03/2018	1: Diffusion	thermco3	K1-15, T1-10	2 hours	1100C	3WETOX recipe in T1, hour to heat up, 2 hours to cool down
05/04/2018	2: Mask #1 (SiO2 Defiinition)	svgcoat2	D5-6, K1-6	x	x	1 um 3612 w/ VP, 5 mm EBR (5000 Rpm, 60 s 90C bake)
05/05/2018	2: Mask #1 (SiO2 Definition)	Heidelberg	D5-6, K1-6	2 hours	x	Fast Mode, Dose 110 and Defocus -2 (80 was underexp)
05/05/2018	2: Mask #1 (SiO2 Definition)	svgdev2 post exp bake	D5-6, K1-6	60 s	110 C	60 seconds 110 C (hotplate recipe #1)
05/05/2018	2: Mask #1 (SiO2 Definition)	Develope and Hard Bake	D5-6, K1-6	90 s	110 C	Develop Recipe #3 (2x20s), hotplate Recipe #3 (90 seconds 110C)
05/07/2018	3: SiO2 Etch	p5000	K1-6, K7 dummy	180s	x	did 2 batches in case tool broke down, Recipe "CH B. Oxide" , turned off edge detection, gases matched book (25 CHF3, 50 CF4, 100 AR, 60 Gauss)
05/07/2018	3: SiO2 Etch	gasonics	K1-6, D6	x	x	Recipe 0-1-3
05/07/2018	3: SiO2 Etch	wbclean_res_piranha + SRD	K1-6, D6	20 min	120C	SRD was ok
05/09/2018	4: Pyramid Etch	wbclean_res_HF + SRD	K1-6	30 seconds		50:1 HF, lesson learned about DI water bath prep BEFORE dip.
05/09/2018	4: Pyramid Etch	wbflexcorr3&4	K1-6	90 min	80C	want SiO2 to remain, not all pyramids will be full (1 hour to prep tool, see next tab for better notes)
05/09/2018	4: Pyramid Etch	wbdecon	K1-6	20 min	70 C	30 min to heat up, SRD 1 wafer broke on loading
05/09/2018	4: Pyramid Etch	wbclean_res_piranha +SRD	K1-6			
05/11/2018	4: Pyramid Etch	wbclean_res_HF + SRD	K2-4	30 seconds		50:1 HF, lesson learned about DI water bath prep BEFORE dip.
05/11/2018	4: Pyramid Etch	wbflexcorr3&4	K2-4	45 min	85C	want SiO2 to remain, not all pyramids will be full (1 hour to prep tool, see next tab for better notes) SiO2 thickness after is 3230A
05/11/2018	4: Pyramid Etch	wbdecon	K2-4	20 min	60 C	took too long to heat up, SRD 1 wafer broke on loading
05/14/2018	4: Pyramid Etch	wbclean_res_piranha +SRD	K3-4	20 min	90 C	
05/14/2018	4: Pyramid Etch	wbclean_res_phosphoric +SRD	C1	50 min	155C	brown residue on handle (possibly piranha skip issue) (skipped dance class for this!)
05/14/2018	5: AlGaN/GaN Growth	wbclean1 + SRD	K3-6, C1	10 min, 30sec, 10 min	50C, RT, 50C	did HF between SC1 and SC2, hope that doesnt make a difference, had to do SRD twice (wasn't dry first time)
05/14/2018	5: AlGaN/GaN Growth	aix-ccs	K3-6, C1			loaded into tool, Plan is to use K3 (best alignment, 300 nm SiO2, should be ok)
05/15/2018	Mask #2 Order	Compugraphics	Ohmic metals only			bright data (for liftoff), mask review approved by CC, AY, PS & HA Monday 5-7, need parity flipped for proper alignment....CHECK past masks (X), messed up CD size on form at first
05/15/2018	5: AlGaN/GaN Growth	aix-ccs	K3			comes out contaminated, used recipe: 001_HEMT_on_Si_heater2, Took K3, K4 and K6 out of the box with a 111 wafer
05/15/2018	Approve mask	remoteview (compugraphics)				CD form updated. Should be shipping today
05/16/2018	5: AlGaN/GaN Growth	nanospec/ microscopes	K3			too rough for nanospec, white powder appearance and looks wierd man
05/16/2018	6: SiO2 Removal Attempt	wbflexcorr	dummy first (p5000 k7 (4011 A), K3			BOE 6:1 (910 A/min -> 2mins K7 .4 minutes K3) or BOE 20:1 (300 A/min ->4 min K7, 12 mins K3)
05/16/2018	SL1: Debugging Oxide	wblitho				mixed New batch of spraycoater resist, see tab for recipe
05/17/2018	SL1: Debugging Oxide	headway	K3, K2	1 min, 1500 rpm	120C, 5 min	220 7 resist from a syringe
05/17/2018	SL1: Debugging Oxide	Wafersaw	K2, K3	hub blade		recipe kd_my_si, cut into quarters, QIV was cut futher to get test pieces for debugging oxide removal
05/17/2018	SI1: Debugging Oxide	Artnet pro	Mask 1.5			SiO2 mask & new one but each side is brought in about 2 um. Need to decide which mask to use for real one
05/18/2018	SL1: Debugging Oxide	wbflexsolv	K3 pieces of QIV			Acetone soak for about 5 mins, A/M/I soak/rinse following
05/18/2018	SL1: Debugging Oxide	novaSEM	K3 pieces of QIV			5 kV or 2kV beam, single lense mode, Imaged surfaces and a few cross sections, issues wtih astigmation arose
				4 min (PR), 33 min (sample), 29 min (PR),		
05/19/2018	SL1: Debugging Oxide	ox35	K3 pieces of QIV, dummy resist wafer	10 min (sample)		recipe is "Xlab GaN etch tst" (about 100 nm/min and 1:1 selectivity with PR)PR etch rate for spray coat resist found to be about 100 nm/min, 6 um resist is sufficient for this
05/19/2018	SL1: Debugging Oxide	svgcoat2	K8, K9, 1 dummy	120s	90C	5000 rpm 3612, 1 um resist, 2 mm EBR
05/19/2018	SL1: Debugging Oxide	Heidelberg	K8, K9	7 min each		110 dose, -2 exposure, used gds file for pocket wafer
05/19/2018	SL1: Debugging Oxide	svgdev1	K8, K9	60 s PEB, 60 HB	115 C	some challenges with badger enabling and alarms going off. Wierd. someone helped me fix it.
05/19/2018	SL1: Debugging Oxide	p5000	K8, K9	180s		"Ch. B Oxide" etch recipe
05/19/2018	SL1: Debugging Oxide	gasonics	K8, K9			"0-1-3"
05/19/2018	SL1: Debugging Oxide	pt-DSE	K9,K8	200 cycles, 289 cycles		"DSE FAT EBTr"
05/19/2018	SL1: Debugging Oxide	wbflexsolv	K3 QIII, Pieces, K2QI			Acetone soak for about 5 mins, A/M/I soak/rinse following
05/19/2018	SL1: Debugging Oxide	yes! oven	K3 QIII, Pieces, K2QI, K8, K9, 2 Si dummies (cont)			prepping for spray coater
05/19/2018	SL1: Debugging Oxide	evgspraycoater	Si Dummy A, Si Dummy B, pieces, 2um receded and regular,			accidentally baked at 120 C instead of 90 C
5/23/2018	SL1: Debugging Oxide	karlsuss	quarter wafers too	2 secs x 7 cycles, 30 s rest		
5/23/2018	SL1: Debugging Oxide	wbmisc	pieces, 2um receded and regular			slow develope since baked at 120c....>60 seconds
5/23/2018	SL1: Debugging Oxide	drytek2	pieces, 2um receded and regular			
5/24/2018	SL1: Debugging Oxide	ox35	pieces, 2um receded and regular	33 min, extra 5 mins for another		
5/24/2018	SL1: Debugging Oxide	karlsuss	dummy and quarters	2 secs x 7 cycles, 30 s rest		40 um align gap, soft lithography, mask was flipped (did not invert for transparency), did regular SiN mask design (not 2 um receeded)
5/24/2018	SL1: Debugging Oxide	wbmisc				
5/24/2018	SL1: Debugging Oxide	ox35	quarter		38 min	did chamber clean with Def Cl2 SF6 O2
5/24/2018	SL1: Debugging Oxide	wbflexcorr1	quarters			6:1 BOE, 3 mins
5/25	7: Mask #2 (Ohmic Metals)	wblitho	--			Mix more spraycoater resist in a new jar (need more!) 24 hours before coating (Target Wed 5-16-18), get casset or wafer holders for these
5/26	7: Mask #2 (Ohmic Metals)	yes oven				bring 3 regualr Si dummies, bring 1 pyramid dummie
5/26	7: Mask #2 (Ohmic Metals)	evgspraycoater	dummies, pockets, quarters			
5/27	7: Mask #2 (Ohmic Metals)	karlsuss	dummies, pockets, quarters	1.9sx7, 30 s rest		sodaline mask
5/27	7: Mask #2 (Ohmic Metals)	wbmisc	dummies, pockets, quarters	50 sec dev		
5/27	8: Ohmic Liftoff	drytek2	quarters, dummies			300 mTorr, O2 deviation light, a tad sketch
5/27	8: Ohmic Liftoff	AJA evaporator	quarters, dummies			Ti - 20 nm, Al - 100 nm, Pt-50 nm, Au - 40 nm, used mostly the fast etch rates (except gold at 1 A/s not 2 A/s)
5/27	8: Ohmic Liftoff	wbsolvent	quarters, dummies			1165 soak 2 overnights, sonicated 20 seconds at high power after a few AMI rinses
5/29	8: Ohmic Liftoff	Heli	quarters, dummies			Measure ohmic structures, some are ok, but nothing worth really recording yet
5/30	9: Anneal Ohmic Metals	RTA	2 Si Dummy, 2 pyramid dummies, real wafer	35s, 850 C, N2 ambient		
5/30	9: Anneal Ohmic Metals	Heli	real wafer			electrical inspection (conitnuity, isolation) pyramid-pyramid edges. it was ok, but higher resistance than expected on no Oxide removal sample, really low on removed oxide sample, Gold messed up Si substrate I think
5/31/2018	9: Anneal Ohmic Metals	Zeiss FESEM (Beckman)	Quarter with and without oxide removal			10 MeV backscatter mode, beautiful images
5/31/2018	11: Wirebond PRactice	Wirebonder-SNC	non removed quarter			did not work - need bondmetal
6/26/2018	11: Mask #3 (Bond Metals)	yes oven	quarters (3), dummies(2), pockets (2)			
6/26/2018	11: Mask #3 (Bond Metals)	evgspraycoater	quarters (3), dummies(2), pockets (2)			6 passes, new solution of resist. see labbook for results
scheduled 6/27	11: Mask #3 (Bond Metals)	karlsuss				transparency mask
scheduled 6/27	11: Mask #3 (Bond Metals)	wbmisc				
scheduled 6/28	12: Bond Liftoff	drytek2				
scheduled 6/28	12: Bond Liftoff	AJA evaporator				
scheduled 6/28	12: Bond Liftoff	wbflexsolv				
scheduled 6/30	12: Bond Liftoff	practice wirebond				
scheduled 6/30	12: Bond Liftoff	Heli				
7/1	12: Bond Liftoff	headway				
7/1	12: Bond Liftoff	wafersaw				
	13: Packaing	wirebonder SNC				

Spray Coater Resist Recipe

	220-7 (7.5%)	MEK (68%)	PGMEA (SU8 Developer, 24.5%)	
Amount	15g	136g	49g	for 8 oz bottle
	30g	272g	98g	for 16 oz bottle

use scale, measure by weight. MEK is nasty stuff, be very careful!
pour in order listed into provided beaker, then into jar
must prep > 24 hours

KOH Etching

05./09/2018

1 Fill up bin halfway
2 Blue tags for water, KOH
3 big beakers: Nalgene (clean), KOH clean, Glass cont (later for aspiration), condenser cap, condenser hose
4 Choose your solution at this website : www.lelandstanfordjunior.com/KOH.html (2500 mL will cover 4 inch wafers)
5 I chose 30% KOH, so I poured 1500 mL of KOH then sprayed 1000 mL of water INTO CLEAN NALGENE BEAKER
6 pour mixture into quartz clean beaker (slippery, wear vinyl gloves on top of yellow gloves)
7 Place quartz wafer into bath (half full remember!) - careful, the llittle balls shouldnt be under the beaker. Go slowly!
8 place condenser cap on beaker, connect short tube from city water to top spout, get long tube and connect low spout to hole
9 turn on city water, fill the tank to the lower sport, turn down til water is just a trickle out exit tube
10 turn on CTB, set to about 90 C (for 85C), wait 40 min
11 Rinse out nalgene beaker, aspirate from a CONTAMINATED BEAKER not the clean beaker!
12 after 20 mins, prep wafers for HF dip at wbclean_res_H
13 30 second 50:1 HF dip, followed by 3 min soak in DI water (Lesson learned: prep DI water FIRST)
14 transfer wafers to KOH holder (red dot, clean KOH)
15 place wafers in nalgene bath until etch at desired temp
16 open up KOH bath : remove tubes on city wafer/ condenser
17 place condenser head on a clean wipe
18 put wafers in quartz bath, mix up and down a little, remove handle & place handle in nalgene water bath
19 put condenser head back on, replace tubes and turn city water back on to a trickle
20 monituor temperature of bath, I changed to 80 C for 90 mins (instead of 85 for 2 hours) because of fear of SiO2 mask etching off. 90 mins should leave ~200 nm behind
21 Lesson learned: MAKE SURE RETURN PIPE is SEALED TIGHT (Some water leaked into KOH bath....will have underetch)

22 93 mins was my actual run time today
23 before removing wafer, give yourself 10 mins to prep decontamination bath, it was ready in about 20 mins for heating up to 70C
24 clean condenser head (empty and rinse bottom without touching it
25 pour KOH into cont beaker and aspirate
26 transfer wafers to wbdecon cassete, can do flippy thing!
27 rinse out whats left, aspirate contaminated things
28 disable
29 move wafers to decontamination (5:1:1 H20:H2O2:HCl
30 20 mins at 70C
Rinser
SRD
pirahna if there's time — there is time

Plan: Redo this for 60 more minutes of KOH etching on a few wafers. — did 45 mins at 85C only on 3 wafers

Oxide thickness post etch ~600 nm, largest cavity etch ~130 um (need about 50 um more, lets say 45 minutes at 80C, or 30 min at 85C) — (pick the best 3 I guess)

MOCVD Recipe: 001_HEMT_on_Si

Notes from Savannah's run on 5-4-2018

Substrate 100 mm (111) Si, p/B Re<1, 750+- 25 um

Growth Conditions:

TmGa_1	5 degC	1900 mbar	71.14 g
TmAl_1	20 degC	1300 mbar	26.11 g

Step	TMAl_1	TmGa_1	NH3	SiH4	Time	Temp	Pressure
Bake				100/60/100	6001	1031/1230	300
Lt AlN	25/175		134/100		720	1029/1290	50
HT AlN	25/175		134/100		1980	1137/1455	50
Al80Ga20N	45/155	4/196	1341/100		1430	1081/1330	100
Al50Ga50N	25/175	8/192	1341/100		2308	1083/1330	100
Al20Ga80N	13.3/186.6	14.1/185.9	1341/100		3240	1075/1330	100
GaN		91.1/108.9	6000/100		2000	1041/1295	400
AlN	5.5/194.5		670/100		40	1032/1295	100
AlGaN	5.5194.5	7.6/192.4	670/100		360	/1280	100
GaN		7.6/192.4	670/100		30	/1280	100

Karen's Growth on Pyramids (expected 5/15/2018)

Substrate 100 mm (100) Si pB Re 10-20 Ohm cm 525 +- 25 um, KOH etched pyramids structures (deepest etch is 140 um deep) (L prime)

- bowing conditions will be different, thickness measure will likely not work

Checks

O2 Monitor	
N2 Monitor	Pressure 120-130 or 55
H2 Monitor	60 or 50
Cooler	80 PSI +- 5
Chiller	50 C
Scrubber	No alarms, no red light (575 upper, 500 lower)

TmGa	5C
TmAl1	20C

cooling water marked

Appendix D

Operator Manual for Noise Measurements

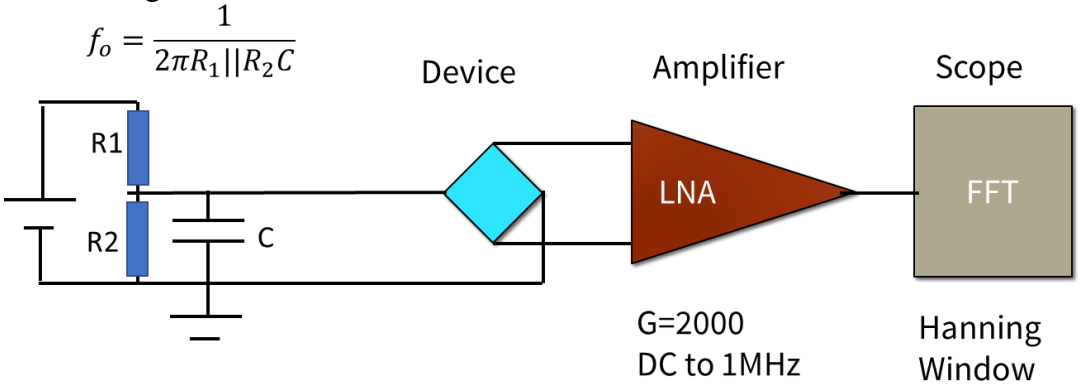
Noise Measurements of Hall Devices
Instructions
Karen Dowling

0. Bill of Materials, Bench Development Considerations

Read this section to understand how to develop this setup for your own lab. It's likely you don't need to repeat everything here, but it's useful to know how this works and where to get things if something breaks.

Here's the general idea:

$$f_o = \frac{1}{2\pi R_1 || R_2 C}$$

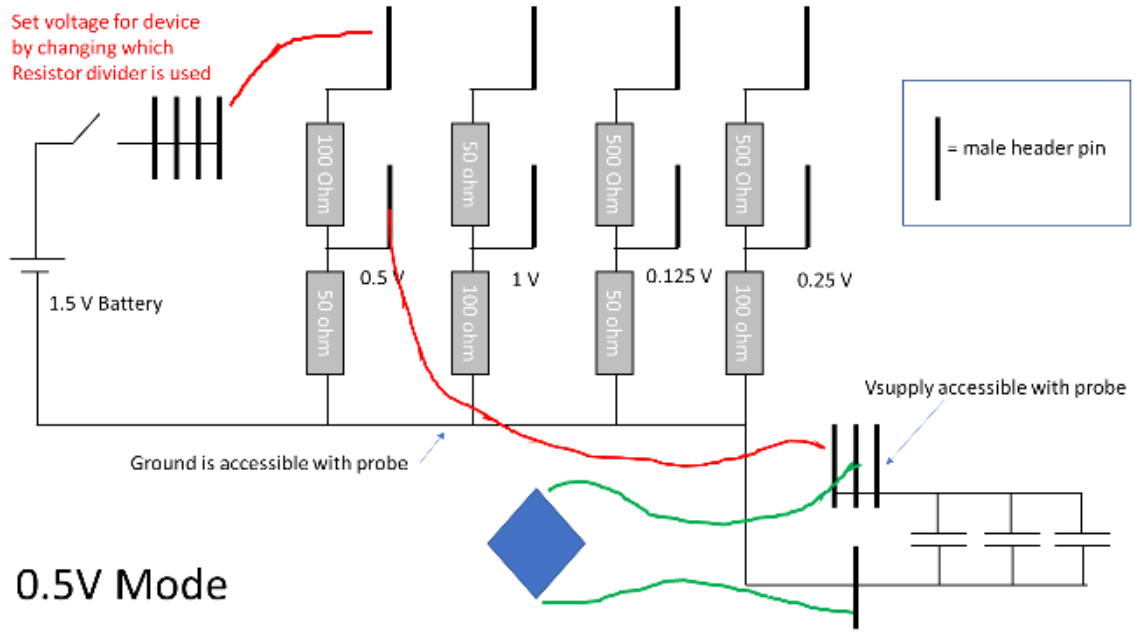


DC Power and Filter

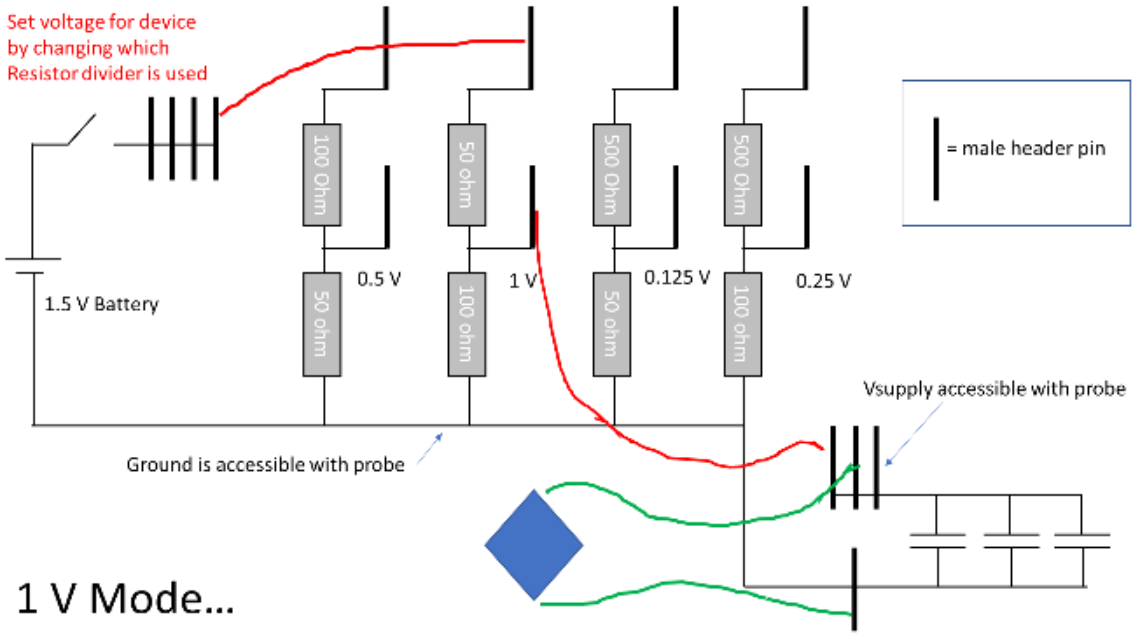
1.5 V AA Battery
1 x Battery pack (modified to use 1 battery)
Low-noise foil resistors from Digikey (copy of original order – spare parts provided)

Quantity	Part Number	Manufacturer Part Number	Description	Reason
10	445-181218-ND	FG11X5R0J107MRT00	CAP CER 100UF 6.3V X5R RADIAL	Low Pass Filter in DC power to sensor
10	PPC3W100CT-ND	AC03000001000JAC00	RES 100 OHM 3W 5% AXIAL	Low Pass Filter and Voltage Divider in DC power to sensor
4	PPC5W500CT-ND	AC05000005000JAC00	RES 500 OHM 5W 5% AXIAL	Low Pass Filter and Voltage Divider in DC power to sensor
5	PPC3W50.0CT-ND	AC03000005009JAC00	RES 50 OHM 3W 5% AXIAL	Low Pass Filter and Voltage Divider in DC power to sensor
1	Y0706-1.0KA-ND	Y07061K00000T9L	RES 1K OHM .4W .01% RADIAL	Reference Resistor for Debugging system
1	Y0706-10KA-ND	Y070610K0000T9L	RES 10K OHM .4W .01% RADIAL	Reference Resistor for Debugging system
1	Y0062-100KA-ND	Y0062100K000T9L	RES 100K OHM 0.6W 0.01% RADIAL	Reference Resistor for Debugging system

A protoboard with varied resistor, capacitor combinations was made. It follows this schematic:



Circuit drawing of the green protoboard, used to supply voltage to the hall device (The blue diamond). Red and green lines correspond to the wiring using breadboard jumper wire.



The squiggly lines represent external wires used to complete the connections. *Always* check V_{supply} before taking a measurement, to know you set it up correctly.

Device

Hall devices with 4 terminals, from XLab or commercial, or collaborator provided. Ideally packaged on a PCB with 4 male header pins provided.

Amplifier (Description of how it was modified, not done every day)
Low noise amplifier from Stanford Research Systems (SR 560). Borrowed from Prof. Amin Arbabian's group, with two key alterations:

1. Replaced batteries in unit with 3 new lead acid batteries from Batterymart.com.

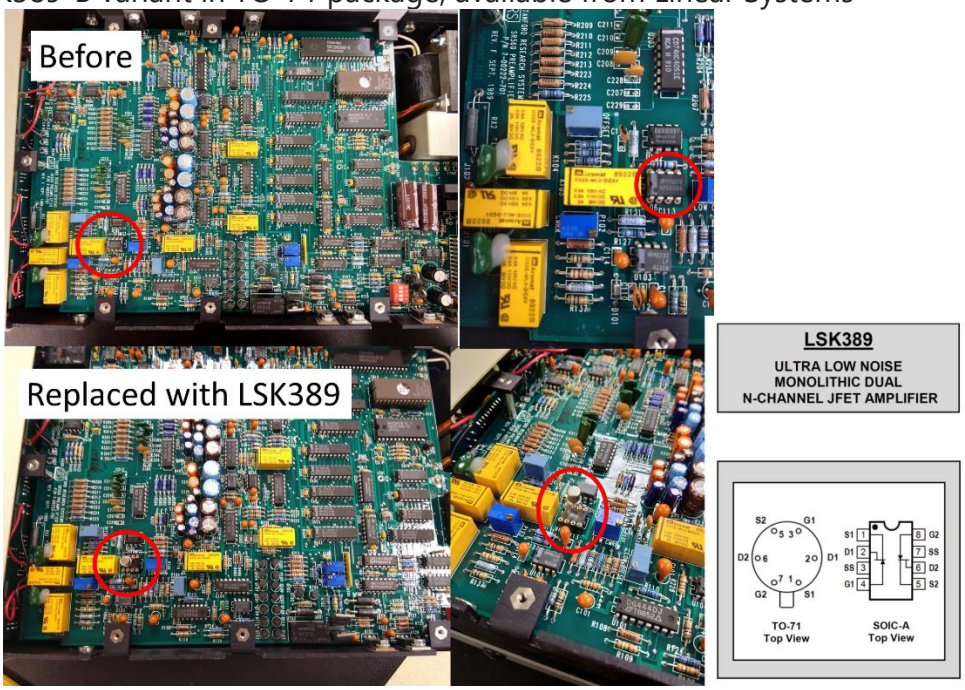
12 Volt 2.2 Ah Sealed Lead Acid Rechargeable Battery - F1 Terminal
Item #: SLA-12V2-3
Overstock Sale Item: $6.00 in Savings!

2. Replaced from end FETs with new JFETs (only during bench development)

Follow this instructable: https://www.instructables.com/id/How-to-repair-a-Stanford-Research-SR560-Low-Noise-/

Using this:

LSK389-B variant in TO-71 package, available from Linear Systems



3. Calibrate the SR560 after replacing the FETS, using this procedure. Information on CMRR, splitters, etc. can be found at: https://www.thinksrs.com/downloads/pdfs/other%20stuff/SR560Offset.pdf

Oscilloscope
The device we use is the picoscope (borrowed from Prof. Boris Murmann's group in Stanford EE). The part number is 5444B. It is currently not sold anymore because it has been updated. We run it with two MATLAB driver packages provided by Dr. Muratore, included in the lab shared drive ("Noise Measurement Procedures") We run it with the USB cable powered and data driven to XMachine computer. Wall power can also be used. The code used may require modification if newer drivers or devices are used instead.

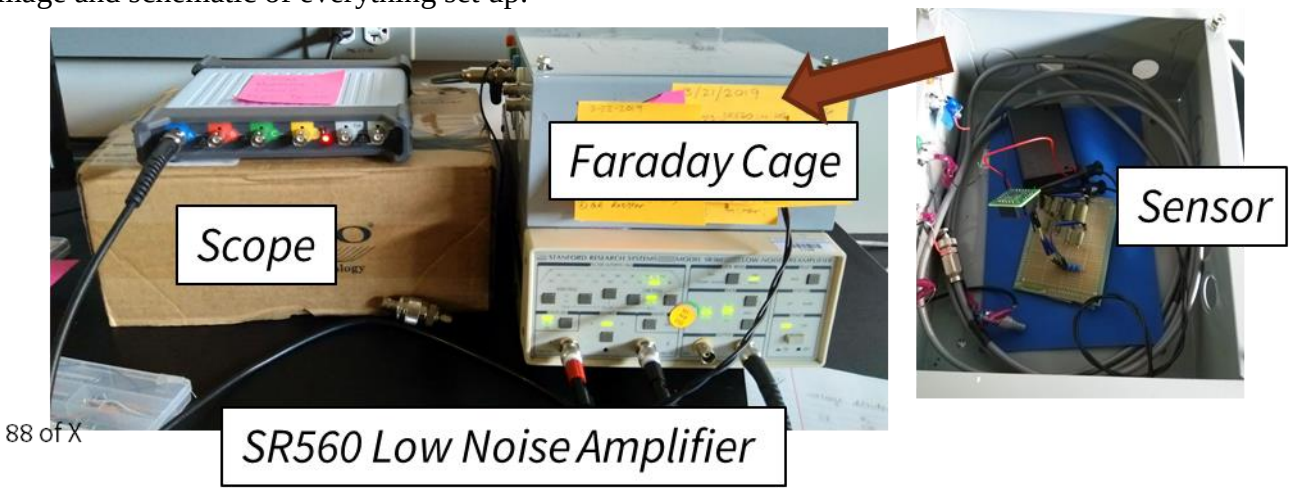
Wiring
4 female breadboard wires, shortened
1 BNC cable
2(3) banana-clip wires.

The battery DC filter is soldered together on protoboard, with male header pins available for connections. Four shortened female protowires are needed (two for board configurations, two for device connections).

SR560 is connected to Hall device with BNC-banana adapters on A and B inputs (differential), with banana-clip wires. (Occasionally, a third banana-clip wire is used to ground the device to a reference ground, if it has a fifth terminal to substrate – like Infineon's silicon devices).

SR560 is connected to picoscope with BNC cable from 50 ohm output. Ideally a short, low noise cable should be used.

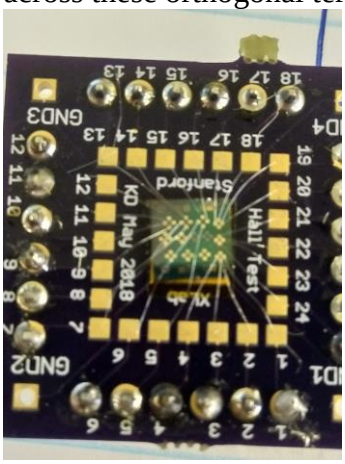
Image and schematic of everything set up:

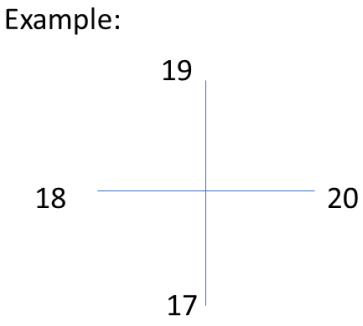


1. Initial Setup for Real Experiments

1. LNA Prep
    a. Charge the LNA (it takes a few hours) by plugging it into the wall. Once charged, you can unplug, turn it on, and use it for 15-20 hours before it needs a recharge.
    b. Suggestion: Charge overnight, run experiments all day, charge overnight, etc.
    c. Leave the input as GND for now (not DC or AC).
2. Device Prep
    a. I assume you have your device packaged on a PCB or board with accessible pins, already wire-bonded or similar.
    b. Make a diagram of your devices outputs and inputs. For Hall devices, these are the opposing pairs (one for supplying a current or voltage, and one for measuring output voltage). Know your pin numbers for plugging into. Measure resistance

across these orthogonal terminals. (In example, R between 19 and 17)





c. Clip output voltage pins with wires for input of LNA.
d. Configure device for measurement: float mode (no input power) to get thermal noise curves will not use the protoboard, protoboard (with input power) will get 1/*f* noise curves, wire using the green wire connections in the schematic in section 0.

3. After Hardware is wired up
    a. Plug Picoscope into computer
    b. Connect BNC to channel A of Picoscope, and 50 ohm output of LNA
    c. Connect device outputs to LNA A and B
    d. Set LNA settings up. Recommended ones here (should be saved at turn on):
        i. AC coupled input (switch over from GND)
        ii. Gain = 2000 (for Hall devices in this Thesis)
        iii. Low pass filter at 100 kHz at 6 dB/oct
        iv. Make sure the battery is being used, not the wall
        v. *Do not* let the OVLD red light come on. Reduce gain/ bandwidth as needed. This will damage the front end JFET and will need replacement. Those parts aren't cheap. If its on a first, reduce gain until red light is off, wait a bit, then slowly increase gain until you're back to your setting.
    e. Check Picoscope waveform before running in MATLAB
        i. Open "Picoscope 6" software
        ii. Check waveform on the screen – change axis and coupling, as needed. Waveform should be stable and close to zero. (not railed at 5V or similar). Signal should be smaller that 500 mV in AC coupled mode.
        iii. Close Picoscope6
4. Set up MATLAB code to run this. Most things are already set, but here are a few checks to make or things you can modify.

See this folder on box for needed files (**https://stanford.app.box.com/folder/85404090493** Must be a member of Prof. Senesky's group) These drivers and code will need an update if a different model of the picoscope is used. (Updates changed some system protocols.)

First, setup drivers from these two folders (and subfolders) to be in the path of the code:

\picotech-picosdk-matlab-picoscope-support-toolbox-c715c96
\picotech-picosdk-ps5000a-matlab-instrument-driver-df18ae9

Add both these picotech folders and subfolders to the path! These have all the functions to run the picoscope. Also make sure your MATLAB folder has “getAveragePSD.m”

```
%% CHANNEL SETUP FOR NOISE
% All channels are enabled by default -
% switch off channels C and D so device can be set to 15-
bit resolution.

% Channel A
channelSettings(1).channel =
ps5000aEnuminfo.enPS5000AChannel.PS5000A_CHANNEL_A;
channelSettings(1).enabled = PicoConstants.TRUE;
channelSettings(1).coupling =
ps5000aEnuminfo.enPS5000ACoupling.PS5000A_DC;
channelSettings(1).range =
ps5000aEnuminfo.enPS5000ARange.PS5000A_1V;
channelSettings(1).analogueOffset = 0.0;

channelARangeMV =
PicoConstants.SCOPE_INPUT_RANGES(channelSettings(1).range +
1);
```

Here, the channel is set up for channel A to have AC coupling and 500mV resolution. Note the all caps in the statements. Leave these be if you’re confused.

```
% GET TIMEBASE

% Driver default timebase index used - use
ps5000aGetTimebase or
% ps5000aGetTimebase2 to query the driver as to suitability
of using a
% particular timebase index then set the 'timebase'
property if required.
% Ts = (tb - 2)/125e6

% timebase     : 65 (default) -> ~2 MS/s
% segment index: 0

time_base = 65; %I usually use 65, others use 7
[status.timebase, timeIntervalNanoSeconds, maxSamples] =
invoke(ps5000aDeviceObj, 'ps5000aGetTimebase', time_base,
0);
set(ps5000aDeviceObj, 'Timebase', time_base);
```

```
fs = double(1e9/timeIntervalNanoSeconds);
```

Here, sampling rate can be changed by modifying `time_base`. 65 provides 2 MS/s (1984126 Samples/second) datalogging speed, which is plenty for low frequency noise measurements. fs is the sampling frequency, and Ts is the time period of the sample. 65 is good for most cases. You could make it bigger to reduce max frequency, and could make it smaller to increase bandwidth. Just leave it at 65 if you're confused.

```
%%
% settings for front-gate input
configFG.Tmeas = 1;
configFG.nRuns = 1000;
configFG.fs = fs;
```

This is VERY IMPORTANT. `Tmeas` sets how long a measurement will be (in this case, 1 second). `nRuns` is the number of repeated measurements (in this case, 1000) – this means this code will run for 1000 seconds, plus dataprocessing and recording time, which is about 30 mins. After all the measurements, they are averaged together to get a power spectral density array that is the average. This is because noise is a stochastic process and several averages are needed to get the real spectrum. Just leave it if you're confused. You can speed up the data processing by changing nRuns to a smaller number, but your data will be less smooth. Changing `Tmeas` will change the sizes of your data arrays, so it's harder to compare with baselines. Stick to one Tmeas and time_base for your whole study. Shorten `nRuns` if you want to speed things up and sacrifice smooth curves.

```
for i = 1:1
```

I usually repeat the whole measurement function a few times, in case the first measurement deviates from the later ones. (Low frequency discharge is very, very finicky!) I have done i=1 and i=1:10 before; it depends. I typically stick to 3. This will be about 1 hour/device datapoint. If rushed for a deadline, set i=1.

```
figure(1)
loglog(f,PSD.^2,'linewidth',1.5), hold on
xlabel('Frequency [Hz]','fontsize',14)
ylabel('PSD [V^2/Hz]','fontsize',14)
title('Measured PSD Input OTA','fontsize',14)
grid on
xlim([0.1 3e5])
set(gca,'fontsize',12,'linewidth',1.5)

figure(2)
A=open('batt2000ac100k_short_float_USB1s65tb500mV6n1000_dat
a.mat');
loglog(f,(PSD.^2-A.PSD.^2)./2000^2,'linewidth',1.5), hold
on
```

```
xlabel('Frequency [Hz]','fontsize',14)
ylabel('Input Ref PSD [V^2/Hz]','fontsize',14)
grid on
xlim([0.1 3e4])
set(gca,'fontsize',12,'linewidth',1.5)

%% Update resistance here
SV=830*1.38e-23*300*4*ones(1,length(f)); %4KbTR
loglog(f,SV), hold on
```

Figure 1 will plot the raw PSD data. Figure 2 will subtract it from a known baseline measurement from before (so you may need to change this if your settings are different than mine). Also make sure to record a baseline measurement file to enable this feature.

The "523" in the update resistance section was an example of a device's resistance. Update this for your device, and you can check the theoretical thermal limit of noise against your measurements. It's a good sanity check.

```
%% save the files, update here
filename = 'batt2000ac100k_southGE_0.207V_USB1s65tb500mV';

save([filename,num2str(i),'n',num2str(configFG.nRuns),'_dat
a.mat'], 'f', 'PSD');
```

MOST IMPORTANT – UPDATE FILENAME FOR EVERY NEW DATA POINT.

[LNAsettings]_[Device under test]_[bias voltage settings]_[picoscope settings]

LNA settings:
Batt – battery powered
2000 – gain
Ac – ac coupled
100k – low pass filter setting

Device under test:
This depends on you, the user. My work followed this format.
Diameter, shape, fabrun, material
"short" for baseline system measurements without a device.

Bias voltage settings:
Measured on protoboard before start, true voltage send to device
"float" for non-powered versions.

Picoscope settings:
USB – USB powered
1s – Tmeas

65tb – time_base is 65
500mV – Range is set to 500MV

You see in the save section, the code will automatically update for each iteration (i) and # samples measured from nRuns.

Finally:

```
%% DISCONNECT DEVICE

pause(100); %wait 1s before going again
toc

end
if(1)
    disconnect(ps5000aDeviceObj);
    clear all
end
toc
```

Pause can be used to let the system "rest" between iterations, but it is not necessary. Right now, it is set to 100 seconds.

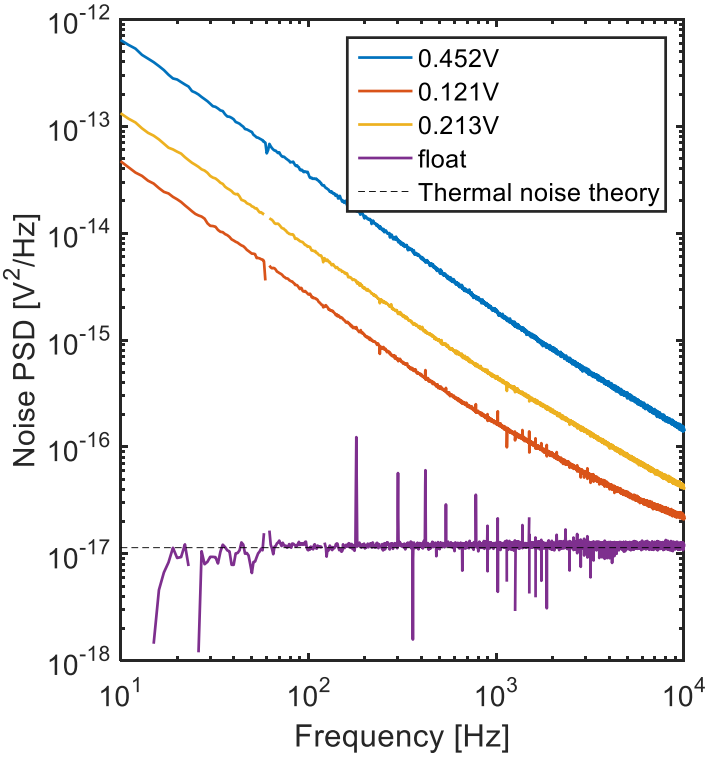
The code ends by disconnecting the picoscope from MATLAB (to release the memory and communication port to the rest of the computer). This is important. If the code is halted early, run the disconnect(ps5000aDeviceObj) in the terminal to free the device to the computer.

Toc will report the time that passed, to help you plan timing of future measurements.

Sometimes things slow down too much. Close and reopen MATLAB and re-add the driver paths and continue. This is likely due to the plots getting really big with all the large data sets.

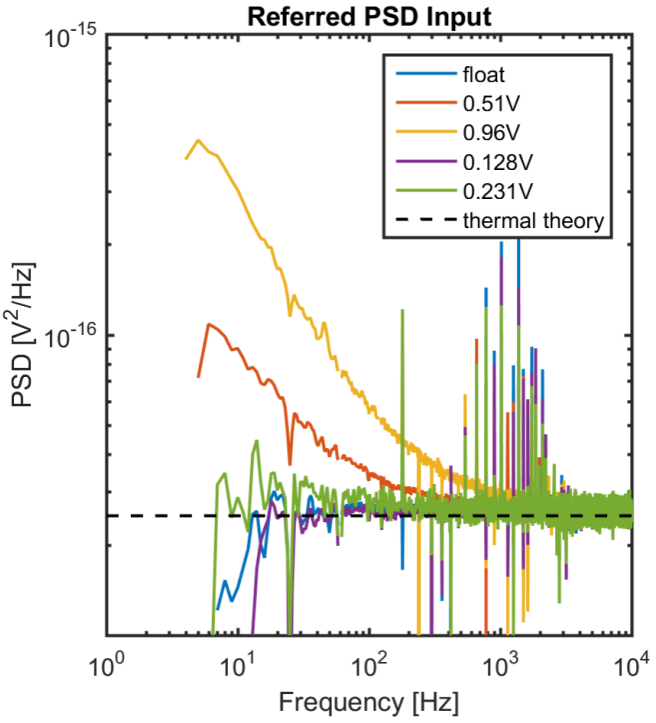
Intermediate Data collection Considerations

Suppose your first 0.5 V measurement looks like this, since your device is very noisy:

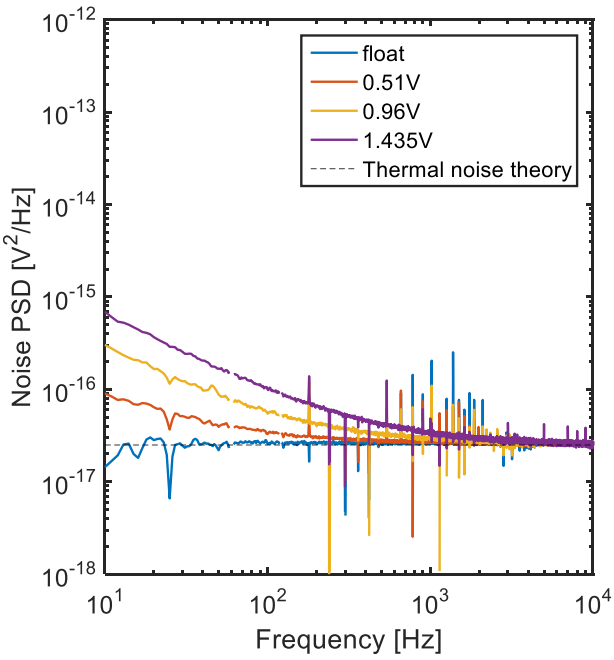


You may not need to measure the 1 V setting, since it will be really big, might OVLD the LNA, and you won't learn much. Modify your voltage choices and use the lower settings.

Suppose your measurement was too small, and you can't really see anything:



Consider boosting your supply voltage, so you can see something. You can go directly to the full battery setting too:



Basically, don't blindly go through the device checklist – make sure the outputs are sane. You can plot them on the same graph between measurements and make sure things make sense. If there's something fishy, repeat those measurements UPDATE FILE NAMES so you don't overwrite data.

This is a first draft of the manual. Best of luck processing your data and learning about the noise measurements of your devices.

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