RESONANT-TYPE ARCHITECTURES FOR ACTIVE POWER DECOUPLING IN GRID-TIED SINGLE-PHASE POWER ELECTRONICS

BY

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THESIS

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ABSTRACT

In single-phase power converters, twice-line frequency power decoupling circuits are used to buffer the instantaneous energy difference between the AC and DC sides of the converter. Active buffer implementations are used to reduce the volume and potentially improve the reliability of the converter by redistributing passive energy storage requirements with combinations of switches, capacitors, and inductors.

This thesis applies resonant impedance behavior to the operation of a specific DC-side twice-line frequency buffer called a series-stacked buffer (SSB). Utilizing this equivalent impedance model, an appropriate voltage-control scheme is derived and experimentally validated. There is also additional consideration of energy performance metrics in the context of DC-side buffers. Furthermore, the SSB equivalent impedance model is extended, applied, and generalized to the full single-phase converter system. This analysis includes an integrated system control method which imposes phase-locking and consistent transient stability. Experimental verification of full system interconnectivity is validated with a 1.5 kW power factor correction (PFC) boost flying capacitor multilevel (FCML) converter.

To my parents, brother, and family for their love and support.

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LIST OF ABBREVIATIONS

AC	Alternating Current
CCM	Continuous Conduction Mode
DC	Direct Current
FCML	Flying Capacitor MultiLevel
LED	Light Emitting Diode
PCB	Printed Circuit Board
PFC	Power Factor Correction
PSPWM	Phase-Shifted Pulse-Width Modulation
SSB	Series-Stacked Buffer

CHAPTER 1

INTRODUCTION

1.1 Introduction

Grid-tied single-phase electronic power converters are circuits which interface the ac electric grid to some system which supplies or requires dc electric power. Chargers for consumer electronics such as cell phones and laptops, photovoltaic (i.e., solar-powered) systems which supply renewable energy to the grid, electric vehicle chargers for on-board dc batteries, consumer lighting implemented with LED (light-emitting diode) technology, and power delivery to server buses in data centers are all applications which require ac-dc (or dc-ac) electric power conversion, and many of these technologies have significant expected future growth as they make up a developing portion of the power and energy industries.

There are pertinent performance metrics in every power electronics application which influence the design and implementation of the power converter. Among the most critical of these are efficiency and power density. Efficiency defines the percentage of electrical input power which converts to electrical output power. Less efficient converters require more power to be thermally dissipated from heat-sensitive components in order to prevent device/system failure. Volumetric power density is a measure of converter size with respect to the power it can process. There is generally a design trade-off between efficiency and power density [1, 2]; consequently, an innovative design seeks to simultaneously improve both.

In particular for single-phase converters, the dc side has constant power flow, while the ac side has a ripple component at twice the line frequency (denoted as ω_{2L}). To satisfy this power difference, an auxiliary sub-circuit must supply the twice-line frequency power component—often referred to as power pulsation buffering, energy buffering, or twice-line frequency buffering—and

is an inherent consideration in all single-phase systems. Energy buffering is nearly synonymous with the traditional ideas of signal filtering and as such is implemented with some combination of reactive (i.e., capacitive and inductive) energy storage circuit components.

The goal of this work is to improve the power density of the power pulsation buffer design by utilizing topological combinations of inductors, capacitors, and switches as well as proper control without degrading the efficiency when compared with traditional buffering solutions. Chapter 2 considers the fundamental motivations of the work regarding twice-line frequency buffering. In Chapter 3, electrical concepts of resonance are defined and applied to the design and control of a buffer to achieve these performance milestones. In Chapter 4, a particular resonant topology called the SSB (series-stacked buffer) is examined, an associated control technique is developed, and an experimental hardware prototype is validated. In Chapter 5, preliminary considerations are made for incorporating the SSB in a full single-phase system by addressing interaction and stability between the SSB and a PFC front-end. Chapter 6 explores defining metrics of efficiency and loss in the context of a DC-side twice-line frequency buffer. Finally, Chapter 7 concludes the work.

CHAPTER 2

BACKGROUND INFORMATION ON TWICE-LINE FREQUENCY ENERGY BUFFERS

Single-phase power electronics either convert a single AC voltage and current waveform to a DC voltage and current waveform, i.e., AC-DC or rectifier, or vice versa, i.e., DC-AC or inverter. Practical converters which process large amounts of power must be highly efficient, motivating the use of switch-mode type topologies to shape the instantaneous waveforms to the desired shape. Unique to single-phase converters, as opposed to three-phase converters, is a fundamental difference in the instantaneous power between the input and output powers. An additional energy buffer is then necessary to regulate this power difference.

2.1 Energy Storage in Single-Phase Converters

Twice-line frequency energy ripple is an intrinsic phenomenon in any single-phase power converter due to the instantaneous power difference between its AC and DC sides [3]. In order to maintain conservation of energy—and by extension, power—the difference in instantaneous power between the AC and DC side must be compensated by an auxiliary "power decoupling" circuit commonly referred to as an energy buffer as shown by the generalized converter schematic illustrated in Fig. 2.1. The DC and AC instantaneous power waveforms can be derived as

$$P_{dc} = v_{dc} i_{dc} = P_o \tag{2.1}$$

and

$$\begin{aligned} P_{ac} = v_{ac} i_{ac} &= (v_o \cos(\omega_L t))(i_o \cos(\omega_L t)) \\ &= P_o + P_o \cos(2\omega_L t) \end{aligned} \tag{2.2}$$

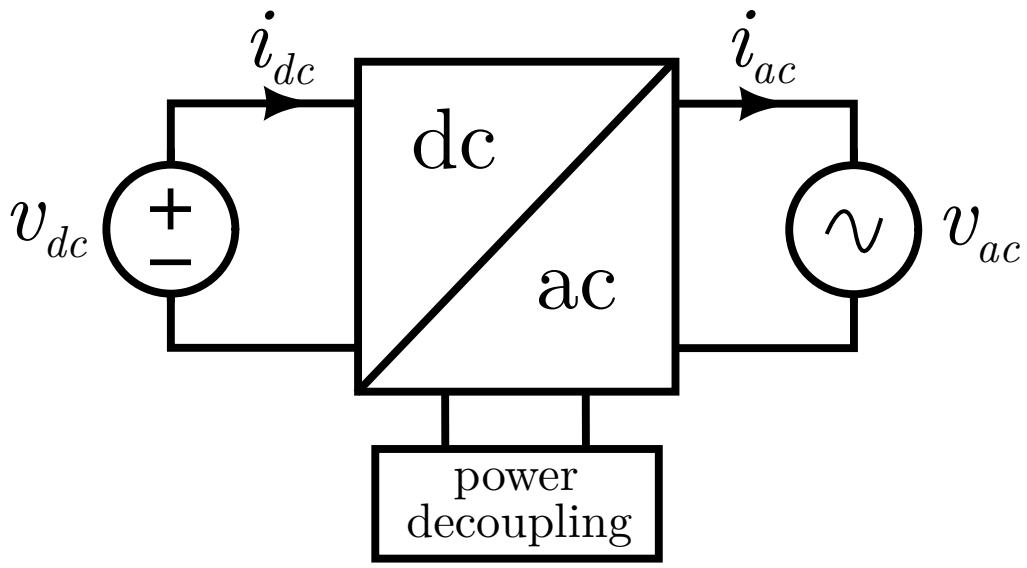


Figure 2.1: Generalized DC-AC converter schematic with instantaneous power decoupling sub-system.

respectively, and the power flowing into this buffer can be derived as

$$P_{buffer} = P_{dc} - P_{ac} = -P_o \cos(2\omega_L t), \tag{2.3}$$

where $\omega_L = 2\pi f_L$ denotes the line frequency of the AC side in radians per second, typically $f_L = 60$ Hz or 50 Hz, and P_o denotes the average power throughput of the converter. Notice the result in (2.3) contains a $2 \cdot \omega_L$ sinusoidal component with magnitude as large as P_o. Figure 2.2 better illustrates the marked disparity in power this decoupling circuit must buffer. For a DC-AC converter, or inverter, when $P_{ac} < P_{dc}$ for half of the $2\omega_L$ cycle, the buffer is storing energy. When $P_{ac} > P_{dc}$, the buffer is releasing the energy it stored in the previous half cycle. It is worth noting that for an AC-DC converter these conditions are reversed for releasing and storing energy.

Resistors are commonly used in non-power-intensive electrical circuits to provide natural damping of oscillations. In power electronics, however, intentional use of resistors in the primary power path proves far too lossy and dissipates too much heat to be practical. This implies a general design rule which minimizes all resistive elements in a power converter by using only combinations (or topologies) of capacitive, inductive, and switching circuit elements. The power decoupling buffer is no different in this requirement. The combination of oscillatory/periodic behavior and ideally equivalent en-

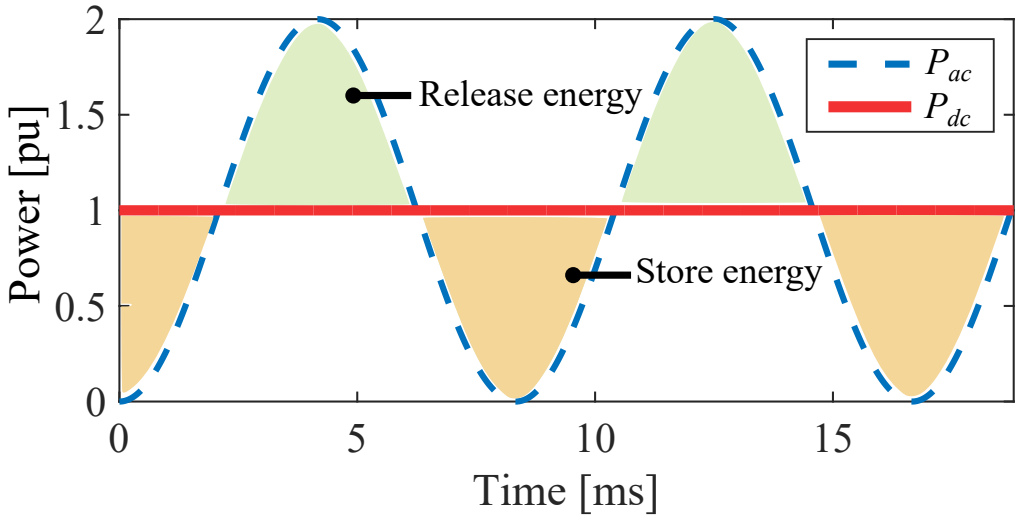


Figure 2.2: Instantaneous DC and AC power waveforms for DC-AC converter.

ergy released to energy stored over each ω_{2L} cycle means the buffer can be implemented "passively" as a combination of reactive circuit elements (i.e., inductors and capacitors), or "actively" with the addition of switching circuit elements (e.g., MOSFETs, IGBTs, GaN FETs, SiC FETs).

The design challenge then becomes clear as different combinations of capacitors, inductors, and switches—or topologies—as well as associated control strategies must be evaluated and explored thoroughly. The bases for comparison between designs are figures of merit such as efficiency, power density, DC bus ripple, cost, and reliability which quantify system performance. These performance metrics are then best utilized when defined as functions of system parameters and operating conditions such as v_{dc} or P_o.

2.2 Classification and Characterization

The twice-line frequency buffer shown in Fig. 2.1 is generalized, and as long as it functions to buffer the ω_{2L} power ripple of the single-phase converter, it can be implemented in any number of ways.

2.2.1 Passive and Active Buffers

The most obvious, and perhaps trivial, buffer characterization is between active and passive buffer topologies. Passive buffers utilize only combinations of capacitors and inductors/transformers to function. They tend to operate robustly and often implicitly reject system-level transient disturbances. Passive buffers also have relatively low component count which translates to minimal design effort and low cost solutions. There is also no high-frequency distortion characteristic of switch-mode converters which also simplifies design. Overall, passive buffers operate very robustly and offer a competitive solution for the large majority of single-phase applications—especially those tied to the grid. However, since component volume and frequency for passive components have an inverse relationship, purely passive buffer implementations tend to be large volumetrically as they must function for relatively low frequencies of $\omega_{2L} = 2\pi f_{2L}$. For typical single-phase applications the operating value of f_{2L} can range between 100 and 800 Hz.

Active buffer topologies, on the other hand, utilize both passive inductive and capacitive components and active switching components. Active buffer topologies effectively operate as switched-mode power converters and thus require an active control implementation. The greatest motivation for active buffers is most often volume reduction although greater reliability is another common consideration.

2.2.2 DC-Side Active Buffer Topologies

There are a number of specific types of twice-line frequency buffer topologies, but the most predominant is the DC-side buffer topology. In a DC-side buffer, the power decoupling circuit generalized in Fig. 2.1 is cascaded on the DC-side as shown in Fig. 2.3. In this configuration the DC-AC converter performs no twice-line frequency buffering, thus the instantaneous power at the AC-side as shown in (2.2) and at the intermediate bus must be equivalent:

$$P_{ac} = v_{ac} i_{ac} = P_o + P_o \cos(2\omega_L t) = v_m i_m, \tag{2.4}$$

where v_m is the intermediate bus voltage and i_m is the intermediate bus current. Assuming the single-phase system to be relatively immovable, the in-

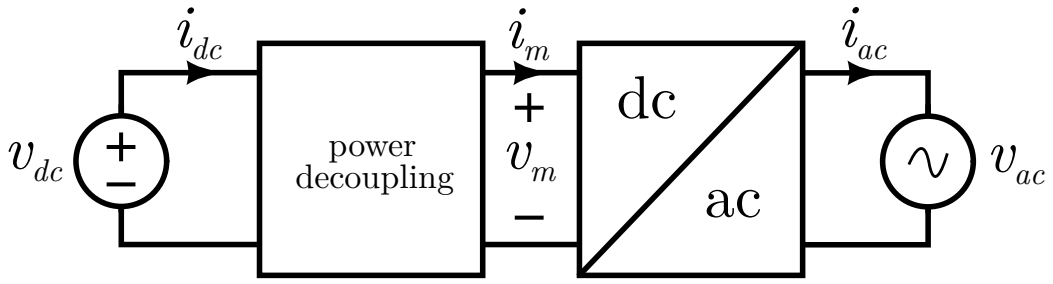


Figure 2.3: Generalized DC-AC converter schematic with DC-side power decoupling sub-system.

stantaneous power—but not necessarily the instantaneous voltage and current—at the AC and DC sides defined by (2.2) and (2.1) is fixed. In this scenario, only one state variable must be regulated on each side of the DC-side power decoupling circuit.

There are then three necessary conditions for successful operation of a DC-side buffer:

A1. Either the DC side voltage or current must be regulated to be constant (DC). Regulating one implies implicit regulation of the other from (2.1).

A2. Either the intermediate voltage or current must be regulated in some controllable way which does not render the buffer or single-phase circuit inoperable (i.e., an over-voltage or over-current condition). Regulating one implies implicit regulation the other from (2.4).

A3. The power decoupling circuit must contain passive energy storage elements (i.e., capacitors or inductors) sufficiently sized to regulate the instantaneous power ripple in (2.3) without rendering the buffer or single-phase circuit inoperable.

For the DC-side system described in Fig. 2.3, conditions A1, A2, and A3 are necessary for correct buffering operation.

The simplest DC-side buffer topologies regulate either the intermediate voltage, v_m, or current, i_m, to be equivalent to the DC bus — i.e., $i_m = i_{dc}$ or $v_m = v_{dc}$. This design choice reduces the necessary buffer voltage and current states which must be regulated from two states (either i_{dc} or v_{dc}, and either i_m or v_m) to one state. The regulation of one state variable makes for a desirable linear control problem. For example, when a DC-side buffer topology dictates $v_m = v_{dc}$, it is a shunt topology, and when it dictates $i_m = i_{dc}$, it is a series

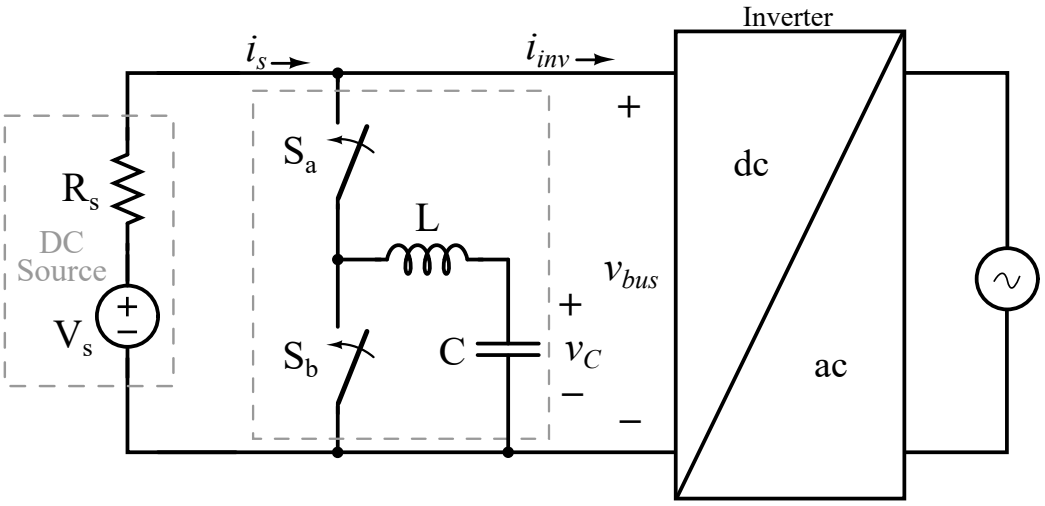


Figure 2.4: Half-bridge or full-ripple port twice-line frequency buffer topology.

topology. The DC-side topology in Fig. 2.4 is an example of a shunt topology where $v_m = v_{dc}$ and thus the intermediate current is defined as

$$i_m = \frac{P_o + P_o \cos(2\omega_L t)}{v_{dc}} \approx i_{dc} + i_{dc} \cos(2\omega_L t) \tag{2.5}$$

by using (2.4) and $v_m = v_{dc}$. The buffer must effectively regulate the current difference between i_{dc} and i_m while keeping the DC bus voltage approximately constant (small-ripple approximation).

The most common passive DC-side buffer is a "DC-link" capacitor placed directly in parallel across the DC bus. In addition, many active types of these "series" or "shunt" DC-side buffer topologies have been explored in literature including the full-bridge buck cell [3, 4], half-bridge buck cell [5], half-bridge boost cell [6, 7], half-bridge split-capacitor cell [8, 9], stacked switched-capacitor cell [10, 11], and series-connected cell [12, 13] amongst others.

2.2.3 Implementation Types

There are, generally speaking, two categories of buffer implementation: dependent (or integrated) and independent. Integrated buffers are integrally dependent on the single-phase converter operation. Both systems must be designed and built tangentially as there is interdependence between com-

ponents. There might for instance be a shared switch or capacitor which provides necessary functionality for both systems. Alternatively, independent buffers should ideally operate independent of the control or topology of the single-phase converter.

It is important to distinguish between topology and operation/implementation. A particular topology, such as the DC-side half-bridge buck cell [5] shown in Fig. 2.4, can have a control implementation which is independent or dependent. In some ways, it is impossible for the active buffer and single-phase converter to remain fully independent as the power pulsation waveform of (2.3) depends on proper DC-AC (or AC-DC) conversion. If the single-phase converter is behaving improperly, then the buffer will in all likelihood fail to completely buffer the ω_{2L} energy, especially if the buffer is active. However, here independent implementation is delineated as buffer operation which does not depend directly on the topology or control of the single-phase power conversion stage.

In this work, Chapter 4 proposes an independent control technique for the SSB but Chapter 5 considers integrating this same SSB control with the control architecture of a single-phase PFC converter to make it dependent. Although the topology remains the same in this case, both buffer implementations (independent and dependent) are shown to operate sufficiently; the use of one implementation over the other depends on the single-phase system implementation.

2.2.4 Further Classification (Resonant Buffers)

There continues, even today, to be great diversity of nomenclature in the discussion of twice-line frequency energy buffers. This is perhaps an indication of the sheer variety of ω_{2L} buffer implementations which can and do exist. Perhaps until an accepted amalgamation of ideas and research appears in a journal review or educational textbook, there will continue to be relatively little coherence within literature. The work in [14] provides an extensive review of existing active buffer topologies and further classifies topology types into categories; this analysis still contains shortcomings and falls markedly short of the aforementioned universally accepted consolidation of designs. It seems evident that worthwhile innovation in fundamental power electronics

design continues to impact the particular specialty or application of twice-line frequency energy buffers.

With relevant justification, this work seeks to introduce and identify, or rather reclassify, *resonant*-type buffer implementations. Resonant behavior has never before been explicitly attributed to the design of twice-line frequency buffers; the intent is to encourage innovation of active buffer topologies and control schemes which are easily derived from desirable behavior of simple passive resonant structures and which share many of the same inherent operating benefits. Although such a classification may appear to only convolute the existing research landscape, the proposals here help to better characterize buffer behavior in some instances and lead to one particularly competitive buffer design called the series-stacked buffer (SSB).

CHAPTER 3

RESONANT-TYPE ACTIVE BUFFERS

This chapter introduces the application of resonant-type behavior to a twice-line frequency buffer topology.

3.1 Application of Time and Frequency Domain

Resonant structures are often used in the design of many electrical circuit applications. Whether filtering signals or shaping the system impedance, resonance behavior is both immensely desirable and uniquely achieved as it controls the distribution of electric charge and, by commutation, instantaneous voltage and current waveforms.

There are two domains utilized to represent waveforms within the discipline of electrical engineering: time and frequency. As the names suggests, the time domain frames a signal as a function of time and the frequency domain as a function of frequency. For a particular problem, either domain can be used to frame, methodize, and understand underlying physical phenomena, and although both are fundamentally equivalent, one might be better suited to designing and implementing a particular solution. Engineering problems which implement resonance can be considered from both domain perspectives as the natural world progresses through time and resonance is a concept of frequency.

To demonstrate versatility, consider the concept of filtering and attenuation in both time and frequency domains for linear time-invariant systems. In the frequency domain, the filtering function can be expressed as input-to-output transfer functions where output signals are simply products of the input signals and the transfer function. If the signal input and transfer function can be quantified as functions of frequency, then determination of the output is straightforward. This is the basis of analog filter design and linear

time-invariant control theory. The time-domain alternative of a product in the frequency domain is a convolution integral, which might be more difficult to compute and visually interpret for specific signals. However, the time domain does give insight into how a filter will shape the instantaneous value of the input. Comparative waveforms such as the step and impulse response and associated metrics of settling time, overshoot, group delay, and phase delay are some of the concepts pertinent to time-domain characterization of a system. Even considering the inherent trade-offs, both domains can be considered mathematical models of real-world phenomenon which distinctively convey the information necessary for engineering design [15].

There is however a difference between steady-state and transient behaviors of a system which precludes the applicability of either time or frequency-domain analysis. In steady-state, signals exhibit periodicity and thus can be composed as a sum of independent sinusoidal signals—the basis of the Fourier series, Fourier transform, and frequency-domain analysis in general. Transient signals are temporary, non-periodic, and can be described as the instantaneous change in a signal as it transitions from one steady-state operating condition to another in the time domain. It is then perfectly natural and reasonable to utilize the frequency-domain to frame the steady-state analysis and the time-domain to frame the transient analysis of electrical system characterization. The analyses in this work are generally approached in this manner, although there are occasions where a time-domain reference frame better conveys the steady-state behavior (and vice versa) as the two domains are mutual and mathematically equivalent.

In the context of DC-side twice-line frequency energy buffers in single-phase power converters, time-domain analysis will be used to holistically determine the ideal behavior of buffer voltages and currents and an appropriate electrical topology, then frequency analysis will be used to characterize buffer impedance. For the extension of active buffers, equivalent converter topologies as well as appropriate control strategies will be derived on the basis of frequency analysis. Finally, the implementation and verification of the buffer operation will be based on the behavior in time. It should be clear from this proposed methodology that the discussion of both time and frequency are heavily integrated and critical to the design process.

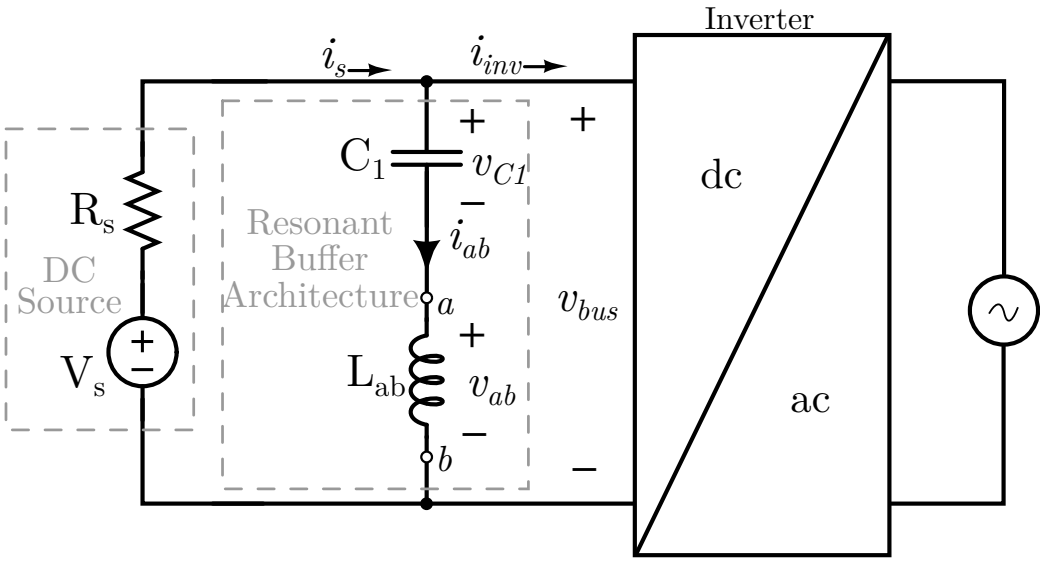


Figure 3.1: A passive series-resonant LC DC-side buffer in a single-phase DC-AC converter.

3.2 Series-Resonant Buffer Topology

Due to its simplicity, the most widespread buffer implementation is a large electrolytic capacitor bank across the DC bus. However, meeting voltage and current ripple specifications often comes at the cost of low power density and limited lifetime due to the large number of electrolytic capacitors necessary [16]. To reduce the required capacitance, series-resonant LC buffers [17], as shown in Fig. 3.1, can be used to achieve perfect voltage ripple cancellation by utilizing resonance at ω_{2L}. For a design where the series capacitance, C_1, and the series inductance, L_{ab}, are chosen to resonate at ω_{2L} according to

$$\omega_{2L} = \frac{1}{\sqrt{C_1 L_{ab}}}, \tag{3.1}$$

the resonant buffer system exhibits the behavior demonstrated by the ideal voltage and current waveforms in Fig. 3.2 and Fig. 3.3, respectively.

However, as the energy density of inductors can be one or two orders of magnitude lower than that of capacitors [18], the added inductor often contributes to a similar or even larger overall volume than the electrolytic capacitor bank solution [19]. There is a clear motivation to further improve the power density of a DC-link capacitor bank, while maintaining similar or better ripple-related performance to the series-resonant LC buffer. This can

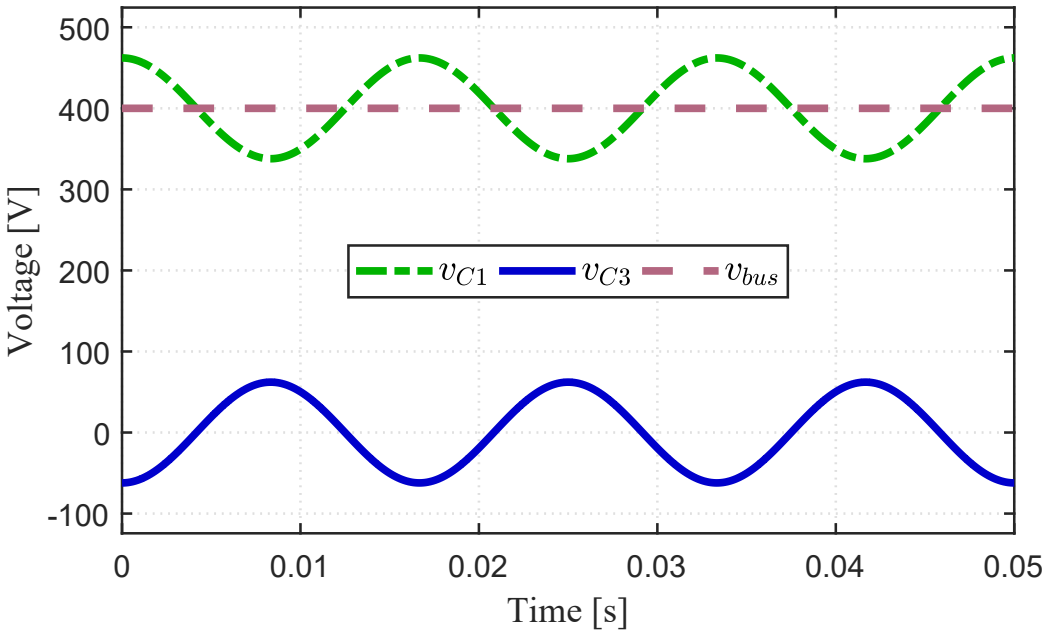


Figure 3.2: Ideal voltage waveforms of a series-resonant LC buffer.

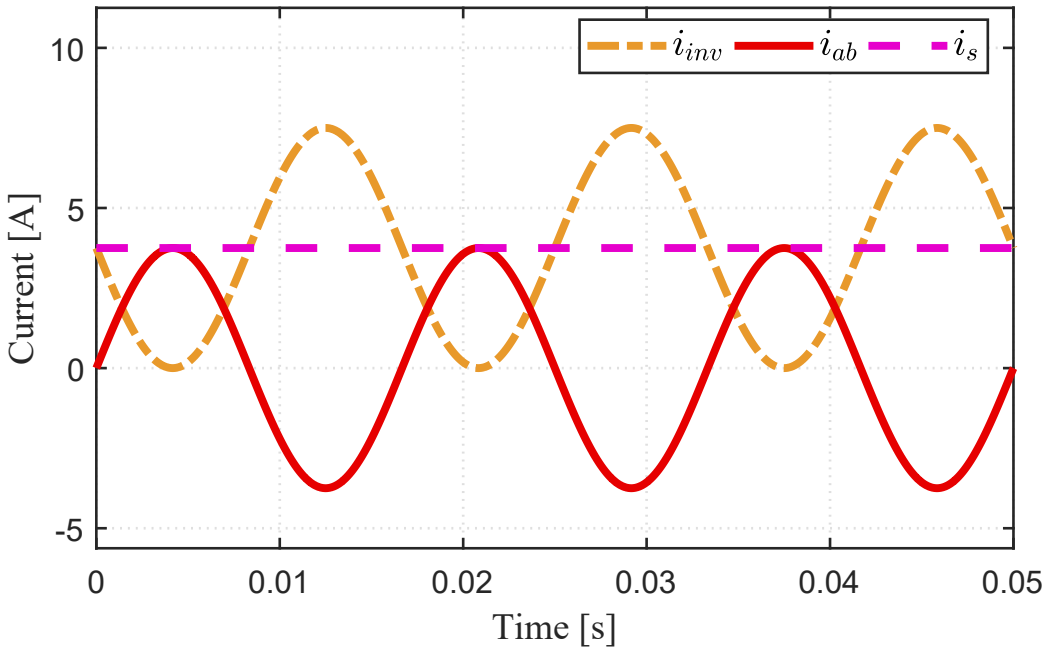


Figure 3.3: Ideal current waveforms of a series-resonant LC buffer.

be accomplished by replacing the inductor in the series-resonant LC buffer with an actively controlled equivalent circuit which has much smaller volume yet exhibits the same inductive terminal characteristics as a physical inductor at ω_{2L}.

An active series-resonant architecture, the series-stacked buffer (SSB), was

demonstrated in [20, 21, 22]. As a continuation, this work presents a generalized impedance model that enables straightforward intuitive analysis and design of this architecture. Unlike the current-controlled method in [20, 21, 22], a voltage-controlled method of the SSB is developed using this generalized approach to illustrate its versatility. The validity of this model has been experimentally demonstrated with a hardware prototype.

CHAPTER 4

IMPEDANCE MODELING AND CONTROL DERIVATION

In this chapter, the passive series-resonant LC buffer is first analyzed and a corresponding impedance model is developed with and without power loss. The active SSB architecture is directly correlated to the passive impedance model and a proper voltage-control regulation method is proposed.

4.1 Passive Series-Resonant LC Buffer

Figure 4.1 shows the equivalent impedance model of the series-resonant LC buffer illustrated in Fig. 3.1, where Z_{C1} and Z_{ab} are the impedance of the capacitor and inductor, respectively. The DC source is represented as a Thevenin equivalent model with voltage, V_s, and source resistance, R_s. Assuming that v_{bus} is constant in steady-state, the inverter can be modeled as a sinusoidal current source with DC offset, i.e.,

$$i_{inv} = i_{inv,DC} + i_{inv,AC} = I_s - I_s sin(\omega_{2L} t), \tag{4.1}$$

as discussed in [22]. Note that i_{inv} consists of a DC component ($i_{inv,DC}$) and an AC component ($i_{inv,AC}$) with frequency ω_{2L}. Superposition of the ideal sources can be applied in this circuit model such that the required total buffer impedance, Z_{buf}, can be considered at DC and at ω_{2L} independently.

In most cases, the passive series-resonant LC buffer is designed to resonate at ω_{2L}. As a result, (1) the total equivalent buffer impedance, $Z_{buf} = Z_{C1} + Z_{ab}$, is an open circuit ($Z_{buf} = \infty$) at DC due to the series connection of the capacitor, and is a short circuit ($Z_{buf} = 0$) at its resonant frequency, ω_{2L}; (2) all of the twice-line frequency ripple current thus flows strictly through the resonant buffer branch and not through the DC source (i.e., $i_{ab} = i_{inv,AC}$ and $i_s = i_{inv,DC}$); (3) the bus voltage, $v_{bus} = V_{bus}$ is a constant DC value with no ripple; (4) the buffer branch components have equal reactance (i.e.,

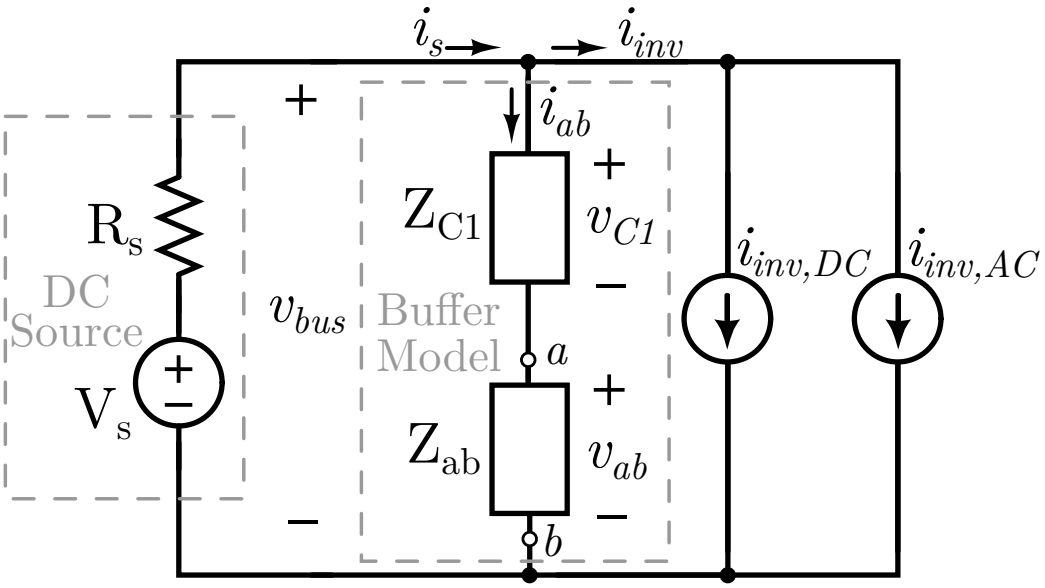


Figure 4.1: The equivalent circuit model of a series-resonant LC DC-side buffer.

$X_{C1} = X_{ab}$). These relationships defined in terms of impedance, current, voltage and reactance are equivalent, and satisfying any one of them implies conditions are met for the buffer branch to resonate at ω_{2L}. The AC components of currents and voltages at ω_{2L} can be expressed in phasor notation by denoting each symbol with an overtilde (e.g., $\widetilde{I}_{inv} = i_{inv,AC} = -I_s sin(\omega_{2L}t)$). The aforementioned relationships between buffer component voltages and currents during resonance can be shown analytically in (4.2) - (4.4) and expressed graphically in Fig. 4.2a as a phasor portrait.

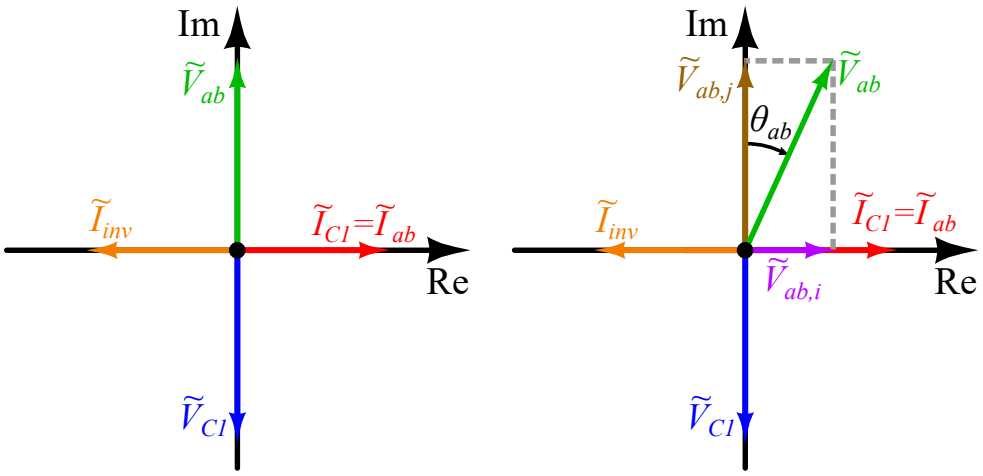
$$\widetilde{I}_s = \widetilde{I}_{inv} + \widetilde{I}_{ab} = 0 \tag{4.2}$$

$$\widetilde{V}_{bus} = \widetilde{V}_{ab} + \widetilde{V}_{C1} = 0 \tag{4.3}$$

$$-j\frac{1}{X_{ab}}\widetilde{V}_{ab} = \widetilde{I}_{ab} = \widetilde{I}_{C1} = j\frac{1}{X_{C1}}\widetilde{V}_{C1} \tag{4.4}$$

4.2 Series-Stacked Buffer (Active Series-Resonant LC Buffer)

Although the overall buffer impedance, Z_{buf}, could be implemented entirely with a single active converter such as in [3, 8, 23, 24, 25, 26, 27, 28, 29], these converters typically exhibit relatively low power density and efficiency due



(a) $R_{ab} = 0$ (b) $R_{ab} \neq 0$.

Figure 4.2: Phasor portrait for buffer impedance model at resonance.

to high voltage and current stresses at the full system power rating. A more detailed analysis can be found in [22].

An alternative is to replace certain passive resonant components with an active converter. This arrangement maintains some natural impedance relationships due to the passive component while still emulating overall resonance behavior through regulation of the active component. As an example, the power density of the passive series-resonant LC buffer is often limited by the inductor, and it is natural to explore the concept of replacing the inductor with a smaller, equally efficient, and actively controlled converter as shown in Fig. 4.3. As long as the terminal characteristics of ab are identical to the passive inductor implementation at ω_{2L}, the same overall power decoupling performance of the system can be achieved. This is the fundamental motivation of the SSB architecture proposed in [20, 21, 22].

The buffer converter between terminals a and b in Fig. 4.3 can be implemented with a full-bridge DC-AC topology as shown in Fig. 4.4. Either the output current or voltage of this converter can be regulated to produce a twice-line frequency component to satisfy (4.2) and (4.3). For example, the terminal voltage of ab can be controlled such that $v_{ab} = -v_{C1,ac}$ in accordance with (4.3); this implementation method is denoted as voltage control. Equivalently, the terminal current of ab can be controlled such that $i_{ab} = -i_{inv,ac}$ in accordance with (4.2); this implementation method is denoted as current control. In the ideal case with no power loss in the buffer, the circuit behaves

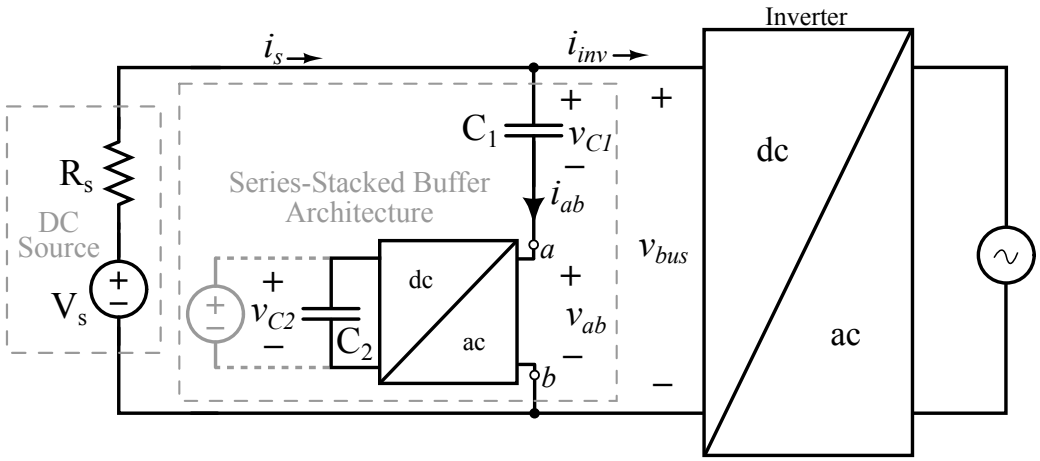


Figure 4.3: SSB architecture where the DC-AC buffer converter functions as the active inductor, L_{ab}, in the series-resonant LC buffer architecture.

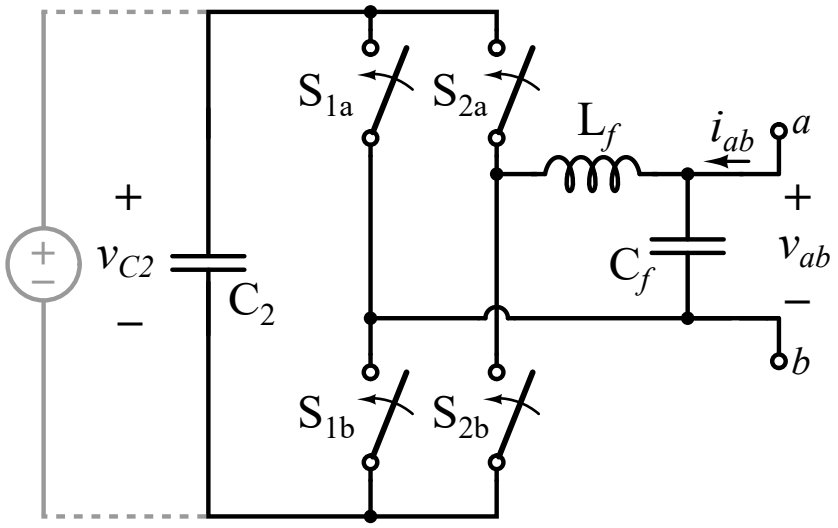


Figure 4.4: Full-bridge buck implementation of DC-AC buffer converter. L_f and C_f are relatively small switching frequency filter components.

exactly like a series-resonant LC buffer at ω_{2L}, with either current or voltage control. Note that the apparent power processed by the buffer converter, $\widetilde{S}_{ab}$, is purely reactive, i.e., $\widetilde{S}_{ab} = \widetilde{V}_{ab}\widetilde{I}^*_{ab} = jQ_{ab}$, since the buffer converter is emulating the behavior of an ideal inductor. As a result, the active source shown on the DC side (i.e., higher voltage side) of the DC-AC buffer converter in Fig. 4.3 and 4.4 is not necessary and an energy storage capacitor C_2 suffices to support the DC-side voltage, v_{C2}, and in turn the necessary terminal voltage, v_{ab}. Experimental verification of both voltage and current control schemes for the SSB architecture have been shown in [30] and [22],

respectively.

4.3 Modeling of Power Loss Compensation

The described twice-line frequency buffer should process only reactive power if it is emulating a purely resonant impedance (i.e., without loss), and for this case, no real (non-reactive) power will flow into terminals a and b. However, any practical implementation of the buffer converter does incur power loss and must be considered. All real power absorbed by the buffer contributes to loss, which will drain the energy stored in C_2, diminish v_{C2}, and disrupt the active decoupling operation proposed. To maintain v_{C2}, power loss must be fully compensated by allowing real power to flow into terminals a and b. This goal can be achieved through an extension in the lossless model of the DC-AC buffer converter in Fig. 4.3.

To derive a suitable loss compensation method, start by considering a practical passive series-resonant LC buffer where the ideal model of L_{ab} in Fig. 3.1 includes a small series resistor R_{ab} representing the parasitic resistance of a physical inductor as shown in Fig. 4.5. The total impedance of the buffer branch then becomes

$$Z_{buf} = Z_{C1} + Z_{ab} = -jX_{C1} + jX_{ab} + R_{ab}. \tag{4.5}$$

The resonance characteristics of Z_{buf} at ω_{2L} (i.e., $X_{ab} = X_{C1}$ and $R_{ab} \ll X_{ab}$) are still desired to absorb the ripple current and minimize the DC bus voltage ripple. These conditions ensure the resonant circuit is "high-Q", and the fundamental assumption, $v_{bus} \approx V_{bus}$, keeps the proposed impedance model of Fig. 4.3 and the sinusoidal relationship of i_{inv} defined by (4.1) accurate.

If $R_{ab} = 0$, the buffer appears as an open circuit at DC and short circuit at ω_{2L}, so no real power can flow into it. The case of $R_{ab} > 0$ induces some real power flow into the buffer as the buffer branch is no longer a short circuit at ω_{2L}, and the power flow changes according to R_{ab}. This observation suggests that instead of emulating a pure inductor across terminals a and b, the buffer converter should emulate a series RL circuit to allow power flow into this terminal. The emulated resistance can be adjusted through proper control to balance the real power drawn due to practical power loss of the

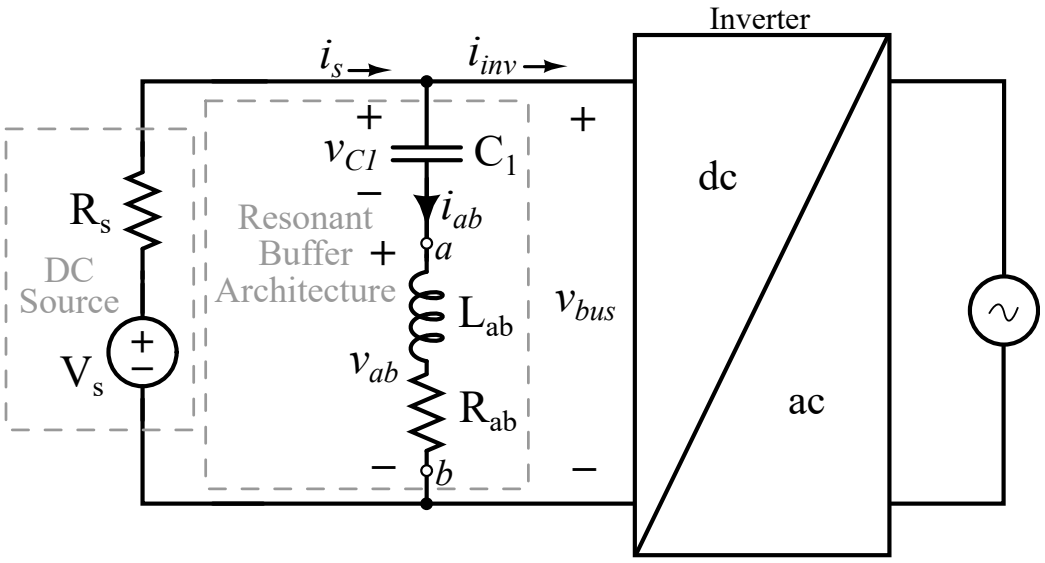


Figure 4.5: A lossy series-resonant LC DC-side buffer in a single-phase DC-AC converter.

buffer converter. In other words, to compensate for the real power loss in the buffer branch, either $\widetilde{V}_{ab}$ or $\widetilde{I}_{ab}$ should be regulated so that the complex power, i.e.,

$$\widetilde{S}_{ab} = \widetilde{V}_{ab}\widetilde{I}^{*}_{ab} = P_{ab} + jQ_{ab}, \tag{4.6}$$

has both a real and reactive part.

The comprehensive current and voltage relationships for this lossy model are derived from Kirchhoff's voltage and current laws

$$\widetilde{I}_s = \widetilde{I}_{inv} + \widetilde{I}_{ab} = \frac{R_{ab}}{R_s + R_{ab}}\widetilde{I}_{inv} \tag{4.7}$$

$$\widetilde{V}_{bus} = \widetilde{V}_{ab} + \widetilde{V}_{C1}. \tag{4.8}$$

With the intent of a voltage-control derivation, the terminal phasor voltage, $\widetilde{V}_{ab}$, is decomposed into the sum of two orthogonal vectors, $\widetilde{V}_{ab,i}$ and $\widetilde{V}_{ab,j}$,

$$\widetilde{V}_{ab} = \widetilde{V}_{ab,i} + \widetilde{V}_{ab,j} = |\widetilde{V}_{ab}|e^{j(\frac{\pi}{2}-\theta_{ab})}, \tag{4.9}$$

where

$$\widetilde{V}_{ab,j} = -\widetilde{V}_{C1} \tag{4.10}$$

$$\widetilde{V}_{ab,i} = R_{ab}\widetilde{I}_{ab} = \beta\frac{d}{dt}\widetilde{V}_{C1} = \beta(j\omega_{2L})\widetilde{V}_{C1} \tag{4.11}$$

and the proportional term β is defined as $\beta = R_{ab}C_1$. The relationships in both (4.10) and (4.11) can be derived directly from the full buffer impedance expression in (4.5). By substituting (4.9) - (4.11) into (4.8), the bus voltage phasor with loss compensation can be simplified to

$$\widetilde{V}_{bus} = \widetilde{V}_{ab,i} = R_{ab}\widetilde{I}_{ab}. \tag{4.12}$$

Similarly to Fig. 4.2a for the case without power loss, the expressions in (4.7) - (4.11) are expressed graphically in Fig. 4.2b as a phasor portrait. In summary, an additional component of $\widetilde{V}_{ab}$ in phase with $\widetilde{I}_{ab}$, denoted as $\widetilde{V}_{ab,i}$, incorporated in the active buffer control scheme will provide the necessary real power component in the buffer for loss compensation.

To better understand the implications of emulated R_{ab} in the preceding series-resonant LC buffer voltage/current relationships, the fundamental limitations of the system are discussed. The source resistance, R_s, is essential to defining the maximum emulated R_{ab}. Using the maximum power transfer theorem, it is clear that maximum power transfer to Z_{buf} occurs when $R_{ab} = R_s$. Applications with a greater R_s allow a larger viable controllable range of R_{ab} when compensating loss. Assume the total buffer power loss is represented by P_{loss} for a specific system load. If P_{loss} is greater than the maximum power which can be transferred to the buffer, denoted by $P_{ab,max} = I_{ab,rms}^2 R_{ab} = I_{ab,rms}^2 R_s$, then the buffer cannot be fully compensated at those operating conditions and buffer performance may suffer. Larger values of R_{ab} also draw more real power away from the primary source-to-load power flow path in a full system and increase the voltage and current ripple on the DC bus. These symptoms deteriorate the system efficiency of the overall inverter or rectifier. The optimal operating solution is minimal power loss in the buffer branch so that the R_{ab} necessary to compensate this loss is minimized.

4.4 Control Design

An implementation of the voltage-controlled method with loss compensation has been developed as illustrated in Fig. 4.6. A similar voltage-controlled method was demonstrated in [30]. The discussion here provides a clear,

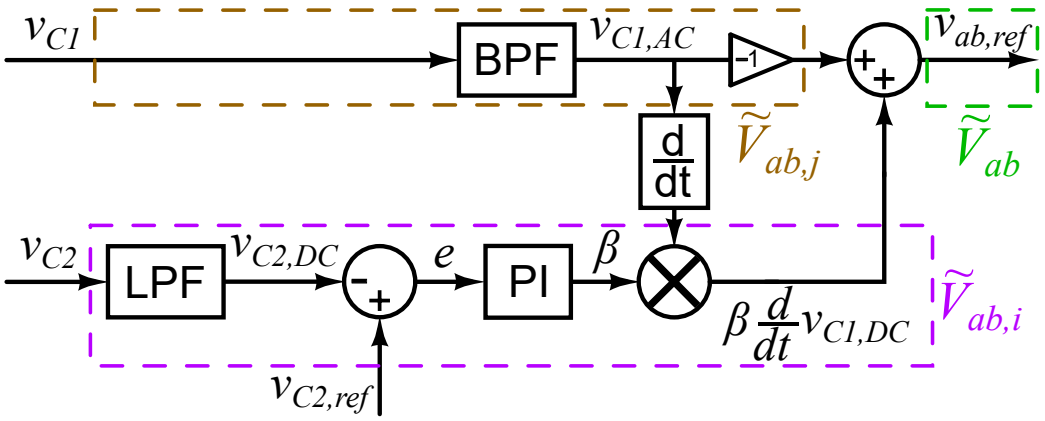


Figure 4.6: Voltage-control architecture of SSB. Assuming the actual voltage $\widetilde{V}_{ab}$ follows the reference $v_{ab,ref}$ closely, $\widetilde{V}_{ab,j}$ is generated from the primary control path and $\widetilde{V}_{ab,i}$ is generated from the loss compensation path.

formal derivation of the control using the developed equivalent impedance model. In this control architecture, a reference voltage $v_{ab,ref}$ for the active buffer converter is generated according the analysis in Section 4.3, and then executed by the buffer converter through open-loop or closed-loop converter control to generate a voltage across terminals a and b. The terminal voltage phasor, $\widetilde{V}_{ab}$, is decomposed into the sum of $\widetilde{V}_{ab,i}$ and $\widetilde{V}_{ab,j}$ as shown in (4.9). Assuming the actual voltage follows the reference closely, $\widetilde{V}_{ab,j}$ is generated from the primary control path and $\widetilde{V}_{ab,i}$ is generated from the loss compensation path as shown in Fig. 4.6.

The primary control path performs the primary twice-line-frequency power pulsation decoupling function and is responsible for most of the overall control effort in $v_{ab,ref}$. This control path extracts the ω_{2L} voltage ripple on C_1 and generates a negated signal as dictated by (4.10) to minimize the voltage ripple on v_{bus}. To accurately extract its ω_{2L} component, v_{c1} must be measured and filtered. This implementation uses a band-pass filter (BPF) with transfer function $G_{BPF}(s) = 1 - G_{notch}(s)$ where $G_{notch}(s)$ is a high-Q second-order notch filter.

The loss compensation control path is responsible for adjusting the phase of $v_{ab,ref}$ to compensate for practical losses in the active buffer. From the phasor relationship of (4.11), $\widetilde{V}_{ab,i}$ is recognized to be in phase with the instantaneous derivative of $\widetilde{V}_{C1}$. There are two elements to this control path: a feed-forward derivative of $v_{C1,ac}$ and a proportional coefficient, β. The deriva-

tive term is implemented with a band-limited differentiator applied to $v_{C1,ac}$. The proportional term, β, is implemented with a feedback control loop and its magnitude regulates the capacitor voltage, v_{C2}. An error term, e, is generated by calculating the instantaneous difference between a desired reference voltage, $v_{C2,ref}$, and the low-frequency filtered measurement, $v_{C2,DC}$. This error term is then passed through a proportional-integral controller to properly regulate $v_{C2,DC}$ to $v_{C2,ref}$. Although it does not measure the converter power loss directly, this method of actively determining β (i.e., the power loss compensation coefficient) using closed-loop feedback of v_{C2} is viable because without active loss compensation the natural decay of v_{C2} is a strong indicator of power loss in the buffer converter.

The overall control effort, $v_{ab,ref}$, is formed by the combined sum of the primary and loss compensation control paths. The computed signal $v_{ab,ref}$ can use open-loop or closed-loop regulation to generate a conversion ratio, M, and an equivalent duty cycle, D, for PWM regulation. In open-loop control, the conversion ratio is derived with one of two formulae: $M = v_{ab,ref}/v_{C2,ref}$ or $M = v_{ab,ref}/v_{C2}$. The former formula, although easier to implement and linear, comes with distinct demerits. During transients $v_{C2} \neq v_{C2,ref}$, so the output v_{ab} will tend to oversaturate (i.e., peak $v_{ab,ref} > v_{C2}$) and during steady-state, the inherent ripple on v_{C2} will propagate directly to v_{ab}. Both effects noticeably distort v_{bus} and increase voltage ripple. The latter formula, although non-linear, is a better alternative as it circumvents both aforementioned issues. Experimental verification of the hardware prototype utilizes open-loop control with the latter, nonlinear, formula.

The reference voltage, $v_{C2,ref}$, can be defined statically, as a discrete predetermined value, or dynamically, as a function of the system load. The dynamic method sets $v_{C2,ref}$ to a value always slightly larger than the measured peak of $v_{C1,AC}$. Using this method, switching losses in the buffer converter can be minimized by minimizing the switch voltage stress (i.e., v_{C2}) applied to the converter. One implementation of the dynamic scheme can be found in [22].

This discussion uses the series-resonant LC buffer to develop an equivalent impedance model and establish basic circuit behavior and foundational control derivation of an analogous active buffer. However, generalization of this LC resonant impedance model for all non-ω_{2L} frequencies is an incorrect application of the prescribed method. The choice of band-pass filter in the

primary control path critically impacts the impedance behavior of the buffer, Z_{buf}, at non-ω_{2L} frequencies—a versatility not available in a passive series-resonant LC buffer. For example, multiple notches in the band-pass filter generate resonant impedance buffer behavior at each notch frequency, a useful method for harmonic suppression. Another example might instead use a high-pass filter to increase the effective capacitance of the active buffer at frequencies above ω_{2L} for improving the overall transient response as described in [30]. Although there are merits in using other filter types (e.g., high-pass and other band-pass variations), a high-Q notch-type response at ω_{2L} is required to ensure proper buffer behavior ($Z_{buf} \approx 0$) for the primary signal component. Other transient considerations include phase delay through the notch filter (ideally none) and minimizing group delay to improve transient response.

Note that even though it is more straightforward to consider the regulation of the terminal voltage, $\widetilde{V}_{ab}$, as the vector sum of two orthogonal vectors, it can also be characterized as a vector exponential with magnitude $|\widetilde{V}_{ab}|$ and angle θ_{ab} as shown in (4.9). The benefit of this outlook is that the loss compensation control could, without an explicit additional term $\widetilde{V}_{ab,i}$ generated by noise-prone differentiation, instead be implemented with a phase delay of $\widetilde{V}_{ab,j}$ for small values of θ_{ab}. Comparison and experimental verification of this alternative control method is not within the scope of this work but will be explored in future work.

4.5 Experimental Validation

For experimental verification of the analysis and control design of the SSB, the hardware prototype shown in Fig's. 4.7 and 4.8 is built with the specifications shown in Table 4.1. The associated PCB schematic and layout can be found in Appendix A. The control is implemented digitally using a Texas Instruments C2000 DSP, capacitors C_1 and C_2 are of the metal film type, and the full-bridge buffer converter is implemented with two Texas Instruments LMG5200 integrated GaN half-bridges. A list of all the key components can be found in Table 4.2.

Special consideration must be made when determining the capacitance of C_1 and C_2 so that the overall buffer operates effectively and yet maintains

Table 4.1: SSB design specifications.

V_s	437.5 Vdc
P_o	1.5 kW
R_s	10 Ω
f_{sw}	160 kHz

the prescribed benefits of minimized capacitor volume. Capacitor C_1 is sized utilizing the same method for a DC-link capacitive buffer solution; however, since the voltage ripple magnitudes ΔV_{C1} and ΔV_{bus} are decoupled in the SSB, ΔV_{C1} should be sized according to the maximum allowable voltage rating across terminals a and b (i.e., the buffer converter).

For this implementation, the LMG5200 voltage rating is 80 V and the corresponding C_1 chosen to meet this specification is 80 μF. The fundamental constraining equations of C_2 are derived in [31]; however, it is clear from inspection a larger C_2 minimizes the ripple on v_{C2}—a value assumed to be approximately constant in steady-state. However, making C_2 too large would counteract the volumetric benefits of the active SSB buffer solution. Utilizing the derivations in [31], C_2 can be as small as about 70 μF for this SSB design while still maintaining correct operation; however, C_2 is chosen to be a conservative 204 μF to adequately fulfill the constant voltage assumption of v_{C2} and validate the basic impedance control strategy proposed.

For the full-bridge buck converter, the switching frequency is $f_s = 160$ kHz and the corresponding filter components at its output are $L_f = 94$ μH and $C_f = 2.2$ μF, both of which are conservative values and might be further optimized for smaller overall volume.

The experimental setup is illustrated in Fig. 4.9 where V_s is a DC voltage supply, R_s is a 10 Ω power resistor rated well above full power, and the inverter load is implemented with a programmable electronic DC load drawing an ω_{2L} sinusoidal current with DC offset as defined by (4.1).

The operating waveforms of the SSB prototype with the aforementioned voltage control are shown for $V_{bus} = 400$ V and $P_o = 1.5$ kW (full power) in Fig. 4.10. The measurements shown in the figure indicate that v_{ab} and v_{C1} exhibit large voltage ripple due to the AC power pulsation, while they are 179° (i.e. $\theta_{ab} \approx 1°$) out of phase and almost equal in magnitude, resembling behavior identical to a lossy passive series-resonant LC buffer. At full power,

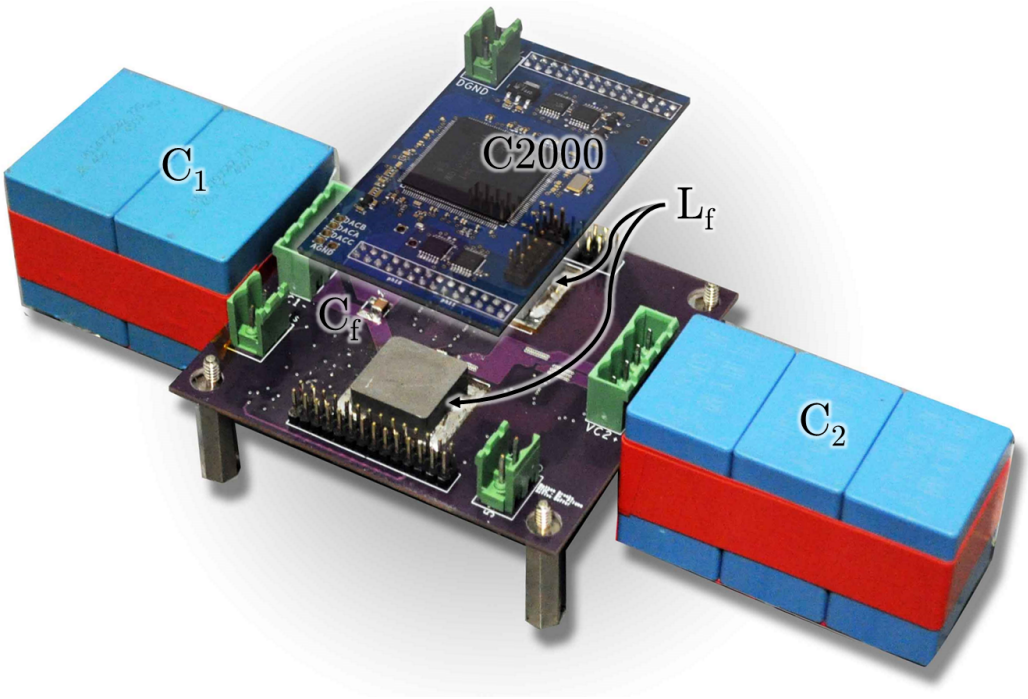


Figure 4.7: Full SSB hardware prototype consisting of a power stage PCB, a control PCB, and energy storage capacitors.

the peak-to-peak voltage ripple on V_{bus} is found to be 7 V (i.e., $\approx 1.8\%$) as a result of the loss compensation scheme. To achieve the same ripple specification with a DC-link capacitor bank solution would require approximately 1.4 mF as shown by

$$C_{DC-link} = \frac{P_o}{\omega_{2L} \Delta v_{bus,p-p} V_{bus}} \tag{4.13}$$

derived in [22]. A capacitor of this size rated for the 400 V bus voltage would be noticeably larger than the proposed active SSB solution. Note that v_{ab} is not exactly 180° out of phase to v_{C1}, suggesting that the power loss compensation mechanism is working and the voltage on C_2 is indeed regulated as shown in Fig. 4.10.

The described system is also able to properly regulate with moderate load step transients. For example, an increase in load induces a larger voltage ripple on v_{C1} and consequently a larger v_{C2} must be regulated with the loss compensation control path. This allows v_{ab} to quickly match $-v_{C1,ac}$ and ensure proper steady-state operation at the new load operating point. As shown in Fig. 4.11, a load step of 50% (750 W) to 100% (1500 W) exhibits a

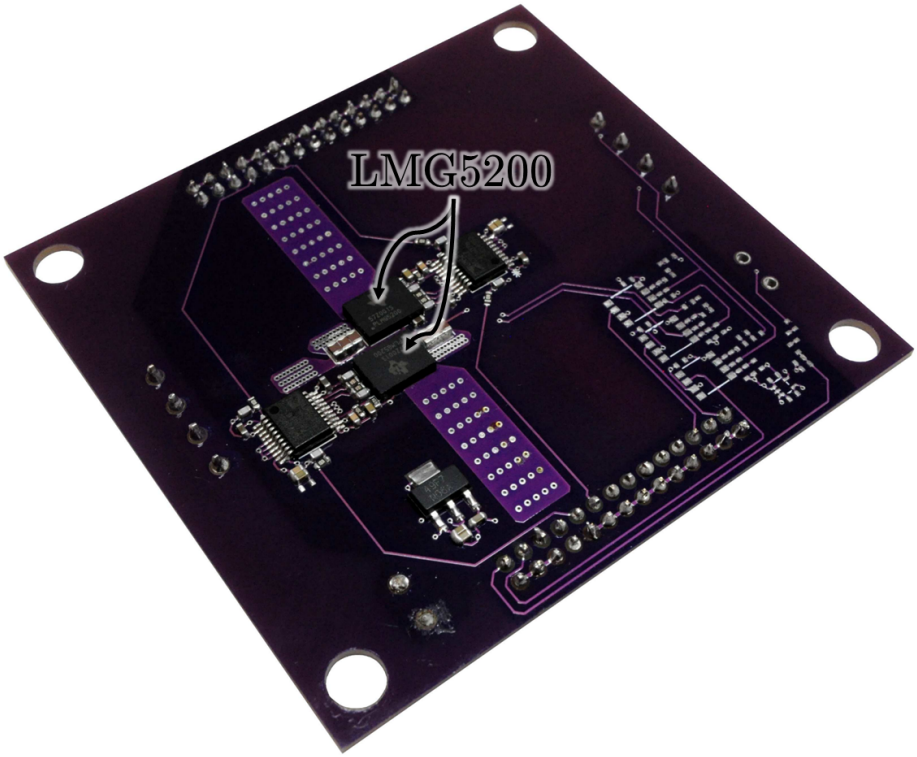


Figure 4.8: Bottom side of the power stage PCB. The buffer converter switches are implemented with two TI LMG5200 GaN half-bridge modules.

stable transient response and it takes v_{bus} about 5 to 6 twice-line frequency cycles to reach its steady-state value.

The buffer converter portion of the SSB processes a fraction of the full rated system power (about an eighth as shown in [22]) and the expected consequence is very high buffer efficiency. A single power meter, configured as shown in Fig. 4.9, measures i_{buf} and v_{bus}, and integrates the net buffer power for a specified duration and accumulates the total energy. Efficiency for a single load operating point can be calculated using the ratio of accumulated output to input energy of the buffer. Using this technique, measured results of the hardware prototype show high efficiency over the full load range as shown in Fig. 4.12. As another point of comparison, the measured absolute loss of the full SBB, is shown in Fig. 4.13.

Table 4.2: Component listing of the demonstrated SSB hardware prototype.

Component	Manufacturer & Part number	Parameters
S_{1a}, S_{1b} & S_{2a}, S_{2b}	Texas Instruments LMG5200	80 V, 15 mΩ, 10 A
C_1	TDK B32776G4406K × 2	40 μF, 450 V
C_2	TDK B32524Q1686K × 3	68 μF, 100 V
C_f	TDK C3216X7S2A225K160AB × 1	2.2 μF, 100 V
L_f	Vishay IHLP6767GZER470M11 × 2	47 μH, 8.6 A
Power & Signal Iso.	Analog Devices ADUM5210	
Logic Level-Shifter	Texas Instruments SN74LV4T125PWR	
Microcontroller	Texas Instruments TMX320F28377D	
Diff. Voltage Amp.	Linear Technology LT1990	

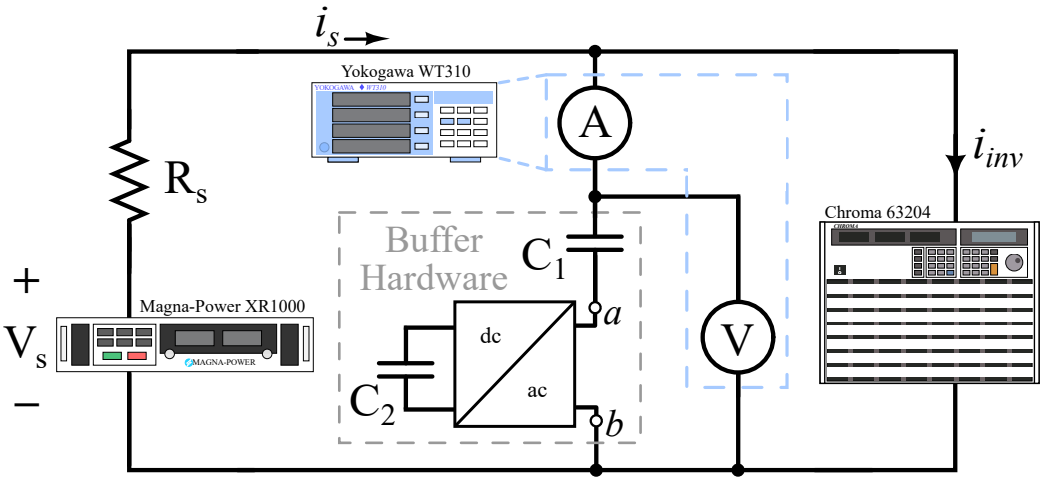


Figure 4.9: Experimental measurement setup.

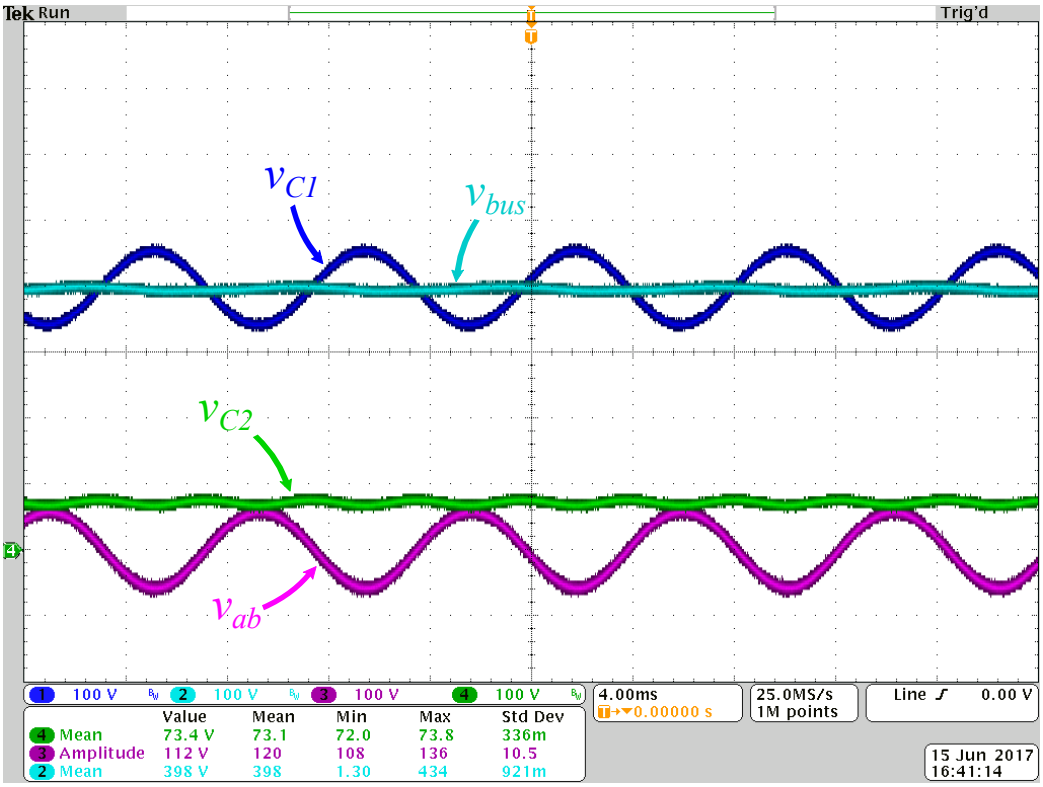


Figure 4.10: Voltage waveforms demonstrating the operation of the buffer converter with loss compensation at full rated power (1.5 kW).

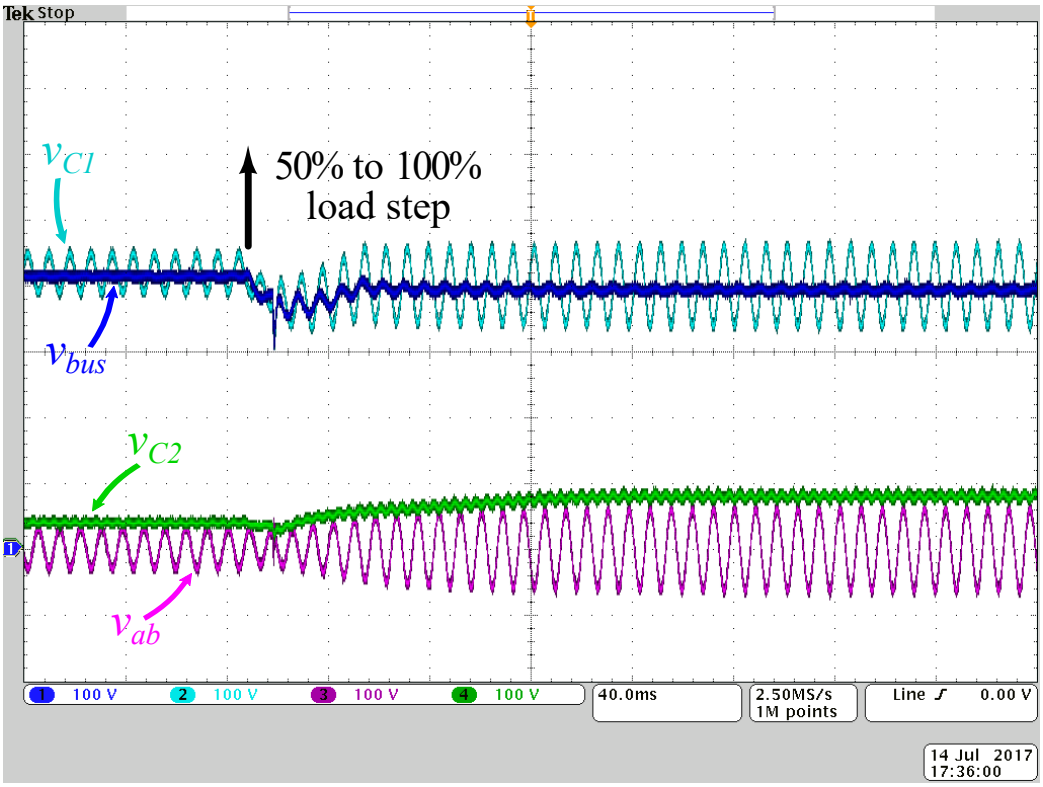


Figure 4.11: Voltage waveforms during a 50% to 100% load step transient.

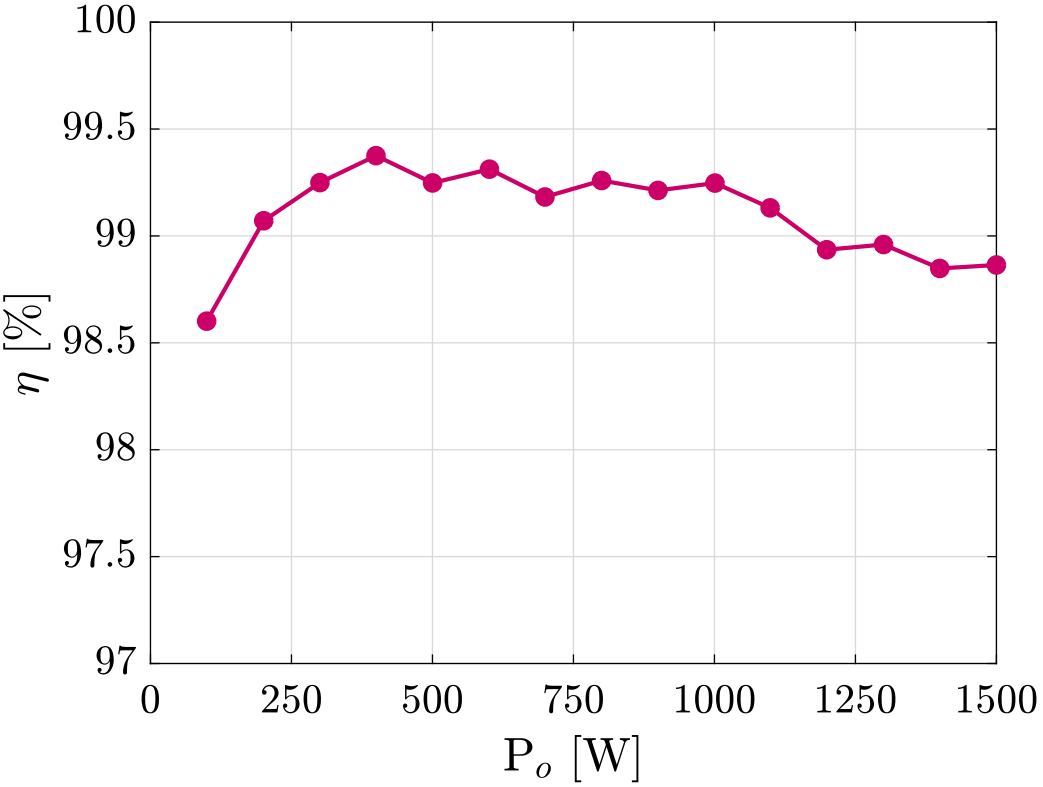


Figure 4.12: Measured SSB efficiency over the full system load range.

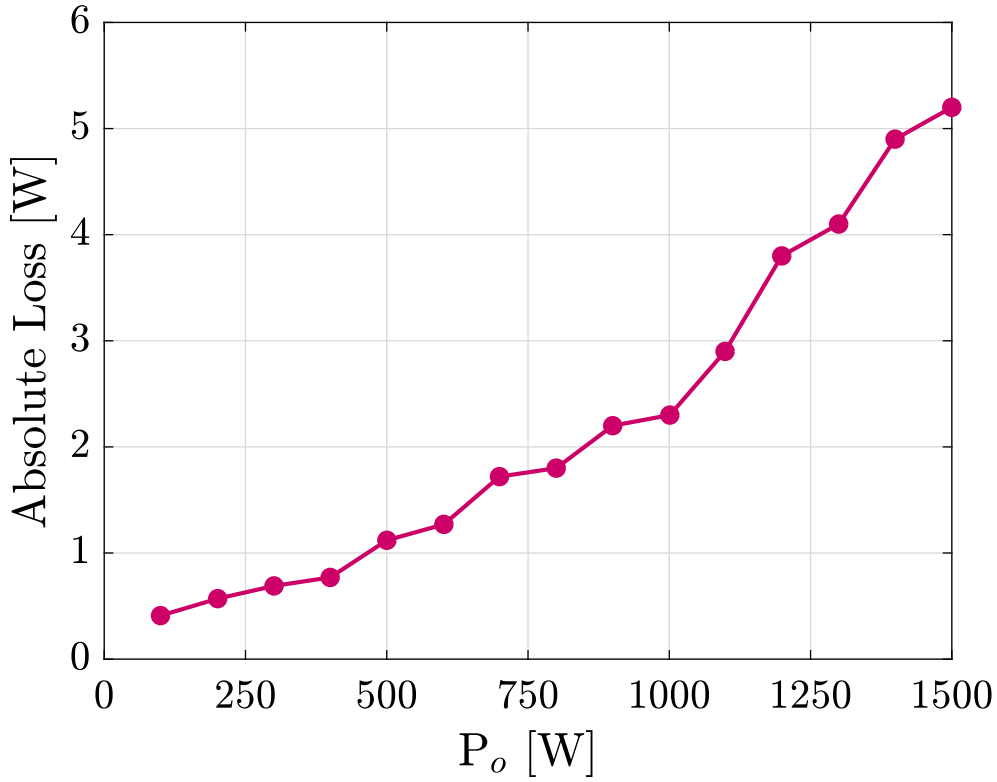


Figure 4.13: Measured SSB absolute loss over the full system load range.

CHAPTER 5

INTEGRATION OF ACTIVE BUFFER AND PFC SINGLE-PHASE RECTIFIER

This chapter seeks to verify the robustness of an SSB twice-line frequency energy buffer for a boost FCML PFC converter with relatively stringent design considerations by validating system-level operation of a single-phase PFC converter with simultaneous high power density and efficiency. Compared to more conventional boost-type PFC designs which necessitate a larger boost inductor, the FCML boost PFC has a naturally smaller inductor requirement which poses unique challenges in achieving adequate control bandwidth, gain margin, and phase margin in closed-loop regulation, especially for a universal AC input [32]. By exhibiting the SSB's and PFC's capability to maintain stability for highly variable system requirements, SSB integration can be made more generalizable to other single-phase conversion systems.

Single-phase power factor correction (PFC) rectifiers are often used in grid-tied ac-dc applications to improve the power conversion quality and efficiency. Conventional front-end PFC designs operate a boost converter to rectify and step-up the AC input voltage to a DC output [33, 34, 35]. A fundamental limitation to achieving high power density in these systems is the twice-line frequency energy ripple. A large DC-link capacitance is often utilized to minimize the ripple on the DC bus; however, this solution dominates the system volume and limits system lifetime [16]. An alternative to the DC-link capacitor passive buffering solution are active buffers which minimize volume by uniquely processing the ω_{2L} power pulsation. The series-stacked buffer (SSB) topology considered in Chapter 4 is a particularly promising active buffer which provides simultaneously high efficiency and power density through the use of partial power processing in the active switching components [36, 37, 38].

Previous SSB implementation lacks an aptly defined methodology for incorporation with a PFC rectifier front-end. However, with continued improvement in the processing and functionality of microcontrollers and FP-

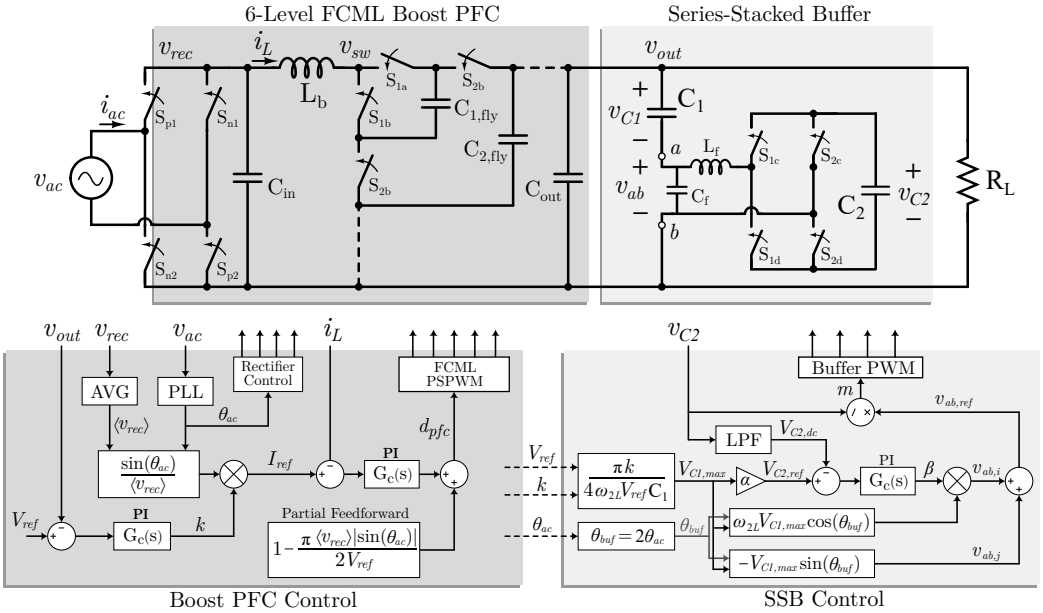


Figure 5.1: System level schematic of 6-level FCML boost PFC front-end and SSB. Includes proposed integrated SSB voltage-control architecture for improved system stability.

GAs, full system integration of the PFC front-end and active buffer subsystems becomes increasingly viable. This chapter proposes a PLL (phase-locked loop) based digital control method of the SSB for use in an FCML (flying capacitor multilevel) boost PFC front-end as shown in Fig. 5.1, which can be generalized to other single-phase systems. Furthermore, by integrating the SSB control with the control architecture of the PFC front-end, stability between these two non-linear systems can be ensured.

5.1 Impedance Modeling of Series-Stacked Buffer

Previous literature has derived the equivalent impedance of the series-stacked buffer (SSB) both at the primary frequency of interest, ω_{2L}, and at other non-ω_{2L} frequencies, but these works have limitations [37, 38]. In the former case, the series-resonant LC equivalent impedance model presented in [38] and Chapter 4 lacks explanation of the external impact of the SSB on single-phase converter design. The model is only valid at precisely ω_{2L} and thus should only be used as a tool for generalizing intended resonant behavior, developing appropriate impedance-control techniques, and understanding the

mechanisms of power loss in converters for twice-line frequency ripple buffering applications.

Works such as [37] characterize the non-ω_{2L} impedance behavior of the SSB and propose a self-powered architecture in an effort to make product integration with the single-phase system more independent; however, additional clarification is necessary to understand the quantitative impact of this impedance behavior on system design.

This work aims to present a design methodology to effectively utilize the SSB in practical systems such as grid-tied inverters or PFC rectifiers. As the SSB is essentially a two-terminal device, accurately modeling its equivalent impedance frequency response offers a tractable and direct incorporation of the buffer dynamics into conventional small-signal modeling and closed-loop controller design of the PFC front-end. In addition, developing a comprehensive impedance model is valuable to an analytical discussion of steady-state and transient stability between the front-end and buffering converter systems. This analysis relies on a linearized frequency-domain representation of the control architecture of the SSB to define its impedance behavior.

Utilizing the voltage-control method derived in Chapter 4 and shown in Fig. 4.6, the small-signal control dynamics of the SSB can be derived as

$$\begin{aligned} v_{ab,ref}(s) &= v_{ab,j}(s) + v_{ab,i}(s) \\ &= -G_{bpf}(s)\ v_{C1}(s) + \beta\ G_d(s)\ G_{bpf}(s)\ v_{C1}(s) \end{aligned} \tag{5.1}$$

where $G_{bpf}(s)$ is a second-order peak or high-Q band-pass filter, $G_d(s)$ is a band-limited differentiator, β is regulated with feedback and is a function of the power loss in the buffer, and v_{C1} is the measured voltage of capacitor C_1. The band-pass filter $G_{bpf}(s)$ can be implemented to extract only the w_{2L} ripple component of v_{C1}, and one straightforward implementation is the inversion of a second-order notch filter, $G_n(s)$.

$$G_{bpf}(s) = 1 - G_n(s) = 1 - \frac{s^2 + \omega_{2L}}{s^2 + \frac{\omega_{2L}}{Q}s + \omega_{2L}^2} = \frac{\frac{\omega_{2L}}{Q}s}{s^2 + \frac{\omega_{2L}}{Q}s + \omega_{2L}^2} \tag{5.2}$$

Assuming proper buffer converter design, appropriate sizing of L_f and C_f for CCM (continuous conduction mode), and the division of $v_{ab,ref}$ by measured v_{C2} in the control loop as shown by the SSB control of Fig. 5.1, the reference voltage dynamics, $v_{ab,ref}(s)$, in (5.1) can be equated to the con-

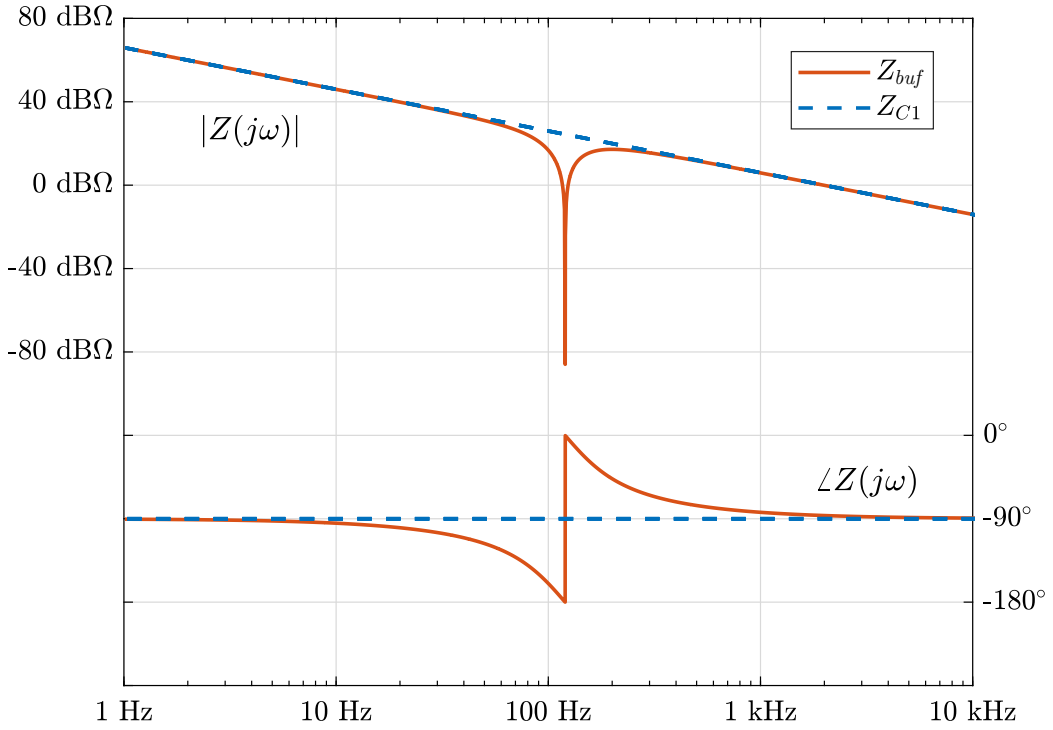


Figure 5.2: Bode plot of SSB small-signal equivalent impedance comparison of buffer ($Q = 1$) and primary buffer capacitor, $C_1 = 80\ \mu$.

verter output voltage dynamics, $v_{ab}(s)$. Finally, to determine the equivalent impedance of the buffer, $Z_{buf}(s)$, divide (5.1) by the small-signal buffer current, $i_{C1}(s) = i_{ab}(s)$, to determine the equivalent impedance at terminals 'a-b', $Z_{ab}(s)$, and add to the series-connected capacitor impedance, $Z_{C1}(s)$.

$$\begin{aligned} Z_{buf}(s) &= Z_{C1}(s) + Z_{ab}(s) \\ &= Z_{C1}(s)\Big(1 - G_{bpf}(s)\ \Big(1 - \beta G_d(s)\Big)\Big) \\ &\approx Z_{C1}(s)\ G_n(s). \end{aligned} \tag{5.3}$$

As the buffer loss compensation constant, β, is relatively small for high efficiency converters, it can be neglected and the result in (5.3) can be simplified. As shown in Fig. 5.2, the equivalent small-signal buffer impedance for the SSB shown by (5.3) is equivalent to the impedance of capacitor C_1 except near ω_{2L} where it exhibits resonance-type characteristics. Variation of the parameter, Q, in (5.2) directly controls the bandwidth and group delay of the notch at ω_{2L}. The bandwidth of $G_n(s)$ should be chosen sufficiently large to minimize the settling time of the buffer converter during load steps, but

sufficiently small as to not adversely effect the capacitive behavior of the SSB at low frequencies. The latter consideration directly influences the PFC front-end control design.

5.2 Boost PFC Front-End Control Design with Series-Stacked Buffer

The FCML boost converter as shown in the schematic of Fig. 5.1 driven with PSPWM (phase-shifted pulse-width modulated) signals and operating in CCM is equivalently modeled as an ordinary boost converter in CCM assuming that the flying capacitors are appropriately sized and consequently the capacitor voltages remain balanced in steady-state [32]; these assumptions are reasonable for conscientious FCML design and layout. Enabling faster and more compact switching converters with the use of GaN, facilitating proper gate driver power regulation and signal isolation [39], ensuring minimized switch pair commutation loops [40], and simply utilizing an even (as opposed to odd) number of levels [41] can improve capacitor balancing and contribute to successfully operable system design.

In conventional multi-loop, PLL-based, average current PFC rectifier control, a wide-bandwidth "inner" input current feedback loop regulates a sinusoidal reference instantaneously to ensure a high power factor with minimal distortion and phase displacement, while a low-bandwidth "outer" feedback loop regulates the average output voltage [33, 34, 42]. In this work, the PFC control architecture as shown in Fig. 5.1 follows the design and methodology presented in [32]. Notable implementation details include a multi-loop control scheme, phase locking to input voltage phase with PLL, and partial feedforward on the current loop as introduced in [35]. This control scheme contains an additional feedforward loop which mitigates the requisite control effort of the feedback loop. Rather than regulating the entire rectified sinusoidal reference necessary for high power factor, the feedback loop compensates for the differences between the feedforward loop and the measured current response, with which proper choice of feedforward can allow for more relaxed feedback compensation design and improved system stability over a larger converter operating range.

Certain considerations must be made when compensating the outer voltage

loop. There should be relatively low closed-loop gain at even harmonics of the line frequency. By choosing a sub-ω_{2L} pole in a low-pass filter compensator, the twice-line frequency component of v_{out} is not over-regulated, which can cause significant distortion in the input current due to the instantaneous power difference between AC and DC sides of the converter [42, 43].

First, the control-to-current transfer function, $G_{id}(s)$, of an average current control boost PFC converter can determine the effect of the SSB on the current control loop. For this type of PFC, $G_{id}(s) = \frac{i_L(s)}{d(s)}$ can be approximated as $\frac{V_{out}}{sL_b}$ assuming a good regulation and small instantaneous ripple of v_{out} [43]. This assumption is valid since the output voltage feedback loop of the PFC control should have bandwidth significantly less than ω_{2L} for proper operation [42, 43] and the buffer converter can operate correctly in steady-state [37, 38]. Consequently, the buffer impedance has negligible impact on the current loop design of the PFC front-end. When determining the effect of Z_{buf} on the voltage control loop, the output voltage feedback loop has non-negligible gain for frequencies less than ω_{2L} and the impedance of the SSB is equivalent to the impedance of the capacitor C_1 as shown by (5.3) in Fig. 5.2.

Considering these effects on the voltage and current loops, the greatest impact of replacing a DC-link output capacitor with an SSB on PFC control stability in steady-state is that the voltage feedback compensator must be adjusted for an output capacitance of $C_1 + C_{out}$ to retain low feedback control bandwidth.

5.3 Proposed SSB Control and Integration with PFC

The voltage-control method of the SSB described in Chapter 4 seeks to control the emulated output impedance of the buffer converter at ω_{2L} by computing an output voltage reference, $v_{ab,ref}$, as the sum of two orthogonal voltage vectors, $v_{ab,j}$ and $v_{ab,i}$, which control the real and reactive power flow of the buffer converter, respectively. By measuring v_{C1} and utilizing the linear high-Q peak filter in (5.2) to extract its ω_{2L} component, $v_{C1,\omega_{2L}}$, the primary control voltage, $v_{ab,j} = -v_{C1,\omega_{2L}}$, and loss compensation control voltage, $v_{ab,i} = \beta \frac{d}{dt} v_{C1,\omega_{2L}}$, are computed.

Similar functionality of the band-pass filter in (5.2) can be obtained uti-

lizing a sinusoidal reference where the magnitude and phase are specified directly. This is the same nonlinear control technique common in conventional PFC rectifiers and used in regulating the current reference of the PFC rectifier in this chapter. As an example, if a desired voltage is defined as $v_{ac}(t) = V_{ac}\sin(\omega_{ac}t + \phi_{ac}) = V_{ac}\sin(\theta_{ac})$, then the information necessary to compute $v_{ac}(t)$ is the desired magnitude, V_{ac}, and the phase, θ_{ac}. For power electronics, the magnitude information is often a function of steady-state operating conditions, such as the load, and can be computed using linear gain feedback of measured signals. The phase information must be computed dynamically in real-time with a PLL (phase-locked loop) to ensure an intended phase relationship—in this example ϕ_{ac}—with other signals such as another current or voltage.

The proposal here is an implementation of this nonlinear real-time control technique to generate the sinusoidal twice-line frequency signals of the SSB as

$$v_{ab,j} = -V_{C1,max}\sin(\theta_{buf}) \tag{5.4}$$

$$v_{ab,i} = \beta\ \omega_{2L}V_{C1,max}\cos(\theta_{buf}). \tag{5.5}$$

Inputs θ_{buf} and $V_{C1,max}$ should be chosen as functions of intermediate feedback states found in the PFC control architecture. In the proposed control shown in Fig. 5.1, the phase is computed simply as a direct function of the PLL phase information, $\theta_{buf} = 2\theta_{ac}$. The phase relationships between (5.4) and (5.5) (i.e., the sine and cosine) correspond directly to the standard operating waveforms of the SSB [36] in relation to the AC input of the PFC front-end. The magnitude, $V_{C1,max}$, is a function of the load and DC output voltage of the system and can thus be computed as

$$V_{C1,max} = \frac{\pi k}{4\omega_{2L}V_{ref}C_1}, \tag{5.6}$$

where k is the feedback regulated PFC voltage-loop factor as shown in the PFC control of Fig. 5.1. The proposed nonlinear filter behaves similarly to the previously defined peak filter in (5.2) since it has notch filter characteristics but without the potential input-output phase mismatch.

With these choices of θ_{buf} and $V_{C1,max}$, the dynamics of the SSB are coupled very closely to the dynamics of the PFC regulation. For instance, as the PLL phase output locks, then both the PFC input current and buffer

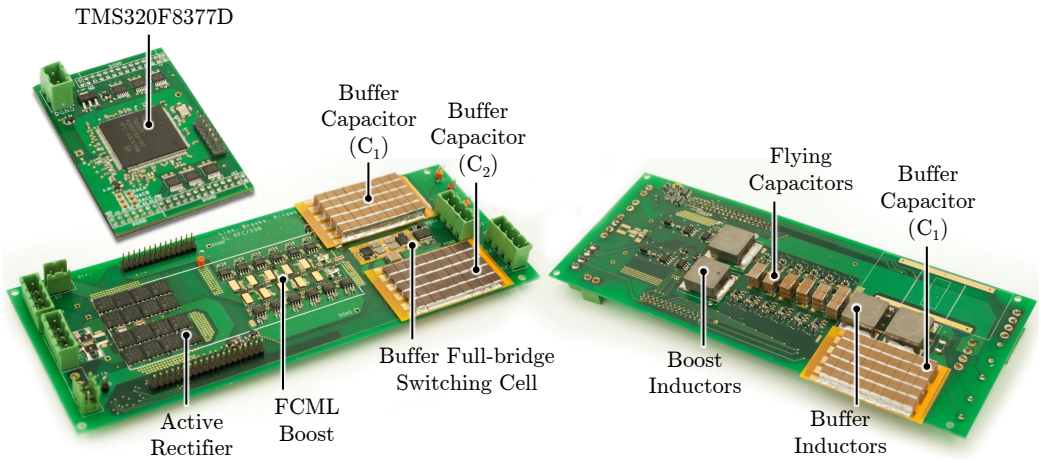


Figure 5.3: Fully integrated hardware prototype of 6-level FCML boost PFC front-end and SSB.

converter output voltage are locked jointly. Similarly, as the PFC voltage-loop factor, k, has low bandwidth in the PFC control design, the computed references in (5.4) and (5.5) remain sinusoidal across the AC line cycle for the SSB. The PFC and SSB responses become near identical, and the anticipated dynamics of each system can be more closely approximated as a single stably controlled system. Within existing PFC literature, the established advantages and disadvantages of using a PLL-based sine reference for PFC control can be applied to the SSB control method proposed here.

5.4 Experimental Validation

The proposed control is experimentally verified with a hardware prototype designed for a 1.5 kW, universal input (i.e., v_{ac} = 120 to 240 V_{rms}), 400 V output PFC rectifier as shown in Fig. 5.3. Experimental waveforms at 750 W are illustrated in Fig. 5.4 and Fig. 5.5 which validate the control scheme. The hardware has a notably high peak system efficiency of 98.4%; volumetric power density by box volume of 490 W/in^3 and 434 W/in^3 for the PFC front-end and SSB, respectively; high power factor greater than 0.994 across the whole load range; and minimal DC bus voltage ripple of less than 5 V_{p-p} at 750 W.

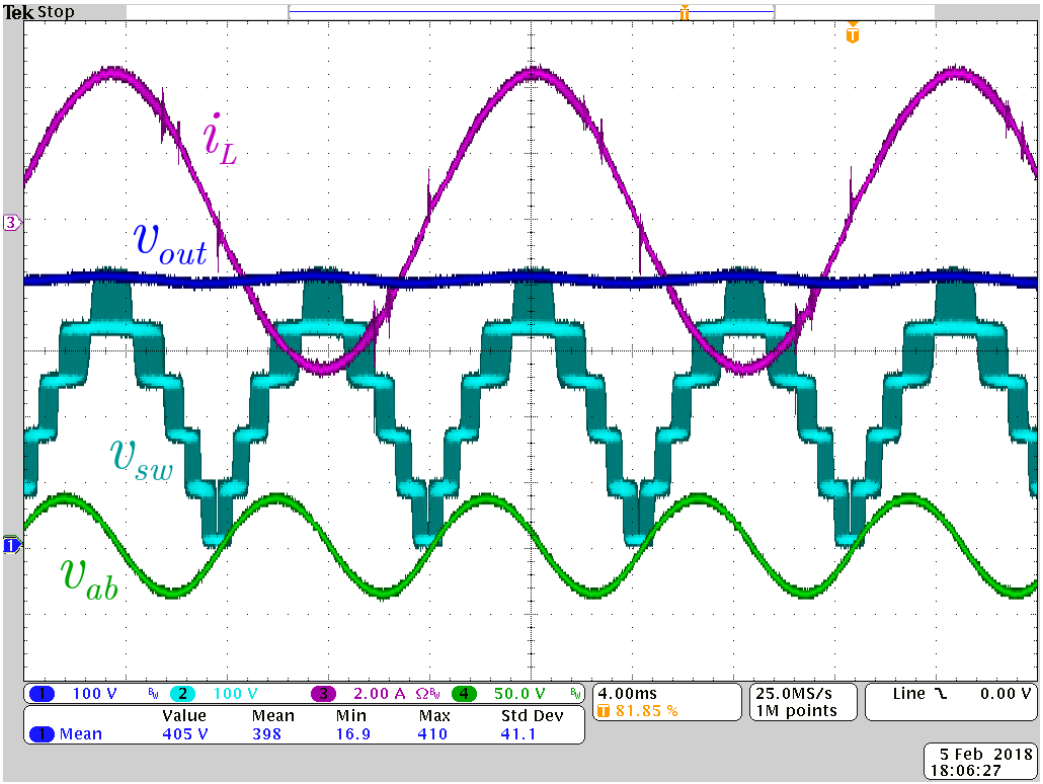


Figure 5.4: Experimental waveforms of input current, i_{ac}; output voltage, v_{out}; switching node voltage, v_{sw}; and buffer converter output voltage, v_{ab}. 240 V_{rms} input, 750 W load.

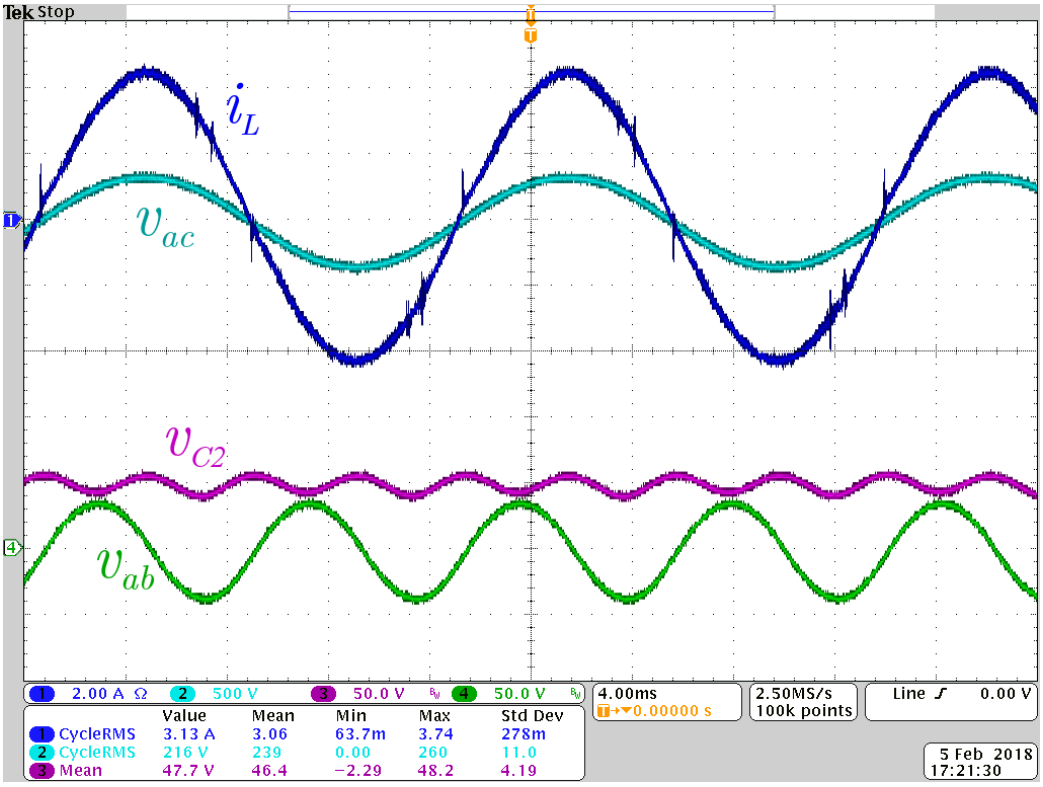


Figure 5.5: Experimental waveforms of input current, i_{ac}; input voltage, v_{ac}; auxiliary buffer converter voltage, v_{C2}; and buffer converter output voltage, v_{ab}. 240 V_{rms} input, 750 W load.

CHAPTER 6

EFFICIENCY IN THE SERIES-STACKED BUFFER

When comparing implementations between power electronics it is useful to have well defined metrics generally agreed upon within industry and academia. These metrics both define correct behavior and quantify how effectively a converter performs. Additionally, critical metrics dictate how electronics should be measured and tested so that they eventually meet the standards specified by the community. Essentially, quantifiable metrics allow one to determine whether one converter is better than another and thus to make technological improvements from day to day.

Most typically, when defining how well energy is converted from the input of a system to its output, the typical standard is the input-to-output efficiency. However, there end up being many definitions of efficiency which are not mathematically equivalent but still provide valid measures for a power converter. This chapter seeks to define and address these competing metrics to determine which is the most useful. Additionally, other metrics which quantify energy processing capabilities of a system are considered including loss, average processed power, and quality factor.

6.1 Power and Energy in Multi-Port Systems

It is important to first distinguish the definitions of power and energy. For an electrical port, the instantaneous power, $P(t)$, is a product of the instantaneous voltage, $v(t)$, and instantaneous current, $i(t)$. Power in units of watts [W] or joules per second [J/s] is a rate of change in energy, $E(t)$, in units of joules [J] and is mathematically defined with a derivative

$$P(t) = \frac{dE(t)}{dt} \tag{6.1}$$

or an indefinite integral

$$E(t) = \int P(t)dt \tag{6.2}$$

where for real systems, the scalar functions of $P(t)$ and $E(t)$ at a port are assumed to be continuous and $E(t)$ is assumed to be differentiable. Considering the practical implications of (6.1) at a port in a system, when energy enters the port, the power is positive—i.e., $\frac{dE(t)}{dt} = P(t) > 0$—and when energy exits the port, the power is negative—i.e., $\frac{dE(t)}{dt} = P(t) < 0$. Throughout the chapter, this convention is indicated graphically with an arrow pointing in the direction of positive power for each port of a system.

Additionally, the time average operation of a time-variable function, $x(t)$, can be defined as

$$\langle x(t) \rangle_T = \frac{1}{T} \int_0^T x(t)dt. \tag{6.3}$$

If the port is periodic (i.e., $v(t)$ and $i(t)$ are periodic) then the time average of $P(t)$ is most meaningful when considering steady-state, periodic waveforms with period T (i.e., when $x(t) \approx x(t+T)$).

6.2 One-Port Systems

In a system defined with one port as shown in Fig. 6.1, there is only one port for which energy, denoted as $E(t)$, flows into and out of the system. The power $P(t)$ at the port can be defined as a superposition of instantaneous power input and power output

$$P(t) = P_{in}(t) + P_{out}(t), \tag{6.4}$$

where the input power is

$$P_{in}(t) = \begin{cases} P(t) & \text{for } P(t) \geq 0 \\ 0 & \text{for } P(t) < 0 \end{cases} \tag{6.5}$$

and the output power is

$$P_{out}(t) = \begin{cases} P(t) & \text{for } P(t) \leq 0 \\ 0 & \text{for } P(t) > 0. \end{cases} \tag{6.6}$$

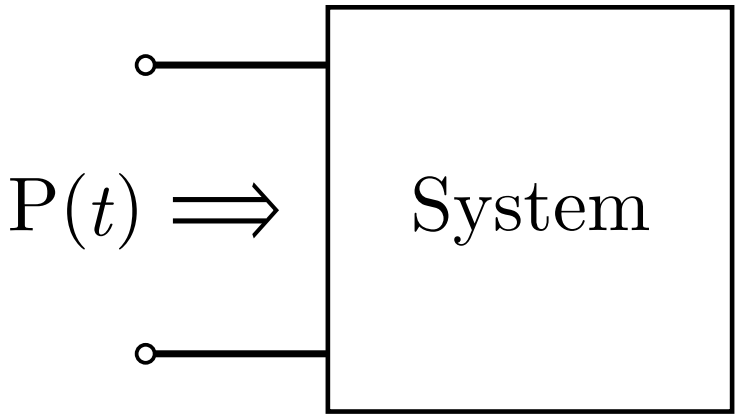


Figure 6.1: General one-port form defining power (energy flow) into a system.

Similarly, the net energy $E(t)$ at the port is defined as a superposition

$$E_{in}(t) = \begin{cases} E(t) & \text{for } P(t) \geq 0 \\ 0 & \text{for } P(t) < 0 \end{cases} \tag{6.7}$$

$$E_{out}(t) = \begin{cases} E(t) & \text{for } P(t) \leq 0 \\ 0 & \text{for } P(t) > 0 \end{cases} \tag{6.8}$$

$$E(t) = E_{in}(t) + E_{out}(t). \tag{6.9}$$

Notice that E_{out} and $E_{in}(t)$ are defined as a function of the direction of power flow—i.e., whether the energy is flowing into or out of the system. The relationships in (6.5) and (6.6) are defined such that $P_{in}(t)$ is strictly positive and $P_{out}(t)$ is strictly negative, and both are periodic if $P(t)$ is periodic; additionally, $E_{in}(t)$ and $E_{out}(t)$ are periodic if $E(t)$ is periodic. As the function definitions in (6.5) - (6.8) can be piecewise, these waveforms are not necessarily continuous or differentiable.

The net energy change at the port for each time cycle T is defined as the difference between the net energy in and out of the port per cycle

$$E_L = |E_{in}| - |E_{out}| \tag{6.10}$$

where E_{in} is computed as an accumulation of power flow into the port per

cycle

$$E_{in} = \int_0^T P_{in}(t)\ dt \tag{6.11}$$

and E_{out} is computed as an accumulation of power flow out of the port per cycle

$$E_{out} = \int_0^T P_{out}(t)\ dt. \tag{6.12}$$

Notice that because of the sign conventions of $P_{in}(t)$ and $P_{out}(t)$, E_{in} is a positive scalar and E_{out} is a negative scalar. For a practically defined system, the net energy E_L is a positive value representing energy loss per cycle since $|E_{in}| \geq |E_{out}|$.

Relating the time-average input power as defined by (6.3) and the net input energy per cycle in (6.11) yields

$$\langle P_{in}(t) \rangle = \frac{1}{T} \int_0^T P_{in}(t)\ dt = \frac{1}{T} E_{in}. \tag{6.13}$$

Similarly,

$$\langle P_{out}(t) \rangle = \frac{1}{T} \int_0^T P_{out}(t)\ dt = \frac{1}{T} E_{out}. \tag{6.14}$$

The results of (6.11) and (6.12) are important in relating both power and energy to a metric of efficiency.

6.3 Multi-Port Systems

In a multi-port system, there are n ports where power and energy can flow. The general two-port power converter shown in Fig. 6.2 indicates the nomenclature of a numerical subscript for each port's instantaneous power and energy. Many of the results for the one-port system can be applied to the multi-port generalization.

Utilizing (6.4) at each port i, the definition for instantaneous input power defined in (6.5) can be extended for each port as

$$P_{i,in}(t) = \begin{cases} P_i(t) & \text{for } P_i(t) \geq 0 \\ 0 & \text{for } P_i(t) < 0 \end{cases} \tag{6.15}$$

and then the total instantaneous input power $P_{in}(t)$ can be expressed as a

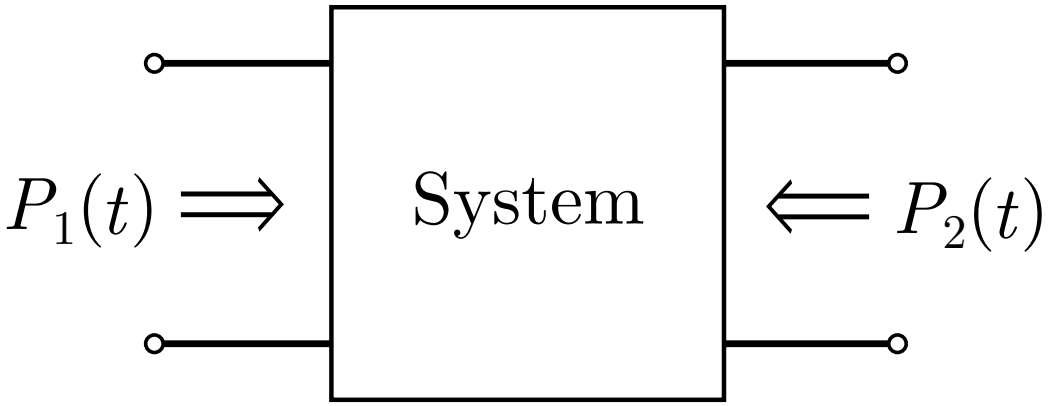


Figure 6.2: General two-port form defining power (energy flow) into a system.

sum of every port's input power waveforms as

$$P_{in}(t) = \sum_{i=1}^{n} P_{i,in}(t). \tag{6.16}$$

A similar derivation for the output power reveals

$$P_{i,out}(t) = \begin{cases} P_i(t) & \text{for } P_i(t) \geq 0 \\ 0 & \text{for } P_i(t) < 0 \end{cases} \tag{6.17}$$

$$P_{out}(t) = \sum_{i=1}^{n} P_{i,out}(t). \tag{6.18}$$

Using these delineations, the definitions of net system energy input and output in (6.10) - (6.12) and the average power to energy relationships in (6.13) and (6.14) are equivalently defined for the multi-port case.

6.3.1 Special Case of Multi-Port Power Converter

A unique case of the multi-port power converter arises when every port has instantaneous power which is either strictly positive or strictly negative. Consequently, the each port can be strictly delineated as an input or an output port. This results in a simplification of $P_{in}(t)$ defined by (6.16) to becoming a sum of the input port instantaneous powers, and $P_{out}(t)$ defined by (6.18) to becoming a sum of the output port instantaneous powers. For instance in

Fig. 6.2, if port 1 was an input and port 2 was an output, then $P_{in}(t) = P_1(t)$ and $P_{out}(t) = P_2(t)$.

This unique case of the multi-port system is the traditional implementation of unidirectional power converters. For instance, a unidirectional DC-DC or a unidirectional resistively loaded AC-DC (or DC-AC) power converter both have strictly positive power input and strictly positive power output.

6.4 Defining Efficiency and Absolute Loss

Two terms must be well defined before continuing: efficiency and absolute loss.

Efficacy, a general form of efficiency, is defined as the ratio of a time-averaged characteristic input and output metric of a system. For instance a light bulb is a power converter as it converts AC electric power to luminous power (i.e., light). The efficacy of a light bulb is defined as the time-average light flux output (in lumens) per unit of time-average power input (in watts). Efficiency is a subset of efficacy for which both the input and output are defined in terms of the same units such as power or energy. In other words, efficiency is normalized efficacy. For a power converter, efficiency is generally defined as the ratio of net energy out of a system to net energy into a system per time cycle T as

$$\eta = \left| \frac{E_{out}}{E_{in}} \right| = \left| \frac{\langle P_{out}(t) \rangle}{\langle P_{in}(t) \rangle} \right|. \tag{6.19}$$

The efficiency defined in (6.19) can also be defined as a ratio of time-averaged power output to time-averaged power input because $E_{in} \propto \langle P_{in}(t) \rangle$ and $E_{out} \propto \langle P_{out}(t) \rangle$ as derived in (6.13) and (6.14).

Utilizing this proportionality, power loss can be similarly defined using (6.10) as the difference between the time-averaged input and output power to a system

$$P_L = |\langle P_{in}(t) \rangle| - |\langle P_{out}(t) \rangle|. \tag{6.20}$$

Also, E_L and P_L are proportional and in fact further equated by

$$P_L = \frac{E_L}{T} \tag{6.21}$$

for the time-averaged period, T.

Notice the efficiency in (6.19) can also be defined as a function of the net energy into a system and the energy lost in a system

$$\eta = 1 - \frac{E_L}{E_{in}} = 1 - \frac{P_L}{\langle P_{in}(t) \rangle}. \tag{6.22}$$

The result of (6.22) will become more crucial later as measurement practicality and ease are considered.

Efficiency, loss, and (average) power processed only have meaning when characterizing the steady-state behavior of a system. This work will apply these aforementioned definitions of efficiency and loss as the discussion progresses for particular situations.

6.4.1 Multi-Port Power Conversion Efficiency

A single electronic power converter is typically one stage in a series of cascaded power conversion stages—e.g., other power electronics, electric machines, light bulbs, solar panels. This system description merits the simple two-port representation as shown in Fig. 6.2 which is widely applicable to the large majority of power converters. Average energy loss is the difference net energy input and output as defined by (6.10). Efficiency is the ratio of energy out to energy in and ranges between zero and one as defined by (6.19) and (6.22). These results are generally applied to a multi-port system as long as $P_{in}(t)$ is the instantaneous sum of all input port power and $P_{out}(t)$ the instantaneous sum of all output port power.

Two-port efficiency is the correct metric for comparison when considering the system efficiency of cascaded power converters (e.g., rectifier/inverter and DC-side buffer). One simply needs to determine the two-port efficiency of each converter and multiply to compute the total system efficiency. Additionally, this portrayal of efficiency complies well with the most widely accepted definitions within the power electronics field of study. This minimizes the potential for confusion and misrepresentation of buffer design and comparison by others.

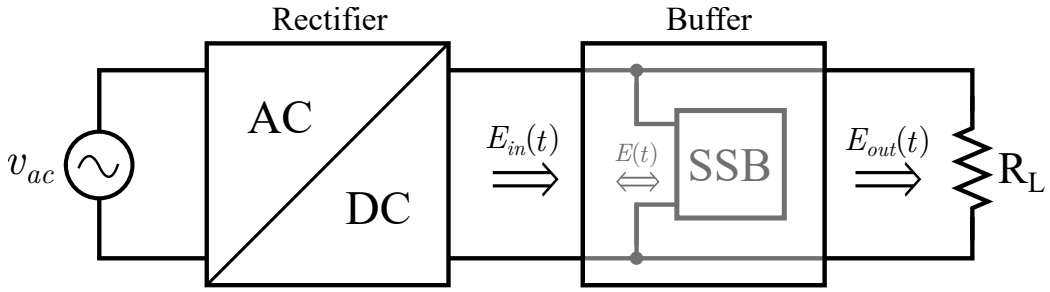


Figure 6.3: Characterization of DC-side twice-line frequency energy buffer in both one-port and two-port form.

6.4.2 One-Port Power Conversion Efficiency

The efficiency metric, being a normalized relative value, will have a different result when the system is defined with one port or two ports. In other words one-port efficiency of a power converter is not necessarily equivalent to the two-port efficiency of the same power converter. For instance a parallel-connected sub-system, such as the DC-side SSB shown in Fig. 6.3, can be characterized as either a one-port or two-port system. With the experimental data obtained using the hardware prototype of Chapter 4, the one-port and two-port efficiencies (η_{1p} and η_{2p}) of the SSB are computed from measured data and shown in Fig. 6.4. It is clear in this circumstance that η_1 and η_2 are not equivalent for the same system, although there is a proportional relationship. Using these described definitions in retrospect, the results illustrated in Fig. 4.12 represent one-port efficiency calculations.

In the case shown in Fig. 6.3, E_{in} and E_{out} defined for a two-port system as in Fig. 6.2 are not equivalent to E_{in} and E_{out} defined for a one-port system by Fig. 6.1. This peculiarity is not unreasonable as there are many possible two-port representations of a one-port sub-system. Each potential two-port representation has differing and arbitrary instantaneous power and energy input and output waveforms. In other words, there is a relationship between the one-port and two-port efficiency, but it is not uniquely defined for all systems.

One-port efficiency only applies to a very specific topologies of power converters or systems which can be characterized with one electrical port. It is not widely used as a metric, perhaps for this precise reason. However, it can still be considered a potentially useful performance metric within the category of DC-side twice-line frequency buffers. Unlike the two-port definition,

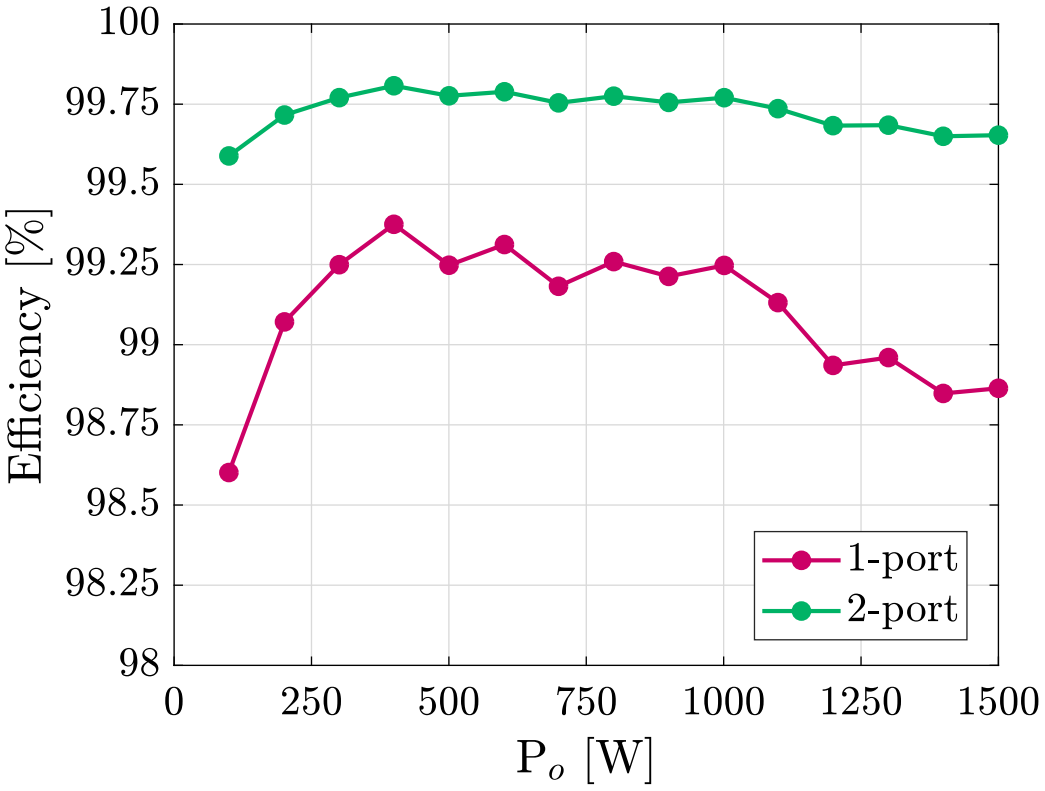


Figure 6.4: Measured one-port and two-port efficiency of the SBB over the full system load range.

one-port efficiency characterizes a different type of ideal converter behavior where all the energy into a port must then output over one periodic cycle. One-port efficiency indicates how the shapes of $E(t)$ and $P(t)$ differ from the ideal.

6.4.3 Quality Factor

Quality factor is another unitless measure of efficiency unique to one-port system representations which quantifies the ratio of energy lost to peak energy stored (in $E(t)$) per cycle T as

$$Q = 2\pi \frac{E_{in}}{E_L}. \tag{6.23}$$

Quality factor is a common measure of efficiency for ideally reactive one-port devices such as capacitors and inductors and can otherwise be expressed

as

$$Q = \frac{X}{R} \tag{6.24}$$

where X is the frequency dependent reactance and R is the equivalent series resistance of an impedance. The measure of Q is clearly related to the efficiency in (6.22) as $\eta = 1 - \frac{1}{Q}$.

6.4.4 Absolute Loss

The absolute loss defined by (6.10) and (6.21) is equivalent for both the one-port and two-port representations. Regardless of the port designation of a system, conservation of energy dictates the net energy of a system is zero per time-averaged cycle. If the electrical energy into does not equal the electrical energy out of the system, then the difference must be energy "lost" which is converted to a form such as heat or motion. This fact in itself implies absolute loss is a unifying measure of performance, especially when the port representation is unclear.

Absolute loss also has much more meaning than efficiency in the context of thermal management requirements. One can determine, for any system, exactly how much thermal power must be dissipated with a heatsink. However unlike efficiency, absolute loss does scale intuitively with system-level operating conditions such as power or voltage requirements. Efficiency is a better metric for comparison of hardware with different processing powers.

6.5 Processed Power

Another unique performance metric for power converters is the average power which must be processed. The average power processed is a high-level indication of how much stress the system power requirements impose on a converter. A higher measure of average power processed implies higher losses in the system. In some ways, this metric functions similarly to the apparent power rating of electromechanical motors and generators in defining to a user how much energy can a system handle.

A reasonable definition of processed power is the "input" power for a power converter since the energy into a system is the energy which must be con-

verted (as the name of a power converter suggests). It is important to specify that once the input port is designated, the instantaneous power at the port $P_i(t)$, whether positive or negative, still represents power that must be processed by the power converter. Thus an absolute value function must be used to mathematically justify the irrelevance of the sign of $P(t)$. For a one-port system, as the only port is the input port, the power processed is defined as

$$\begin{aligned} P_{proc,1p} = \langle |P_{proc,1p}(t)| \rangle &= \langle |P(t)| \rangle \\ &= \langle |P_{in}(t)| \rangle + \langle |P_{out}(t)| \rangle \\ &= |\langle P_{in}(t) \rangle| + |\langle P_{out}(t) \rangle| \end{aligned} \tag{6.25}$$

according to the definitions of $P_{in}(t)$ and $P_{out}(t)$ defined by (6.5) and (6.6).

For a two-port system, the input power is defined differently as $P_{in}(t) = P_i(t)$ where i is the designated input port. Consequently, the average power processed is defined as

$$P_{proc,2p} = \langle |P_{proc,2p}(t)| \rangle = \langle |P_{in}(t)| \rangle. \tag{6.26}$$

6.5.1 Series-Stacked Buffer

For an ideal instantaneous power waveform for a twice-line frequency buffer as defined by (2.3), the one-port power processed can be computed using (6.25) as

$$P_{proc,1p} = \langle |P_{buffer}(t)| \rangle = \langle |-P_o \cos(2\omega_L t)| \rangle = \frac{2}{\pi} P_o. \tag{6.27}$$

For the two-port representation DC-side buffer as shown in Fig. 6.3, the two-port power processed can be computed using (2.2) and (6.26) as

$$P_{proc,2p} = \langle |P_{ac}(t)| \rangle = \langle |P_o + P_o \cos(2\omega_L t)| \rangle = P_o. \tag{6.28}$$

The differences in defining the power processed in a system is relative to the system representation. In fact the efficiency defined by (6.22) can be simplified as

$$\eta_{1p} = 1 - \frac{P_L}{\langle |P_{in}(t)| \rangle} = 1 - \frac{P_L}{P_{proc,1p}}. \tag{6.29}$$

for a one-port system and as

$$\eta_{2p} = 1 - \frac{P_L}{\langle |P_{in}(t)| \rangle} = 1 - \frac{P_L}{P_{proc,2p}}. \tag{6.30}$$

for a two-port system.

To compute the power processed by the active components—i.e., buffer converter—of the SSB as shown in Fig. 4.3, then one computes the instantaneous power at terminals a and b as $P_{ab}(t) = v_{ab}(t)i_{ab}(t)$ and uses (6.25) to compute the average processed power. In this way, any active DC-side twice-line frequency buffer can be compared on the basis of power processing requirement/capability. The terminal power of the buffer converter in the SSB, P_{ab}, can be approximately defined (assuming negligible loss or loss compensation in the control) as

$$\begin{aligned} P_{ab}(t) = v_{ab}(t)i_{ab}(t) &= \Big(\frac{I_{dc}}{\omega_{2L}C_1}\cos(\omega_{2L}t)\Big)\Big(I_{dc}\sin(\omega_{2L}t)\Big) \\ &= \frac{I_{dc}^2}{2\omega_{2L}C_1}\sin(2\omega_{2L}t), \end{aligned} \tag{6.31}$$

where I_{dc} is the DC load current. Now having a quantitative expression for the terminal power, the average power processed by the buffer converter of the SSB can be determined as

$$\begin{aligned} P_{proc,ab} = \langle |P_{ab}(t)| \rangle &= \frac{I_{dc}^2}{2\omega_{2L}C_1} \cdot \frac{2}{\pi} \\ &= \frac{I_{dc}^2}{\pi\omega_{2L}C_1}. \end{aligned} \tag{6.32}$$

For the SSB hardware prototype in Chapter 4 where $I_{dc} = 3.75$ A, $C_1 = 80$ μF, and $\omega_{2L} = 2\pi 120$ rad/s, the power processed by the buffer converter utilizing (6.32) is evaluated as approximately $P_{proc,ab} = 75$ W which is 5% of the system power rating of 1500 W. This relatively low processed power allows the SSB to fundamentally obtain minimal losses comparable to a DC-link capacitor bank.

6.6 Measurement

The result of (6.19) is the traditionally accepted definition of efficiency for multi-port systems—the ratio of average energy out of the system per cycle (T) over average energy into the system per cycle. As measuring instantaneous voltages and currents is a relatively straightforward process for electrical systems, power measurements are often used to compute efficiency rather than the energy. Modern digital Yokogawa power meters measure instantaneous voltage and current, compute instantaneous power, and cycle average to obtain the average power through a port. A calorimetric measurement, a costlier and higher resolution alternative, is a type of power measurement testbed which instead monitors changes in temperature to compute energy loss over some specified time instead of power flow. Both testbeds can compute the total energy and/or power lost in a multi-port system as energy into the system passes through to the output.

For the one-port SSB efficiency testbed as shown in Fig. 4.9, the average power across the port is measured and consequently corresponds directly to the system absolute power loss. This is potentially a high fidelity, low error measurement as the range and resolution of the Yokogawa WT310 differ by merely three orders of magnitude (range = 10 W, resolution = 10 mW). The two-port efficiency can then be calculated with (6.22). Additionally, values of E_{in} and E_{out} can be measured directly using a power integration feature of the digital power meter. This allows ease of calculation of the one-port efficiency of the system using (6.19).

Power processed by the buffer converter could be ascertained with a single power meter across terminals a and b and the use of the integration feature, however, one could argue that exact determination of this value is unnecessary. For most purposes, power processed is more of an indication of potential stress on a power converter than the exact limitation which influences practical converter design.

6.7 Apparent Power

As already mentioned, apparent power is a standard measure in the field of power systems. "Real" power, or the average of the instantaneous power,

cannot fully capture the stresses imposed on a power system. For instance, a near-lossless capacitor processes no real power and thus performs no work, yet there are still oscillatory power fluctuations which degrade performance over time. The missing component is called "reactive" power which defines how much energy is sloshed back and forth periodically within the capacitor. Observing the instantaneous power of an AC system with sinusoidal voltage and current, real power would be the average power throughput of the system and reactive power would be related to the magnitude of its ripple. Apparent power, then, defined using frequency-domain phasor notation as (4.6), is a vector sum of the real and reactive power. In the time-domain, apparent power is the magnitude of the ripple oscillation at twice the system electrical frequency in the instantaneous power waveform. The instantaneous power of the general single-phase system as shown in Fig. 2.2 indicates an example of these three power components: real, reactive, and apparent power.

Understanding how apparent power is defined, it cannot be easily used as a metric for characterizing DC-side ω_{2L} buffers. Unlike the electrical modeling of electric machines and power systems such as the grid, power analysis within the realm of power electronics is inherently non-linear. A power converter chops a voltage/current signal with circuit switch states. Consequently instantaneous power waveforms, defined as the instantaneous product of extremely non-sinusoidal voltage and current waveforms, is rife with harmonics which cannot be reasonably characterized with a single component of frequency as done with phasor analysis. This might appear counter-intuitive when considering the phasor/frequency domain analysis used to derive the control of the SSB in Section 4.4. However, this is because the ideal waveforms for $v_{ab}(t)$ and $i_{ab}(t)$ such as in Fig. 4.3 are purely sinusoidal.

There is perhaps one significant factor dissuading the use of apparent power as a measure for power electronics, specifically single-phase converters. While apparent power aptly characterizes AC ports, where voltage and current are pure sinusoids, it is ill-defined for DC ports or any other combination of $v(t)$ and $i(t)$. This is not to say apparent power is not a potentially useful metric to define buffer performance, but rather that it is simply not as tractable as the traditional definitions of efficiency and power processed which are easily applied to any power conversion system. Thus, apparent power is not a useful metric for the quantifiable comparison of buffer converters due to its lack of breadth applied to non-AC electrical ports.

CHAPTER 7

CONCLUSIONS

This work presents the fundamental design considerations of a resonant-type architecture for a DC-side twice-line frequency energy buffering application. Specifically, by emulating the desired behavior of a passive series-resonant LC tank, an active buffering topology and associated control methodology can be defined. This active topology, denoted as the series-stacked buffer (SSB), is modeled by this equivalent series-resonant impedance. Furthermore, a voltage control method which accounts for loss within the buffer is fully developed based on this equivalent impedance model.

Once the independent operation of the SSB is established, efforts are made to characterize interaction with the single-phase conversion stage of the full single-phase system. The frequency-dependent equivalent impedance of the SSB is used as a direct substitute for the output (buffering) capacitance in the traditional small-signal model of a PFC boost rectifier. Stability of the PFC front-end is defined quantitatively as a function of the SSB design. Furthermore, an integrated control scheme is proposed between the PFC front-end and SSB which imposes phase-locking in steady-state and a uniform response during transients for the full system. As an additional consideration, definitions of efficiency, power loss, and power processed for a DC-side buffer, specifically for one-port systems, are established and compared quantitatively.

REFERENCES

[1] J. Kolar, U. Drofenik, J. Biela, M. Heldwein, H. Ertl, T. Friedli, and S. Round, "PWM converter power density barriers," in *Power Conversion Conference*, 2007, pp. 9–29.

[2] J. W. Kolar, J. Biela, S. Waffler, T. Friedli, and U. Badstuebner, "Performance trends and limitations of power electronic systems," in *2010 6th International Conference on Integrated Power Electronics Systems*, March 2010, pp. 1–20.

[3] P. T. Krein, R. S. Balog, and M. Mirjafari, "Minimum energy and capacitance requirements for single-phase inverters and rectifiers using a ripple port," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4690–4698, Nov 2012.

[4] S. Harb, M. Mirjafari, and R. S. Balog, "Ripple-port module-integrated inverter for grid-connected pv applications," *IEEE Transactions on Industry Applications*, vol. 49, no. 6, pp. 2692–2698, Nov 2013.

[5] R. Wang, F. Wang, D. Boroyevich, R. Burgos, R. Lai, P. Ning, and K. Rajashekara, "A high power density single-phase pwm rectifier with active ripple energy storage," *IEEE Transactions on Power Electronics*, vol. 26, no. 5, pp. 1430–1443, May 2011.

[6] S. Wang, X. Ruan, K. Yao, and Z. Ye, "A flicker-free electrolytic capacitor-less ac-dc led driver," in *2011 IEEE Energy Conversion Congress and Exposition*, Sept 2011, pp. 2318–2325.

[7] Y. Yang, X. Ruan, L. Zhang, J. He, and Z. Ye, "Feed-forward scheme for an electrolytic capacitor-less ac/dc led driver to reduce output current ripple," *IEEE Transactions on Power Electronics*, vol. 29, no. 10, pp. 5508–5517, Oct 2014.

[8] Y. Tang, F. Blaabjerg, P. C. Loh, C. Jin, and P. Wang, "Decoupling of fluctuating power in single-phase systems through a symmetrical half-bridge circuit," *IEEE Transactions on Power Electronics*, vol. 30, no. 4, pp. 1855–1865, April 2015.

[9] Y. Tang, Z. Qin, F. Blaabjerg, and P. C. Loh, "A dual voltage control strategy for single-phase pwm converters with power decoupling function," *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 7060–7071, Dec 2015.

[10] M. Chen, K. K. Afridi, and D. J. Perreault, "Stacked switched capacitor energy buffer architecture," in *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Feb 2012, pp. 1404–1413.

[11] K. K. Afridi, M. Chen, and D. J. Perreault, "Enhanced bipolar stacked switched capacitor energy buffers," in *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2012, pp. 4209–4216.

[12] H. Wang, H. S. H. Chung, and W. Liu, "Use of a series voltage compensator for reduction of the dc-link capacitance in a capacitor-supported system," *IEEE Transactions on Power Electronics*, vol. 29, no. 3, pp. 1163–1175, March 2014.

[13] W. Liu, K. Wang, H. S. h. Chung, and S. T. h. Chuang, "Modeling and design of series voltage compensator for reduction of dc-link capacitance in grid-tie solar inverter," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2534–2548, May 2015.

[14] H. Wang, H. Wang, G. Zhu, and F. Blaabjerg, "A generic topology derivation method for single-phase converters with active capacitive dc-links," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2016, pp. 1–8.

[15] J. C. Hancock, "On the convolution integral," *IEEE Transactions on Education*, vol. 8, no. 4, pp. 107–109, Dec 1965.

[16] H. Wang and F. Blaabjerg, "Reliability of capacitors for dc-link applications in power electronic converters - an overview," *Industry Applications, IEEE Transactions on*, vol. 50, no. 5, pp. 3569–3578, Sept 2014.

[17] C. Zhao, B. Trento, L. Jiang, E. A. Jones, B. Liu, Z. Zhang, D. Costinett, F. F. Wang, L. M. Tolbert, J. F. Jansen, R. Kress, and R. Langley, "Design and implementation of a gan-based, 100-khz, 102-w/in3 single-phase inverter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 824–840, Sept 2016.

[18] C. B. Barth, I. Moon, Y. Lei, S. Qin, C. Robert, and Pilawa-Podgurski, "Experimental evaluation of capacitors for power buffering in single-phase power converters," in *Energy Conversion Congress and Exposition (ECCE), 2015 IEEE*, Sept 2015, pp. 6269–6276.

[19] Y. Lei, C. Barth, S. Qin, W. Liu, I. Moon, A. Stillwell, D. Chou, T. Foulkes, Z. Ye, Z. Liao, and R. Pilawa-Podgurski, "A 2 kw, single-phase, 7-level, gan inverter with an active energy buffer achieving 216 w/in3 power density and 97.6% peak efficiency," in *Applied Power Electronics Conference and Exposition (APEC), 2016 Thirty-first Annual IEEE*, 2016.

[20] S. Qin, Y. Lei, C. Barth, W.-C. Liu, and R. C. Pilawa-Podgurski, "A high-efficiency high energy density buffer architecture for power pulsation decoupling in grid-interfaced converters," in *Energy Conversion Congress and Exposition (ECCE), 2015 IEEE*, Sept 2015, pp. 149–157.

[21] S. Qin, Y. Lei, C. Barth, W.-C. Liu, and R. Pilawa-Podgurski, "Architecture and control of a high energy density buffer for power pulsation decoupling in grid-interfaced applications," in *Control and Modeling for Power Electronics (COMPEL), 2015 IEEE 16th Workshop on*, July 2015, pp. 1–8.

[22] S. Qin, Y. Lei, C. Barth, W. C. Liu, and R. C. N. Pilawa-Podgurski, "A high power density series-stacked energy buffer for power pulsation decoupling in single-phase converters," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4905–4924, June 2017.

[23] T. Shimizu, K. Wada, and N. Nakamura, "Flyback-type single-phase utility interactive inverter with power pulsation decoupling on the dc input for an ac photovoltaic module system," *Power Electronics, IEEE Transactions on*, vol. 21, no. 5, pp. 1264–1272, Sept 2006.

[24] A. Kyritsis, N. Papanikolaou, and E. Tatakis, "A novel parallel active filter for current pulsation smoothing on single stage grid-connected ac-pv modules," in *Power Electronics and Applications, 2007 European Conference on*, Sept 2007, pp. 1–10.

[25] R. Wang, F. Wang, D. Boroyevich, R. Burgos, R. Lai, P. Ning, and K. Rajashekara, "A high power density single-phase pwm rectifier with active ripple energy storage," *Power Electronics, IEEE Transactions on*, vol. 26, no. 5, pp. 1430–1443, May 2011.

[26] H. Li, K. Zhang, H. Zhao, S. Fan, and J. Xiong, "Active power decoupling for high-power single-phase pwm rectifiers," *Power Electronics, IEEE Transactions on*, vol. 28, no. 3, pp. 1308–1319, March 2013.

[27] H. Hu, S. Harb, N. Kutkut, I. Batarseh, and Z. Shen, "A review of power decoupling techniques for microinverters with three different decoupling capacitor locations in pv systems," *Power Electronics, IEEE Transactions on*, vol. 28, no. 6, pp. 2711–2726, June 2013.

[28] S. Li, W. Qi, S.-C. Tan, and S. Hui, "Integration of an active-filter and a single-phase ac/dc converter with reduced capacitance requirement and component count," *Power Electronics, IEEE Transactions on*, vol. PP, no. 99, pp. 1–1, 2015.

[29] D. Neumayr, D. Bortis, and J. W. Kolar, "Ultra-compact power pulsation buffer for single-phase dc/ac converter systems," in *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, May 2016, pp. 2732–2741.

[30] H. Wang and H. Wang, "A two-terminal active capacitor," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1–1, 2017.

[31] Z. Liao, N. Brooks, and R. C. N. Pilawa-Podgurski, "Design constraints for series-stacked energy decoupling buffers in single-phase converters," *IEEE Transactions on Power Electronics*, pp. 1–1, 2018.

[32] S. Qin, Z. Liao, Z. Ye, D. Chou, N. C. Brooks, and R. C. N. Pilawa-Podgurski, "A 99.1 efficient, 490 w/in3 power density power factor correction front end based on a 7-level flying capacitor multilevel converter," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2018.

[33] J. Chen, A. Prodic, R. W. Erickson, and D. Maksimovic, "Predictive digital current programmed control," *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 411–419, Jan 2003.

[34] G. Chu, C. K. Tse, S. C. Wong, and S. C. Tan, "A unified approach for the derivation of robust control for boost pfc converters," *IEEE Transactions on Power Electronics*, vol. 24, no. 11, pp. 2531–2544, Nov 2009.

[35] M. Chen and J. Sun, "Feedforward current control of boost single-phase pfc converters," *IEEE Transactions on Power Electronics*, vol. 21, no. 2, pp. 338–345, March 2006.

[36] S. Qin, Y. Lei, C. Barth, W. C. Liu, and R. Pilawa-Podgurski, "A high power density series-stacked energy buffer for power pulsation decoupling in single-phase converters," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1–1, 2016.

[37] H. Wang, H. Wang, and M. Lu, "Impedance characteristics modeling of a two-terminal active capacitor," in *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, July 2017, pp. 1–7.

[38] N. C. Brooks, S. Qin, and R. C. N. Pilawa-Podgurski, "Design of an active power pulsation buffer using an equivalent series-resonant impedance model," in *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, July 2017, pp. 1–7.

[39] Z. Ye, Y. Lei, W. C. L. Liu, P. S. Shenoy, and R. C. N. Pilawa-Podgurski, "Design and implementation of a low-cost and compact floating gate drive power circuit for gan-based flying capacitor multi-level converters," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2017, pp. 2925–2931.

[40] T. Modeer, C. B. Barth, N. Pallo, W. H. Chung, T. Foulkes, and R. C. N. Pilawa-Podgurski, "Design of a gan-based, 9-level flying capacitor multilevel inverter with low inductance layout," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2017, pp. 2582–2589.

[41] Z. Ye, Y. Lei, Z. Liao, and R. C. N. Pilawa-Podgurski, "Investigation of capacitor voltage balancing in practical implementations of flying capacitor multilevel converters," in *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, July 2017, pp. 1–7.

[42] A. Fernandez, J. Sebastian, P. Villegas, M. M. Hernando, and D. G. Lamar, "Dynamic limits of a power-factor preregulator," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 1, pp. 77–87, Feb 2005.

[43] R. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Kluwer Academics, 2000.

APPENDIX A

SCHEMATICS AND PCB LAYOUT

Figures A.1 to A.5 show the printed circuit board (PCB) schematic and layout for the hardware prototype presented in Chapter 4. The custom Texas Instruments C2000 microcontroller daughter card—as shown in Fig. 4.7—design files are not included.

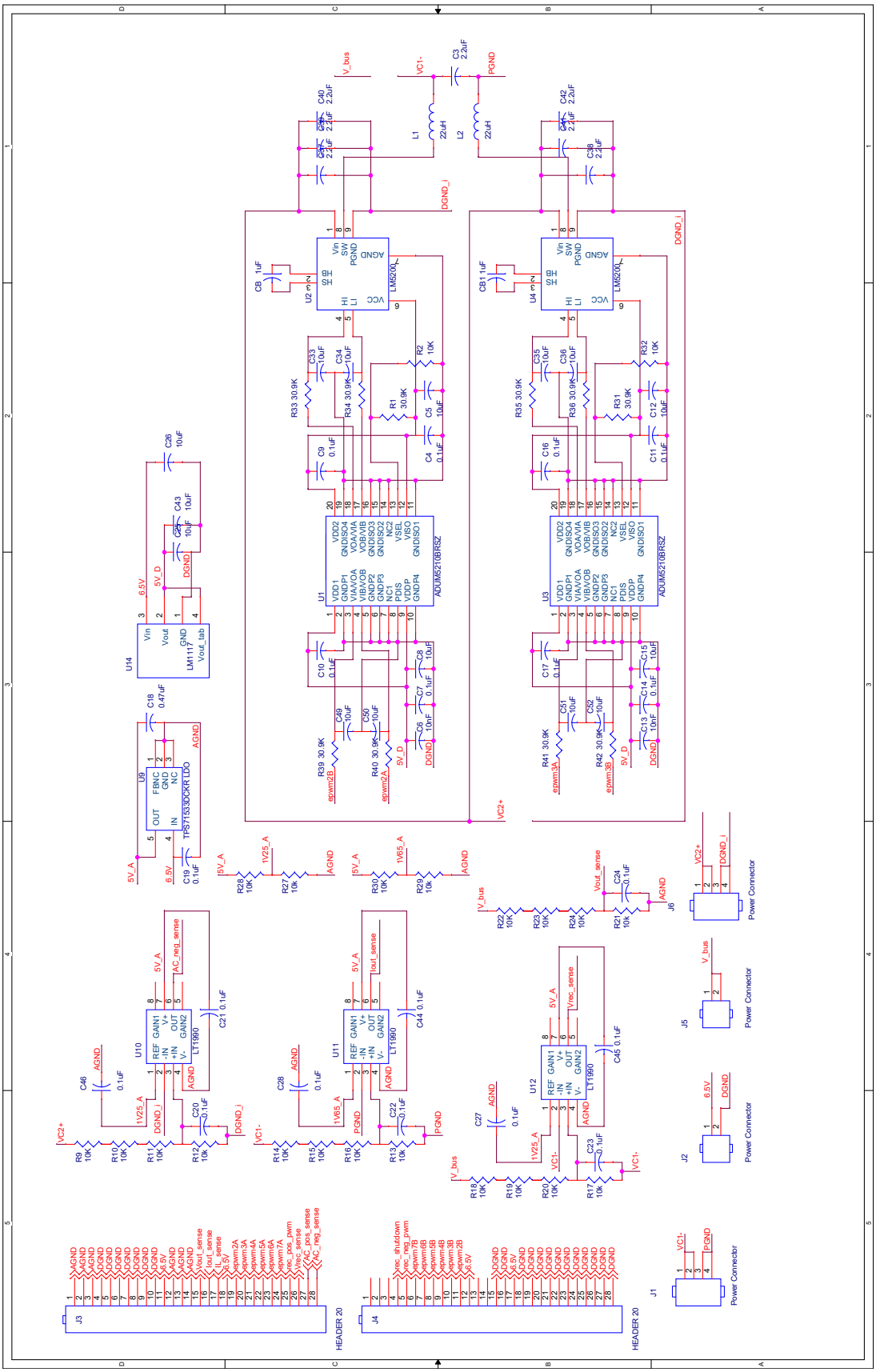


Figure A.1: PCB schematic of SSB hardware prototype in Chapter 4.

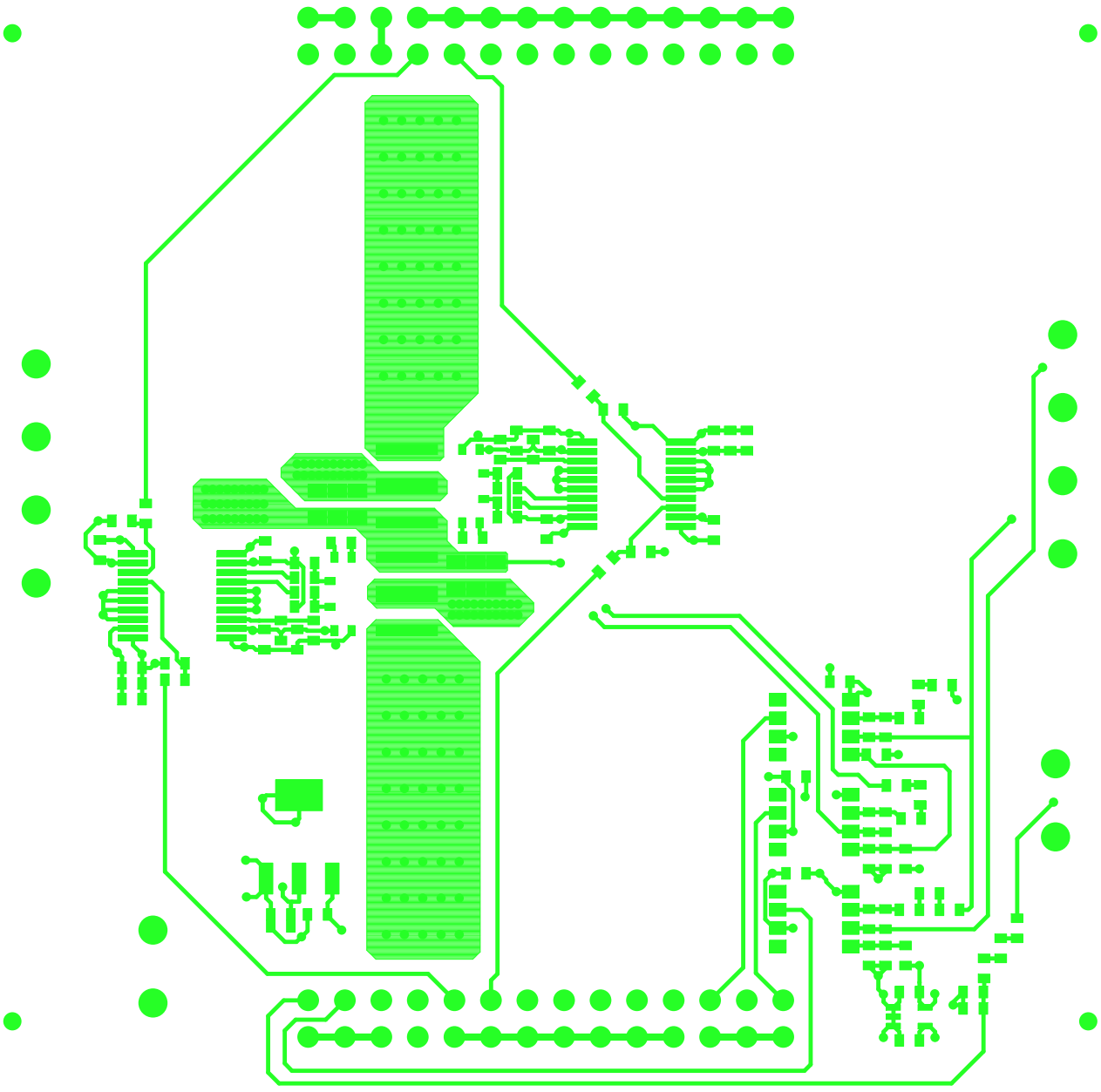


Figure A.2: PCB layout top layer of SSB hardware prototype in Chapter 4.

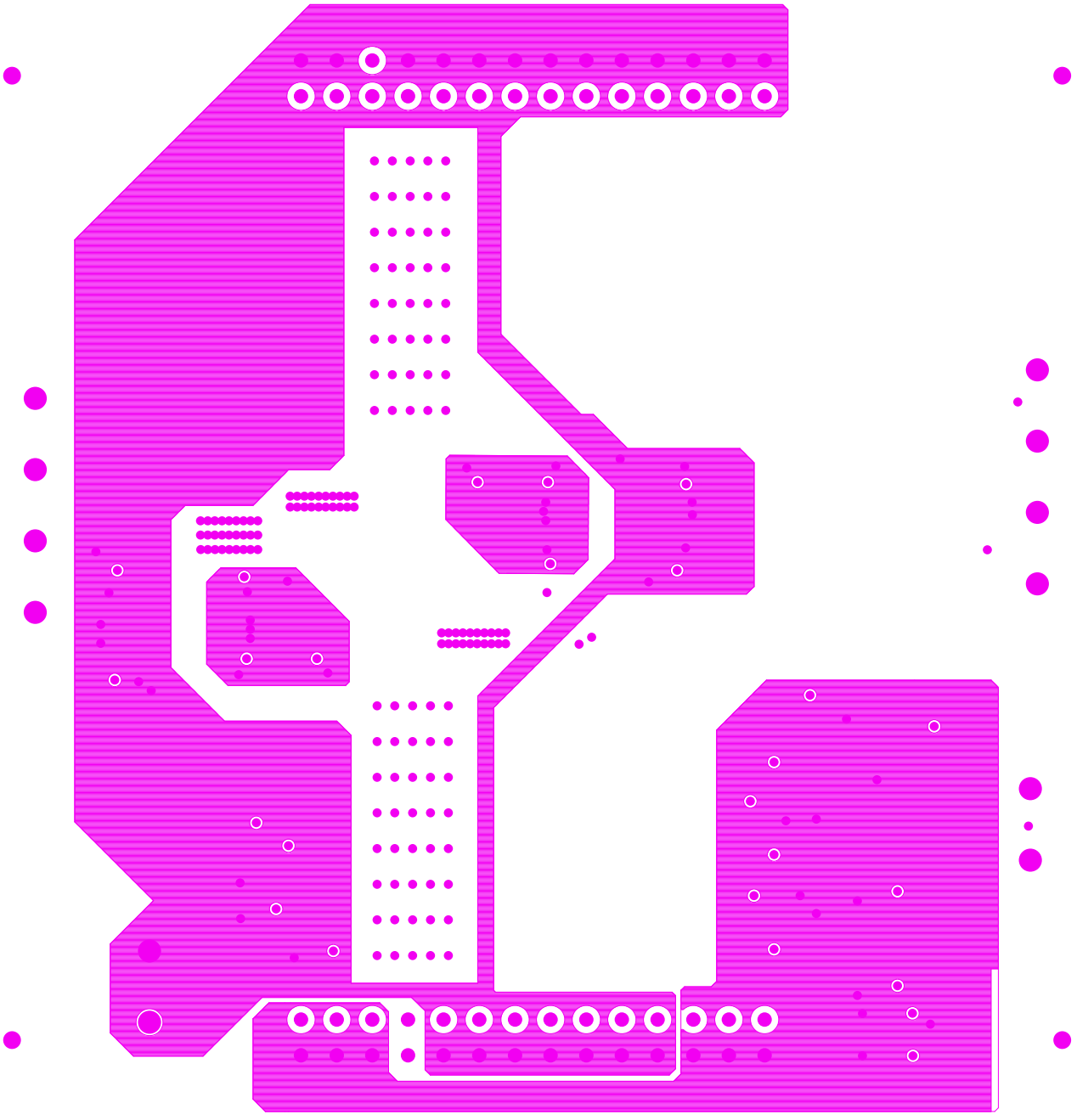


Figure A.3: PCB layout inner layer 1 of SSB hardware prototype in Chapter 4.

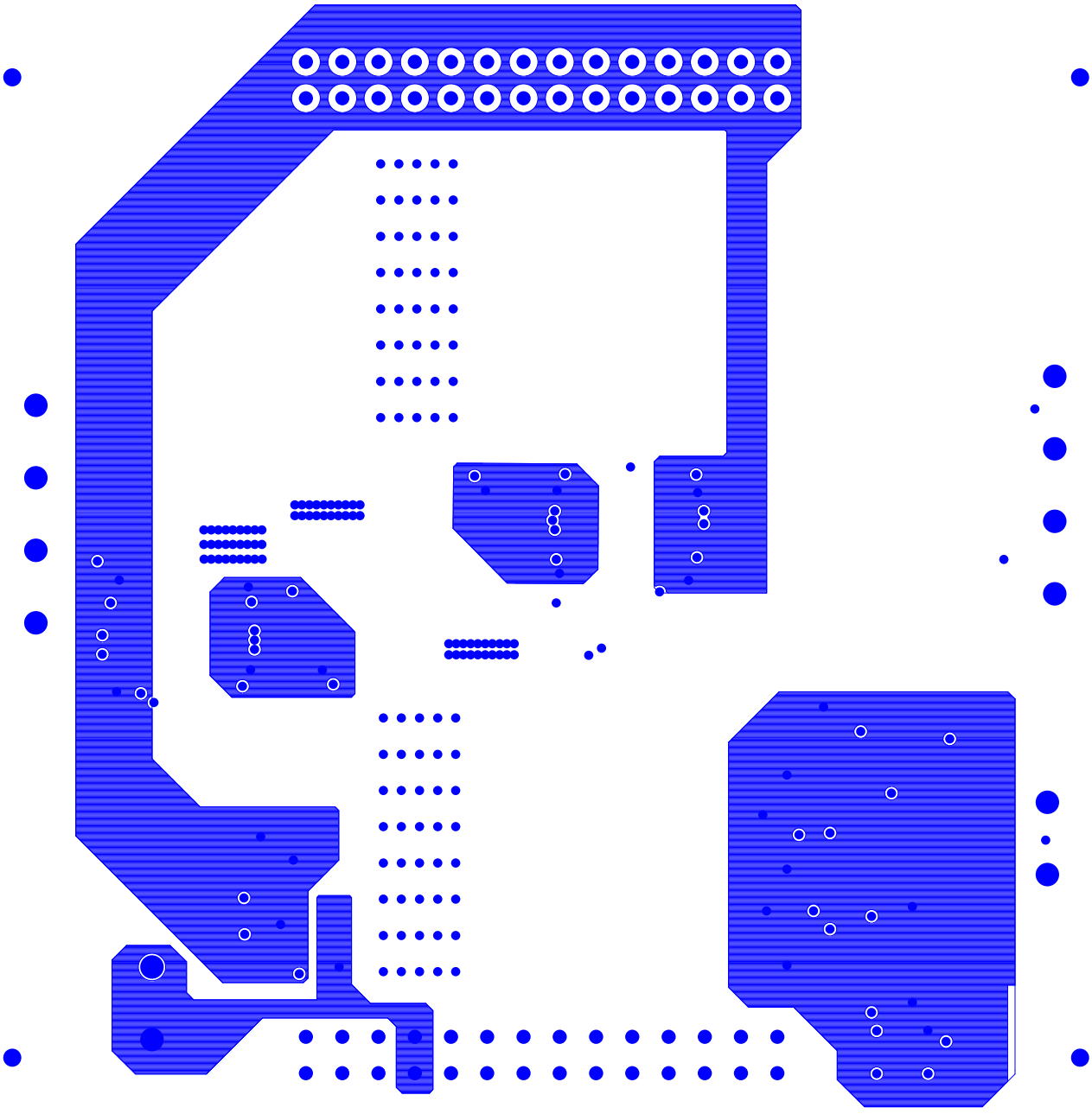


Figure A.4: PCB layout inner layer 2 of SSB hardware prototype in Chapter 4.

Figure A.5: PCB layout bottom layer of SSB hardware prototype in Chapter 4.