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Constraint-Aware, Scalable, and Efficient Algorithms for
Multi-Chip Power Module Layout Optimization

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy in Computer Engineering

by

Imam Al Razi
Bangladesh University of Engineering and Technology
Bachelor of Science in Electrical and Electronic Engineering, 2016

August 2022
University of Arkansas

This dissertation is approved for recommendation to the Graduate Council.

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Abstract

Moving towards an electrified world requires ultra high-density power converters. Electric vehicles, electrified aerospace, data centers, etc. are just a few fields among wide application areas of power electronic systems, where high-density power converters are essential. As a critical part of these power converters, power semiconductor modules and their layout optimization has been identified as a crucial step in achieving the maximum performance and density for wide bandgap technologies (i.e., GaN and SiC). New packaging technologies are also introduced to produce reliable and efficient multichip power module (MCPM) designs to push the current limits. The complexity of the emerging MCPM layouts is surpassing the capability of a manual, iterative design process to produce an optimum design with agile development requirements. An electronic design automation tool called PowerSynth has been introduced with ongoing research toward enhanced capabilities to speed up the optimized MCPM layout design process. This dissertation presents the PowerSynth progression timeline with the methodology updates and corresponding critical results compared to v1.1. The first released version (v1.1) of PowerSynth demonstrated the benefits of layout abstraction, and reduced-order modeling techniques to perform rapid optimization of the MCPM module compared to the traditional, manual, and iterative design approach. However, that version is limited by several key factors: layout representation technique, layout generation algorithms, iterative design-rule-checking (DRC), optimization algorithm candidates, etc. To address these limitations, and enhance PowerSynth's capabilities, constraint-aware, scalable, and efficient algorithms have been developed and implemented. PowerSynth layout engine has evolved from v1.3 to v2.0 throughout the last five years to incorporate the algorithm updates and generate all 2D/2.5D/3D Manhattan layout solutions. These fundamental changes in the layout generation methodology have also called for updates in the performance modeling techniques and enabled exploring different optimization algorithms. The latest PowerSynth 2 architecture has been implemented to enable electro-thermo-mechanical and reliability optimization on 2D/2.5D/3D MCPM layouts, and set up a path toward cabinet-level optimization. PowerSynth v2.0 computer-aided design (CAD) flow

has been hardware-validated through manufacturing and testing of an optimized novel 3D MCPM layout. The flow has shown significant speedup compared to the manual design flow with a comparable optimization result.

Acknowledgements

First, thanks to the Almighty Creator who has showered blessings throughout my life and has enabled me to complete this dissertation. Then, I would like to express my heartiest gratitude to my dissertation director, mentor, research, and academic advisor, Dr. Yarui Peng for his continuous direction, support, and efforts over the last five years. I have learned a lot from his invaluable expertise and guidance. His constructive advice and critiques enabled me to improve my research from time to time. Without his supervision and encouragement, this dissertation would not have materialized. Thanking him would not be enough for the knowledge I have learned from him. I would like to thank Dr. Alan Mantooth for his guidance, and feedback throughout my research works. His expertise has always helped me towards shaping myself as a better researcher. Also, his strong network and popularity in the power electronics society have helped me to achieve attention in different places. Thanks to Dr. Jia Di and Dr. David Andrews for taking time out of their schedules to participate in the committee for this dissertation. Moreover, I have learned a lot from their courses, which helped me to lay the foundation for CAD research as well as a computer engineer. I am really grateful for all the help and cooperation I have received from them for the last five years. Also, I want to thank Dr. David Huitink for his suggestions and helps with my research progress. I want to extend my gratitude to Dr. Brajendra Panda, our graduate coordinator, who has directed me in every formal step towards graduation and also taught several courses, which helped me in earning my degree as well. Also, I would like to thank Tom Vrotsos for his suggestions during the early stage of this disseration work.

I would like to thank my parents, my wife, my sister, and other family members, who have supported me in every step to achieve this goal. It would not have been possible for me to finish this degree without all of them. I am grateful to have such a supporting family.

I would like to express my great appreciation to my colleagues, Quang Le, Tristan Evans, and Shilpi Mukherjee, who helped me from the beginning of my research. They have guided me with valuable resources to make the onboarding very smooth. Quang's support on the research and development works helped me a lot to improve my skills. Besides, Tristan's and Shilpi's

suggestions have helped me to improve my writing and presentation skills a lot. I would like to thank Joshua Mitchener for helping with the PowerSynth v2.0 GUI development. I would like to mention MD Arafat Kabir, who has been very helpful in both my academic and personal life. As a former lab-mate, he helped me on brainstorming, coding, and many other technical issues. His in-depth technical knowledge in engineering and technology encourages me a lot to be a better tech-enthusiast. Also, I would like to thank Dr. S M Nahian Al Sunny, and Dr. Md Rakib Shahriar for their help with my programming skills improvement. I want to thank students from the UA power group especially Dr. Md Hazzaz Mahmood, Md Bakhtiyar Nafis, Ange Iaradukunda, Dr. Mahsa Montazeri, Ahmed Rahouma Fares Rahouma, Yuheng Wu, Yuqi Wei, Andrea Wallace, David Gonzalez Castillo, Hao Chen, Md Jabed Hossain, Dr. Yuxiang Chen, Reece Whitt who helped me throughout the manufacturing and testing of the power modules. Also, I would like to thank Md Asif Imran Emon for helping me with his power module packaging and testing expertise.

I want to express my gratitude to the National Science Foundation (NSF) funded research center Power Optimization of Electro-Thermal Systems (POETS) and the Army Research Lab (ARL) for supporting the projects that led to this dissertation. POETS has been a great platform for me to develop and improve my communication, technical, and behavioral skills. POETS helped me to improve my research quality through the Annual meetings and Tech conferences in every year, where I interacted with a lot of experts from both academia and industry.

Finally, I would like to thank Bangladeshi students and community people who have made my life in Fayetteville, AR very happening and eventful. Dr. Samrat Nath is one of the kind-hearted persons I have ever seen, who helped me to settle down in Fayetteville, AR.

Dedication

To my mother, who always cares for me

To my father, who always believes in me

To my sister and brother-in-law, who always inspire me

To my beautiful wife, who has been by my side supporting me in every step of my career

This thesis and all of my achievements are the results of the care, support and sacrifices from you all. Without your continued belief in me and prayer to succeed, I would not be where I am today.

I LOVE YOU ALL

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Chapter 1

Introduction

Power electronics systems and components are an inevitable part of the modern world. Recent advancements in electric automobiles, aircraft, smart grids, and consumer devices all require next-generation power conversion circuits and systems with extremely high density, efficiency, and reliability [1, 2, 3]. The demand for a more-electric world has initiated a call for high-density and reliable power conversion circuits and systems. Designing these converters is a sophisticated multi-physics problem, which requires joint efforts from the users, researchers, and manufacturers of energy conversion systems to solve. Continuous research and development are ongoing to address the challenges associated with the design process and improve the efficiency of the systems. Researchers from both academia and industries are working on the different hierarchies of these power electronic equipment to push the power density higher and higher. Therefore, power electronics designers are trying to cope with a higher complexity resulting from the shortening of product development cycles and increasing use of power electronics with the demand for more tailored solutions [4]. Design automation has been identified as the key to addressing these emerging challenges and adapted by researchers from all the branches such as devices, components, systems, grids, etc. Innovative, automated design tools and methodologies are emerging in all different areas of power electronics society.

1.1 Design Automation in Power Electronics

To optimize different power electronic components and systems, researchers propose design automation methodologies. For example, for effective thermal management solutions, heat sink design and optimization is very crucial. A lot of heat sink design optimization works can be found in the literature [5, 6, 7, 8]. In [8], authors have developed a rapid design optimization tool for liquid-cooled heat sinks based on reduced-order models for the thermal-hydraulic behavior. Their tool-generated solution has reduced the SiC junction-to-coolant thermal resistance by 25% for the

same pressure drop compared to an aggressive state-of-the-art single-phase liquid cooling solution for commercial silicon carbide (SiC) power module. Another significant component of power electronic equipment is the electromagnetic interference (EMI) filter, which design needs to be optimized very carefully to increase the power density of the system. Among several efforts [9, 10, 11] in EMI filter design optimization methodologies, the authors from [11] have developed an automatic design method for EMI filters aiming at volume and weight reduction and satisfying the electromagnetic compatibility standards. They have obtained a reduction of 56%, 67% in weight, and about 46%, 62% in volume in two case studies, respectively. Design automation has been adopted by the power converter designers as well. New design and optimization methodologies can be studied [12, 13, 14, 15, 16] from the literature on different converter topologies. For example, a generic and automated RMS current-oriented optimal design tool is developed in [15] for the LLC resonant converters used in renewable energy applications. This tool-optimized converter has achieved a 2.14% efficiency improvement over the traditional design method.

Researchers have been applying machine learning (ML) and artificial intelligence (AI) algorithms to improve the efficiency of the design cycle in the power electronics domain. These efforts are computer-aided and can achieve significant speedup compared to the traditional design process, thus falling into the design automation track. ML/AI-based techniques are widely used in component-level [17, 18, 19], system-level [20, 21, 22], and grid-level [23, 24] design problems. In [17], three nonlinear machine learning-based models are constructed to automatically estimate the junction temperature of the IGBT module to predict the reliability of the module, which can be used in module layout design automation to accelerate the design cycle. ML-based estimators can be used to reduce the computational expense associated with dc-dc converter characterization in the design and optimization problem of power electronics systems [20]. The authors have shown that system optimization approaches using ML estimators can generate power electronics systems with efficiency and size within 15% of systems are designed using high fidelity but computationally expensive models using test cases. Authors from [23] identified the need for

AI/ML-based prediction techniques for a resilient and reliable power electronics-dominated grid. ML algorithms are widely used in load forecasting, fault detection, and cyber-physical security of the grids.

Based on the aforementioned literature, it is clear that design automation is an emerging area in power electronics that can speedup the design optimization process of the equipment. Therefore, targeting designers, tool providers including simulation, physical design and design for reliability, manufacturers of test and characterization equipment for high power, high voltage systems, and researchers in universities and research labs working on power electronic design automation. Since MCPMs are the fundamental components of the power converters, design automation methodologies are obvious for optimizing them. This dissertation focus on such methodologies, and the rest of the content is centered around MCPM layout design and optimization.

1.2 Need for Design Automation in MCPM Layout Optimization

The design and packaging evolution of MCPMs are happening by integrating wide bandgap (WBG) devices (e.g., SiC/GaN) and passive components [25, 26, 27]. WBG devices are beneficial for power modules because of their reduced switching time and correspondingly higher switching frequency and lower losses [28]. However, the advantages of SiC devices cannot be utilized fully due to the impact of the parasitic inductance of the module. The inductance in the power loop coupled with the high di/dt of the SiC devices introduces higher voltage overshoot, increased switching losses, and electromagnetic interference and compatibility issue [29]. The switching loss mismatches among different devices on the same switching position would cause the temperature distribution uneven, and ultimately derate the performance and lifetime of the module. Therefore, novel packaging and design techniques are introduced to minimize parasitics, improve cooling, increase power density, and reduce voltage overshoot [30, 31, 32]. These techniques include integrating multiple substrates into a single package, flip-chip wire bondless modules, and packaging heterogeneous components like gate drivers, heat sinks, thermal sensors

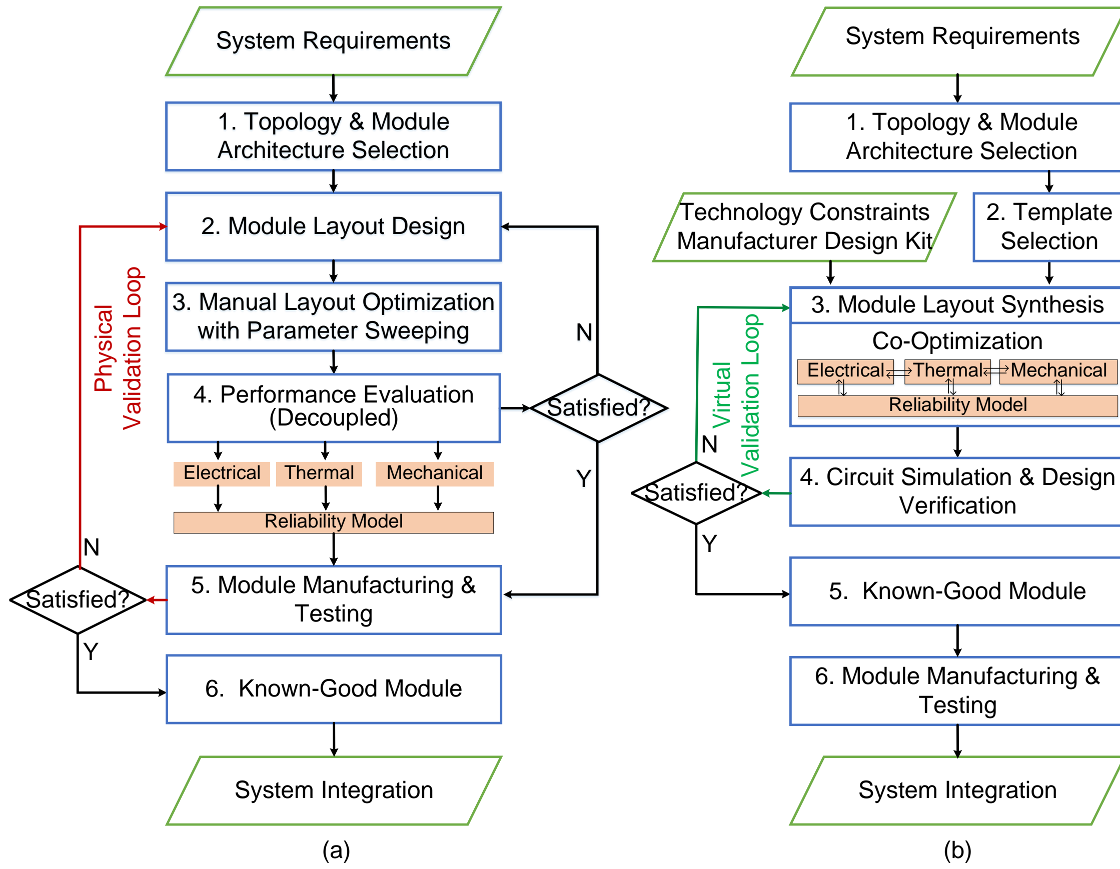


Figure 1: Power module design flow: (a) traditional vs. (b) automated

and switches, decoupling capacitors along with power devices. These advances in the power electronics industry have enabled power conversion design with enhanced efficiency, compact physical structure, and higher reliability [33]. Among different steps of the module design, layout design and optimization are very critical due to the high degree of design freedom and wide range of applications [4].

The current power module design process is a manual, repetitive, tedious task that requires expertise in several tools and software [34, 35]. To come up with a satisfactory solution, the designer requires several iterations of finite element analysis (FEA) to account for changes in the trace orientation, device spacing, etc. Due to the conflicting nature of electrical, thermal, and mechanical aspects of a power module, one trial to improve one aspect affects the other one. Therefore, it generally takes at least four to six iterations in the industry for an expert to come up with a satisfactory design ready for fabrication [4]. There is no standard Computer-Aided Design

(CAD) tool available to verify real-world performance before manufacture. Once the module is fabricated and if the module does not perform according to expectation, a costly redesign is required. This causes a limited solution space and a long development period that is hard to fulfill the cost and time-to-market requirements [36]. It is evident that with the ever-growing complexity of the MCPM layouts, this manual and iterative design process is not capable of generating high-performance designs that are both cost and time-effective. Also, the solution space is often restricted due to limitations in engineering time. Therefore, the traditional, iterative design approach is unable to satisfy the ever-growing demands for optimized power modules with high power density. To reduce engineering time and cost, the industry is looking for electronic design automation (EDA) tools. Though the very large-scale integrated circuit (VLSI) industry has adapted the design automation concept for quite a long time, this concept is relatively new in the power electronics society. Traditional, manual design flow vs. the EDA tool-aided design flow comparison is summarized in Figure 1. A significant speedup can be achieved in the automated design flow as the electro-thermo-mechanical and reliability co-optimization is possible. Moreover, the virtual validation loop ensures the round trip engineering before fabrication, which can save prototyping costs as well. Considering the technology constraints in the manufacturer design kit (MDK) guarantees the manufacturable solution generation. Such benefits can be achieved from an EDA tool that has a scalable, efficient, and generic layout synthesis engine and reduced-order, hardware-validated, accurate models to evaluate electro-thermo-mechanical and reliability performances.

1.3 MCPM Design Variations

To categorize the existing MCPM designs, the number of routing and device layers present in a design is considered. Based on these criteria, the MCPM designs are classified into three types: 2D, 2.5D, and 3D. To clearly define these types of multi-chip power module layouts under this dissertation scope, an illustration is shown in Figure 2. A full-bridge MCPM circuit consisting of two half-bridge circuits is shown in Figure 2(a). A 2D layout refers to a single device layer, as

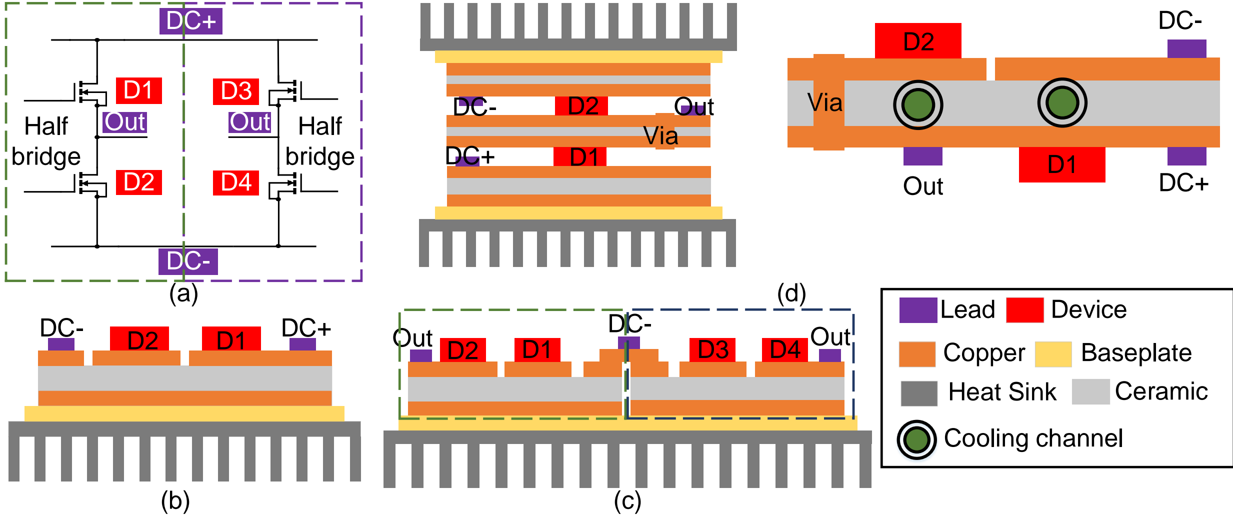


Figure 2: (a) Full-bridge power module circuit, cross sections of three MCPM structures: (b) 2D half-bridge, (c) 2.5D full-bridge, (d) 3D half-bridge

shown in Figure 2(b). Here, Figure 2(c) represents a 2.5D full-bridge layout, which is defined by multiple device-supporting substrates horizontally connected with additional routing resources. Finally, Figure 2(d) shows a 3D half-bridge module that consists of multiple devices and multiple routing layers stacked vertically. Vias are used for establishing vertical connections across different routing layers. Also, the device's gate and source connections can be performed through metallic posts, which can be treated as vias between two different layers. Due to the 3D stacking, the electrical performance has been improved, but thermal management has become a challenge. Double-sided cooling is one solution for face-to-face stacking of the devices as well as flip-chip devices. However, for face-to-back stacking (shown in Figure 2(d)), it requires at least four layers to form a half-bridge module with double-sided cooling, which increases the fabrication cost and complexity. To reduce fabrication complexity and cost, back-to-back stacking can be performed to create a half-bridge module with embedded heat sink/micro-cooler water channels between two DBCs [37]. Since different layout architectures are possible in 3D configurations, the design tool must handle all these variations.

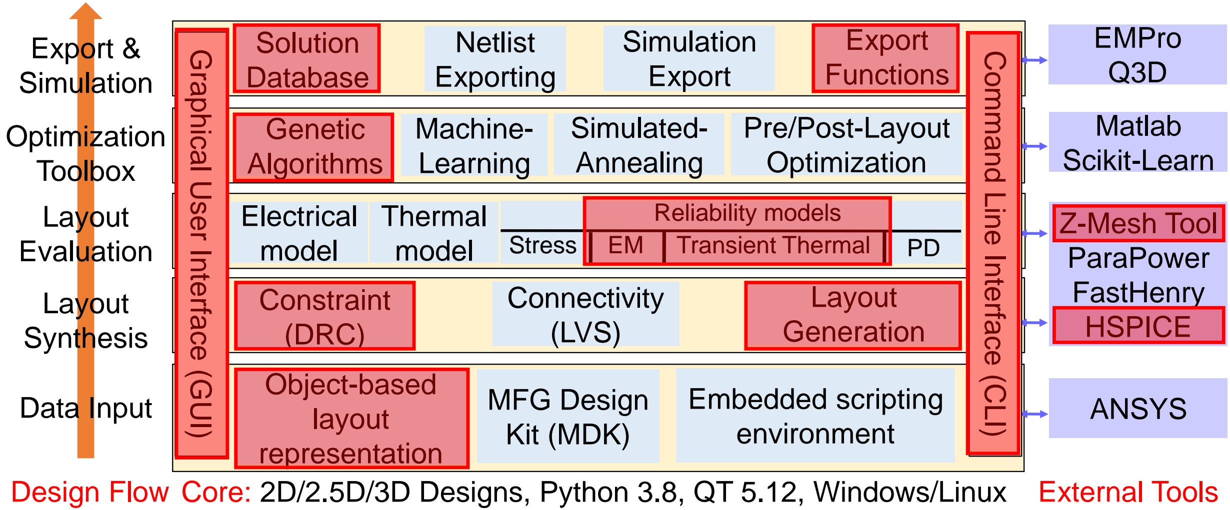


Figure 3: PowerSynth 2 architecture

1.4 Dissertation Contributions

The core contribution of this dissertation is a constraint-aware, scalable, and efficient layout engine for PowerSynth that can be used in multi-objective optimization for satisfying high power density requirements. There is no commercial tool available that can consider MCPM layout impact on performance optimization and intelligently search the solution space for satisfying the requirements for electro-thermo-mechanical and reliability aspects. Therefore, PowerSynth is the first tool offering all of these features in a complete package. This dissertation has not only addressed the limitations with PowerSynth v1.1 [38] but also introduced some new features in PowerSynth 2. PowerSynth 2 architecture (shown in Figure 3) is a modular and hierarchical one, which is laid out by Dr. Peng. This architecture is more flexible compared to previous versions that can interact with external tools through application programming interfaces (APIs). PowerSynth 2 architecture has a very generic and hierarchical design flow, which can be used for any power electronic component/system layout optimization. Therefore, this is the first proposed architecture in the power electronics design automation area, which design flow is generic enough to be easily applicable for any power electronic component or even system. In this dissertation, this architecture has been used for the MCPM layout optimization case and the contribution areas

have been highlighted in the architecture.

- **Layout Representation Technique:** An initial layout is required for any design automation tool to perform optimization. Some tools can generate the initial layout combining the circuit netlist and components template library [36], whereas some tools require the initial layout from the user in terms of some abstraction method or detailed description. PowerSynth v1.1 considered symbolic layout method as an abstraction technique, whereas PowerSynth 2 needs the detailed layout information through a text script. Each method has pros and cons. For example, the netlist with a template library can generate different initial layouts based on the templates and find an optimum layout for further optimization. However, this method is limited by the template library as these libraries are not editable by the user. Therefore, the methodology becomes very application-specific. The methodology cannot be extended easily across different component/system layout optimization. The symbolic layout is a user-friendly and simple method for taking the initial layout as input. However, the complex geometry and non-collinear components cannot be represented through this method. PowerSynth 2 requires a hierarchical text script with a layer stack and manufacturer design kit (MDK) to describe the initial layout geometry. This script introduces an object-based layout representation technique, which is generic and scalable enough to represent any component/system. However, the drawback with such script is it cannot overcome any connectivity error introduced by the user while declaring the script. If the script is not representing the circuit netlist, the layout engine cannot detect that, and hence can generate wrong solutions. To consider more generic layout description technique, an embedded scripting environment with power electronics hardware description language is required.

- **Layout Generation Methodology:** DRC-clean solution generation is a must for an MCPM layout optimization tool. The sequence pair method is used in [39] for layout generation, where the layout is mapped into a 1D binary string for introducing variations in the solution space. However, due to the simplified geometrical representation, lack of interconnection,

and constraint information, the method requires a tedious DRC process and is hence inefficient for handling complex geometries. In PowerSynth v1.1, the matrix-based layout generation methodology does not consider the design constraints in the layout generation phase, which leads to ignoring a lot of solutions due to DRC violation. PowerSynth v1.3 has first introduced the constraint-aware layout generation methodology, which considers the design constraints in the layout generation phase and eliminated the tedious DRC step. This constraint graph methodology has been adapted by [36] as the method has been proven to be efficient. However, their methodology is still limited to 2D layout solution generation only as they did not consider hierarchical evaluation methodology. PowerSynth v1.9 can handle all 2D/2.5D Manhattan geometries by considering hierarchical corner-stitching data structure with constraint graph evaluation technique. Corner-stitching data structure has been proven to be efficient to derive the design constraints easily. PowerSynth 2 layout engine can handle all 2D/2.5D/3D Manhattan layouts. The baseline algorithms from v1.9 have been updated to handle inter-layer connections (i.e., via). The fixed dimension handling algorithms have been generalized to consider all types of edges in a generic way. This methodology has a linear time complexity with the number of components in the layout that makes the methodology scalable. Also, PowerSynth 2 methodology can generate minimum-sized, variable-sized, and fixed-sized solutions, whereas most of the other methodologies are capable of generating only fixed-sized solutions, and [36] can also generate the minimum-sized solution as they are using constraint graph approach inspired by PowerSynth works.

- **Improved User Experience:** One of the outstanding features that PowerSynth 2 has the user interfaces. Both graphical user interface (GUI) and command-line interface (CLI) are available for the user's flexibility. The other methodologies in literature did not clearly disclose their user interfacing method. The initial layout geometry description script is updated to make it more user-friendly. With help from Joshua (a formar REU student), an interactive GUI has been developed for PowerSynth 2. The command line interface for

PowerSynth v1.9 and v2.0 has been developed with help from my colleague Quang Le.

- **Reliability Modeling Efforts:** Electrical and thermal performance optimization is necessary for safe operation of SiC MCPM modules at high switching frequency. So, all of the other research groups have tried to develop electrical and thermal models. However, no one considered layout impact on other reliability metrics like transient thermal performance, electromigration associated risk assessment, partial discharge, performance at high-voltage-current, etc. Besides electro-thermal performance models, reliability modeling efforts are initiated in PowerSynth 2. A transient thermal model has been developed for 2D layouts that can predict both static and transient thermal performance with about 3500 times speedup while keeping the accuracy within 10% compared to ANSYS Fluent. Also, an electromigration-aware reliability model is proposed in [40] to assess the risk of different interconnects and optimize accordingly. The new layout engine has been enabled PowerSynth 2 to handle both wire bonds and solder bumps, whereas the other tools can handle only wire-bonded layouts. Therefore, such reliability modeling study is possible with PowerSynth 2.

- **Optimization Algorithms:** Optimization algorithm is one of the key parts of the CAD flow. The other works from the literature have considered only genetic algorithm (NSGAII [41]) as the optimization algorithm candidate. Though NSGAII can converge faster, it has certain limitations: Many generations are required before convergence; the distribution of the weights to the objectives is complicated; generated solutions are not guaranteed to be globally optimum; solution space is not large enough. Therefore, PowerSynth 2 has an exhaustive search option (Randomization) for optimization alongside the NSGAII option. Though off the shelf NSGAII python package has been used, the design string formulation and modification algorithm has been developed and generalized for PowerSynth 2 layout engine to consider 2D/2.5D/3D MCPM layouts.

- **Hardware-Validation of CAD Flows:** The generic CAD flow for 2D/2.5D/3D MCPM

layout optimization has been validated with brand-new 2D/2.5D design and 3D design cases. For both cases, the initial module layout is optimized for electrical and thermal performance. An optimized solution for both cases has been fabricated and tested for result comparison. In 2D/2.5D case, PowerSynth prediction is within 10% for both electrical and thermal, whereas for 3D case, those are within 13%, and 10%, respectively. Though the other tools have also verified their optimized designs with hardware prototype, efficiency and capability wise PowerSynth 2 is way ahead of them. For example, the hardware-validated 2D module can be found within 1288 s by iterating for 100 generations of NSGAII in PowerSynth 2, whereas the the methodology in [36] took almost 5,400 s for 30 generations, and [42] took 266,343 s for 10 generations of NSGAII. Performance-wise all the solutions are comparable, as PowerSynth 2, [36], and [42] has achieved 8.33, 5.59, and 7.44 nH of power loop inductance. The layout from [36] has a lower loop inductance as that layout has two parallel power loops, whereas the others have a single loop.

1.5 Contributions from Other Team Members

Apart from the highlighted parts in the PowerSynth 2 architecture, other components are required to complete the design flow. My colleagues are working on those parts. A brief summary of their efforts is summarized below.

- My colleague Quang Le has helped me with the electrical modeling efforts, user interfacing, external APIs development, and hardware-validation of the CAD-flows. He has built the interfaces for all of the electrical performance evaluations. In the case of 2.5D MCPM hardware validation, the PEEC model [43] is developed by Quang. Also, the netlist extraction methodology that is used in [44] is solely developed by Quang. Thanks to his enormous contribution to PowerSynth 2 code base that has made my layout engine results get validated. Besides, his contribution toward the solution export, database maintain features have played an important role in this dissertation. The electrical performance validation work for the 3D module would not be possible without him.

- Another colleague Tristan Evans has been working on ParaPower interfacing, EMI modeling, electro-thermo-meachanical co-optimization study, and layout synthesis from input netlist. Among his several contributions the ParaPower integration effort has made it possible to evaluate the 3D MCPM design [45]. Also, he has helped in many ways to validate the thermal performance of both 2.5D and 3D modules.

- Another team member, Shilpi Mukherjee has been working on partial discharge (PD) modeling and post-layout optimization feature like filleting the sharp corner to minimize the current crowding and field focusing. She has helped a lot to test the high-voltage-current dependent reliability constraints implementation as those constraints are obvious at high power operation and reduce partial discharge threats.

- Last but not the least, Joshua Mitchener (former REU student) has helped to put together the GUI for PowerSynth 2. His works are summarized in [46].

Therefore, it is clear that without the other team members' enormous support and contributions this dissertation would not be possible. Finally, combining all the team efforts, we have been able to release binary packages for different versions of PowerSynth. All of these packages can be found in [47].

1.6 Dissertation Outline

Since this dissertation includes the updates after the PowerSynth v1.1 release, the goal of this dissertation is to present the background, methodology, and results starting from PowerSynth v1.3 to v2.0. The dissertation outline is as follows.

- **Chapter 2** represents a detailed literature review of design automation efforts in MCPM layout synthesis and optimization area. PowerSynth v1.1 research and development history is also summarized in this chapter.

- **Chapter 3** contains the motivations behind this dissertation. Also, the progression flow

from PowerSynth v1.1 to v2.0 is summarized in this section along with the preliminary research works that laid the foundation of PowerSynth 2.

- **Chapter 4** describes the MCPM layout optimization flow and validation results for PowerSynth v1.9, which is released for handling 2D/2.5D MCPM layouts. The methodology, key results, and limitations of v1.9 are stated in this chapter.
- **Chapter 5** includes the PowerSynth 2 architecture description including the updated methodology, results, and limitations.
- **Chapter 6** represents the reliability optimization efforts using PowrSynth updates in layout generation and modeling efforts. Both thermal and electromigration-aware reliability optimization methodology and results are presented.
- **Chapter 7** concludes the dissertation with some potential future works.

Chapter 2

Literature Review

Realizing the importance of an EDA tool for MCPM design and optimization, several research groups have been working on this topic. Since both analog/mixed-signal and power electronics design processes are manual and iterative, researchers from both societies have been adapting the design automation methodologies from VLSI as the EDA tools for digital IC design are highly matured compared to the others [48]. The similarity between VLSI and analog CAD flow has led a large group of researchers towards developing different CAD tools for analog/mixed-signal layout design automation to address critical challenges like handling device parameterization, constraint generation, maintaining symmetrical placement and routing, etc. [48, 49, 50, 51]. Unlike analog and digital CAD flow, Power-CAD [52] requires simultaneous analysis of thermal, electrical, and mechanical parameters to design an optimal layout. As such, recently, design automation tools with multi-objective optimization have been investigated by the power electronics society to explore a large variety of designs, reduce cost and computational effort, and alleviate design complexity. A brief literature review on MCPM layout synthesis and co-optimization (Step 3 in Figure 1(b)) efforts are described below.

2.1 MCPM Physical Design Automation and Optimization Efforts

2.1.1 Existing Works Outside PowerSynth Scope

In [53], the authors proposed an automatic layout generation method to consider a legitimate trade-off between electromagnetic compatibility (EMC) and thermal constraints. A simplified EMC and a thermal model are applied individually to generate a "Thermal-EMC" plane with Pareto-front solutions. Though the proposed method may determine a theoretical optimum solution for a given technology, it is hindered by limited solution space and design rule violations.

In [54], a sequentially coupled approach is proposed for optimizing power module layouts by integrating a few FEA modeling tools (e.g., ANSYS). These tools are coupled in a

multidisciplinary design optimization (MDO) framework to interact with each other while generating solution layouts. Though the methodology has been proven superior to the traditional manual design flow, some limitations like the time-consuming finite element method (FEM) for electro-thermal evaluation, few design variables in the solutions, and a single variable in each iteration of the optimization make this methodology infeasible for 2.5D/3D layout optimization.

Another research also adapted the placement and routing concept from the VLSI design automation area and implemented it in power electronics design automation [39]. The components like die, wire bonds, and connected traces are merged into a single rectangle to simplify the problem. Relative position, component orientation, and the gap among components are translated into a binary string, which is manipulated in the optimization phase to generate new solutions. Two-folded optimization is performed by a genetic algorithm, where the outer loop aims at placement optimization via the sequence pair method [55], and the inner loop focuses on routing. The optimization cost function involves only footprint area and electrical parasitics, which arises concern about the thermal reliability of the solutions. Also, simplified representation saves computation time by sacrificing accuracy in calculating parasitics. Though the methodology has been extended to 3D layout optimization [56], no hardware validation has been presented even with a simplified technology.

In [42], researchers have developed a genetic algorithm-based multi-objective electro-thermal optimization framework, where only the device placement varies with a fixed routing of the traces. FEM tools are used for electro-thermal performance evaluation. Though the proposed methodology can optimize the device placement, the trace routing impact is not considered, resulting in a smaller solution space. Moreover, the time-consuming FEM solver is infeasible for rapid design space exploration of the high-density and heterogeneous layouts.

Authors from [36] developed an MCPM layout optimization method that uses a graph model to describe heterogeneous layouts with all interconnectivity and design constraints. Integer programming is introduced to generate layout templates with variable geometric topologies from the initial graph model. An in-house discrete extractor is used for evaluating loop and branch

inductance, and thermal resistance. This extractor is leveraged to achieve the Pareto-front from the genetic algorithm providing a tradeoff boundary for loop inductance and branch mismatch. This methodology does not require a complete initial input layout from the user as it generates the initial layout based on the user's choice from the template library. However, the methodology is very application-specific with a limited number of components handling capability. The integer programming method is not scalable as with the number of increasing components, the runtime exponentially increases and it may face convergence issues in some cases. Moreover, the proposed methodology is applied and verified through a 2D design. Any 2.5D/3D module is not optimized and verified with the methodology.

2.1.2 Preliminary Research and Development Efforts on PowerSynth

The initial work in [52] has introduced a simultaneous electro-thermal optimization methodology named "Power-CAD" for design, analysis, and optimization of a discrete power module. Power-CAD has been proven to be both cost and time-effective for the power module design industry by significantly reducing the number of design cycles. However, this methodology treats the maximum temperature in the module as a constraint without considering the trade-off between electrical parasitics and temperature. Realizing the significance of considering the balance between electrical and thermal performance, the foundation of PowerSynth is established in [57]. The very early version of the tool provides a flexible framework for synthesizing not only half-bridge MCPMs but any circuit topology, and able to generate a set of optimal trade-off MCPM designs considering any number of thermal or electrical performance criteria. The reduced-order electrical and thermal models used in this version are built based on the study from [58]. The models require an initial layout design and a layer stack to start with. Then, a thermal behavior extraction tool like ANSYS Workbench is used to create the lumped thermal model. An electrical parasitic extraction tool like Ansoft Q3D Extractor, is used to create a lumped electrical parasitic model. The limped thermal model is a Cauer thermal network, which allows 1D heat dissipation and requires characterization by FEM tool. The electrical model

considers the MCPM structure as a micro-strip structure and uses staight-forward micro-strip equations for parasitic modeling. However, the assumptions like infinite ground plane and very thin, large traces are not valid for accurate modeling effort and results in mismatches with FEM results. Including these efforts, an internal release of PowerSynth v1.0 is done in 2015. After a few more years of research and development effort, a complete EDA tool "PowerSynth" for MCPM layout optimization was presented in [38]. Since ANSYS tools require licensing, the characterization for thermal modeling is done by open source GMesh [59] and Elmer [60] tools in this version. To address the limitations with micro-strip method, a response surface-based method [29] is used for electrical parasitic modeling. Both of these models are hardware-validated in [38]. PowerSynth v1.1 release is performed in 2019 integrating these fast, accurate, hardware-validated electrical, and thermal models for MCPMs within a multi-objective optimization framework. PowerSynth v1.1 uses a symbolic layout for layout abstraction, which consists of lines and points representing traces, devices or lead connections with normalized coordinates. Then, each trace or component is stamped into a matrix representation to effectively update the trace dimension and component locations during the optimization process. It has a built-in technology library to account for a wide range of materials and design rules from the manufacturer. Another important capability is the back-annotation of layout-extracted parasitics to the original circuit schematic, which enables round-trip engineering before fabrication. Also, exporting 3D models to several commercial FEA tools are another must-have feature for detailed analysis. However, this layout generation method does not consider any design constraints during the layout generation phase. Therefore, once a layout is generated, it has to go through an iterative DRC checking process. In some complicated layout cases more than 90% layout solutions are discarded due to DRC failures. Also, this DRC step could be time-consuming on complicated 2D/2.5D/3D layouts with many heterogeneous components and limits geometric configurations due to many built-in assumptions. This dissertation is based on further research and development efforts of PowerSynth. Therefore, rest of the works are described in the following chapters.

A brief summary of comparison with this dissertation methodology and other most recent

MCPM layout optimization methodologies is provided in Table 1.

2.2 Power Modules' Reliability Optimization Efforts

The most dominating challenges for high-density modules are from the reliability perspective due to their highly inhomogeneous structures. The prominent cause of the failures like solder joint fatigue, wire bond fatigue, and isolation substrate delamination is thermal cycling [61]. Another reason behind most of the interconnect failures, especially at high-current density is electromigration (EM) [62]. Since different materials with different coefficients of thermal expansion (CTE) are used in an MCPM, CTE mismatch of the components leads to induced thermal stresses within the module that causes mechanical failures [63]. To reduce the failure rate and increase the reliable operation period of the modules, reliability optimization before fabricating a module is obvious. From the literature, two types of reliability optimization approaches can be found: a) Optimization aiming at specific failures [61, 63, 64], b) Optimizing thermal management aiming at reducing thermal cycling effects [65, 66, 67].

In the first approach, researchers have focused on a part (i.e., wire bond, solder joints, substrate) of the module rather than the module as a whole. Since this approach has a limited scope, physics-based modeling and finite element analysis produced helpful results for predicting failure and lifetime. Among different failure mechanisms, EM is one of the prevalent ones, especially at high-current density. EM is a material migration based on the flow of current through it, which is a diffusion-controlled process. Though high current density drives the migration process, high temperature also plays an important role in increasing the diffusion rate. Therefore, the combination of high current density and high temperature in the interconnect/solder material can cause very severe EM-induced failures that can affect the long-term reliability of the component. In the second approach, researchers have focused on the reliability of the module as a whole and tried to reduce thermal cycling effects by changing materials in the layer stack. In this approach, thermal management using phase change materials (PCM) have been found as a prevalent solution for reliability enhancement. For both of these

Table 1: Methodology and feature comparison with most recent MCPM layout design automation works

Methodology Features	Puqi Ning et. al. (2017) [39]	Shuhei et. al. (2021) [42]	Zhou et. al. (2022) [36]	PowerSynth 2 (Dissertation)
Initial layout	Simplified	Actual	Not Required	Actual
Optimization goal	Placement & routing	Die placement only	Placement & routing	Placement & routing
Layout generation method	Sequence pair	Parameter sweep	Integer linear programming & Block graph model	Corner stitching & Constraint graph
Layout types	2D	2D	2D	2D/2.5D/3D
Scalability	Yes	No	No	Yes
Interconnection technology	Wire bond	Wire bond	Wire bond	Wire bond, solder bump, via
DRC checking	Required	Not required	Not required	Not required
Hierarchical optimization	Not considered	Not considered	Not considered	Considered
Performance modeling	Discrete model	FEA	In-house models	In-house & External models
Reliability optimization	Not considered	Not considered	Not considered	Considered
Optimization algorithm	Evolution (GA)	Evolution (NSGA II)	Evolution (NSGA II)	Evolution (NSGA II) & Exhaustive (Randomization)
Release packages	Not available	Not available	Not available	Available [47]

approaches, the existing researches are based on FEA-based modeling and optimization.

2.2.1 Thermal Cycling Impact Minimization Efforts

In [63], authors have developed an optimization methodology that uses a mathematical function relating system response to design parameters. This process parameterizes the design variables within a permissible range that uses commercially available optimization packages to generate new solutions, simulated using the finite element method (FEM) tools. The design-for-reliability tool concept has been presented in [61] that has built-in reduced-order stress prediction models with numerical optimization. While optimizing a module, it can consider uncertainty data from material properties and manufacturing processes using a Monte Carlo method that provides a stochastic approach to reliability predictions.

Authors from [68] have proposed a design automation and optimization methodology based on FEM simulation to optimize the layer stack of a double-sided cooling power module. Several research groups have identified PCMs as an effective ingredient of the power module layer stack that acts as buffers against the intermittent temperature spikes from thermal cycling. In [67], authors have used PCM to reduce the peak temperature of the module under thermal cycling. In [66], authors have shown that PCM can be modeled as a voltage-controlled variable RC-network and verified the benefits of using PCM over encapsulant using such a network model.

2.2.2 Electromigration Impact Minimization Efforts

In [69], authors have studied the combined effect of high current and high temperature on Ag, Cu, and Au wire bonds through experiments. Authors of [70] performed an electrical-thermal-mechanical coupled analysis of electromigration in a bonding wire of a power module. A test method is developed for studying the current effect on the aging process of a wire-bonded Silicon Carbide (SiC) MOSFET module under a power cycling test in [71]. The experimental and analysis results showed that different current densities have different impacts on both the bond wire resistance and die-attach solder layer. This methodology is also an

experimental case study whose results can be used in validating the modeling effort for EM risk assessment. In [72], authors have tried to optimize the packaging structure of a flip-chip device by studying a few variations in solder material, solder bump diameter as well as pitch, and the drain connector geometry. All these variations are manually designed by the authors, and the module layout variation impact has not been studied. Therefore, the solution space is limited. Authors have studied a few solder bump distribution orientations in [73] to optimize the electromigration reliability by applying a more balanced current distribution among solder bumps. This trial is also a manual one and is limited by the designer's choice.

From the literature review, it is clear that there is no software tool exists that is scalable, efficient, and generic enough to perform electro-thermo-mechanical and reliability optimization on 2D/2.5D/3D MCPM designs. Most of the layout optimization methodologies are limited to 2D modules and cannot perform any reliability optimization. Design for reliability optimization toolbox for power electronic system has been introduced in [30], which is suitable for system-level reliability assessment. Therefore, no existing tool can perform reliability optimization accounting for thermal cycling and electromigration on power modules.

Chapter 3

Motivations and PowerSynth Progression Flow

3.1 Motivations

PowerSynth is the first tool that focuses on MCPM layout optimization. Though PowerSynth v1.1 has shown the complete optimization flow for simple 2D layouts as a proof of concept, there is room for improvements in the methodology associated with the layout optimization flow. The critical items include:

- **Layout Representation Technique:** Symbolic layout representation using lines and points is unable to represent the 2.5D/3D layouts, even some complex 2D layouts. The method restricts the wire bonding and trace routing orientation, and unable to handle multiple non-collinear components.

- **Layout Generation Methodology:** The matrix-based layout generation methodology has limited types of geometry handling capability. While generating solutions, it requires design rule checking (DRC) for each solution, which makes the methodology inefficient for a broader range of geometry handling.

- **Layout Engine Efficiency:** The layout engine generated solutions are not always DRC-clean, which shows a variable efficiency with a varying number of devices in the same layout. For example, in a half-bridge module, the number of parallel devices is varied from 4 to 12 with an increment of 2. For each case, total of 15,015 solutions are generated and among all cases, it generates a maximum of 20.47% DRC-clean solutions [74].

- **Reliability Modeling:** Since PowerSynth v1.1 cannot consider arbitrary layer stack and does not equipped with any transient thermal model, it cannot optimize layouts accounting for thermal cycling. The reduced-order, compact thermal model is not capable of capturing detailed temperature distribution that makes the tool incapable of assessing EM-associated

risk. Besides, the matrix-based layout generation methodology cannot handle user-defined/reliability constraints.

- **Optimization Framework:** A non-dominated sorting genetic algorithm (NSGA-II) [41] has been used for optimization since the matrix-based methodology is not compatible with some other optimization algorithms. Though NSGA-II can converge faster, it has certain limitations: Many generations are required before convergence; The distribution of the weights to the objectives is complicated; Generated solutions are not guaranteed to be globally optimum; Solution space is not large enough. These limitations initiated a study toward assessing the viability of other optimization algorithms. Also, for heterogeneous power module layouts, the layout complexity and number of design variables grow exponentially, which makes it difficult due to dependency between variables.

To address these limitations, a more generic, efficient, and scalable layout optimization methodology is required. Therefore, research and development have been carried out to improve PowerSynth from time to time. A brief description of the progression flow is described below.

3.2 PowerSynth Progression Flow

PowerSynth progression flow is shown in Figure 4. A brief feature comparison among different versions from v1.1 to PowerSynth 2 has been described in this section. Released packages of these versions can be found in the PowerSynth release webpage [47].

- **PowerSynth v1.1:** This version has the following key features: (1) Simple 2D layout geometry handling capability; (2) Symbolic layout representation; (3) Matrix-based layout engine; (4) Iterative DRC-checking; (5) A user-extensible technology library and manufacturer design kit (MDK); (6) Reduced-order electrical and thermal model validated against both FEA simulation and experimental measurements; (7) Back annotation of layout-extracted parasitics to the original circuit schematic; (8) Export of 3D structure of the 2D MCPM layouts to several commercial FEA tools for further analysis.

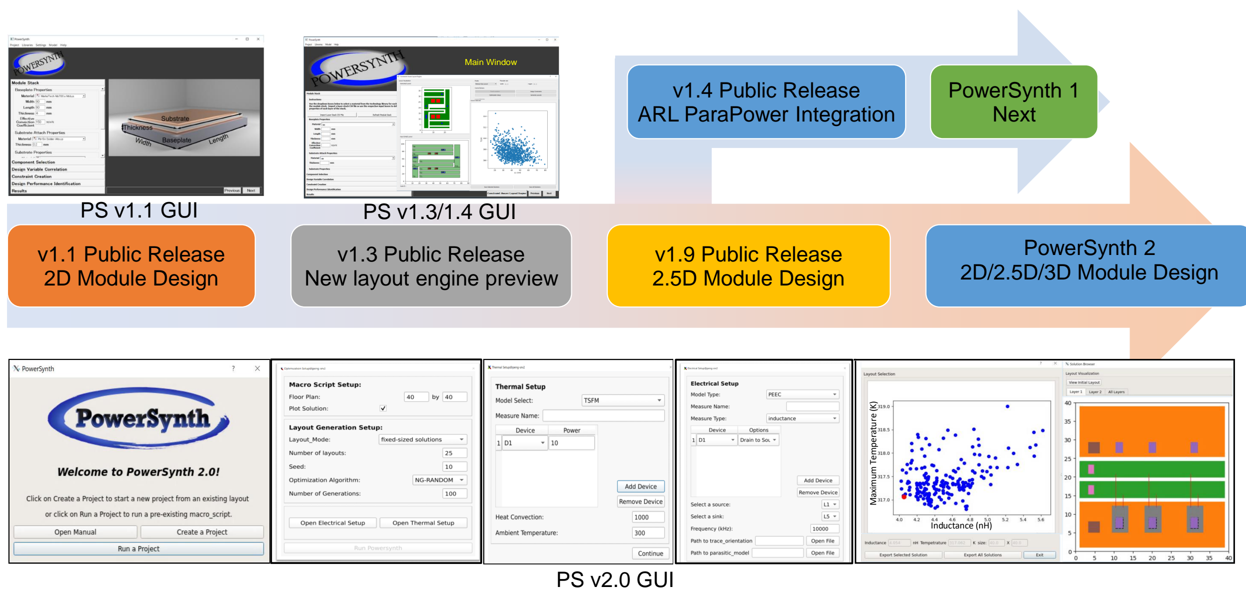


Figure 4: PowerSynth package release flow with GUI

- **PowerSynth v1.3/1.4:** A constraint-aware, flat-level layout engine has been introduced in v1.3. This new layout engine requires a text script-based input to represent the initial layout. Such input script enables to describe 2D layouts with complex geometry. With the updated layout representation technique, the layout engine can handle arbitrary types of components including heterogeneous passive elements. Besides, the new layout engine has enabled studying multiple optimization techniques like stochastic approach, gradient-based, and evolutionary approach. In v1.3, the new layout engine has been launched as an alternative option for the user to generate layout solutions and the optimizer is still dependent on the symbolic layout-based input, and the electrical and thermal models are also the same as in v1.1.

  In v1.4, the Army Research Lab (ARL) developed ParaPower [75] tool has been interfaced with PowerSynth v1.3 for leveraging their thermal and stress evaluation capability. Therefore, in this version, the user has an additional thermal model compared to v1.3. Since ParaPower uses a 3D matrix-based representation of the module structure, it has better accuracy and coverage of layout geometries compared to the built-in 1D thermal model with a small runtime overhead. PowerSynth has a very similar graphical user interface for

v1.1 to v1.4 except the **Constraint-Aware Layout Engine** button.

- **PowerSynth v1.9:** The major updates on PowerSynth research and development have been released in this version. The flat-level constraint-aware layout engine has been updated to a hierarchical one to leverage the hierarchical optimization benefits. Hierarchy has been considered in the layout geometry description script as well to replicate the real-world scenario. With these major updates, this version is capable of handling all 2D/2.5D Manhattan geometries and can generate a larger solution space compared to the previous versions. This new flow has been hardware-validated with a real-world 2.5D full-bridge module. The electrical model has been updated from the response surface technique to the partial element equivalent circuit (PEEC) method. This version has a command-line interface to ensure linux compatibility. Since significant updates have been performed on the underlying algorithms, details have been described in Chapter 4.
- **PowerSynth v2.0:** A completely new modular architecture has been implemented in this version. The modular architecture allows the integration of modeling techniques from other research groups and external tools through application programming interfaces (APIs). The algorithms have been updated to consider both intra-layer and inter-layer interconnects (wire bonds and vias). This version can handle high-density 2D/2.5D/3D MCPM layouts and state-of-the-art (SOTA) packaging technologies. A completely new code base has been developed that has both command-line and graphical user interfaces. The latest version has enabled reliability optimization alongside the basic electro-thermal optimization. PowerSynth 2 CAD flow has been hardware-validated with a novel 3D MCPM module design. Detail algorithms and modeling updates with the hardware-validation results for this version have been described in Chapter 5.

Before diving deep into the PowerSynth v1.9 and 2 updates, some preliminary concepts and topics are discussed in the following to better understand the algorithms and CAD flows. These concepts include the flat-level layout engine implementation and results, which are the backbone

of the hierarchical layout engine introduced in v1.9 and extended in v2.0.

3.3 Preliminary Research

Due to inefficiency and restrictions with the matrix-based methodology, to transform the layout engine into constraint-aware, the corner stitching data structure and constraint graph evaluation methodology have been considered.

Data Structure: The corner stitching data structure and the constraint graph evaluation technique have been adapted from VLSI and customized for power modules. A brief overview of the basic corner stitch and constraint graph is introduced here.

The basic corner stitch data structure was introduced by John Ousterhout [76] and widely used in VLSI CAD tools. In this data structure, there are two types of non-overlapping rectangular tiles: solid and empty. Four pointers are used in each tile to traverse the layout area efficiently. The planar corner stitch has two orientation types: horizontal corner stitch (HCS) and vertical corner stitch (VCS). The basic rules for creating HCS (and VCS) are: (1) Each tile must be as wide (tall) as possible; (2) After satisfying rule (1), each tile must be as tall (wide) as possible. Due to the linear time complexity of associated algorithms (e.g., insert, merge, search) to create corner stitch data structure and the convenience of obtaining necessary design constraints, this data structure has been extended to represent power module layouts in PowerSynth. Horizontal and vertical corner stitch planes of a sample layout are shown in Figure 5.

A constraint graph is a computation technique for a set of inequalities. In this graph, if a vertex A should always maintain a minimum distance of W from another vertex B, then the relationship between A and B can be expressed as:

$$B - A \geq W \tag{1}$$

Here, A is the source, and B is the sink. To maintain the minimum design constraints among all components, two types of constraint graphs (CGs) are created: horizontal (HCG) and vertical

(VCG). HCG maintains the relative location among components horizontally, and VCG vertically. For each corner-stitched plane, two constraint graphs are used to maintain the constraints, where coordinates are mapped into vertices, and the constraints are mapped into edges. Sample HCG and VCG are shown in Fig 5.

Customization for Power Modules: Though the basic corner stitch data structure has only two types of tile, in the case of the power module, each component is represented as a tile of an individual type. Therefore, heterogeneous components can be easily represented and the number of components is not bounded, which ensures the scalability of the methodology. Also, the basic version does not allow overlapping tiles. However, overlapping is a must for proper representation of the layout structure of the power module, because devices (such as power FETs and diodes) are normally placed on top of traces. Therefore, the basic tile insertion function has been modified to allow overlapping of tiles.

Incorporated Constraints: For power module design, two types of constraints are considered: design constraints and reliability constraints. Design constraints are minimum constraints imposed by the technology, to ensure the proper fabrication of the module. Reliability constraints are considered to address issues related to high voltage and current such as partial discharge and thermal.

i. Design Constraints: The following design constraints are considered to have DRC-clean layouts. An illustration of the constraints is shown in Figure 5.

- Minimum Width: Minimum width is associated with each component in the power module. Some components can have a different minimum width along the x and y-axis. All horizontal widths are taken from horizontal corner stitch and vertical widths are taken from vertical corner stitch.

- Minimum Spacing: Minimum spacing value is considered between two components. When there are multiple components in between the same vertices maximum value determines the spacing to ensure DRC validity. All horizontal spacing and vertical spacing are taken from horizontal corner stitch, and vertical corner stitch, respectively.

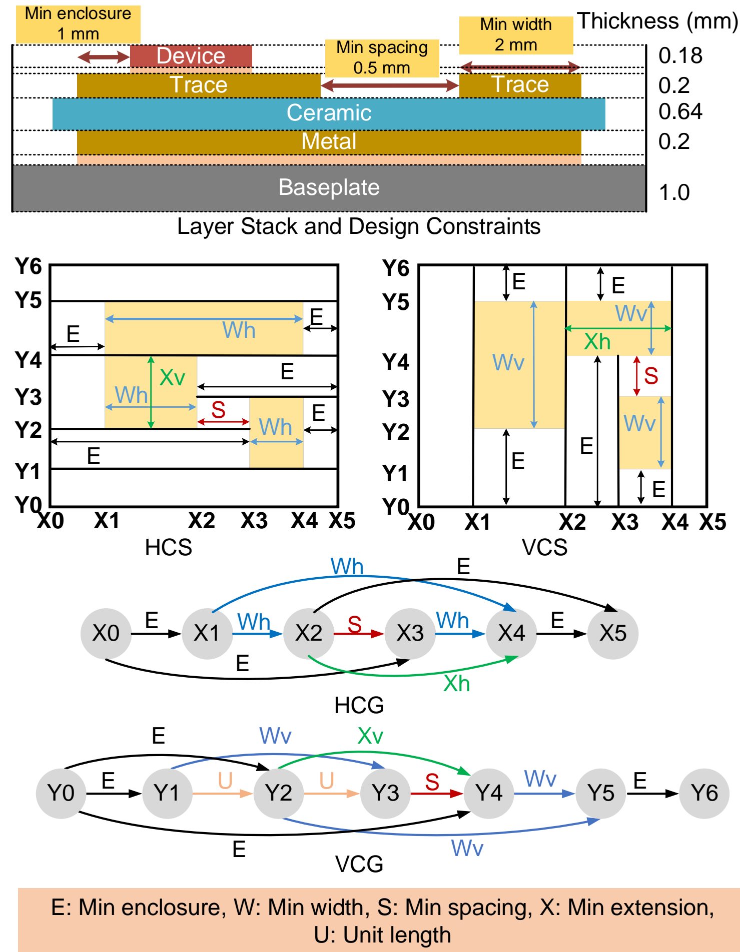


Figure 5: Layer stack and design constraints illustration, corner-stitched planes (HCS/VCS) and corresponding constraint graphs (HCG/VCG)

- Minimum Enclosure: To ensure proper connectivity, some components are required to be surrounded by some other components underneath, with a spacing known as minimum enclosure. For example, when a device is placed on top of a trace, there should be a minimum enclosure of the trace to the device.

- Minimum Extension: In some cases, there may be L-shaped or T-shaped components, where one leg extends in the direction perpendicular to the components routing direction. For those cases, the minimum extension rule appears. Horizontal extensions can be found from the vertical corner stitch, whereas vertical extensions can be found from the horizontal corner stitch.

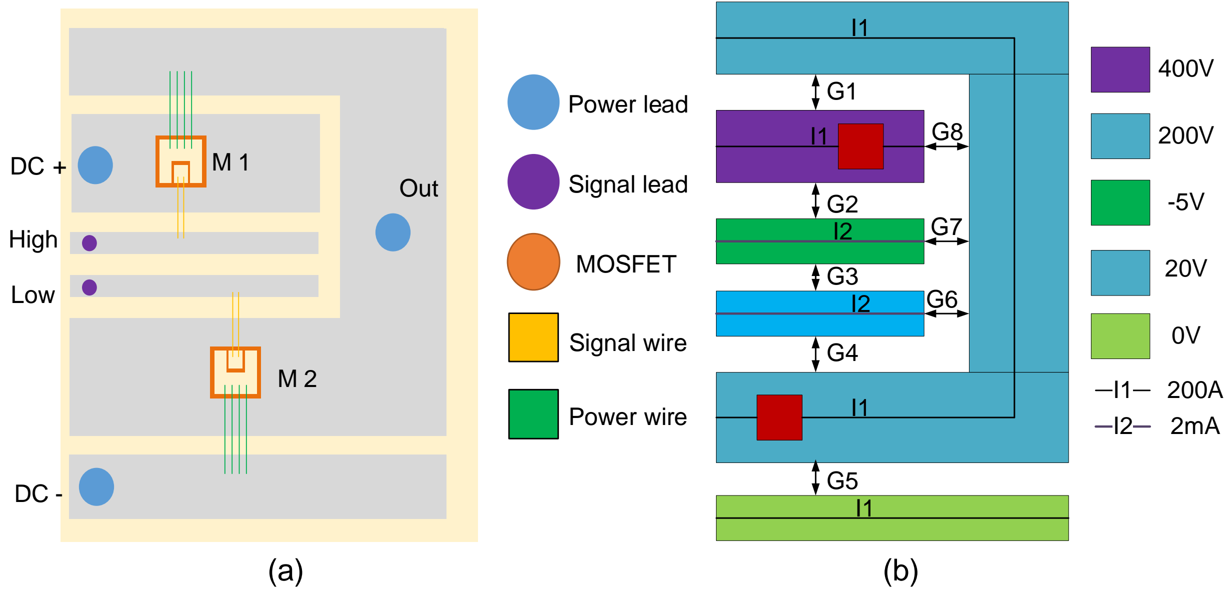


Figure 6: (a) Half bridge power module layout and (b) associated reliability constraints: G1 through G8 are voltage-dependent minimum spacing, and traces have current-dependent minimum width.

ii. Reliability Constraints: The following reliability constraints are considered to minimize partial discharge, current crowding, field focusing, and increase the reliability of the power module. An illustration of the constraints is shown in Figure 6.

- Minimum width: In a power module, power traces can carry a very high current, whereas signal traces carry a very low current. So, for power and signal traces, there should be different minimum widths. As these minimum widths are current-dependent, a user-defined minimum width rule is considered in these cases. Between two minimum widths (design constrained and reliability constrained), the higher value is applied to the graph as the corresponding edge weight.

- Minimum spacing: To minimize the effects of partial discharge in the layout, a voltage-dependent spacing rule is applied. This minimum spacing depends on the voltage difference over the dielectric. To comply with the dielectric breakdown voltages, minimum trace spacing is calculated based on the voltage drop. Same as current-controlled constraints, the higher value between design and reliability constraints dominates. For

Table 2: Summary of operating modes

Mode	Purpose	Evaluation Methodology
0	Minimum sized layout	Minimum constraint values
1	Variable floorplan sized layouts	All weights are randomized with minimum constraints. No maximum constraints
2	Fixed floorplan sized layouts	All weights are randomized with minimum constraints. Some have maximum constraints
3	Fixed floorplan with fixed component locations	

example in Figure 6, each gap is subjected to a voltage-dependent constraint apart from the minimum spacing value imposed by the technology.

Constraint Graph Creation: From each corner-stitched plane, the constraint graph is created by iterating over the entire design and reliability constraints. Each corner-stitched plane is traversed from left to right to create the HCG and bottom to top to create the VCG, which results in horizontal and vertical weighted directed acyclic graphs (DAGs). In the CGs (shown in Figure 5), to keep the relative locations between neighbor vertices, the edges with unit length (U) are added in the VCG. These are non-orthogonal constraints. For the given example, there is no vertically orthogonal relationship between Y1, Y2, and Y2, Y3. Therefore, those edges cannot be found directly from corner-stitched layouts.

Layout Generation: Layout generation algorithms can serve four purposes to have better flexibility, which initiates four operating modes. These modes are summarized in Table 2. The matrix-based layout engine has only fixed floorplan size solutions, whereas the constraint-aware one is giving three more options that can generate more candidates for the designers to choose the optimum solution.

Mode-0: Mode-0 produces the minimum-sized layout that reflects the maximum possible power density for a certain layout. To evaluate the constraint graph, the longest path algorithm is used. In this algorithm, the source vertex is the reference vertex. For the rest of the vertices in the topological order, incremental locations from the source are calculated. The maximum distance from the source to each vertex is set as the minimum location of that vertex. This algorithm has a time complexity O(E), where E is the number of edges in the graph.

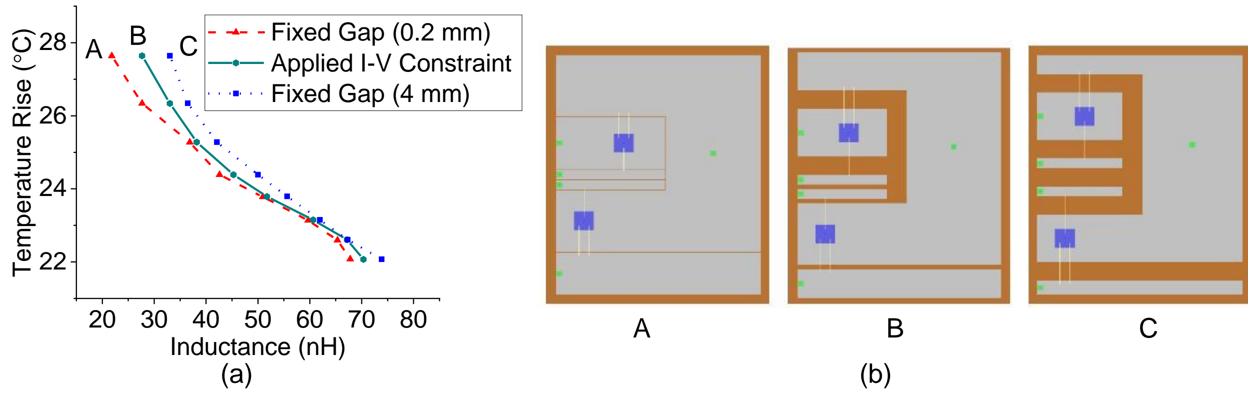


Figure 7: (a) Three Pareto-fronts of layout solutions. Sample 45 mm $\times$ 55 mm layouts generated with (b) 0.2 mm gaps, (c) I-V dependent constraints, (d) 4 mm gaps.

Mode-1: Mode-1 can produce variable-sized layouts. In this mode, all edge weights of the constraint graph are randomized based on minimum constraint values. Gaussian distribution is used to vary each edge weight within the limit of (min constraint, c$\times$min constraint), where c is a constant. The average is set to a value close to the minimum constraint value, and the standard deviation is adjusted accordingly. Then, the constraint graph is evaluated using the longest path algorithm and all vertex locations are determined. The whole procedure is iterated over N times to generate N number of layouts.

Mode-2 and 3: Mode-2 generates layouts having fixed floorplan sizes. In the fixed area it randomizes the component location and generates different solutions. Whereas in Mode-3, not only the floorplan size but also any component location can be fixed. Algorithm has been developed to solve the generic multiple sources and multiple sinks problems (Mode-3). Since Mode-2 is the special case of Mode-3, where the only initial source and sink vertices locations are to be fixed, the same algorithm can be used for both modes. However, Mode 3 has been dropped from the hierarchical optimization in v1.9 and v2.0 as fixing the absolute location of a component in the hierarchical 2D/3D layout is not convenient for the user and very easy to provide wrong inputs.

Benefits of Corner-Stitch with Constraint Graph Evaluation Methodology: The flat-level corner stitching data structure with constraint graph evaluation methodology has proved the following claims.

- The constraint-aware methodology is efficient compared to the matrix-based layout generation methodology. A layout generation efficiency comparison between PowerSynth matrix-based layout engine (old) and the constraint-aware layout engine (new) is shown in Table 3. Three layouts with increasing geometrical complexity are chosen for comparison. As the old layout engine can only generate fixed-sized layouts, only Mode-2 solutions of the proposed engine are comparable. From the table, it is clear that the old layout engine is way less effective than the new one. For some cases, the old layout engine just fails to generate a single valid layout, whereas the new layout engine generates 100% valid layout solutions for all cases with a small runtime overhead.

- The layout representation technique and linear time complexity of layout generation algorithms prove that the new layout engine is both generic and scalable. To evaluate the runtime of the new algorithms, several layouts with a different number of components and different geometrical complexity are chosen. The runtime summary for different operating modes of the algorithms is shown in Table 4. For mode-1 and 2, 3015 layouts are generated for comparison. Mode-3 operation comparison is not a good choice as it is not possible to fix the same vertex locations for each layout. However, Mode-2 is a special case of Mode-3, except that only a single source and single sink are fixed. From Table 4, it is clear that the proposed methodology has a linear time complexity that ensures scalability for heterogeneous power module layout optimization.

- The layout engine can honor different types of application-specific constraints, which proves that the methodology can handle a broader range of applications. To demonstrate the capability of handling reliability constraints such as voltage-dependent spacing and current-dependent width, three different solution sets for the layout shown in Figure 6(a) are generated. For the first layout set, a fixed trace-to-trace distance of 0.2 mm is applied. This layout set represents the minimum manufacturable requirements without considering reliability constraints. In the second data set, both designs and reliability constraints are

Table 3: Algorithm efficiency comparison between the old and new layout engines

Case #	Valid # out of 3015		Total Time(s)		Floorplan Size (mm $\times$ mm)
	Old	New	Old	New	
1	76	3015	0.74	3.57	30×30
2	1883	3015	1.25	7.16	40×50
3	0	3015	N/A	34.13	98×78

applied. Here, trace-to-trace distance is varied with the voltage difference between traces. The current dependent constraints are also applied in this case. To have reliable layouts rated at 200 A peak current, the min trace width is set to be 2 mm. The third data set is generated using a constant 4 mm trace-to-trace distance to minimize PD and thermal issues. In each case, 1000 candidate solutions with varying floorplan sizes from 2475 mm^2 to 9000 mm^2 are generated for optimization. Then, PowerSynth electrical and thermal models are applied to evaluate the maximum temperature and the power loop inductance for each layout. Three different Pareto-frontiers for the corresponding data sets are shown in Figure 7(a). As seen in the figure, the results from three data sets illustrate expected relationships among inductance, temperature, and layout area. Inductance increases due to a larger conduction loop while temperature tends to reduce with the increased layout area. Due to the smallest fixed gap of 0.2 mm, the first layout set has the largest trace variation while the third case has the smallest. By applying both reliability and design constraints, the second data set provides not only DRC-clean layout solutions with good performance but also ensures higher reliability in terms of thermal and partial discharge. This provides designers an opportunity to choose a tradeoff between performance and reliability. The third one can ensure better reliability but has higher parasitics. Three selected layouts having minimum inductance from three Pareto-fronts are shown in Figure 7(b). The first layout has the minimum gap, with the least reliability, whereas the third one is the most reliable but with the highest parasitics. Therefore, the second layout is the most optimum in terms of both electrical, thermal, and reliability.

Limitations: Due to the use of a flat-level constraint graph, the components are correlated

Table 4: Runtime analysis of proposed algorithms, with 3015 layouts generated for optimization

Case #	**Tile #**	**Vertex #**	**Edge #**	**Runtime (s)**		
				Mode-0	**Mode-1**	**Mode-2**
1	8	18	36	0.0159	2.4432	3.5713
2	15	28	68	0.0165	4.10597	7.1645
3	34	43	165	0.0294	7.7506	12.2803
4	72	63	311	0.0551	11.9551	34.1308

with each other and results in in-feasible solutions. All components in the layout always maintain a global relative location to each other. Therefore, there is less variation among the solutions and the solution space reduces. Also, during randomization, the dimensions of all components are randomized. So, in the solutions, all component sizes become variable although some components (i.e., MOSFETs, diodes, leads) should have fixed sizes.

Chapter 4

Hierarchical 2D/2.5D MCPM Layout Optimization

To address the limitations associated with the flat-level approach, and leverage some of the advantages from the symmetricity of a power module layout, the corner stitching data structure and the constraint graph evaluation methodology have been extended to consider hierarchy. The hierarchical approach allows modeling and optimizing individual blocks that result in better optimization of the entire system efficiently. Hierarchy consideration generates more feasible layouts and reduces the computational effort for the symmetric 2.5D full-bridge power module layout optimization.

4.1 Methodology

The hierarchical physical design automation of a 2.5D full-bridge power module has four steps. First, the full-bridge symmetric layout needs to be broken into two parts and only one part needs to be considered. Second, a corner stitched tree structure and hierarchical constraint graphs are generated. Then, this constraint graph is manipulated to generate layout solutions. Finally, these solutions are evaluated using a cost function to optimize the objectives. The tradeoffs among multiple objectives can be represented as a Pareto-front to the user. This hierarchical approach requires an update in layout geometry representation, corner stitch data structure, and constraint graph evaluation. Each part is described below.

Layout Geometry Script: With the updated layout description script, a layout is described in a hierarchical manner, where each component is considered as a group of rectangles. This rectilinear representation ensures to process any kind of Manhattan structure, and the hierarchical representation ensures to place an arbitrary grouping depth of any components.

A sample 2.5D power module layout, and the corresponding tree structure are shown in Figure 8(a), and Figure 9, respectively. Since this 2.5D full-bridge module layout is symmetrical, it can be split into two sub designs. The geometry script shown in Figure 8(b) represents the

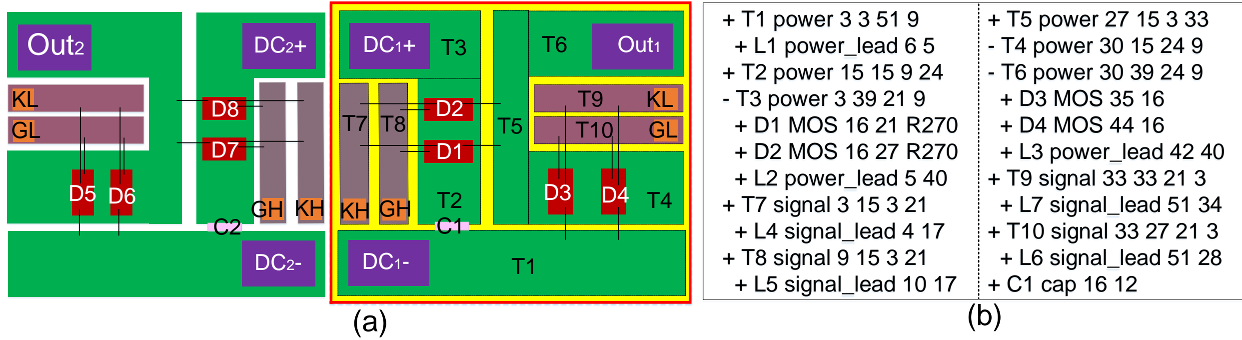


Figure 8: (a) Two half-bridge modules of a 2.5D full-bridge power module, (b) input geometry script for the right half module

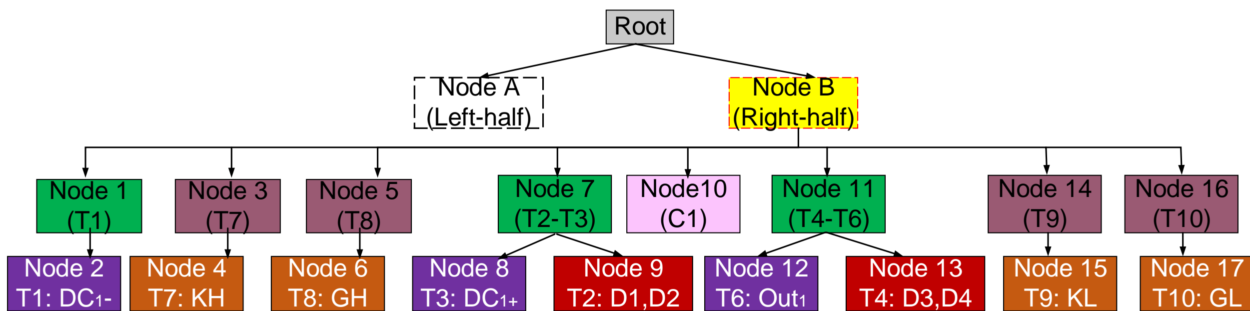


Figure 9: (a) Tree structure of the full-bridge module from Figure 8(a)

highlighted half-bridge power module in Figure 8(a). Here, L1, L2, L3, L4, L5, L6, L7 represent DC_1-, DC_1+, Out_1, KH, GH, GL, and KL respectively. In this example script, the indentation refers to the hierarchy level. The directly connected rectangular traces are inserted in a group-wise manner. Each new group starts with a '+' character while a '-' character represents the continuity of that group. Each trace component is represented by six fields: name, type, lower-left X, Y coordinates, width, and length. Each terminal or device representation has four or five fields: name, type, bottom-left corner X, Y coordinates, and an optional orientation field. The technology library contains the terminal and device dimensions. In the example script, T, L, D, C stand for trace, lead terminal, device, and capacitor, respectively. R270 means the device is rotated by 270 degrees.

Hierarchical Corner Stitch Data Structure: The flat-level corner stitch data structure is a representation of a 2D plane, in which tile overlapping is not allowed. This data structure is modified to handle tile overlapping hierarchically. Generally in power layouts, die and leads are

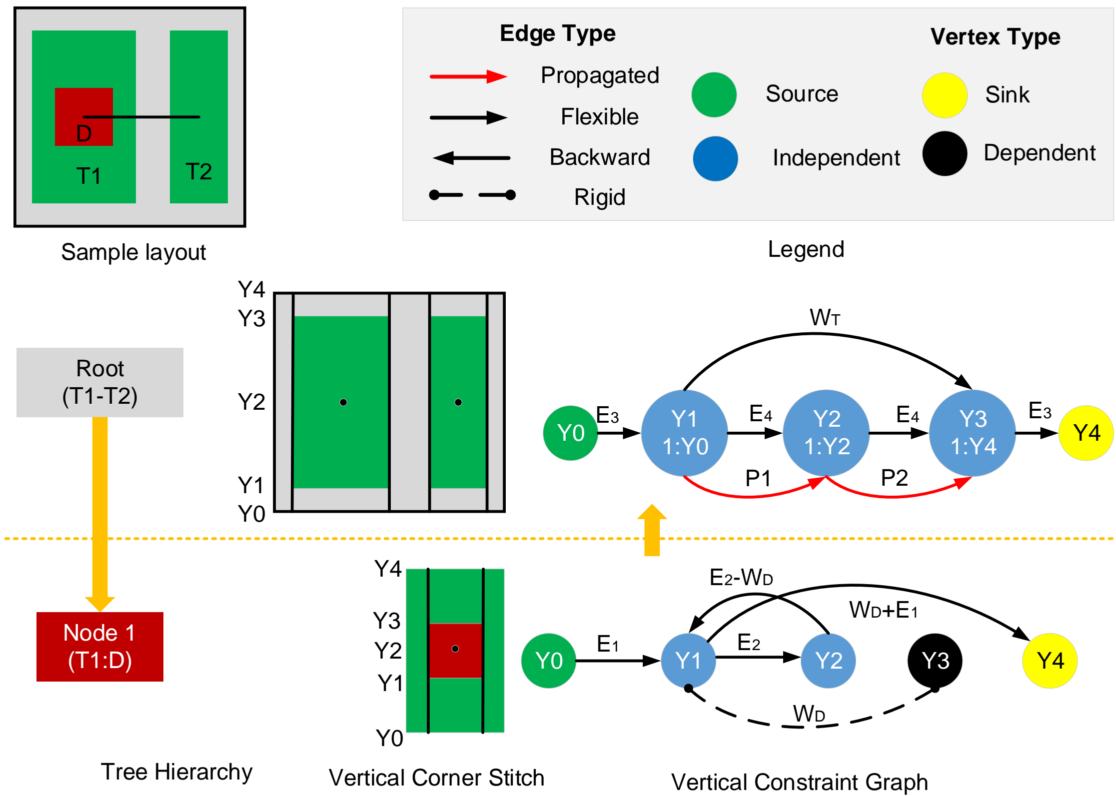


Figure 10: Illustration of edges, vertices, and constraint propagation for a sample layout.

placed on top of traces while pins and bonding wires are placed on top of die. To handle the hierarchical placement of components in the layout, a tree structure is maintained in the layout engine, and each node of the tree is a corner-stitched plane. Due to the hierarchical representation, two additional tile types are considered: foreground and background. When a tile is placed on top of another, the former one is treated as the background and the latter one foreground. For the symmetrical example in Figure 8, no additional computation is required for the left-half. As T2 and T3 are connected, they are in the same node (Node 7). D1 and D2 are inserted on top of T2, which makes D1, and D2 foreground tiles and T2 background tile in Node 9.

Hierarchical Constraint Graph Creation: Once both HCS and VCS planes are created, the corresponding horizontal constraint graph (HCG) and vertical constraint graph (VCG) are created by applying all design constraints (shown in Algorithm 2). After creating both constraint graphs, the bottom-up constraint propagation algorithm (Algorithm 3) is applied to propagate minimum design constraints from the child to the parent node. Once the second for loop in Algorithm 1

Algorithm 1: Layout Generation Workflow

1 Read input geometry script
2 Create a root node with initial floorplan rectangle
3 **for** *each symmetrical module* **do**
4   Create a child node of the root
5 Choose one child node and build the sub-tree
6 **for** *each child node in the sub-tree* **do**
7   CreateCornerStitch(child node)
8   CreateConstraintGraph(HCS/VCS plane)
9   Perform bottom-up constraint propagation
10 Evaluate the root node using the longest path algorithm
11 Perform top-down location propagation

ends, the root node contains all the propagated minimum constraints. For each node in the tree, the foreground tiles are used to find minimum width and length constraints, whereas the background tiles provide the minimum enclosure and spacing constraints. The graph creation starts with leaves in the tree. This paper refers 'node' to a corner stitch tree and 'vertex' to a constraint graph to distinguish between hierarchical trees and constraint graphs.

Each graph is evaluated by the longest path algorithm. After the evaluation of each child node, the longest distance from the source vertex to the sink vertex is propagated to the parent node graph as a propagated edge between the corresponding vertices. For each corner-stitched plane, the lowest coordinate is considered as the source vertex, and the highest coordinate is considered as the sink vertex. In between, there may exist independent and dependent vertices. If there is a fixed dimension component (i.e., devices, leads) in the corner-stitched plane, that component width (length) is mapped with a rigid edge in the HCG (VCG). Any destination vertex of a rigid edge is a dependent vertex. The dependent vertex always maintains a fixed distance from the corresponding independent vertex. All other vertices and edges are independent and flexible, respectively.

Two types of bonding wires are considered: flexible and rigid. For flexible bonding wires, no alignment between the connected group is maintained. Therefore, each group can move independently without violating constraints, resulting in the excessive length of bonding wires.

Algorithm 2: CS and CG Construction

```
1  Function CreateCornerStitch(Node):
2    foreach tile in Node do
3      Perform corner stitch tile insertion operation
4      H_neighbors=list of east/west neighbors
5      V_neighbors=list of north/south neighbors
6      foreach neighbor in H(V)_neighbors do
7        if neighbor.type==tile.type then
8          Perform corner stitch merge operation
9        Perform shadow rectification for the new tile
10   return
11 Function CreateConstraintGraph(CS plane):
12   H_coordinates=list of all x-coordinates of the plane
13   V_coordinates=list of all y-coordinates of the plane
14   foreach index in the H(V)_coordinates do
15     Create a vertex in HCG/VCG
16   foreach tile in the plane do
17     Find proper constraint type and value
18     Create an edge in HCG/VCG
19   foreach pair of vertices in HCG/VCG do
20     if no edge exists then
21       Add a missing edge
22   return
```

The rigid bonding wires are treated as point connections and have source and destination coordinates. Source and destination vertices either have the same Y or X coordinate for horizontal and vertical bonding wires, respectively. A set of horizontal rigid connections is shown in Figure 11. Except for Type-1 connections, all other types of connection handling require vertices propagation from the child node to the parent node and can also introduce a backward edge in the constraint graph with both fixed edge and connection points. The connection processing algorithms are generic to all these types. A detailed illustration of minimum constraint propagation from the child to parent for a Type-2 connection is shown in Figure 10. In the sample layout, a device (D) placed on top of a trace (T1) is connected with another trace (T2) by a horizontal rigid bonding wire. The corresponding tree is shown on the bottom-left. In the child node (Node 1), the trace is the background tile and the device is the foreground tile with a bonding wire terminal point. The parent node (Root) includes an outline of the layout with both

Algorithm 3: Bottom-up constraint propagation

```
1 Input: Parent constraint graph(G1), Child's evaluated constraint graph (G2)
2 Output: Updated G1
3 shared_vertices=list of shared vertices V,where
```

$$V \in (G1, G2)$$

```
4 location=dictionary of evaluated G2
5 for i = 0 to length(shared_vertices) − 1 do
6     source= shared_vertices[i] destination = shared_vertices[i+1]
       v=location[destination]-location[source] G1.add_edge(source,destination,V)
7 Return G1
```

traces and wire terminal points. The left terminal point of the wire has been propagated from the child node as the connection is only visible at the root node. Since the VCS of Node 1 has five Y coordinates, there are five vertices in the corresponding VCG. Here, E_1, E_2, and W_D stand for the minimum enclosure of the trace to the device, the minimum enclosure of the device to the bond wire, and the minimum length of the device, respectively. There is a non-fixed edge from Y2 to Y3 with a weight of E_2. Since Y3 is a dependent vertex, and Y1 is its reference point, the incoming edge from Y2 can be re-directed from Y1. The math expressions are shown in (2) and (3). By substituting Y3, (4) can be derived, which is represented as a backward edge in the VCG. This backward edge imposes a maximum constraint, whereas the forward edge imposes the minimum constraint. As a result, the edge from Y3 to Y4 is also redirected to the reference vertex Y1 with a weight of $W_D + E_1$. Both the dependent vertex and connection point vertex are handled with this algorithm.

$$Y3 - Y1 = W_D \tag{2}$$

$$Y3 - Y2 \geq E_2 \tag{3}$$

$$Y1 - Y2 \geq E_2 - W_D \tag{4}$$

As Y0, Y2, and Y4 vertices are propagated from Node 1 to the root node, they are labeled in

Algorithm 4: Top-down location propagation

```
1  Input: Parent's evaluated constraint graph(G1), Child's evaluated minimum constraint
     graph(G2)
2  Output:Updated Location of each vertex in G2
3  shared_vertices=list of shared vertices V,where
```

$$V \in (G1, G2)$$

```
4  parent_Location=locations of vertices in G1
5  predecessors=locations of vertices in G2
6  location={}
7  A = adjacency Matrix(G2)
8  for i = 0 to length(A) − 1 do
9      if i in shared_vertices then
10         location[i]=Parent_Location[i]
11     else
12         p=predecessor[i]
13         location[i]=Location[p]+A[p][i]
14 Return location
```

Root VCG with the prefix '1:'. In the root node, the design constraints are E_3, E_4, W_T, which stand for minimum enclosure of the substrate to the trace, and minimum enclosure of the trace to the bonding wire, and the minimum length of the trace, respectively. Here, there are two propagated edges P1 and P2 from the child node (Node 1). P1 is the minimum distance from Y0 to Y2, and P2 is the minimum distance from Y2 to Y4 in Node 1. Both P1 and P2 are equal to E_1+E_2 . In this way, constraint propagation is performed throughout the tree to reserve a minimum space for child components in the parent node.

Hierarchical Constraint Graph Evaluation: After the bottom-up constraint propagation is done, the constraint graphs are ready for the second phase of evaluation, where the solutions are generated using the top-down location propagation algorithm (shown in Algorithm 4). Similar to the flat-level solutions, users can generate layout solutions in different modes to have minimum-sized (Mode 0), variable-sized (Mode 1), and fixed-sized (Mode 2) solutions.

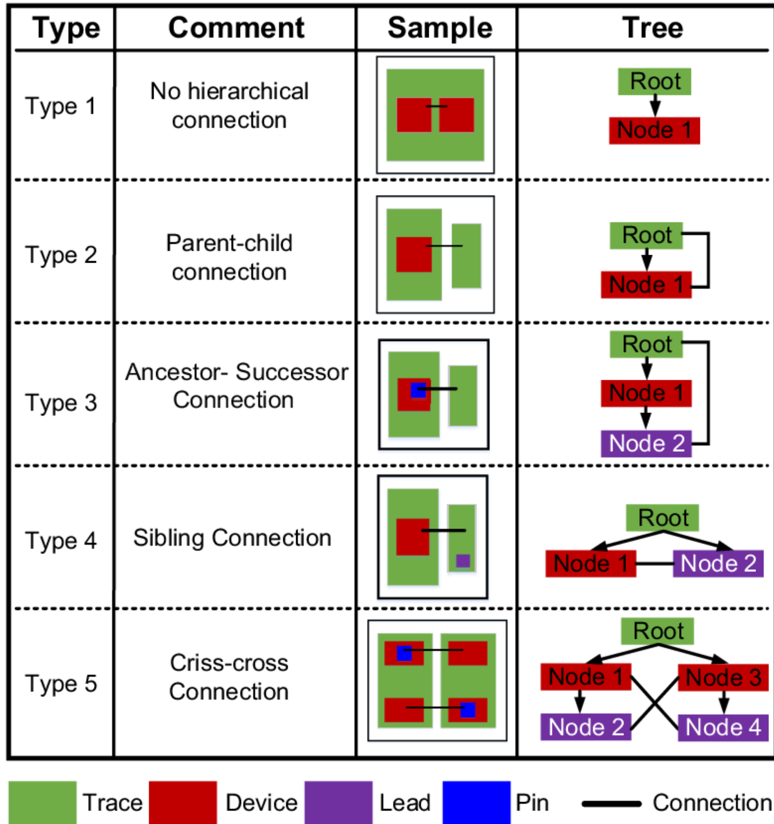


Figure 11: Five types of rigid wire bond connections.

4.2 Models and Optimization Algorithms

4.2.1 Performance Evaluation Models

The first version of the PowerSynth has already validated the first-order linear approximation technique through the Laplacian matrix model [38] with physical measurements. Since this methodology does not consider current density and mutual coupling among components, for some 2D layouts with planar traces, it overestimates the loop inductance. Mutual coupling consideration is necessary, especially for high-density, multi-layer layouts. A partial element equivalent circuit (PEEC) based model [43] has been developed by my colleague Quang Le to address these limitations. This model constructs a controlled mesh structure and produces a detailed voltage-current distribution map. In addition, PowerSynth thermal model [38] can estimate the maximum junction temperature of the layout with good accuracy. Besides, ARL

ParaPower API has enabled PowerSynth users to use a 3D thermal model and stress evaluation method. For the 2.5D power module, optimization objectives include minimizing loop inductance and reducing the maximum temperature of the module. The electrical and thermal models used for power loop inductance and temperature evaluation are summarized in this section.

Electrical Model: The partial element equivalent circuit (PEEC) based distributed electrical model with an adaptive mesh derived from the corner stitch data structure from the new layout engine is used for power loop inductance evaluation. A planar data structure with rectilinear objects is used to pass the layout information to the model. The mesh nodes are generated from the corner stitch data structure by filtering the intersection points from both HCS and VCS planes. Initially, all mesh nodes are distributed into two groups: internal and boundary, where the boundary nodes are nodes located on the connected trace group perimeter, and the rest of the nodes are treated as internal. The internal nodes always have four neighbors, as opposed to the boundary nodes. Each node is tagged with a unique index, and possible edges are created from the node to connect the surrounding neighbors. This edge stores the width and length information of each trace and may be either internal or boundary type. A good approximation of the skin effect is achieved as boundary edges are always smaller than internal edges.

The response surface model from [38] is used to evaluate the self-inductance of every edge and while the mutual inductance between every pair of edges is evaluated using the equation in [77]. A hierarchical approach is implemented to handle the connections between device terminals and traces. This hierarchical representation reduces the total number of meshes, improves computational efficiency, and handles multi-layer structures. Experimental verification of this model has been performed in [43]. This updated model can report distributed parasitic netlist, including R, L, C, and M components. This distributed netlist can be back annotated to the circuit for validation. Since in a layout, the number of mutual inductance components (M) is very large, these values cannot be directly used in the time domain simulation. Therefore, a weighted distributed parasitic netlist based on the loop computation from the PEEC model can be used for transient simulation.

Thermal Model: Thermal performance is also one of the most important factors for MCPM layout optimization. In this work, the hardware-validated, fast, reduced-order thermal model [38] is used for 2.5D power module optimization. The thermal model has already proven to accurately estimate the steady-state maximum temperature of a power module. The model takes the layer stack material properties and dimensions, heat transfer coefficient, and steady-state power dissipation of each device as input. Then, a finite element analysis (FEA) simulation is performed using GMesh [59] and Elmer [60] for each device. The temperature and flux values at the top metal layer of the stack are mapped to a regular grid, which is used to construct multiple rectangular contours for both temperature and heat flux magnitude. This format enables faster computation at contour intersections during the superposition calculation, since it approximates the thermal coupling effect among devices. The thermal resistance network is then extracted, and an impedance matrix is built using the 1D heat transfer circuit topology. Later this matrix is used to quickly evaluate the steady-state thermal performance of each solution. This model has been proved to predict the result correctly with less than 10% error compared to the FEA simulations and approximately 10,000 times faster.

4.2.2 Optimization Algorithms

For optimizing a power module layout, the first version of PowerSynth and many other studies have used a genetic algorithm. Though a genetic algorithm like NSGA II has proven to be beneficial for multi-objective optimization in general, to have a legitimate tradeoff among the objectives in case of the power module, a properly tuned algorithm is required. Also, for heterogeneous power module layouts, the layout complexity and number of design variables grow exponentially, which makes it difficult due to dependency between variables. Two optimization algorithms are considered in this version:

Genetic Algorithm (NSGAII): This is a multi-objective optimization algorithm that generates new solutions as a next offspring by performing crossover, and mutation on the current population. It takes a set of design variables and the number of generations as initial input and

generates initial solutions as a starting point. These solutions are evaluated by the performance models and ranked based on the objectives. A non-dominated sorting is performed on each generation to select the solutions on the Pareto-front. The procedure runs until it reaches the maximum number of generations. This algorithm can generally reach the Pareto-front within a few thousand solutions, thus yields a fast computational time.

Randomization: This is the built-in solution generation algorithm for PowerSynth latest version. In this algorithm, the edge weights of the constraint graphs are randomized within the floorplan upper bound depending on the layout generation mode. This algorithm can generate an arbitrary number of solutions by varying edge values in the constraint graphs. This algorithm can explore a larger and more distributed solution space than that of the NSGAII at the cost of longer run time. Since this algorithm does not have any guidance about particular cost function or objective, if the solution space is large enough with sufficient run time, it can find a better-optimized solution compared to the NSGAII.

Several well-established performance metrics [78, 79, 80] are considered to compare the efficiency of the algorithms. These include: Hyper volume (HV), epsilon-indicator, generational distance (GD), inverted generational distance (IGD), etc. Hyper volume (HV) reflects the accuracy and diversity of the solutions and is measured against a reference point. The higher HV value represents a better solution space. Epsilon indicator measures the accuracy, diversity, and cardinality of the solution space. Generational distance is an indicator of the accuracy and the inverted GD indicates both accuracy and diversity. These three indicators are preferred to be lower values for better-optimized solution space. A study has been performed for a quantitative comparison of the solution spaces from both of the algorithms. For a sample power module, a non-dominated sorting is performed on 20000 solutions for each of the optimization algorithms. The Pareto-front solution space is shown in Figure 12(a). A reference Pareto-front is generated from these two Pareto-solution sets, which is used to calculate the above-mentioned quantitative indicators and the result illustrated in a table (shown in Figure 12).

From the table, it is evident that NSGAII is better in terms of IGD, whereas Randomization is

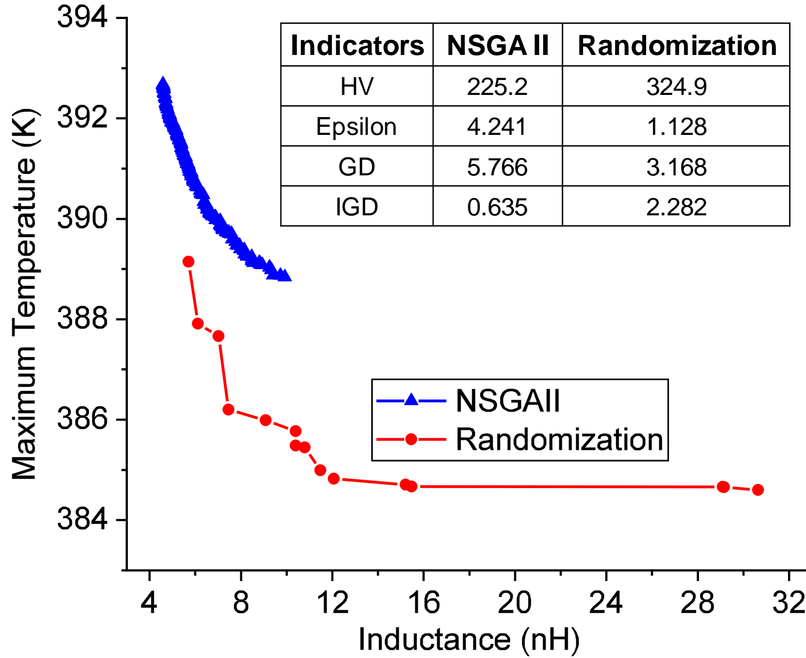


Figure 12: Pareto-front solution set comparison and tabular representation of the performance indicator values. Here, HV reference point is (33,397).

better in case of other three indicators for the particular case. Based on our study, it can be said that no single generic optimization algorithm is enough for the best performance, and customized algorithms are in great need of expanding design capability without sacrificing flexibility and efficiency.

4.3 Results

Since the 2.5D full-bridge power module has two symmetrical half-bridge modules, optimization results from one half can be mapped to the other one. The hierarchical optimization approach allows the re-use of the optimization results and hence reduces the computational effort by half [81]. Therefore, to optimize the 2.5D full-bridge power module shown in Figure 9(a), the right-half module is taken as the input using the layout description script. A standard set of minimum design constraints are applied to generate the minimum-sized solution shown in Figure 13(a). The solution layout is then evaluated using built-in electrical and thermal models. Since a decoupling capacitor is inserted into the power module, the power loop is considered from

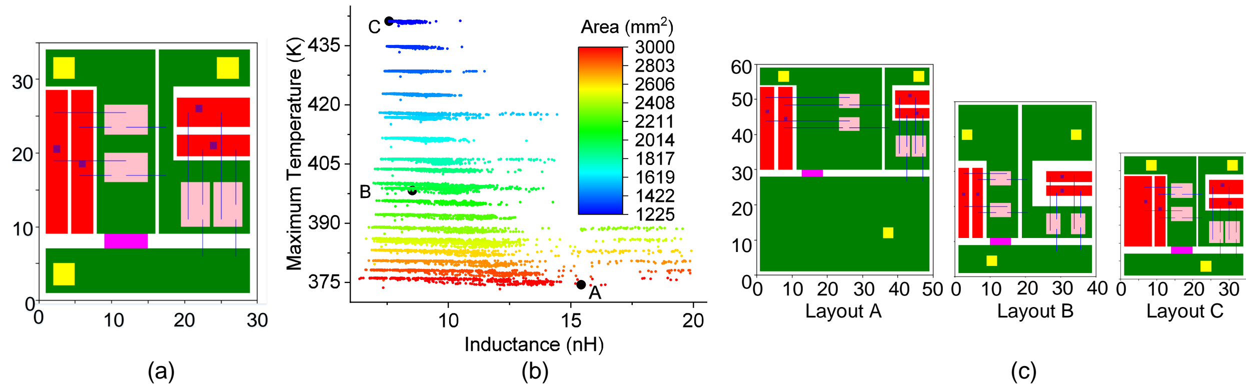


Figure 13: (a) Minimum-sized solution ($30mm \times 35mm$), (b) complete solution space, (c) selected three layouts

the capacitor (C1) top terminal to the capacitor (C1) bottom terminal, and the evaluated loop inductance is 7.986 nH. A layer stack with a baseplate and a DBC substrate is characterized using GMesh [59] and Elmer [60] to evaluate the maximum temperature. The ambient temperature is set to 300 K, and the heat transfer coefficient is set to 150 $W/m^2.K$. The maximum temperature for this half-bridge is found 457.954 K. Since this is the minimum-sized solution, it reflects the theoretical maximum power density of the layout family. However, this design is not reliable in terms of thermal performance due to such a high temperature, though the loop inductance is quite low.

To have a balanced electro-thermal solution, the optimization target is to minimize power loop inductance and maximum temperature of the module by varying the placement and route of the components. To optimize the layout, about 10,000 solutions are generated with varying floorplan sizes. Since the minimum-sized solution is $30mm \times 35mm$, the floorplan sizes are chosen to be greater than the minimum size. Floorplan sizes are varied from $35mm \times 35mm$ to $50mm \times 60mm$ to explore a large solution space. For each floorplan size, around 500 solutions are generated and evaluated. The complete solution space is shown in Figure 13(b). Here, three solutions are labeled to show the tradeoff between the electrical and thermal objectives, and their corresponding layouts are shown in Figure 13(c). Generally, the tool suggests a Pareto-front solution set and the user can choose from the solution set based on the tradeoff requirement. However, in this case, the complete solution space is shown for all evaluated design cases.

Table 5: Performance tradeoff of three selected solutions

Layout ID	Inductance (nH)	Max Temperature (K)	Size (mm×mm)
A	15.426	374.401	50×60
B	8.538	398.278	40×50
C	7.582	441.159	35×35

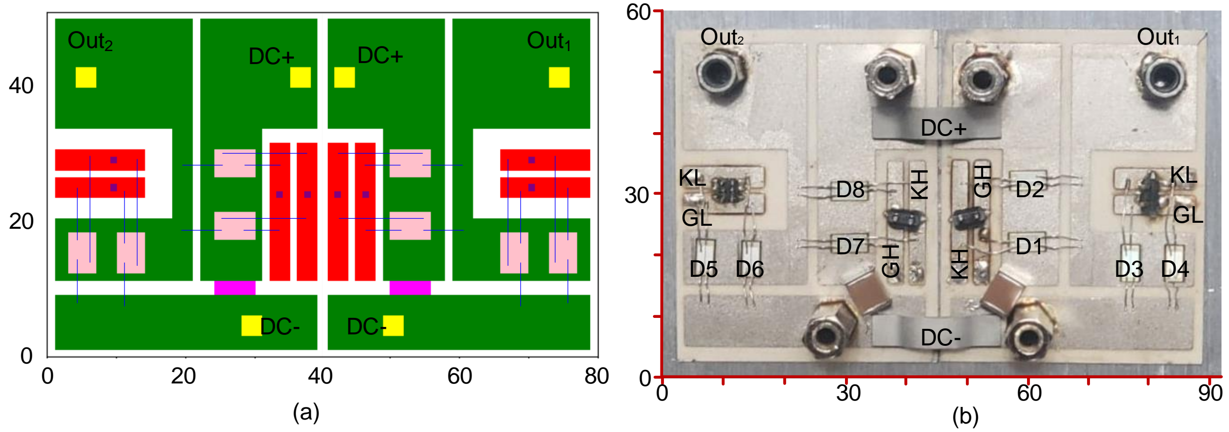


Figure 14: (a) Balanced 2.5D solution layout from the tool, (b) fabricated 2.5D full-bridge power module (92 mm $\times$ 60 mm)

In Table 5, the performance of each selected solution is provided. The table shows that Layout C has a lower inductance value with the highest temperature due to spacing constraints. On the other hand, Layout A has a better thermal result with a worse electrical, which is reasonable as it has the largest floorplan area. Among the solutions, Layout B holds a reasonable tradeoff between the two extreme choices. Therefore, out of all 10,000 solutions, Layout B with a floorplan size of $40mm \times 50mm$ and balanced design objectives, is chosen for fabrication and testing.

Fabrication: The High-Density Electronics Center (HiDEC) of the University of Arkansas has complete processing, packaging, and assembly facilities for developing state-of-the-art power electronic module packages. To leverage the facilities, the selected power module has been fabricated and assembled in-house with a standard SiC-based MCPM fabrication flow. The selected layout information is exported into standard CAD files for manufacturing using the PowerSynth export feature. Then the DBC is prepared for attaching the devices and terminals through the chemical etching process. 1.2 kV SiC devices (CPM2-1200-0040B) from CREE are attached, and the wire bonding is performed by an automatic machine with 12-mil aluminum

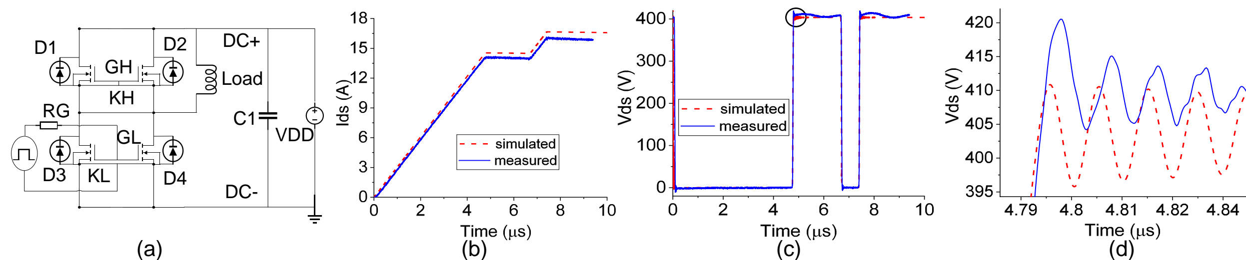


Figure 15: (a) DPT schematic and measurement results for (b) Ids, (c) Vds, and (d) zoom-in shot of (c)

wires. Then, the terminals and the capacitor are attached to complete the half-bridge module fabrication. The room for the capacitor is not enough on the DC- trace since the octagon terminals in the fabricated module are different from the square terminals in the PowerSynth solution. Therefore, the capacitor needs to be placed diagonally. The substrate has been diced into two half-bridge modules to form a modular 2.5D full-bridge module. Both of the modules DC+ and DC- traces are connected through metal bridges for inter-substrate connections. Finally, the base plate and heatsink are attached for heat dissipation. The fabricated power module is shown in Figure 14(b), which has a current rating of 76 A.

Double Pulse Testing: To verify the PowerSynth electrical result, a double pulse test is performed with the fabricated power module. The test schematic is shown in Figure 15(a). An FR4 small bus has been used to connect the module (DUT) terminals with the 1.2 kV laminated bus bar terminals. Due to the custom interface, a jumper wire has been used to connect the gate driver with the gate and Kelvin source terminals of the DUT. The load has an inductance of 131 μH. As the fabricated module has no encapsulating gel, both of the modules are tested under 400 V/15 A rating for safety consideration. The Ids and Vds waveforms are shown in Figure 15 (b), and (c), respectively.

Thermal Measurement: To verify the thermal result, a maximum temperature measurement experiment is performed in an access-controlled lab environment. The KEYSIGHT U5855A TrueIR Thermal Imager has been used to measure the temperature of the devices and heat sink. A J-type thermocouple from National Instruments is used to measure ambient temperature. While

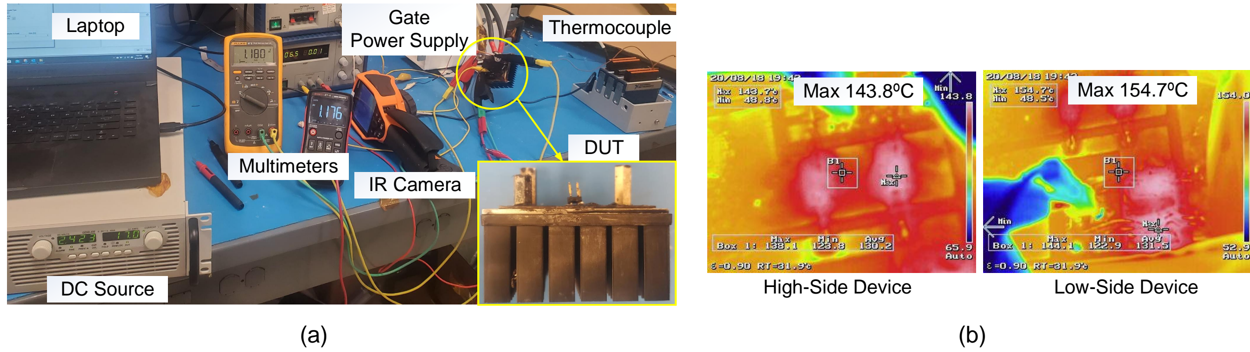


Figure 16: (a) Thermal measurement experimental setup, (b) measurement results

fabricating the module, an aluminum baseplate is used as a copper baseplate was not available. So, silver epoxy is used to attach the aluminum baseplate ($50mm \times 60mm$) to the substrate. A $60mm \times 60mm$ commercial heat sink (shown in Figure 16(a)) is attached to the baseplate using thermal grease material (thermal conductivity 4.5 W/m-K) to achieve a close match with the assumed heat transfer coefficient in the optimization case. However, based on the methodology from [38], the calculated equivalent heat transfer coefficient of natural convection is approximately 123 $W/m^2 - K$. Here, the heat sink surface area is 4.83E-02 m^2 and the temperature is 407 K. The measurement setup is shown in Figure 16(a). A high-current DC power supply is used to supply the necessary current to the devices so that the power dissipation for each parallel connected devices pair is approximately 20 W as we assumed 10 W heat dissipation for each die while performing the optimization. Two multimeters are used to measure the voltage drop across each pair of parallel-connected devices. From electrical measurements, the supply current is found 17 A to achieve a total power dissipation of 40.052 W for the module. In the measurement case, the same assumed boundary conditions as in the optimization case cannot be achieved due to several obvious factors like defects in insulation, heat transfer coefficient mismatch, manufacturing defects, material mismatch of the baseplate, etc.

Validation Results: Electrical and thermal performance validation results are described below.

- **Electrical Performance:** PowerSynth extracted distributed netlist for the Layout B (shown in Figure 13(c)), has been used for time-domain simulations in LTSPICE. The parasitic

Table 6: Comparison between thermal measurement, ANSYS, and PowerSynth

Case	Maximum Temperature (K)				Error in Temp. Rise
	D1	D2	D3	D4	
Measurement	416.8	416.5	427	427.7	-
ANSYS	418.9	416.8	422.4	422.9	-3.57%
PowerSynth	418	417.9	418.3	418.5	-7.15%

values are extracted at 100 MHz, and a gate pulse with -5 to +20 V is applied with a gate on and off resistance of 15 Ω and 5 Ω, respectively. Since only low-side devices are switched, the high-side switches are turned off. A 400V DC voltage is applied to the circuit, while Vds and Ids are measured for low-side switches. The resultant plots are shown in Figure 15. From the Vds and Ids comparison result, it is clear that the simulation has a close match with the measurement. In the case of Ids, the difference is around 3.71% with 16.49 A in simulation vs. 15.90 A in measurement. The measured Vds has a higher overshoot of about 10V and higher noises than the simulated one due to the additional jumper wire inductance and noises from the gate signal in the measurement setup. In the case of measurement, the turn-off ringing frequency is found at 89.43 MHz, while the simulation shows 86 MHz as illustrated in Figure 15(d). The extracted loop inductance from PowerSynth is within 3.84% accuracy.

- **Thermal Performance:** To have a fair comparison between the measurement result and PowerSynth predicted result, the thermal performance is re-evaluated for the same layout in both ANSYS Workbench and PowerSynth by introducing all possible changes in the boundary conditions from the measurement. The thermal camera images are shown in Figure 16(b). The result comparison is shown in Table 6. In simulations, for each SiC device, the heat dissipation is set to 10 W (2.31 W/mm^3). The heat transfer coefficient of the baseplate backside is 123 $W/m^2.K$, and the ambient temperature is 299 K.

  From the results in Table 6, it is evident that the maximum temperature rise result from PowerSynth compared to the measurement and ANSYS result is within 10%, and 5%, respectively. There are a few factors like measurement equipment (power supply,

multimeters, thermocouple, IR camera) tolerances, defects in the structure itself, heat dissipation through radiation is present in the measurement case, which cannot be considered in both ANSYS and PowerSynth cases. The IR camera tolerance is within +2°C and -2°C. The thermocouple reading accuracy is within ±0.1%. The natural convection air cooling is applied and heat sink temperature is measured using the IR camera. The total power dissipation is not completely across the structure and a part of the heat is dissipated through radiation. Therefore, the equivalent heat transfer coefficient value estimation is not 100% accurate. All these unavoidable factors are causing the discrepancy between the measurement and simulation results.

4.4 Limitations

Few limitations with the v1.9 layout generation algorithms are:

1) Dependency on the initial layout from the user and maintaining the relative position of the components throughout the solutions.

2) Connection handling algorithm is restricted to handle intra-layer connections (i.e., wire bonds) only. Also, the wire bond length is not optimized to have reduced parasitics.

3) The rigid edge handling algorithm can handle a limited depth of dependent vertices.

4) Inability to handle non-Manhattan routing.

Chapter 5

PowerSynth 2: High-Density 3D MCPM Layout Optimization

To support high-density state-of-the-art packaging technologies, a new series for PowerSynth is initiated. PowerSynth 2 is the superset of the previous versions with extended capabilities. In this chapter, the 3D CAD-flow validation is presented with description of the algorithm updates.

5.1 PowerSynth 2 Architecture

PowerSynth 2 architecture is shown in Figure 3. Compared to PowerSynth 1, the new architecture is a module-based one. It has multiple design layers, and each layer has a flexible API to communicate within or outside the tool. The tool has two fundamental parts: A core that contains the built-in algorithms, methodologies, and modeling techniques; External tools that include commercial tools or models developed by other research groups, which are linked through APIs developed by the PowerSynth team members. This architecture is scalable and can be extended toward cabinet-level optimization.

5.1.1 User Interfaces and Design Input

PowerSynth v2.0 has both GUI-based interactive mode and CLI-based unattended mode to support Windows and Linux compatibility. The command-line interface works on user input through the terminal, which has both step-by-step mode and script mode available. The step-by-step mode generates and saves the necessary scripts that can be re-used in the script mode. The step-by-step mode is for a new project and new users, whereas the script mode is suitable for regular users.

Besides, there is an interactive GUI for the users. Some of the windows of the GUI are shown in Figure 17. The main window of the user interface provides two main flows: (a) Creating a new project from an existing layout; (b) Running a project using the macro script already prepared. Users can modify the material library, layer stack, and design constraints through the GUI. Then,

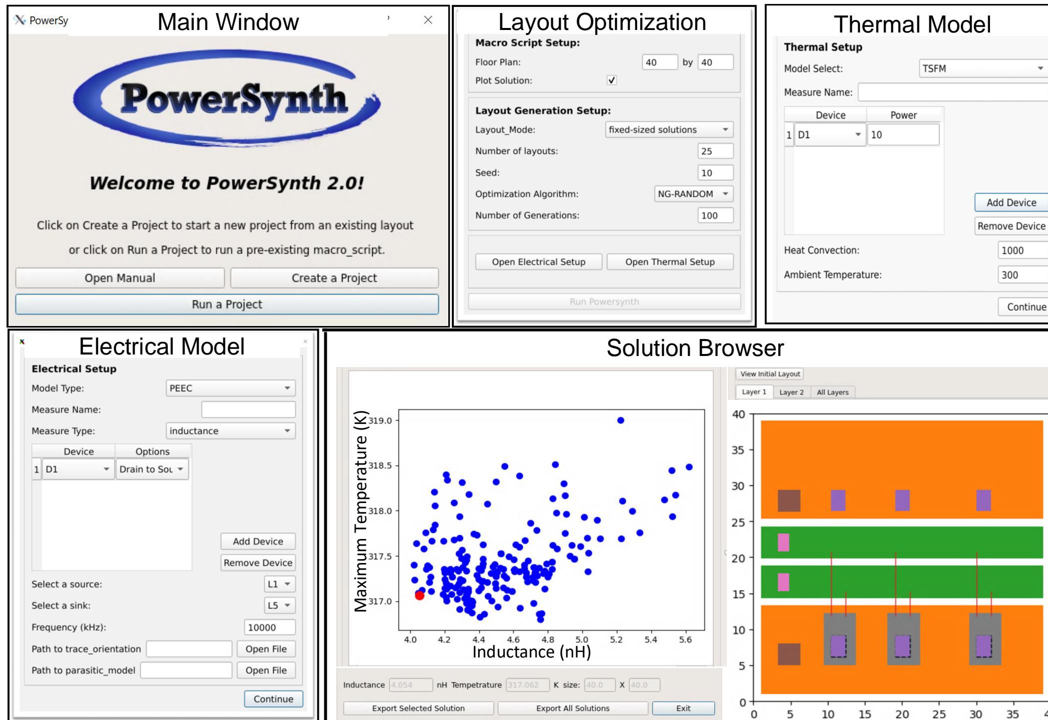


Figure 17: PowerSynth 2 graphical user interface (GUI)

the layout generation/optimization setup window can run PowerSynth 2 in three different modes: performing performance evaluation of the initial layout, generating layout solutions only, and optimizing layout solutions based on the performance models. For optimization/evaluation mode, the user needs to set up necessary files and parameters through different model setup windows. Once the necessary parameters are defined, the layout optimization process begins, and results are shown in the solution browser. Finally, the user can choose an individual solution from the solution space and export both individual and complete solution space for further processing. More details about the GUI development can be found in [46].

PowerSynth 2 requires an initial description of the technology that contains the layer stack, power devices, substrates, connectors, heat spreaders, wire bonds, and via information. As an umbrella module, the built-in manufacturer design kit (MDK) contains a library of materials and other technology information similar to the process design kit (PDK) in Very Large-Scale Integration (VLSI). An interface is built to interact with MDK so that users can update the libraries. Besides, the initial placement of the devices, leads, and routing of the traces information

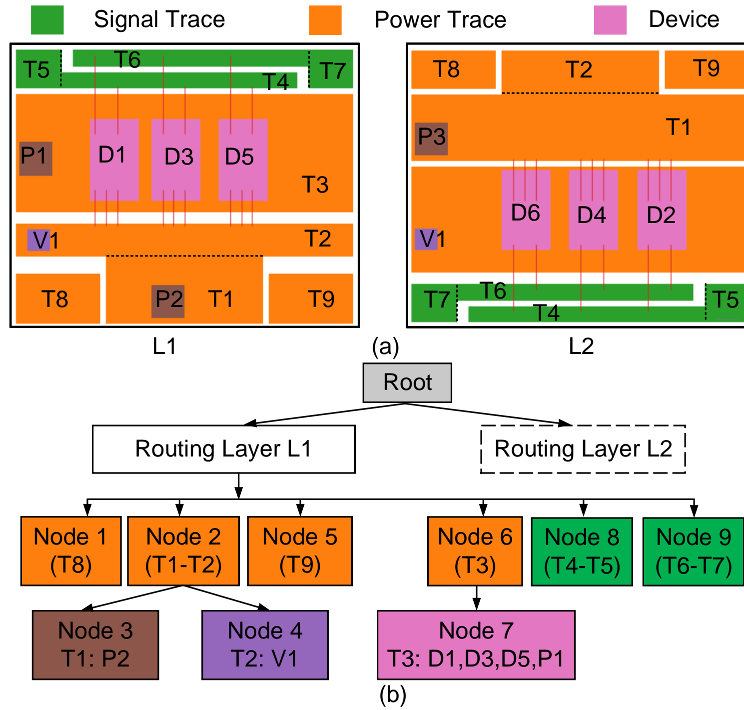


Figure 18: Input layout structure of a 3D MCPM: (a) 2D view of each routing layer, (b) the L1 layer hierarchical tree

is taken through a hierarchical geometry description script, which is represented through an object-based data structure. An embedded scripting environment can be used to accelerate the layout geometry processing.

5.1.2 Layout Generation and Evaluation

The initial input layout is stored using two hierarchical corner-stitched tree structures: One for horizontal and another for vertical corner-stitched planes. From this data structure, two sets of constraint graphs are created for layout solution generation using the values of the minimum constraints as edge weights provided by the manufacturer or user. Several efficient algorithms are used to generate different types of layout solutions by randomizing the edge weights of the constraint graphs. Constraint graph creation and evaluation ensure the DRC-clean solution generation.

As WBG devices can switch faster at higher voltage and current, electrical parasitics in the MCPM layout must be minimized to achieve the target circuit performance. With the increased

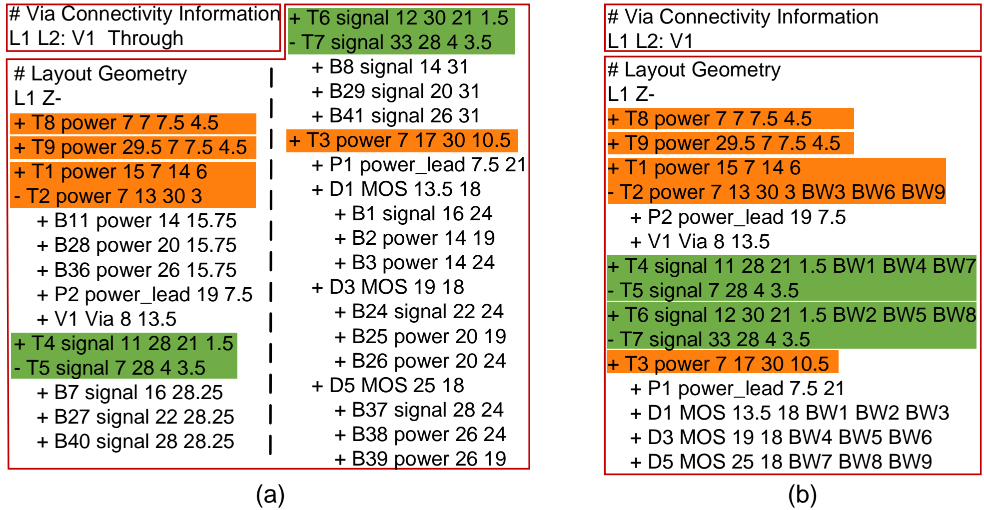


Figure 19: Input geometry script of routing layer L1: (a) developer mode, (b) user mode

density in a 3D MCPM layout design, the parasitic loop inductance is significantly reduced compared to its 2D counterparts. However, as the 3D layout solution is more compact, ensuring thermal and mechanical reliability becomes challenging. Therefore, electro-thermo-mechanical performance and reliability optimization are required before fabricating a module. Available multi-physics or FEA-based analysis tools can be used for capturing these performances. However, these methods are not efficient to be used in the optimization loop due to long runtime. To address these issues, PowerSynth 2 is equipped with reduced-order electrical, thermal, and reliability models, which are fast and quite accurate compared to FEA tools. The electrical model performs resistance, capacitance, and inductance evaluation. Research is ongoing to extend electrical models to 3D layouts. Thermal metrics include static and transient junction temperature evaluation. Reliability optimization refers to transient thermal cycling impact minimization and electromigration risk assessment. Maximum, average, and peak-to-peak temperatures of different components due to the transient thermal cycling input are considered, which is proportional to the thermal stress endured by the devices. Multi-level APIs have been developed inside the tool to leverage the existing electrical, thermal, and mechanical models from other research groups or companies. In this work, FastHenry [82] from FastFieldSolvers is used for loop parasitics extraction, and ParaPower [75] from Army Research Lab for thermal evaluation.

5.1.3 Design Optimization and Solution Export

For providing optimization options, PowerSynth 2 has a genetic algorithm and built-in randomization algorithm framework with other optimization algorithms such as simulated annealing and the neural network under investigation. Currently, PowerSynth 2 flow users can choose any available options for performing electrical, thermal, and reliability optimization. A comparison study between randomization and genetic algorithm shows that genetic algorithm can converge faster to the Pareto-optimal solution set for a given number of generations. Though randomization provides little guidance toward optimization objectives, it can explore a larger solution space and potentially find better solutions with an acceptable runtime overhead [83]. Once the optimizer generates the solution space, a non-dominated sorting is applied to get the Pareto-optimal solutions. After choosing an optimized solution for fabrication, post-layout optimization features like filleting the sharp corners to reduce current crowding and field focusing can be performed. From the solution browser, the user can choose a solution to export. APIs have been developed by my colleague Quang Le to export the solution in commercial 3D CAD tools like ANSYS Q3D, SolidWorks, etc. Exporting a complete distributed parasitic netlist with RLC elements is one of the killer features. Round-trip engineering of power modules is enabled by the extraction of the parasitics into netlist form for annotation back onto the original netlist. This work, performed by my colleague Quang Le, enables the designer to simulate their layout with parasitics before committing to manufacturing. Finally, the optimized solution can be fabricated to validate and fine-tune models through physical measurements.

5.2 Physical Design Automation Methodology

Layout optimization starts with a user-provided initial layout geometry script and ends with generating a fabrication feasible optimized layout solution set. Major steps include layout representation, layout synthesis (solution generation), performance evaluation/optimization, and solution export. Each of these steps is briefly described below.

5.2.1 Layout Representation and Data Structures

PowerSynth 2 takes a layer stack, a set of constraints, and a hierarchical layout geometry script along with the via connectivity information as input. A sample 3D layout consisting of two routing layers (L1 and L2) connected through a via (V1) is considered for describing the layout representation in PowerSynth 2. The planar view of each routing layer of the 3D layout is shown in Figure 18 (a). The hierarchical tree structure for the sample 3D layout is shown in Figure 18 (b). Both Routing layers have six groups of traces. Each group can have single or multiple connected traces. L1 has DC+ (P1) and OUT (P2) power leads along with three SiC devices (D1, D3, D5). L2 has DC- (P3) and three SiC devices (D2, D4, D6). Both layers' have via (V1) connected OUT trace. Since both routing layers have a very similar structure, only the L1 layer sub-tree is shown. From the tree structure, it is clear that six trace islands are mapped into six nodes in the L1 sub-tree. Since Node 2 and Node 6 traces contain additional components, they have child nodes (Node 3, 4, 7). To provide such an initial layout as input in PowerSynth 2, the user needs to generate the text script shown in Figure 19. The layout geometry script needs to be created based on the same hierarchical placement concept as shown in Figure 18 (b).

PowerSynth 2 supports two types of geometry scripts: (a) Developer mode, (b) User mode. The developer mode has a detailed geometry description including absolute coordinate of the bond wire landing pad locations, whereas in the user mode, those detailed locations are hidden and automatically calculated to optimize the wire lengths. The developer mode requires another wire bond connectivity script to make the wire bond connection across the geometry, whereas the user mode does not require such script. The script has two parts: **Via Connectivity Information** and **Layout Geometry**. In the **Via Connectivity** section, each line has two fields separated by a colon. The fields are names of the via connected layers separated by a space, names of the vias separated by a space, and the via type (Through or Connector). 'Through' type vias connect two routing layers of the same substrate, whereas the 'Connector' type vias connect two routing layers of different substrates. In this example, there are six different types of components: power and signal trace (T), wire bond (B), power lead (P), via (V), and device (D). The layer names are

mapped from the layer stack information. In the **Layout Geometry** section, for each layer, the first line represents the layer name and corresponding routing direction. The following lines represent each component in the layout. Each new group starts with a plus sign, and a dash represents the continuation of the same group. Traces have six fields, and other components have 4 or 5. Each component has four basic fields: ID, type, bottom-left corner's x, and y coordinate. The geometry is described using a global coordinate system. Since the trace dimensions can be varied, two extra fields are required for the initial layout description: width and length. Other components' except bonding wire width and length are constant and read from the corresponding component description files available in the MDK. Sometimes, the devices can have a rotation field to describe the orientation. Three different orientations (R90, R180, R270) are considered that represent device rotation of 90°, 180°and 270°. Each wire bond group is treated as a connection between two points in PowerSynth 2. Therefore, this type does not require width and length. Since the wire bond locations are not defined in the user mode script, the wire bond source and destination locations are decided based on the wire bond connection name. For each device, the ordering of the wire bond should be Gate, Kelvin Source, and Source, respectively. For example, in Figure 19 (b), D1 MOSFET has three wire bonds: BW1 (Gate), BW2 (Kelvin Source), BW3 (Source). If there is no Kelvin Source connection, there will be two wires per device.

The initial layout description script is parsed and stored in horizontal (HCS) and vertical corner stitch (VCS) tree structure combining information from the layer stack. The basic corner stitch data structure [84] is modified to allow overlapping of tiles by implementing a hierarchical tile insertion algorithm. For each node in the tree, the parent node corner stitched plane is the background tile, and the new tile is inserted as the foreground tile. The background tiles are used to find both minimum enclosure and spacing constraints. And the foreground tiles are used to get the minimum width and length constraints. Besides these design constraints, user-defined reliability constraints can be considered as well. For example, current-dependent minimum width, and voltage-dependent minimum spacing are required for reliable operation at a high

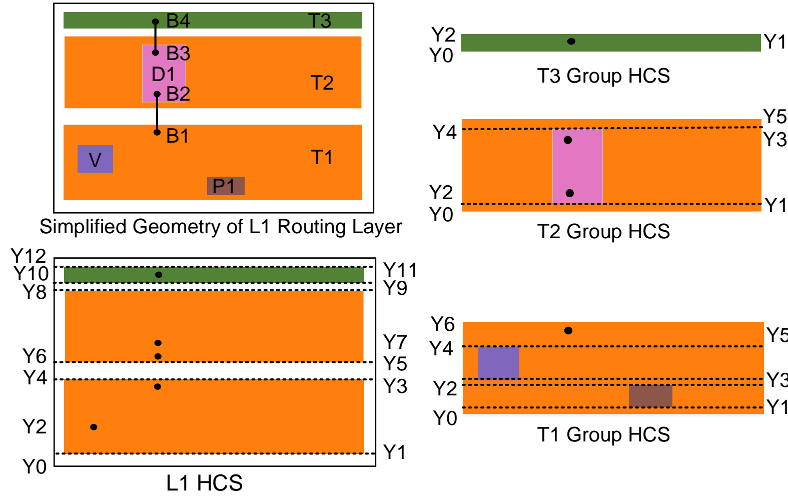


Figure 20: Constraint propagation using a simplified example from Figure 18(a)

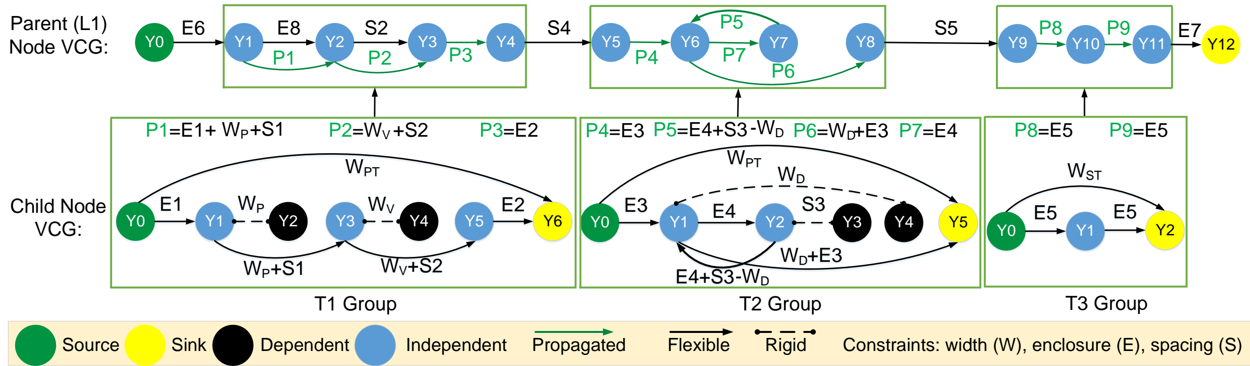


Figure 21: Bottom-up constraint propagation illustration for HCS shown in Figure 20. Here, subscripts P, V, D, PT, ST represents power lead, via, device, power trace, signal trace, respectively.

voltage-current rating. For 3D layouts, the minimum clearance and creepage distance among multiple layers also need to be considered for safe operation. All these reliability constraints can be applied while generating the constraint graphs (CG). For each node in the tree, two constraint graphs are created by mapping the coordinates into vertices and corresponding constraint values as edge weights. These constraint graphs are used to generate layout solutions by edge weight manipulation through randomization. The horizontal constraint graph (HCG) maintains the horizontal relative location among the components, and the vertical constraint graph (VCG) maintains the vertical relative locations. The layout solutions can be generated by computing the vertices' locations from both graphs after the edge weight manipulation.

Algorithm 5: Layout Generation Workflow

```
1  Parse the input geometry script
2  Read layer stack and design constraints
3  Create a root node of the structure
4  Create group of routing layers connected with a same via
5  for each connected group do
6  |   Create an interfacing layer
7  |   for each routing layer in the group do
8  |   |   Create HCS and VCS
9  |   |   Create HCG and VCG
10 |   |   Evaluate HCG and VCG
11 for each ancestor from leaf to root do
12 |   Perform bottom-up constraint propagation
13 Evaluate root node and compute available space
14 for each sub-tree from root to leaf do
15 |   Perform top-down location propagation
```

5.2.2 Constraint-Aware Layout Synthesis Algorithms

A high-level workflow of layout solution generation is shown in Algorithm 5. This algorithm is the updated version of the previous one (Algorithm 1). For the multi-layered 3D structure, abstract nodes (interfacing layers) are maintained to ensure the alignment of the via coordinates. After creating the HCG and VCG for each node in the tree, bottom-up constraint propagation is performed to ensure the minimum required room for the child node in the parent node. Each constraint graph is evaluated using the longest path algorithm. Starting from leaf nodes, the longest shared subgraph between the child and parent is propagated towards the parent nodes. This bottom-up constraint propagation continues until the root node receives all necessary constraints. To demonstrate the bottom-up constraint propagation, a simplified structure of the L1 routing layer from Figure 18(a) has been considered and shown in Figure 20. Here, the horizontal corner stitch (HCS) view of the L1 sub-tree is demonstrated. In each child's HCS (T1, T2, T3), the bonding wire landing point coordinates are represented as dots. However, in the parent HCS (L1), all propagated coordinates are shown as dots. For this simplified structure, the corresponding bottom-up constraint propagation is illustrated in Figure 21. Each coordinate from HCS is mapped into a vertex in the VCG. Each edge in the VCG represents a design constraint. In

Algorithm 6: Constraint validation and graph reduction

Input : node CG, user constraints
Output: trimmed CG

1. select candidate vertices and edges for removal
2. push all candidate vertices into a stack
3. **while** *stack is not empty* **do**
4. current vertex (vi) = stack.pop()
5. determine the reference vertex (vr)
6. redirect all incoming rigid edges to vr
7. **if** *edge(vr, vi) is the Longest_Path(vr, vi)* **then**
8. Edge redirection and constraint validation(CG, vi, vr)
9. **else**
10. return no solution found
11. update the stack based on the CG

this simple geometry, three types of constraints are considered: minimum width (W) of each component, minimum enclosure between two components (E), and minimum spacing between two components (S). In the child VCGs, there is no propagated edge, whereas, in the parent VCG, most of the edges are propagated (solid green). The weights of the propagated edges are computed at the child node's CG. The other two types of edges are: flexible (solid black) and rigid (dashed black). A rigid edge has a fixed weight having the destination as a dependent vertex. On the other hand, a flexible edge with both origin and destination as independent vertices can vary its weight. The notations of the constraint values considered in the example are: E1 through E7 represent minimum enclosure rules while S1 through S5 represent minimum spacing rules between different components. From the child nodes, the minimum necessary subgraph is propagated to their parent node. For example, in the L1 VCG, the subgraph of Y1-Y4, Y5-Y8, and Y9-Y11 contains propagated edges from T1, T2, and T3 VCG, respectively. Here, P1 through P9 are edge weights propagated from child VCGs. The detailed algorithms for solving constraints and evaluating locations are based on the algorithms shown in Algorithm 7 and Algortihm 6. Details about these algorithms can be found in [83].

The root node can be evaluated in the three modes: Mode 0, Mode 1, Mode 2 using the top-down location propagation algorithms [85, 83].

Algorithm 7: Edge redirection and constraint validation

```
    Input   : CG, vi (dependent vertex), vr (reference vertex)
    Output: updated CG
1   f = constraint(vr,vi)
2   foreach non-fixed incoming edge do
3   |   vj = edge.source; e = edge.constraint
4   |   if vj is a successor of vr then
5   |   |   g = Longest_Path(vr,vj); weight = e-f
6   |   |   if weight==g then
7   |   |   |   add_edge(vr,vj,weight,rigid)
8   |   |   else if weight<g then
9   |   |   |   add_edge(vj,vr,weight,flexible)
10  |   |   else
11  |   |   |   return no solution found
12  |   if vj is a predecessor of vr then
13  |   |   h = Longest_Path(vj,vr); weight = max(h,e-f)
14  |   |   add_edge(vj,vr,weight,flexible)
15  |   remove the incoming edge
16  foreach outgoing edge do
17  |   vj = edge.sink; e = edge.constraint; weight = f+e
18  |   if vj is a predecessor of vr then
19  |   |   h = Longest_Path(vj,vr)
20  |   |   if weight+h==0 then
21  |   |   |   add_edge(vr,vj,abs(weight),rigid)
22  |   |   else
23  |   |   |   add_edge(vr,vj,max(h,weight),flexible)
24  |   else
25  |   |   add_edge(vr,vj,weight,flexible)
26  |   remove the outgoing edge
```

Once the root node evaluation is performed, the locations of the shared vertices are propagated in a top-down fashion until all leaf nodes are evaluated. This process is called top-down location propagation, where each node is allocated with some space for expansion, which creates more design variants in the solution space. A sample illustration of the top-down location propagation for minimum-sized and fixed-sized solution generation is shown in Figure 22. Here, to simplify the illustration, a partial HCG (only the T1 group region) from the complete L1 layer(shown in Figure 20) is considered the parent HCG. For minimum-sized solution generation, minimum edge weights are assumed as shown in the figure. The source is

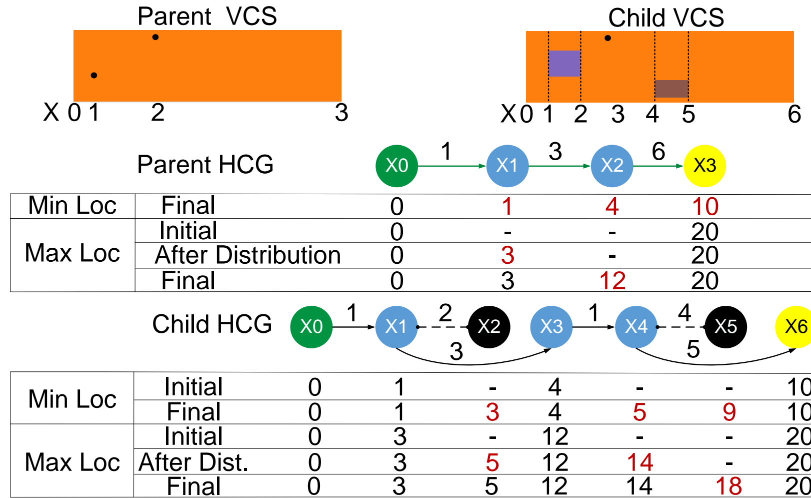


Figure 22: Top-down location propagation illustration for T1 in Figure 20.

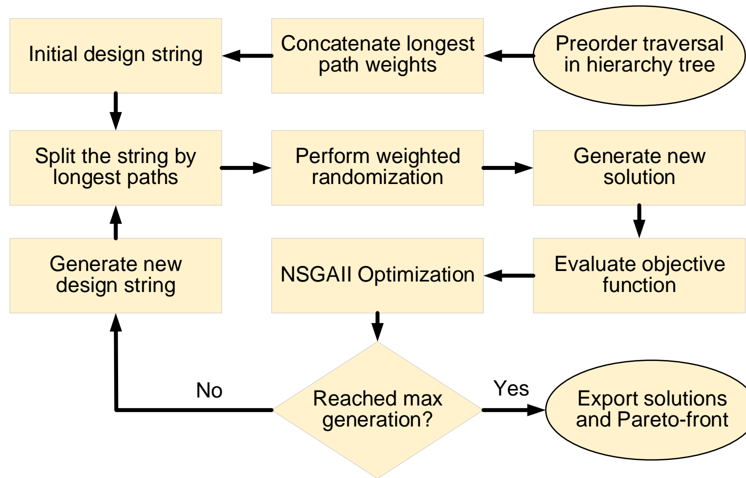


Figure 23: NSGAII implementation workflow

always considered a reference vertex, and the location is set to 0. The rest of the vertices are calculated based on the longest path. In the child HCG, shared vertices (X0, X1, X3, X6) are propagated from the parent. The rest of the vertices are calculated based on the longest path from the source to that vertex. In the case of the fixed-sized solution generation, both min and max locations are necessary. Max location computation is an iterative process. In each iteration, one flexible vertex location is determined after distributing the weight from randomization. For example, in the parent node case, if the user sets the X3 vertex location at 20, the X1 vertex has room for randomization between 1 (0+1) and 11 (20-6-3). So, after distribution, if the value is set

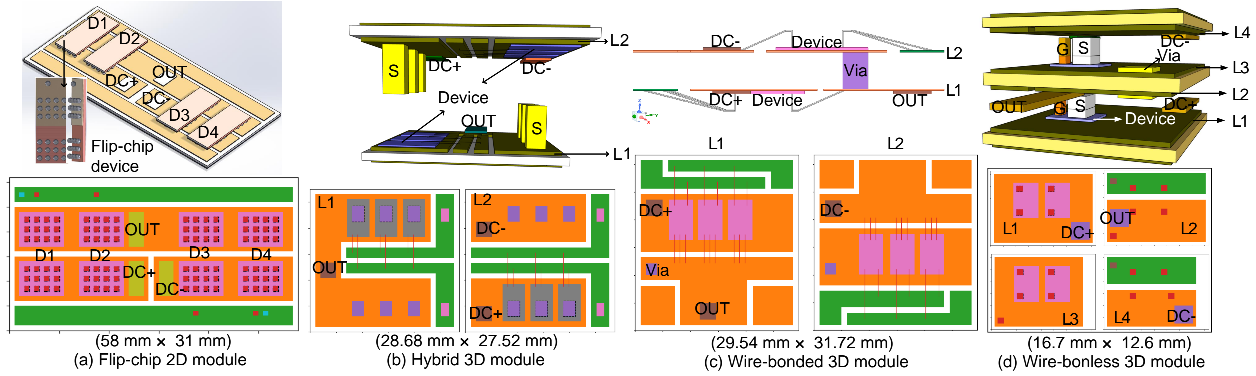


Figure 24: 3D structure and minimum-sized solution of high-density packaging layouts

to 3, X2 must be between 6 and 1. Any value in that range ensures a DRC-clean solution. The child node's maximum locations are also determined similarly. The detailed algorithm is described in [83].

5.2.3 Multi-Objective Modeling and Optimization

Since PowerSynth 2 can perform multi-objective optimization, fast and accurate models are required for performance evaluation to explore a large solution space within an acceptable runtime. The electrical and thermal models used in this work are described below.

Electrical Modeling: To extract electrical parasitics (i.e., loop inductance, resistance, capacitance), PowerSynth 2 has two options: an API for evaluating through FastHenry and a built-in electrical model. The loop-based method from VLSI has been adapted by my colleague Quang Le to capture the mutual coupling among conduction paths in the power module. This method has several advantages for high-density 3D MCPM layouts, including more efficient mutual inductance extraction, a significantly smaller netlist size, and compatibility for parallelization [86]. Firstly, a path-finding algorithm is applied to each layout solution to determine the current direction through each trace. These current directions are then stored in a directed graph, where they are later partitioned and grouped into two different sets, namely horizontal and vertical bundles. Each set only contains trace segments of equal length. Next, an iterative algorithm runs through each bundle to evaluate the parasitics of all segments. A

lumped-elements netlist is formed during this iterative process to store all parasitic results. Finally, a current source is applied between the source and sink nets to evaluate the overall voltage drop in the loop. The loop impedance value can be calculated based on the voltage drop and input current. A significant improvement in speed and memory has been achieved while maintaining the same extraction accuracy for the loop-based method compared to FEM and PEEC models. For a 2D case, the model has shown 56 times speedup with 6% accuracy compared to ANSYS Q3D results. Though this method is efficient for 2D layout cases, rigorous testing for 3D layout evaluation is ongoing. Therefore, in this work, FastHenry [82] is used for the electro-thermal optimization case study for 3D layouts.

Thermal Modeling: PowerSynth 2 has two options for thermal performance evaluation. Firstly, ParaPower [75] developed by the Army Research Lab is linked with PowerSynth 2 by my colleague Tristan Evans for accurate thermal performance evaluation of 3D layouts. Secondly, the built-in transient thermal model [44] can predict both static and transient thermal performance of 2D layouts with a 3500 times speedup while keeping the accuracy within 10% compared to ANSYS Fluent. This transient model can report maximum, average, and peak-to-peak temperature for each layer. Though ParaPower can be used for transient simulation, the built-in model is 316 times faster than ParaPower and hence more suitable for optimization. In this work, ParaPower has been used for static thermal performance evaluation of the 3D MCPM layout.

Layout Optimization and Finishing: In PowerSynth 2, two optimization algorithms are implemented: A built-in randomization method and a Non-dominated Sorting Genetic Algorithm II (NSGAII) [41]. The randomization method generates the solution space and performs performance evaluation using the corresponding models. Then, a non-dominated sorting is applied to generate the Pareto-front solutions. On the other hand, the genetic algorithm approach takes the number of generations as input and applies crossover and mutation to spawn a new generation of the solutions. Based on the ranking, a subset is passed to the next generation. This procedure continues until it reaches the maximum number of generations. In this process, the layout is represented by a design string that is created by concatenating the longest path weights

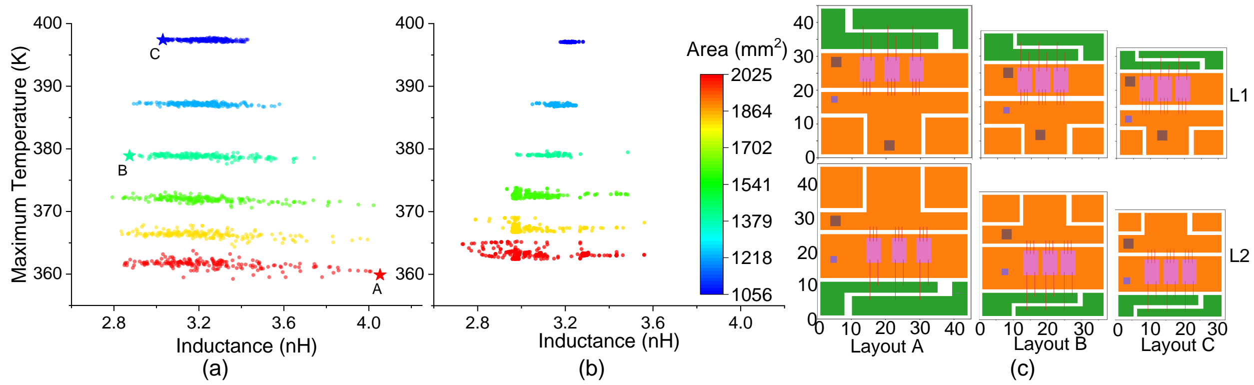


Figure 25: Solution space generated by PowerSynth 2 using (a) Randomization, (b) NSGAII, (c) 2D view of the three selected solutions

of each node and iterating through the hierarchy tree. In this work, both the native randomization and non-dominated sorting genetic algorithm (NSGAII) have been used to perform electro-thermal optimization. In randomization, both uniform distribution and truncated normal distribution functions can be used to generate new solutions. The genetic algorithm workflow is summarized in Figure 23 with user-tunable configurations. Since randomization is the key to the layout generation workflow, for each longest path, the extra room is distributed among the edges according to the design string generated by the optimizer. When a solution is generated from the design string, it is evaluated by the performance models and follows the genetic algorithm steps to create a new design string. Finally, PowerSynth 2 reports the solution space and Pareto-optimal solution set in a user-interactive solution browser. A particular solution of interest can be selected and exported to commercial 3D CAD tools from the Pareto-front. In addition, any post-layout optimization like filleting of the sharp corners can be performed to improve manufacturability and yield. Finally, the design can be taped out for fabrication.

5.3 Supported High-Density Power Packaging

A high-density MCPM layout can be achieved with four types of 2D/2.5D/3D packaging technologies. The 2D planar power loop can be converted into a vertical loop to reduce the power loop parasitics. Double-sided cooling or embedded cooling can improve the thermal performance of the high-density layouts. However, in some cases, the fabrication complexity can be

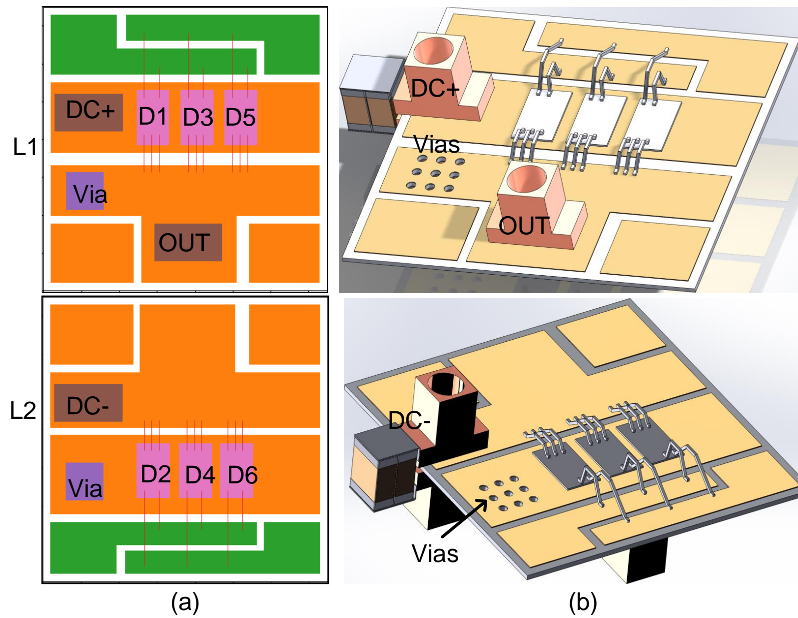


Figure 26: (a) Modified layout of solution B, (b) exported 3D structure

significantly increased due to the compact placement and routing of components in a multi-layered fashion. Each of these packaging technologies is described and demonstrated using PowerSynth 2.

Flip-Chip Module: In flip-chip designs, the devices are connected in a flipped fashion with the routing traces. Figure 24 (a) shows a half-bridge 2D flip-chip module that has solder balls for connecting the gate, source, and drain with traces. The drain has an extended metallic connection that converts the typical vertical device into a planar one. In this configuration, no via is used, and the OUT trace has high-side devices' sources and low-side devices' drains on the same plane. Flip-chip 3D module needs multiple DBCs, and the fabrication complexity of such designs is much higher compared to the wire bonding technology.

Hybrid 3D Module: A hybrid 3D module refers to the package where both wire bond and metallic post-type connections are used. Wire bonding is used for gate and kelvin source connections, whereas metallic post connectors are used for power loop connections. The initial 3D structure and minimum-sized solution generated by PowerSynth 2 are shown in Figure 24 (b). Here, two DBCs are connected face-to-face through metallic post-type connections. The L1 layer has the OUT terminal and low-side devices' drain connections. The sources (S) are connected to

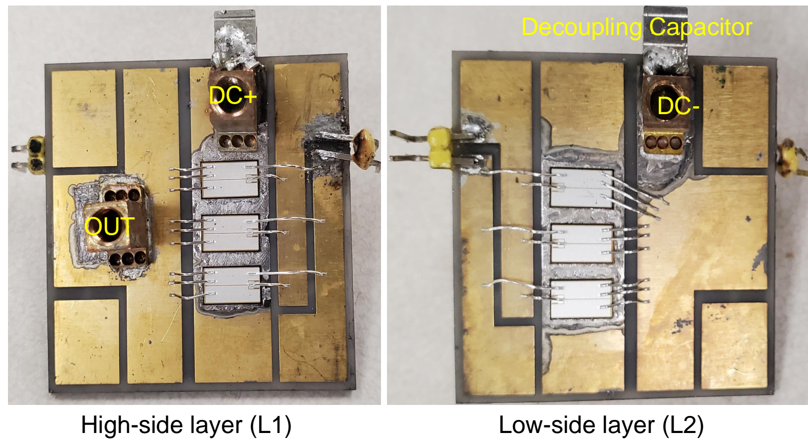
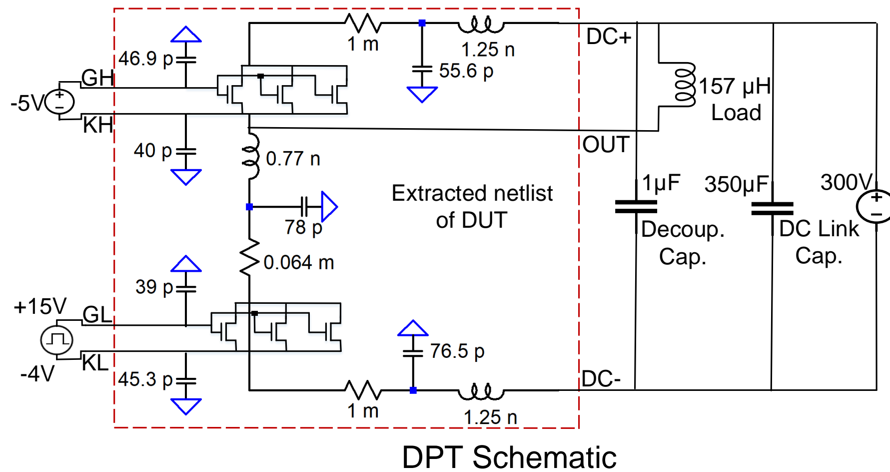


Figure 27: Fabricated 3D module

the L2 layer through metallic posts. L2 layer has DC+ and DC- terminals, as well as high-side devices' drain connections. Double-sided cooling can be enabled by attaching heat sinks on both sides. However, the power loop area is increased due to the planar part. To make a vertical power loop, four routing layers are required, where there needs to be one through DBC via type connection as shown in [85]. However, the metallic post attachment to the device source pads is a challenging task as there is no established recipe for that.

Wire-Bonded 3D Module: A sample 3D structure of the wire-bonded 3D module is shown in Figure 24 (c). The planar view of each layer of the 3D structure is shown in Figure 18 (a). Here, the bottom layer (L1) consists of high-side power devices, gate and kelvin source connections, DC+ and OUT terminals. The top layer (L2) has low-side power devices with gate and kelvin source connections and DC- terminal. A through ceramic via is used to connect both layers' OUT traces. Thus a 3D half-bridge wire-bonded layout is created using two routing layers. Since devices are on both sides of the structure, heat sink attachment is not possible for thermal management. Therefore, a direct-bonded copper (DBC) ceramic board with an embedded cooling channel is required for the best thermal performance. The current rating of such design is limited by the number of parallel vias and their diameter. Another wire-bonded structure is possible using two substrates and replacing the through DBC vias with metallic posts, where the face-to-face stacking of the devices is required, as shown in [87]. In such structures, the heat sink



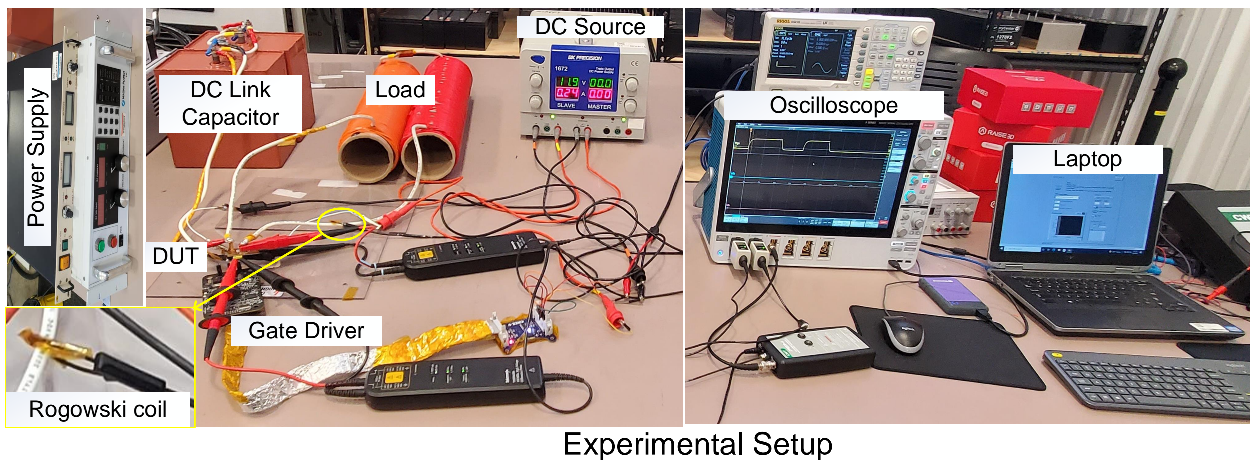


Figure 28: Double pulse test schematic and experimental setup

can be attached to both DBCs, and the volume between two device layers can be filled with encapsulant gel or LTCC interposer for electrical isolation. Though this structure can have cheaper thermal management than embedded cooling, the fabrication complexity is much higher than the single substrate through ceramic via case as the metallic post connection is required between two substrates.

Wire-Bondless 3D Module: From the literature, it is evident that the bonding wire in the power loop is the critical part that contributes to the loop parasitics and is more prone to failure compared to other parts in the module. Eliminating the wire bonding, wire-bondless 3D designs are investigated. Figure 24 (d) shows a sample 3D wire-bondless structure with per-layer layouts. Here, three DBCs have been used to form a half-bridge module. Among the four routing layers, L2 and L3 are connected through a via. L1 layer has a DC+ terminal, and high-side devices with

Table 7: Performance metrics for the three selected layouts

Layout ID	Inductance (nH)	Max Temperature (K)	Size (mm × mm)
A	4.05	359.87	45 × 45
B	2.87	378.88	37.5 × 37.5
C	3.03	397.41	32.5 × 32.5

both source (S) and gate (G) connections are ported to the L2 layer through metallic posts. The L3 layer has the low-side devices' drains, which sources (S) and gates (G) are connected to the L4 layer that contains the DC- terminal.

5.4 3D Layout Optimization Case Study

Though PowerSynth 2 can optimize all the above-mentioned packaging technologies, 3D CAD-flow validation through hardware prototyping depends on complexity, cost, and equipment for module manufacturing. Considering the fabrication complexity, the wire-bonded 3D module design has been chosen (shown in Figure 24 (c)). This layout has a few benefits over any 2D design: a vertical power loop, reduced footprint size, embedded cooling opportunity, etc. Throughout the optimization process, PowerSynth 2 does not change the relative locations of the components. Due to this limitation, the initial layout of the module needs to be designed carefully to reduce coordinate correlation among components. Also, the fabrication steps need to be planned as both sides of the single DBC have devices. In this section, the electro-thermal optimization flow of PowerSynth 2 using the 3D wire-bonded module is demonstrated.

5.4.1 Layout Optimization

The optimization target is reducing power loop (from DC+ to DC-) inductance and static maximum junction temperature. FastHenry [82] is used for loop inductance extraction, and ParaPower [75] from Army Research Lab is used for static thermal evaluation. Before optimizing the layout, the electro-thermal performance of the minimum-sized solution (shown in Figure 24 (c)) is evaluated. Since the 3D structure has bare devices with wire bonding on both sides, there is

no baseplate attached to this design. For thermal performance evaluation, a heat transfer coefficient on an even surface is required as an input to the ParaPower interface. To have an even surface, the 3D structure is considered to be encapsulated with silicone gel (thermal conductivity 0.2 W/mK) with a thickness of 0.5 mm on both sides. To mimic the forced air cooling, the heat transfer coefficient of 350 W/m^2K is applied on both sides of the encapsulated DBC substrate (Cu/ AlN/ Cu) with filled Cu vias. The ambient temperature is set to 300 K. The power loop inductance is found 3.26 nH at 1 MHz, and the maximum junction temperature is found 381.68 K for 2.5 W heat dissipation for each device. Since the minimum-sized solution provides the most compact solution, to optimize this layout assuming the same boundary conditions, six different floorplan sizes are considered ranging from 1056 mm^2 to 2025 mm^2. For each floorplan size, both randomization and NSGAII are used to generate solution spaces. The result is shown in Figure 25. For randomization, each floorplan size has 200 solutions, and the runtime for solution generation and evaluation is 100 s, and 2500 s, respectively. On the other hand, for the NSGAII, the number of generations is varied from 25 to 35 with the increasing floorplan size. The average runtime for each solution is approximately 1 minute. Since NSGAII generates and evaluates one solution at a time, parallelization on performance evaluation is not possible. Therefore, the runtime is higher than the randomization. From the solution space plot, NSGAII finds better solutions with larger footprints but has a narrower solution space than randomization. From both solution spaces, the balanced solution can be chosen and fabricated. In this study, the optimized layout is chosen from the randomization solution space. Because for the same footprint size ($<$1800 mm^2), it has a better electrical performance. However, tuning NSGAII parameters (crossover, mutation, etc.) might lead to similar results with randomization. To demonstrate design variation, three corner solutions have been chosen from the randomization solution space and labeled in Figure 25 (a). The planar view of each layout is shown in Figure 25 (c). The performance metrics comparison is shown in Table 7. From the layouts, it is evident that Layout A has the highest footprint with higher loop inductance and a lower temperature rise. Layout C has the smallest floorplan size with the highest temperature rise and relatively lower loop inductance. Layout B shows the

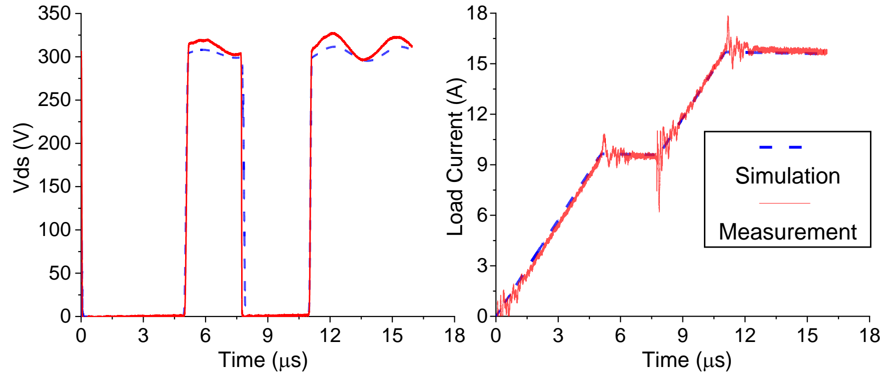


Figure 29: Double pulse test comparison on Vds and load current

tradeoff between two objectives and achieves a balanced electro-thermal performance.

5.4.2 Post-Layout Optimization

The selected layout B has been further tuned before taping out for fabrication. Since the optimization target was to reduce the power loop inductance, the gate loop in the L2 layer is not optimized. Therefore, the OUT trace width in the L2 layer is further reduced, and the width of the DC- trace is increased by 1.5 mm. A 3×3 via array is used to enhance the current rating. These post-layout optimizations helped in reducing the gate and kelvin source wire bond lengths as well as the power loop length. This modified layout has a power loop inductance of 2.77 nH at 1 MHz. The updated layout has been exported to SolidWorks for 3D rendering. The final layout and exported 3D model are shown in Figure 26. In the 3D model, the decoupling capacitor is also shown between DC+ and DC- terminal.

5.5 Experimental Results

5.5.1 3D Power Module Fabrication

The CAD drawing of the optimized layout is fabricated with a gold-plated DBC substrate (0.1 mm Cu/ 0.5 mm AlN/ 0.1 mm Cu). The gate and kelvin source headers are chosen according to the gate driver interfacing pins. The power leads are machined from copper bars at the High Density Electronics Center (HiDEC). CPM3-0900-0010A SiC devices from CREE are used for

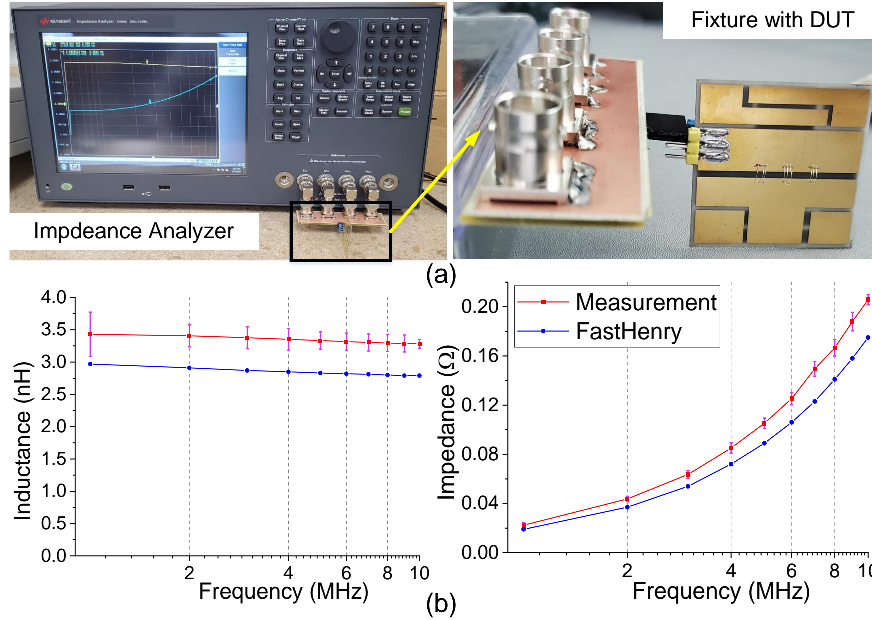


Figure 30: (a) Impedance measurement setup and (b) result comparison for the power loop

the module. All these parts are assembled at HiDEC to manufacture the module. Two sets of graphite fixtures are machined to make the die and terminal attachment process smoother. One set of fixtures is used for high-side components assembly and another for the low-side. The attachment process is divided into two steps. Since the devices need to be attached on both sides of the DBC, the high-side layer components are assembled first using a Pb95/Sn5 preform solder material as it has a higher melting temperature (308 °C). The substrate is plasma cleaned priorly to remove any organic residue. Then, a vacuum furnace performs the attachment process. For low-side components, the Sn63/Pb37 eutectic solder paste with a lower melting temperature (183 °C) is used. Then, the substrate is cleaned using the flux remover solution and plasma cleaner to remove any organic residue. Finally, the substrate is placed in another custom graphite fixture, and 12-mil automatic wire bonder is used to perform the wire bonding on both sides. Then, the 1 μF capacitor is soldered between the DC+ and DC- terminal edges. The final fabricated design is shown in Figure 27.

Table 8: Comparison between thermal measurement, ANSYS, and ParaPower

Case	Maximum Temperature (°C)			% of Mismatch
	D1	D3	D5	
Measurement	37.00	38.80	37.90	-
ANSYS	39.76	41.54	40.23	7.06%
ParaPower	40.75	42.30	40.78	9.02%

5.5.2 Functionality Verification

A double pulse test (DPT) is performed to validate the functionality of the assembled module. The test setup of the DPT is shown in Figure 28. CGD1700HB3P-HM3 from CREE is used as the gate driver. The load inductor used in the setup has an inductance of 157 μH. As the module has no encapsulation, the test is performed at a 300 V/15 A rating for safety considerations. PowerSynth 2 extracted parasitic netlist (shown in Figure 28) is used to simulate the double pulse test. The Vds, and load current waveform comparison are shown in Figure 29. The current is measured using a mini Rogowski coil around the wire, adding some noise to the collected data. The maximum voltage overshoot of Vds is approximately 27 V. The low-frequency ringing in the Vds is due to the 1 μF decoupling capacitor used in the module. This capacitor has to be used to decouple the parasitics from the external connections as there is no custom busbar used in the test setup. Both voltage and current waveforms are within acceptable accuracy for simulation compared to the measurement results. A 200 MHz voltage probe has been used for voltage measurement. From the Vds waveform, there shows no high-frequency ringing at the turn-off cycle in both simulation and experiment. This is because of low parasitic inductance, high gate resistance (5 Ω from the gate driver and 2 Ω from the device), high rise (400 ns), and fall (230 ns) time of the gate driver output signal, etc. Since the turn-off ringing frequency could not be measured from the experiment, the loop inductance cannot be verified through DPT. However, from the switching waveforms, it is clear that the assembled optimized module is fully functional.

Table 9: Summary of high-density packaging designs

Source	Architecture	Packaging	Power Loop Inductance (nH)	Cooling	Device Rating	Devices/ Sw. Position	Area ($mm \times mm$)
[88]	2D Phase-leg	Wire-Bonded	9.7 (Planar loop)	Single	1200 V/ 100 A	5 SiC MOS	88.1 × 50.1
[89]	2D Half-bridge	Wire-Bonded	7.5 (Vertical loop)	Dual	650 V/ 200 A	3 SiC MOS	60 × 80
[42]	2D Half-bridge	Wire-Bonded	7.44 (Planar loop)	Single	1200 V/ 40 A	1 SiC MOSFET	54.8 × 28
[36]	2D Half-bridge	Wire-Bonded	5.59 (Planar loop)	Single	1200 V/ 40 A	4 SiC MOSFET	60 × 40
[90]	2.5D Half-bridge	Hybrid	2.60 (Vertical loop)	Dual	1200 V/ 90 A	1 SiC MOS	40 × 37
[91]	2.5D Half-bridge	Hybrid	3.38 (Vertical loop)	Single	1200 V/ 24 A	1 SiC MOS	21 × 11.5
[92]	2.5D Half-bridge	Hybrid	4.3 (Vertical loop)	Single	1200 V/ 40 A	2 SiC MOS	23.7 × 14.2
[93]	2.5D H-bridge	Wire Bondless	4.5 (Vertical loop)	Dual	1200V/ 50A	4 SiC MOS	76.9 × 74.9
[44]	2D Half-bridge/ 2.5D Full-bridge	Wire-Bonded	8.33 (Planar loop)	Single	1200 V/ 40 A	2 SiC MOS	40 × 40
[94]	3D Half-bridge	Wire-Bondless	0.93 (Vertical loop)	Dual	650 V/ 60 A	2 GaN HEMT	45 × 35
[95]	3D Half-bridge	Wire Bondless	4 (Vertical loop)	Dual	1200 V/ 50A	2 Si IGBT	42.5 × 40.1
[96]	3D Half-bridge	Flip-chip	4.5 (Vertical loop)	Dual	900 V/ 194 A	2 SiC MOS	28 × 50.5
[96]	3D Half-bridge	Wire Bondless	5.1 (Vertical loop)	Dual	3300 V/ 50 A	2 SiC MOS	27 × 46.4
This Work	3D Half-bridge	Wire-Bonded	3.43 (Vertical loop)	Embedded	900 V/ 194 A	3 SiC MOS	37.5 × 37.5

5.5.3 Electrical Validation

To validate the power loop inductance, an impedance analyzer is used. For this test, another copy of the optimized via connected DBC substrate is used. In this device under test (DUT), no SiC devices are attached. For the power loop, wire bonds are used at the device locations. For each device position, three parallel 5 mil Aluminum wires are used. The module (DUT) image is shown in Figure 30 (a). A Keysight E4990A impedance analyzer is used to measure the loop inductance and impedance. Based on the sensitivity and frequency range of the analyzer, 1 MHz - 10 MHz is selected for this test. A custom PCB fixture (shown in Figure 30 (a)) is used to interface between the impedance analyzer BNC ports and the module design. An open and short calibration is performed before measuring the DUT. For short calibration, two similar connectors (DC+ and DC-) as used in the DUT are soldered at one side to nullify the terminal parasitics. The measurement results are shown in Figure 30 (b). For electrical model validation, a frequency sweep is performed within the selected frequency range, and both loop inductance and resistance data are collected. Shown in Figure 30 (b), the max inductance error is 13.4% (3.43 vs. 2.97 nH at 1 MHz) while the max impedance error is 12.5% (0.20 vs. 0.175 Ω at 10 MHz). There are several uncontrollable factors: (a) From the impedance analyzer datasheet, it is evident that for the low impedance measurement case (< 200 mΩ), the analyzer itself has a 10% error that decreases with the increasing frequency (Figure 30 (b)); (b) The short calibration cannot perfectly nullify the terminal impedance impact as the short terminals are not connected exactly the same way as those are in the module. Though the absolute mismatch is around 13%, considering the very low impedance and the analyzer error, the measurement is still close to the model prediction. This experiment is carried out with the help from my colleague Quang Le.

5.5.4 Thermal Validation

The simplified boundary conditions used in the optimization flow are challenging to reproduce in the lab environment due to several reasons: (a) Encapsulant gel is not used for the fabricated module, which makes it impossible to create an even surface on both sides of the module; (b) The

assumed heat transfer coefficient is for forced air cooling on both sides, which is hard to achieve in such small scale experiment setup as no direct relationship is found in the literature with low fan speed and heat transfer coefficient; (c) More complicated equipment is required to match the heat transfer coefficient of the forced air cooling. Such a high-density power module cannot be used reliably without any active cooling. Therefore, an alternative cooling method is proposed. A custom DBC can be manufactured that has an embedded liquid cooling channel by adding some electrical impedance overhead in the power loop, as shown in Figure 31. To demonstrate the thermal solution, a cold plate is used for active cooling, resembling the embedded cooling channel. For this test, only the high side of the half-bridge module is assembled and attached on top of the cold plate, as shown in Figure 32, using a silicone-based interfacing material (thermal conductivity 13.9 W/mK). A DC power supply is used for providing current through the devices. A multimeter is used to measure the voltage drop across the devices. A coolant loop with water cooling (flow rate 0.5 gallons/min) is set up through the cold plate. A thermal camera from FLIR is used to record the temperature of the module. The devices are connected to operate in diode mode (higher resistance) as the purpose is heat generation only. At 15 A supply current, total heat dissipation across three parallel devices is 30.6 W. The inlet and outlet temperatures of the cold plate are 22.2 °C, and 22.43 °C, respectively. The measured case temperature is 25.6 °C. The resultant IR image is shown in Figure 32. Based on Newton's law of cooling, the effective heat transfer coefficient is approximately 7394 W/m^2K. This heat transfer coefficient is applied on the bottom side, and 10.2 W power is provided for each device in the ParaPower evaluation. The ambient temperature is set to the same as the experiment (24 °C). The maximum junction temperature from ParaPower thermal model is 42.30 °C. For the same boundary condition and module structure, ANSYS Workbench has reported 41.54 °C as the maximum temperature. The comparison result for each device among different sources is shown in Table 8. From the results, it is clear that ParaPower predicted temperature is within 10% error. A few factors in the measurement cannot be considered in simulation, such as measurement equipment (power supply, multimeters, thermocouple, IR camera) accuracies, voids in the solder attach, and heat dissipation

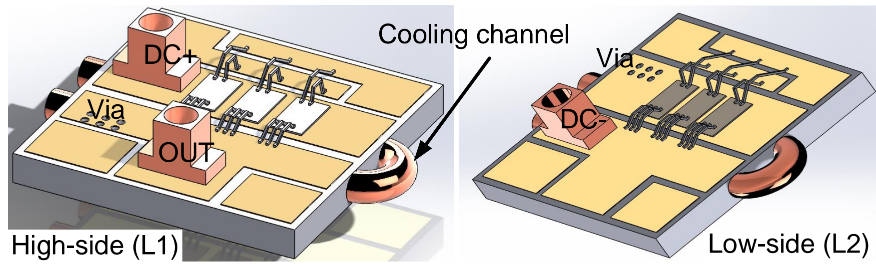


Figure 31: Proposed embedded cooling structure

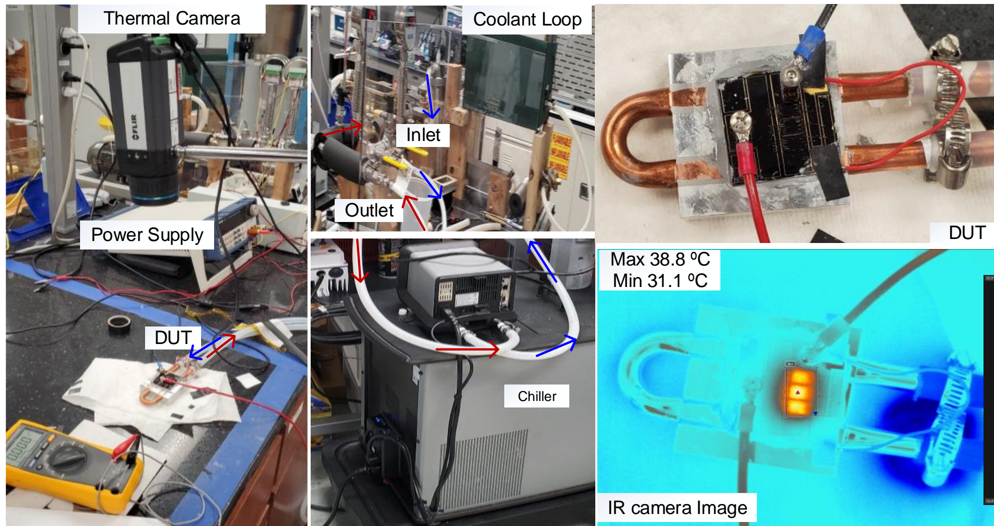


Figure 32: Thermal test setup and temperature measurement result

through radiation. Therefore, the equivalent heat transfer coefficient is not 100% accurate. However, the overall thermal result still agrees with the model prediction.

5.5.5 Comparison with Other High-Density Designs

Since there is no design tool like PowerSynth 2 that can optimize 2.5D/3D high-density module, the optimization results are compared against mostly manual designs. However, there are two 2D half-bridge module design cases, which are optimized by the automated methodology proposed in [42], and [36]. Compared to these two optimization results, PowerSynth 2 has achieved significant speedup with comparable performance values. For example, PowerSynth v1.9 optimized module [44], which is also generated by PowerSynth 2 and took only 1,288 s for 100 generations, whereas the methodology in [36] took almost 5,400 s for 30 generations, and [42]

took 266,343 s for 10 generations of NSGAII. The optimized design from [36] has a lower power loop inductance as they have two parallel power loops with two snubber capacitors. Most of the commercial modules from the power electronics industry are wire-bonded 2D designs. Therefore, high-density (2.5D/3D) power module designs are mainly found in the literature. However, as a reference design, a commercial wire-bonded 2D phase-leg module [88] is considered for comparison shown in Table 9. The table clearly shows that 2D/2.5D wire-bonded modules generally have a higher loop inductance than other packaging technologies. From Table 9, it is clear that PowerSynth 2 optimized 3D design has achieved comparable or better performance compared to all other manual designs. Provided the necessary manufacturing capabilities, PowerSynth 2 optimized design can achieve 372.48 W/mm^2 power density, which is the highest power density in bare modules compared in the table. The power loop inductance value is not the lowest since most of the inductance comes from the wire bonds. However, the vertical power loop has a reduced loop inductance compared to most of the other 3D designs. Therefore, it is clear that PowerSynth 2 optimized design can even outperform many manual designs with SOTA manufacturing capability. Though the embedded cooling concept is not fully implemented in the manufactured module, PowerSynth 2 can optimize design prototypes to push the power packaging industry toward higher power density.

5.6 Limitations

Since PowerSynth v2.0 is an extended version from the baseline methodology presented in PowerSynth v1.9, there are some limitations, which couldn’t be addressed in this version. The key limitations are as follows.

1) The initial layout dependency and inability to perform non-Manhattan routing.

2) The NSGAII implementation needs improvement to determine the stop criteria intelligently. Currently, the criteria is only the maximum number of generations. Checking for performance improvement tolerance needs to be added as another stopping criterion to improve runtime.

3) The variable-sized floorplan generation algorithm needs to be improved to explore a larger solution space. The current implementation performs multiple fixed-sized solution generation runs for some arbitrary floorplan sizes generated based on the user-provided number of layouts.

4) The GUI of PowerSynth v2.0 is still attached to the command line flow, which needs to be more flexible for the users.

5) The solution browser needs to add 3D layout visualization and rendering feature.

6) Though PowerSynth 2 can perform more than two performance optimization from a methodology perspective, the current version is allowed to set only two objectives at a time.

Chapter 6

Reliability Optimization Using PowerSynth

PowerSynth's modular architecture and hierarchical layout engine has enabled performing reliability optimization studies alongside the electro-thermal optimization of MCPM layouts. Reliability optimization has been performed from two perspectives: (a) Thermal cycling impact minimization, and (b) Electromigration impact minimization. The methodologies and key results are for each perspective are described below.

6.1 Optimization for Reducing Thermal Cycling Impact

Existing efforts stated in the literature review (Section 2.2.1) have some obvious drawbacks such as the limited solution space from the parameterized approach and the requirements of customized models for different failure mechanisms. Besides, no prior work has considered the layout placement and routing impact as all methods involve highly time-consuming FEM simulations. To incorporate thermal cycling impact optimization, PowerSynth v1.3 has been considered. The code base has been updated to incorporate the following changes: (a) Adding phase change material (PCM) in the layer stack, (b) Parameterizing the layer stack thickness and material, (c) Integrating a fast and accurate transient thermal model. The methodologies and key results are described below.

6.1.1 Methodology

Optimization Flow Overview: To optimize the reliability of a power module, two aspects have been considered in this work. One is to suppress temperature spikes from the thermal cycling by guiding the designer towards an optimum layer stack of materials and thickness. Another one is varying the placement and routing of the components to reduce electrical parasitics and junction temperature. To accumulate both of the steps in an automated CAD flow, a two-folded optimization approach is demonstrated using PowerSynth. The overview of the approach is

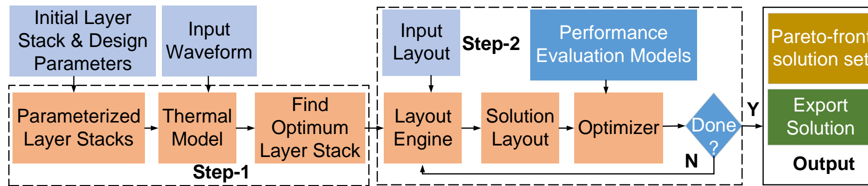


Figure 33: Two-step optimization flow

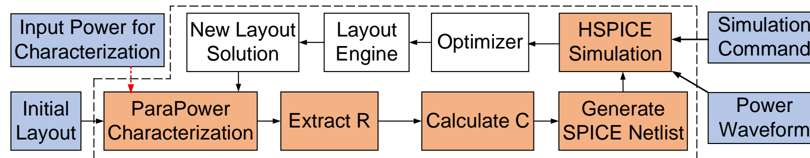


Figure 34: Thermal model workflow

shown in Figure 33.

For optimizing the performance during thermal cycling, it is important to absorb the heat generated by power devices. To start with a reasonable threshold value for maximum junction temperature under a given thermal cycling waveform, an optimum layer stack is necessary. Therefore, in the first step, the layer stack parameters like materials and thickness are varied to find an optimum layer stack for heat buffering and dissipation. In this version of PowerSynth, the order of stacking material and components can also be varied. Since the previous fast thermal model [38] cannot predict the transient behavior, a new thermal model has been developed to predict maximum, average and peak-to-peak temperature for the given thermal cycling waveform. Based on the user's choices of parameters (i.e., thickness, material) associated with the layer stack, this newly developed model has been used to generate a solution space that represents the tradeoff among the parameters. An optimum layer stack is chosen from the solution space and fed into the next step to perform electro-thermal optimization by varying placement and routing with a set of different floorplan sizes. For each floorplan size, a pre-defined number of solutions is generated, and the complete solution space is saved in the solution database. A non-dominated sorting is applied to generate the Pareto-front solution space. From the Pareto-front, users can choose any solution to export and fabricate.

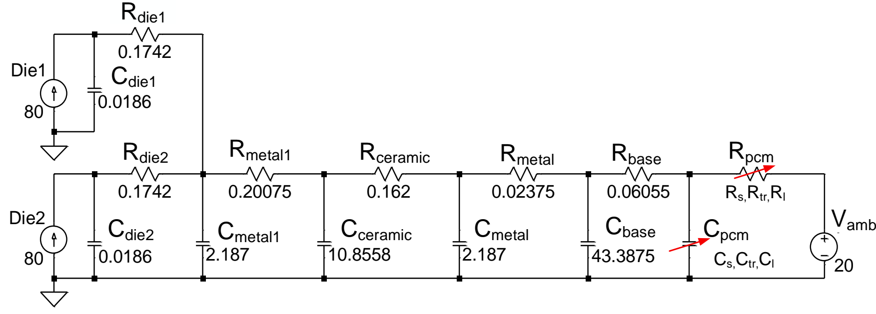


Figure 35: Cauer thermal network for the test structure (shown in Figure 38(a))

Transient Thermal Model: The transient thermal model represents an MCPM structure as a compact 1D Cauer thermal RC-network [66] to have a fast evaluation. The HSPICE engine has been used to solve the network to extract each layer temperature. In a Cauer network, each layer of the MCPM structure is represented as an equivalent RC-block. As long as each layer material has constant thermal conductivity and heat absorption capability, the RC conversion is straight-forward. However, as the PCM layer can change the physical state due to temperature rise during MCPM operation, it has a variable thermal conductivity and heat absorption capability. Therefore, the equivalent RC-network (shown in Figure 35) for the PCM layer is modeled with a variable capacitor and a variable resistor. This capacitance and resistance value is temperature-dependent. Thus, in the electrical network, it is voltage-dependent. For organic PCM, the variable resistance and capacitance values are shown in Figure 36. The thermal modeling flow has been summarized in Figure 34. The model has four important steps described below.

Model Characterization through ParaPower: In the model workflow, there is a characterization step, which is required to account for the impact of any change in the structure. Since the complete optimization methodology involves two steps and the thermal model is used in both of them, this characterization phase of the model is subject to turn on or off depending on the current step. In the first step, where the layer stack material and thickness are parameterized, each solution structure is different. So, structure characterization is required to get the thermal resistance value of each layer. However, in the second step, where the placement and routing of the trace and device layer are varied, a temperature and heat flux contour mapping

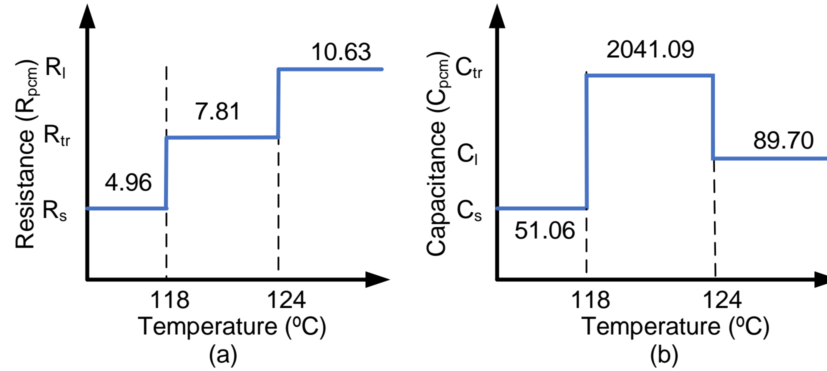


Figure 36: Variation of (a) thermal resistance, (b) thermal capacitance for organic PCM (Erythritol) against temperature

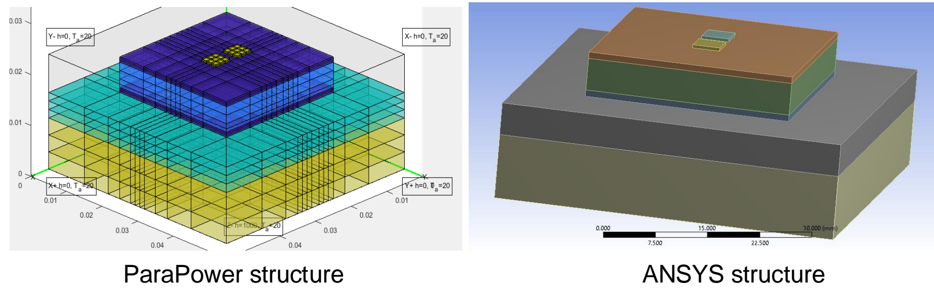


Figure 37: Test structure in the state-of-the-art tools

methodology [38] has been adapted to bypass the characterization for each solution. In this methodology, each layer stack is characterized once, and the resultant temperature and heat flux distribution on the ceramic layer are saved as rectangular contours. In the optimization phase, the change in trace layout and device position impact is reflected by placing each device's characterized temperature distribution in a superposition and considering the interaction of each device's heat flux distribution with the current trace layout. So, in the case of step-2, the characterization is run only once. Bypassing the characterization phase makes the thermal evaluation much faster within acceptable accuracy. However, if the layer stack contains PCM, the error from this method increases in some cases. To improve the accuracy in such cases, the runtime is increased by about 13 times as the characterization step can not be bypassed.

Thermal Resistance Extraction: To construct a Cauer thermal RC network of an MCPM structure, the thermal resistance (R) of each layer needs to be extracted. The R-values are

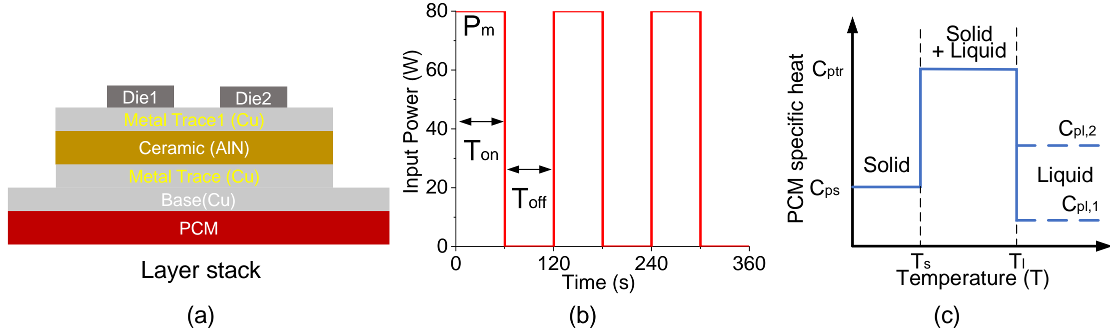


Figure 38: (a) Layer stack of the test structure, (b) model validation result input power waveform, (c) specific heat variation of PCM against temperature.

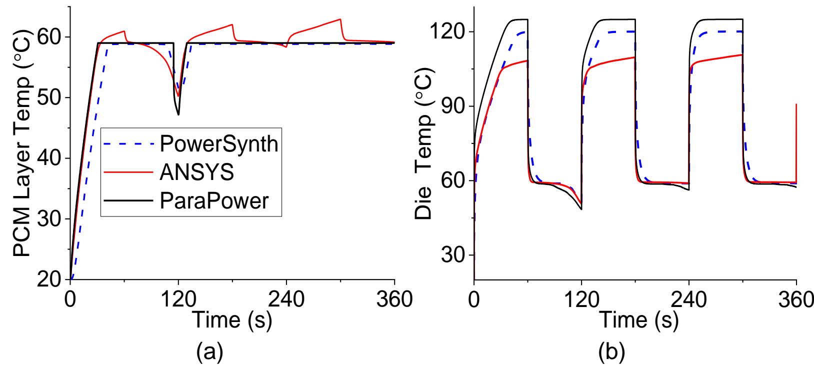


Figure 39: Maximum temperature result comparison for the input waveform shown in Figure 38 (b): (a) PCM layer, and (b) die layer.

extracted from the characterization results. A static (transient) thermal simulation is performed in ParaPower using a pre-defined heat dissipation for each die in the non-PCM (PCM) layer stack. Each layer's maximum temperature is fed back to PowerSynth. Since the temperature of each layer is known, the temperature difference (ΔT_{ij} in K) can be found by subtracting the temperature (T) of layer j from layer i. Thus, each layer's R-value can be computed using Eq. (1), where R_j, P_j are thermal resistance (K/W), and heat flow (W) of layer j, respectively.

$$R_j = \Delta T_{ij}/P_j \tag{1}$$

To capture PCM layer resistance in both solid and liquid states, two sets of temperature values are considered by performing the characterization twice: one with a lower heat dissipation that ensures the PCM layer is not melted and another with a higher heat dissipation for each die that

ensures the melting of the PCM.

Thermal Capacitance Calculation: The capacitance value for each layer is calculated by inserting the material properties in Eq. (2).

$$C_j = Volume \times Specific\ heat \times Density \tag{2}$$

Here C_j is the capacitance (Ws/K) of layer j, and other properties (corresponding SI units) are associated with the material of layer j. However, as the PCM layer has different specific heat (shown in Figure 38(c)) and densities in different states, the variable capacitance value is calculated in a piece-wise fashion. A PCM layer has three specific heat values as well as three capacitance values. Here, C_{ps}, C_{pl}, C_{ptr} are specific heat value at solid, liquid and transition state, respectively. Depending on material properties, specific heat in liquid can be greater or less than that in the solid. However, in the transition phase, it has a very high value.

$$C_{ptr} = C_{pavg} + L_v/(T_l - T_s) \tag{3}$$

Here, T_s, and T_l represent the solidus and liquidus temperature of the material. C_{ptr} is calculated using Eq. (3), where C_{pavg} is the average specific heat of C_{ps} and C_{pl}. L_v represents the latent heat of the material. For each region, depending on the voltage (temperature) of the PCM layer, the capacitance value is calculated and used in the RC network.

HSPICE Netlist Creation & Simulation: Once R and C values are known for each layer, a SPICE netlist is written in a file for the Cauer thermal network (shown in Figure 35). PCM resistance and capacitance are inserted using HSPICE voltage-dependent resistance (GRes) and capacitance (GCap) elements. With these elements' syntax, the waveforms shown in Figure 36 can be represented easily. Each die is mapped as a current source, and the heat dissipation value (waveform) is set as the current value (waveform) for each source. Finally, a voltage source is added with the value of the ambient temperature at the end of the network. For simulation, the heat dissipation value (waveform) and simulation command (i.e., transient simulation runtime)

Table 10: Layer stack properties of the test structure in Figure 38(a)

Layer Name	Dimension (mm)	Thermal Conductivity (W/m-K)	Density (Kg/m^3)	Specific Heat (J/kg-K)
Die (SiC)	4×4×0.5	120	3100	750
Trace (Cu)	30×30×1	390	8900	390
Ceramic(AlN)	30×30×5	170	3260	740
Baseplate (Cu)	50×50×5	390	8900	390
PCM (Metal)	50×50×10	18.9-18.5	7900-7700	300-250

are taken as input from the user. Depending on the metric of performance evaluation, the HSPICE measure statement is used to calculate the maximum, average, peak-to-peak (P-to-P) voltage (temperature) of each node (layer) in the network. This netlist file is provided as an input to the HSPICE engine and the result is saved in an output file in CSV format. This file is read in to report the performance metric value in the optimization loop. However, other than just computing the performance metrics, in HSPICE, a sweep of input power waveform parameters (i.e., maximum power, period) can be performed to compare the performance against different waveforms. This approach has been used in Section IV to get Figure 40 energy sweep results.

6.1.2 Thermal Model Validation

To validate the proposed model, a simple layer stack shown in Figure 38(a), with two SiC devices is considered. In the PCM layer, a metallic PCM (Fields' Metal [97]) has been used, which melting temperature is 59 °C. Each layer's dimensions and material properties are shown in Table 10. For the PCM layer, solid and liquid phase values are shown in the table. In this case, the ambient temperature is considered as 20 °C and a heat transfer coefficient of 1000 $W/m^2 - K$ has been provided at the bottom face of the structure. To characterize the structure using ParaPower, each die consumes 80 W power. The corresponding ParaPower and ANSYS structures are shown in Figure 37. Then, a pulsating waveform shown in Figure 38(b), is supplied to each die to compare the temperature of different layers in the structure with the transient thermal model. The resultant PCM and die layer temperature have been shown in Figure 39(a) and (b), respectively.

The temperature difference, runtime, and memory usage comparison for our model against

Table 11: Runtime and memory comparison between ANSYS, ParaPower, and PowerSynth model

Approach	Max. Temp. (°C)	Avg. Temp. (°C)	P-to-P Temp. (°C)	Avg Runtime (s)	Speedup	Memory (MB)
ANSYS	110.7	84.87	51.73	11165	1×	3373
ParaPower	125	90.64	68.67	35.27	316×	2361
PowerSynth	120.1	89.57	61.14	3.2	3489×	315

the state-of-the-art tools with the test structure have been shown in Table 11. As this comparison is for a PCM case that requires characterization for each solution for the proposed model, the runtime is higher than the non-PCM case due to characterization runtime. For the non-PCM case, the average runtime of the PowerSynth model is only 0.31 s (excluding single characterization runtime of about 12 s). For 500 solutions, in the PCM case, the total runtime is found approximately 1600 s. As the HSPICE engine has been used to solve the RC-network, the runtime for solving each network is only 0.14 s. The results show that the PowerSynth model can predict an MCPM structure temperature with very good accuracy at a significant speedup compared to the state-of-the-art tools for a given thermal cycling waveform. Therefore, our model can be used in the optimization loop to optimize the MCPM structure for both static and transient thermal performance.

6.1.3 Optimization Results

Layer Stack Optimization: To perform reliability optimization, the initial layer stack is considered similar to the one shown in Figure 38(a). An example half-bridge power module layout is shown in Figure 42(a). A waveform similar to Figure 38(b) is used as thermal cycling input power for each device. The input layer stack has a 3mm PCM layer and a 1mm copper baseplate. Two sample PCM materials are studied in this case: metallic PCM (Fields' metal) and organic PCM (Erythritol [98]). Since PCM has a lower thermal conductivity with higher heat absorption capacity, the optimized amount of PCM can reduce temperature fluctuations as well as stress for a power module. Therefore, the energy supplied to the power module in each cycle is varied by sweeping two variables of the input power waveform: a) duty cycle (T_{on}) and b) maximum power (P_m) for each cycle. For both of the cases, the behavior of the PCM is similar as supplied energy is the key determinant. The result from the duty cycle variation is shown in Figure 40. From the results, it is evident that on the metric of maximum transient temperature in Figure 40 (b): PCM usage is advantageous within its thermal buffering limit but worse once all materials are melted. For the average temperature in Figure 40(a), organic PCM is worse for the

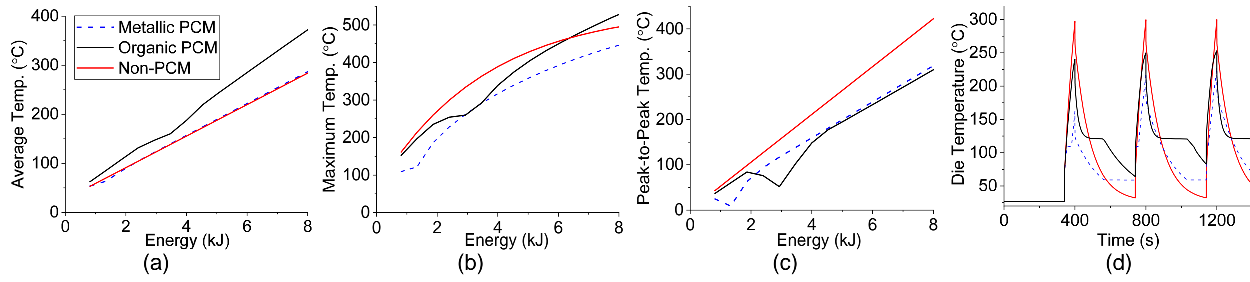


Figure 40: Energy sweep result for three metrics: (a) average, (b) maximum, (c) peak-to-peak, and (d) maximum transient temperature waveform comparison for device layer.

complete range and metallic PCM, and the non-PCM case has a similar response. For the peak-to-peak temperature metric in Figure 40(c), the PCM case is always better than the non-PCM case. Depending on this experiment, a thermal cycling waveform with 40 W maximum power and a duty cycle in between 5%-to-15% can be chosen as an input waveform. For this input waveform, the maximum device temperature comparison among non-PCM, organic PCM, and metallic PCM cases is shown in Figure 40(d).

Upon selecting a suitable thermal cycling waveform, reliability optimization is performed. In this study, for step-1 optimization, the baseplate and PCM layer material and thickness are varied. However, other layers' material and thickness can also be varied. To find the optimum thickness for both baseplate (copper) and PCM (organic, metallic) layers, three metrics (i.e., maximum, average and peak-to-peak temperature) are considered. They affect the failure mechanisms like thermal over-stress associated with material limits, thermal degradation modes, and thermo-mechanical fatigue, respectively. These metrics are plot against the PCM thickness in Figure 41. From the figure, it is clear that metallic PCM usage is advantageous for all three metrics compared to the organic PCM (Figure 41 (a)). Figure 41(b) shows that a 15 mm thick PCM layer with a 3 mm thick copper baseplate is optimum from the thermal reliability perspective. In the current order of layer stack, organic PCM has marginal benefits over the non-PCM case because the thermal conductivity of the organic PCM is quite low compared to the metallic one. If the PCM layer can be placed on top of the devices (close to the heat source), it would show a large temperature reduction. Due to the limitation of layer stack representation, such case will be considered in future work.

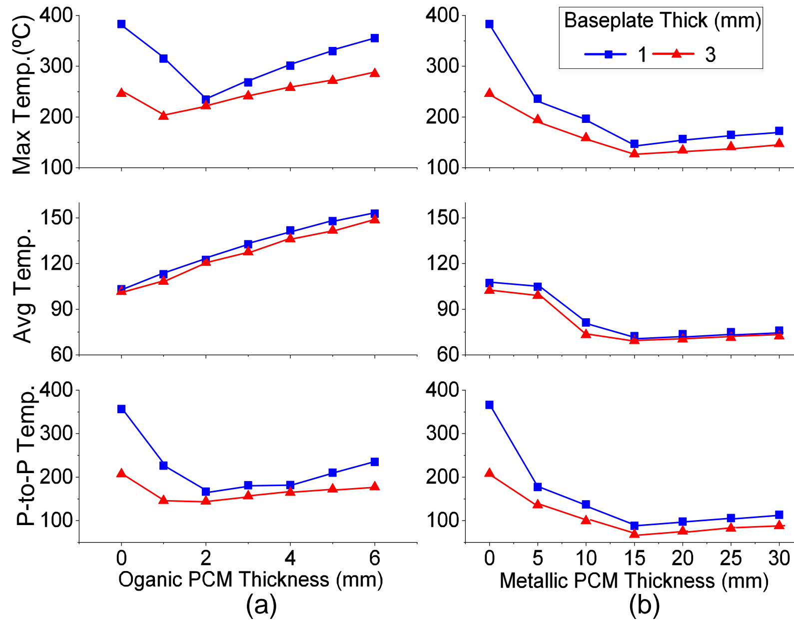


Figure 41: Multiple temperature metrics vs. layer thickness: (a) organic PCM case, (b) metallic PCM case.

Layout Optimization: Since thermal stress is mostly dependent on the temperature fluctuations from the thermal cycling, in this step, only peak-to-peak temperature metric has been used for comparison, and the target maximum threshold temperature is set to 65°C. Two layer stacks are considered: 3 mm copper baseplate with (a) no PCM, (b) 15 mm metallic PCM. In this phase, two iterations of optimization are performed. In the first iteration, a set of fixed floorplan size layout solutions is generated for both cases to find the best case. Then, based on the best case, another iteration is performed, where the floorplan size is varied to further optimize the electro-thermal reliability performance.

For the layout shown in Figure 42(a)), in the first iteration, an electro-thermal optimization is performed by evaluating 200 solutions for both non-PCM and metallic PCM cases with a floorplan size of 46 $mm \times 36$ mm. In this case, the waveform has a duty cycle of 15%, and the power for each die is varied from 0 W to 40 W. For the PCM case in Figure 42(c), the runtime for generating the solution space is approximately 814.64 s, and for the non-PCM case in Figure 42(b), that value is 147.11 s. From Figure 42, it is evident that for the same inductance range (12 nH to 36 nH), the metallic PCM case provides better temperature control compared to

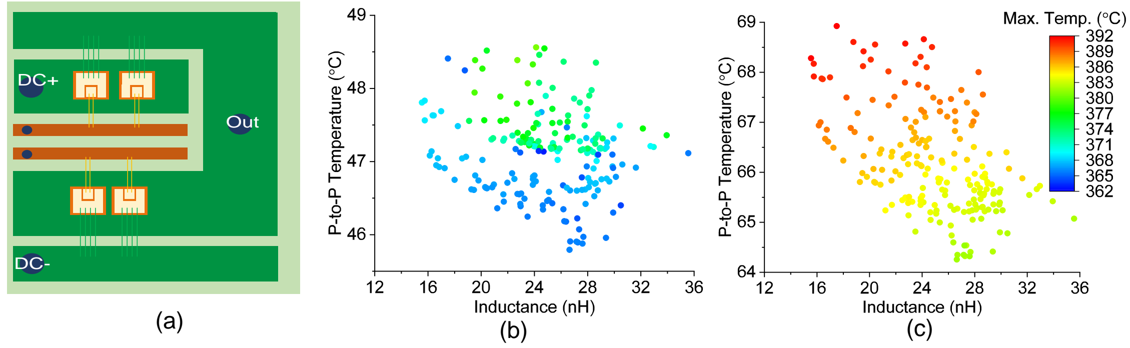


Figure 42: (a) Layout of a half-bridge power module and fixed-floorplan size ($46mm \times 36mm$) solution space. (b) metallic PCM, and (c) Non-PCM case.

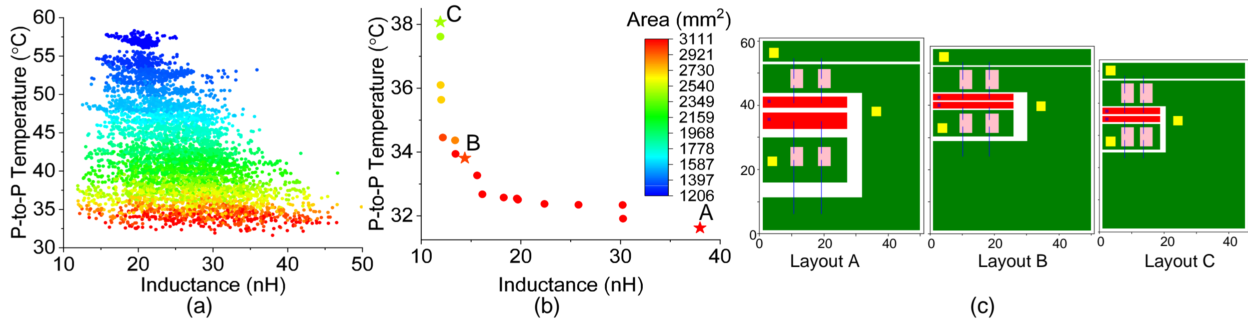


Figure 43: (a) Complete solution space with variable floorplan sizes and (b) the Pareto-front with (c) three selected solutions: Layout A (51 $mm \times$ 61 mm), Layout B (51 $mm \times$ 58.5 mm), Layout C (46 $mm \times$ 53.5 mm)

the non-PCM case. From the color mapped data in Figure 42 (b) and (c), the maximum temperature range for non-PCM case and PCM is 381.47 °C to 391.91 °C and 363.08 °C to 380.55 °C, respectively. So, for the same floorplan size, in both maximum temperature and peak-to-peak temperature metrics, the metallic PCM case has outperformed the non-PCM case and metallic PCM has been able to limit the peak-to-peak temperature within the maximum target threshold (65 °C). Therefore, the metallic PCM case is passed through the second iteration. In this iteration, the input power waveform is kept the same as the fixed floorplan size case. However, the floorplan size is varied from 1206 mm^2 to 3111 mm^2, and 32 different floorplan sizes are considered in this range. A total of 6400 solutions (200 solutions for each case) are generated to find a good tradeoff between power loop inductance and peak-to-peak temperature. The complete solution space is shown in Figure 43(a). The total runtime for the complete solution space (6400

solutions) generation is about 6.5 hours. A non-dominated sorting is applied to the solution space to get the Pareto-front shown in Figure 43(b). From the thermal results, it is evident that changing the floorplan area can further optimize the layouts. To demonstrate the impact of placement and routing of the components on the objectives, three solutions are chosen and shown in Figure 43(c). The figure shows that layout A has the highest footprint with the lowest peak-to-peak temperature (31.62 °C) but a much higher power loop inductance (37.98 nH). On the other hand, layout C has a smaller footprint with lower inductance (11.91 nH) value and higher temperature (38.07 °C). Between these two, layout B shows a balanced performance (14.38 nH and 33.81 °C) for both of the objectives. The balanced layout can be exported to 3D CAD tools, and detailed analysis can be performed before fabrication.

So, combining both layer stack and layout optimizations provide the best combination to reduce max temperature and stress from thermal cycling.

6.2 Optimization for Reducing Electromigration (EM) Impact

Existing efforts stated in the literature review (Section 2.2.2) are manual and case-specific studies. The commercial CAD tools can be used for EM modeling without any intellectual optimization capability. Besides, the runtime overhead is too much to be used in an optimization loop. EM is a well-known issue in industries like high-frequency integrated circuits (HFIC), ultra/very-large-scale ICs (U/VLSI), communication appliances, etc [62]. Since these applications include very high-frequency operations, the EM-model should be capable of capturing both DC and high-frequency AC current density impacts properly. Though flip-chip modules [99, 100] with SiC and GaN devices are very recent attractions to the power electronics due to their low parasitics, this technology has been widely used in U/VLSI for a while. Therefore, EM modeling and mitigating efforts are quite common in those fields. To assess the risk associated with EM for MCPM layouts, PowerSynth 2 has been used. The EM-aware optimization methodology along with key are described below.

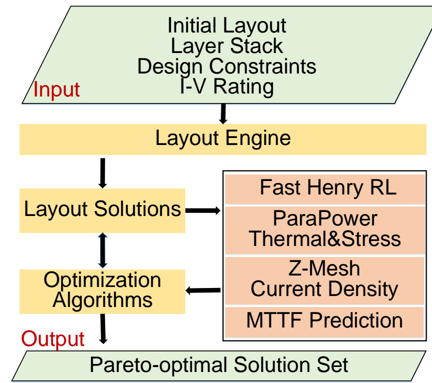


Figure 44: EM-aware optimization flow

6.2.1 Methodology and Design Tools

EM-aware electro-thermal and reliability optimization workflow is shown in Figure 44. The flow involves PowerSynth, Z-Mesh tool, HSPICE, FastHenry, and ParaPower to perform different steps. PowerSynth takes the input information from the user, and the layout engine generates layout solutions. Each solution is evaluated for each performance metric by the corresponding model or tool.

Z-Mesh Tool: Since parasitic inductance has a significant impact at higher switching frequencies of the WBG devices, the impedance distribution of the power loop of a module needs to be considered for current density distribution evaluation. A quick and accurate resistive mesh modeling (R-Mesh) tool is reported in [101], which has shown a 517× speed up against Cadence Encounter Power System (a commercial power integrity analysis and optimization tool for VLSI) with only 1.3% error for a 2D memory die design. This tool has been modified to consider the inductance impact for each mesh element and is named as the Z-Mesh tool. Z-mesh tool takes the layer stack, layout geometry, material, supply voltage, current, and mesh size information from the user through PowerSynth API. Each layer material's resistivity is updated to reflect the equivalent inductive impedance of the material. FastHenry evaluated loop inductance is used to calibrate the modeling of resistivity to capture the inductance impact properly. This calibration needs to be performed at each frequency case, thanks to the PowerSynth API that makes the evaluation very fast. Then, it creates a Z-mesh network modeling the impedance distribution of

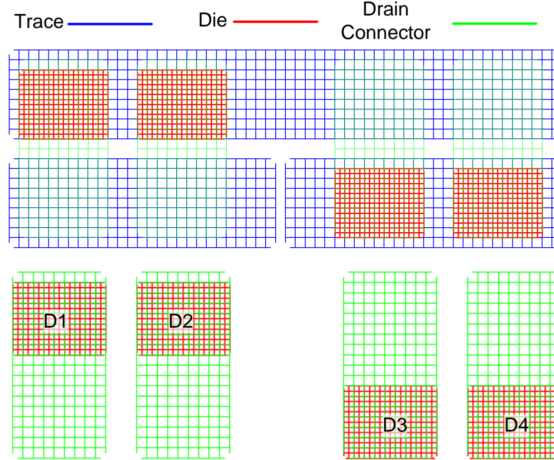


Figure 45: Sample mesh from our Z-Mesh tool

each layer for a given mesh size. The resultant impedance network is stored as a SPICE netlist, where DC+ and DC- terminals are mapped as current sources, and sink, respectively. The rated current provided by the user is considered during HSPICE simulation, and current through each element is extracted. Since this tool uses an impedance circuit model, and SPICE engine for solving the circuit, it is much faster than the FEA simulation. A flip-chip half-bridge module is considered for the demonstration of the Z-Mesh tool meshing results. The module structure is shown in Figure 46. This half-bridge module has two SiC MOSFETs per switching position on a direct-bonded copper (DBC) substrate. Both source and drain sides have a 4×3 array of solder bumps. For this case, the Z-Mesh tool creates three layers of meshes, where the bottom layer contains all traces, the middle layer has the SiC die, and the top layer has the drain connectors. To improve the impedance model accuracy, a finer mesh is used on device layers compared to trace and connector layers. The solder bumps are modeled as copper vias to complete the loop. The corresponding meshing is shown in Figure 45, where the top one shows the combined meshing for all three layers, and the bottom one shows the die and connector layer's combined meshing. To calculate the current density for each solder bump, the current through each via is obtained from SPICE simulation results. This current value is divided by the cross-sectional area (1 mm^2 for this example), to achieve the current density distribution. The extraction efficiency comparison between our Z-Mesh tool and ANSYS Workbench is shown in Table 12. From the table, it is clear

Table 12: Efficiency comparison of current density extraction

Model	Runtime (s)	Speedup	Memory (MB)	Memory Reduction
ANSYS	310	$\times 1$	10329	$\times 1$
Z-Mesh	0.28	$\times 1107$	513	$\times 20$

that the Z-Mesh tool has orders of magnitude speedup and 20 times memory reduction compared to the FEA tool and hence make this tool suitable to be used in the optimization loop.

EM Modeling: EM-associated reliability metrics include MTTF for the solder bumps and resistance increment for the wire bonds. These metric values can be calculated based on a closed-form model, which can be used for relative performance measurement by excluding the experimental result-dependent parameters. Also, the lifetime can be estimated based on a data-driven model developed by purely experimental results. EM-associated risk assessment for both wire-bonded and flip-chip module can be performed by both of these models. Both of the modeling techniques are described below.

- **Closed Formula Model:** In this model, the well-known Black's equation is used for the lifetime estimation of each interconnect. The equation is as follows.

$$MTTF = \frac{A}{J^n} e^{(E_a/kT)}$$

  Here, A is a constant based on the cross-sectional area of the interconnect, J is the current density, E_a is the activation energy (0.9 eV), T is the temperature of the interconnect, n is a scaling factor (set to 2), and k is the Boltzmann's constant [102]. The current density and the maximum temperature are extracted for each interconnect. Then, Black's equation is used to measure the relative value of MTTF for each interconnect, considering the A as the same constant for all the bumps. Thus, a relative number can be used for comparing the interconnects' reliability in the same layout.

- **Data-Driven Model:** To develop a data-driven model, experiments need to be designed very carefully to capture the parameters that initiate EM-associated failure. The

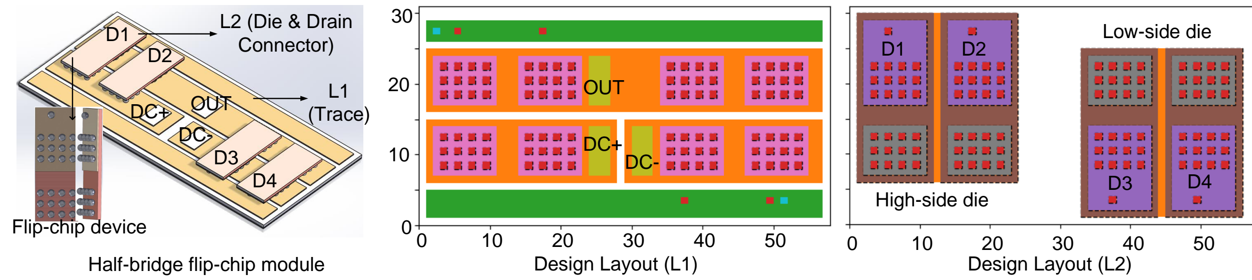


Figure 46: Minimum-sized solution from PowerSynth

experiments need to be customized based on the interconnect type. A parameter sweep is required to collect data at different current and temperature ranges. The temperature range needs to be planned carefully based on the solder materials used in the module. Once the data are collected, a look-up table can be generated to develop the model. Also, the data can be used to tune the constant parameters of the closed formula model to predict the absolute lifetime rather than the relative one.

Implementation Methodology: In this work, a Black's-law-based model has been used for the flip-chip module with solder bump interconnects, and a data-driven model has been used for the wire-bonded module.

Solder Bump: Since solder bumps are emerging interconnects with low electrical parasitics [99, 72] and the PowerSynth 2 layout engine can optimize flip-chip designs with solder bump arrays, current density and temperature distribution across those arrays are extracted for MTTF evaluation using the closed formula model. The module structure is ported to Z-Mesh tool to get the current density for each solder bump. The maximum temperature distribution across the solder bumps is read from the ParaPower interface under the given boundary conditions. Using the closed formula model, the relative MTTF value is determined for each bump.

Wire Bond: A look-up table from the data-driven model is used for the lifetime estimation of wire bonds in a power module. Data can be collected from FEA results, which is time consuming and requires experimental validation as well. Also, it is hard to get data from power module industries due to proprietary issue. Therefore, an accelerated test is performed in-house on 5-mil aluminum wire bonds under different current and temperature conditions using a custom fixture

assembly (shown in Figure 51(a)). Details on the experimental setup and data collection are described in Section IV. PowerSynth 2 parasitic netlist extraction feature is used to set up the circuit simulation under given operating conditions. SPICE simulation is performed to get the current through each device. It is assumed that each device has an equal current distribution through the source-side wire bonds. Therefore, the current through each wire bond is calculated from the resultant device current. The current density of the wire bonds is found from the result of dividing the current through the wire by the cross-sectional area of each wire. ParaPower has been used to find the temperature distribution of the die and wire bond interfacing area. Then, these current density and temperature values are mapped in the experimental results to estimate the failure time.

Reliability Optimization: In this work, three objectives are considered: electrical parasitics (loop inductance), the static maximum junction temperature of the module, and MTTF for interconnects. The solution space is generated based on the first two objectives. The API between PowerSynth and FastHenry is leveraged for electrical loop inductance evaluation, and the ParaPower API is used for the static maximum junction temperature. Then, the MTTF value for each interconnect of the solutions is evaluated. Since each solution has multiple interconnects, the minimum value of MTTF is considered for comparison among different solutions. The built-in randomization algorithm is used to optimize the power loop inductance and maximum junction temperature. Both flip-chip and wire-bonded modules are considered for electro-thermal optimization. Before optimization, a minimum-sized solution layout is generated and evaluated to capture the maximum possible power density. To further optimize, a set of fixed floorplan-sized solutions with different floorplan sizes are generated and evaluated. For each fixed-sized solution set, the extra room is calculated from the difference between the minimum size and the given floorplan size. In randomization, the extra space is distributed by following either a uniform or multinomial distribution. However, a genetic algorithm uses mutation and crossover to generate a new set of design variables in each generation and distributes the extra room among the constraint graph edges by using those design variables as weighting factors. Finally, a Pareto-optimal

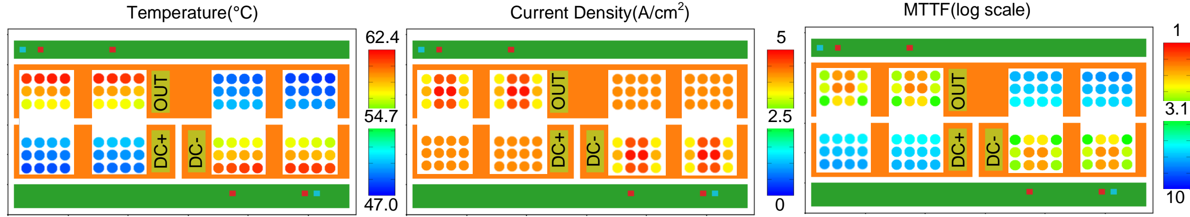


Figure 47: Temperature, current density, and MTTF results at DC

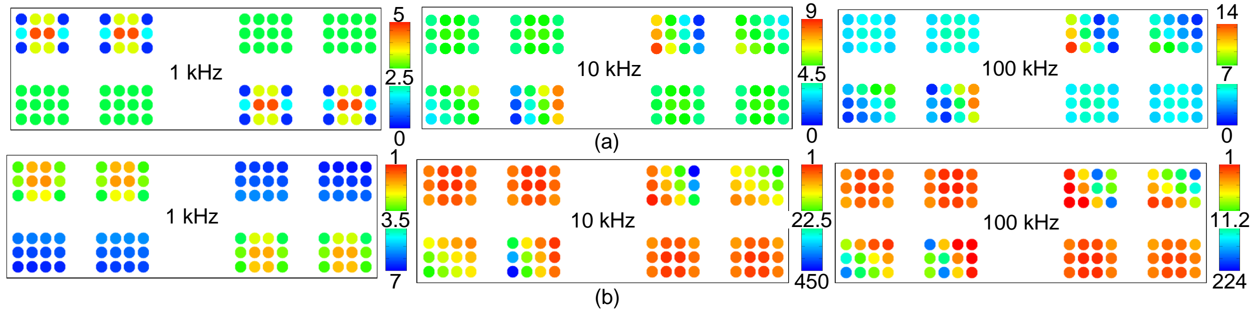


Figure 48: AC results: (a) current density distribution (linear scale), (b) relative MTTF values (log scale)

solution set is reported from both algorithms by applying non-dominated sorting on the solution space.

Though static maximum temperature has been used in this flow to estimate the interconnection lifetime, the PowerSynth transient thermal model [103] can provide maximum, average, and peak-to-peak temperature under a certain thermal cycling condition. Our fast and accurate transient thermal model has been proven to be about 3,489 times faster with less than 10% error compared to ANSYS simulation for 2D cases. PowerSynth-guided reliability optimization flow can reduce the induced stress on the interconnect due to thermal cycling by optimizing the layer stack material, thickness, placement, and routing of the components. PowerSynth 2 already handles custom reliability constraints to ensure safe high power operations. Therefore, PowerSynth 2 can produce more reliable layouts upon integrating the EM-aware reliability optimization flow.

6.2.2 Experimental Results

A flip-chip module and a wire-bonded module are considered for optimization. Results for each case are described below.

Flip-Chip Module Design: As a case study, the flip-chip half-bridge module shown in Figure 46 has been considered for optimization. In the planar view of the solution layout, L1 contains the traces, power, and gate terminal footprints. On the L2 layer, the SiC MOSFETs with drain connector footprints are available. Both layers have the solder bumps footprints, which make the inter-layer connection and complete the loop.

To demonstrate both DC and AC modeling capabilities in the Z-Mesh tool, the minimum-sized solution layout case is chosen. The temperature distribution and current density distribution at DC (100 V, 1 A) are shown in Figure 47. For the temperature distribution, a 1000 W/m^2K heat transfer coefficient is applied on both sides of the module, and 25 W heat dissipation is applied to each device. At DC, the current density results show a uniform distribution for the drain side connector bumps, whereas the SiC source side bumps have a symmetric distribution from the center towards the edges as the device has the gate region in the center. Since the resistance is dominated at DC, and trace resistance is neglected compared to the SiC and solder joint resistances, there is almost no variation in inter-die distribution. The current density is pretty small as the total current is considered only 1 A, thus each device is getting approximately 0.5 A and distributed among 12 solder bumps. For the temperature distribution, since source side solder bumps are closer to the device compared to the drain connector bumps, they have a higher temperature. Using Black's law, MTTF is evaluated for each solder bump. From the MTTF results in Figure 47, it is evident that the MTTF is very much dependent on the temperature distribution. The source-side solder bumps are hot spots, thus they have a lower MTTF compared to the drain-side solder bumps.

Figure 48(a) shows the current density variation at different frequencies. At low frequency, the resistance and inductance are comparable, and the variation in current density distribution is still similar to the DC case. However, with the increasing frequency, the trace inductance is

dominating compared to the resistance. Therefore, variation in current density distribution depends on the distance of the device from the source or sink. The inter-die current density distribution variation is captured at AC, whereas the intra-die variation at DC. The MTTF results (shown in Figure 48(b)) show the current density dependency of the MTTF values with the increasing frequency. At low frequency, the distribution is more temperature-dependent. Since the temperature distribution does not change with frequency, the current density distribution impact dominates. For example, 10 kHz MTTF distribution shows that the drain side solder bumps have a lower MTTF compared to many source side solder bumps due to higher current density. Therefore, both temperature and current density variations must be properly captured for reliability analyses.

To optimize the sample flip-chip half-bridge module, ten different floorplan sizes varying from 2100 mm^2 to 2992 mm^2 are considered with 15 solutions for each floorplan size at DC operating conditions. The runtime is only 135 s per layout with electrical, thermal, and reliability evaluations. The solution space is shown in Figure 49(a). For each solution, the area is color mapped. Three layout solutions are chosen from the Pareto-front to demonstrate the layout impact on the optimization and are shown in Figure 49(b). Figure 49(c) shows the distribution of MTTF for each selected layout. From the layouts, it is clear that Layout A has the lowest footprint area (60 mm $\times$ 35 mm) and has the highest temperature rise, which results in a lower MTTF value (1.26). On the other hand, layout C has the largest footprint area (68 mm $\times$ 44 mm), which helps reduce temperature. This layout has achieved the highest minimum MTTF (1.92). Between two extreme solutions, layout B (66 mm $\times$ 44 mm) shows a balanced performance in all objectives with a minimum MTTF value of 1.65. Since this is the DC current distribution case, the MTTF is temperature-dominated. From the MTTF distribution, it is clear that no solder bumps from layout A have achieved an MTTF value greater than 9, whereas both B and C have a good number of solder bumps with higher MTTF values. These results can be used to filter out reliable solutions by setting up a threshold value for MTTF.

Apart from varying floorplan sizes, the solder bump array size can vary within the same

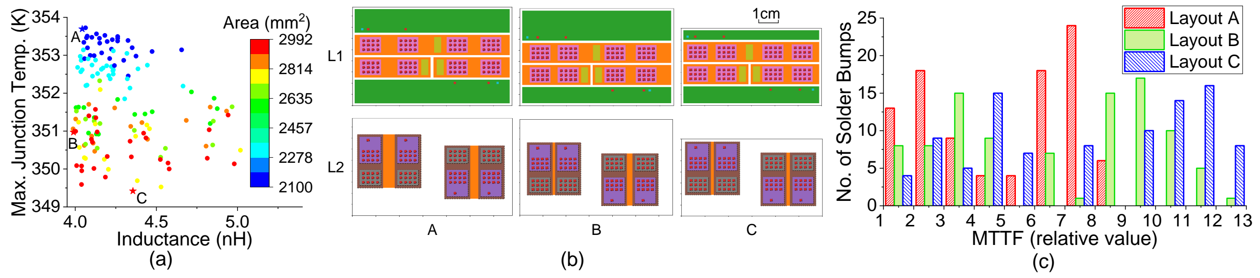


Figure 49: (a) Optimization solution space, (b) three selected layouts, (c) MTTF distribution of three layouts.

Table 13: MTTF optimization with various solder bump array sizes

Array Size	Max. Current Density (A/cm^2)	Max. Temperature (°C)	Min. MTTF	MTTF Increment
4×3	4.86	62.43	1.19	$\times 1$
5×4	3.13	62.34	2.89	$\times 2.4$

floorplan size. This variation can help optimize the MTTF with more even current distribution. For example, for the same minimum-sized solution case (shown in Figure 46), if the solder bump array is changed from 3×4 to 5×4, the minimum MTTF can be improved by 2.4 times as shown in Table 13, where MTTF values are relative numbers.

Wire-Bonded Module Design: To demonstrate the EM assessment capability, a sample 2D wire-bonded module design is chosen and shown in Figure 50(a). The module has two SiC devices per switching position and an on-module decoupling capacitor (C1). Here, KL, GL, KH, and GH represent low-side kelvin source, low-side gate, high-side kelvin source, and high-side gate pins, respectively. This initial module has been optimized for electro-thermal performances, and the solution space is reported in [74], where a balanced solution (shown in Figure 50(b)) has been validated through manufacturing. Since this design has already been hardware-validated, we have chosen this optimized design case for EM-associated risk assessment. Failure of a wire bond in this study is a 10% increase in electrical resistance of the wire [104]. PowerSynth extracted parasitic netlist has been used for circuit simulation with 23 A current source and 131 μ H load inductor between DC+ and OUT terminals. From simulation results, the current through D1, D2, D3, and D4 is found at 11.53 A, 11.26 A, 11.55 A, and 11.24 A, respectively. There are three

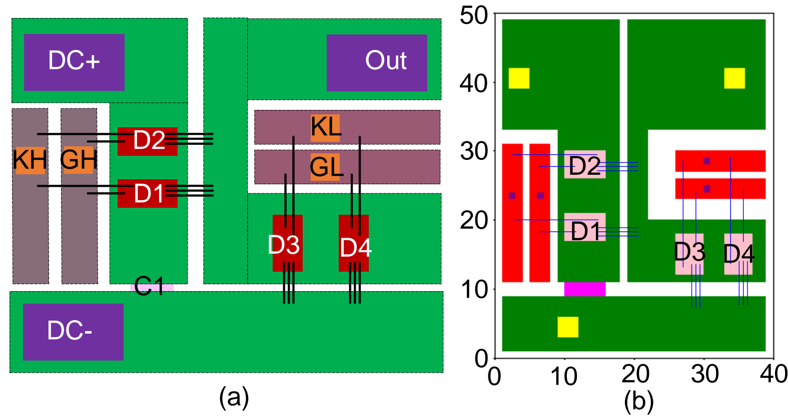


Figure 50: Wire-bonded case: (a) initial layout, (b) balanced solution

parallel wire bonds in each device. Therefore, the current through each wire bond is calculated by dividing the corresponding device current by the number of wire bonds. Since 5-mil wire bonds are considered, the current density is extracted by dividing the current by the cross-sectional area. The current density and the temperature distribution results are mapped from the experimental results described in the following section to get the failure metric. The results are summarized in Table 14.

Wire Bonds EM Test: The test setup is shown in Figure 51(a). The wire-bonded samples consist of two independent DBC cards, outfitted with SAC305 soldered hex standoffs for power and voltage monitoring connection to the DBC card pads. The two cards are connected using four aluminum wire bonds, creating a series of four independently measurable bonds for each experimental run. DC power connection is supplied to the bonded samples within an oven using a low-noise power supply. This setup is used to apply ambient temperatures of 295 °C, and currents of up to 15 A to each set of wire bonds. The failure criteria for experiments is a 10% increase in electrical resistance. This change in resistance is monitored over time using a high-fidelity DATAQ voltage module. It is connected to the wire bonds with a 4-wire voltage measurement configuration. By monitoring the change in voltage over time and dividing by the constant electrical current imposed on the wire bonds during testing, the change in electrical resistance is obtained.

Table 14: Reliability Evaluation of Wire-Bonded 2D Module

Device	Current (A)	Temperature (K)	Wire Bond Current Density (A/cm2)	10% R Increment Time (Hrs)
D1	11.53	416.8	3.03×10^4	217.4
D2	11.26	416.5	2.95×10^4	229.6
D3	11.55	427.0	3.03×10^4	210.8
D4	11.24	427.7	2.95×10^4	221.9

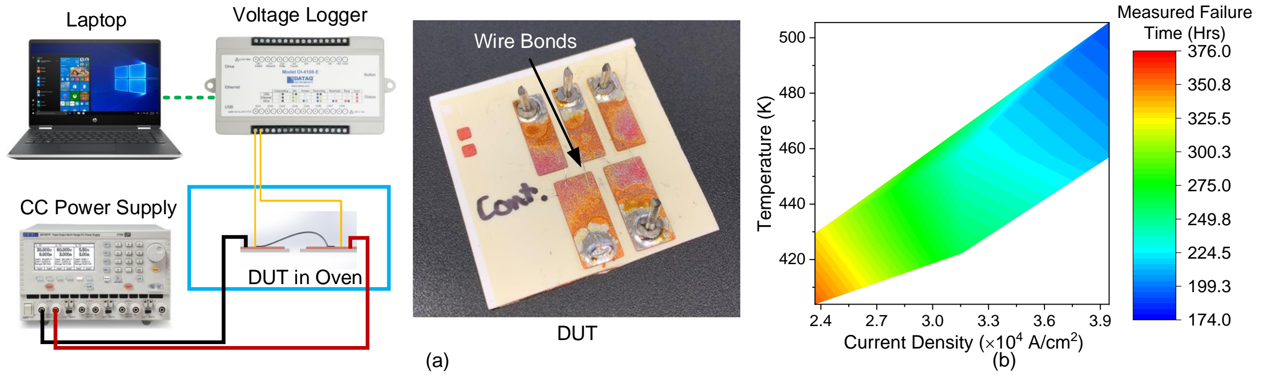


Figure 51: (a) Test Vehicle for Establishing EM experimental failure risk in Al wire bonds, (b) Reliability data library based on the experimental results

24 wire bonds are tested under EM conditions (elevated ambient temperatures and current densities) using the accelerated testing setup to gather failure time data. In addition to these experiments, the temperature coefficient of resistance is measured to account for wire bond joule heating. By combining the EM results with the temperature coefficient of resistance measurements, a contour plot of the results is shown in Figure 51(b). It aggregates the current density through the wire bonds, the temperature of the wire bonds at that current density, and the corresponding failure time.

From the experimental results, it is clear that as current density and ambient temperatures are elevated, the lifetime of the wire bonds is reduced. These results are used in the data-driven model to evaluate the failure time of the 2D wire-bonded module case. As power density increases, current density and temperature impacts may be amplified on power module interconnection, emphasizing the need for a tool to optimize a module layout for a longer lifetime.

Chapter 7

Conclusion and Future Work

7.1 Conclusion

PowerSynth is the first tool that can perform physical design optimization of MCPMs using a multi-objective optimization framework. This dissertation is based on the research and development of more generic, scalable, and efficient algorithms to extend PowerSynth's capability and make it as a state-of-the-art (SOTA) tool.

PowerSynth core architecture has been updated from the planar approach to a modular, and hierarchical one to optimize more complex, and high-power density power modules. The hierarchical corner stitch with constraint propagation has outperformed the traditional matrix-based layout generation methodology in efficiency and success rate. The updated constraint-aware layout engine is more efficient, scalable, and generic compared with the previous approach. This layout engine is demonstrated with the capability of processing complex geometry with heterogeneous components, exploring a broader solution space, and adapting to different optimization algorithms. Updated electrical and thermal models with hierarchical layout description script enable PowerSynth to optimize not only 2D but also 2.5D power module layouts efficiently in v1.9. A full-bridge 2.5D power module layout is optimized using v1.9, and a well-balanced solution is fabricated and tested. The measurement and FEM simulation show a close agreement (within 10% error) with PowerSynth-predicted electrical and thermal results. Thanks to my colleagues for coming up with such an efficient, and accurate electrical and thermal models.

To extend the capability by handling 3D high-density layouts, the methodology has been updated in v2.0 by supporting inter-layer via connections. A new code base with updated architecture has been developed for PowerSynth 2. PowerSynth 2 is suitable for performing electro-thermo-mechanical and reliability optimization of SOTA high-density and heterogeneous power modules. The underlying methodology is scalable, which is the key feature that

distinguishes this tool from other concurrent efforts. There is no CAD tool available that can perform 2D/2.5D/3D layout generation intelligently. This methodology has been helpful for other researchers as well to explore in this field. PowerSynth 2 can simulate and optimize high-density layout solutions beyond the current manufacturing capability, which provides an early testing platform for future packaging and thermal solutions. This module-level design framework can also be extended toward system-level optimization. A completed round-trip PowerSynth-assisted design flow is demonstrated to achieve better productivity over the traditional manual design approach. A high-density 3D MCPM layout is optimized and validated through a fabricated 3D SiC power module. The measurement and FEM simulation show a close agreement with PowerSynth 2 predicted electrical (within 13%) and thermal (within 10%) results for the 3D layout with minimum parasitics.

7.2 Future Work

To make PowerSynth more useful, continuous research and development are ongoing. The limitations addressed in Chapter 5 need to be addressed for better performance.

In the future, the following steps/features would be required to unleash its full potential and extend the capability toward system-level optimization:

- A layout description language is necessary for a structured and generalized description of power electronic designs. This language should have some keywords and methods that can be useful for both layout description and layout manipulation.
- A layout synthesis engine that can generate initial layout templates from the circuit netlist. Currently, the PowerSynth layout engine is heavily dependent on the user-provided initial layout, which might not be a good starting point for optimization. A carefully designed initial input layout would result in a good solution space, which would be possible with some template generation method implemented in the synthesis part from where the best template can be used for further placement and routing optimization.

- Current version has considered wire bonds as point connection. For more flexibility with the connections, wire bond pads with 2D rectangular geometry can be considered.
- Proper tuning can be useful for randomization algorithm to generate the Pareto-front faster and even better quality. The built-in randomization algorithm has no guidance toward optimization, hence it performs an exhaustive search to generate the solution space.
- Careful identification of the design variables for optimization would help in faster convergence for the genetic algorithm.
- PowerSynth 2 can be used for gathering the data for a machine-learning (ML) model calibration. The correlation between the performances and different layout parameters can be studied based on the data set. Finally, ML/deep neural network-based models can be developed to predict the performance metrics of MCPM layouts.
- Besides randomization and genetic algorithm, simulated annealing can be studied to find a better global optimum solution. As simulated annealing has a hill-climbing nature, it can avoid some local minima at a high furnace temperature.
- The performance models need to be updated for 3D/system-level designs. Though the ParaPower thermal and stress model is widely used in PowerSynth 2, a built-in model could save runtime and improve efficiency significantly.
- The reliability optimization methodology needs more research and development efforts for being matured and integrated with the release packages. The initial electromigration model has not considered the stress impact. Adding a stress model and distribution would provide a more reliable mean time to failure assessment.
- Partial discharge modeling efforts can be integrated for custom module optimization at a high power rating.

- More 3D designs can be optimized, fabricated, and tested for improving the confidence of PowerSynth 2 CAD flow. The hybrid and flip-chip designs would show better optimization results compared to the wire-bonded design case.
- PowerSynth 2 architecture's modularity can be leveraged to interface other modeling/optimization efforts from different groups/tools for system-level optimization.

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Appendix

List of Publications

Chapter 4 through Chapter 6 are partial reproductions of papers that have been published or considered for publication at the following outlets:

Chapter 4:

Imam Al Razi, Quang Le, Tristan Evans, Shilpi Mukherjee, H. Alan Mantooth, and Yarui Peng, "PowerSynth Design Automation Flow for Hierarchical and Heterogeneous 2.5D Multi-Chip Power Modules," in IEEE Transactions of Power Electronics, vol. 36, no. 8, pp. 8919–8933, 2021.

Chapter 5:

Imam Al Razi, Quang Le, Tristan Evans, H. Alan Mantooth, and Yarui Peng, "PowerSynth 2: Physical Design Automation for High-Density 3D Multi-Chip Power Modules," (under review) in in IEEE Transactions of Power Electronics.

Chapter 6:

Imam Al Razi, David Huitink, and Yarui Peng, "PowerSynth-Guided Reliability Optimization of Multi-Chip Power Module," in IEEE Applied Power Electronics Conference and Exposition, Jun. 2021, pp. 1516–1523.

Imam Al Razi, Whit Vinson, David Huitink, and Yarui Peng, "Electromigration-Aware Reliability Optimization of MCPM Layouts Using PowerSynth," (accepted) in IEEE Energy Conversion Congress and Expo.

Other Publications:

Journals:

Quang Le, Imam Al Razi, Tristan Evans, Shilpi Mukherjee, Yarui Peng, and H. Alan Mantooth, "Fast and Accurate Parasitic Extraction in Multichip Power Module Design Automation Considering Eddy-Current Losses", (accepted) in IEEE Journal of Emerging and Selected Topics in Power Electronics, 2022.

Yarui Peng, Quang Le, Imam Al Razi, Shilpi Mukherjee, Tristan Evans, and H. Alan Mantooth, "PowerSynth Progression on Layout Optimization for Reliability and Signal Integrity", IEICE Nonlinear Theory and Its Applications, vol. 11, no. 2, pp. 124–144, Apr 2020

Tristan Evans, Quang Le, Shilpi Mukherjee, Imam Al Razi, Tom Vrotsos, Yarui Peng, and H. Alan Mantooth, “Powersynth: A Power Module Layout Generation Tool”, IEEE Transactions on Power Electronics, vol. 34, no. 6, pp. 5063–5078, Jun 2019

Conferences:

David Huitink, Whit Vinson, Collin Ruby, Imam Al Razi, and Yarui Peng, “Factoring Interacting Stress Mechanisms in Design for Reliability of Extreme Environment Power Modules”, (under review) in Proc. IEEE Workshop on Wide Bandgap Power Devices and Applications, 2022.

Imam Al Razi, Quang Le, H. Alan Mantooth, and Yarui Peng, “Hierarchical Layout Synthesis and Optimization Framework for High-Density Power Module Design Automation”, in Proc. International Conference on Computer-Aided Design, pp. 1-8, Nov 2021.

Quang Le, Imam Al Razi, Yarui Peng, and H. Alan Mantooth, “Fast and Accurate Inductance Extraction For Power Module Layout Optimization Using Loop-Based Method”, in Proc. IEEE Energy Conversion Congress and Exposition, pp. 1358-1365, Oct 2021.

Joshua Mitchener, Imam Al Razi, and Yarui Peng, “Designing a Graphical User Interface for the Power Module Optimization Tool PowerSynth”, in Proc. ASEE Midwest Section Conference, pp. 1-12, Sep 2021.

Quang Le, Imam Al Razi, Yarui Peng, and H. Alan Mantooth, “PowerSynth Integrated CAD Flow for High Density Power Modules”, in Proc. IEEE Design Methodologies Conference, pp. 1-6, Jul 2021.

Imam Al Razi, Quang Le, H. Alan Mantooth, and Yarui Peng, “Physical Design Automation for High-Density 3D Power Module Layout Synthesis and Optimization”, in Proc. IEEE Energy Conversion Congress and Exposition, pp. 1984–1991, Oct 2020.

Bakhtiyar Md Nafis, Ange Iradukunda, Imam Al Razi, David Huitink, and Yarui Peng, “System-level Thermal Management and Reliability of Automotive Electronics: Goals and Opportunities in the Next Generation of Electric and Hybrid Electric Vehicles”, in Proc. ASME International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems, pp. 1–8, Oct 2019.

Imam Al Razi, Quang Le, H. Alan Mantooth, and Yarui Peng, “Hierarchical Layout Synthesis and Design Automation for 2.5D Heterogeneous Multi-Chip Power Modules”, in Proc. IEEE Energy Conversion Congress and Exposition, pp. 2257–2263, Sep 2019.

Imam Al Razi, Quang Le, H. Alan Mantooth, and Yarui Peng, “Constraint-Aware Algorithms for Heterogeneous Power Module Layout Synthesis and Optimization in PowerSynth”, in Proc. IEEE Workshop on Wide Bandgap Power Devices and Applications, pp. 323–330, Oct 2018