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Design and Optimization of a High Power Density Silicon Carbide Traction Inverter

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Design and Optimization of a High Power Density Silicon Carbide Traction Inverter

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by

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This thesis is approved for recommendation to the Graduate Council

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ABSTRACT

This project was initiated with the goal of demonstrating a 3-phase silicon carbide based 150-kW 25 kW/L DC-AC power conversion unit capable of operation with coolant temperatures up to 90°C. The project goals were met and exceeded by first analyzing the established inverter topologies to find which one would yield the highest power density while still meeting electrical performance needs in the 150-kW range. Following topology selection, the smallest silicon carbide power module that met the electrical requirements of the system was found through experimental testing and simulation. After a power module selection was finalized, a DC link capacitor bank was designed by calculating the electrical requirements of the system and choosing the capacitor available that added the least volume to the overall system while still meeting the system's electrical requirements. PCB-based bussing was designed around the power modules and capacitors in SolidWorks and then electrically optimized through simulations in Ansys. A custom DSP-based controller built around the Texas Instruments 28379D control card was designed and created for the control basis of the power converter. The complete system was constructed and tested at low power with great success, demonstrating the ability to operate at the desired full power of 150 kW, while achieving an overall volume of 1.35 L.

ACKNOWLEDGEMENTS

I would like to give great thanks to my advisor Dr. Yue Zhao for his invaluable knowledge and guidance during my time as his student. I would also like to give special thanks to my advisory board members Dr. Juan Balda and Mr. Robert Saunders for their knowledge and support throughout my academic career.

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DEDICATION

I dedicate this thesis to my parents whose love, guidance, and support made this possible.

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CHAPTER 1
INTRODUCTION

1.1 Motivations for Research

The use of electric vehicles in the United States can be traced back to the 19th century, when William Morrison built the first functional electric powered "vehicle". Although it was essentially an electric powered wagon with a top speed of 14 miles per hour, the next best method of personal transport was by horseback. Not surprisingly, Morrison created an interest that would last well into the 21st century.

Around 1890, when Morrison first introduced his electrified wagon, other modes of powered personal transport had already been demonstrated, namely steam engine-based vehicles and combustion engine-based vehicles. Initially, electric vehicles addressed the shortcomings of both other types transport. Electric vehicles of the time were not held back by the excessive time required to start a steam engine, which could be up to 45 minutes. More than that, electric vehicles did not require the user to carry a supply of water. In comparison to combustion engine-based vehicles of the time, the electric vehicle was much more user friendly because gasoline engine cars required manual cranking at startup and changing gears required so much physical strength that some users were unable to operate them at all. Gasoline engines were also known for being extremely noisy.

Because of these factors, electric vehicles were considered by many people—including Thomas Edison—to be the superior mode of transport. Although electric vehicles made up about a third of the vehicles on the road in 1900, the introduction of Henry Ford's Model T in 1908 cut the electric vehicle's success story short. Not long after the Model T was introduced, Ford began

selling the vehicle with an electric starter and to add insult to injury, the cost of an electric vehicle was almost three times what a Model T could be obtained for.

By 1935, electric vehicles had virtually disappeared. This can partly be attributed to the lack of electric power delivery to anyone who didn't live in a city. Couple that with the fact that gasoline had become inexpensive to produce and could be easily delivered to almost any anyone and one can clearly understand the reason behind electric vehicles' sharp decline. As combustion engine technology continued to improve, electric vehicles didn't gather much attention again, that is until oil prices began to rise and the United States dependence on foreign oil was brought to showcase. In 1973, the Arab members of the Organization of Petroleum Exporting Countries placed an embargo on the United States, which resulted in enormous waiting times at the fuel pump, and a near 400% increase in the price of oil compared to the previous year.

This prompted Congress to pass the Electric and Hybrid Vehicle Research, Development, and Demonstration Act of 1976. At the same time, companies such as General Motors, American Motor Corporation (later acquired by Chrysler), and NASA began building prototype electric cars as alternative fuel vehicles. Although these vehicles were operational and did see some use—even by the United States Postal Service—they failed to gain market traction. This failure can largely be attributed to their performance issues, which included top speeds under 50 mph and a maximum range of around 40 miles. Again, interest in electric vehicles died down for a while.

As a result of a great economy and low fuel prices during the 1990s, people in general were not concerned with fuel efficient vehicles. Congress, however, passed the Clean Air Amendment and the Energy Policy Act and continued to sponsor research in electric vehicle technology. At the same time, several states developed incentives to lower emissions.

In the early 2000s, the Toyota Prius gained huge success by becoming the very first mass produced hybrid electric vehicle. It was made possible by research supported by the Department of Energy. In 2006, just three years after it was founded, Tesla Motors announced that it would be releasing to the public an all-electric vehicle capable of 200 miles per charge. Because of its success, Tesla was awarded a $465 million loan from the Department of Energy. Naturally, other automakers became interested in the electric vehicle market and by the end of 2010, both Chevy and Nissan had brought their own electric vehicles to market. As more companies began bringing electric vehicles to market, it quickly became apparent that there were not enough places on the go to charge these vehicles. As a response to the shortage, in 2009 The Department of Energy invested $115 million to add to the nation-wide charging infrastructure that auto companies and private business had already started building. Since 2009, the Department of Energy has spent over $5 billion to get the United States electric vehicle market on its feet.

Now, electric vehicles are again gaining popularity. This can be attributed to the wider selection of electric vehicles available, increased performance, lower prices, and public opinion. Transportation electrification has also found attention in other areas, such as ships, railways, and airplanes. This is a direct result of the massive amount of emissions released from the traditional conventional combustion engine-based transportation methods. It is well known that by electrifying transportation, the net amount of pollutants emitted into the atmosphere would be significantly reduced—even if the electricity used is generated from oil. That net savings is because consumer transportation accounts for around half of the urban pollution in the U.S. and combustion engine are much less efficient at converting the chemical energy in oil to mechanical energy for transportation than oil-based generation techniques are at converting the same chemical energy into electrical energy. Nonetheless, transportation electrification has not widely adopted

because of its performance limitations. Many of these performance limitations—including range, cargo space, and cost—can be addressed by increasing the power density (kW/l) and specific power (kW/kg) of the power electronic systems used in the transportation system.

1.2 Electric Motor Drive

As stated previously, the range, cargo space, and cost of electric vehicles are closely tied to the electrified drivetrain, especially the power electronics that power the electric motors which provide the propulsion for the vehicle. Most commonly, alternating current (AC) motors are used to power electric vehicles because they are more efficient and require less maintenance than direct current (DC) motors.

For any type of electrified transportation system to operate with the user's desired characteristics—which may include a certain speed, torque, acceleration and/or deceleration profile—the electric motor(s) providing propulsion must perform accordingly. To operate at the desired speed and torque, AC motors require an electric motor drive to supply the correct voltage, frequency, and current. The fundamental component of an electric drive is the inverter, which converts DC power into AC power. Whenever the drive is used in a vehicular application, it is usually referred to as a "traction" application. The following section will discuss the common topologies of traction inverters and explain their operation.

1.3 Traction Inverter

In general, an inverter is any device that converts electricity from the DC form to AC form. This would include devices that do not provide a variable voltage or frequency output, such the portable power inverters available today used to provide 60 Hz, 120 V power from a DC battery. As previously mentioned, to get the proper mechanical output from an AC motor, electricity with

proper characteristics—voltage, frequency, and current—must be supplied to the motor. Providing this power is the job of the inverter. A traction inverter's job is much more complex than a basic portable power inverter because it must have the ability to regulate its output voltage, such that the motor can track its speed and torque references, which is usually changing in real time.

Before discussing the topology of the inverter in vehicular applications, it is important to realize the role that the inverter fills in the vehicle to give context to the discussion. There are many different types of electric and hybrid electric vehicle configurations that share same fundamental components, i.e., the battery, electric motor, differential, combustion engine, and inverter. Some examples of these vehicle configurations are shown below in Figure 1. From these figures, it is shown that the inverter always serves as the link between the battery (a DC source) and the electric motor (an AC machine).

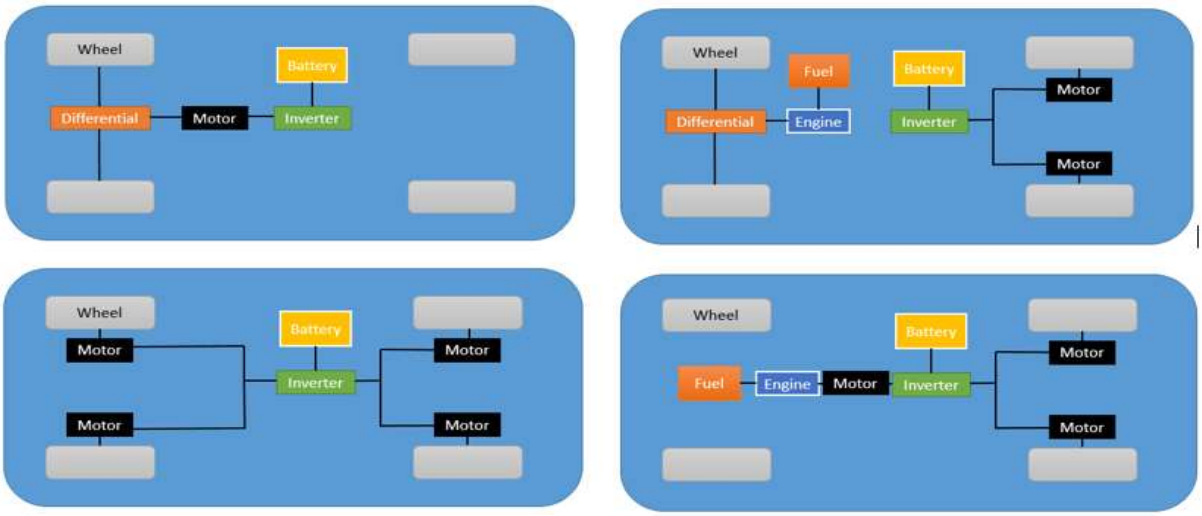

Figure 1 Common Electric and Hybrid Electric Vehicle Configurations

A common traction inverter topology is shown below in Figure 2, which consists of 3 essential parts, i.e, the DC source, DC-link, and the inverter. The gate driver and controller are not part of the energy transfer from DC to AC but are still essential to operation, as they serve to

control the power electronics which handle the energy transfer. The DC-link, gate driver, and controller are shared with all traction inverter topologies, with the most prevalent topologies for vehicular applications being the voltage source inverter, the current source inverter, and soft switching inverters. Most commonly, the DC source is a battery bank, but in some cases, it may be connected to a type of synchronous or active-front-end AC to DC converter.

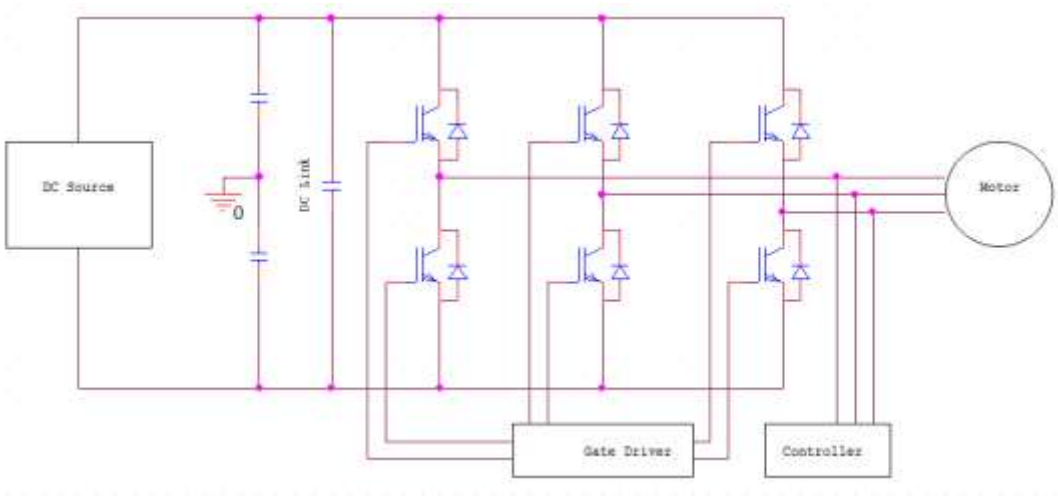

Figure 2 Traction Inverter System Overview

1.4 Traction Inverter Topologies

1.4.1 Voltage Source Inverter

The voltage source inverter (VSI), as shown in Figure 3, is the most popular topology for electric vehicle applications because electric vehicles use batteries to store energy and batteries provide a constant DC voltage. The natural constant DC voltage provided by batteries, which may be further stepped up by a boost converter, make the VSI very easy to implement when compared to other inverter types such as the current source inverter (CSI). In addition, the output voltage of a VSI is independent of the loading condition of the motor. This is noteworthy because for CSI, the output voltage is dependent on the load, which further complicates the control of the inverter.

In general, the VSI operates at higher efficiency than other topologies and is arguably reliable because it has fewer components than the alternatives.

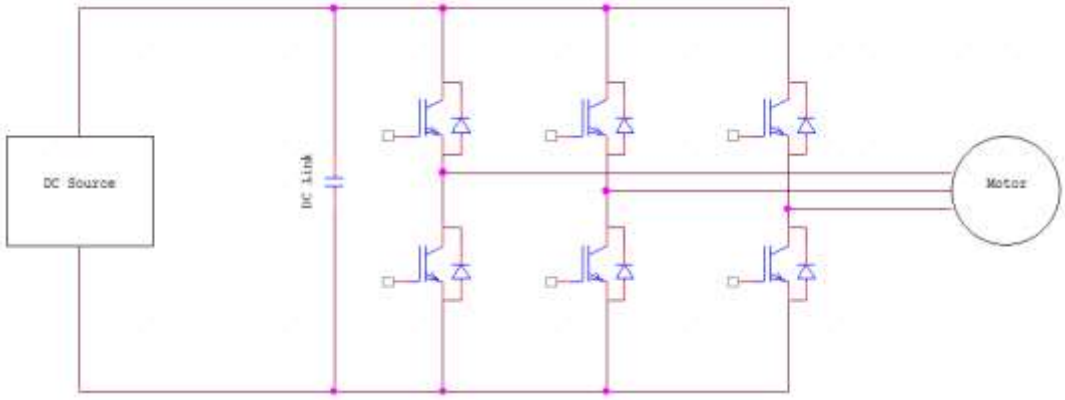

Figure 3 Voltage Source Inverter Topology

The VSI does have a handful of inherent shortcomings. Its dependence on a constant DC voltage power supply usually requires that a large capacitance be connected across its input as shown in Figure 3 to overcome the output impedance of the DC source. This capacitance must be placed as close to the switches as possible to maximize the power quality, especially for inverters built by wide bandgap devices. The capacitors are required to be of very high quality so that they have the highest reliability possible—the capacitors are often the sole cause of inverter failure—and the lowest equivalent resistance and inductance. This is a disadvantage because the DC link capacitors available that would fit this bill are often very expensive and large, accounting for almost a third of the inverter's size. In addition, the output voltage of the VSI cannot exceed the DC link voltage. This effectively limits the constant power-speed range of the connected motor, because in the same given system, if a CSI were to be connected to the DC supply, the inverter output voltage would be able to exceed the DC link voltage.

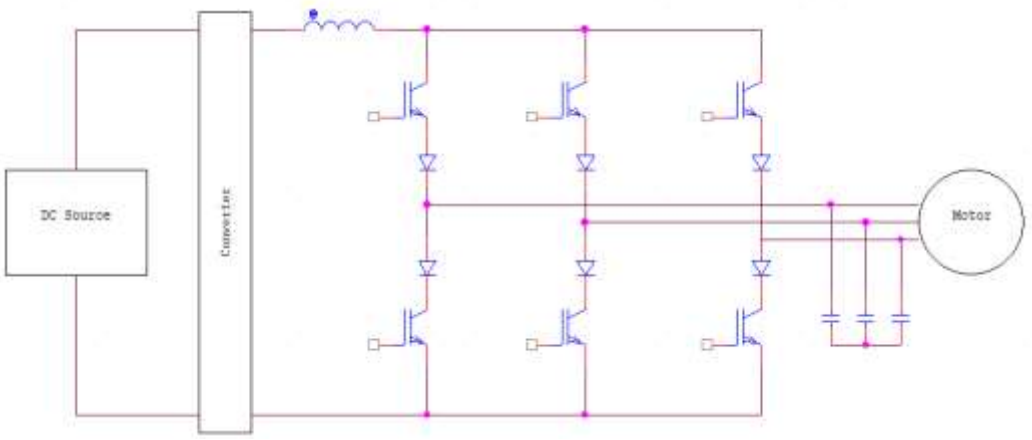

Figure 4 Current Source Inverter Topology

1.4.2 Current Source Inverter

As presented in Figure 4, the CSI topology is sometimes selected to address the weaknesses of the VSI. At first glance, many would notice that the CSI does not utilize DC bus capacitors. Instead, its energy storage is through inductance. Even though there are no DC link capacitors required, the CSI typically necessitates the use of filter capacitors at its output to filter the inverter's current pulses at its output. The CSI has some inherent benefits, being that it provides cleaner voltage with less dv/dt to the motor because of its output filter and that the shoot through short circuit possibility does not have to be considered. What may be considered the largest advantage of the CSI is its ability to allow operation with the output voltage of the inverter above the DC-link voltage. Of course, another stage could be implemented with the VSI to boost the DC voltage up to the desired level, but the CSI negates that need, possibly allowing for higher power density. By allowing for a higher output voltage, the CSI extends the constant power-speed range of the connected motor.

The CSI does have its own list of drawbacks. The CSI has been shown to be difficult to reliably control under light loading and slow speed conditions. Also, to date, the CSI has been

difficult to implement in many applications because the semiconductor switches used must be able to block both forward and reverse voltages. In many cases, there are no switches available that are rated to block forward and reverse voltages whose magnitudes are as large as the DC-link voltage. This means that diodes must be placed in series with the switches. Besides increasing cost and size, the diodes also increase losses, which is generally why the VSI is more efficient than the CSI. Furthermore, the CSI should have a converter at its front end to ensure that the DC source behaves as similarly to an ideal current source as possible, since the CSI depends on a near-constant current source. It is also worth noting that generally, the inductor on the DC link is large compared to the whole inverter system—even larger than the DC link capacitors used in a VSI.

1.4.3 Soft Switching Topologies

Some consideration in industry has been paid to soft switching inverter topologies, which encompass many circuits that have one thing in common—they utilize zero voltage switching (ZVS) and/or zero current switching (ZCS). Theoretically, employing ZVS and ZCS eliminates switching losses. This is because power dissipation is given by $p(t) = i(t) \times v(t)$, where p is power in watts, i is current in amps, and v is the applied voltage. Switching losses occur when the switch switches states from open to closed or from closed to open. While switching, there is a voltage difference across the switch while it is simultaneously carrying current, as shown below in Figure 5. If either the voltage or the current were decreased to zero first, and then the switch changed states, no switching losses would occur, as illustrated in Figure 6. By using ZVS and ZCS, the inverter's efficiency may be increased because a large portion of the inverter's losses come from switching losses.

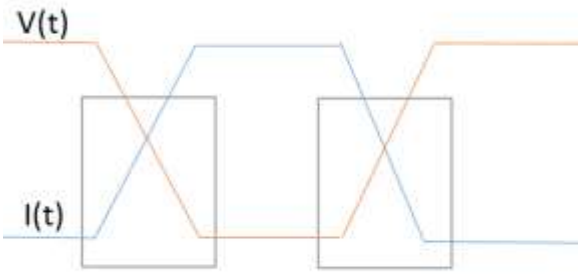

Figure 5 Typical Hard Switching Waveform

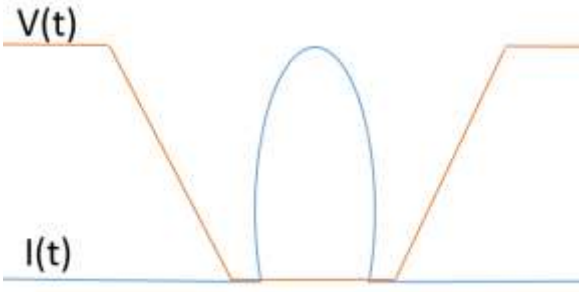

Figure 6 An Example Waveform of Soft Switching

Soft switching topologies have seen limited use in traction applications because of two primary reasons, the first being reliability. Soft switching topologies always have a much higher number of devices, which means that a failure of a single component within the complete system is more probable. The increased number of components also implies that the overall system will have a larger size. Secondly, the efficiency of the VSI and CSI typically are not low enough to justify the small efficiency gain yielded in exchange for lower reliability, higher cost and device count, lower power density, and much more complex control.

1.4.4 Multilevel Inverters

Multilevel inverters have seen widespread use in industry because of several attractive traits which make them suitable for medium and high-power applications. There are several major

multilevel inverter topologies being used today: the neutral point clamped (NPC) inverter, the capacitor clamped inverter, and the cascaded H bridge inverter. Since the output voltage (line-to-line) generated by multilevel inverters usually has over 5 voltage levels—as opposed to the 2-level inverter's 3 voltage levels—multilevel inverters generate outputs with lower dv/dt, which allows for significantly lower distortion in the output voltage and lends itself to a more practical high-power system implementation. The reason for this increased power capability is that every switching device used in the real world will have some finite dv/dt limit that cannot be exceeded without device failure. If the system designer increases the output voltage levels—which is usually required for high power applications—without increasing the number of output voltage levels in the inverter, eventually the power level will become limited by the dv/dt that comes with increasing the voltage. This problem is solved by using a multilevel inverter. Furthermore, it is common for high power applications to require very clean output and input power, both of which multilevel inverters naturally satisfy by achieving lower harmonic content due to additional voltage levels.

1.5 POETS Traction Inverter Goals

This project was sponsored by the Center of Power Optimization of Thermo Electrical Systems (POETS), which is a National Science Foundation (NSF) Engineering Research Center that seeks to create optimized integrated thermo-electrical systems that push the achievable power densities by electrical systems beyond what is currently available. POETS initiated this project to explore what power densities they could achieve by a power converter designed for traction-based application by using silicon carbide power modules instead of the traditional silicon-based devices. This goal is desirable because silicon carbide-based power modules enable module designers to create smaller packages while simultaneously allowing system designers to operate at higher switching frequencies, which allows for smaller passive devices.

More specifically, major specifications for the designed POETS traction inverter include: a power conversion unit using SiC, capable of handling up to 150 kW with a maximum line-to-line voltage 440 V_{rms} using a realistic-for-hybrid-electric-vehicles coolant, which may have a temperature up to 105 °C. Furthermore, the power density of the inverter system should be greater than 25 kW/L.

Because the top priority of POETS is to reach the highest power density possible, the 2-level inverter topology was chosen. Although it may not be practical for very high power or high voltage applications because of power quality and device rating issues, its output power quality is typically considered to be sufficient for the 150 kW motor drive goal of this project. More importantly, the 2-level inverter requires the least number of components, which means that the overall system can be reduced more easily than the other inverter topologies listed.

1.6 References

[1] Aaron VanderMeulen and John Maurin, "Current source inverter vs. voltage source inverter topology," in Eaton White Paper WP020001EN., June 2014

[2] AC. Chan. "An overview of electric vehicle technology," in Proceedings of the IEEE., Sep. 1993, vol. 81, no. 9

[3] Ali Bazzi. "Automotive power electronics multidisciplinary design," in IEEE Transportation Electrification Community., Feb. 2014

[4] Aaron VanderMeulen and John Maurin. "Current source inverter vs. voltage source inverter topology," in Eaton White Paper WP020001EN., June 2014

[5] Najafi Ehsan and Abdul Halim Mohamed Yatim. "design and implementation of a new multilevel inverter topology," in IEEE Transactions on Industrial Machines., Nov. 2012, vol. 59, no. 11

[6] Chris Mi, Fang Z. Peng, Kenneth J. Kelly, Michael O'Keefe, and Vahab Hassani. "Topologyk design, analysis and thermal management of power electronics for hybrid electric vehicle applications," Inderscience Enterprises Ltd. Geneva, Switzerland., 2008, vol. 1, no 3

[7] Sheldon S. Williamson, Ali Emadi, and Kaushik Rajashekara. “Comprehensive efficiency modeling of electric traction motor drives for hybrid electric vehicle propulsion applications,” in IEEE Transactions., July 2007, vol. 56, no. 4

[8] Steven E. Schulz. “Exploring the high-power inverter,” in IEEE Electrification Magazine., Mar. 2017

[9] Y.K. Chin and J. Soulard. “Design study of a traction motor for electric vehicles,” Department of Electrical Engineering, Royal Institute of Technology., Stockholm, Sweden.

[10] “Lesson 33 introduction to voltage source inverters,” in EE IIT, Kharagpur, India

[11] G. Su and L. Tang, "Current source inverter based traction drive for EV battery charging applications," 2011 IEEE Vehicle Power and Propulsion Conference, Chicago, IL, 2011, pp. 1-6.

CHAPTER 2

2-Level 3-Phase Inverter Theory of Operation

2.1 Half Bridge Inverter

2.1.1 Switching States

Because a 2-level 3-phase inverter can be thought of as 3 half bridge inverters, its operation will begin with an overview of a single half bridge inverter. A single-phase half bridge inverter—which consists of two active devices, two capacitors, and a voltage source with an accessible neutral point—is presented below in Figure 7.

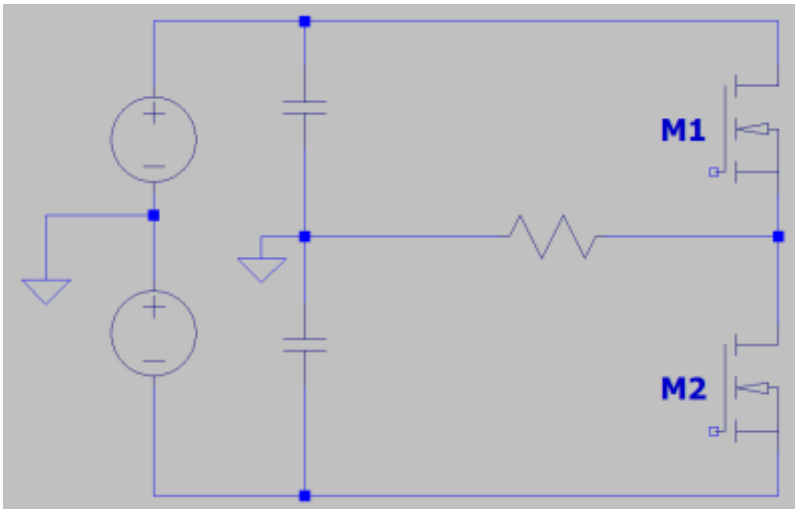

Figure 7 Single Phase Half Bridge Inverter

In this topology, if switches M1 and M2 are turned on and off at the correct time and in the correct sequence, the load will be subjected to an alternating positive and negative voltage level. To achieve a functioning inverter, M1 and M2 are always switched complementary to each other, ensuring that they can never be on at the same time—activating both switches at the same time would directly short the voltage source. When M1 is active, the load is subjected to $V_{source}/2$ and when M2 is active, the load is subjected to $-V_{source}/2$. The same half bridge topology with a

simplified gate driver model for M1 and M2 is presented below, along with relevant switching waveforms.

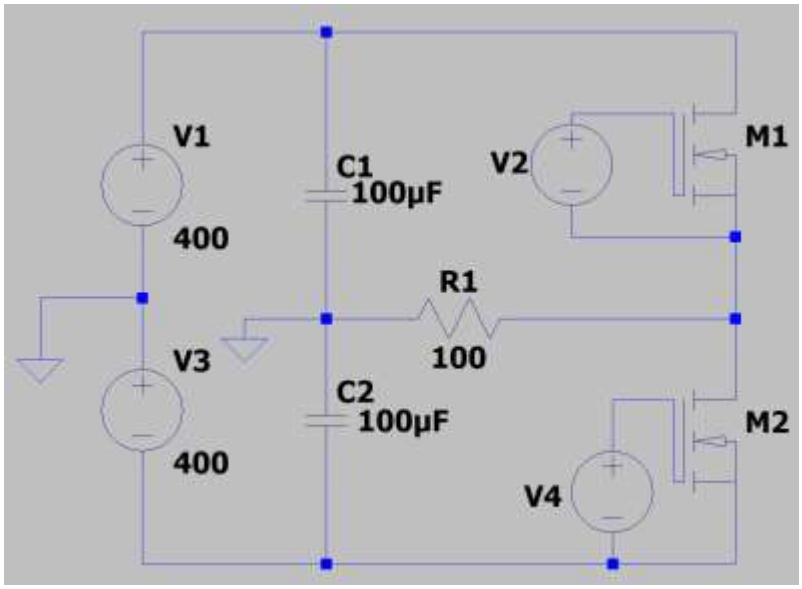

Figure 8 Single Phase Half Bridge with Gate Drive Model and Component Values

To demonstrate the circuit behavior as it pertains to the state of M1 and M2, the above half bridge inverter circuit was simulated at a switching frequency of 500 Hz with M1 and M2 each having a duty cycle of approximately 50% minus a short time interval that was inserted between the switching states of both devices, referred to as dead time, that keeps the voltage source from being directly shorted.

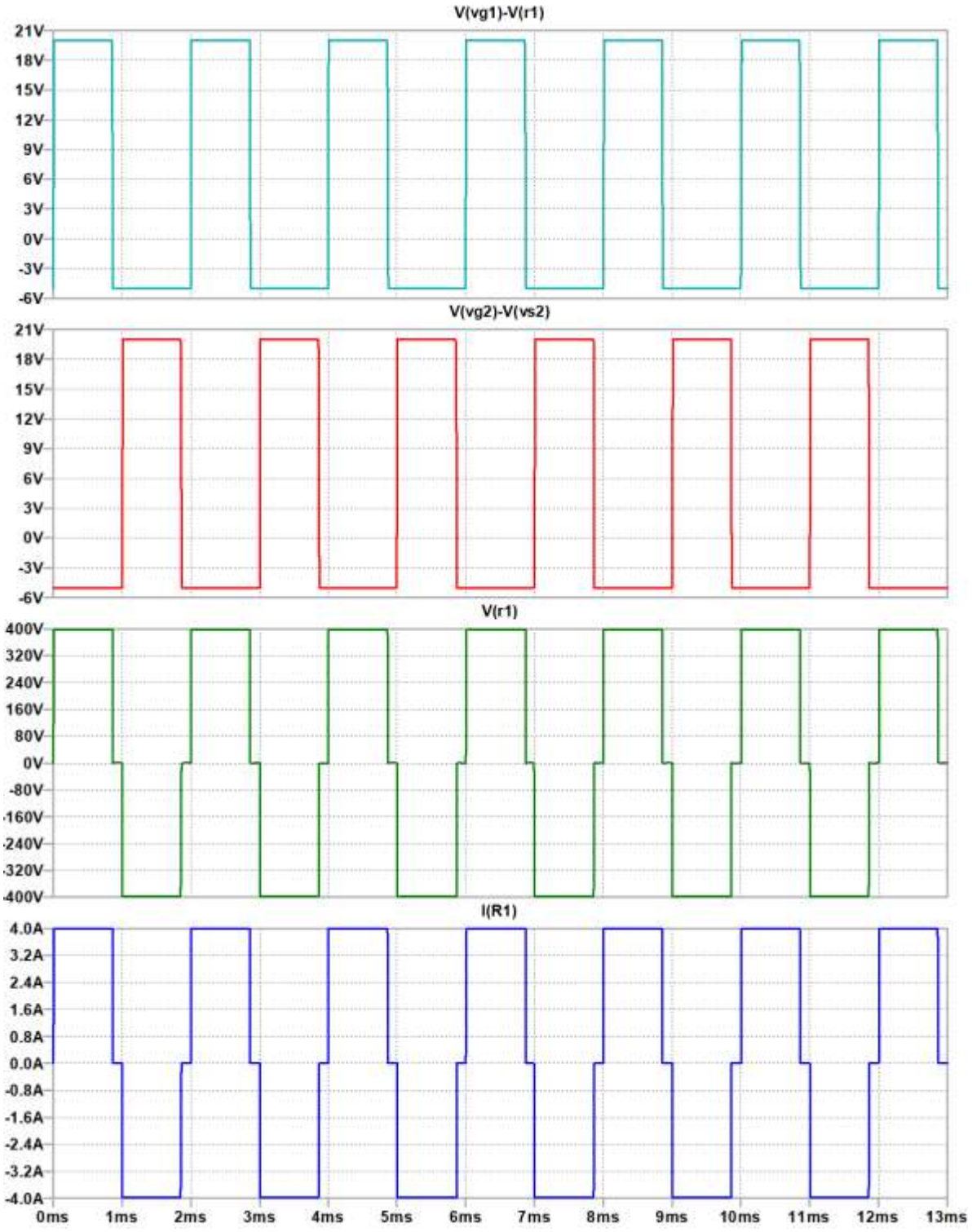

Figure 9 Half Bridge Inverter Switching Waveforms

In the above figure, V(g2)-V(s2) refers to the gate-to-source voltage of device M2, and similarly, V(g1)-V(r1) refers to the gate-to-source voltage of device M1. When either device's gate-source voltage is high, the device will turn on and it will conduct. As such, it is clear from the switching waveforms that when M1's gate-source voltage is high, M1 is conducting, M2 is off, and the load current, I(r1) is positive which follows the positive load voltage that spawns from M1 being on. Conversely, when M2's gate-source is high, M2 is conducting, M1 is off, and the load current, I(r1) is negative because of the negative load voltage that is applied when M2 is activated. Because the load is purely resistive, the current has the exact same shape and phase as the applied load voltage.

2.1.2 Control Method Selection

There are several well-established high-performance control methods for the active devices used in inverters, however, because the goals of this work did not encompass an optimized high-performance controller, a simpler and easier to deploy control method was desirable. With that in mind, along with the ability to test one phase at a time and then easily extend to a three-phase system, sinusoidal pulse-width-modulation (SPWM) was chosen as the method of control for the MOSFETS within the inverter.

2.1.3 Sinusoidal Pulse Width Modulation for Half Bridge Inverter

The following section will explain SPWM as it applies to the half bridge inverter. It can easily be extended to a 2-level 3-phase inverter and will be explained in further detail in a preceding section.

SPWM consists of continuously comparing a sinusoidal reference signal, v_r with a triangle carrier signal, v_c, whose frequency is several orders higher than the reference signal. The output

voltage from the inverter will have square edges because there are only two possible output voltages from the inverter, $\pm V_{source}/2$, however, if the square output voltage is connected to a filter or inductive load, the output voltage have a sinusoidal shape at the same frequency as the reference signal. As such, the reference signal's frequency is set to the user's desired output voltage fundamental frequency. The reference signal and triangle carrier may be scaled however the user desires, but generally for a half bridge inverter the reference and carrier signals span from -1 to +1, where -1 represents the minimum output voltage of the inverter, $-V_{source}/2$, and +1 represents the maximum output of the inverter, $+V_{source}/2$. Whenever the reference signal, i.e., the scaled desired instantaneous magnitude of the output voltage, is greater than the carrier signal, M1 is turned on and the instantaneous output voltage of the inverter becomes $V_{source}/2$. Conversely, whenever the reference signal is less than the carrier signal, M2 is turned on and the instantaneous output voltage of the inverter becomes $-V_{source}/2$.

While the range of the carrier waveform will remain fixed—usually at -1 to +1—the reference signal's range may be changed as necessary. The relationship between the amplitude of the carrier signal and the amplitude of the reference signal is called the modulation index, m, and is given as

$$m = \frac{v_r}{v_c}. \tag{1}$$

If m is regulated $0 \leq m \leq 1$, the output voltage maximum will be given as

$$V_o = m \times \frac{V_{source}}{2} \tag{2}$$

SPWM simulation results are now presented to present a simple implantation of an SPWM half bridge inverter.

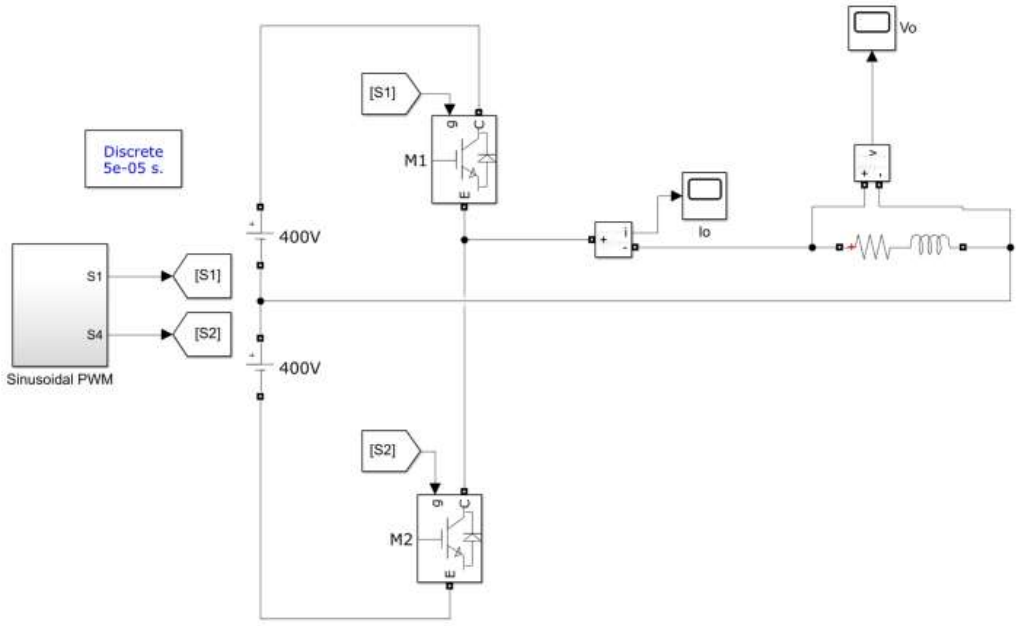

Figure 10 SPWM Half Bridge Inverter Simulation Circuit

In the above figure for simulating SPWM, the two gate signals, S1 and S2, are generated inside the "Sinusoidal PWM" block, which is shown below. The block labeled "m" multiplies the instantaneous value of the sine generator by a factor, the modulation index, which will modify the output voltage as described in equation 2.

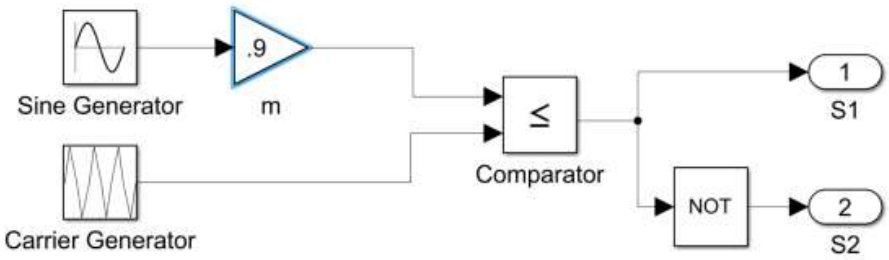

Figure 11 Sine and Carrier Wave Generation

In the simulation, the sine generator was used to create the sinusoidal reference signal, with the following parameters, spawning a fundamental output frequency of 60 Hz.

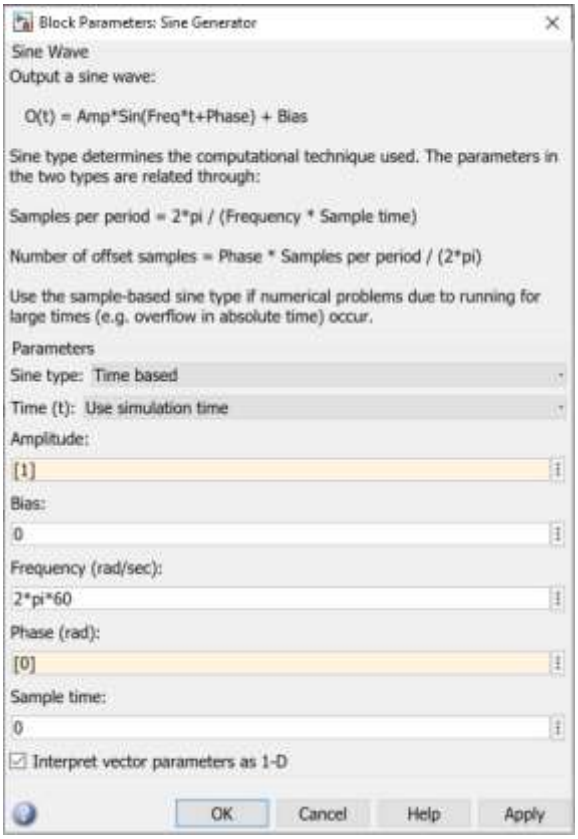

Figure 12 Sine Generator Parameters

Similarly, the carrier waveform was generated using the carrier generation block with the parameters following parameters, for a switching frequency of 20kHz.

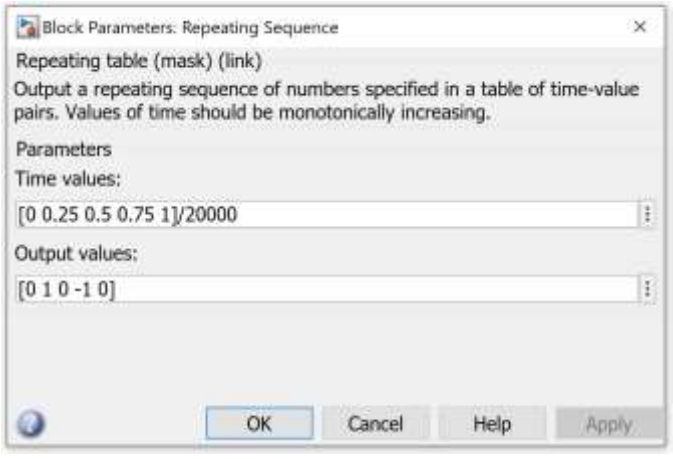

Figure 13 Carrier Waveform Generator Parameters

The circuit shown in Figure 10 was simulated with a modulation index of 0.9 to generate the relevant waveforms, which are presented below. To make the waveforms easier to read, the frequency the sine, carrier, comparator, and gating signals were reduced by a factor of 10. The output fundamental frequency was not changed, as its frequency of 60Hz is much lower than the original switching frequency of 20kHz.

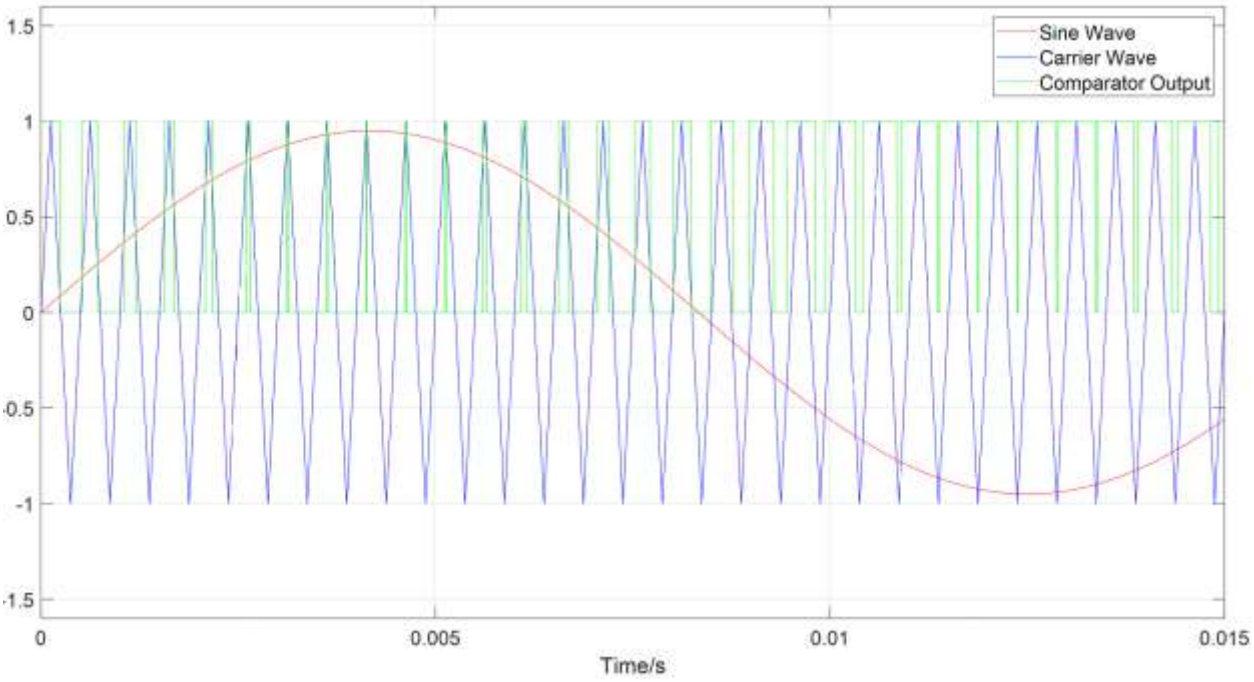

Figure 14 SPWM Sine, Carrier, and Comparator Waveform Full Period

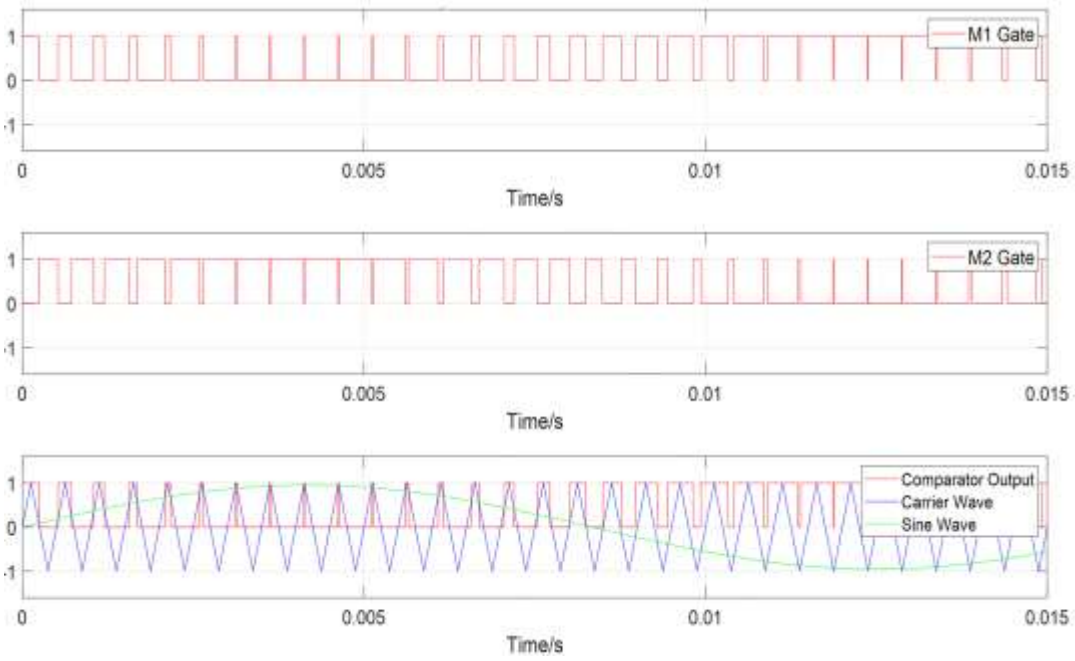

Figure 15 SPWM Sine, Carrier, and Comparator Waveforms with Half Bridge Gating Signals

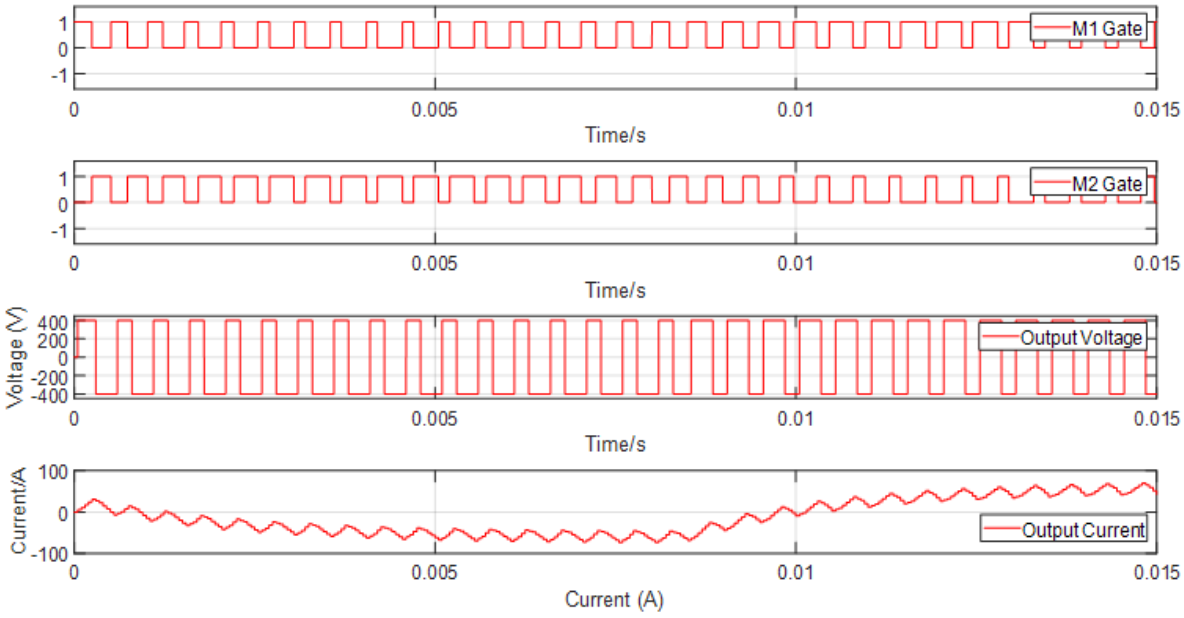

Figure 16 SPWM Half Bridge Gating Signals with Output Current

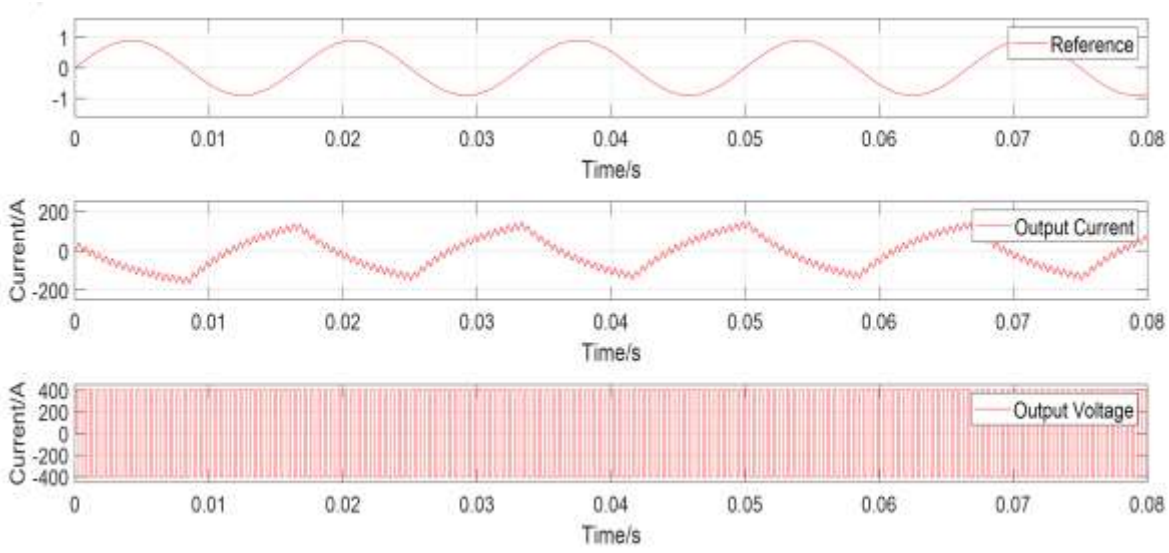

Figure 17 SPWM Half Bridge Inverter Reference Waveform vs Output Current and Voltage

2.2 2-Level 3-Phase Inverter

2.2.1 Switching States

Depicted below in Figure 18 is the 2-level 3-phase inverter topology, which consists of a voltage source, 6 active devices, and their gate drivers. Although there are control methods which treat the complete inverter as one control system, the SPWM controlled 2-level inverter may be thought of as 3 single-phase half bridge inverters—called poles—operating separately, where the 3 phase voltages are taken between each of poles, just as the load is connected in the figure. The phase-to-neutral voltage is given by the voltage difference between the output an inverter phase and the phase neutral point, which is where all three phases are tied together. Just as with any three-phase wye system, the phase-to-phase voltage is given as 1.73 ($\sqrt{3}$) times the phase-to-neutral voltage.

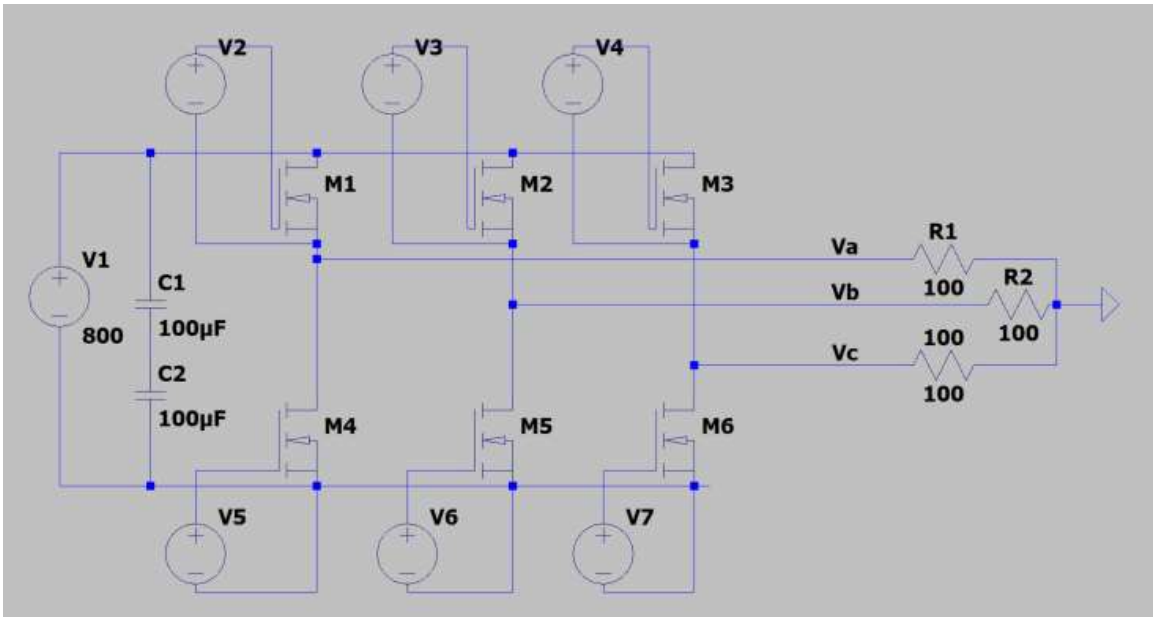

Figure 18 3-Phase 2-Level Inverter

As stated previously, there are many control methods for the 2-level inverter, however, all control methods must utilize the finite number of switching state possibilities, which are presented in Table 1, where the pole formed by M1 and M4 is denoted as S_A, the pole formed M2 and M5 is S_B, the pole formed by M3 and M6 is S_C, and the top position of each pole is taken as that pole's state—either 0 or 1. Just as with the half bridge inverter, the two switches in each pole are activated complementary to each other. Because there are 6 devices that each have 2 possible states, the total number of switching states for the topology is given as 2^3 states. The values in Table 1 are normalized to the source voltage.

Table 1 2-Level Inverter Switching States

Switch State		Pole State				Line Voltage				Phase Voltage		
		S_A	S_B	S_C		V_{AB}	V_{BC}	V_{CA}		V_{aN}	V_{bN}	V_{cN}
1		0	0	0		0	0	0		0	0	0
2		0	0	1		- 1/3	- 1/3	2/3		0	-1	1
3		0	1	0		- 1/3	2/3	- 1/3		-1	1	0
4		0	1	1		- 2/3	1/3	1/3		-1	0	1
5		1	0	0		2/3	- 1/3	1/3		-1	0	1
6		1	0	1		2/3	- 1/3	- 1/3		1	0	-1
7		1	1	0		1/3	1/3	- 2/3		0	1	-1
8		1	1	1		0	0	0		0	0	0

To help visualize each pole's role in generating a three phase output and produce a graphical presentation of the information of the data contained in Table 1, the circuit presented in Figure 18 was simulated with a source voltage of 800 VDC while the phase-phase and phase-neutral voltages were measured. The same gating method used in the half bridge inverter simulation of Figure 10 was used for each pole, however, each of the 3 poles' output were offset 120° from each other. The results are presented below.

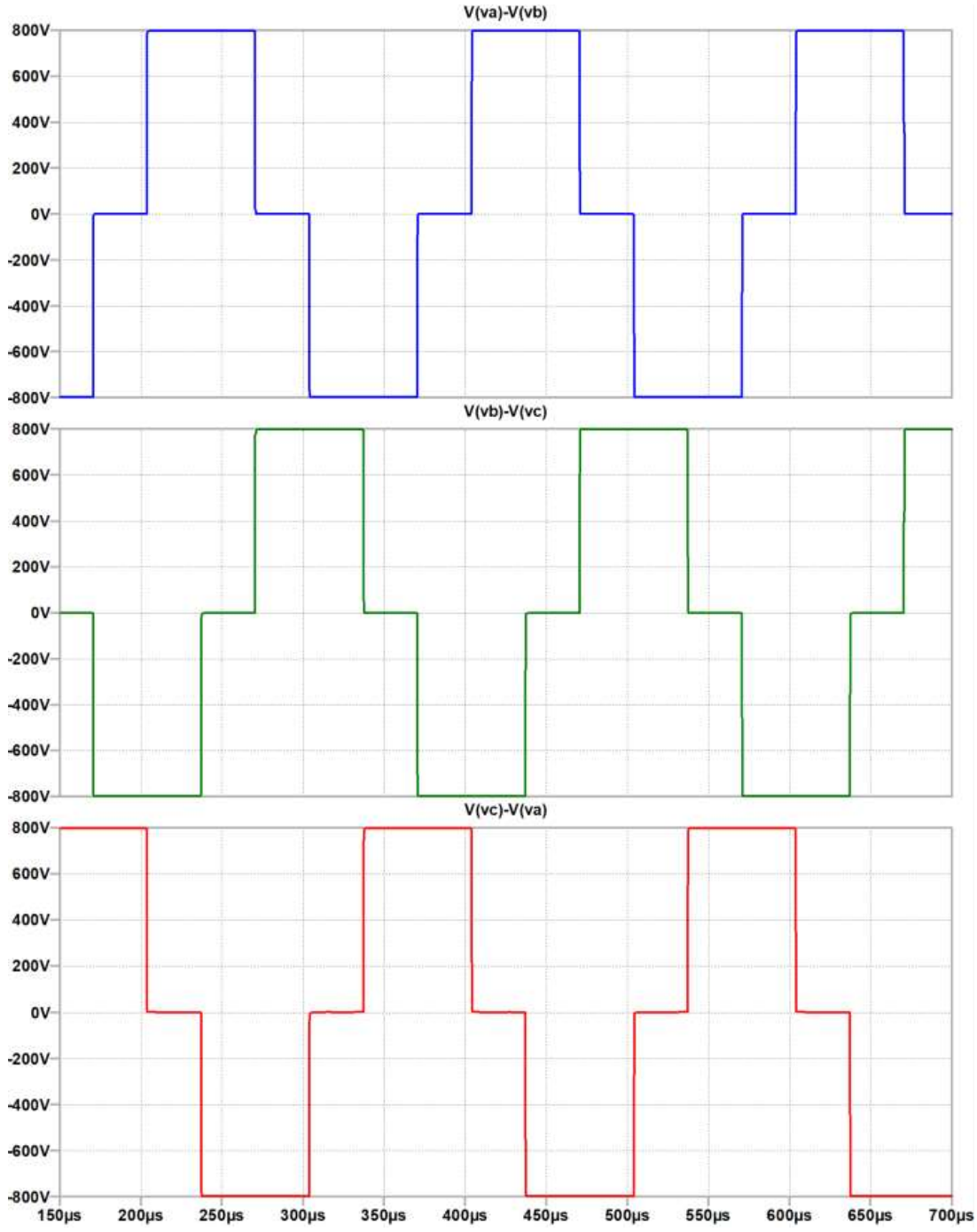

Figure 19 2-Level Inverter Line-Line Voltages

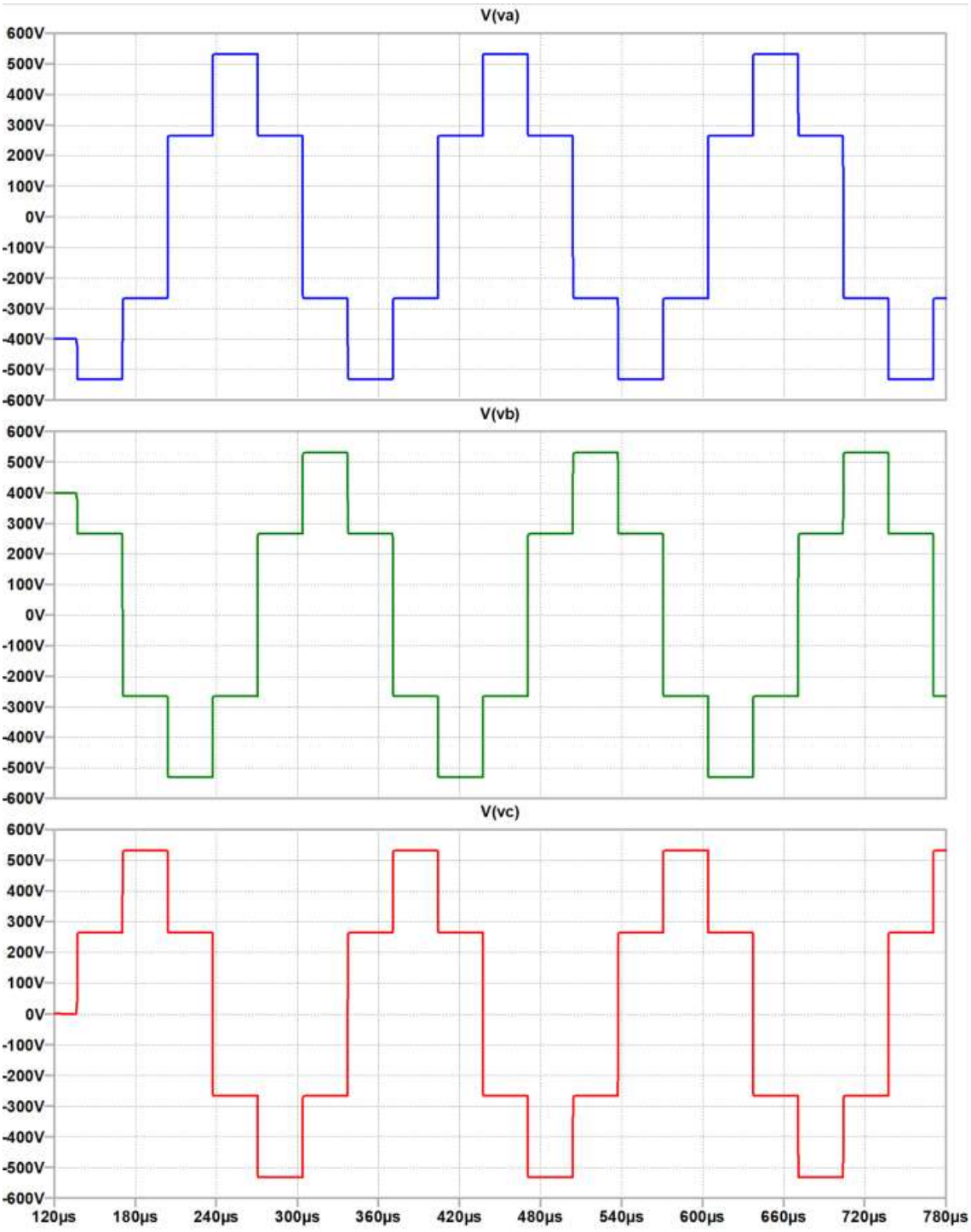

Figure 20 2-Level Inverter Phase Voltages

2.2.2 Sinusoidal Pulse Width Modulation for 2-Level Inverter

SPWM for 2-level inverters follows very straightforward from SPWM for half-bridge inverters. The primary difference is that instead of a single sinusoidal reference waveform, there are three sinusoidal waveforms that are displaced 120° from each other. Each waveform is used as a reference for a single phase of the inverter. Conversely, the controller designer may instead use a single sinusoidal reference waveform and 3 carrier waveforms that are displaced 120° from each other.

For the controller used in this project, three reference waveforms and a single carrier waveform were used. Just as with the half bridge inverter, the value of the sinusoidal reference waveform is continuously compared with the value of the carrier waveform and the result of the comparison is used to control the gating for each switch. For a three-phase inverter, each pole's reference waveform is used to control its respective pole's switches.

The RMS value of the phase output voltage at the fundamental output frequency is given by

$$V_{L-n} = m \times \frac{V_d}{2\sqrt{2}} = 0.354m \times V_{d,} \tag{3}$$

where m is the modulation index as described previously and V_d is the DC-link voltage. The RMS value of the line-line output voltage at the fundamental output frequency is given by

$$V_{L-L} = m \times \frac{\sqrt{3V_d}}{2\sqrt{2}} = 0.612m \times V_d. \tag{4}$$

With the 440 $V_{L\text{-}L}$ output voltage target and the equation for the output voltage of a two-level inverter operating under SPWM, the DC link of the inverter must be no less than 800V—that is if the modulation index is kept at below 0.9.

To further investigate the operation of a SPWM controlled 2-level inverter, the simulation presented in Figures 10 and 11 was extended to 3 phases as shown below.

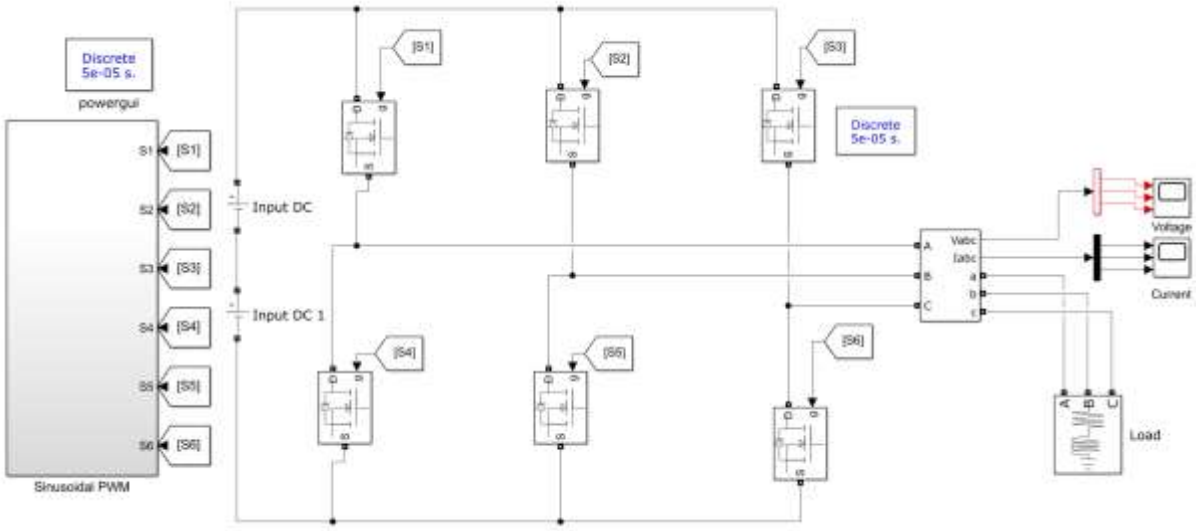

Figure 21 SPWM 2-Level Inverter Simulation

The gating signals, S1-S6, are generated inside the "Sinusoidal PWM" block which is expanded below.

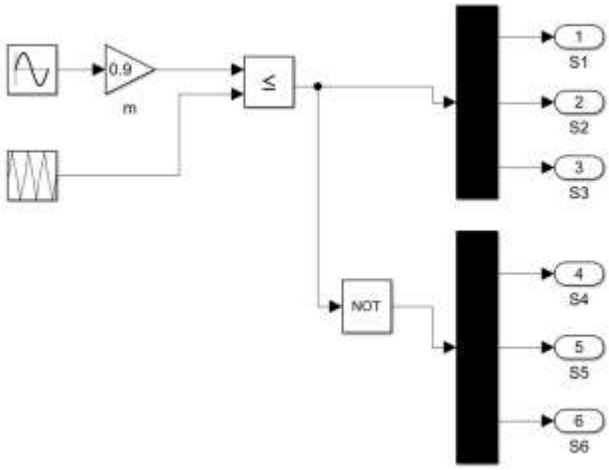

Figure 22 3-Phase Sine and Carrier Wave Generation

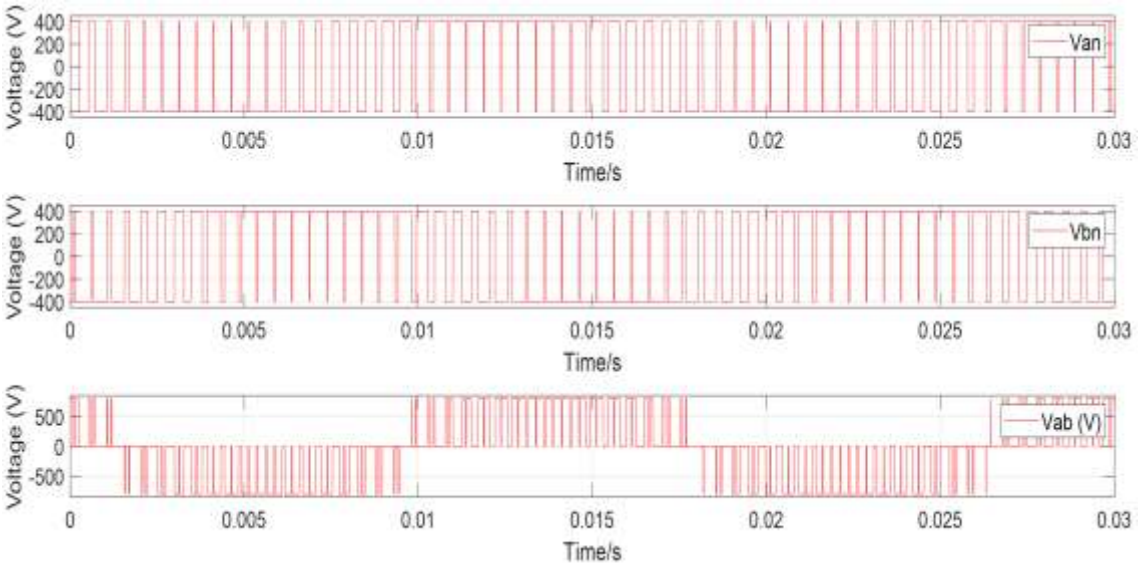

Figure 23 V_{An} and V_{Bn} vs V_{AB}

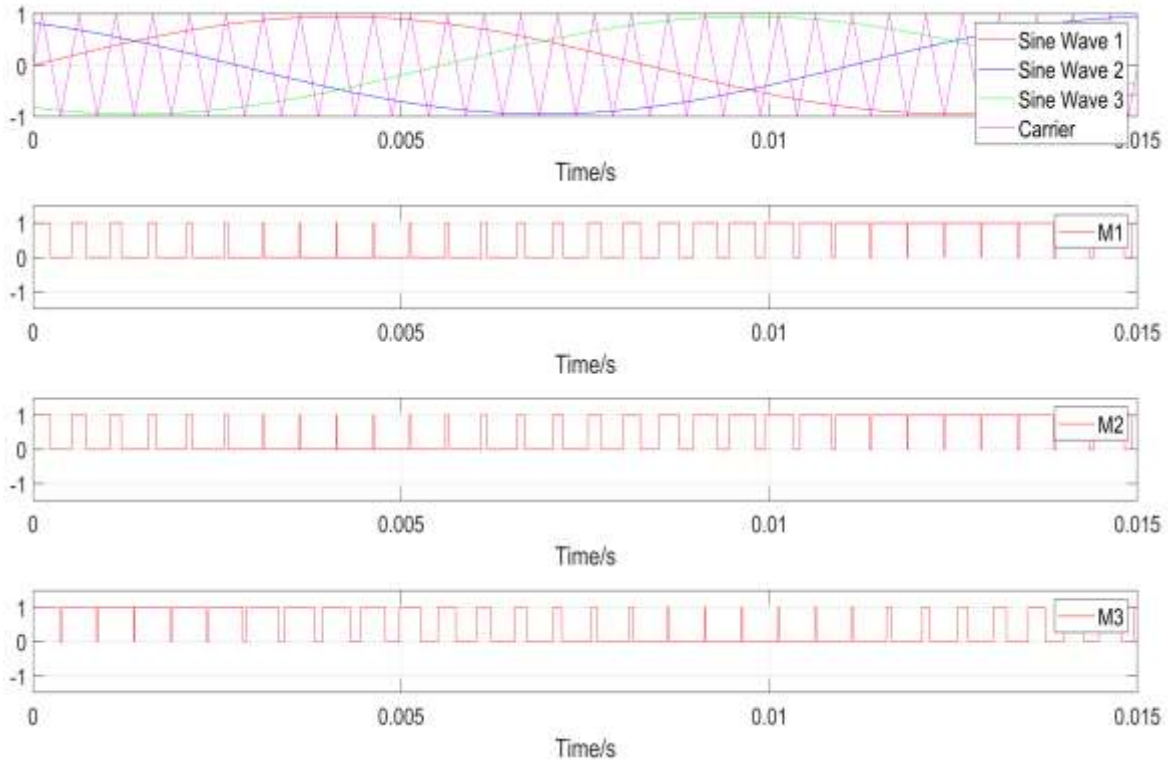

Figure 24 3 Phase Sinusoidal Reference Waveforms with High Side Gating Signals

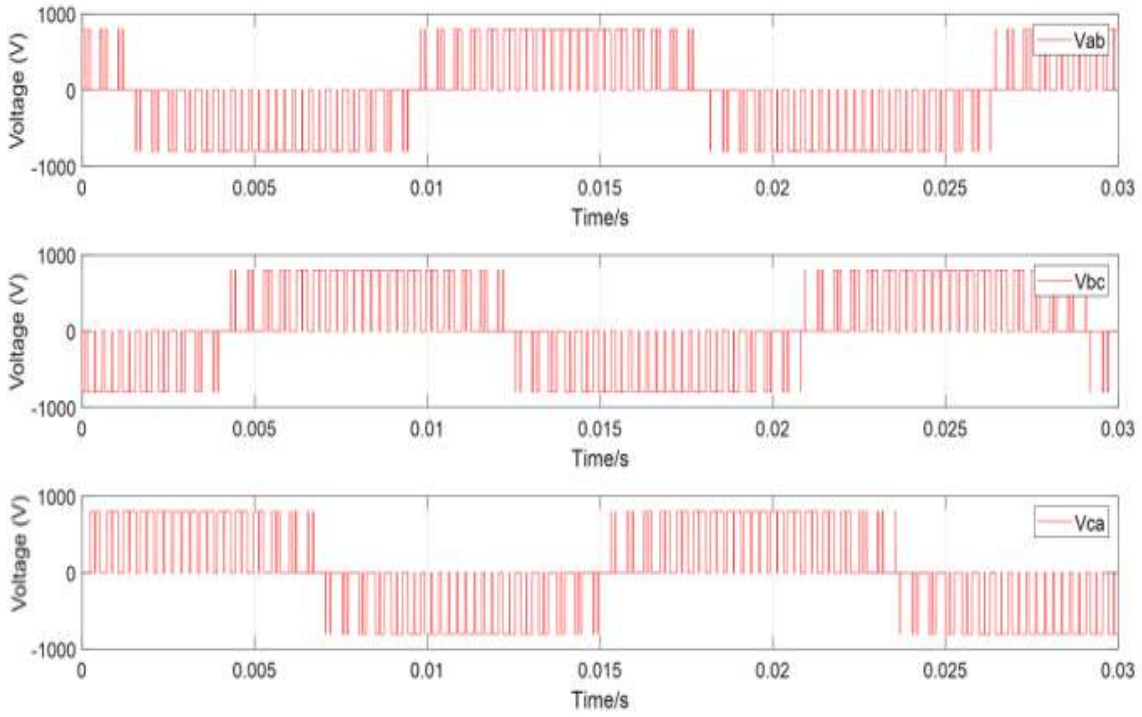

Figure 25 3 Phase Line-Line Voltages

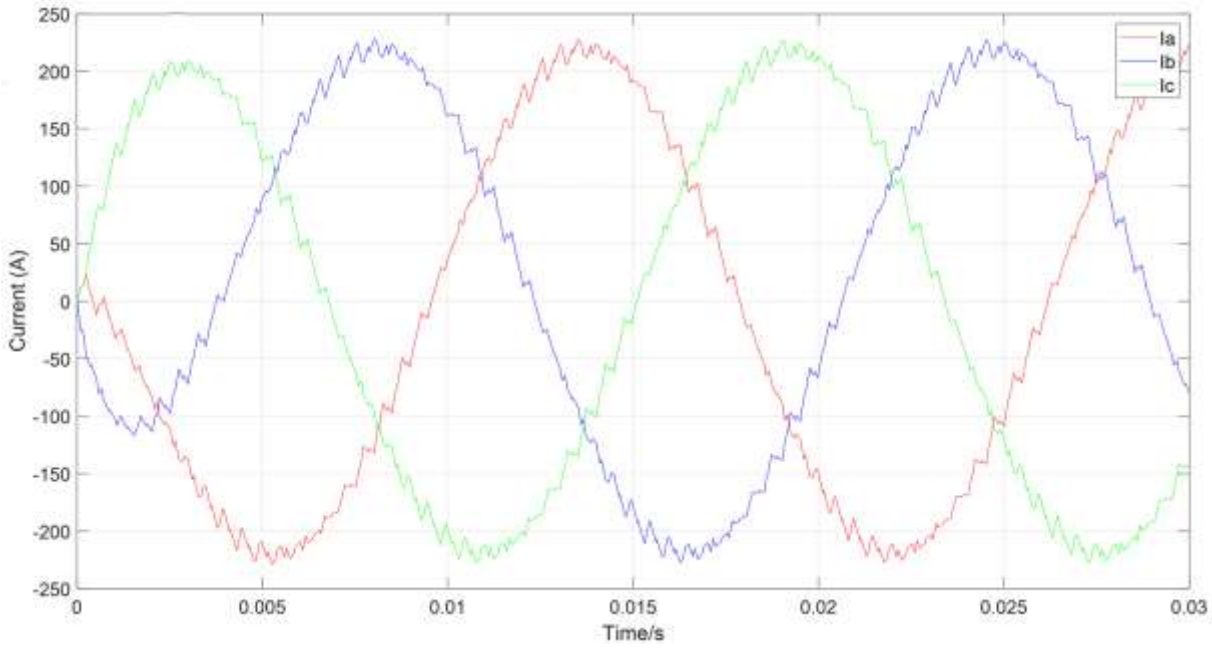

Figure 26 3-Phase Output Current

The above figures were obtained with a very low switching frequency to make the sinusoidal PWM output voltage clear. To demonstrate an output current waveform obtained from a realistic

switching frequency of 15k, the simulation was repeated, and the following waveform was generated.

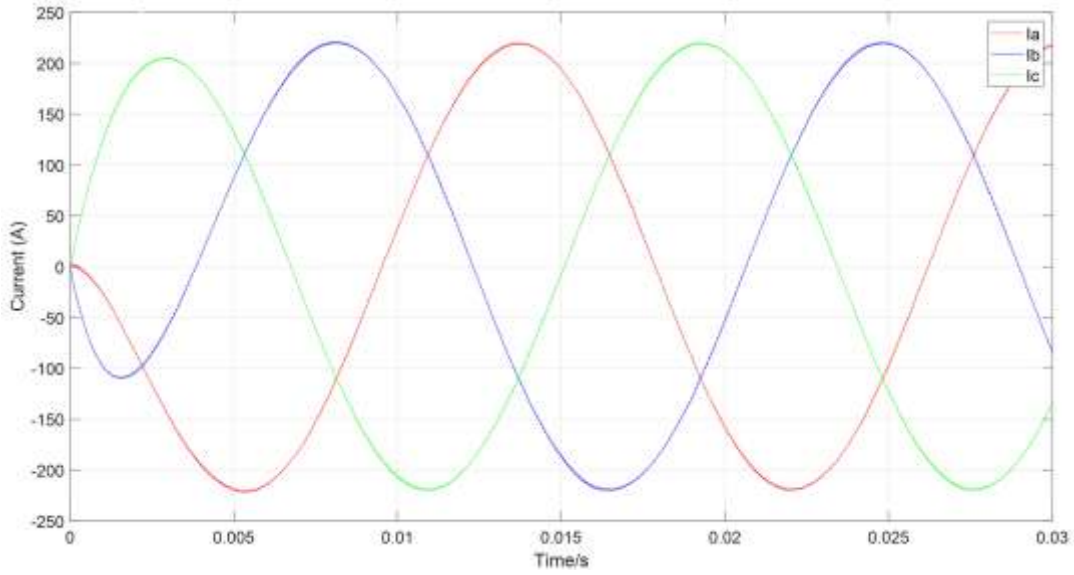

Figure 27 3-Phase Output Current

2.3 References

[1] *Basic Electrical Technology*. Kharagpur, India: Indian Institute of Technology, 2008.

[2] Vanaparthy, S. (2012). PWM SCHEMES FOR THREE PHASE CURRENT SOURCE CONVERT. [online] Tntech.edu. Available at: https://www.tntech.edu/engineering/pdf/cesr/ojo/sravan/thesis_report.pdf [Accessed 10 May 2019].

[3] Tntech.edu. (2012). SINGLE PHASE PULSE WIDTH MODULATED INVERTERS. [ebook] Available at: https://www.tntech.edu/engineering/pdf/cesr/ojo/asuri/Chapter2.pdf [Accessed 10 Feb. 2019].

[4] Collins, M. (2013). Multi-level converter topologies for low voltage drives. [ebook] Helsingborg: Lund University. Available at: https://www.iea.lth.se/publications/BS-Theses/Full%20document/3026_Max_Collins.pdf [Accessed 8 Jan. 2019].

[5] Rahman, F. (n.d.). Three-phase SPWM inverters. [ebook] Sydney, Australia: UNSW Sydney. Available at: https://subjects.ee.unsw.edu.au/elec4614/Lecture%2023%20-%20Three-phase%20SPWM%20Inverters.pdf [Accessed 17 Apr. 2019].

[6] Panda, S., Mishra, A. and Srinivas, B. (2009). Control of Voltage Source Inverters using PWM/SVPWM for Adjustable Speed Drive Applications. [ebook] Rourkela, India: National Institute Of Technology Rourkela. Available at: https://pdfs.semanticscholar.org/5175/79e7abc7e231d2cfff86bfcea7e5f6161cc5.pdf [Accessed 24 Mar. 2019].

CHAPTER 3

The Traction Inverter System Design and Optimization

3.1 Power Module Selection

3.1.1 Inverter Output Current Requirement

Given the maximum power target of 150 kW with a 3-phase output voltage of $440V_{L\text{-}L}$, the required rms output current at unity power factor is 180 amps, given by

$$P_{3\emptyset} = \sqrt{3} \times V_{L-L} \times I_L. \tag{5}$$

Considering that the inverter is designed for traction applications, the power factor of an induction motor must be considered. According Motor Challenge [1], a Program of the U.S. Department of Energy, the typical power factor for a fully loaded induction motor is 0.9, as shown below. Additionally, the induction motor will draw the highest current value when it is fully loaded.

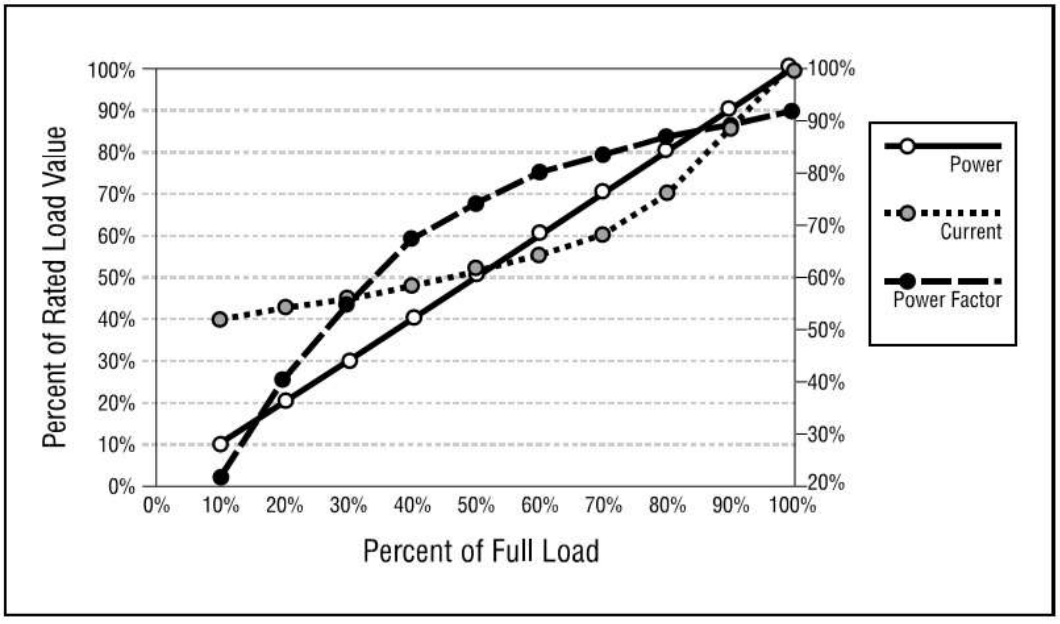

Figure 28 Induction Motor Power, Current, and Power Factor Relationship

Considering the 0.9 power factor at full load, the inverter should be rated for a continuous current of 200 amps, given by

$$P_{3\emptyset} = \sqrt{3} \times V_{L-L} \times I_L \cos\theta, \tag{6}$$

where θ is the phase difference between the current and voltage. The phase angle between the current and voltage can be converted to the power factor using

$$Power\ Factor = \cos^{-1}(\theta). \tag{7}$$

With the output the current requirement in mind, an early assessment based on current ratings was conducted to see what silicon carbide power modules were available that may possibly meet the electrical requirements without being over-sized. Of the possibilities, the Wolfspeed HT-4321 half bridge SiC power module which is in HT-4000 package and rated for a drain current of 264 amps, was selected because it was the smallest power module that may have allowed for the electrical performance targets of the system to be reached. As an added benefit, the HT-4000 series modules are designed to be used with a PCB, which grants the system designer much more design flexibility than traditional bussing compatible power modules. The design flexibility offered by a PCB compatible power module may allow for an increase in power density over a system governed by the limitations of routing copper busbars. Following the early qualification based on current capability, a much more rigorous process was initiated to complete the power module selection process.

When designing power electronic systems, it is common for designers to use the target output power and voltage level to calculate the required current to achieve that power, as was completed above. Following that, a power module is selected based on output current requirement by choosing a module whose datasheet current rating satisfies the calculated current requirement. Although that is a common and convenient approach, it is not the *best* approach to power module

selection. In fact, doing so and pushing the system to its maximum output power may lead to power module failure. Conversely, it may also lead to a system whose power modules are significantly oversized.

3.1.2 Power Module Selection Criteria

In a datasheet provided by the power module manufacturer, the module's maximum continuous current, I_D and maximum power dissipation P_D are usually provided. The reason that a system designer should not directly use those numbers lies within the thermal aspects of the system, in this case the ability to remove the heat generated within the power module as a result of switching and conduction losses. The maximum continuous current and power dissipation rating from the manufacturer is given under very specific conditions, as shown below where a section of the datasheet for the module used in this project is presented.

Maximum Ratings (T_c = 25 °C Unless Otherwise Specified)

Symbol	Parameter	Value	Unit	Test Conditions
V_{DSmax}	Drain – Source Voltage	1200	V	V_{GS} = 0 V, I_D = 100 µA
V_{GSop}	Gate-Source Voltage, Recommended	-5 / +20	V	Static
V_{GSmax}	Gate-Source Voltage, Absolute Maximum	-10 / +25		AC (f > 1 Hz)
I_D	Continuous Drain Current*	264	A	V_{GS} = 20 V, T_C = 25 °C, T_J = 175 °C
		200		V_{GS} = 20 V, T_C = 90 °C, T_J = 175 °C
P_D	Power Dissipated	909	W	T_C = 25 °C, T_J = 175 °C (per switch)
$T_{C(max)}$	Maximum Case Temperature	150	°C	
$T_{J(max)}$	Maximum Junction Temperature	175		
T_{stg}	Storage Temperature Range	-55 to 150		

Figure 29 Maximum Ratings of A Wolfspeed 1200V HT-4000 Power Modules

As shown in Figure 29, the maximum continuous drain current is given under two test conditions, at 175 °C junction temperature with 25 °C case and at 175 °C junction temperature with 90 °C case. Similarly, the maximum power dissipation of the power module is rated at 175°C

junction temperature with 25°C case. Additionally, the continuous drain current rating applies to DC only, while no real continuous AC current rating is provided. If the system designer were seeking to create a system that only used the power module to conduct continuous DC current, the drain current rating may be a fairly suitable number to use, however, when the power module is used to conduct AC or a switching current, the drain current rating becomes much more complex.

It is important to note that neither the amount of current going through the power module nor the amount of power that the power module dissipates are what will cause the module to fail. What will cause the module to fail is operating the module at a point that causes the junction temperature of the MOSFETs within the module exceed their temperature rating (typically 175°C for SiC), at which point the die within the module will start to de-attach from the substrate that they are bonded to or the wire bonds will de-attach from the die and the module will fail. Power dissipation, or power losses, within the module are the sole source of heat within the module. Power losses are unavoidable when a power module is use to conduct any current, and as such, to appropriately select a power module for an AC or switching application, it is imperative to select a power module that will be able to dissipate the amount of power that will be required by the system that the power module will be used in without exceeding the junction temperature rating of the device.

This requirement raises two questions: how much power is the module able dissipate without exceeding the rated junction temperature, and how much power will the system require that the power module dissipate? The power module must be able to dissipate the maximum amount of power that the system requires. To address the first question, theoretically, the system designer could design the system around the power dissipation rating given by the datasheet, in this case 909 W, but there are a couple problems with that approach. The higher the temperature

of the baseplate (case) becomes, the less power the module can dissipate before reaching 175°C at its junction. With that in mind, the power dissipation rating provided in the datasheet is typically given at a case temperature that the system will never operate at, in this case 25°C, which is likely to be very far from where the system designer intends for their system to operate—automotive coolant temperature loops typically operate anywhere from 90°C to 105°C and the module baseplate may reach 30° to 40°C above the coolant temperature. Adding to the coolant temperature dilemma, there is also a significant amount of variability introduced by the type of cooling system used. Because the junction is the source of heat and the coolant in the cold plate or air around the heat sink is what removes the heat from the module, it is desirable to have the highest thermal conductivity from the junction of the module to the liquid or air used in the heat exchanger. As already stated, power module manufacturers give the maximum ratings for their devices based on a given baseplate temperature, typically 25°C. However, because different cooling systems all have varying thermal conductivity, different cooling systems will be able to remove different amounts of heat from the power module even with the coolant or ambient air temperature held constant at say, 25°C. This means that a power module will actually be able to achieve varying amounts of power dissipation from its rating depending on what type of cooling system is used, even when the case is at the temperature specified in the module datasheet.

Furthermore, the thermal interface material (TIM) that is used to minimize the thermal resistance introduced at the interface between the module baseplate and heat exchanger that the baseplate is attached to introduces more variability in the amount of power that a module can dissipate, as different TIMs will also have different thermal conductivities and will therefore allow for varying amounts of heat to be removed from the module. Generally, the datasheet for a power module does not specify which TIM or more importantly, which heat exchanging system—

whether a heat sink, tubed cold plate, gun-drilled cold plate, channeled cold plate, brazed internal fin cold plate, or even a sintered copper pipe—was used. Because cold plates are the most common type of liquid cooling for power electronics in traction applications, the typical thermal impedance of the common types of cold plates is presented below.

Table 2 Typical Cold Plate Thermal Impedances

Type of Cold Plate	**Thermal Impedance**
Pressed Tube	>0.15°C/(W/in2)
Gun-Drilled	>0.12°C/(W/in2)
Channeled	>0.10°C/(W/in2)
Brazed with internal fin	>0.06°C/(W/in2)

These figures are significant because the rate that thermal energy can transferred from the junction of the module to the liquid flowing through a cold plate, P, is controlled by the thermal impedance from the junction of the module to the liquid of the cold plate, R_{jl}, and the temperature differential between the two, as shown in Equation 8. There is a factor of 2.5 between the thermal impedance of a typical brazed internal fin cold plate and a typical pressed tube cold plate.

$$R_{jl} = \frac{T_{junction} - T_{liquid}}{P} \tag{8}$$

With Equation 8 in mind, one may ask why they should not simply calculate the maximum possible power transfer achievable from the module junction to the liquid from the start, using a simplified thermal stack up of a power module and its heat exchanger, which is modeled below. In short, it is because the R_{jl} in every real-life system will be different.

While that approach would yield some accuracy, it is well known that each of the impedances in the model—R_{JC}, R_{TIM}, and R_{SL}—are all values advertised by manufacturers but still may not align

with what the end users see in their system. In addition, it is not uncommon for power module manufacturers to circumvent an actual measurement of R_{jl} and simply simulate it.

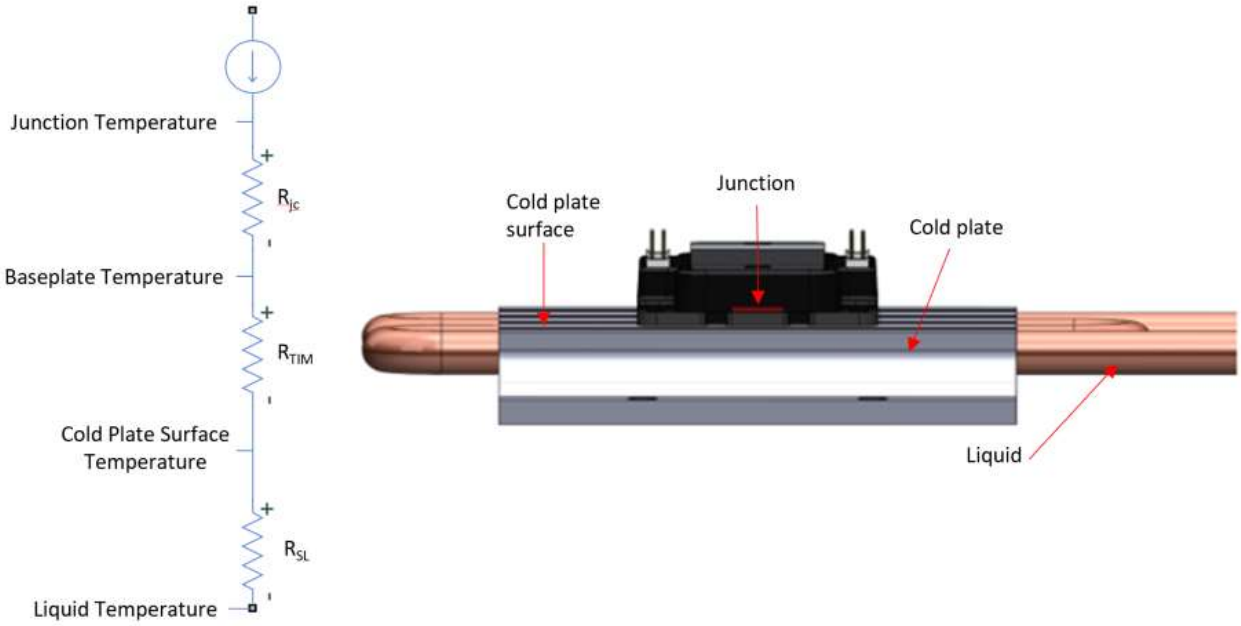

Figure 30 Power Module and Cold Plate Simplified Thermal Stack Up

Considering the unclarity that is introduced by both power module datasheet ratings for continuous current and power dissipation has been discussed, the most accurate way to find the maximum possible power dissipation that the module can achieve in the actual system—which is comprised of its TIM, cold plate, and cold plate coolant temperature—will be presented.

Since the real limiting factor to a power module is the ability to keep its junction temperature under its maximum rating and the ability to remove heat from the power module depends on many variables which can be simplified to the TIM selection and heat exchanger selection, it is highly desirable to thermally characterize the potential power module selection in the real system that it will be used in. This thermal characterization consists of assembling the prospective system, with the prospective power module, TIM, and heat exchanger. Following the

assembly, DC current is pushed through one of the switch positions in the module and increased until the junction temperature of the module reaches its maximum rating. At the time that the maximum junction temperature is reached, the power dissipation of the module is measured. This power measurement is the maximum achievable power dissipation of the module in the constructed system with the given TIM, cold plate, and coolant temperature.

Although this test is strictly DC, this maximum power dissipation measurement is a system property that can be directly used for AC applications as well because the temperature rise of the module does not depend on whether the power dissipation in the module results from purely DC conduction losses or a combination of AC conduction and switching losses. Likewise, the power transfer in Equation 8 does not depend on whether the power dissipation results from only DC conduction losses or AC conduction and switching losses.

3.1.3 Power Module Maximum Power Characterization

In this work, a 1200 V HT-4321 module sample was considered and for the same reasons mentioned above, a test setup was built to find the maximum power dissipation achievable in the system being designed. To accomplish this, the required data to create a virtual junction temperature plot was recorded using a curve tracer, a cold plate was selected, and a custom PCB for the HT-4000 module was made. The test requires a hole to be present in the cold plate to place a thermocouple probe through to enable probing of the module baseplate. In this work, a pressed tube cold plate was obtained and modified to allow the module under test to be mounted to it and have its baseplate probed. This approach was much more cost effective because the liquid in the cold plate only travels through the pipes so there are no issues with simply drilling a hole in the cold plate body. The cold plate shown below was modified by tapping mounting holes for the

module and drilling holes to allow for probing of the baseplate. Next, a fixture was 3d printed to hold the thermocouple probe on the module baseplate.

Figure 31 A Picture of the Cold Plate (Ohmite CP4A-114B-108E) Used in This Work

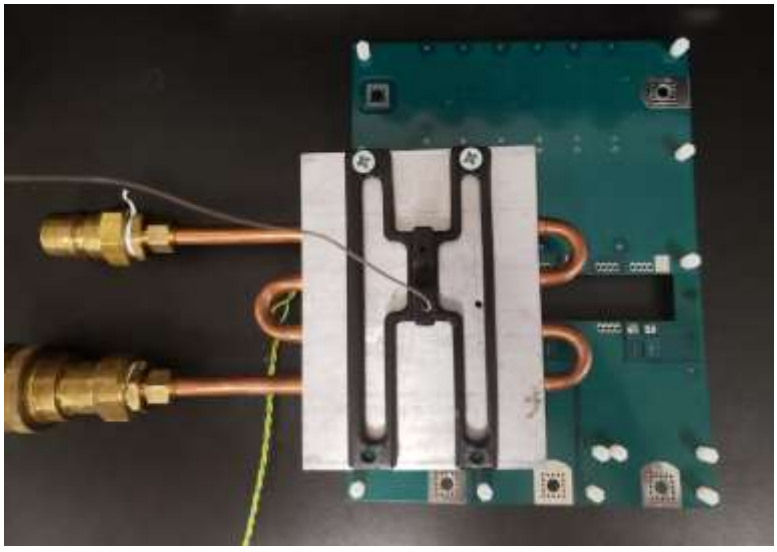

Figure 32 Thermal Characterization Test Setup (Bottom View)

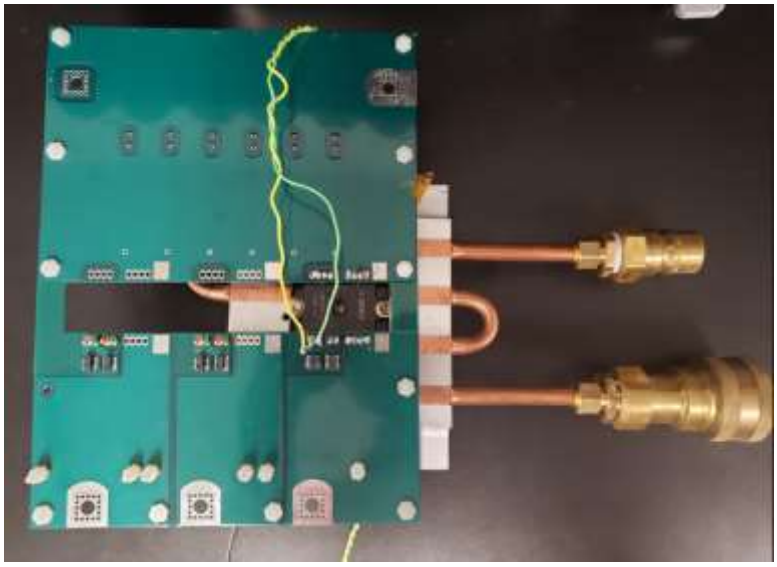

Figure 33 Thermal Characterization Test Setup (Top View)

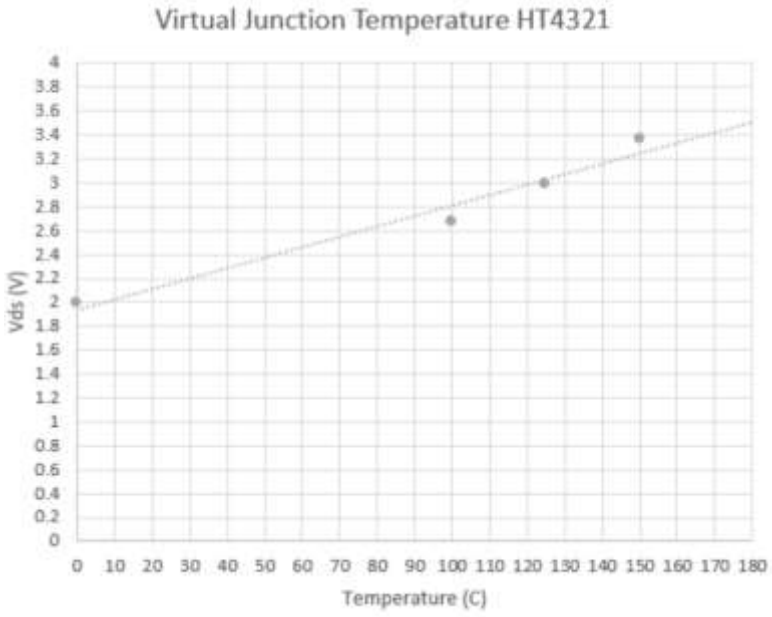

Figure 34 HT-4321 Virtual Junction Temperature Plot

Following the test setup assembly, the PCB was connected to a DC power supply, the cold plate pipes were connected to a recirculating cooler, the module gate connections were connected to a 15V supply, a power analyzer was connected across the module to monitor its drain current

and drain-source voltage (V_{ds}), and the test was commenced. The DC supply was placed in current control mode and the drain current was increased while V_{ds} was monitored. When V_{ds} reached the value that corresponded to a 175°C junction temperature on the virtual junction plot, the power dissipation of the module was recorded. This process was repeated for several different coolant temperatures and the results are presented in Table 3 and Figure 35.

Table 3 HT-4321 Thermal Testing Results

SW1	T_{liquid} (°C)	P_{max} (W)	V_{DS} (V)	I_D (A)	T_{case} (°C)	$T_{junction}$ (°C)	R_{jc} (°C/W)
	25	640	2.75	244	76	175	0.155
	40	620	2.65	234	84	175	0.147
	47	595	2.50	230	86	175	0.150
	61	560	2.56	219	98	175	0.138
	70	510	2.41	212	103	175	0.141
	80	473	2.31	205	110	175	0.137
SW2	T_{liquid} (°C)	P_{max} (W)	V_{DS} (V)	I_D (A)	T_{case} (°C)	$T_{junction}$ (°C)	R_{jc} (°C/W)
	25	645	2.80	230	76	175	0.153
	40	623	2.67	233	84	175	0.146
	47	590	2.55	231	86	175	0.151
	61	555	2.50	222	98	175	0.139
	70	515	2.43	212	103	175	0.140
	80	470	2.30	204	110	175	0.138

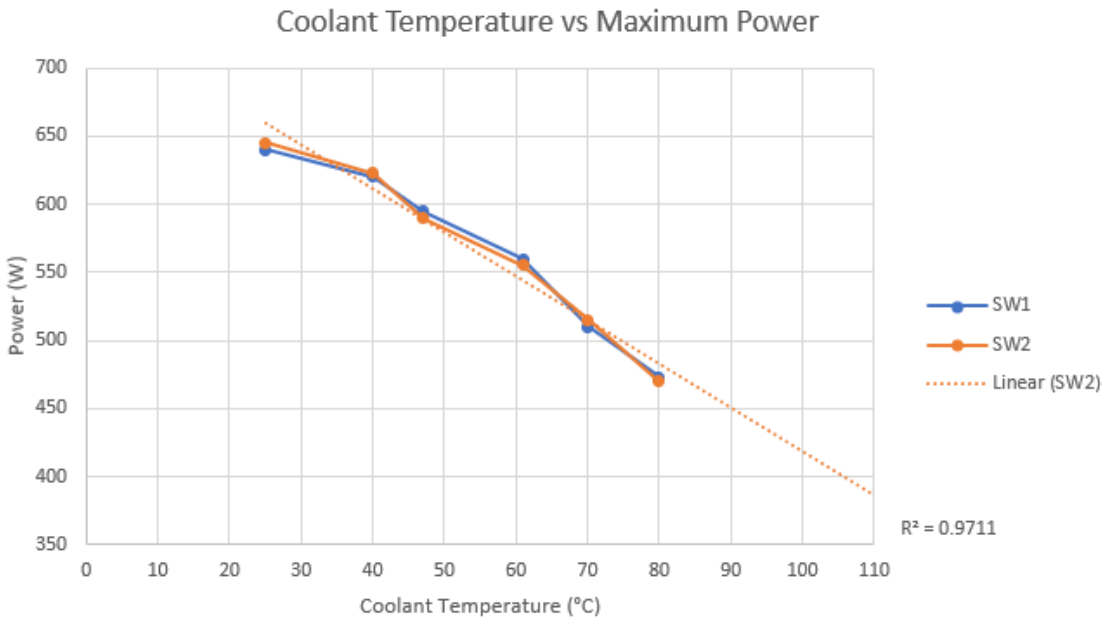

Figure 35 HT-4321 Coolant Temperature vs Maximum Power Results

Based on testing, it is shown that with 25 °C coolant the maximum power dissipation the module can achieve without exceeding its rated junction temperature is 640 watts, which is 30% lower than the datasheet rating of 909 W, when the baseplate is 25°C. Although the design target of the traction inverter is 90°-105°C operation, the highest temperature coolant that the test was conducted with was 80°C because of safety concerns in the lab. It is reasonable to expect the power module to be able to handle around 450 watts with 90°C coolant and 400 watts with 105°C coolant, based on the linearity of Figure 35.

The results from both switch positions being similar means that the thermal impedance from each switch position's die to the baseplate is very similar, however, the maximum power measurement taken should be considered the maximum power dissipation of the complete module as the sum of both positions. In other words, the 909 W datasheet rating is the maximum sum of dissipation by both positions. It does not mean that the module can safely handle 909 W per

position. Similarly, the maximum power test conducted yields the maximum capability of the complete module, but not the simultaneous maximum capability of each switch position. The sum of the power dissipation by both switch positions must not exceed the complete module's rating.

3.2.4 Power Module Loss Calculation

To address the second question, which is how much power will the system require the power module to dissipate, the system designer must calculate the amount of electrical losses that the power module will have in the envisioned system. The electrical losses will be directly converted into thermal energy which is what will cause the module to heat up. With any semiconductor switch, there are two types of losses—conduction losses and switching losses. The total amount electrical power loss associated with a semiconductor switch is equal to

$$P_{Loss,Total} = P_{Conduction} + P_{Switching}. \tag{9}$$

Conduction losses occur whenever the semiconductor carries current and is equal to

$$P = I^2 \times R_{on} \tag{10}$$

where I is the rms of the current going through the switch and R is the on-state resistance of the device. If the device is not in the on state, the conduction losses are zero because the device is not conducting.

Switching losses occur whenever a semiconductor switch changes states resulting in the switch's instantaneous current and voltage being nonzero, as shown by the time periods t_{on} and t_{off} in Figure 36. In a MOSFET, this occurs because the device's unavoidable parasitic capacitance stores energy and then releases it whenever the device transitions between states. Because a MOSFET dissipates energy both when it turns on and when it turns off, its switching losses may be broken down into two components, P_{on} and P_{off}, which are the power dissipations associated

with turning on and turning off, respectively. P_{on} only occurs during t_{on}, and similarly, P_{off} only occurs during t_{off}.

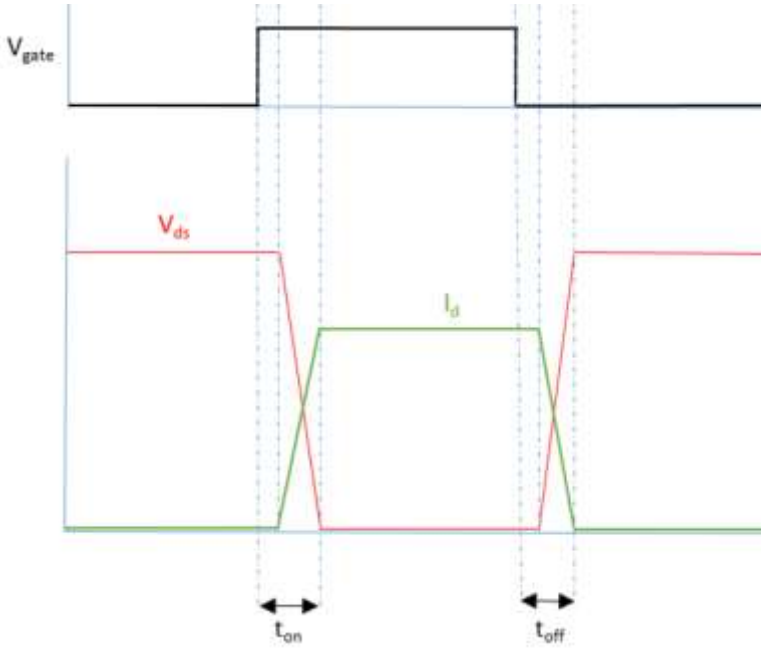

Figure 36 Simplified Waveform of MOSFET Turn-On and Turn-Off Transitions

From the switching waveform figure, it is clear that the switching loss during each transition period is simply the time integral of the voltage and current waveforms multiplied by each other over the switching period, that is,

$$P_{sw} = P_{on} + P_{off} = \frac{1}{T_p}\left(\int_{t_{on-}}^{t_{on+}} i_d(t) \times v_{ds}(t)\, dt + \int_{t_{off-}}^{t_{off+}} i_d(t) \times v_{ds}(t)\right) \quad (11)$$

where:

T_p = switching period,
t_{on-}= the beginning of the turn-on transition,
t_{on+}= the end of the turn-on transition,
t_{off-} = the beginning of the turn-off transition,
t_{off+}= the end of the turn-off transition,
I_d = the drain current of the MOSFET, and
V_{ds} = the drain-source voltage of the MOSFET.

For a MOSFET, the losses that occur in the anti-parallel body diode must be considered as well because they are in the same package as the MOSFET. The MOSFET body diode will generally conduct for a short time when compared to the MOSFET, but it may still contribute significant losses during its turn-off process, which occurs during the "reverse recovery" time, or the time it takes for the forward current carrying diode to switch states to open. During this time, the voltage and current waveforms are both above zero and the switching power dissipation may be calculated in a similar method to a MOSFET, by integrating the product of the voltage and current waveforms of the diode. Considering the diode, the total MOSFET losses are given as

$$P_{Loss,Total} = P_{Conduction} + P_{Switching} + P_{RR} \tag{12}$$

where P_{RR} is the reverse recovery losses from the anti-parallel diode.

With respect to a two-level inverter, the above equations still apply, however, the system designer much consider that an inverter is used to process time-varying voltage and current levels. Because of the varying voltage and current levels, the calculations become much more complicated because as shown above, both the conduction and switching loss of the power module directly depend on the current and voltage level at the time of the switching action. By using the information from the datasheet of the power module, one may estimate the power dissipated by a half bridge (2 positions) power module as the sum of the following:

$$P_{Conduction} = \frac{I_{RMS}^2 \times R_{ON}}{8} \tag{13}$$

$$P_{ON} = \frac{f_{sw}}{\pi} \times \frac{I_m}{2} \times V_{DC} \times \frac{E_{ON_{test}}}{V_{DS_{test}} I_{D_{test}}} \tag{14}$$

$$P_{OFF} = \frac{f_{sw}}{\pi} \times \frac{I_m}{2} \times V_{DC} \times \frac{E_{OFF_{test}}}{V_{DS_{test}} I_{D_{test}}} \tag{15}$$

$$P_{RR} = \frac{f_{sw}}{12} \times t_b \times I_{RR} \times V_{DC} \tag{16}$$

where:

I_{RMS}= the RMS of the output current,
R_{ON}= the on-state resistance of the MOSFET,
f_{sw}= the switching frequency,
I_m = the magnitude of the output current,
V_{DC}= the DC Link Voltage,
E_{ON} = the turn on energy of MOSFET, and
E_{ON} = the turn off energy of the MOSFET.

In both MOSFET equations, the parameters with the "test" subscript are parameters that were measured at the same instant. In other words, for the P_{ON} equation, the E_{ON} value was recorded when switching with a certain recorded V_{DS} and I_D value. As established before, the switching energy will vary depending on V_{DS} and I_D. While certainly possible, the above calculations become very complicated—especially if the system designer uses the turn-on and turn-off vs V_{DS}, I_D, and temperature data provided by the manufacturer. It is much more practical to use a simulation to obtain the estimated switching losses a power module in a 2-level inverter will see. The simulation presented below which operates based on the preceding equations is what was used in this project to find the anticipated power losses in the power module.

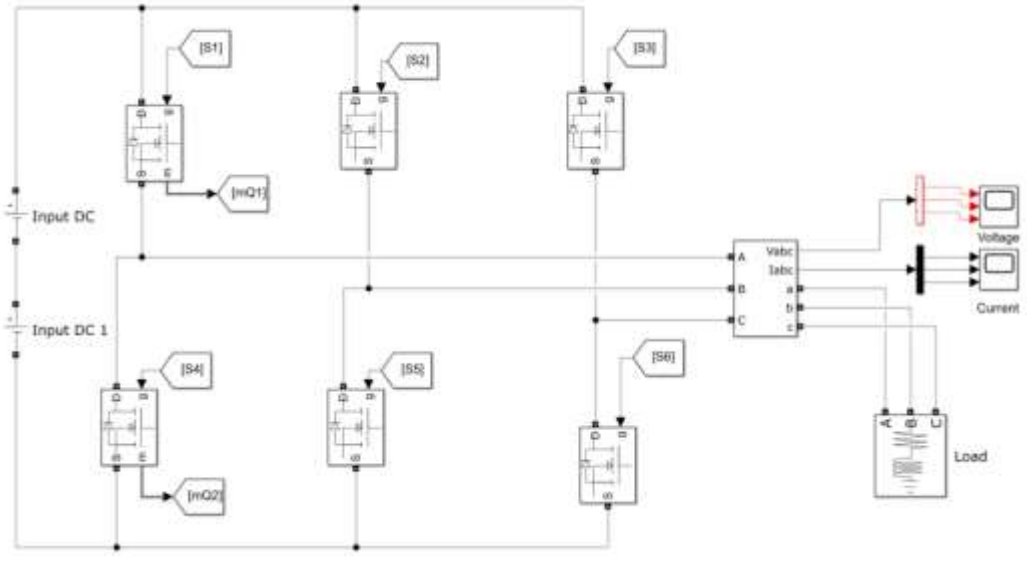

Figure 37 2-Level Inverter Schematic for Loss Simulation

The loss simulation hardware and control circuit are the same as the circuits presented in the theory of operation circuit presented before, with the addition that data from one pole of the inverter is used to calculate the switching losses of that pole. The data stream from MOSFETs S1 and S4, labeled “mQ1” and “mQ2,” contains the instantaneous device current and voltage and is sent to a separate simulation block which calculates the losses based on the “m” block of each device. The loss calculation simulation block is hereby presented and summarized as follows.

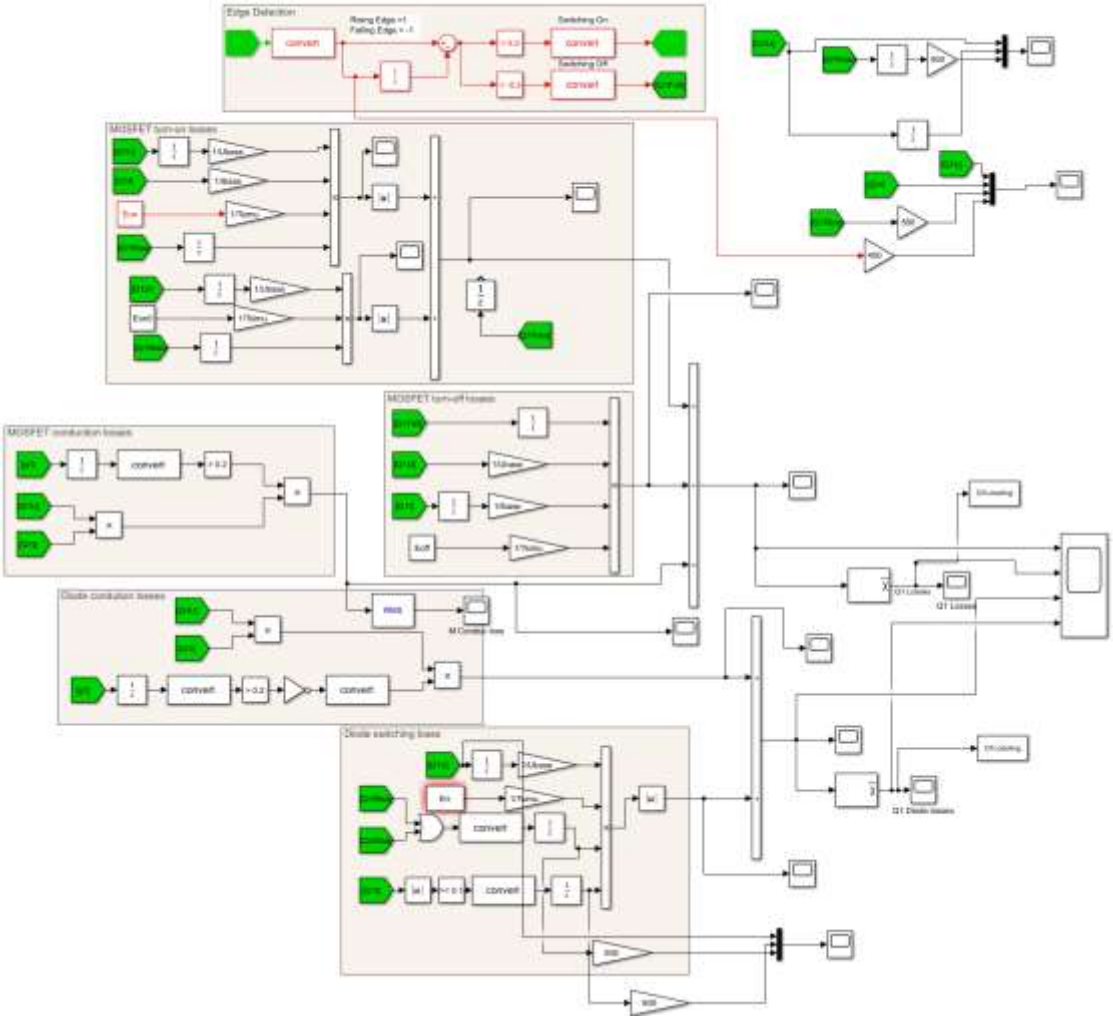

Figure 38 2-Level Inverter Loss Calculation for A Single Pole

The simulation consists of 6 main modules, which are Edge detection, MOSFET turn-on losses, MOSFET turn-off losses, MOSFET conduction losses, Diode conduction losses, and Diode switching losses—each module calculates the parameter that it is named after. The edge detection module is responsible for detecting each switching action and triggering a loss calculation. Each of the other modules is conceptually the same and follows the reasoning previously discussed by calculating each relevant integral while simultaneously looking up the correct Eon and Eoff value. For example, in the MOSFET turn-on section of the simulation, presented below, "Q1U" is the drain-source voltage of MOSFET S1 and "QI1" is the drain current of MOSFET S1. Eon contains a lookup table of the manufacturer provided Eon vs drain current and drain-source voltage data. The correct value of Eon—which varies depending on the device current, voltage, and rise time—is looked up and interpolated based on the manufacturer provided data. Similarly, the MOSFET conduction losses section calculates the conduction losses of the device by multiplying the voltage across the device, Q1U, by the current through device, Q1I.

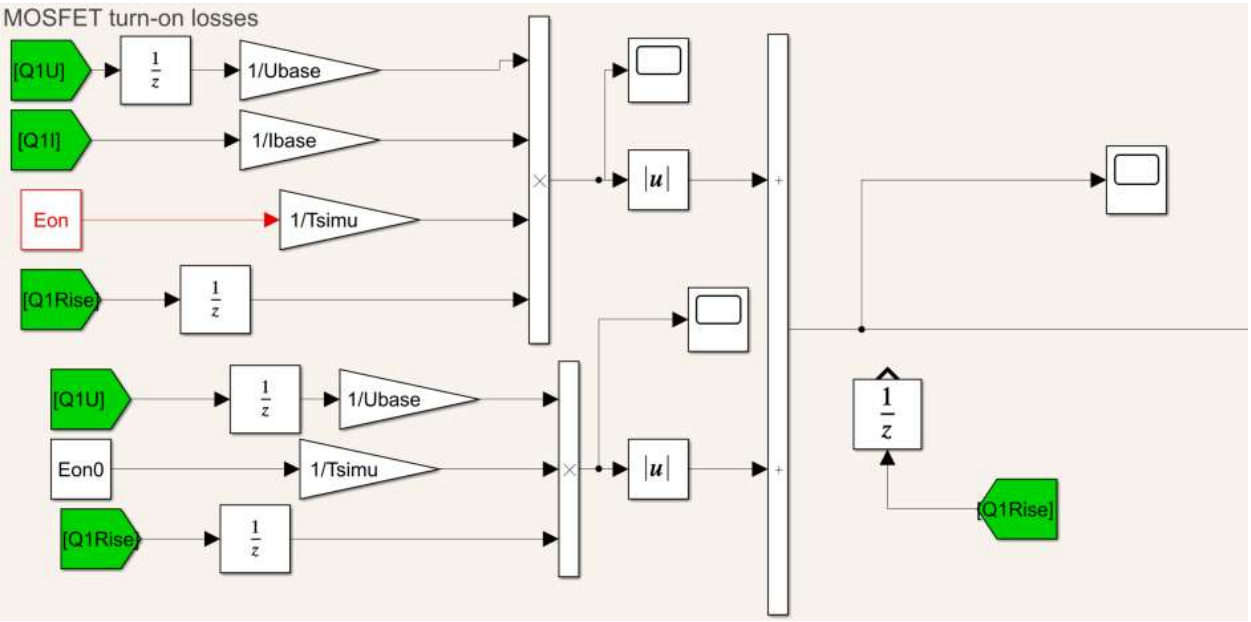

Figure 39 MOSFET Turn-On Losses Simulation Section

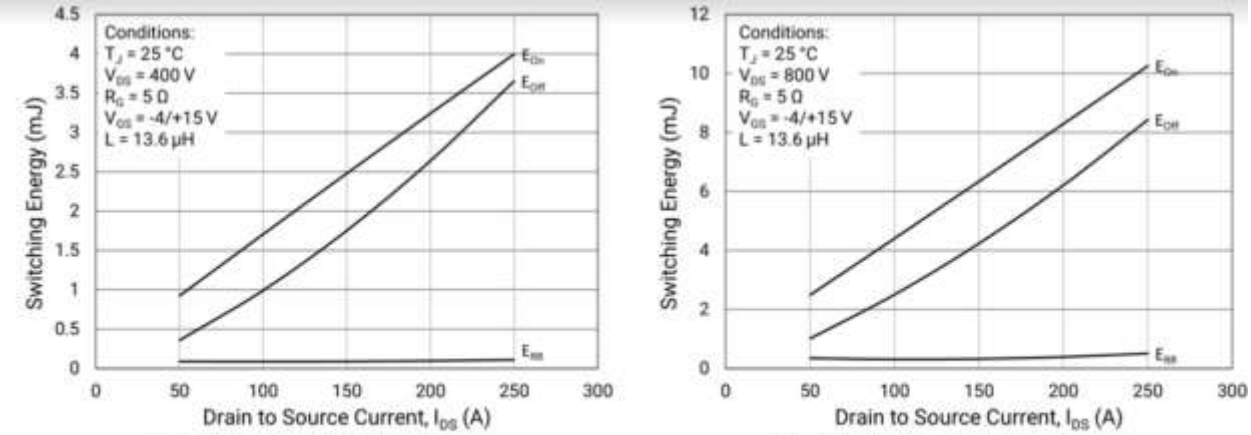

Fig 7. Inductive Switching Energy
T_J = 25 °C, V_{DS} = 400 V, R_G = 5 Ω

Fig 8. Inductive Switching Energy
T_J = 25 °C, V_{DS} = 800 V, R_G = 5 Ω

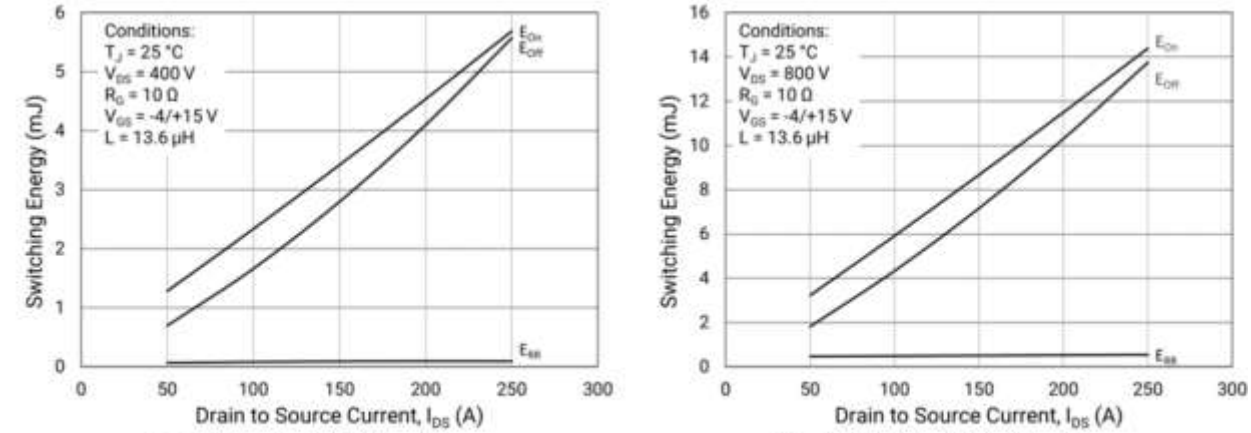

Fig 9. Inductive Switching Energy
T_J = 25 °C, V_{DS} = 400 V, R_G = 10 Ω

Fig 10. Inductive Switching Energy
T_J = 25 °C, V_{DS} = 800 V, R_G = 10 Ω

Figure 40 HT-4321 Eon & Eoff Switching Data

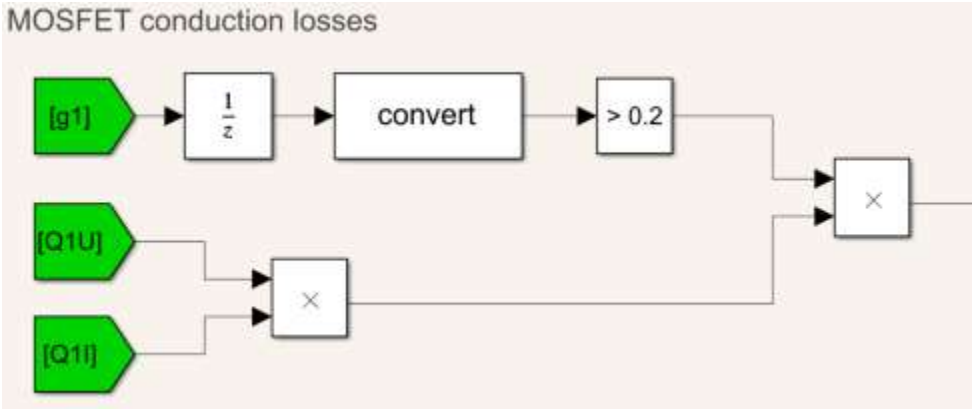

Figure 41 MOSFET Conduction Losses Simulation Section

The preceding section only considered one switch position, S1. The loss simulation procedure for S2 is identical to S1, but because the module under consideration is a half bridge module with two switch positions, the power maximum power rating is for the total module. Therefore, the losses obtained from the simulations for S1 and S2 must be added together. Simulation results are now presented.

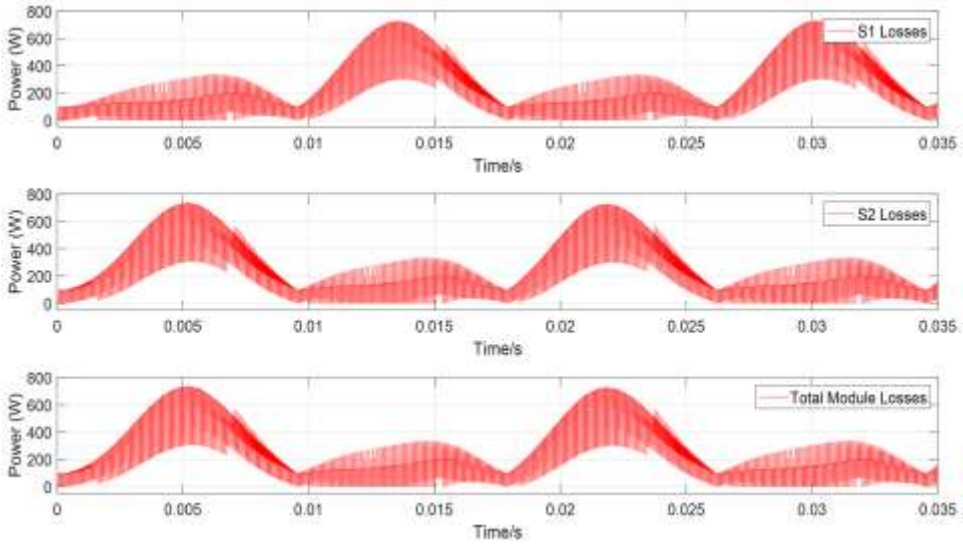

Figure 42 Single Pole Loss Simulation for Proposed HT-4321 2-Level Inverter with f_{sw} = 15 kHz

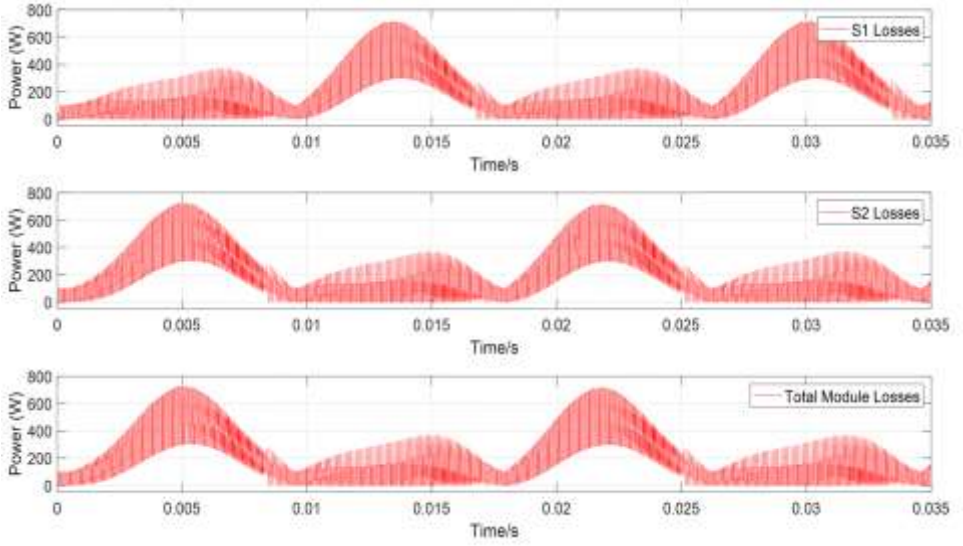

Figure 43 Single Pole Loss Simulation for Proposed HT-4321 2-Level Inverter with f_{sw} = 10 kHz

According to the power loss simulation that includes the switching data specific to the HT-4321 power module sample, under the full load of 150 kW with a power factor of 0.9 and utilizing SPWM, the module power dissipation average is 480 W if switching at 15 kHz and 380 W if switching at 10 kHz. These average values follow directly from calculating the average of the total module losses in Figures 42 and 43. When compared to the data collected during the thermal characterization of the system, it is clear that the power module meats the power dissipation requirements of the system at full load, however, to achieve 150 kW with 105°C coolant, the switching frequency must be decreased to 10 kHz. This follows from the predicted achievable module power dissipation being only 400 W at 105°C, while the calculated power dissipation for the system is 480 W at 15 kHz and 380 W at 10 kHz. Considering that the system is traction driven, 10 kHz or slightly below to allow a larger safety margin is still a reasonable switching frequency. Typical AC motors are operated with a switching frequency range of anywhere from 4-16 kHz.

Table 4 System Power Module Requirements and Realistic Power Module Capability

	System	Module Capability (W)						Module Capability (Predicted) (W)			
	Requirement (W)	T_L=25C	T_L=40C	T_L=47C	T_L=61C	T_L=70C	T_L=80C		T_L=90C	T_L=105C	
f_{sw} = 10 kHz	340	642.5	621.5	592.5	557.5	512.5	471.5		450	400	
f_{sw} = 15 kHz	440										
		Module Capability (Predicted) (W)									
				T_L=90C	T_L=105C						
				450	400						

It is worth noting that the actual system that the power module is used in should allow the module to handle more power because the cold plate that the module was characterized with has higher thermal impedance than the cold plate that the system was to be constructed with. With the anticipated system power module dissipation requirements, power module power dissipation

capability across different coolant temperatures, and overall system volume with the power module and cold plate selection in mind, the 1200 V HT-4321 module from Wolfspeed met all the requirements and thus was selected.

Figure 44 Wolfspeed HT-4000 Power Module

3.2 Cold Plate Selection

A cold plate build by Wieland Microcool was selected for the project. The cold plate is a channeled cold plate that offers very low thermal impedance without sacrificing much in terms of volume. It was custom made specifically for the HT-4000 series mounting footprint with the goal of being as compact as possible while still yielding high performance.

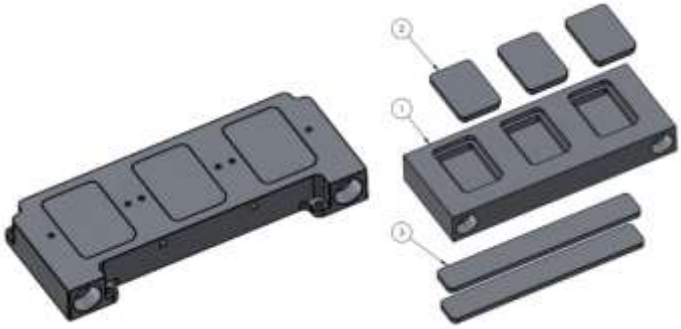

Figure 45 Microcool Custom Channeled Cold Plate for HT-4000 Series Power Modules

3.3 DC Link Capacitor Selection

The DC-link capacitors of an inverter typically account for a large amount of the volume in the system. To achieve high power density, special consideration was given to the selection of the capacitors. Although power density was the focus of the project, functionality was given top priority—the power density could be significantly increased if the DC-link were electrically undersized for the system, but the system would have no value because it would not be functional.

For a 2-level inverter, calculations for finding the electrical requirements of the DC-link capacitor(s) are straightforward and allow for some variability depending on user requirements. In practice, user requirements that directly affect the DC-link capacitance sizing are the allowable ripple voltage across the DC-link, the voltage of the DC-link, and the desirable dynamic response of the inverter. The minimum allowable DC-link capacitance can be calculated as

$$C_{link,\ min} \geq \frac{\Delta P_{max} \cdot T_d}{2 \cdot V_{dc} \cdot \Delta V_{dc}}, \tag{17}$$

where ΔP_{max} is the desired maximum change in output power, T_d is the number of switching cycles that the designer desires the ΔP_{max} to occur within, V_{dc} is the DC-link voltage, and ΔV_{dc} is the allowable voltage ripple on the DC-link. In this work, ΔP_{max} was set to change 20% within 10 switching cycles with an allowable voltage ripple of 15%. This means that the DC-link was chosen to allow the inverter to ramp up 20%, or 30 kW, within 10 switching cycles, or 70 μs.

In addition to maintaining the allowable ripple voltage in the system, the DC-link capacitors must be able to supply the required ripple current of the system under any rated loading condition. The RMS input current to the inverter is given by

$$I_{RMS} = \frac{I_M}{\sqrt{2}} \sqrt{\frac{2\sqrt{3}}{\pi} M \left(\frac{1}{4} + cos^2 \Phi\right)}, \tag{18}$$

where I_M is the magnitude of the phase current, M is the modulation index, and Φ is the lagging phase angle of the phase current. The DC component of the RMS input current to the inverter is given by

$$I_{AVG} = \frac{3}{4} I_M \, M \cos \Phi \, . \tag{19}$$

With the RMS and DC component of the input current known, the AC component of the inverter input current, or ripple current, with the given power factor and phase current is given by

$$I_{cap,\,RMS} = \sqrt{I_{RMS}^2 - I_{AVG}^2} \, . \tag{20}$$

Based on ΔP_{max} being set to 20% within 10 switching cycles, an allowable DC-link ripple of 15%, phase current of 260 amps, and power factor of 0.9, the DC-link capacitor must be at least 78µF and be rated to at least 85 amps RMS ripple current capacity.

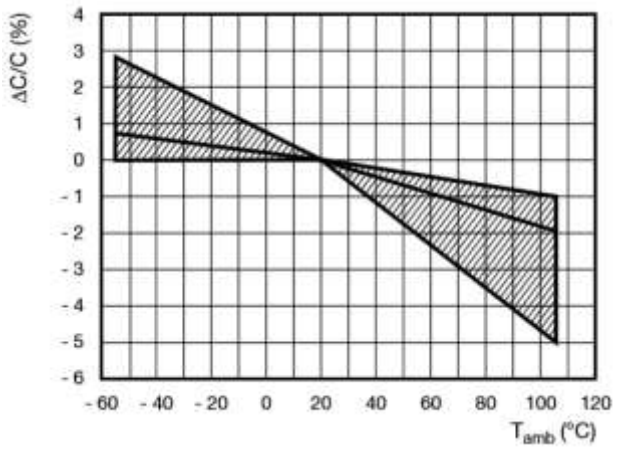

Figure 46 Capacitance vs Temperature for Vishay MKP Capacitors [14]

Moreover, given the target of 90°C-105°C operation, additional requirements must be met by the capacitor selection. The DC-link capacitor selection must be rated to withstand the DC bus voltage plus some safety margin of 20-30%, depending on the voltage overshoot experienced under switching. Generally, the voltage rating of power capacitors is significantly reduced as their

temperature increases. Additionally, the capacitance decreases as ambient temperature increases, as demonstrated by the capacitance vs. temperature plot of Vishay's MKP series capacitors.

Lastly, the reliability and safety of the capacitor selection was of interest because of the reliability requirements of traction applications. At the cost of power density, the decision was made to select a film capacitor over a ceramic capacitor because of the failure modes of the two technologies. Though ceramic capacitors are typically available with comparable electrical ratings to film caps but in significantly reduced package sizes, they are also known short circuit when they fail. On the other hand, film capacitors fail as an open circuit. A film capacitor short circuit across the DC-link of a traction inverter would pose a tremendous safety risk to the user while also taking the inverter offline. On the other hand, a failure of a film capacitor on the DC-link would only result in a slight decrease in the available capacitance connected across the DC-link and the system could continue to operate. Traction applications require high reliability, and as such, at the time of this project ceramic capacitors were not a practical choice even though using them would allow for higher power density.

With the reliability, overall system volume, capacitance rating, ripple current requirement, voltage rating at high temperature, and capacitance rating at high temperature in mind, an array of 8 Vishay MKP1848C61012JP4 capacitors in parallel was chosen as the DC-link capacitor. Each capacitor is rated for 1440 V at 70 °C, 850 V at 105 °C, 10 μF, and 11 $A_{RMS.}$ Combined, the capacitor array yields a total DC-link capacitance of 80 μF and ripple current capability of 88 $A_{RMS,}$ which satisfies the minimum electrical characteristics calculated using "worst case" parameters for ΔP, I_M, and T_d.

Figure 47 Vishay MKP1848C61012JP4 Capacitor

3.4 Gate Driver Selection

The gate driver controls the power module which is connected to a high power supply. The gate driver should be thoroughly tested before use in a live high power system. Aside from reliable operation, gate drivers should have several protections built in to prevent catastrophic failures. In this work, a custom PCB mounted gate driver for the Wolfspeed HT-4000 series was selected. The gate driver was a great option because it had all the necessary protections such as undervoltage lockout, reverse polarity, and fault indicators with lockout built in. As an added benefit, it has roughly the same size footprint as the HT-4000 power module.

Figure 48 Wolfspeed HT-4000 Series Gate Driver.

3.5 Bussing Design

The goal of the PCB design was to maximize electrical performance while minimizing system size. Being that the power module selection was designed to be mounted to a PCB, the bussing design for the system was flexible. This flexibility allowed for minimizing the size that the bussing added to the system as well as distances between the system components, which helped minimize electrical parasitics. To achieve the size and performance goals, all components were modeled in SolidWorks and arranged in the most compact fashion possible. Making use of the PCB layout flexibility, the decision was made to rout all power connections away from the connectors to the cold plate to minimize any risks of the power terminals becoming wet in the event that the piping to the cold plate developed a leak. Following the arrangement of the components, a PCB outline was drawn around the arrangement of the components.

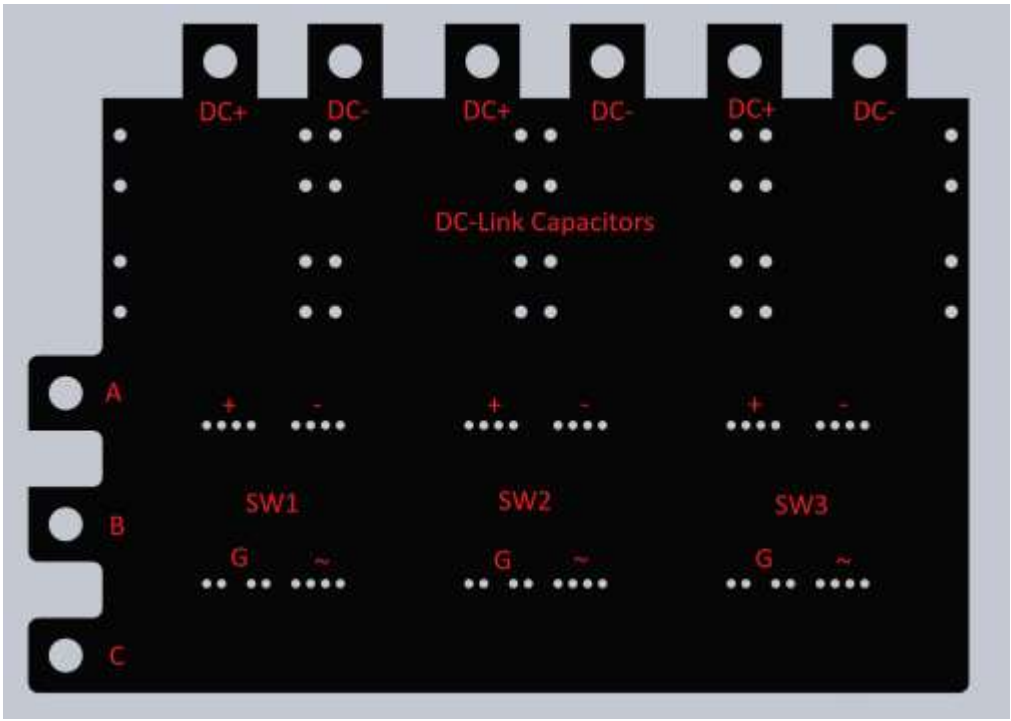

Figure 49 Desired PCB Outline to Minimize System Volume

After the desired PCB outline was drawn, the location of each electrical connection given the physical location of each device was noted. From Figure 49 each component's position and electrical connections may be deduced. With the HT-4000 module, added convenience is given to the user because the DC connections are on one side of the module while the midpoint of the half-bridge is on the other side of the module.

Next, the board outline was imported into Allegro PCB Editor to route the traces. In designing the inner workings of the PCB, the goals were reliability and electrical performance. Regarding reliability, special attention has to be given to the trace width and copper weight when dealing with systems that may carry large currents. If the traces in a PCB are not sufficiently wide or the copper is not thick enough, the current carrying copper in the PCB will reach its glass transition temperature—typically rated around 175°C—and begin to delaminate, causing the PCB to come apart and fail. Apart from that, attention must be given to the spacing between the different traces within a PCB because different voltage potential traces within a PCB can arc inside the PCB, causing catastrophic failure. Generally, the spacing between the external layers of a PCB require greater spacing than the internal layers.

Both the copper width/weight and trace spacing in PCBs have industry recommended specifications according to IPC-2221A and IPC-2221B. IPC-221A outlines the minimum copper weight and thickness required for a given current level and desired temperature rise to avoid overheating the PCB and IPC-2221B outlines the minimum clearance between different PCB traces to avoid short circuits between traces. Several online calculators that simplify the calculation of copper weight, trace width, and trace spacing by pulling data from IPC-2221A and IPC-2221B exist and simplify the application of the standards.

Parasitic inductance minimization with even current density between phases was the top priority in the layout aside from following the listed IPC standards. To minimize the parasitic inductance and make the current density throughout the bussing as even as possible, several simulations using Ansys were conducted to optimize the location and number of DC power terminals to the inverter, orientation of the DC-link capacitors, and shape of the DC traces. Ansys was especially useful for extracting the DC current density of the inverter bussing. The DC-link bussing was made as wide as possible to minimize its inductance as much as possible.

Regarding the PCB performance in the inverter system, it is very advantageous to have the least inductance possible in the power loop, which consists of the DC supply, bussing, power module, and DC-link caps. Excessive inductance in the power loop can lead to voltage ringing, instability, large amounts of EMI, and excessive voltage and current overshoots—all of which can destroy system components, the most vulnerable generally being the power module. Balanced impedance from the input to each power module is also important because if the impedance from the input to each module is significantly different, the loop inductance to each module will be different, which will result in dissimilar switching performance between different phases of the inverter. To help minimize the power loop inductance, the DC-link bussing was split into four layers, consisting of alternating identical positive and negative layers, as shown by the PCB stack up in the top of Figure 52. In addition, the DC-link bussing was made as wide as possible to minimize its inductance as much as possible.

A current density simulation in Ansys of an early proposed PCB design for this project, presented in Figure 50, demonstrates the impedance balance between each phase.

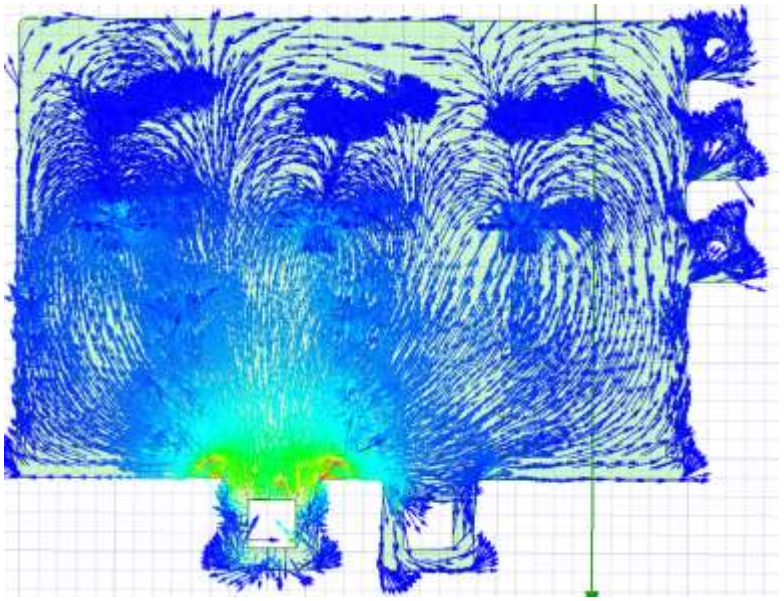

Figure 50 Current Distribution of 2-Terminal Design

From the simulation, it is very evident that with a two DC terminal design, the impedance from the input to each power module was very imbalanced, resulting in more current sinking to the power module on the left than any other devices. Furthermore, the current at the single input tab resulted in a current density above 35A/mm^2, which exceeds the maximum safe current density for a PCB. Together, those facts pointed toward a multiple input tab design. Contrary to the two-terminal design, the 6 terminal design, shown in Figure 51, exhibits relatively even current distribution from the DC+ tabs to the drain of the high side position of each power module—especially considering that there are several holes in the DC plane because of the capacitor array.

Also clear from the simulation presented in Figure 51 is that the DC current distribution does not cross the midpoint of the modules, above the middle output tab of the inverter. This means the space above the midpoint of the modules is essentially wasted space. Recalling that the this was the desired board outline if all connections could be made and the IPC standards could be

satisfied, the AC traces were routed in the leftover space above the midpoint of the power modules as shown in the final layout, presented in Figure 52.

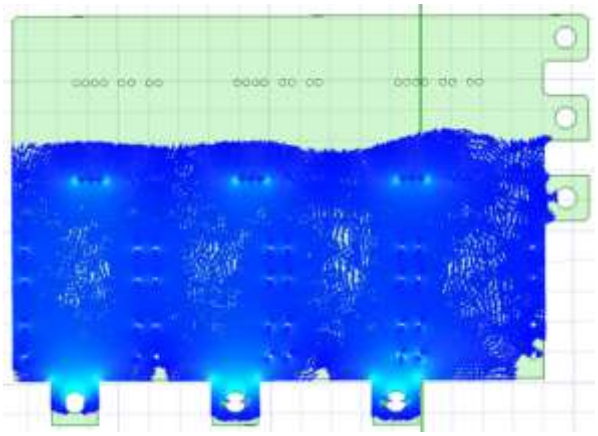

Figure 51 Current Distribution Simulation of Multiple Tab Design (DC+ Layer)

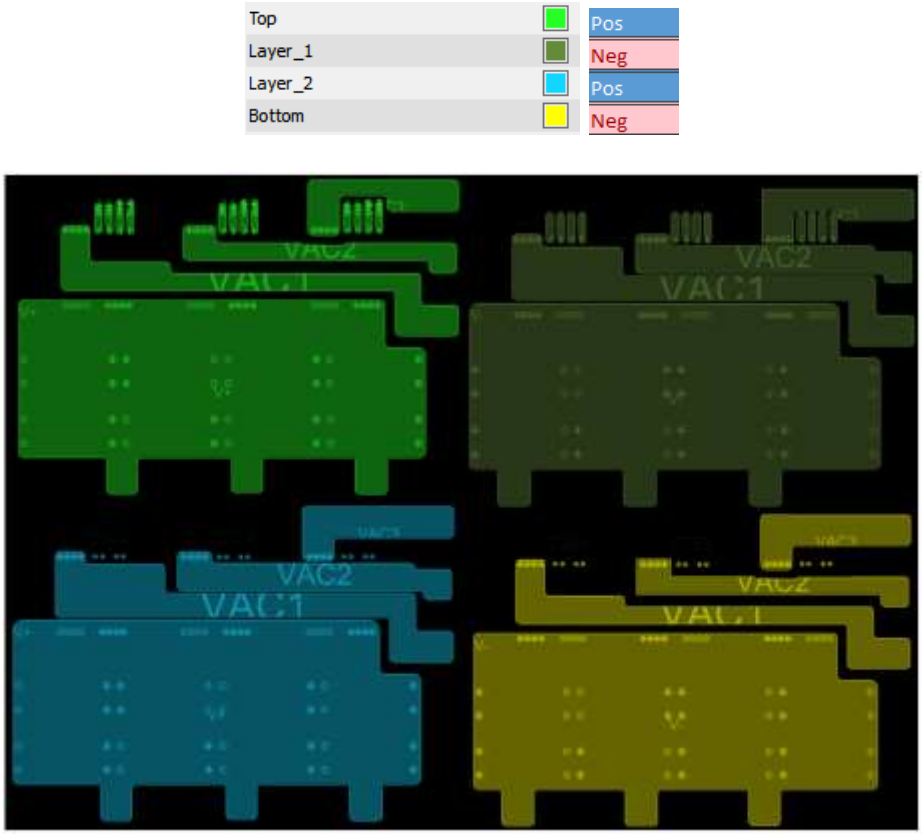

Figure 52 Inverter Final PCB Layout

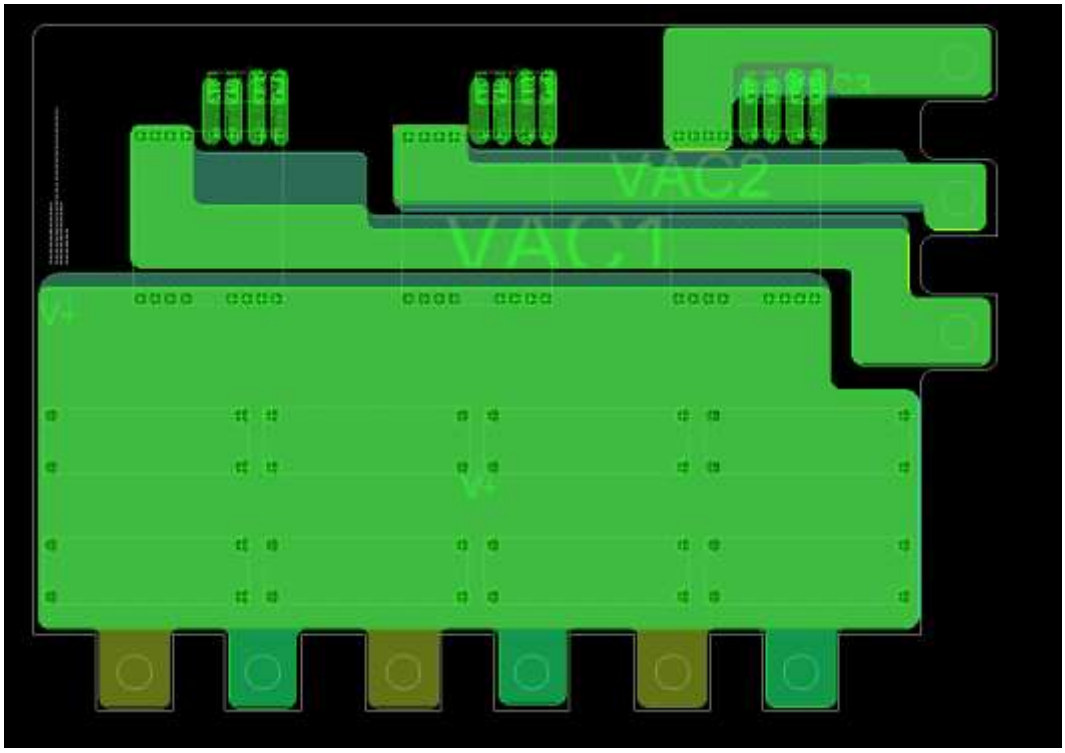

Figure 53 Inverter Final PCB Layout

Based on the IPC-2221A and IPC-2221B standards, 200 amps with a realistic ambient temperature of 32°C (90°F), an allowable PCB temperature rise to 175°C, and 4 oz. copper, the minimum copper trace width was calculated as 51.3 mm. The required spacing between the high voltage traces to achieve electrical insulation up to 1000V is 1.5 mm for internal PCB layers and 2.33 mm for coated external PCB layers. The PCB was designed using these parameters. The 51.3mm minimum trace width was divided by four and split between the four layers to avoid increasing the size of the PCB past the edges of the cold plate which would result in an increase in size for the overall system.

3.6 System Assembly

The proposed system which consists of the selected components, being the Wolfspeed HT-4000 modules and their gate drivers, 8 Vishay MKP1848C61012JP4 capacitors, the custom

Microcool cold plate, and the PCB was modeled to assemble as shown below. The overall system dimensions are 6.88” × 4.80” × 2.49,” for a total volume of 1.35 L, yielding an overall maximum power density of 111 kW/L.

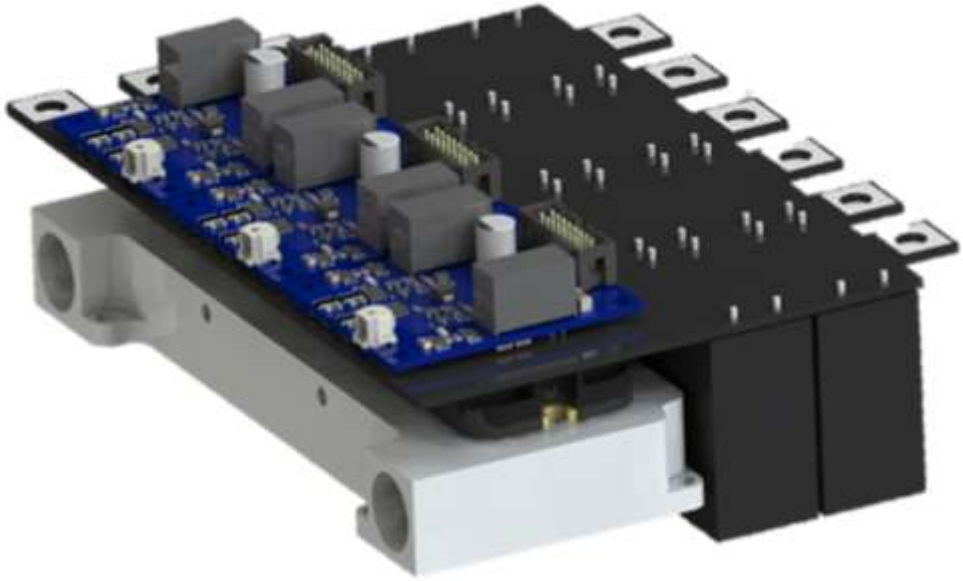

Figure 55 Final Inverter System Design

Figure 54 Final Inverter System Design (Exploded)

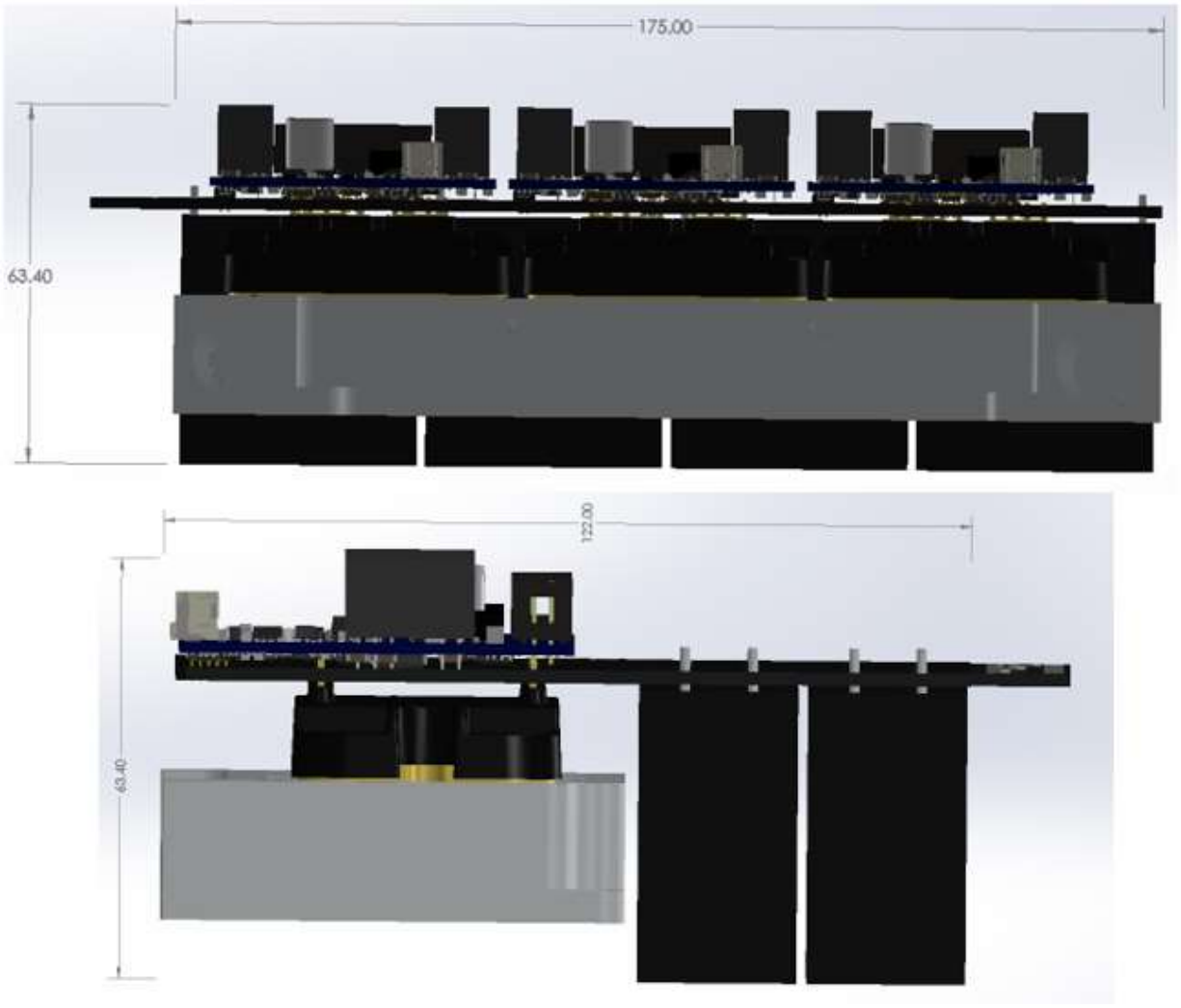

Figure 56 System Dimensions

3.7 Controller Hardware Design

To add further value to the project as a whole and make it more of a standalone unit, a custom controller for the inverter was designed, constructed, and tested. The main objectives of the controller included interfacing the with three gate drivers and enabling control of an AC motor. To adequately control an AC motor, the instantaneous phase currents must be known, and if the motor is a permanent magnet AC motor (PMAC), the instantaneous rotor position must also be known. PMAC motors are commonplace in traction applications because they may achieve higher

power density than traditional induction motors. To achieve these goals, at minimum the control board was required to provide the required signals for each of the 3 gate drivers, listed in the gate driver datasheet and shown in Figure 57, and read the output signals from the current sensors used to monitor the output phase currents.

Input Connector Information

Pin Number	Name	Description
1	VDC	Power Supply Input Pin
2	Common	Common
3	HS-P (*)	Positive Line of 5 V Differential High Side PWM Signal Pair. Terminated Into 250 Ω.
4	HS-N (*)	Negative Line of 5 V Differential High Side PWM Signal Pair. Terminated Into 250 Ω.
5	LS-P (*)	Positive Line of 5 V Differential Low Side PWM Signal Pair. Terminated Into 250 Ω.
6	LS-N (*)	Negative Line of 5 V Differential Low Side PWM Signal Pair. Terminated Into 250 Ω.
7	$\overline{\text{FAULT}}$ - P (*)	Positive Line of 5 V Differential Fault Condition Signal Pair. Drive Strength 20 mA.
8	$\overline{\text{FAULT}}$ - N (*)	Negative Line of 5 V Differential Fault Condition Signal Pair. Drive Strength 20 mA.
9	RTD-P (*)	Positive Line of 5 V Temperature Dependent Resistor Output Signal Pair. Drive Strength 20 mA. Temperature Measurement is Encoded Via PWM.
10	RTD-N (*)	Negative Line of 5 V Temperature Dependent Resistor Output Signal Pair. Drive Strength 20mA. Temperature Measurement is Encoded Via PWM.
11	$\overline{\text{PS-Dis}}$	Pull Down to Disable Power Supply. Pull Up, or Leave Floating to Enable. Gate-Source will be Connected with 10 kΩ when disabled.
12	Common	Common
13	PWM-EN	Pull Down to Disable PWM Input Logic. Pull Up/Leave floating to enable. Gate-source will be held low through gate resistor if power supplies are enabled.
14	Common	Common
15	OC-EN	Over-current Protection Enable. Pull down to disable detection of over-current fault. PWM and UVLO will continue to function. Pull up or leave floating to enable detection of over-current fault.
16	Common	Common

Figure 57 HT-4000 Gate Driver Signals

To accomplish standalone functionality, the controller needed to be powered directly from the high-voltage DC-bus, provide power to all the controller circuitry, and provide power to the gate drivers. Without the ability to be powered from the DC-bus, the controller would require a separate low voltage DC supply, which may be undesirable in some applications. In addition to the minimum features, it was highly desirable for the controller to be able to function with a wide

range of analog and digital hardware enhance the adaptability. The minimum number required by the proposed system which requires two three analog input channels to read the signals from the current sensors and where each of the three gate drivers requires two PWM channels, one I/O for the fault signal, one I/O for the RTD, one I/O for the power supply disable, one I/O for the over current protection. Additional desirable features included bipolar wide range voltage reading, LED outputs, and CAN interfacing ability.

The Texas Instruments (TI) 28379D control card was chosen as the basis of the controller based on ease of use and performance. This control card is a high component density layout board that is built around the dual core 200 MHz TMS320C28x DSP from TI. The board enables rapid prototyping by preconfiguring and making the most used features—ADC, DAC, PWM, and GPIOs—of the DSP core easily accessible to the end user.

Figure 58 Texas Instruments 28379D Control Card

Major sections of the controller schematic are presented and described as follows.

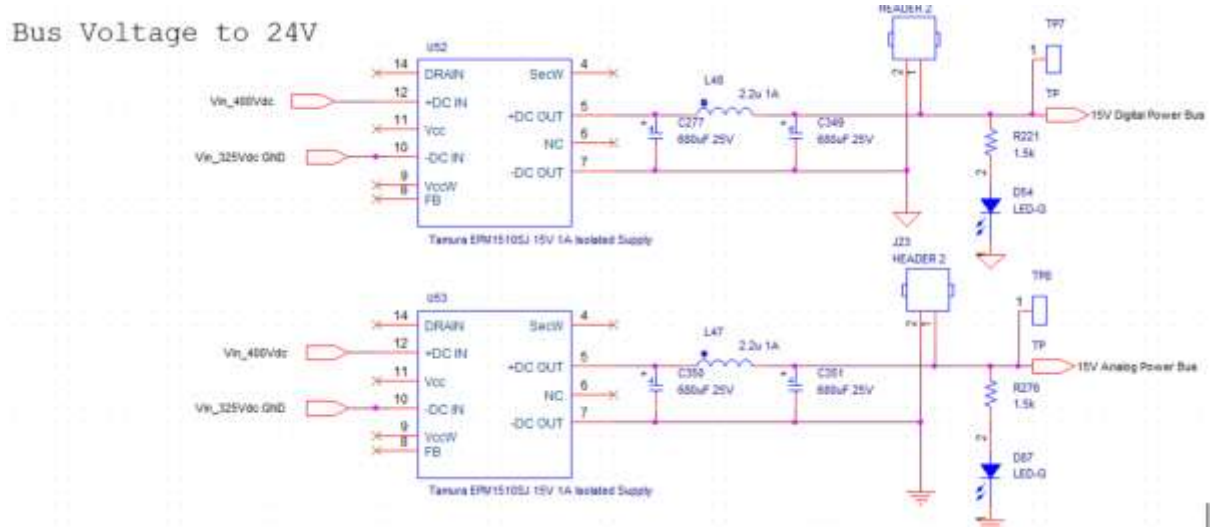

Figure 59 Bus Voltage to Low Voltage Conversion

Following power entry through a PCB-mounted terminal block connector, the high-voltage DC link is routed to two DC-DC converters which step the voltage down to two separately grounded 15 V buses, which serve power to the rest of the board. Both converters are isolated, which serves as a protection but more importantly isolates the analog and digital signals grounding loops from each other. Keeping the analog and digital ground return paths separate from each other in a mixed-signal PCB helps prevent the high-frequency digital signals from polluting the sensitive low-frequency analog signals which are generally produced with the intent to be read with high accuracy. If the grounds are not kept separate, the high frequency switching of the digital circuitry—in this case, 6 pairs of differential 15 kHz PWM signals—will occur on the same ground plane that the ADC uses to reference its readings, resulting in inaccurate analog signal samples. Throughout the rest of the schematic, the analog signals are referenced to the analog ground plane and the digital signals are referenced to the digital ground plane. Observing best PCB design practices, the grounds are only connected inside the ADC of the DSP itself. The 15 V buses created by the high-voltage DC-DC converters are connected to four power supplies which create the

commonly used 5 V and 3.3 V references throughout schematic. Two of the power supplies create the references to the digital ground plane while two of the power supplies reference the analog ground plane.

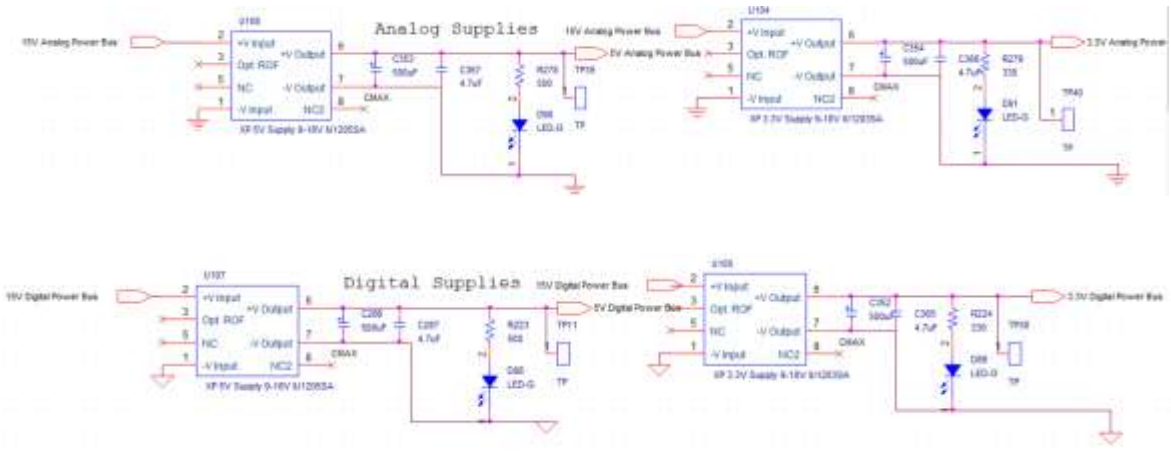

Figure 60 Digital and Analog 5 V and 3.3 V Bus Creation

The selected 28379D control card operates at 3.3 V logic, while the HT-4000 gate drivers require differential ±5 V signals. To make the two compatible with each other, a 3.3 V to 5 V bidirectional level shifter and a differential driver/receiver was placed between each gate driver and the DSP. With regard to the output signals of the DSP that are sent to the gate drivers, the use of these two components first changes the level of the 0 to 3.3 V single ended signals to 0 to 5 V signals and then converts the 0 to 5 V single ended signals to ±5 V differential signals. With regard to the differential status signals that the gate driver generates and sends back to the controller, the signal flow works in reverse, resulting in a single ended signal being sent to the DSP.

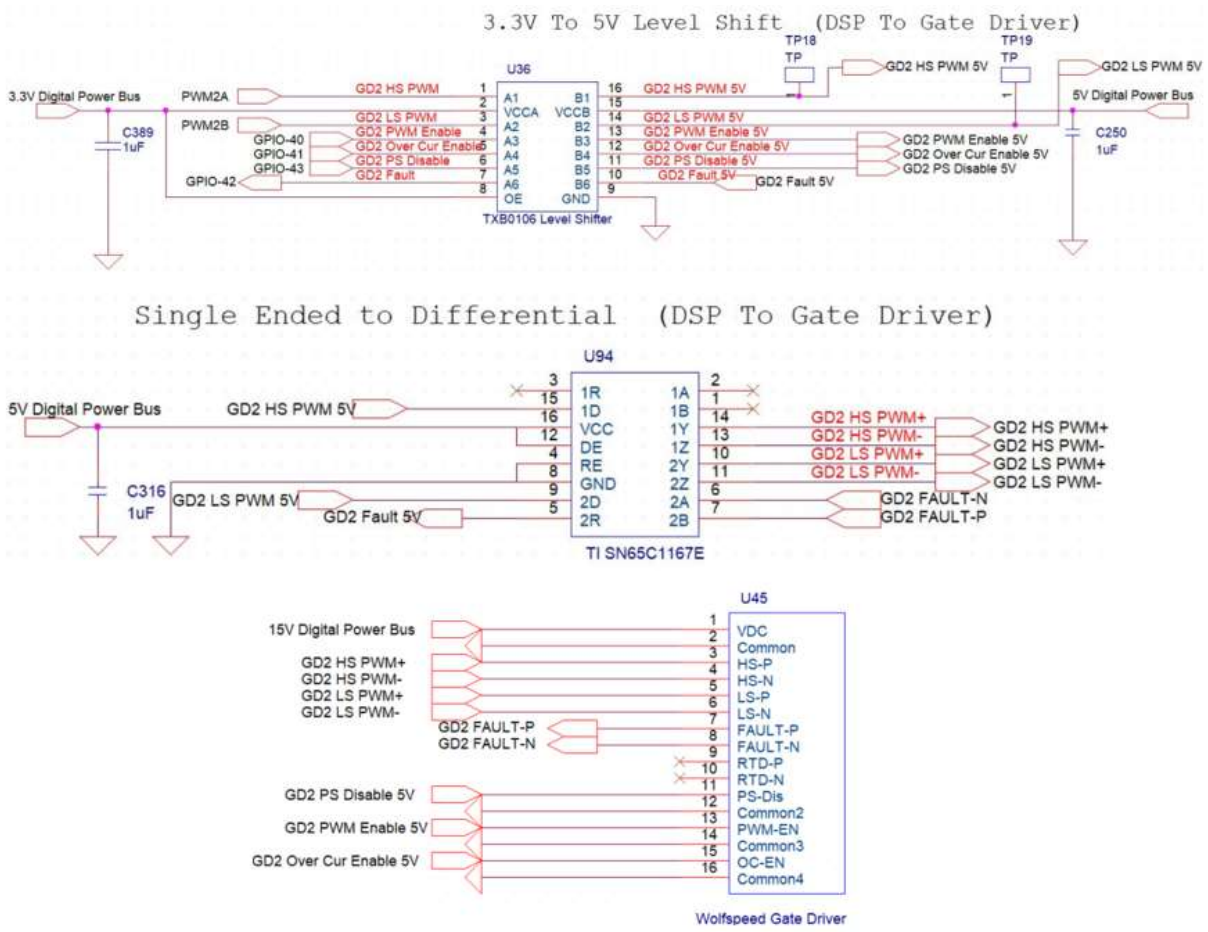

Figure 61 DSP to Gate Driver Interface Stage

12 low pass filtering circuits were included in the controller design to allow the DSP to sample analog 0 to 5 V unipolar signals. The circuit uses a 5 V OPA4322 op amp and the low pass filter topology to apply a low pass filter to the sampled signal before its 0 ~ 5 V output is changed to a 0 ~ 3.3 V output with a resister divider. For the 28379 to correctly read a signal that ranges outside of 0 V to 3.3 V, the signal must be level shifted prior to reaching the ADC of the DSP.

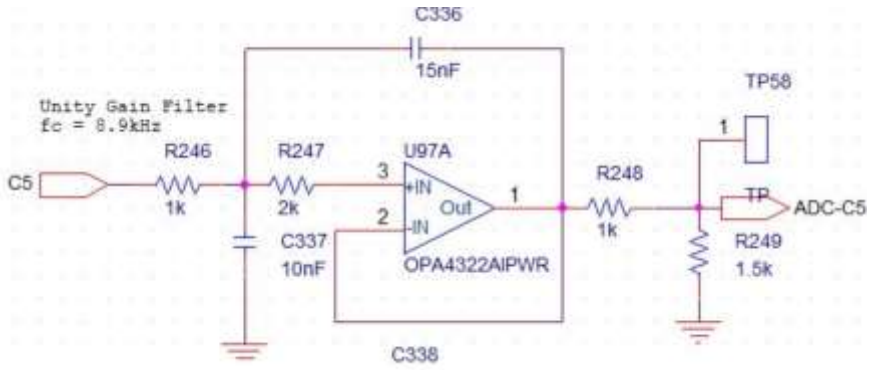

Figure 62 Low Pass Filtering and Level Shifting

Six of the depicted differential amplifiers circuits were placed on the controller layout to allow the controller to read bipolar analog signals ranging from -10 V to +10 V.

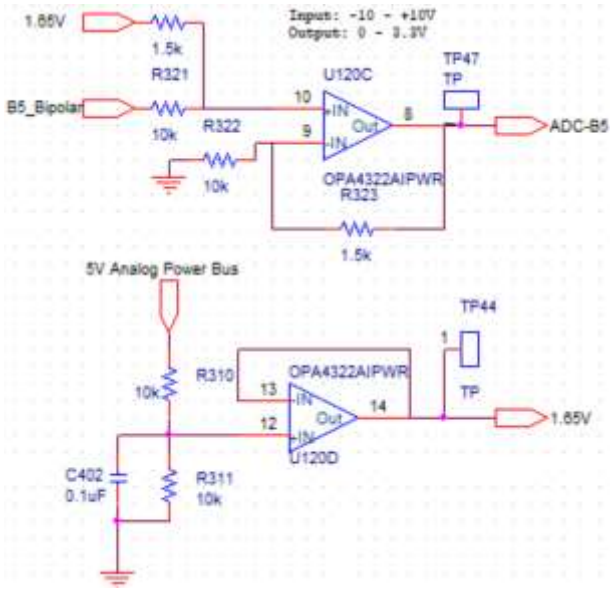

Figure 63 Differential Amplifier

An isolated CAN interface was included on the board to allow the controller to communicate with other control units using a standard protocol.

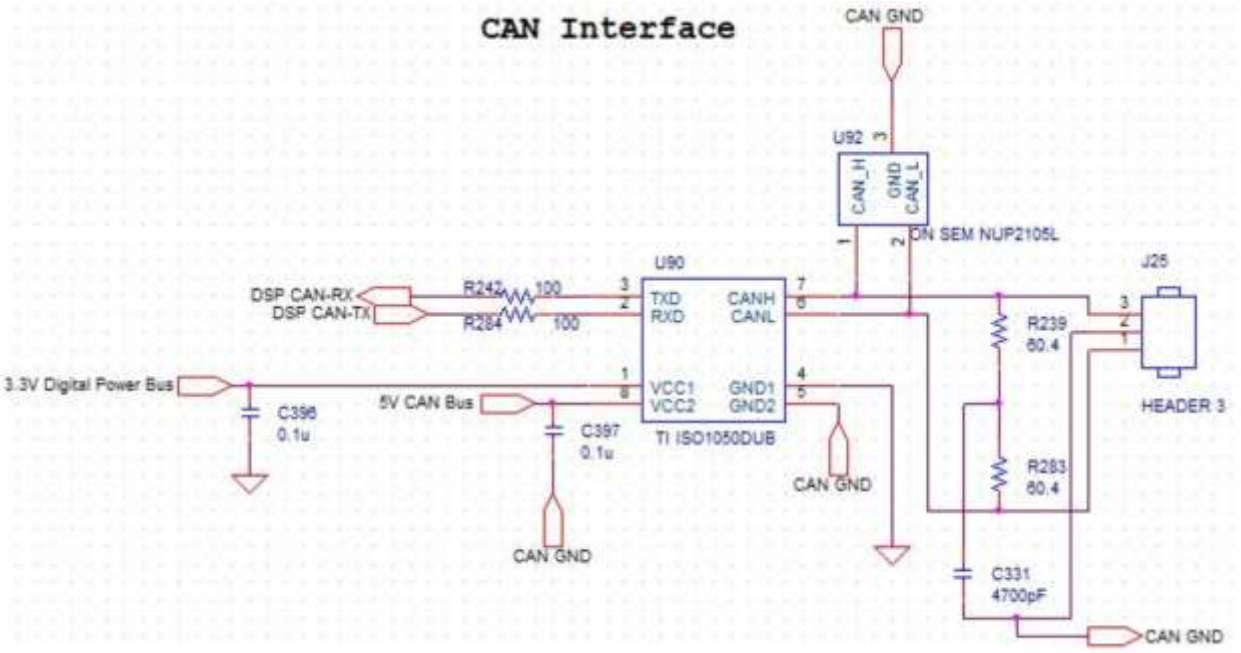

Figure 64 CAN Interface

Aside from meeting functionality requirements, the controller was designed to fit onto the power conversion unit without increasing its overall volume by fitting into space that was previously unoccupied in the system.

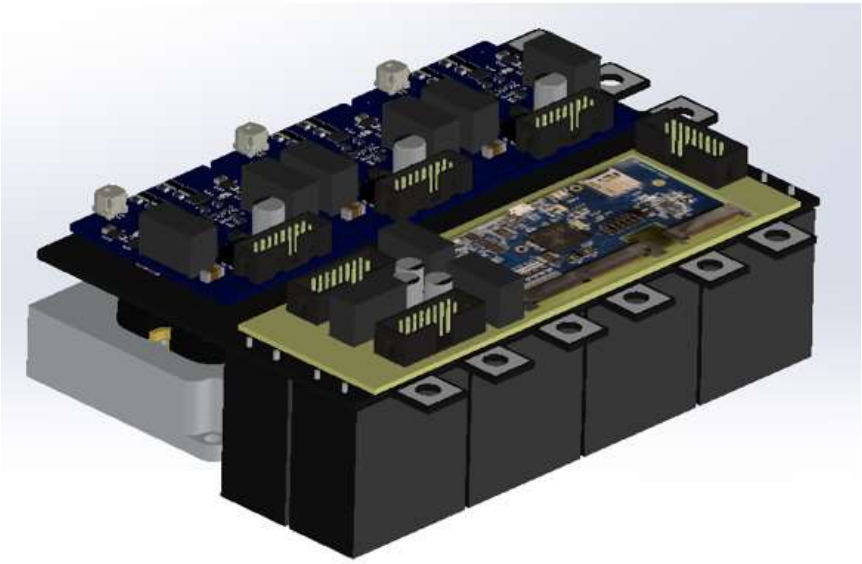

Figure 65 Initial System Design with Placement and Targeted Dimensions of Controller

3.8 Controller Assembly

Two layouts of the controller design were fabricated—the first for ease of debugging and the second specifically for fitting into the overall system as designed

Figure 66 Controller Layout V1 Top View

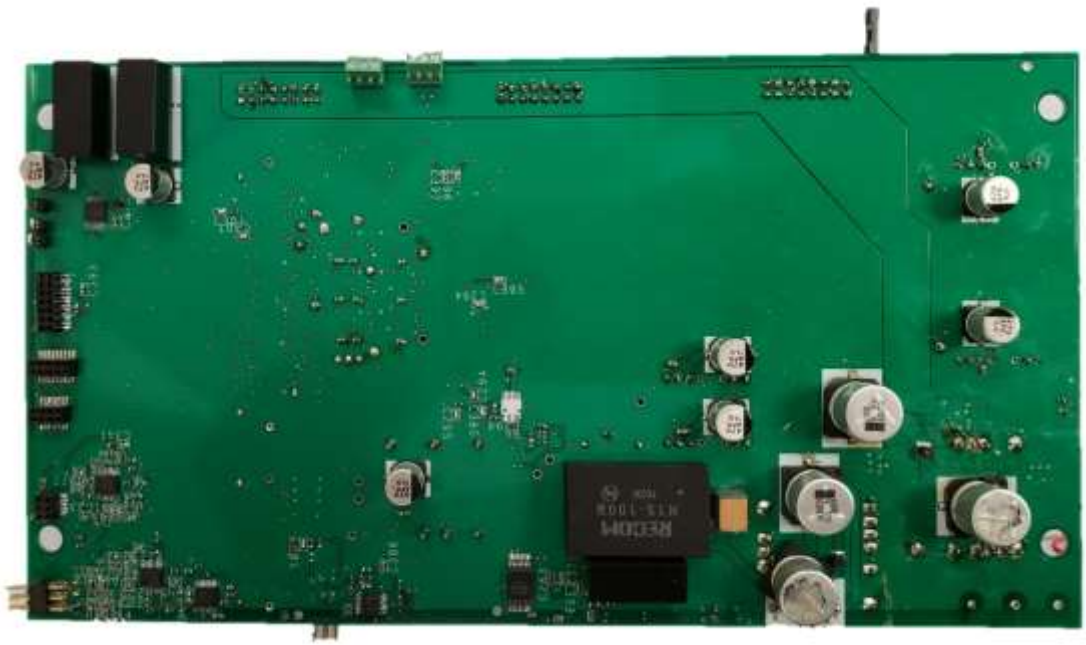

Figure 67 Controller Layout V1 Bottom View

Figure 68 Controller Layout V2 Top View

Figure 69 Controller Layout V2 Bottom View

3.9 References

[1] DETERMINING ELECTRIC MOTOR LOAD AND EFFICIENCY. (n.d.). [ebook] U.S. Department of Energy. Available at: https://www.energy.gov/sites/prod/files/2014/04/f15/10097517.pdf [Accessed 26 Feb. 2019].

[2] Glampe, M. (2019). VFD switching frequency and its affects on distortion and output. [online] KEB America. Available at: https://kebblog.com/vfd-switching-frequency/ [Accessed 30 Nov. 2019].

[3] Gurpinar, E. and Ozpineci, B. (2019). Loss Analysis and Mapping of a SiC MOSFET Based Segmented Two-Level Three-Phase Inverter for EV Traction Systems. [online] Oak Ridge: U.S. Department of Energy Office of Scientific and Technical Information. Available at: https://www.osti.gov/biblio/1474641 [Accessed 18 Dec. 2018].

[4] Lytron.com. (2019). Designing Custom Cold Plates. [online] Available at: https://www.lytron.com/product-support/resource.cfm?aid=1262 [Accessed 22 Feb. 2019].

[5] Vujacic, Marija & Hammami, Manel & Srndović, Milan & Grandi, Gabriele. (2018). Analysis of dc-Link Voltage Switching Ripple in Three-Phase PWM Inverters. Energies. 11. 471. 10.3390/en11020471.

[6] W. Mazgaj, B. Rozegna and Z. Szular, SWITCHING LOSSES IN THREE-PHASE VOLTAGE SOURCE INVERTERS. Kraków, Poland: Cracow University of Technology, 2015.

[7] "Design Considerations for Designing with Cree SiC Modules Part 1. Understanding the Effects of Parasitic Inductance", 2019. [Online]. Available: https://www.wolfspeed.com/downloads/dl/file/id/180/product/0/design_considerations_for_designing_with_cree_sic_modules_part_1_understanding_the_effects_of_parasitic_inductance.pdf. [Accessed: 19- May- 2019]

[8] "Design Considerations for Designing with Cree SiC Modules Part 2. Techniques for Minimizing Parasitic Inductance", 2019. [Online]. Available: https://www.wolfspeed.com/downloads/dl/file/id/181/product/0/design_considerations_for_designing_with_cree_sic_modules_part_2_techniques_for_minimizing_parasitic_inductance.pdf. [Accessed: 19- May- 2019]

[9] Notes for PrimePACKTM Modules. Neubiberg, Germany: Infineon, 2015 [Online]. Available: https://www.infineon.com/dgdl/Infineon-Application_and_Assembly_Notes_PrimePACK_Modules-ApplicationNotes-v02_00-EN.pdf?fileId=db3a30431375fb1a011376a24657002d. [Accessed: 12- Jan- 2019]

[10] Thermal design and temperature ratings of IGBT modules. Lenzburg, Switzerland: ABB [Online]. Available: https://library.e.abb.com/public/d2e8a4289f27490f8469527bf6c1f1ab/Thermal%20design%20and%20temperature%20_5SYA%202093.NewLay.pdf. [Accessed: 12- Jan- 2019]

[11] A. Wintrinch, Thermal design and temperature ratings of IGBT modules. Lenzburg, Switzerland: ABB [Online]. Available: https://library.e.abb.com/public/d2e8a4289f27490f8469527bf6c1f1ab/Thermal%20design%20and%20temperature%20_5SYA%202093.NewLay.pdf. [Accessed: 12- Jan- 2019]. Nuremberg, Germay: Semikron, 2014 [Online].

[12] S. Pithadia and S. More, Grounding in mixed-signal systems demystified, Part 1. Dallas: Texas Instruments, 2013 [Online]. Available: http://www.ti.com/lit/an/slyt499/slyt499.pdf. [Accessed: 10- Mar- 2019]

[13] S. Pithadia and S. More, Grounding in mixed-signal systems demystified, Part 2. Dallas: Texas Instruments, 2013 [Online]. Available: http://www.ti.com/lit/an/slyt512/slyt512.pdf. [Accessed: 10- Mar- 2019]

[14] Metallized Polypropylene Film Capacitor DC-Link Capacitor. Vishay, 2017 [Online]. Available: http://www.vishay.com/docs/26015/mkp1848cdclink.pdf. [Accessed: 07- May- 2019]

[15] HT-4321 High Performance Silicon Half-Bridge Power Module. Durham: Cree.

[16] A. D. Callegaro et al., "Bus Bar Design for High-Power Inverters," in IEEE Transactions on Power Electronics, vol. 33, no. 3, pp. 2354-2367, March 2018.

CHAPTER 4

Experimental Studies and Performance Verification

4.1 Complete System Assembly

All components were assembled into the system, which is presented below. The complete converter had a volume of 1.35 L, as expected.

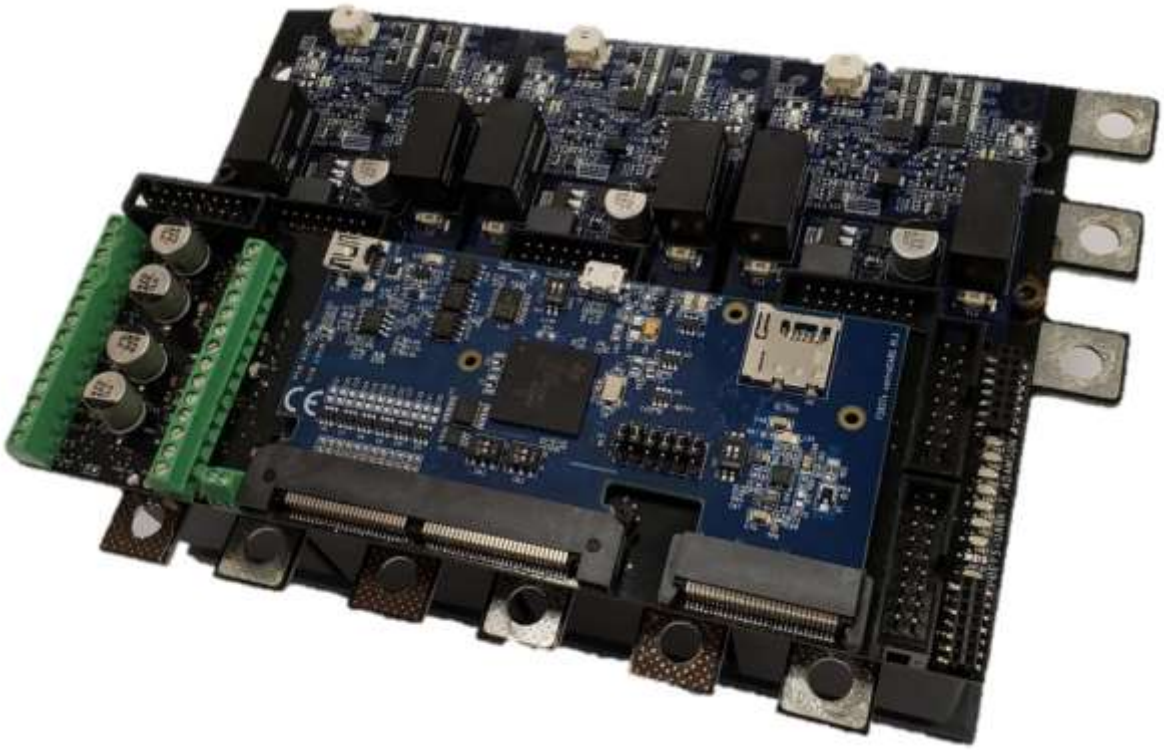

Figure 70 Complete 150 kW DC-AC Power Conversion System

Figure 71 150 kW Power Conversion Unit at POETS Poster Presentation

4.2 Test Setup for Controller Performance Validation

The controller was assembled and tested on a bench top dynamometer that had a PMAC and DC motor coupled to each other. The controller was programmed using Simulink embedded coder and successfully demonstrated the ability to maintain closed loop speed control on either motor while the other motor was operated as a generator.

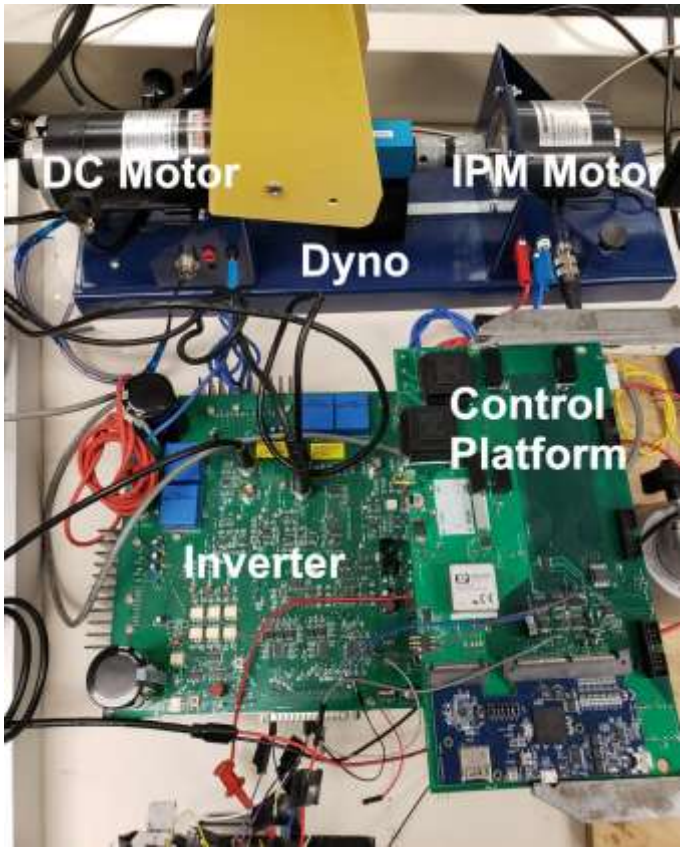

Figure 72 Controller Verification Test Setup

4.3 Inverter Electrical Performance Results

Following assembly, the parasitic inductance of the power loop—from the midpoint of the power module to the drain of the high-side MOSFET—was measured for each of the 3 phases using a Keysight E4990 impedance analyzer. Each phase's inductance measured in the range of 6.8 nH to 7.0 nH, which is a relatively low value that should yield good switching performance.

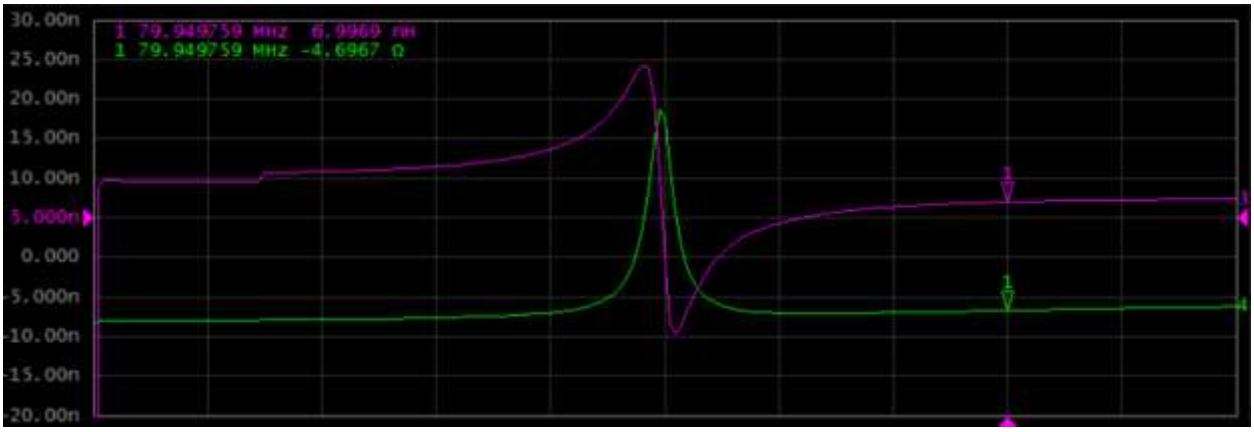

Figure 73 Single Phase of Inverter Measured Impedance Plot

Prior to 3-phase testing, double pulse testing with an 800V DC-link and the module rated current of 264 amps was completed on each of the inverter's three phases. As predicted by the relatively symmetrical phase impedance simulation in Ansys and very similar phase impedance measurements, the switching results of each phase were nearly identical, as shown below in the full current and voltage double pulse results from each phase. Because of its rapid prototyping capability, flexibility, and ability to monitor internal signals using Control Desk, a dSPACE Microlabox was used to control the inverter during initial testing. The double pulse test results also demonstrate that the inverter's switching overshoot voltage at full power is less than 900 V, which means the inverter could be operated with a higher DC-link voltage if desired, leading to even higher power output capability without destroying the 1.2 kV rated power modules.

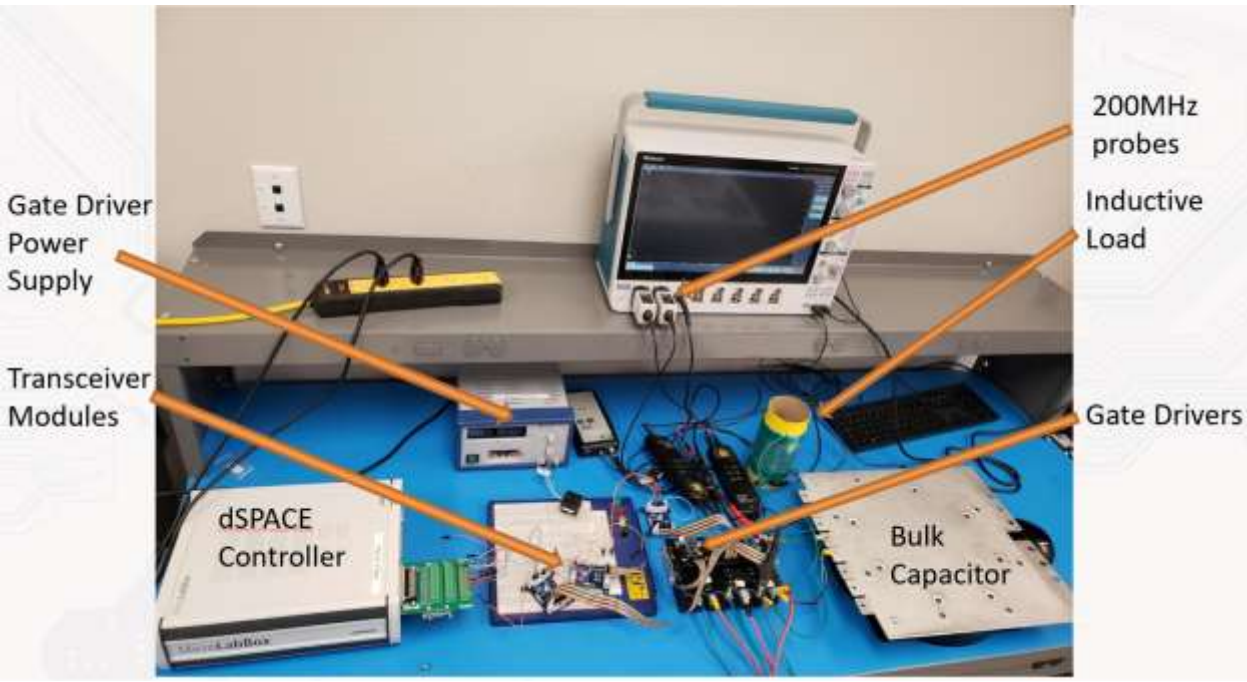

Figure 74 Double Pulse Test Setup

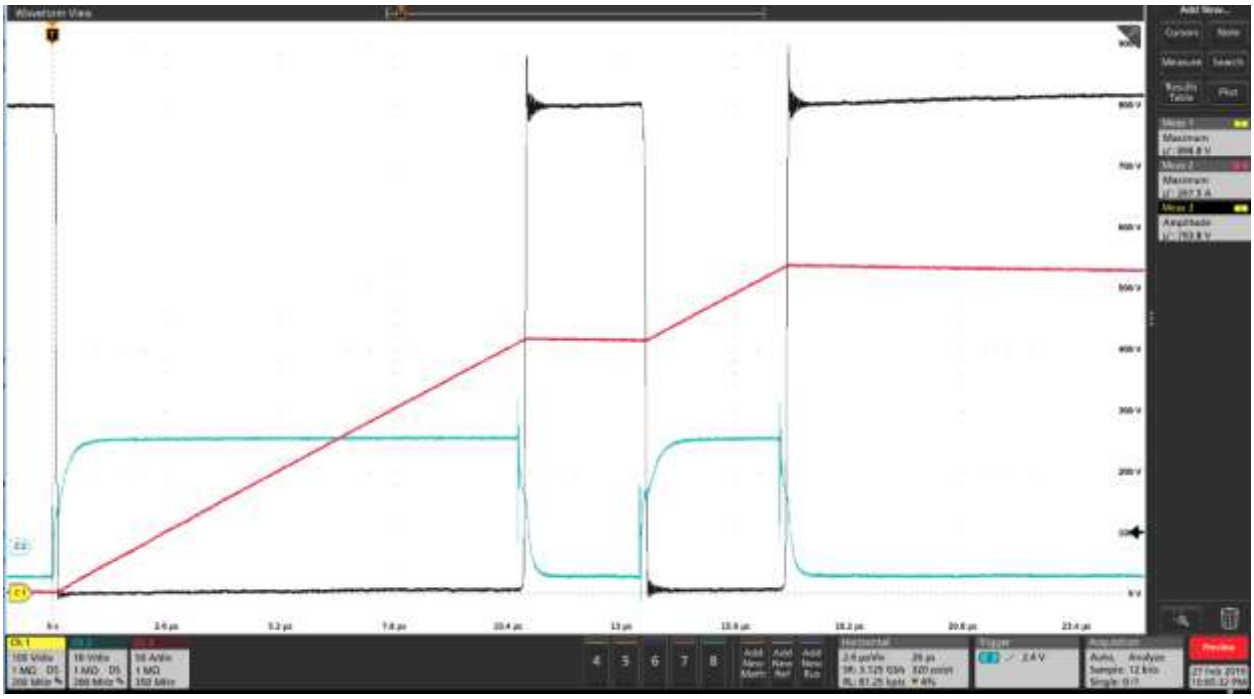

Figure 75 Phase A Double Pulse Test

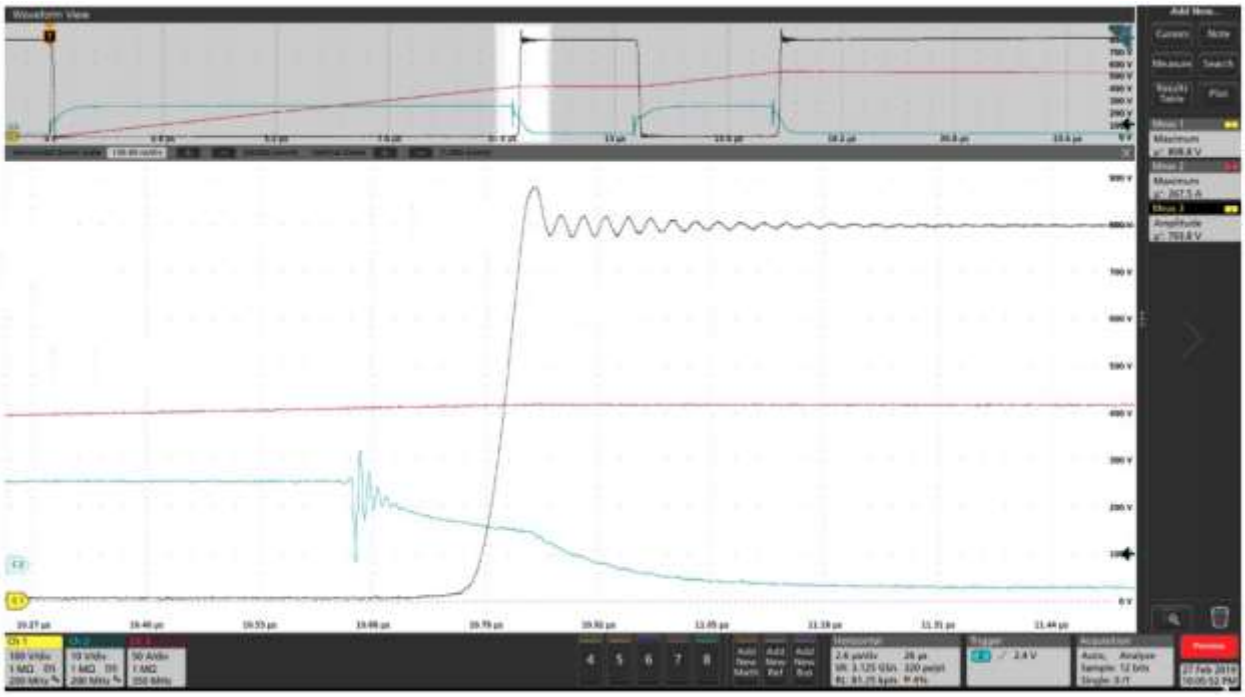

Figure 76 Phase A Double Pulse Test (Zoomed In)

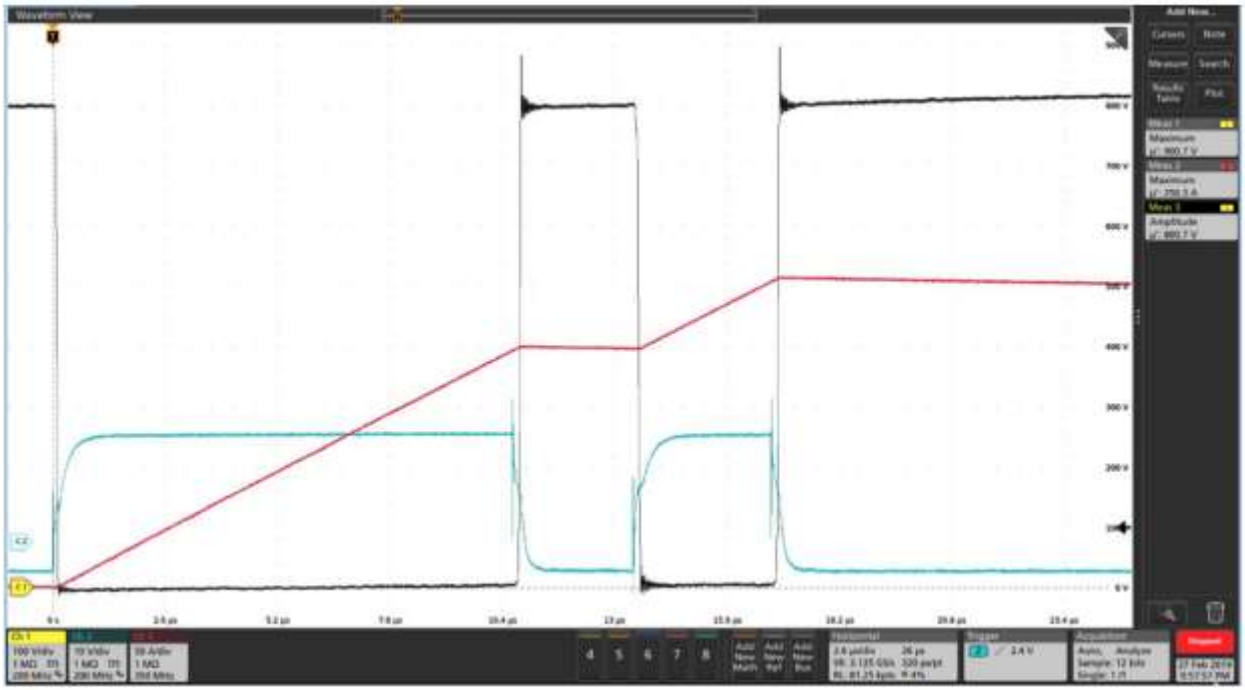

Figure 77 Phase B Double Pulse Test

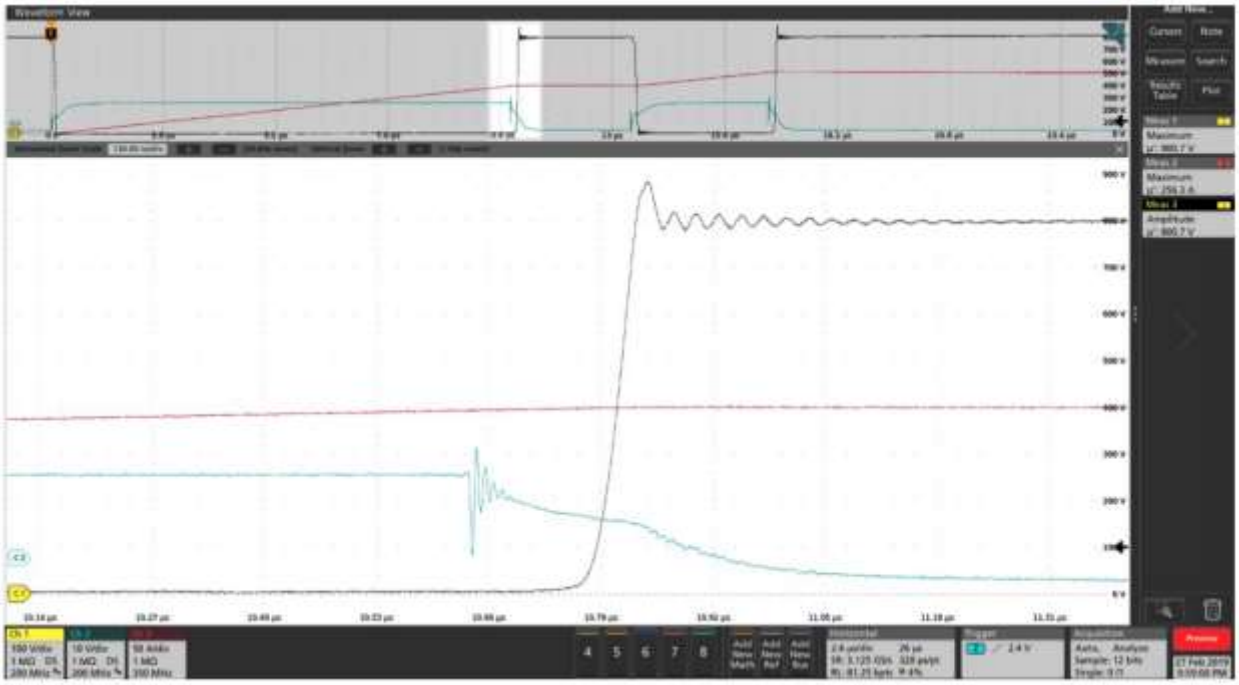

Figure 78 Phase B Double Pulse Test (Zoomed In)

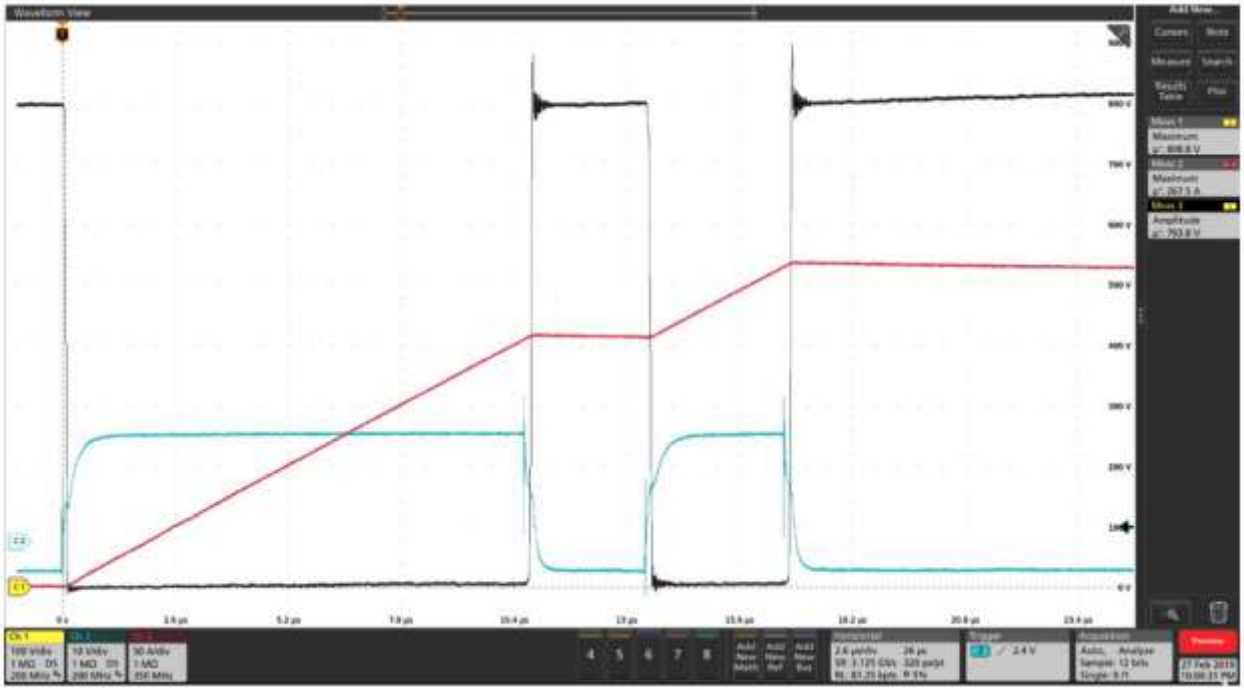

Figure 79 Phase C Double Pulse Test

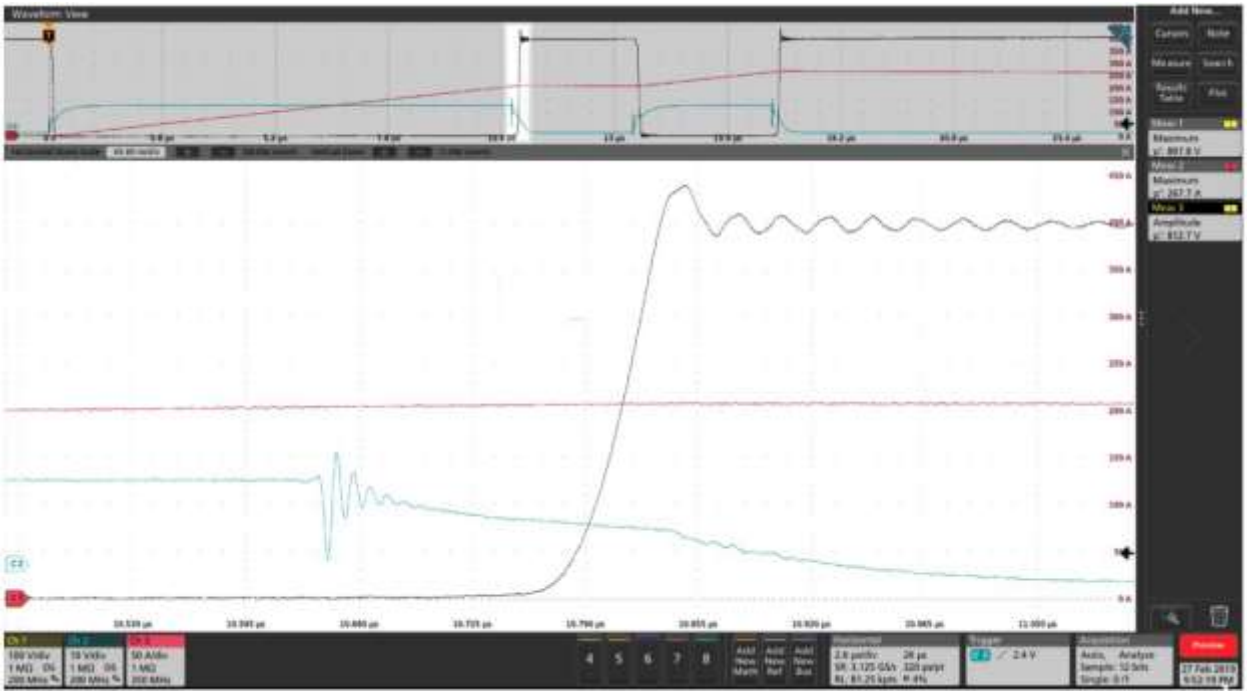

Figure 80 Phase C Double Pulse Test (Zoomed In)

Multiple pulse testing was also completed for each phase prior to 3 phase testing to show the ability of each phase of the inverter to withstand the full current and voltage required to achieve 150 kW.

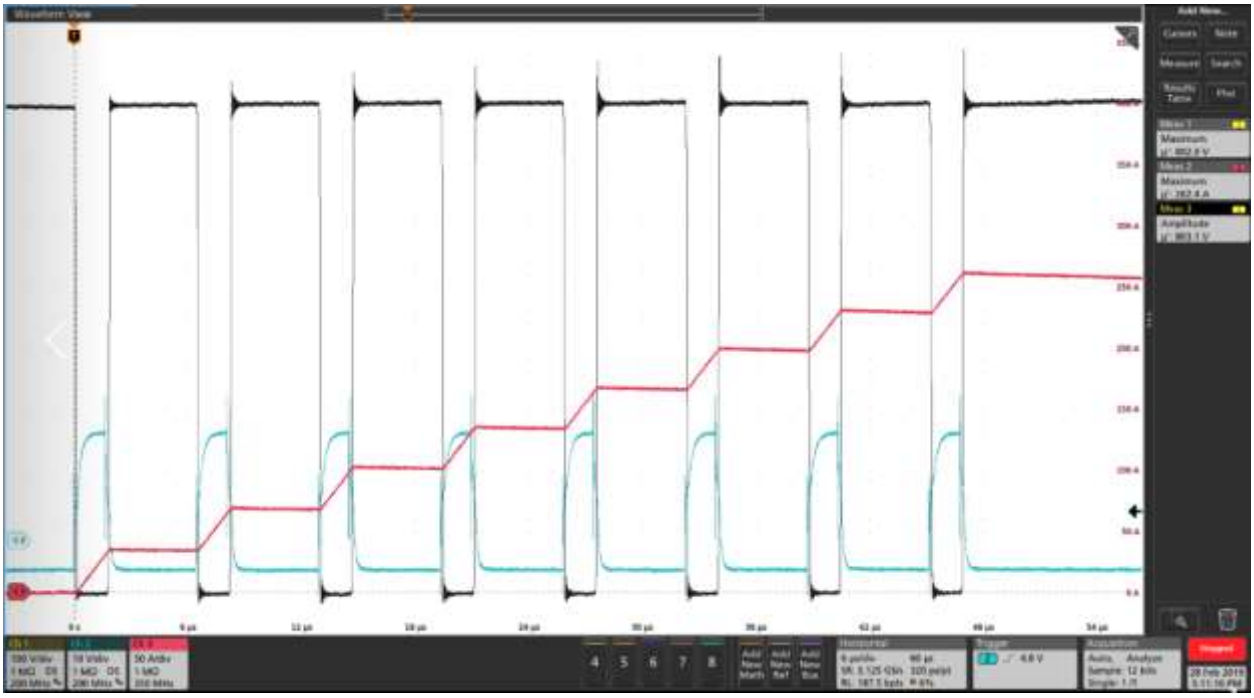

Figure 81 Phase A 8-Pulse Test

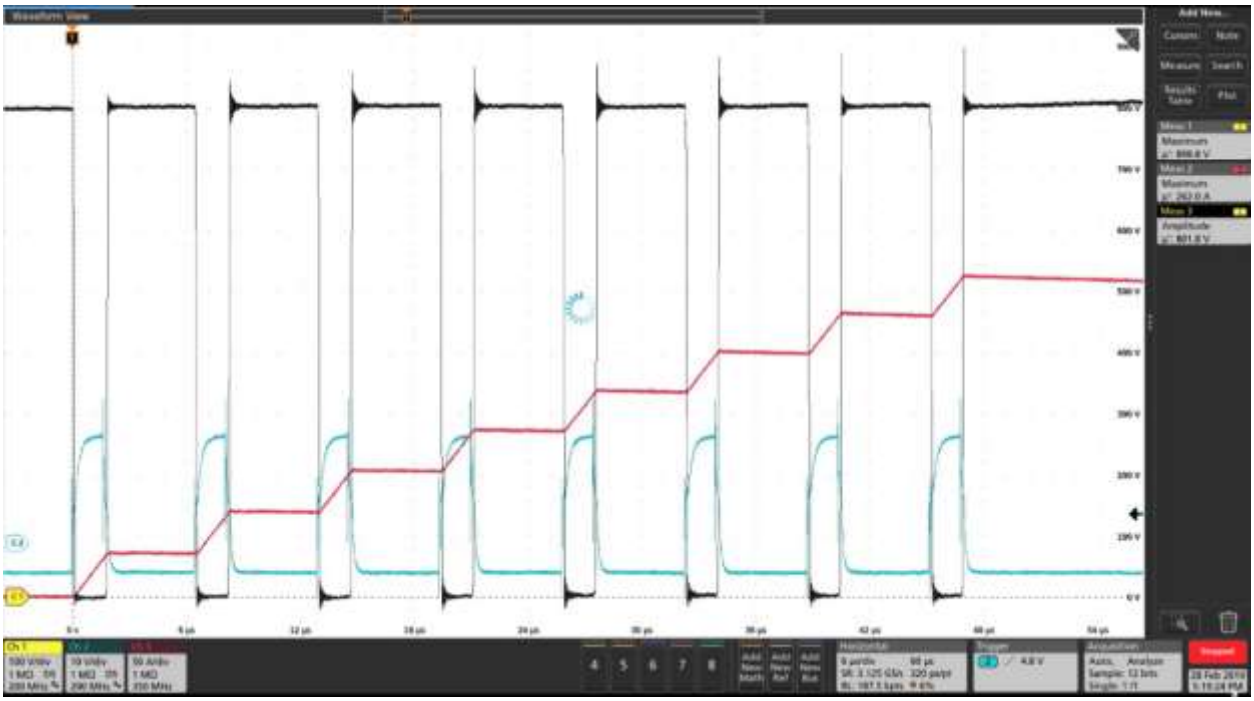

Figure 82 Phase B 8-Pulse Test

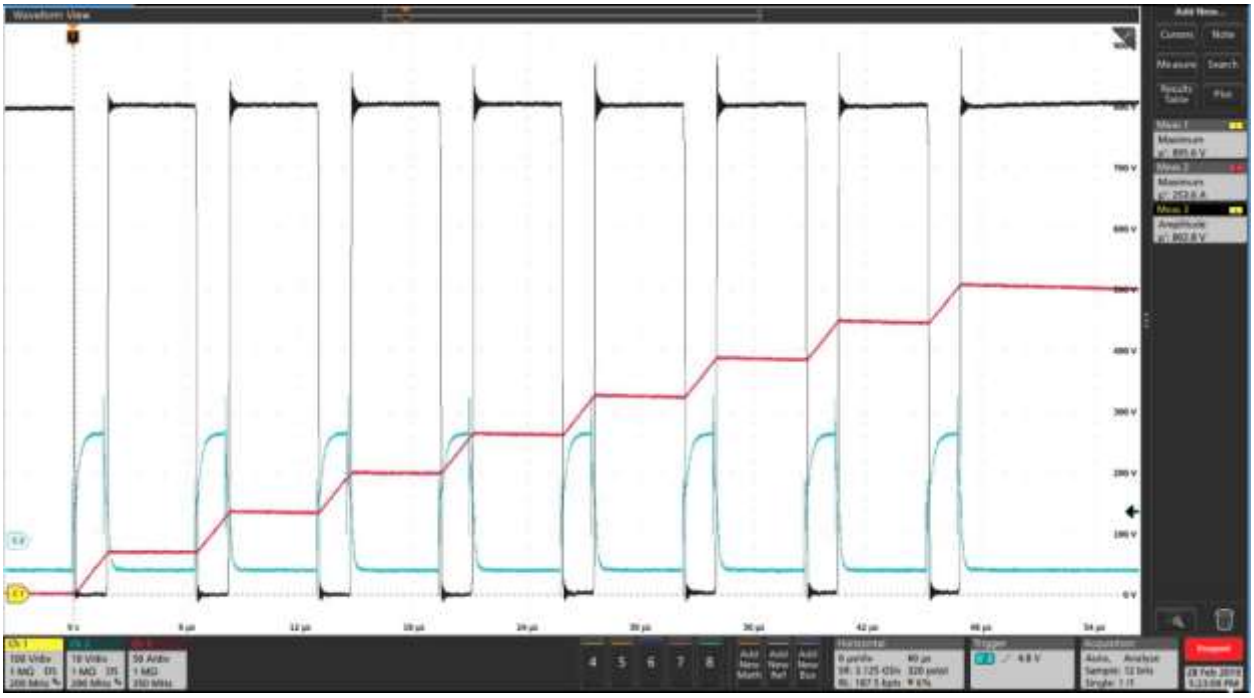

Figure 83 Phase C 8-Pulse Test

Several low-power 3-phase tests have been completed, but because of lack of access to a high-power test facility capable of providing 150 kW continuous through a DC supply, 3-phase high power testing has not been completed yet at the time of this writing. The previously presented tests show the ability of each phase to handle what the inverter would require of them when operating at 150 kW. These tests were able to be conducted without a 150 kW supply by only operating each phase for several switching periods at most while operating at full voltage and current. The last test performed demonstrates the ability of the inverter to produce a 3-phase sinusoidal output current.

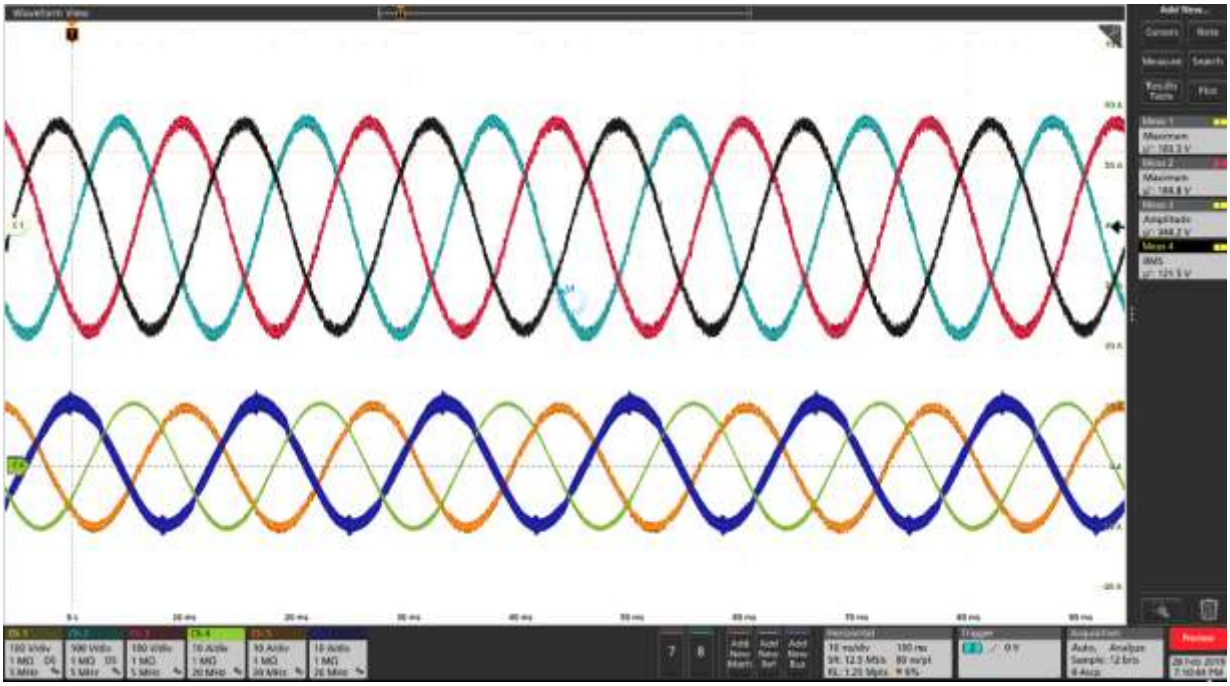

Figure 84 Successful 3-Phase Testing

4.4 References

[1] P. Tu, P. Wang, X. Hu, C. Qi, S. Yin and M. A. Zagrodnik, "Analytical evaluation of IGBT turn-on loss with double pulse testing," 2016 IEEE 11th Conference on Industrial Electronics and Applications (ICIEA), Hefei, 2016, pp. 963-968.

[2] S. S. Ahmad and G. Narayanan, "Double pulse test based switching characterization of SiC MOSFET," 2017 National Power Electronics Conference (NPEC), Pune, 2017, pp. 319-324.

CHAPTER 5

Conclusion and Future works

5.1 Conclusion

The main goal of this work was to build a 150 kW 25 kW/L DC-AC silicon-carbide based inverter system that is capable of operation while using a practical 90°C-105°C coolant temperature that is typically seen in the engine coolant loop on a hybrid electric vehicle. To accomplish this goal, several inverter topologies were reviewed and weighed against the goals of the project. After choosing the 2-level inverter due to its lower component number requirement, a power module was selected based on results gathered by experimentally finding the maximum power dissipation achievable by the module candidate and comparing that value to the power dissipation requirement of the system at full load that was found through simulation. Following power module selection, the minimum suitable electrical characteristics of the DC-link capacitors were calculated and the smallest volume capacitor bank that met the requirement was selected. Then, a PCB was designed to form the required bussing between the electrical components while minimizing overall system size. The PCB was analyzed in Ansys to maximize electrical performance through current density and parasitic simulations. The inverter along with its custom DSP-based control platform was assembled to allow the commencement of double pulse and multiple pulse testing. Lastly, successful 3-phase testing was completed to show the ability of the inverter to create a sinusoidal 3-phase output. The overall volume of the constructed inverter measures 1.35L, has a continuous power rating of 150 kW, and has an overall power density of 111 kW/L, which far surpasses the 25 kW/L target.

5.2 Future Works

Depending on the specific application that is targeted, it may be highly desirable to include a front-end AC-DC converter that connects to the DC-link of this converter. The AC side of the complete system would be used to rectify AC power generated from a motor within a hybrid electric vehicle into a stiff enough DC-link to support this inverter's operation. Through synchronizing the switching of the AC-DC converter and the DC-AC converter, the required DC-link capacitance could be significantly reduced, leading to an optimized complete AC-AC conversion unit.